

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

FERMAT INTERNATIONAL, INC.,
Patent Owner.

IPR2026-00358
U.S. Patent No. 11,886,750

PATENT OWNER'S PRELIMINARY RESPONSE

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PATENT OWNER'S EXHIBIT LIST

Exhibit No.	Description
2001	Declaration of Robert Bismuth dated July 16, 2026.
2002	Delaware Division of Corporations, Statement of Good Standing for Fermat International, Inc., dated July 7, 2026.
2003	Email chain between Manish Muthal, Ivo Bolsens and Carrie Chong of Xilinx and Robert Bismuth and Arnaud Blandin of Fermat, dated January 11-January 14, 2019.
2004	Fermat presentation to Xilinx.
2005	January 25, 2019 email from Robert Bismuth to various recipients at Fermat summarizing January 25, 2019 meeting with Xilinx.
2006	February 14, 2022 press release titled “ADM Completes Acquisition of Xilinx,” <i>available at</i> https://www.amd.com/en/newsroom/press-releases/2022-2-14-amd-completes-acquisition-of-xilinx.html ; <i>last accessed</i> July 6, 2026.

I. INTRODUCTION

The Petition does not establish a reasonable likelihood that any challenged claim is unpatentable. Sole independent claim 1 is challenged in ground 1A (Dalal-Ng) and ground 2A (Heil-Jun). In both cases, the Petition fails to demonstrate a reasonable likelihood that claim 1 is unpatentable.

For ground 1A, the Petition maps Dalal's data transfer fabric to both the claimed "storage interface component" and the claimed "plurality of communications channels." Pet., 43-44. Even if a single element in Dalal could map to two separate limitations of the '750 Patent, claim 1 requires that "the storage interface component *utilizes* a plurality of communications channels to transfer data" EX1001 ['750 Patent], cl. [1i]. The Petition attempts to overcome this problem by alleging Ng's memory interfaces are simultaneously both the claimed "storage interface components" and "plurality of communications channels." Pet., 44-45. But this mapping fails for the same reason as Dalal—the Petition fails to explain how those memory interfaces "*utilizes* a plurality of communication channels to transfer data" as required by the claims.

Because limitation [1i] is missing from both Dalal and Ng, the Petition relies on background knowledge of a POSITA to supply the missing limitation. Pet., 46. But Petitioners may not rely on background knowledge of a POSITA to supply limitations that are missing from the asserted references, and even if they could,

the support cited by the Petition at best demonstrate that storage interface components existed, not that storage interface components utilized a plurality of communications channels to transfer data in the manner required by the claims.

For ground 2A, the Petition relies exclusively on Heil as disclosing limitations [1a] and [1c]. Pet., 74-77, 81-83. But Heil does not disclose either limitation. For limitation [1a], the Petition's mapping does not explain how Heil supplies the claimed node interface for Heil's alleged router module, or how the alleged node interface is coupled to a claimed first tier compute node.

Accordingly, the Director should deny institution on the merits because the Petition fails to demonstrate a reasonable likelihood that any challenged claim is unpatentable.

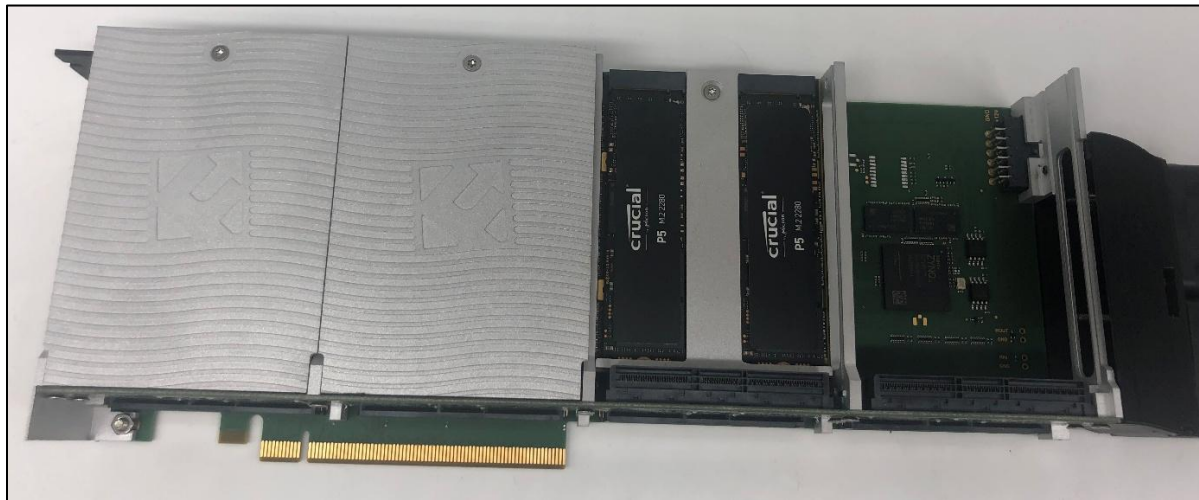
II. BACKGROUND

A. Patent Owner Fermat

Patent Owner Fermat International, Inc. ("Fermat") is a small company that operated in the U.S. and France manufacturing near memory high speed compute modules for servers that included flash-based storage and significant DRAM memory. Ex. 2001 [Bismuth Decl.], ¶ 2. Founded in 2016, at its largest, Fermat had approximately 10 employees. *Id.*

Fermat sold its storage computation solutions primarily to U.S.-based customers. Ex. 2001 [Bismuth Decl.], ¶ 6. The U.S.-based company Micron was

Fermat's largest customer. *Id.* A photograph of Fermat's commercialized module is shown below:



Id.

By the end of 2023, Fermat was faced with increased competition from major vendors like Petitioner who were adopting architecture covered by Fermat's issued U.S. patents. *Id.* Even though Fermat's products still held a performance advantage, the ability of major companies like Petitioner to sell to and support the customers Fermat was targeting was beyond Fermat's capability. *Id.* In other words, scaling Fermat was proving difficult due to market competition from large companies like Petitioner that had adopted Fermat's patented technology. *Id.* As a result, Patent Owner ceased operations in 2024 and filed a lawsuit for patent infringement against Petitioner in January 2026. *Id.*

B. The '750 Patent

1. Background of the Invention

The inventors of the '750 Patent recognized that that the volume of data available for computation was growing at a much greater rate than processor speed. With the advent of the “internet of things” in addition to the automation of almost all processes in the world (plus the increasing speed of the Internet for moving data), the rate of data collection is constantly accelerating and does not suffer from the slowing down that Moore’s Law produces for processors.

At the same time, storage densities had also increased to the point where data storage costs are not a significant factor. With the advent of massive SSD storage modules, data had become very energy efficient since data essentially uses zero energy unless it is actively being accessed. In reality, most data is not accessed very frequently, if at all.

No matter how fast a processor is, there are mass storage to memory transfers, memory to processor data transfers, memory to processor instruction transfers, results are transferred to memory, and, in some cases, results from memory are transferred to mass storage. All these steps take significant amounts of time and cannot be executed in parallel. So, total computation time is the total length of time taken to transfer and execute whatever computation per data element multiplied by the total number of data elements. The time taken for all this

movement of data and instructions vastly exceeds the time a processor spends actually executing computational instructions on data loaded into its registers.

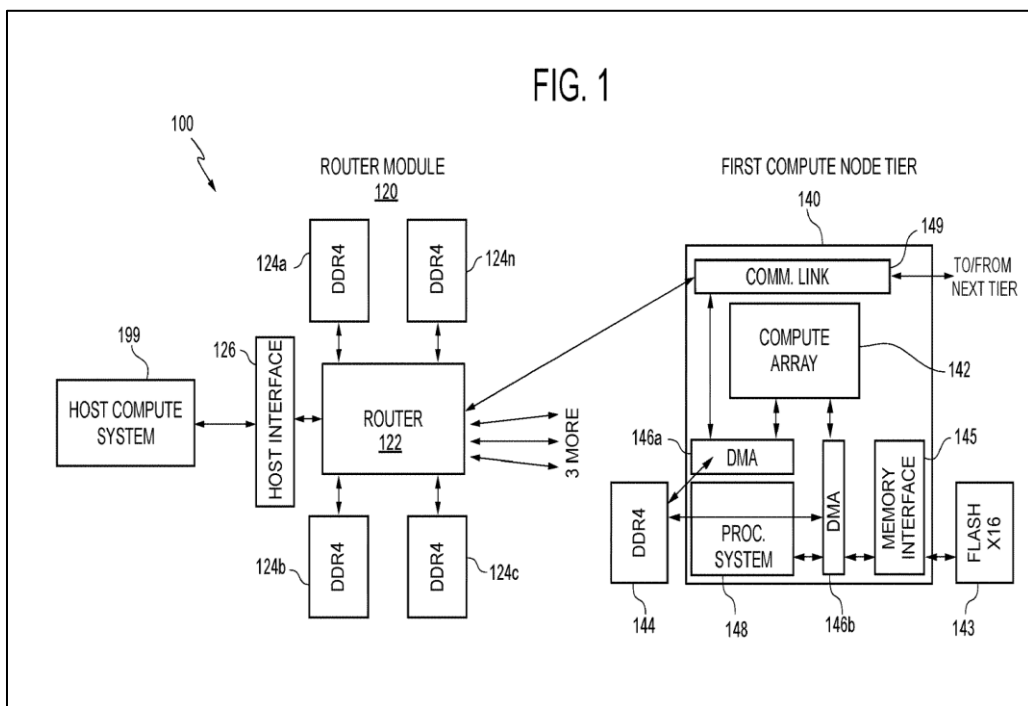
The inventors behind the Fermat architecture realized that by placing processors (any type of processors) extremely “close” to mass storage, these transfer times could be minimized and, in some cases, eliminated. The key was integrating processors with storage in the sense of providing a direct very high-speed connection between processors and storage with either the silicon of the processor pre-configured for the specific algorithm of interest or the processor linked by a dedicated separate high speed bus to high speed DRAM holding the algorithm. In this way, data could be streamed directly from mass storage to the processor, eliminating the need to first move it to DRAM or from DRAM to the processor, and, depending on the processor type, either eliminating or drastically speeding up instruction fetch times.

C. The '750 Patent

The '750 Patent reflects the problem identified by the inventors, explaining that “with the explosion of data available to such systems ... the sheer volume of available data to process is increasing faster than traditional hardware and software systems are able to evolve in order to process those data in a meaningful and efficient manner.” '750 Patent, 1:47-55. “As a practical matter, it will be appreciated that for as long as the rate at which new data become available for

processing continues to outpace the rate at which processing methodologies advance to accommodate the increased size of a given dataset, it will continue to take longer to solve bigger and more complex data processing problems.” *Id.*, 1:63-2:2. Accordingly, “there is a need for an improved system and method employing a distributed hardware architecture that facilitates high throughput data processing and analytics solutions for resource-intensive applications.” EX1001 [’750 Patent], 2:3-6.

To address this need, the ’750 Patent proposed “an architectural framework that may employ high performance data processing elements (compute nodes) coupled with massive data storage (a data store) in a unique configuration that minimizes or eliminates typical processor/network wait states, optimizes instruction fetch memory cycles, and analyzes data that are streamed from an attached or associated data store at the maximum rate at which the data can be accessed or streamed by the storage subsystem.... .” *Id.*, 7:5-13. Figure 1 (below) is a “functional block diagram illustrating one implementation of a data processing and analytics system for use in connection with a host compute system” *Id.*, 5:53-55:

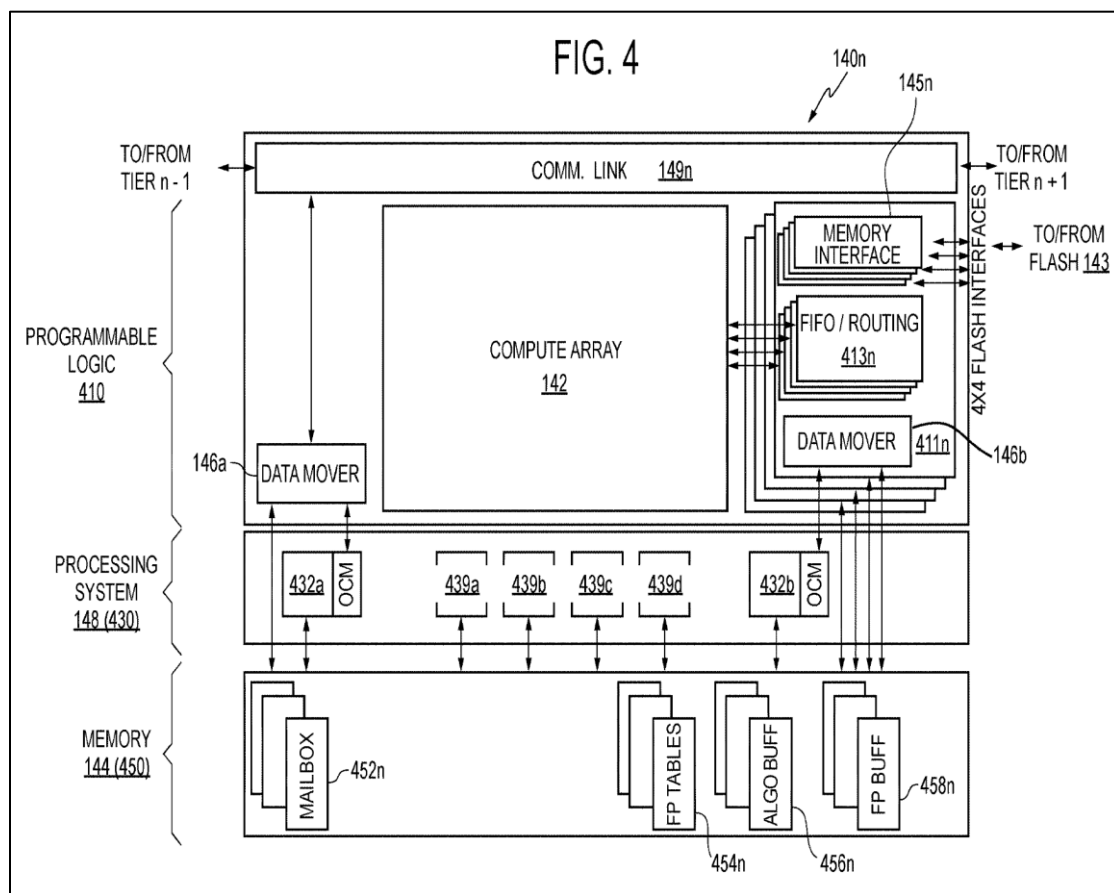


EX1001 [’750 Patent], Fig. 1.

As shown, Figure 1 comprises “a host compute system 199, a router module 120, and a compute node 140.” *Id.*, 8:25-27. “Host compute system 199 may generally be embodied in or comprise a computer server, a desktop or workstation 30 computer, a laptop or portable computer or tablet, or a combination of one or more of such components.” *Id.*, 8:28-31. “Router module 120 may generally comprise a router 122, one or more router memory components 124a, 124b, 124c, . . . 124n (‘router memory 124’) and a host interface 126.” *Id.*, 9:4-9. “[R]outer module 120 may also include one or more node interfaces [] such as network interface cards, wireless or inductive hardware components, or communications ports, jacks, or plugs, for instance, to enable router 122 to communicate with a

respective compute node 140... .” *Id.*, 9:7-13.

The compute nodes 140 are the data processing elements coupled to data stores to minimize wait states and optimize memory cycles. “[E]ach compute node 140 may generally comprise a compute array 142, a data store 143, a data store interface 145, node memory 144, one or more datamover apparatus (DMA) 146a and 146b (“DMAs 146”), and a processing system 148.” EX1001 [’750 Patent], 10:5-9. Figure 4 “is a functional block diagram illustrating components of an implementation of a compute node.” *Id.*, 5:64-67:



EX1001 [’750 Patent], Fig. 4.

The '750 Patent envisions the use of multiple compute nodes. The '750 Patent explains that each compute node “may be communicatively coupled, via communications link 149n to one or more additional compute nodes 140 connected in series at different successive tiers.” *Id.*, 14:59-63.

D. Claims of the '750 Patent

The '750 Patent has seven claims. Claim 1 is independent and claims 2-7 depend on claim 1. Because there is only one independent claim, the Petition may not be instituted unless the Petition demonstrates a reasonable likelihood that the Petitioner would prevail in proving claim 1 is unpatentable. 35 U.S.C. § 314(a). As discussed below, Petitioner fails to do so.

Similar to Figure 1, the claims of the '750 Patent address the problem identified by the inventors by claiming a data processing system comprising a routing module and multiple parallel first tier compute nodes coupled to one or more additional compute nodes in series. Claim 1 is reproduced below:

[1pre]	A data processing system operative in cooperation with a host compute system, the data processing system comprising:
[1a]	a router module comprising a host interface and a node interface, wherein the router module is communicatively coupled to the host compute system via the host interface; and

[1b]	multiple parallel first tier compute nodes coupled to one or more additional compute nodes in series, each compute node comprising:
[1c]	a communications link, wherein each first tier compute node is communicatively coupled to the node interface at the router module via the communications link, at different successive tiers, each compute node in a series being communicatively coupled, via its communications link to one or more additional compute nodes connected at different successive tiers;
[1d]	a data store comprising records associated with a data processing operation;
[1e]	a programmable logic component to execute the data processing operation in cooperation with the data store;
[1f]	a node memory comprising data and instructions to support operation of the programmable logic component in connection with the data processing operation and to facilitate data communications via the communications link;
[1g]	a data mover component to facilitate data communications between the programmable logic component and the node memory; and
[1h]	a storage interface component to facilitate data communications between

	the programmable logic component and the data store;
[1i]	wherein the storage interface component utilizes a plurality of communications channels to transfer data between the programmable logic component and the data store.

E. Related Proceedings

On January 13, 2026, Patent Owner asserted the '750 Patent, along with several related patents, in *Fermat International, Inc. v. Advanced Micro Devices, Inc.*, Civil Action No. 7-26-cv-00011 (W. D. Tex.). That case is currently proceeding in Texas.

On May 12, 2026, Petitioner filed this IPR, along with IPR2026-00359 and IPR2026-00360 challenging related U.S. Patent Nos. 11,550,512 and 12,271,636, respectively. All three IPRs are in the pre-institution phase.

III. LEVEL OF ORDINARY SKILL

The Petition proposes the following level of ordinary skill:

A person of ordinary skill in the art (“POSITA”) relating to the subject matter of the '750 patent as of the Critical Date would have had a bachelor’s degree in Computer Engineering, Electrical Engineering, Computer Science, or a comparable field and at least two years of experience related to computer architecture. AMD1003, ¶¶27–28. Additional experience could substitute for a formal degree or formal

training (and *vice versa*). *Id.*

Pet., 4. For purposes of this preliminary response, Patent Owner does not dispute Petitioner’s level of ordinary skill.

IV. CLAIM CONSTRUCTION

Petitioner identifies the claim term “programmable logic component” as a “logic component programmable by reconfiguring its internal hardware connections, such as an FPGA.” Pet., 5. For purposes of this preliminary response, Patent Owner does not believe any claim term needs to be construed. Patent Owner reserves the right to propose constructions if this IPR is instituted.

V. THE PETITION DOES NOT ESTABLISH A REASONABLE LIKELIHOOD THAT CLAIM 1 IS UNPATENTABLE

The Petition alleges four grounds:

ID	Claims	Prior Art Basis Under §103
1A	1–2, 5–9	Dalal-Ng
1B	3–4	Dalal-Ng-Raghava
2A	1–3, 5–8	Heil-Jun
2B	4, 9	Heil-Jun-Raghava

Pet., 1.

The ’750 Patent has only one independent claim (claim 1), and the Petition only challenges claim 1 in grounds 1A (Dalal-Ng) and 2A (Heil-Jun). This Petition may only be instituted if either Dalal-Ng or Heil-Jun demonstrates a reasonable likelihood that claim 1 is unpatentable. 35 U.S.C. § 314(a). Thus, for purposes of

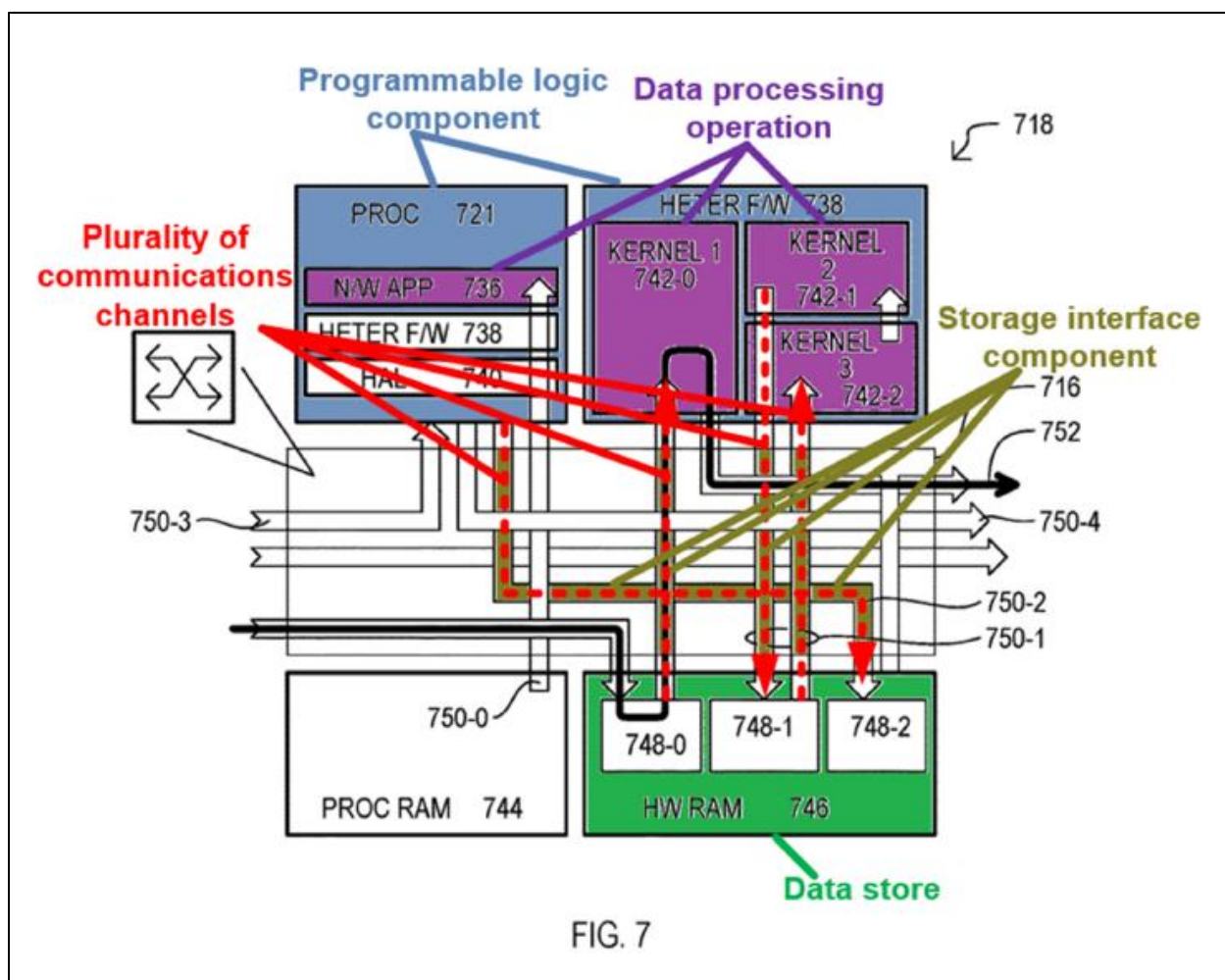
this POPR, Patent Owner analyzes only ground 1A claim 1 and ground 2A claim 1. Because neither Dalal-Ng nor Heil-Jun demonstrate a reasonable likelihood that claim 1 is unpatentable, institution must be denied.

A. The Dalal-Ng Combination Does Not Establish A Reasonable Likelihood That Claim 1 Is Unpatentable

The Dalal-Ng combination fails to demonstrate that claim 1 is unpatentable. For example, the Dalal-Ng combination does not establish the relationship expressly required by limitation [1i]: “wherein the storage interface component utilizes a plurality of communications channels to transfer data between the programmable logic component and the data store.” EX1001 [’750 Patent], cl. 1. The Petition identifies structures for the storage interface and for the channels, but never demonstrates that the alleged interface utilizes the alleged channels for the claimed transfer.

For Dalal, the Petition alleges path 750-0 through Dalal’s data transfer fabric 716 is the claimed “data mover” in limitation [1g]. Pet., 37 (“Dalal’s processing circuits (*programmable logic component*) access the first memory (*node memory*) through the data transfer fabric via the path 750-0 (*data mover component*) such that path 750-0 facilitates *data communications* between these components.”) (emphasis in original). The Petition simultaneously alleges data transfer paths through Dalal’s data transfer fabric 716 are the claimed “storage interface

component” in limitation [1h]. Pet., 39 (“To *facilitate* these *data communications*, the computing element includes data transfer paths (*storage interface component*) through Dalal’s data transfer fabric 716 that connect the *programmable logic component* to the *data store*.”) (emphasis in original). For limitation [1i], the Petition identifies paths through that same data transfer fabric 716 as the claimed “plurality of communications channels”:



Pet., 43. Thus, the Petition’s annotated Figure 7 labels paths through data transfer fabric 716 as both the claimed “plurality of communications channels” and

simultaneously as the claimed “storage interface component.” Pet., 43–44.

The Petition asserts that Figure 7’s data transfer fabric 716 contains “at least four” paths between processing circuits 721 and second memory 746, but the Petition body does not identify four numbered routes. Pet., 43. Petitioner’s expert, Dr. Alpert, names only 750-1 and 750-2. EX1003 [Alpert Decl.], ¶99. Dalal describes 750-1 as a “kernel-to-kernel” connection through second-memory spaces and 750-2 as a “processor-to-kernel” connection through a second-memory space. EX1004 [Dalal], [0081].

Whether either path connects the structures Petitioner identifies as the programmable logic component and the data store depends on how Petitioner applies its collective mapping of processing circuits 721 and framework 738 as the programmable logic component. The Petition never explains how those paths fit that mapping when it counts channels. Pet., 28–30, 43–44; EX1003 [Alpert Decl.], ¶¶75–80, 99; EX1004 [Dalal], [0081].

Claim 1 requires a relationship between the two: the storage interface component “utilizes” the communications channels. Simply applying both labels to paths in fabric 716 does not show that the alleged interface utilizes the alleged channels. The Petition does not identify what within fabric 716 performs the storage interface function, which paths it uses as channels, or how it uses those paths for the claimed transfer. Even if the interface and channels could be mapped

to the same component as the Petition attempts, the Petition still must show that the alleged interface utilizes the alleged channels. It does not. EX1001 [’750 Patent], cl. 1; Pet., 39–44.

Moreover, the Petition fails to establish that the alleged storage interface component “*utilizes* a plurality of communications channels” as required by Claim 1. Pet., 43–44. The Petition states that a POSITA would implement Dalal’s computing elements with a “dedicated storage interface component” comprising circuitry configured with one or more memory protocols of the data store. Pet., 41–42; EX1003 ¶95. Dedicated circuitry and protocol support do not show the utilization required by the claim. The Petition never connects that circuitry to the paths it separately identifies as communications channels.

The Petition next points to two read operations involving Dalal’s memory spaces 848-0 and 848-1, associated with different computing elements within an HWA module, as the alleged plurality of communications channels. Pet., 44–45 (citing EX1003 [Alpert Decl.] ¶100; EX1004 [Dalal] [0094]). But the Petition does not identify a claimed storage interface component—within either computing element or at the module level—that utilizes both read operations as the asserted plurality of communications channels. That is, the Petition alleges that the two read operations involving Dalal’s memory spaces 848-0 and 848-1 are the claimed “plurality of communications channels” but then does not show that a single

“storage interface component” utilizes both read operations as channels. Dalal Figure 8 therefore does not establish [1i].

Because the Petition fails to establish [1i] through Dalal, it next alleges Ng discloses the limitation. Pet., 45–46. For Ng, the Petition alleges Ng’s first and second memory interfaces 312 in Ng Fig. 3 collectively constitute the claimed “storage interface component” and, simultaneously, individually constitute the claimed “plurality of communications channels.” Pet., 45 (“DNC also incorporates Ng’s express teaching of memory interfaces (*storage interface component*) including a first memory interface used to read from the RAM and a second memory interface used to read from and write to the RAM (*plurality of communications channels*).”).

Ng presents the same problem as Dalal. The Petition simultaneously maps Ng’s memory interfaces 312 collectively to the claimed storage interface component and individually to the claimed plurality of communications channels. Pet., 45-46. Claim 1 requires the mapped storage interface component to “utilize” the channels. EX1001 [’750 Patent], cl. 1. The Petition never explains how the pair of memory interfaces 312, which it treats as the storage interface component, utilizes the individual interfaces as channels in the proposed Dalal-Ng combination. Pet., 45–46. The Petition states only that Ng’s memory interfaces 312 “would have utilized” multiple channels without identifying how the pair utilizes

those interfaces as channels. Pet., 45. Dr. Alpert’s assertion that two of Ng’s memory interfaces “represent” channels and that the component “utilizes” them merely states the conclusion; it does not provide an explanation as to how these memory interfaces perform the claimed functionality. EX1003 [Alpert Decl.] ¶102. Thus, Ng fails to cure the same underlying defect.

Having failed to establish a reasonable likelihood that limitation [1i] is taught or suggested by Dalal or Ng, the Petition alleges a POSITA’s general knowledge to supply the missing limitation. Pet., 46 (“a POSITA would have understood that it was well known for *a storage interface component* to include a *plurality of communications channels* in a hardware accelerator.”) (emphasis in Petition). That attempt to use general knowledge to provide a limitation missing from the asserted references is impermissible under 37 C.F.R. § 42.104(b)(4) and the Acting Director’s July 31, 2025 Memorandum Re: Enforcement and Non-Waiver of 37 C.F.R. §42.104(B)(4) and Permissible Uses of General Knowledge In Inter Partes Reviews.

Even apart from that deficiency, the extrinsic materials cited by the Petition to demonstrate a POSITA’s general knowledge do not supply the missing mapping. Pet., 46. EX1028 [Jung], EX1043 [Li], and EX1003 [Alpert Decl.] ¶103 show, at most, that multichannel storage interfaces existed. They do not show that a POSITA would have understood that the storage interface component in

Petitioner's Dalal-Ng combination utilized the particular paths or interfaces identified as channels. Nor does the Petition separately map [1i] to Jung or Li or articulate a modification using particular structures from either reference. And Jung and Li are not part of any ground in the Petition. Thus, Petitioner's general-knowledge showing does not establish limitation [1i].

Because neither Dalal nor Ng teach or suggest limitation [1i], ground 1A does not demonstrate a reasonable likelihood that any challenged claim is unpatentable.

B. The Heil-Jun Combination Does Not Establish A Reasonable Likelihood That Claim 1 Is Unpatentable

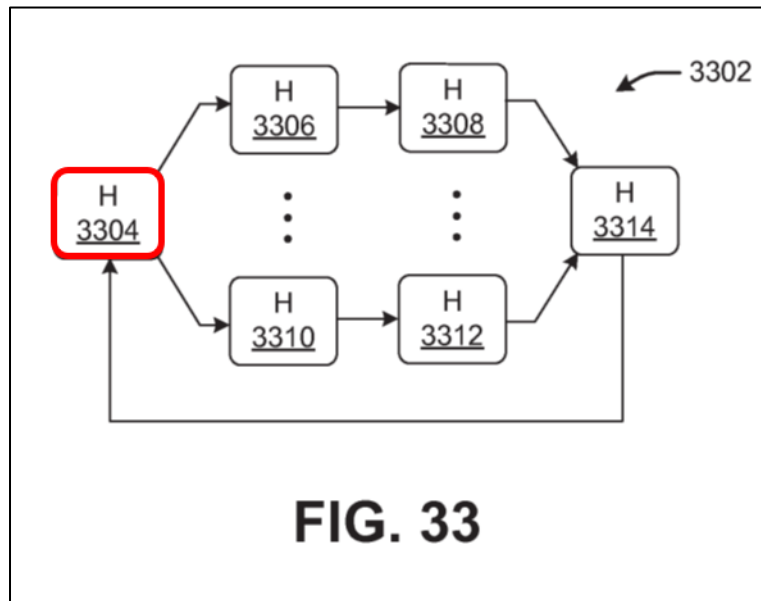
The Heil-Jun combination fails to establish the router-side node-interface-to-link relationship required by limitations [1a] and [1c]. As discussed below, Heil-Jun fails at least because the Petition does not establish that Heil's communications link is coupled to the router module's node interface, as limitations [1a] and [1c] require.

1. Limitation [1a]

Limitation [1a] requires "a router module comprising a host interface and a node interface, wherein the router module is communicatively coupled to the host compute system via the host interface." EX1001 ['750 Patent], cl. 1. The Petition relies on Heil for this limitation. Pet., 74-77. Heil Figure 33 shows Heil's system-

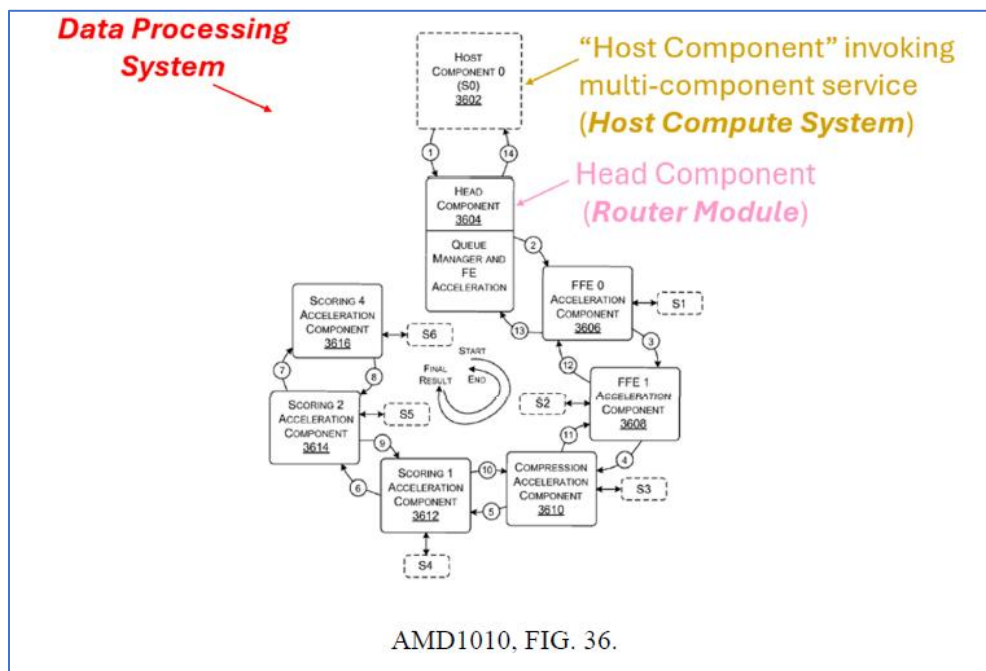
level topology: head component 3304 branches to first-tier acceleration

components and then to components at successive tiers:



EX1010 [Heil], Fig. 33 (annotated by Patent Owner).

The Petition similarly alleges Heil Fig. 36's head component 3604 is the claimed router module:



Pet., 75 (annotating EX1010 [Heil], Fig. 36).

But Heil Figures 33 and 36 depict head component 3304 and 3604 only as a single component and do not show the head component’s internal interfaces. The Petition does not identify in Figures 33 or 36 which structure within Heil’s head component Petitioner relies on as the node interface under [1a]. Pet., 76-77 (alleging that “Heil teaches or renders obvious that the head component (*router module*) includes a *node interface* to communicate with the server unit components” (emphasis in original) but failing to identify a node interface in Figures 33 or 36).

The Petition alleges that the claimed node interface is satisfied by Heil’s transport component 2530, which, in “one implementation” “may provide a

register interface to establish connections between nodes.” Pet., 77 (quoting EX1010 [Heil], [0181]); EX1003 ¶160. But Heil [0181] discusses the embodiments at Figures 25 and 29. EX1010 [Heil], [0181]. The Petition does not explain how the [0181] register-interface disclosure supplies the claimed node interface for Fig. 33 or 36’s head component 3304/3604, or how the first-tier communications links shown in Figures 33 and 36 are coupled to that alleged node interface.

The Petition also cites the ’750 Patent’s statement that node interfaces were “generally known in the art” as support for its allegations that “Heil’s head component (*router module*) includes a *node interface*.” Pet., 76-77 (citing EX1001 [’750 Patent], 9:7–14) (emphasis in original). But even if node interfaces were known in the art, that does not mean that Heil’s head component 3304 or 3604 includes a node interface. To the extent Petitioner relies on a POSITA’s background knowledge to supply the node interface itself, that reliance is impermissible under 37 C.F.R. § 42.104(b)(4), which does not permit a petition to use background knowledge of a POSITA to supply a claim limitation missing from the asserted prior art references.

2. Limitation [1c]

The Petition also fails to demonstrate that Heil teaches or suggests limitation [1c]. Limitation [1c] requires that “each first tier compute node is communicatively

coupled to the node interface at the router module via the communications link,” and separately recites additional compute nodes at successive tiers. For limitation [1c], the Petition alleges that Heil’s server unit components each contain a “transport component” with a “register interface to establish connections between nodes” as discussed for Heil Fig. 25. Pet., 82 (quoting EX1010 [Heil], [0181]). The Petition does not establish that Heil’s first-tier communications links are coupled to the particular register interface from Fig. 25. Petitioner alleges is the claimed node interface. Pet., 81-83 (discussing Heil Fig. 33 and alleging “the head component 3304 (*router module* using a *node interface*) is *communicatively coupled* to the acceleration components 3406 [sic] and 3410 [sic] of the *first tier* server unit components (*compute nodes*) directly.” (emphasis in original)). Figure 33 thus shows accelerator-level connectivity, but does not itself establish that the “first tier compute node is communicatively coupled to the node interface at the router module via the communications link” as required by [1c]. EX1001 [’750 Patent], cl. 1.

Petitioner alleges that Heil’s transport component 2530 “functions as part of a communications link.” Pet., 82; EX1003 [Alpert Decl.], ¶172. The Petition’s cited sections allege Heil’s transport component 2530 and its register interface as the alleged node interface for [1a], and the dedicated first-tier accelerator links and transport component 2530 as part of the communications link structure for [1c], but

they do not establish the claimed connection between them. At Pet. 81, the Petition labels Heil's head component 3304 a "router module using a node interface" and then points to the links shown in Figure 33. Pet., 81. But the links in Heil Figure 33 are only connected to Heil's head component 3304 as a whole; Heil does not identify or connect them to the particular register interface Petitioner relies on as the alleged node interface. The parenthetical therefore assumes, rather than establishes, that Heil's head component 3304 contains a node interface that is communicatively coupled to the compute node as required by limitation [1c].

Petitioner alleges Heil's server unit containing a local host and an acceleration component is the claimed compute node. Pet. 77–80; EX1003 [Alpert Decl.], ¶140. The Petition relies on Heil's local host's main memory for the claimed node memory and on Heil's host-to-accelerator PCIe/DMA path for the claimed data mover. Pet. 90–95 & n.7; EX1003 [Alpert Decl.], ¶¶181–190 & n.3. Heil Figure 33 depicts acceleration components—3306 and 3310 on parallel paths, followed by 3308 and 3312 at a successive tier. EX1010 [Heil] [0203], Fig. 33. The Petition describes the alleged compute nodes (Heil's server-unit nodes) as coupled "via their respective acceleration components." Pet. 80; EX1003 [Alpert Decl.] ¶¶162, 165. Even assuming, without conceding, that this accelerator-level arrangement establishes the topology required by limitation [1b] (i.e., "multiple parallel first tier compute nodes coupled to one or more additional compute nodes

in series, each compute node”), limitation [1c] separately requires “each first-tier compute node is communicatively coupled to the node interface at the router module via its communications link.” Figure 33 does not establish that router module-side connection (i.e., the connection at the node interface), and the Petition does not allege limitation [1c] is supplied by Jun.

Petitioner’s reliance on the ’750 Patent’s statement that node interfaces were “generally known in the art” does not supply the missing mapping. Pet., 76-77. In particular, it does not identify how the first-tier links connect to the specific alleged node interface in Heil or otherwise establish the claimed coupling. *Id.* Heil [0181] states that transport component 2530 “may provide a register interface to establish connections between nodes” and that software may allocate those connections before 2530 can transmit or receive. EX1010 [Heil] [0181]. The Petition later characterizes the same disclosure as host-managed “setup information.” Pet., 93; EX1003 [Alpert Decl.] ¶186. Heil separately describes transmission and reception through connection tables, packet-processing component 2904, switch 2532, the network, and the remote transport endpoint. EX1010 [Heil] [0181]–[0186], Fig. 29. If Heil’s register interface were the claimed node interface, the Petition does not show how the dedicated first-tier links and downstream transport components connect to it. If Petitioner instead relies on head-side transport component 2530 as a whole as the node interface, the Petition still does not establish that the first-tier

links shown in Figure 33 couple to 2530 rather than merely to head component 3304 at an unspecified point. Either way, the Petition does not establish the interface-to-link relationship required by [1c].

Thus, Heil-Jun fails at least because the Petition does not establish that each first-tier compute node's communications link is coupled to the router module's node interface, as limitations [1a] and [1c] require. Heil Figure 33's topology, the dedicated accelerator links, the transport components, and Jun's storage subsystem do not supply the claimed connection. The Petition therefore has not shown a reasonable likelihood that Claim 1 is unpatentable.

VI. CONCLUSION

For the foregoing reasons, the Petition fails to demonstrate a reasonable likelihood that the single independent claim 1 is unpatentable. Thus, institution must be denied.

Dated: August 19, 2026

Respectfully submitted,

By: / Stephen McBride /
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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(b)(1), the undersigned certifies that this Patent Owner Preliminary Response complies with the word limitation of that section because it contains 4,710 words as calculated by Microsoft Word.

Dated: August 19, 2026

Respectfully Submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE was served electronically via email on August 19, 2026, on the following counsel of record for Petitioners:

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