

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

FERMAT INTERNATIONAL INC.,
Patent Owner.

Case IPR2026-00358
U.S. Patent No. 11,886,750

**PETITIONER'S OPPOSITION TO PATENT OWNER'S REQUEST FOR
DISCRETIONARY DENIAL OF INSTITUTION**

TABLE OF CONTENTS

I.	INTRODUCTION.....	1
II.	ARGUMENT	2
A.	Referral and Institution Will Promote Predictable Patent Rights	2
1.	This Challenge Is Early in the '750 patent's Term and Years Before Expectations of Validity Could Vest	2
2.	Meetings with Xilinx Before the '750 Patent Was Filed Did Not Create Settled Expectations	2
3.	Fermat Undercut Any Claim to Settled Expectations by Concealing Its Patent Filings from Xilinx and Withholding Known Prior Art from the Office	5
B.	Institution Is Warranted to Cure Material Examination Errors Compounded by Fermat's Withholding of Known Prior Art	6
C.	Referral and Institution Will Conserve Resources and Make This Proceeding a True Alternative to District Court Litigation	10
1.	The Advanced Timeline of This Proceeding Ensures Institution Will Conserve Resources and Prevent Needless Discovery.....	10
2.	Overlap with the District Court Proceeding Is Minimized Because AMD's Stipulation Activates Immediately Upon Institution	12
3.	Baseless Speculation That AMD Might Take Inconsistent Claim Construction Positions Should Be Rejected	14
D.	Institution Protects the Critical United States Semiconductor Industry from Disruption	14
E.	The Petition's Grounds 1A–2B Present a Strong Challenge That Fermat Fails to Meaningfully Rebut.....	17
III.	CONCLUSION	20

LIST OF EXHIBITS

AMD1001	U.S. Patent No. 11,886,750 to Bismuth et al. (“the ’750 patent”)
AMD1002	Excerpts from the Prosecution History of the ’750 Patent (“the Prosecution History”)
AMD1003	Declaration of Dr. Donald Alpert
AMD1004	U.S. Publication No. 2019/0109793 (“Dalal”)
AMD1005	U.S. Publication No. 2019/0114538 (“Ng”)
AMD1006	U.S. Publication No. 2019/0108145 (“Raghava”)
AMD1007	[RESERVED]
AMD1008	U.S. Patent No. 9,043,526 (“Freking”)
AMD1009	U.S. Publication No. 2015/0301900 (“Whitehead”)
AMD1010	U.S. Publication No. 2016/0306668 (“Heil”)
AMD1011	Jun et al. “BlueDBM: An Appliance for Big Data Analytics” ACM (June 13, 2015) (“Jun”)
AMD1012	Liu et al. “BlueFlash : a reconfigurable flash controller for BlueDBM” Massachusetts Institute of Technology (2014) (“Liu”)
AMD1013	Declaration of June Ann Munford
AMD1014	Putnam et al. “A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services” Microsoft, (2014)

AMD1015	Vipin et al. “FPGA Dynamic and Partial Reconfiguration: A Survey of Architectures, Methods, and Applications” ACM Comput. Surv. Vol. 51, No. 4, Article 72 (July 2018)
AMD1016	[RESERVED]
AMD1017	[RESERVED]
AMD1018	Verma et al. “PCIe BUS: A State-of-the-Art-Review” (2017)
AMD1019	[RESERVED]
AMD1020	U.S. Patent No. 11,169,727 (“Doucette”)
AMD1021	U.S. Patent No. 10,802,995 (“Singh”)
AMD1022	Park et al. “PFFS: A Scalable Flash Memory File System for the Hybrid Architecture of Phase-change RAM and NAND Flash” (2008)
AMD1023	Prasad et al. “Design and Verification of Phy Interface for PCIe Gen 3.0 and USB Gen 3.1 Using UVM Methodology” (2017)
AMD1024	U.S. Patent No. 11,055,252 (“Constantinides”)
AMD1025	“AXI Central Direct Memory Access v4.1: LogiCORE IP Product Guide” (April 4, 2018)
AMD1026	“PCI Express Base Specification Revision 1.0” (April 29, 2002)
AMD1027	IEEE “IEEE Standard for In-System Configuration of Programmable Devices” IEEE Std 1532™ (2002)
AMD1028	U.S. Patent No. 10,831,376 (“Jung”)
AMD1029	Jung et al. “HIOS: A Host Interface I/O Scheduler for Solid State Disks” (2014)

AMD1030	IEEE “The Authoritative dictionary of IEEE Standards Terms, Seventh Edition” (2000)
AMD1031	U.S. Patent No. 9,152,592 (“Galles”)
AMD1032	McCarthy et al. “Visualizing the Five-dimensional Torus Network of the IBM Blue Gene/Q” (2014)
AMD1033	“Serial ATA: High Speed Serialized AT Attachment” Revision 1.0a (January 7, 2003)
AMD1034	U.S. Patent No. 6,711,701 (“Roohparvar”)
AMD1035	U.S. Publication No. 2013/0318285 (“Pignatelli”)
AMD1036	U.S. Patent No. 9,678,842 (“Zhang”)
AMD1037	Ousterhout et al. “The Case for RAMClouds: Scalable High-Performance Storage Entirely in DRAM” SIGOPS Operating Systems Review, Vol. 43, No. 4, December 2009, pp. 92-105.
AMD1038	Kang et al. “Performance Trade-Offs in Using NVRAM Write Buffer for Flash Memory-Based Storage Devices” IEEE Transactions on Computers, Vol. 58, No. 6, June 2009, pp. 744-758.
AMD1039	Zazo et al. “A PCIe DMA engine to support the virtualization of 40 Gbps FPGA-accelerated network appliances” 2015 International Conference on ReConFigurable Computing and FPGAs (ReConFig) (2015).
AMD1040	[RESERVED]
AMD1041	[RESERVED]
AMD1042	[RESERVED]
AMD1043	U.S. Publication No. 2020/0233588 (“Li”)

AMD1044	Voluntary Search Disclosure Declaration of Kenneth Darby
AMD1045	[RESERVED]
AMD1046	U.S. Patent No. 8,527,949 (“Pleis”)
AMD1047	Toulson et al. “Fast and Effective Embedded Systems Design: Applying the ARM mbed. 2nd ed.” Newnes (2017)
AMD1048	[RESERVED]
AMD1049	June 18, 2026 Stipulation
AMD1050	“Samsung Electronics Unveils Xilinx-Based SmartSSD Solution,” <i>available at</i> https://web.archive.org/web/20191016154347/https://forums.xilinx.com/t5/Xilinx-Xclusive-Blog/Samsung-Electronics-Unveils-Xilinx-Based-SmartSSD-Solution/ba-p/902137
AMD1051	Mehra, “Introducing Samsung SmartSSD: From Devices to Subsystems,” <i>available at</i> https://vimeo.com/showcase/7710614?video=307422994
AMD1052	Scheduling Order in <i>Fermat International, Inc., v. Advanced Micro Devices, Inc.</i> , 7-26-cv-00011 (WDTX) (Aug. 9, 2026)
AMD1053	Fermat, A New Generation of Computing Architecture: designed for Big Data Analytics & AI, <i>available at</i> https://fermatinternational.com/
AMD1054	LinkedIn, Fermat, <i>available at</i> https://www.linkedin.com/company/sasfermat
AMD1055	The UPS Store Midtown, <i>available at</i> https://locations.theupsstore.com/ca/palo-alto/2625-middlefield-rd

AMD1056	Zynq-7000 SoC Data Sheet: Overview, DS190 (v1.11.1) (July 2, 2018)
AMD1057	Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics, DS922 (v1.13) (August 1, 2018)
AMD1058	Job Opening: Senior Algorithm Software Engineer, <i>available at</i> https://fermatinternational.com/senior-algorithm-software-engineer/
AMD1059	Job Opening: Software Engineer, <i>available at</i> https://fermatinternational.com/fermat-software-engineer/
AMD1060	Job Opening: Senior System Software Engineer, <i>available at</i> https://fermatinternational.com/fermat-senior-system-software-engineer/
AMD1061	“Samsung Debuts Semiconductor Innovations at Samsung Tech Day that Maximize Data Center Efficiencies and Enable AI, Enterprise and Emerging Technologies,” <i>available at</i> https://web.archive.org/web/20190203012857/https://news.samsung.com/global/samsung-debuts-semiconductor-innovations-at-samsung-tech-day-that-maximize-data-center-efficiencies-and-enable-ai-enterprise-and-emerging-technologies
AMD1062	Complaint in <i>Fermat International, Inc., v. Advanced Micro Devices, Inc.</i> , 7-26-cv-00011 (WDTX) (Jan. 13, 2026)
AMD1063	Environmental Performance Indicators, <i>available at</i> https://www.amd.com/en/corporate/corporate-responsibility/cr-data-tables.html
AMD1064	How many employees work at AMD?, <i>available at</i> https://www.reveliolabs.com/companies/amd/employees
AMD1065	AMD Instinct™ MI200 Series Accelerators, <i>available at</i> https://www.amd.com/en/products/accelerators/instinct/mi200.html

AMD1066	New AMD Instinct™ MI200 Series Accelerators Bring Leadership HPC and AI Performance to Power Exascale Systems and More, <i>available at</i> https://ir.amd.com/news-events/press-releases/detail/1032/new-amd-instinct-mi200-series-accelerators-bring-leadership-hpc-and-ai-performance-to-power-exascale-systems-and-more
AMD1067	Frontier: Direction of Discovery, <i>available at</i> https://www.olcf.ornl.gov/frontier/
AMD1068	International Publication No. WO2020/163025 (“Bismuth”)
AMD1069	United States Securities and Exchange Commission, Form 10-K, <i>available at</i> https://www.sec.gov/Archives/edgar/data/2488/00000024882400012/amd-20231230.htm
AMD1070	Chapter 900 Prior Art, Classification, and Search (E9R-07.2022, Feb. 2023)
AMD1071	AMD takes the wraps off its Instinct MI455X AI accelerator — CDNA 5 and Helios rack-scale architecture combine to take the fight to Nvidia in the data center, <i>available at</i> https://www.tomshardware.com/pc-components/gpus/amd-takes-the-wraps-off-its-instinct-mi455x-ai-accelerator-cdna-5-and-helios-rack-scale-architecture-combine-to-take-the-fight-to-nvidia-in-the-data-center
AMD1072	Excerpts from the Prosecution History of US11,249,690
AMD1073	U.S. Publication No. 2018/0081840 (“Custodio”)
AMD1074	Excerpts from the Prosecution History of EP3,921,739

I. INTRODUCTION

AMD asks the Honorable Director to refer this case for consideration on the merits for at least the following reasons. First, the '750 patent is less than three years old, and AMD acted promptly to begin this IPR as soon as it learned of the patent via Fermat's 2026 lawsuit. AMD's validity challenge seeks to promote legal and economic certainty early on, not only months before the tentatively scheduled District Court trial but also at a point when Fermat admittedly has not commercialized the patented technology in the United States. Second, Fermat's conduct during prosecution raises serious doubt regarding the '750 patent's validity. Indeed, although Fermat concedes that it learned of "similar" prior art products before filing, Fermat failed to disclose that critical information to the Office. Fermat's own submission and exhibits further show that it failed to fully disclose the details of the pre-existing Xilinx technology that Fermat essentially repackaged and tried to sell back to Xilinx. The detrimental effects of Fermat's omissions were then compounded by the Examiner's deficient prior art searching. These material errors prevented the kind of careful vetting on which our patent system depends.

This case is not the David versus Goliath picture that Fermat paints. It instead involves a foreign company that failed to commercialize its product in the U.S. and responded by suing a U.S. technology leader based on a patent it obtained with less than full candor before the Office. Referral and institution will not only correct

material examination errors but also protect the domestic industry from Fermat's attempt to disrupt the production of critical A.I. infrastructure.

II. ARGUMENT

A. Referral and Institution Will Promote Predictable Patent Rights

1. This Challenge Is Early in the '750 patent's Term and Years Before Expectations of Validity Could Vest

Referral is warranted because AMD pursued this IPR at the earliest practicable juncture. Early challenges foster “robust, predictable patent rights and weigh against discretionary denial,” and AMD's challenge is early in multiple respects. *Sun Pharm. Indus., Inc. v. Nivagen Pharm., Inc.*, IPR2025-00893, Paper 18 at 2 (Sep. 19, 2025) (informative). It both outpaces the parallel District Court litigation (*see infra*, §II.C.1) and challenges a patent that is less than three years old. In *Amgen Inc. v. Bristol-Myers Squibb Co.*, the Office referred a petition challenging a three-year-old patent because the patent had “not been in force for a significant amount of time.” *Amgen*, IPR2025-00601, -00602, -00603, Paper 9 at 2 (Jul. 24, 2025) (informative). Here, the facts are even more compelling.

2. Meetings with Xilinx Before the '750 Patent Was Filed Did Not Create Settled Expectations

Fermat incorrectly argues that two meetings with Xilinx, Inc. in January 2019, before Fermat ever sought patent protection of the claimed subject matter, created equitable settled expectations. Paper 7 at 2, 12–14. They did not. First, no such

patent existed in 2019. Fermat fails to explain how “patented” technology could have possibly been discussed in the 2019 meetings when the ’750 patent’s claims did not exist until its filing date in 2022. Paper 7 at 2. This fact exposes Fermat’s accusations as meritless.

Second, Fermat notably failed to provide any evidence that it ever informed Xilinx of any technology that was patented or patent-pending, or even of an intent to apply for any patents. Fermat cannot show on this record that Xilinx, much less AMD, had any knowledge of any then-existing or anticipated “patented” technology. Paper 7 at 2.

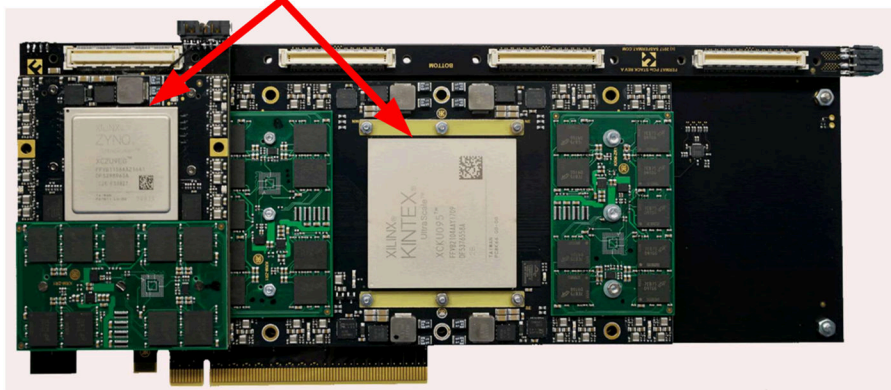
Third, Fermat cannot reasonably assert settled expectations derived from meetings about a product Fermat concedes was just a “combination of Xilinx [prior art] FPGAs with massive storage.” EX2003, 3. Xilinx had no reason to believe that Fermat would pursue patent protection on what appears to be little more than Xilinx’s own chips repackaged on a board with off-the-shelf storage. And while AMD would go on to purchase Xilinx in 2022, Fermat does not accuse any Xilinx products of infringing. This telling omission underscores the lack of any logical nexus between the 2019 meetings and the ’750 patent.

These facts are driven home by Fermat’s evidence, which does not include any discussion of key ’750 patent claim features. For instance, the Declaration of Fermat CEO Robert Bismuth, an attendee at one of the meetings and the lead named

inventor on the '750 patent, offers only vague testimony that the parties “discuss[ed] the prospect of collaborating,” and that Fermat’s “technology” was discussed in a general sense. EX2001, ¶8. A similarly vague presentation from the January 11, 2019 meeting includes generic descriptions and photographs of Fermat’s module but contains no discussion of the later-patented claim features, such as “parallel first tier compute nodes coupled to one or more additional compute nodes in series” and “a data mover component.” EX2004, 1–13. Fermat described the module as a “PCIe carrier board” hosting two Xilinx chips, “32 TB high performance flash storage,” “128GB DDR 4 DRAM,” and “64 GBs DRAM buffer,” confirming it was just a “combination of Xilinx FPGAs with massive storage.” EX2003, 3; EX2004, 6.

Fermat boasted in the presentation that the module incorporated the Zynq™ system-on-chip (SoC) device containing “ARM cores” and the Kintex™ “FPGA managing interface”—both Xilinx products. EX2004, 6. Both Xilinx chips are featured prominently in photographs of Fermat’s module. EX2004, 11, 13.

Multiple Xilinx chips appear on the “module” that Fermat presented to Xilinx in January 2019



EX2004, 13 (annotated).

3. Fermat Undercut Any Claim to Settled Expectations by Concealing Its Patent Filings from Xilinx and Withholding Known Prior Art from the Office

As noted above, Fermat did not disclose any patent applications or plans to file patent applications in the January 2019 meetings with Xilinx. *Supra*, §II.A.2. Fermat only began filing provisional patent applications after the meetings and without ever informing Xilinx or AMD (post-acquisition). Paper 7 at 13; AMD1001, Cover (incorporating provisional applications filed in February, May, and August of 2019). Fermat deliberately chose to remain silent until it surprisingly sued AMD in 2026. Fermat's failure to provide timely notice of its patent filings to Xilinx/AMD, paired with its unexplained delay in bringing suit, undercuts any expectations Fermat could have possibly held.

To make matters worse, Fermat possessed relevant prior art that it never disclosed to the Office during prosecution. For example, Fermat's own evidence shows that it learned of a Samsung-Xilinx joint venture in the January 2019 meetings that Mr. Bismuth believed was "actually...something similar to Fermat." EX2005, 1. But Fermat never disclosed any information relating to this known and publicized technology to the Office. AMD1061, 1 (describing a "SmartSSD, a field programmable gate array (FPGA) SSD, that will offer accelerated data processing and the ability to bypass server CPU limits"); AMD1050, 1–2 (explaining that the SmartSSD is "powered by Xilinx FPGAs" and "SmartSSD is focused on

accelerating storage services such as compression, de-duplication and encryption, as well as compute functions, like machine learning inference and big data analytics”); AMD1051. Fermat also failed to disclose detailed information relating to the Xilinx Zynq™ and Kintex™ chips to the Office, even though these chips were relevant to specific claim features, such as the ’750 patent’s claimed “programmable logic component” and “storage interface component.” *Supra*, §II.A.2. At the very least, Fermat could have and should have cited relevant data sheets regarding the Xilinx chips, which were readily available to (and likely possessed by) Fermat. AMD1056, 1–25; AMD1057, 1–70.

Because our patent system relies on “candor and good faith in dealing with the Office,” Fermat’s failure to disclose this art undermines its claimed expectations of validity and further warrants a full merits review. 37 CFR §1.56(a).

B. Institution Is Warranted to Cure Material Examination Errors Compounded by Fermat’s Withholding of Known Prior Art

Examination of the application leading to the ’750 patent suffered a critical and material error. The Examiner failed to search for multiple key claim limitations which ultimately led to allowance.

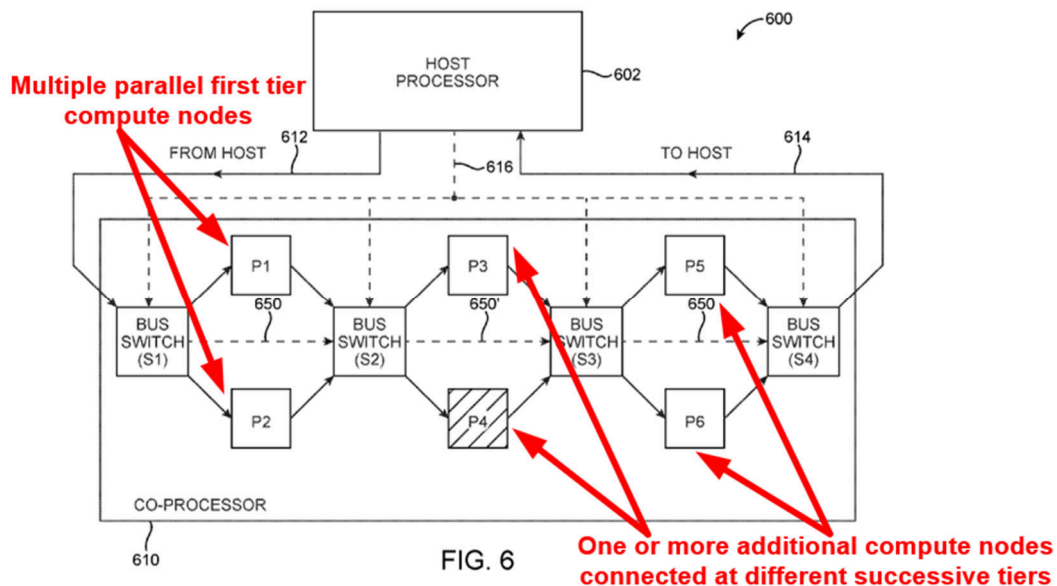
A patent examiner is tasked to “conduct a thorough and complete search of the prior art.” AMD1070, 36; 37 C.F.R. 1.104 (“thorough investigation”). Doing so is a “must,” not an option. *Id.* It requires “obtain[ing] a thorough understanding of the invention disclosed and claimed,” and “search[ing] the prior art as disclosed in

patents and other published documents.” AMD1070, 34. Accordingly, as here, the Office has found material errors when an examiner overlooked teachings of the relevant prior art by failing to identify key references. *E.g.*, *Microsoft Corp. v. Partec Cluster Competence Center GmbH*, IPR2025-00318, Paper 9 at 4 (referring to the merits because “the Examiner erred in overlooking the prior art”).

The Examiner allowed the claims of the ’750 Patent without issuing a single prior art rejection. *See* AMD1002, 333–338, 352–356. During prosecution of US 11,249,690, a parent application of the ’750 patent, the Examiner rejected an independent claim based on Whitehead (AMD1009) that was nearly word-for-word identical to claim 1 of the ’750 patent but did not recite Element [1b] (“multiple parallel first tier compute nodes coupled to one or more additional compute nodes in series”) and part of Element [1c] (“at different successive tiers, each compute node in a series being communicatively coupled, via its communications link to one or more additional compute nodes connected at different successive tiers”). AMD1072, 1, 8–18. Yet the Examiner allowed the ’750 patent’s claims without ever searching for any of these added limitations, and without consulting European counterpart applications in which the EPO rejected an identical independent claim. AMD1002, 170–174. These failures represent a material error. Searches directed at the relevant claim limitations would have surfaced invalidating references like

Dalal, Heil, and Jun, and consideration of foreign prosecution would have yielded an additional reference that provides Elements [1b]–[1c].

In rejecting an independent claim identical to claim 1 of the '750 patent, the EPO cited Custodio (AMD1073) as disclosing Elements [1b]–[1c]. AMD1074, 5–7. For example, the EPO asserted that Claudio discloses “nodes P1-P4...connected in a strict pipelined configuration in which nodes P1-P4 are coupled in a chain” and that Claudio’s FIG. 6 depicts a pipeline that includes multiple parallel first tier compute nodes that are each connected to one or more additional compute nodes. *Id.*; AMD1073, [0042]–[0052], FIGS. 5–6. As depicted below, Claudio is highly relevant to Elements [1b]–[1c]. And the Examiner’s failure to consider Claudio is a material error because Claudio discloses the purportedly novel limitations of the '750 patent’s claim 1.



AMD1073, FIG. 6 (annotated).

AMD's voluntary search disclosure declaration highlights the deficiencies in the Examiner's search. *See* AMD1044. The search declaration establishes that references like Dalal, Ng, Heil, and Jun were located using "multiple, complementary pathways, including keyword and Boolean text string searching." AMD1044, ¶5. Multiple G06F classes were used in AMD's search, just as patent examiners use in their searches. AMD1044, ¶7. The Examiner could have and should have used these same basic strategies to locate the same invalidating references that AMD did. But he did not.

None of the search strings used after Fermat's amendment invoke the key concepts of "multiple parallel first tier compute nodes" that are "coupled to one or more additional compute nodes in series" or each first tier compute node being coupled to "one or more additional compute nodes connected at different successive tiers," which ostensibly led to the quick allowance of the '750 patent. AMD1002, 319–328, 357–373. Perhaps most egregiously, the Examiner's search terms include only a singular "tier" and only a singular "node," (e.g., "tier WITH node WITH memory") and the examiner never searched for references that include more than one compute node arranged into different successive tiers. If the Examiner had used search terms like "processing WITH series," he would have located references like Dalal, Heil, and Jun. AMD1002, 319–328, 357–373.

Dalal expressly discloses a “processing pipeline that can be deepened by a serial flow through multiple hwa modules” and “processing by hwa modules in series and/or in parallel.” AMD1004, [0045], [0047]. Heil explains that “a series of acceleration components are traversed” and describes “connections between nodes” AMD1010, [0073], [0181]. Jun describes multiple “nodes.” AMD1011, 5–9. Simply put, if the Examiner had used relevant keywords to search for these limitations, the search would have returned pertinent portions of references that disclose them. Instead, the Examiner’s chosen search strategy yielded numerous references that refer generally to memory, compute nodes, and routers without providing targeted results that relate to the key claim features.

Fermat’s decision to withhold prior art from the Office during prosecution compounded these examination errors. *Supra*, §II.A.3. Had the Examiner been privy to the information Fermat withheld, it would have materially influenced his conclusions and enhanced his ability to competently search the prior art.

C. Referral and Institution Will Conserve Resources and Make This Proceeding a True Alternative to District Court Litigation

1. The Advanced Timeline of This Proceeding Ensures Institution Will Conserve Resources and Prevent Needless Discovery

The Office has declined to exercise discretionary denial when the Final Written Decision of an early challenge like this one is scheduled to precede a jury trial. *E.g., Google LLC v. Withrow Networks Inc.*, IPR2025-00775, Paper 10 at 2

(“likely that a final written decision in this proceeding will issue before the district court trial occurs, reducing the concern of inconsistent outcomes or significant duplication of efforts”). In this case, the Board’s Final Written Decision will be issued by November 12, 2027, nearly three months before the scheduled start of jury selection on February 7, 2028. AMD1052, 3. And the Board’s Institution Decision will be issued by November 12, 2026, nearly three months before the District Court’s *Markman* hearing on February 1, 2027. AMD1052, 2. Because this proceeding will outpace the parallel litigation, there is a clear and present opportunity for the Board to be the true alternative validity forum that Congress intended.

The advanced timeline of this proceeding relative to the District Court’s schedule also increases the likelihood of a stay upon institution. *E.g.*, Order Staying Case (Document 41), *Resonant Systems, Inc. v. Meta Platforms, Inc.*, 7-25-cv-00035 (WDTX) (Judge Gilliland granting a joint motion to stay litigation pending Final Written Decision); Joint Motion to Stay Case (Document 106), *Greenthread, LLC v. Cirrus Logic, Inc.*, 1-23-cv-00369 (WDTX) (Judge Gilliland granting a joint motion to stay litigation pending Final Written Decision in a case where the IPR petitions were filed seven months after the complaint). A stay would provide significant savings for both parties and the District Court, and it would potentially relieve a jury from the burden of scrutinizing complex computer technology.

Even without a stay, institution would result in the parties saving great expense on expert discovery in the District Court. To ensure this efficiency, “AMD stipulates to not pursue” numerous prior art grounds, including “Grounds 1A–2B” in the Petition, “[a]ny other ground that could have been reasonably raised” in the Petition, “[a]ny ground based on a combination of system prior art... and the references that form the basis of Grounds 1A–2B,” and “[a]ny ground...on the basis of system art mirroring the references that form the basis of Grounds 1A–2B.” AMD1049, 1. Contingent upon institution, none of the grounds foreclosed by AMD’s stipulation can be asserted or developed, which would narrow the scope of AMD’s invalidity case considerably.

2. Overlap with the District Court Proceeding Is Minimized Because AMD’s Stipulation Activates Immediately Upon Institution

Fermat mischaracterizes AMD’s *Sotera*+ stipulation as only attaching “if the IPR reaches ‘an appealable final decision.’” Paper 7 at 7–8. To be clear, AMD stipulated not to pursue any of the named grounds “[i]f *inter partes* review is instituted.” AMD1049, 1–2. AMD has the right to assert the grounds after institution only if (1) “institution is later vacated or reversed,” or (2) if the IPR “is otherwise terminated or de-instituted by the Board or the Director for any reason other than by an appealable final decision.” AMD1049, 1–2.

In short, AMD’s stipulation is contingent upon institution, immediately activates at the time of institution, and remains in place as long as this proceeding remains instituted. AMD1049, 1–2. The Office has referred petitions for consideration on the merits based on similar stipulations, and AMD respectfully requests a consistent outcome here. *See, e.g., Wybotics, Co. Ltd. v. Zodiac Pool Systems LLC*, IPR2026-00158, -00159, -00160, Paper 12 at 10–11 (referring to the merits when petitioner reserved the right to pursue the grounds “if the PTAB declines institution (or if the institution or final written decision resulting from the proceeding is later vacated, withdrawn, or reversed...)”).

Fermat’s assertion that AMD is “pursuing alternative theories under a ‘wait and see’ approach...to gain a litigation advantage” is likewise without merit. Paper 7 at 8–11. First, Fermat has not provided any evidence that AMD has pursued any such “alternative theories” because there are none. *Infra*, §II.C.3. Second, AMD’s stipulation is extremely robust, and institution would prevent a broad range of invalidity grounds from being raised in District Court, including numerous printed publication grounds that are not asserted in this proceeding and even certain grounds employing system art. *See* AMD1049, 1–2. Fermat’s complaint that such a broad stipulation somehow confers a “litigation advantage” on AMD rings hollow.

3. Baseless Speculation That AMD Might Take Inconsistent Claim Construction Positions Should Be Rejected

Fermat's complaint that AMD will "likely" assert inconsistent claim constructions is entirely unsubstantiated. Paper 7 at 11–12. Fermat has provided no evidence that AMD has advanced any inconsistent constructions in this proceeding or in District Court, again, because there are none. If AMD ever asserts conflicting claim construction positions (which it will not), Fermat will have the opportunity to petition for Director Review. AMD has not engaged in such gamesmanship, nor does it have any reason to do so.

D. Institution Protects the Critical United States Semiconductor Industry from Disruption

Fermat is primarily a foreign-based company located in France and Switzerland. Paper 7 at 3–6; AMD1053, 10 (identifying "27/29 Rue Raffet, 75016 Paris" as Fermat's address); AMD1054, 2 (Fermat's LinkedIn profile identifying Paris, France and Basel, Switzerland as "Locations"). In Fermat's online profile, the United States is barely mentioned at all. *Id.* Three job openings are advertised on Fermat's website, all based in Paris with "[t]ravel to Fermat's Basel offices." AMD1058, 2–3; AMD1059, 2–3; AMD1060, 2–3.

As Fermat tells it, the entity named, Fermat International, Inc. (incorporated in Delaware) became the parent of French company SAS Fermat in 2023 in a corporate inversion to allegedly "move...manufacturing from Switzerland to the

U.S.” as part of a broader “shift to the United States.” Paper 7 at 3–6; EX2001, ¶7. But this effort failed, as Fermat could not manage to sell its products in the U.S. *See* Paper 7 at 3–6 (supporting target customers was “beyond Fermat’s capability”); EX2001, ¶7. After failing to gain a foothold in the domestic semiconductor market, Fermat remains a primarily foreign-based company.

Fermat International, Inc. is incorporated in Delaware and claims a “principal place of business” at 2625 Middlefield Road #800, Palo Alto, California 94306. AMD1062, ¶2. But this address is nothing more than a UPS Store where Fermat rents a mailbox. AMD1055, 2. The evidence of record does not reveal any official U.S. address aside from the UPS mailbox.

It is undisputed that Fermat “did not make, offer for sale, sell, or import into the United States any products that practice the Patents-in-Suit during the relevant time period,” and it is unclear whether Fermat ever did. AMD1062, ¶18. While Fermat claims that “[t]he U.S.-based company Micron was Fermat’s largest customer,” there is no evidence on record that Fermat as a whole—much less any domestic part of Fermat—sold anything to Micron in the United States or ever delivered any products to Micron. Paper 7 at 5; EX2001, ¶6. A contemporaneous email from Mr. Bismuth implies that Fermat was Micron’s customer, not the other way around. EX2005, 1 (“we currently use Micron parts everywhere”). Mr. Bismuth told Xilinx that “we...started down the road of a partnership with Micron”

but did not claim that a partnership existed at that time. *Id.* What’s more, Fermat concedes that it “liquidated SAS Fermat in 2024” after facing extreme difficulty in selling its products. Paper 7 at 3–6; EX2001, ¶7.

In contrast, AMD is a U.S.-based semiconductor and technology company that employs thousands of people domestically. AMD1063, 15; AMD1064, 1. AMD manufactures the Instinct™ MI200 Series Accelerator, which is one of the accused products in Fermat’s complaint. AMD1062, ¶¶31–33. The AMD Instinct™ is a Graphics Processing Unit (GPU) that delivers “exceptional performance for the data center, at any scale—from single-server solutions up to the world’s largest, Exascale-class supercomputers.” AMD1065, 2. The Instinct™ is used in the Frontier supercomputer, developed in collaboration with the U.S. Department of Energy and Hewlett Packard Enterprises (HPE). AMD1066, 2 (“AMD, in collaboration with the U.S. Department of Energy, Oak Ridge National Laboratory, and HPE, designed the Frontier supercomputer...[p]owered by...AMD Instinct MI250X accelerators”); AMD1067, 3 (“[t]he system is based on...AMD Instinct 250X accelerators”).

The Instinct™ is a leading product in the hardware accelerator and AI data center market. AMD1071, 5 (“the MI455X offers peak performance” that makes “AMD...more competitive in the AI data center capacity race than ever before”). The strategic importance of this technology to the United States cannot be

overstated. Indeed, the Instinct™ is so mission-critical that it is subject to U.S. Government export control restrictions. AMD1069, 51 (“These controls prevent us from shipping our AMD Instinct™ MI250, MI300X, MI300A, MI388X integrated circuits and our Versal™ VC2802, VE2802 FPGAs to China, or to customers outside of the United States whose ultimate parent is headquartered in a D5 country (including China), without a license.”). AMD’s Instinct™ is unquestionably key to the United States’ efforts to remain a force in artificial intelligence and supercomputing. Instituting this IPR therefore directly serves the national interest by ensuring that a foreign entity cannot use an invalid patent to disrupt the production of critical American infrastructure.

Unlike AMD, Fermat could not sell products in the United States. Having failed, Fermat now seeks to enjoin AMD from contributing to the United States’ leading efforts in artificial intelligence and other major industries. AMD1062, ¶70. The Office should not reward Fermat’s efforts by granting discretionary denial of this timely IPR that presents strong grounds of invalidity against the ’750 patent.

E. The Petition’s Grounds 1A–2B Present a Strong Challenge That Fermat Fails to Meaningfully Rebut

The Director should reject Fermat’s misrepresentations of AMD’s Petition. Grounds 1A–2B are exceptionally strong and demonstrate the obviousness of each challenged claim.

Regarding Ground 1A, Fermat commits the fatal legal error of dissecting the Dalal-Ng Combination and attacking the references individually. *See* Paper 7 at 17 (separately arguing “For Dalal...” and “For Ng...”). Worse, when addressing each individual reference, Fermat falsely asserts that the Petition maps the same prior art teaching to both the “plurality of communications channels” and the “storage interface component.” Paper 7 at 17–18. In fact, the Petition separates them. It explains that paths within a data transfer fabric of Dalal’s hardware accelerators provide the claimed “plurality of communications channels.” Paper 2 at 43–45. And it separately identifies Ng’s memory interfaces as a distinct “storage interface component.” Paper 2 at 45–46. The Petition demonstrates this clear-cut mapping using the following annotated drawing, which Fermat tellingly disregards:

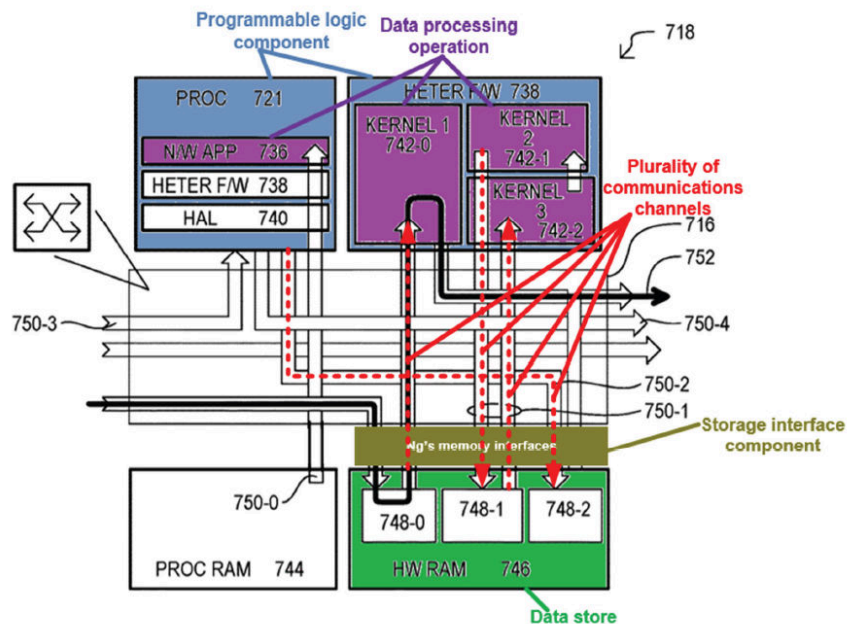


FIG. 7

AMD1004, FIG. 7 (modified).

Paper 2 at 46. Fermat’s remaining complaints are baseless for similar reasons. The Petition clearly “show[s] that the alleged storage interface utilizes the alleged channels.” Paper 7 at 17. It explains that the Dalal-Ng storage interface uses the communications channels to transfer data via intra-node reading and writing operations. Paper 2 at 45–46 (citing AMD1003, ¶102 (“In the combination, the storage interface component utilizes at least one communication channel for reading, and at least one communications channel for reading and writing.”)). Far from leveraging “a POSITA to provide limitations missing from the prior art,” (Paper 7 at 18), the Petition accurately portrays how the POSITA would have understood the art in view of the claimed limitations.

Fermat’s arguments on Ground 2A are conclusory and lack merit. There is no dispute that Heil’s head component (“router module”) includes a transport component with an interface for establishing connections between nodes (“node interface”). Paper 2 at 76–77. It is likewise undisputed that each of Heil’s server unit components (“compute nodes”) includes its own transport component that forms a “communications link” with other connected members of the execution pipeline. Paper 2 at 81–83. The Petition fully explains how the respective transport components satisfy the “router-side node-interface role” and “communications-link role.” Paper 7 at 18–19. Fermat’s refusal to engage with the Petition’s substance is

telling. A bare denial, devoid of evidence or technical reasoning, only underscores the strength of AMD's Petition.

III. CONCLUSION

For all these reasons, AMD respectfully asks the Director to refer this case for merits consideration.

Respectfully submitted,

Dated: August 19, 2026

/Kenneth Wayne Darby Jr./
Kenneth W. Darby Jr., Reg. No. 65,068
David M. Hoffman, Reg. No. 54,174
Usman A. Khan, Reg. No. 70,439
Cameron A. Ubel, Reg. No. 77,081
Joseph W. Bauer, Reg. No. 81,218
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
T: 202-783-5070
F: 877-769-7945
Counsel for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §42.6(e)(4), the undersigned certifies that on August 19, 2026, a complete and entire copy of this Petitioner's Opposition and its supporting exhibits were provided via email, to the Patent Owner by serving the email correspondence addresses of record as follows:

Stephen McBride
Jason S. Charkow
DAIGNAULT IYER LLP
8229 Boone Boulevard, Suite 450
Vienna, VA 22182
Tel: 703-372-9186
smcbride@daignaultiyer.com
jcharkow@daignaultiyer.com
fermat@daignaultiyer.com

/Anastasia Renard/
Anastasia Renard
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
renard@fr.com