

IPR2026-00359
U.S. Patent No. 11,550,512

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

FERMAT INTERNATIONAL, INC.,
Patent Owner.

IPR2026-00359
U.S. Patent No. 11,550,512

PATENT OWNER'S PRELIMINARY RESPONSE

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PATENT OWNER'S EXHIBIT LIST

Exhibit No.	Description
2001	Declaration of Robert Bismuth dated July 16, 2026.
2002	Delaware Division of Corporations, Statement of Good Standing for Fermat International, Inc., dated July 7, 2026.
2003	Email chain between Manish Muthal, Ivo Bolsens and Carrie Chong of Xilinx and Robert Bismuth and Arnaud Blandin of Fermat, dated January 11-January 14, 2019.
2004	Fermat presentation to Xilinx.
2005	January 25, 2019 email from Robert Bismuth to various recipients at Fermat summarizing January 25, 2019 meeting with Xilinx.
2006	February 14, 2022 press release titled “ADM Completes Acquisition of Xilinx,” <i>available at</i> https://www.amd.com/en/newsroom/press-releases/2022-2-14-amd-completes-acquisition-of-xilinx.html ; <i>last accessed</i> July 6, 2026.

I. INTRODUCTION

The Petition does not establish a reasonable likelihood that any challenged claim is unpatentable. Sole independent claim 1 is challenged in ground 1A (Dalal-Ng) and ground 2A (Heil-Jun). In both cases, the Petition fails to demonstrate a reasonable likelihood that claim 1 is unpatentable.

For ground 1A, limitation [1i] requires that “the storage interface component utilizes a plurality of communications channels to transfer data between the programmable logic component and the data store at the respective compute node.” EX1001 [’512 Patent], cl. 1. The Petition simultaneously maps Dalal’s data transfer fabric 716 as both the “storage interface component” limitation and the “communications channels” limitation in claim [1i]. Pet., 40-41. But the Petition does not explain how Dalal discloses that the alleged storage interface component utilizes the alleged communications channels to transfer data as required by the claim. The Petition attempts to overcome this problem by alleging Ng’s memory interfaces are simultaneously both the claimed “storage interface component” and “plurality of communications channels.” Pet., 42-43. But this mapping fails for the same reason as Dalal—the Petition fails to explain how those memory interfaces utilize a plurality of communications channels to transfer data as required by the claim.

For ground 2A, the Petition relies exclusively on Heil as disclosing

limitations [1a] and [1c]. Pet., 72-74, 77-79. The Petition also defines each claimed compute node as a host-plus-accelerator server unit, but relies on accelerator-level coupling and execution to establish the “serially coupled compute nodes in an execution pipeline” required by [1b]. Pet., 74–77. But Heil does not disclose [1a] or [1c]. For limitation [1a], the Petition does not explain how Heil supplies the claimed node interface for Heil’s alleged router module, or how the alleged node interface is coupled to a claimed compute node. For limitation [1c], the Petition does not establish that the alleged router module (head component 3604) contains a node interface communicatively coupled to the alleged compute node.

For these and the other reasons discussed below, the Petition fails to demonstrate a reasonable likelihood that any challenged claim is unpatentable. Accordingly, the Director should deny institution on the merits.

II. BACKGROUND

A. Patent Owner Fermat

Patent Owner Fermat International, Inc. (“Fermat”) is a small company that operated in the U.S. and France manufacturing near memory high speed compute modules for servers that included flash-based storage and significant DRAM memory. Ex. 2001 [Bismuth Decl.], ¶ 2. Founded in 2016, at its largest, Fermat had approximately 10 employees. *Id.*

Fermat sold its storage computation solutions primarily to U.S.-based customers. Ex. 2001 [Bismuth Decl.], ¶ 6. The U.S.-based company Micron was Fermat's largest customer. *Id.* A photograph of Fermat's commercialized module is shown below:



Id.

By the end of 2023, Fermat was faced with increased competition from major vendors like Petitioner who were adopting architecture covered by Fermat's issued U.S. patents. *Id.* Even though Fermat's products still held a performance advantage, the ability of major companies like Petitioner to sell to and support the customers Fermat was targeting was beyond Fermat's capability. *Id.* In other words, scaling Fermat was proving difficult due to market competition from large companies like Petitioner that had adopted Fermat's patented technology. *Id.* As a

result, Patent Owner ceased operations in 2024 and filed a lawsuit for patent infringement against Petitioner in January 2026. *Id.*

B. The '512 Patent

1. Background of the Invention

The inventors of the '512 Patent recognized that that the volume of data available for computation was growing at a much greater rate than processor speed. With the advent of the “internet of things” in addition to the automation of almost all processes in the world (plus the increasing speed of the Internet for moving data), the rate of data collection is constantly accelerating and does not suffer from the slowing down that Moore’s Law produces for processors.

At the same time, storage densities had also increased to the point where data storage costs are not a significant factor. With the advent of massive SSD storage modules, data had become very energy efficient since data essentially uses zero energy unless it is actively being accessed. In reality, most data is not accessed very frequently, if at all.

No matter how fast a processor is, there are mass storage to memory transfers, memory to processor data transfers, memory to processor instruction transfers, results are transferred to memory, and, in some cases, results from memory are transferred to mass storage. All these steps take significant amounts of time and cannot be executed in parallel. So, total computation time is the total

length of time taken to transfer and execute whatever computation per data element multiplied by the total number of data elements. The time taken for all this movement of data and instructions vastly exceeds the time a processor spends actually executing computational instructions on data loaded into its registers.

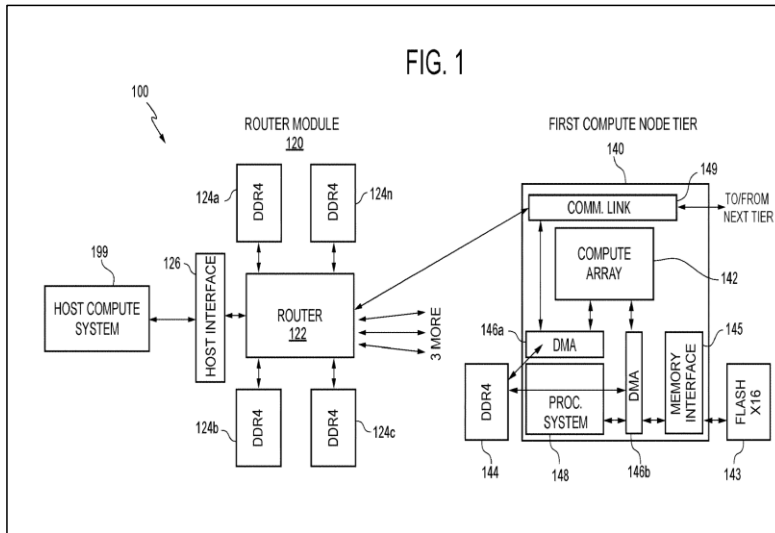
The inventors behind the Fermat architecture realized that by placing processors (any type of processors) extremely “close” to mass storage, these transfer times could be minimized and, in some cases, eliminated. The key was integrating processors with storage in the sense of providing a direct very high-speed connection between processors and storage with either the silicon of the processor pre-configured for the specific algorithm of interest or the processor linked by a dedicated separate high speed bus to high speed DRAM holding the algorithm. In this way, data could be streamed directly from mass storage to the processor, eliminating the need to first move it to DRAM or from DRAM to the processor, and, depending on the processor type, either eliminating or drastically speeding up instruction fetch times.

C. The '512 Patent

The '512 Patent reflects the problem identified by the inventors, explaining that “with the explosion of data available to such systems ... the sheer volume of available data to process is increasing faster than traditional hardware and software systems are able to evolve in order to process those data in a meaningful and

efficient manner.” ’512 Patent, 1:45-53. “As a practical matter, it will be appreciated that for as long as the rate at which new data become available for processing continues to outpace the rate at which processing methodologies advance to accommodate the increased size of a given dataset, it will continue to take longer to solve bigger and more complex data processing problems.” *Id.*, 1:61-67. Accordingly, “there is a need for an improved system and method employing a distributed hardware architecture that facilitates high throughput data processing and analytics solutions for resource-intensive applications.” *Id.*, 2:1-4.

To address this need, the ’512 Patent proposed “an architectural framework that may employ high performance data processing elements (compute nodes) coupled with massive data storage (a data store) in a unique configuration that minimizes or eliminates typical processor/network wait states, optimizes instruction fetch memory cycles, and analyzes data that are streamed from an attached or associated data store at the maximum rate at which the data can be accessed or streamed by the storage subsystem.” *Id.*, 7:4-13. Figure 1 (below) is a “functional block diagram illustrating one implementation of a data processing and analytics system for use in connection with a host compute system” *Id.*, 5:53-55:

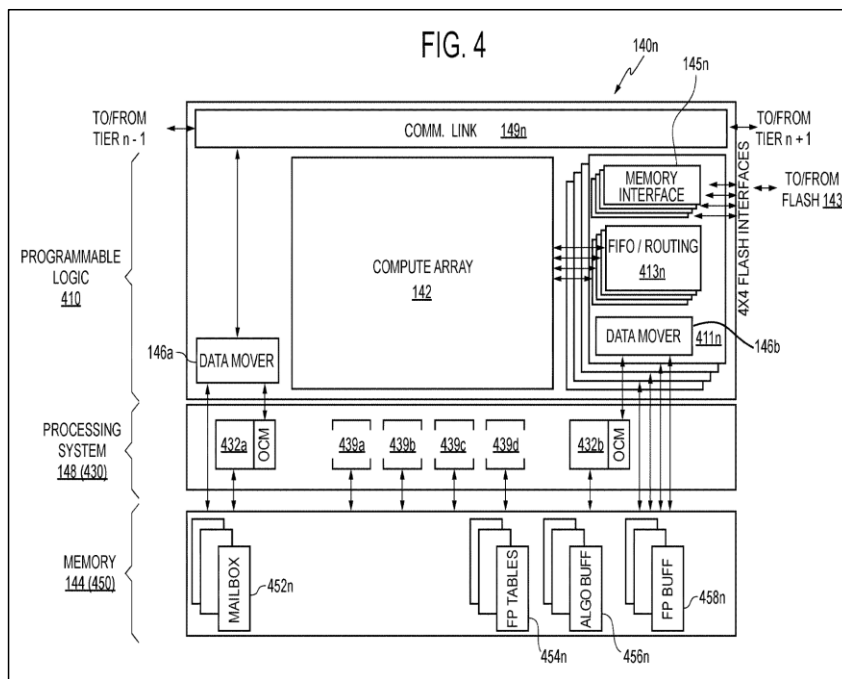


EX1001 [’512 Patent], Fig. 1.

As shown, Figure 1 comprises “a host compute system 199, a router module 120, and a compute node 140.” *Id.*, 8:25-27. “Host compute system 199 may generally be embodied in or comprise a computer server, a desktop or workstation 30 computer, a laptop or portable computer or tablet, or a combination of one or more of such components.” *Id.*, 8:28-31. “Router module 120 may generally comprise a router 122, one or more router memory components 124a, 124b, 124c, . . . 124n (‘router memory 124’) and a host interface 126.” *Id.*, 9:4-9. “[R]outer module 120 may also include one or more node interfaces [] such as network interface cards, wireless or inductive hardware components, or communications ports, jacks, or plugs, for instance, to enable router 122 to communicate with a

respective compute node 140... ” *Id.*, 9:7-13.

The compute nodes 140 are the data processing elements coupled to data stores to minimize wait states and optimize memory cycles. “[E]ach compute node 140 may generally comprise a compute array 142, a data store 143, a data store interface 145, node memory 144, one or more datamover apparatus (DMA) 146a and 146b (“DMAs 146”), and a processing system 148.” EX1001 [’512 Patent], 10:4-9. Figure 4 “is a functional block diagram illustrating components of an implementation of a compute node.” *Id.*, 5:64-67:



EX1001 [’512 Patent], Fig. 4.

The '512 Patent envisions the use of multiple compute nodes. The '512 Patent explains that each compute node “may be communicatively coupled, via communications link 149n to one or more additional compute nodes 140 connected in series at different successive tiers.” *Id.*, 14:59-63.

D. Claims of the '512 Patent

The '512 Patent has twelve claims. Claim 1 is independent and claims 2-12 each depend on claim 1. Because there is only one independent claim, the Petition may not be instituted unless the Petition demonstrates a reasonable likelihood that the Petitioner would prevail in proving claim 1 is unpatentable. 35 U.S.C. § 314(a). As discussed below, Petitioner fails to do so.

Similar to Figure 1, the claims of the '512 Patent address the problem identified by the inventors by claiming a data processing system comprising a routing module and a plurality of serially coupled compute nodes in an execution pipeline. Claim 1 is reproduced below:

[1pre]	A data processing system operative in cooperation with a host compute system, the data processing system comprising:
[1a]	a router module comprising a host interface and a node interface, wherein the router module is communicatively coupled to the host compute system via the host interface; and
[1b]	a plurality of serially coupled compute nodes in an execution pipeline, each respective compute node in the execution pipeline comprising:

[1c]	a communications link, wherein the respective compute node is communicatively coupled to the node interface at the router module via the communications link either directly or indirectly via an adjacent compute node;
[1d]	a data store comprising records associated with a data processing operation;
[1e]	a programmable logic component to execute the data processing operation in cooperation with the data store;
[1f]	a node memory comprising data and instructions to support operation of the programmable logic component in connection with the data processing operation and to facilitate inter-node data communications via the communications link;
[1g]	a data mover component to facilitate intra-node data communications between the programmable logic component and the node memory at the respective compute node; and
[1h]	a storage interface component to facilitate intra-node data communications between the programmable logic component and the data store at the respective compute node;
[1i]	wherein the storage interface component utilizes a plurality of communications channels to transfer data between the programmable logic component and the data store at the respective compute node.

E. Related Proceedings

On January 13, 2026, Patent Owner asserted the '512 Patent, along with several related patents, in *Fermat International, Inc. v. Advanced Micro Devices*,

Inc., Civil Action No. 7-26-cv-00011 (W. D. Tex.). That case is currently proceeding in Texas.

On May 12, 2026, Petitioner filed this IPR, along with IPR2026-00358 and IPR2026-00360 challenging related U.S. Patent Nos. 11,886,750 and 12,271,636, respectively. All three IPRs are in the pre-institution phase.

III. LEVEL OF ORDINARY SKILL

The Petition proposes the following level of ordinary skill:

A person of ordinary skill in the art (“POSITA”) relating to the subject matter of the ’512 patent as of the Critical Date would have had a bachelor’s degree in Computer Engineering, Electrical Engineering, Computer Science, or a comparable field and at least two years of experience related to computer architecture. AMD1003, ¶¶27–28.

Additional experience could substitute for a formal degree or formal training (and *vice versa*). *Id.*

Pet., 4. For purposes of this preliminary response, Patent Owner does not dispute Petitioner’s level of ordinary skill.

IV. CLAIM CONSTRUCTION

Petitioner identifies the claim term “programmable logic component” as a “logic component programmable by reconfiguring its internal hardware connections, such as an FPGA.” Pet., 5. For purposes of this preliminary response, Patent Owner does not believe any claim term needs to be construed. Patent Owner reserves the right to propose constructions if this IPR is instituted.

**V. THE PETITION DOES NOT ESTABLISH A REASONABLE
LIKELIHOOD THAT CLAIM 1 IS UNPATENTABLE**

The Petition alleges four grounds:

ID	Claims	Prior Art Basis Under §103
1A	1–3, 6–12	Dalal-Ng
1B	4, 5	Dalal-Ng-Raghava
2A	1–4, 6–9, 11–12	Heil-Jun
2B	5, 10	Heil-Jun-Raghava

Pet., 1.

The '512 Patent has only one independent claim (claim 1). The Petition only challenges claim 1 in grounds 1A (Dalal-Ng) and 2A (Heil-Jun). This Petition may only be instituted if either Dalal-Ng or Heil-Jun demonstrates a reasonable likelihood that claim 1 is unpatentable. 35 U.S.C. § 314(a). Thus, for purposes of this POPR, Patent Owner analyzes only ground 1A claim 1 and ground 2A claim 1. Because neither Dalal-Ng (ground 1A) nor Heil-Jun (ground 2A) demonstrate a reasonable likelihood that claim 1 is unpatentable, institution must be denied.

**A. The Dalal-Ng Combination Does Not Establish A Reasonable
Likelihood That Claim 1 Is Unpatentable**

**1. The Petition Does Not Establish the Storage-Interface-to-
Channels Relationship Required by [1i]**

Limitation [1i] requires that the storage-interface component “utilizes a plurality of communications channels to transfer data between the programmable

logic component and the data store at the respective compute node.” EX1001 [’512 Patent], cl. 1. The Petition maps Dalal’s HWA modules as the alleged “compute nodes.” Pet., 19. The Petition maps Dalal’s second memory 746 as the alleged “data store” (Pet., 23), and Dalal’s processing circuits 721 plus framework 738 collectively as the “programmable logic component.” Pet., 26. For limitation [1g], the Petition relies on path 750-0 through data transfer fabric 716 as the alleged “data mover” (Pet., 35); for [1h], on data transfer paths through the same data transfer fabric 716 as the alleged “storage interface component” (Pet., 37); and for [1i], on paths through that same data transfer fabric 716 as the alleged “communications channels.” Pet., 40-41. Thus, the Petition simultaneously relies on paths through Dalal’s data transfer fabric 716 to satisfy not only the “data mover” and “storage interface component” limitations, but also the “communications channels” limitation.

Even if the claimed storage interface and claimed communications channels could be simultaneously mapped to the same paths in Dalal’s data transfer fabric 716, this does not establish that the alleged storage interface component *utilizes* those paths as “communications channels to transfer data between the programmable logic component and the data store at the respective compute node” as required by limitation [1i]. The Petition does not identify what within data transfer fabric 716 performs that interface function, which paths it uses as

Commented [S1]: Sanjay: The reason for this change is to correct the malformed quotation so it tracks the language of limitation [1i].

communications channels, or how it uses them for the claimed data transfer. The Petition's separate assertion that a POSITA would implement a "dedicated storage interface component" with memory-protocol circuitry likewise establishes, at most, interface capability; the Petition does not connect that circuitry to the paths it separately maps as limitation [1i]'s communications channels. Pet., 35–39. Thus, the Petition has not demonstrated that Dalal teaches or suggests limitation [1i].

2. Dalal Figures 7 and 8 Do Not Supply the Missing Relationship

The Petition asserts that Dalal Figure 7 contains "at least four" data-transfer paths between processing circuits 721 and second memory 746, but the Petition body does not identify four numbered routes. Pet. 41 (discussing Dalal Fig. 7). The path count does not itself establish the storage-interface operation that utilizes the asserted paths as communications channels for the claimed transfer at the respective compute node. The Petition still must establish the relationship required by [1i], not merely identify paths through the same fabric it separately maps as the storage-interface component.

The Petition also points to Dalal Figure 8, asserting that it depicts a plurality of communications channels transferring data between memory spaces and execution processes "within an hwa module." Pet. 41–42 (discussing Dalal Fig. 8). Even accepting that characterization and the Petition's allegation that Dalal's HWA

modules are the claimed compute nodes, the Petition does not identify a storage interface component at Dalal's HWA modules that utilizes the asserted plurality of transfers as communications channels. Dalal Figures 7 and 8 therefore do not establish limitation [1i].

3. Ng Does Not Cure the Dalal Mapping

Because Dalal does not teach or suggest limitation [1i], Petitioner also alleges Ng's first and second memory interfaces 312 are collectively the claimed "storage interface component" and individually the claimed "plurality of communications channels." Pet., 42–43; EX1005 [Ng], Fig. 3, [0038]. The Petition does not identify the collective storage interface component that utilizes Ng's memory interfaces as communications channels "to transfer data between the programmable logic component and the data store at the respective compute node" as required by limitation [1i]. The Petition also does not explain how Ng's memory interfaces operate with the retained Dalal fabric to perform the claimed transfer at the respective compute node. Thus, Ng does not cure the deficiencies in Dalal, and Ground 1A does not teach or suggest limitation [1i].

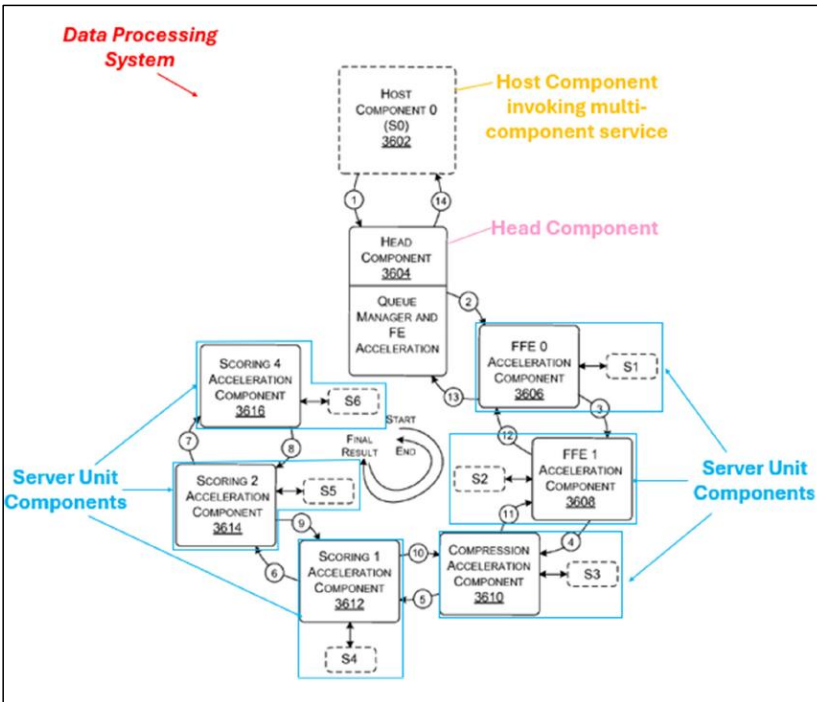
B. The Heil-Jun Combination Does Not Establish A Reasonable Likelihood That Claim 1 Is Unpatentable

1. Petitioner Defines Each Compute Node Broadly but Proves the Pipeline Through Acceleration Components

The Petition alleges Heil's server units containing a local host component

and a local acceleration component are collectively the claimed “compute node.” Pet., 74–75, 85 & n.5. Thus, the Petition alleges the claimed “compute node” consists of several components in Heil. That broader node boundary causes the Petition’s mapping to fail. The Petition also alleges Heil’s local host’s main memory supplies the claimed node memory [1f], and Heil’s “components used for PCIe/DMA” supply the intra-node data mover limitation [1g]. Pet., 85–90. Petitioner relies on Heil’s accelerator-side logic and transport component 2530 for other node functions and adds Jun’s storage subsystem for limitations [1d], [1h], and [1i]. Thus, Petitioner alleges the claimed “compute node” spans more than Heil’s acceleration component alone.

Limitation [1b] requires “a plurality of serially coupled compute nodes in an execution pipeline.” EX1001 [’512 Patent], cl. 1. While the Petition broadly alleges the compute nodes are Heil’s server units, the Petition maps that relationship more narrowly to functionality between Heil’s acceleration components alone. The Petition states that Heil’s pipelined server-unit components “would have been serially coupled via at least two respective acceleration components.” Pet. 76 (emphasis omitted). The Petition points to Heil Figure 36 as depicting the service sequence and result return through acceleration components 3604–3616, while S1–S6 are the local hosts associated with those accelerators. EX1010 [Heil], [0221]–[0223], Fig. 36.



Pet. 64 (Petitioner's annotated EX1010 Figure 36).

The distinction is not merely graphical. Heil describes the multi-component service, its neighbor relationships, connection map, partitioning, execution, and repair in terms of acceleration components. EX1010, claim 1, [0068], [0095], [0199]-[0202], [0206]-[0211], [0221]-[0223], [0232]. Heil discloses this activity as being organized and operated at acceleration component granularity, not at the higher level of server units.

The fact that a composite node may communicate through a constituent component does not resolve Petitioner's mapping. The Petition still must establish

that the combined host and accelerator server units it alleges are the claimed compute nodes are the entities serially coupled in the claimed execution pipeline. *See, e.g.*, EX1001 ['512 Patent], limitation [1b] (“a plurality of serially coupled compute nodes in an execution pipeline...”). The Petition alleges Heil’s local host contains a main memory corresponding to the claimed node memory (Pet., 85) and that Heil’s local host component and local acceleration component “using PCIe in conjunction with DMA [(direct memory access)] transfer” correspond to the claimed data mover. Pet., 89-90. But the Petition relies on Heil’s accelerator-level coupling and execution to establish the “serially coupled compute nodes in an execution pipeline.” Pet., 77. The Petition’s statement that the server units (i.e., the claimed compute nodes) would have been “serially coupled via at least two respective acceleration components” identifies the constituent through which Petitioner proposes to couple them; it does not itself establish that Heil’s server units themselves are “serially coupled ... in an execution pipeline” as required by claim 1. Put another way, Heil’s acceleration components are not the complete server unit components Petitioner alleges are the claimed compute nodes under [1b]. Pet. 76 (emphasis omitted).

The express language of limitations [1f] and [1g] makes the Petition’s mismatch consequential. Those mappings confirm that Petitioner’s claimed compute node is the broader server unit, not the acceleration component alone.

Claim 1 requires node memory in each respective pipeline node to support the programmable logic and facilitate inter-node data communications, and requires the data mover to facilitate intra-node communications between that node memory and programmable logic “at the respective compute node.” EX1001, cl. 1.

Petitioner’s host memory and PCIe/DMA mappings place those functions inside Heil’s broader server unit component. Pet., 85–90. The specific deficiency is [1b]: the Petition does not establish that Heil’s server unit components are the entities Heil serially couples and executes as the service pipeline.

2. The Petition Fails to Establish the Router Module-Side Node Interface Relationship Required by [1a] and [1c]

The Petition’s mapping for limitations [1a] and [1c] also fails. Limitation [1a] requires “a router module comprising a host interface and a node interface.” Limitation [1c] requires each of the “plurality of serially coupled compute nodes” to be “communicatively coupled to the node interface at the router module” by its communications link. EX1001, cl. 1.

For limitation [1a], the Petition alleges Heil’s head acceleration component 3604 is the claimed router module and alleges Heil’s transport component 2530’s “register interface to establish connections between nodes” is the claimed node interface. Pet., 71-74. For [1c], the Petition alleges the connection shown in Heil Fig. 36 between head component 3604 and acceleration component 3606 is the

claimed communicative coupling and that Heil's transport components 2530 "functions as part of [the claimed] communications link." Pet., 77–79; EX1010 [0181]. But while the Petition identifies an alleged router module (Heil's head acceleration component 3604) and an alleged node interface (Heil's transport component 2530), it does not establish that the mapped communications link is coupled to that node interface.

Figure 36 shows head component 3604 connected to the nearest pipeline acceleration component, but depicts 3604 only as a whole. Pet., 77-78; EX1010 Fig. 36. The Petition still must establish that the alleged router module (head component 3604) contains a node interface communicatively coupled to the alleged compute node. EX1001 ['512 Patent], claim [1c] ("compute node is communicatively coupled to the node interface at the router module via the communications link."). Figure 36 does not do so.

If Heil's register interface of transport component 2530 is the alleged node interface, the Petition does not establish how Heil's downstream server unit components (the alleged compute nodes) couple to that register interface. If Petitioner instead relies on head-side transport component 2530 as a whole as the node interface, the Petition still does not establish that the link between head component 3604 and acceleration component 3606 couples to 2530 rather than merely to head component 3604 at an unspecified point. Either way, the Petition

does not establish the router-side node-interface-to-link relationship required by [1a] and [1c].

3. Petitioner’s One-Dimensional Topology Rationale and Jun Do Not Cure These Deficiencies

Petitioner argues that modifying Heil’s two-dimensional torus to a one-dimensional topology would have been obvious from Figure 36’s service flow, related Catapult work, reduced cabling complexity, and the finite number of practical torus dimensions. Pet., 75–77. Even accepting that rationale, it only changes the topology of the acceleration-component network; it does not establish that Petitioner’s broader host-plus-accelerator server units are “serially coupled compute nodes in an execution pipeline” as required by [1b], and it does not establish the router-side interface-to-link coupling required by [1a]/[1c].

The Petition does not allege that Jun supplies limitations [1a], [1b], or [1c]; those limitations are mapped to Heil. Pet., 71–79. Accordingly, Ground 2A does not establish a serial execution pipeline of the compute nodes Petitioner maps and separately does not establish the node-interface-to-link relationship required by [1a] and [1c]. The Petition therefore has not shown a reasonable likelihood that Claim 1 is unpatentable.

VI. CONCLUSION

For the foregoing reasons, the Petition fails to demonstrate a reasonable

likelihood that the single independent claim 1 is unpatentable. Thus, institution must be denied.

Dated: August 19, 2026

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(b)(1), the undersigned certifies that this Patent Owner Preliminary Response complies with the word limitation of that section because it contains 4,037 words as calculated by Microsoft Word.

Dated: August 19, 2026

Respectfully Submitted,

By: / Stephen McBride /
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IPR2026-00359
U.S. Patent No. 11,550,512

CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing PATENT OWNER'S
PRELIMINARY RESPONSE was served electronically via email on August 19,
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