CLAIMS

1. A data processing system operative in cooperation with a host compute system, the data processing system comprising:

a router module comprising a host interface and a node interface, wherein the router module is communicatively coupled to the host compute system via the host interface; and

multiple parallel first tier compute nodes coupled to one or more additional compute nodes in series, each compute node comprising:

a communications link, wherein each first tier compute node is communicatively coupled to the node interface at the router module via the communications link, at different successive tiers, each compute node in a series being communicatively coupled, via its communications link to one or more additional compute nodes connected at different successive tiers;

a data store comprising records associated with a data processing operation;

a programmable logic component to execute the data processing operation in cooperation with the data store;

a node memory comprising data and instructions to support operation of the programmable logic component in connection with the data processing operation and to facilitate data communications via the communications link;

a data mover component to facilitate data communications between the programmable logic component and the node memory; and

a storage interface component to facilitate data communications between the programmable logic component and the data store;

wherein the storage interface component utilizes a plurality of communications channels to transfer data between the programmable logic component and the data store.

2. The data processing system of claim 1 wherein the communications link employs a serial communications protocol.

3. The data processing system of claim 1 wherein the data store comprises an Electronically Erasable Programmable Read Only Memory device.

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4. The data processing system of claim 3 wherein the storage interface component employs and Open NAND Flash Interface protocol.

5. The data processing system of claim 1 wherein the programmable logic component comprises a field programmable gate array.

6. The data processing system of claim 1 further comprising a processor to manage operation of the data mover component.

7. The data processing system of claim 6 wherein the data mover component comprises a device controller.

8. The data processing system of claim 1 wherein the host compute system executes instructions to influence operation of the compute node.

9. The data processing system of claim 1 wherein the router module and the compute node are integrated into an interface card communicatively coupled to the host compute system.

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Applicant: Fermat International, Inc..		

Communication pursuant to Article 94(3) EPC

The examination of the above-identified application has revealed that it does not meet the requirements of the European Patent Convention for the reasons enclosed herewith. If the deficiencies indicated are not rectified the application may be refused pursuant to Article 97(2) EPC.

You are invited to file your observations and insofar as the deficiencies are such as to be rectifiable, to correct the indicated deficiencies within a period

of 4 months

from the notification of this communication, this period being computed in accordance with Rules 126(2) and 131(2) and (4) EPC. One set of amendments to the description, claims and drawings is to be filed within the said period on separate sheets (R. 50(1) EPC).

If filing amendments, you must identify them and indicate the basis for them in the application as filed. Failure to meet either requirement may lead to a communication from the Examining Division requesting that you correct this deficiency (R. 137(4) EPC).

In case you withdraw the application within the above-mentioned period, the examination fee will be refunded at a rate of 50% (Art. 11 (b) RFees).

Failure to comply with this invitation in due time will result in the application being deemed to be withdrawn (Art. 94(4) EPC).

Registered letter

Freitas, Arthur
Primary Examiner
For the Examining Division

Enclosure(s): 5 page/s reasons (Form 2906)
US-20180081840-A1

The examination is being carried out on the **following application documents**

Description, Pages

1-69 as published

Claims, Numbers

1-9 filed in electronic form on 25-07-2023

Drawings, Sheets

1/29-29/29 as published

Reference is made to the following documents; the numbering will be adhered to in the rest of the procedure.

D1 US 2016/196077 A9 (HITACHI LTD [JP]) 7 July 2016 (2016-07-07)

D2 US 2004/268088 A1 (LIPPINCOTT LOUIS A [US] ET AL) 30 December 2004 (2004-12-30)

The following document is cited by the Examiner . A copy of the document is annexed to the communication and the numbering will be adhered to in the rest of the procedure.

D5 US 2018/081840 A1 (CUSTODIO EVAN [US]) 22 March 2018 (2018-03-22)

1 Inventive Step (Article 56 EPC)

1.1 Claim 1

1.1.1 The subject-matter of claim 1 does not involve an inventive step within the meaning of Article 56 EPC, and the requirements of Article 52(1) EPC are therefore not met.

1.1.2 D5 may be considered to be the prior art closest to the subject-matter of said claim, and discloses (references in parentheses applying to this document):

A data processing system operative in cooperation with a host compute system, the data processing system comprising: (figure 3)

a router module comprising (paragraph 8: "bus switch ") a host interface and a node interface (figure 6: "612", "614"), wherein the router module is communicatively coupled to the host compute system via the host interface; and (figure 3: see host 302 connected via 312)

multiple parallel first tier compute nodes coupled to one or more additional compute nodes in series, (paragraph 42: " nodes P1-P4 are connected in a strict pipelined configuration in which nodes P1-P4 are coupled in a chain")

each compute node comprising:

a communications link, wherein each first tier compute node is communicatively coupled to the node interface at the router module via the communications link,

at different successive tiers, each compute node in a series being communicatively coupled, via its communications link to one or more additional compute nodes connected at different successive tiers; (figure 6: see that the nodes are connected to the bus switch)

a data store comprising records associated with a data processing operation; (paragraph 50: " data is being received and processed at the intended processing nodes."; It is implicit that the received data is stored when it is received)

a programmable logic component to execute the data processing operation in cooperation with the data store; (paragraph 50: " data is being received and processed at the intended processing nodes.")

~~a node memory comprising data and instructions to support operation of the programmable logic component in connection with the data processing operation and to facilitate data communications via the communications link;~~

~~a data mover component to facilitate data communications between the programmable logic component and the node memory;~~

and a storage interface component to facilitate data communications between the programmable logic component and the data store; (paragraph 50: " data is being received and processed at the intended processing nodes." and interface therefore is implicit)

~~wherein the storage interface component utilizes a plurality of communications channels to transfer data between the programmable logic component and the data store.~~

1.1.3 The subject-matter of said claim therefore differs from said document in that:

a) a node memory comprising data and instructions to support operation of the programmable logic component in connection with the data processing operation and to facilitate data communications via the communications link; a data mover component to facilitate data communications between the programmable logic component and the node memory

b) the storage interface component utilizes a plurality of communications channels to transfer data between the programmable logic component and the data store.

1.1.4 The technical effect caused by this difference is:

a) The are implemented as microprocessors with a local memory, that is, they can programmed to process data from a local memory. A microprocessor can execute a variety of tasks through software instructions, allowing for easy updates and changes in functionality without the need for physical circuit modifications.

b) The communication with the data store is performed at a higher speed

1.1.5 Since (a) and (b) are merely juxtaposed without having any relation or synergistic effect to each other, a separate problem-solution reasoning is formulated for each of those problems independently (see G-VII, 5.2, last paragraph). Thus, the objective technical problems to be solved by the present invention may be regarded as:

a) How to improve the flexibility and reprogrammability of the nodes?

b) How to accelerate the communication with the data store?

1.1.6 The solution proposed in said claim of the present application cannot be considered as involving an inventive step (Articles 52(1) and 56 EPC) for the following reasons:

1.1.7 The skilled person, in the expectation of improvement or advantage, would naturally consider the above-mentioned problems.

Re a) using a microprocessor with a local cache for data and instructions and a local cache controller is a common measure.

Re b) Accessing a data store via plural communication channels is a common measure.

1.1.8 The indications provided in the prior art are sufficient to prompt the skilled person, namely when the above-mentioned problem is to be solved, to use the features of **D5 and common general knowledge**, thus arriving at the system according to said claim without the need of any inventive activity. Consequently, the proposed solution in said independent claim cannot be considered inventive (Article 56 EPC).

2 **Dependent Claims**

2.1 The subject-matter of the dependent claims does not appear to contain any additional features which, in combination with the features of any claim to which they refer, meet the requirements of the EPC for essentially the same reasons provided in the previous official communication.

3 **Further Proceedings**

3.1 Should the applicant decide to counter-argument to these objections, a fully reasoned problem-solution analysis should please be provided to the Examining Division to substantiate the applicant's standpoint **(Guidelines G-VII. 5, Article 56 EPC)**. The applicant should please indicate the difference of any new claim vis-à-vis the cited prior art, the technical problem solved by this difference and how this technical problem is solved in a non-obvious way by the features of all independent claims.

3.2 To meet the requirements of **Rule 42 (1) (a) EPC** the technical field of the invention must be specified before the indication of the background art.

3.3 To meet the requirements of **Rule 42(1) (b) EPC**, the cited prior art should be identified in the description and the relevant background art disclosed therein should be briefly discussed.

3.4 Any amended independent claim should be in the two-part form in accordance with **Rule 43(1) EPC**, with those features known in combination from prior art being placed in the preamble (**Rule 43(1)(a) EPC**) and the remaining features being included in the characterizing part (**Rule 43(1)(b) EPC**).

3.5 The features of claims should be provided with reference signs placed in parentheses to increase the intelligibility of the claims (**Rule 43(7) EPC**). This applies to both the preamble and characterizing portion (**see Guidelines F-IV, 4.19**).

3.6 When filing amended claims the applicant should at the same time bring the description into conformity with the amended claims. Care should be taken during revision, especially of the introductory portion and of any statements of problem or advantage, not to add subject-matter which extends beyond the content of the application as originally filed (**Article 123(2) EPC**).

3.7 Furthermore, the amended claims may not relate to unsearched subject matter which does not combine with the originally claimed invention or group of invention to form a single general inventive concept (**Rule 137 (5) EPC**). The applicant may pursue such subject-matter only in the form of a divisional application (**Article 76 EPC**).

3.8 In order to facilitate the examination of the conformity of the amended application with the requirements of **Article 123(2) EPC**, the applicant should clearly identify the amendments made, irrespective of whether they concern amendments by addition, replacement, or deletion, and indicate the passages of the application as filed on which these amendments are based (**see Guidelines H-III.2.2**).

3.9 It is kindly requested that the applicant provides for each amendment a narrowly identified basis **in the original application documents**. Whenever an amendment does not find a literal support in the original application documents, it is kindly requested that the applicant provides an explanation of why the words of a certain passage of the original application documents support the wording used in the current application documents.