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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,130	04/18/2022	Nima Badizadegan	00287-0016	3228

1912 7590 10/01/2024

AMSTER, ROTHSTEIN & EBENSTEIN LLP
405 LEXINGTON AVENUE
FLOOR 48
NEW YORK, NY 10174

EXAMINER
BURD, KEVIN MICHAEL

ART UNIT	PAPER NUMBER
2632	

MAIL DATE	DELIVERY MODE
10/01/2024	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

APPLICATION NO.	ISSUE DATE	PATENT NO.
17/723,130	01-Oct-2024	12107587

AMSTER, ROTHSTEIN & EBENSTEIN LLP
405 LEXINGTON AVENUE
NEW YORK, NY 10174

EGRANT NOTIFICATION

Your electronic patent grant (eGrant) is now available, which can be accessed via Patent Center at https://patentcenter.uspto.gov

The electronic patent grant is the official patent grant under 35 U.S.C. 153. For more information, please visit https://www.uspto.gov/electronicgrants

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,130	10/01/2024	12107587	00287-0016	3228

1912 7590 09/11/2024

AMSTER, ROTHSTEIN & EBENSTEIN LLP
405 LEXINGTON AVENUE
FLOOR 48
NEW YORK, NY 10174

ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at https://patentcenter.uspto.gov/. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

The USPTO is implementing electronic patent issuance with a transition period, during which period the USPTO will mail a ceremonial paper copy of the electronic patent grant to the correspondence address of record. Additional copies of the patent (i.e., certified and presentation copies) may be ordered for a fee from the USPTO's Certified Copy Center at https://certifiedcopycenter.uspto.gov/index.html. The Certified Copy Center may be reached at (800)972-6382.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 117 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Center (https://patentcenter.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PATENT CENTER site https://patentcenter.uspto.gov for additional inventors):

Nima Badizadegan, Salem, NH;

APPLICANT(s) (Please see PATENT CENTER site https://patentcenter.uspto.gov for additional applicants):

HFT Solutions, LLC, New Canaan, CT;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/723,130	**08/27/2024 05:07:17 PM Z ET**	**00287-0016**

Title of Invention

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3228	FILED BY	Victoria GILMORE
PATENT CENTER #	66948204	FILING DATE	04/18/2022
CUSTOMER #	1912	FIRST NAMED INVENTOR	Nima Badizadegan
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Benjamin Halpern

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
16-PTOL-85.pdf	1	Issue Fee Payment (PTO-85B)	163 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
16-PTOL-85.pdf	C75364A5DB05FB8CD631753651C1E4BD6820D6A3E5BFAD46 8B55FA4F3DC8A94CA564CE8BF6D1D628B72CEF20081F6EC5 8E3A83CBF179E9633C1339AA92E43A79

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

1912 7590 05/30/2024
AMSTER, ROTHSTEIN & EBENSTEIN LLP
405 LEXINGTON AVENUE
FLOOR 48
NEW YORK, NY 10174

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

Benjamin M. Halpern	(Typed or printed name)
/Benjamin M. Halpern/	(Signature)
August 27, 2024	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,130	04/18/2022	Nima Badizadegan	00287-0016	3228

TITLE OF INVENTION: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0.00	$0.00	$480	08/30/2024

EXAMINER	ART UNIT	CLASS-SUBCLASS
BURD, KEVIN MICHAEL	2632	375-219000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Amster, Rothstein & Ebenstein LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: HFT Solutions, LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): New Canaan, CONNECTICUT

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☑ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☑ Electronic Payment via the USPTO patent electronic filing system ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 011785

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Benjamin M. Halpern/ Date August 27, 2024

Typed or printed name Benjamin M. Halpern Registration No. 46,494

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/723,130	**08/27/2024 05:07:17 PM Z ET**	**00287-0016**

Title of Invention

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3228	FILED BY	Victoria GILMORE
PATENT CENTER #	66948204	AUTHORIZED BY	Benjamin Halpern
CUSTOMER #	1912	FILING DATE	04/18/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Nima Badizadegan

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 1051	**E20248QH08095306**	**Victoria GILMORE**

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2501	UTILITY ISSUE FEE	480.00	1	480.00
			TOTAL AMOUNT:	**$480.00**

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

1912 7590 05/30/2024

AMSTER, ROTHSTEIN & EBENSTEIN LLP
405 LEXINGTON AVENUE
FLOOR 48
NEW YORK, NY 10174

EXAMINER	
BURD, KEVIN MICHAEL	
ART UNIT	PAPER NUMBER
2632	

DATE MAILED: 05/30/2024

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,130	04/18/2022	Nima Badizadegan	00287-0016	3228

TITLE OF INVENTION: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0.00	$0.00	$480	08/30/2024

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

1912 7590 05/30/2024
AMSTER, ROTHSTEIN & EBENSTEIN LLP
405 LEXINGTON AVENUE
FLOOR 48
NEW YORK, NY 10174

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,130	04/18/2022	Nima Badizadegan	00287-0016	3228

TITLE OF INVENTION: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0.00	$0.00	$480	08/30/2024

EXAMINER	ART UNIT	CLASS-SUBCLASS
BURD, KEVIN MICHAEL	2632	375-219000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via the USPTO patent electronic filing system ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,130	04/18/2022	Nima Badizadegan	00287-0016	3228

1912 7590 05/30/2024

AMSTER, ROTHSTEIN & EBENSTEIN LLP
405 LEXINGTON AVENUE
FLOOR 48
NEW YORK, NY 10174

EXAMINER	
BURD, KEVIN MICHAEL	
ART UNIT	**PAPER NUMBER**
2632	

DATE MAILED: 05/30/2024

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/ owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013).
https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf

Routine uses of the information in this record may include disclosure to:

1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
2) a federal, state, local, or international agency, in response to its request;
3) a contractor of the USPTO having need for the information in order to perform a contract;
4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;
5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;
6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;
7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;
8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));
9) the Office of Personnel Management (OPM) for personnel research purposes; and
10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Notice of Allowability	Application No. 17/723,130	Applicant(s) Badizadegan, Nima	
	Examiner KEVIN M BURD	Art Unit 2632	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the after final amendment filed 5/14/2024.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-12 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/KEVIN M BURD/
Primary Examiner, Art Unit 2632

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Response to Arguments

1. The after final amendment is approved. The amendment is consistent with the claim 1 submitted on 1/23/2024 though the canceled phrase was not indicated as cancelled in the previous claims.

2. Applicant's representative has pointed out the difference between claim 1 of US 11,575,381 and claim 8 of the instant application on page 17 of the remarks. This difference has overcome the previous statutory double patenting rejection of claim 8. The statutory double patenting rejection is withdrawn.

3. The terminal disclaimer received 5/14/2024 has been reviewed and approved. This terminal disclaimer has overcome the previous double patenting rejections. The previous double patenting rejections are withdrawn in view of the terminal disclaimer.

4. Regarding the rejection of claim 1, applicant's representative provided arguments stating Zheng does not disclose converting the second plurality of parallel data streams by a serializer into a second serial data stream on pages 11-12 of the remarks. An Affidavit stating the opinion of James M. Knox PhD was filed on 5/14/2024. Points 25-31 recite Dr. Knox opinion that the K delayed parallel data streams 240 are different data streams than the K delayed parallel data streams 242 that are provided to the transmitter circuit 207 (the serializer) (25) and since the K delayed parallel data signals 242 and the K parallel data signal 240 are different data streams, the K parallel data

streams 240 generated by the demux 206 are not the same K delayed parallel data streams 242 provided to the transmitter circuit 207 that the examiner identifies as the serializer in claim 1 (30). The examiner agrees to this claim interpretation of these recited limitations. The limitations of the generation of the second plurality of parallel data streams by the computation circuitry and the converting of the second plurality of parallel data stream, by a serializer, into a second serial data stream as recited in claim 1 requires that the second plurality of parallel data streams cannot be changed in any manner from being generated and output from the computational circuitry and being input and converted to the second serial data stream in the serializer. If any changes were to occur to the second plurality of parallel data streams, the signals would be different from the second plurality of parallel data streams generated in and output from the computational circuitry. These changes would include changes to timing, delay, phase, frequency, amplitude or magnitude or any alteration to the second plurality of parallel data streams generated by and output from the computational circuity that makes the data streams different while providing the second plurality of parallel data streams to the serializer to convert the second plurality of parallel data streams to the second serial data streams. Any changes would make the second parallel data streams different and not the same.

5. Regarding the rejection of claim 1, applicant's representative provides arguments stating Zhang uses clock domain crossing operations that delay processing of the first set of parallel data streams on pages 13-14 of the remarks. An Affidavit stating the opinion of James M. Knox PhD was filed on 5/14/2024. Points 32-39 recite Dr. Knox opinion that the clock domain crossing operations are operations on the data used to

pass the data between clock domains that add latency above and beyond the phase difference between the transmitter side clock and the receiver side clock signal . Asynchronous FIFO use clock domain operations since they use a memory write, a memory read and a synchronous operation that adds latency associated with a synchronizer above and beyond the phase difference between the transmitter side clock signal and receiver side clock signal (33) and the operation of FIFO in Zhang is consistent with the definition of a clock domain crossing operations discussed above (39).

In the previous interviews conducted 11/14/2023 and 2/28/2024, the examiner indicated he was unsure of the scope of the wherein clause limitation of claim 1, "wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams". The example provided in the final office action mailed 2/1/2024 recited "For example, Zhang does not utilize a plurality of serial FIFO buffers in FIFO buffer 232 of figure 6. Since a plurality of FIFO buffers are not utilized, Zhang does not use the clock domain crossing operations that delay processing of a set of parallel data streams that would be present in the second or third or more FIFO buffers if a plurality of buffers were taught in Zhang." As stated on pages 3-4 of the final office action. Said another way, Zhang discloses using the FIFO buffer of figure 6, which would use clock domain crossing operations but does not use clock domain crossing operations that delay processing of the first set of parallel data streams in a second or third or more FIFO buffers that could be present if a plurality of serial FIFO buffers were utilized. The examiner agrees to the claim interpretation set forth in applicant's representative's remarks and the affidavit stating the opinion of Dr. Knox,

that Zheng discloses using the FIFO buffer of figure 6, which uses clock domain crossing operations and therefore does not teach "wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams". No use of clock domain crossing operations can be present in the method recited in claims 1-12. The examiner further agrees to the claim interpretation set forth in applicant's representative's remarks and the affidavit stating the opinion of Dr. Knox, that the definition of "clock domain crossing operations" of claim 1 is "operations on the data used to pass the data between clock domains that add latency above and beyond the phase difference between the transmitter side clock and the receiver side clock signal . Asynchronous FIFO use clock domain operations since they use a memory write, a memory read and a synchronous operation that adds latency associated with a synchronizer above and beyond the phase difference between the transmitter side clock signal and receiver side clock signal".

6. Regarding the rejection of claim 1, applicant's representative states "during the February 28, 2024 interview, the examiner alleged that this motivation to modify Zhang can be found in *What is an FPGA? – Design Support, DSL,*" as stated on page 14-16 of the remarks. However, the examiner said in the interview that when the examiner does a google search on "advantages" and fpga" the first item that comes up is this reference that states "the main advantage of a FPGA over the equivalent discrete circuit or an application specific IC (ASIC) is the ability to easily change its functionality after a product has been designed. In addition, FPGA requires smaller board space and can be more energy efficient than the equivalent discrete circuit." This reference was not utilized in the previous rejections of the claims. This reference was provided in an

interview with applicant's representative as an example of the types of references that were available that shows the advantages of the use of field programable gate arrays. The examiner also indicated that the advantages and disadvantages of using a FPGA would have to be weighted by a designer to determine if the net result would be helpful in the implementation of a system. The examiner has review applicant's representative's arguments and the Affidavit stating the opinion of James M. Knox PhD that was filed on 5/14/2024. The examiner disagrees that the examiner failed to provide proper motivation and that Cho teaches away from the applicant's invention for the reasons stated in the previous office actions and interviews.

7. The claim interpretation of the limitations as stated above has overcome the previous rejections of the claims. Claims 1-12 are allowed for the reasons stated below.

Allowable Subject Matter

8. Claims 1-12 are allowed.

9. The following is an examiner's statement of reasons for allowance: None of the cited references disclose each and every limitation recited in the claims. The limitations of the generation of the second plurality of parallel data streams by the computation circuitry and the converting of the second plurality of parallel data stream, by a serializer, into a second serial data stream as recited in claim 1 requires that the second plurality of parallel data streams cannot be changed in any manner from being generated and output from the computational circuitry and being input and converted to the second serial data stream in the serializer. If any changes were to occur to the second plurality of parallel data streams, the signals would be different from the second

plurality of parallel data streams generated in and output from the computational circuitry. These changes would include changes to timing, delay, phase, frequency, amplitude or magnitude or any alteration to the second plurality of parallel data streams generated by and output from the computational circuity that makes the data streams different while providing the second plurality of parallel data streams to the serializer to convert the second plurality of parallel data streams to the second serial data streams. Any changes would make the second parallel data streams different and not the same. The examiner agrees to the claim interpretation set forth in applicant's representative's remarks and the affidavit stating the opinion of Dr. Knox, that Zheng discloses using the FIFO buffer of figure 6, which uses clock domain crossing operations and therefore does not teach "wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams". No use of clock domain crossing operations can be present in the method recited in claims 1-12. The examiner further agrees to the claim interpretation set forth in applicant representative's remarks and the affidavit stating the opinion of Dr. Knox, that the definition of "clock domain crossing operations" of claim 1 is "operations on the data used to pass the data between clock domains that add latency above and beyond the phase difference between the transmitter side clock and the receiver side clock signal . Asynchronous FIFO use clock domain operations since they use a memory write, a memory read and a synchronous operation that adds latency associated with a synchronizer above and beyond the phase difference between the transmitter side clock signal and receiver side clock signal".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. BURD whose telephone number is (571)272-3008. The examiner can normally be reached 9:30 - 5:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197

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Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KEVIN M BURD/
Primary Examiner, Art Unit 2632
5/20/2024

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,130	Badizadegan, Nima
	Examiner	Art Unit
	KEVIN M BURD	2632

CPC - Searched*		
Symbol	**Date**	**Examiner**
H03L7/085;	10/24/2023	KMB
H03K19/1774	10/24/2023	KMB
H04B 1/40	10/24/2023	KMB
H03M 9/00	10/24/2023	KMB
G06F13/4291	10/24/2023	KMB
H03L7/085;	01/31/2024	KMB
H03K19/1774	01/31/2024	KMB
H04B 1/40	01/31/2024	KMB
H03M 9/00	01/31/2024	KMB
G06F13/4291	01/31/2024	KMB
H03L7/085	05/16/2024	KMB
H03K19/1774	05/16/2024	KMB
H04B 1/40	05/16/2024	KMB
H03M 9/00	05/16/2024	KMB
G06F13/4291	05/16/2024	KMB

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**
	10/24/2023	KMB

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
375	219	10/24/2023	KMB
375	219	1/31/2024	KMB
375	219	05/16/2024	KMB

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,130	Badizadegan, Nima
	Examiner	Art Unit
	KEVIN M BURD	2632

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
search search	10/24/2023	KMB
inventor name search	10/24/2023	KMB
NPL (google) search	10/24/2023	KMB
updated inventor name search	01/31/2024	KMB
updated inventor name search	05/16/2024	KMB
NPL (google) search	05/16/2024	KMB
search search	05/16/2024	KMB

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
375	219	05/16/2024	KMB
H03L	7/085	05/16/2024	KMB
H03K	19/1774	05/16/2024	KMB
H04B	1/40	05/16/2024	KMB
H03M	9/00	05/16/2024	KMB
G06F	13/4291	05/16/2024	KMB

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,130	Badizadegan, Nima
	Examiner	**Art Unit**
	KEVIN M BURD	2632

CPC						
Symbol					**Type**	**Version**
H03L	/	7	/	085	F	2013-01-01
H03K	/	19	/	1774	I	2013-01-01
H03M	/	9	/	00	I	2013-01-01
G06F	/	13	/	4291	I	2013-01-01
H04B	/	1	/	40	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/KEVIN M BURD/ Primary Examiner, Art Unit 2632	20 May 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3A

U.S. Patent and Trademark Office — Part of Paper No.: 20240516

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,130	Badizadegan, Nima
	Examiner	**Art Unit**
	KEVIN M BURD	2632

INTERNATIONAL CLASSIFICATION					
CLAIMED					
H03L	/	7	/	08	
NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
375	219

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 12	
/KEVIN M BURD/ Primary Examiner, Art Unit 2632 (Primary Examiner) 20 May 2024 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3A

U.S. Patent and Trademark Office Part of Paper No.: 20240516

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,130	Badizadegan, Nima
	Examiner	**Art Unit**
	KEVIN M BURD	2632

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10												
	2		11												
	3		12												
	4														
	5														
	6														
	7														
	8														
	9														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/KEVIN M BURD/ Primary Examiner, Art Unit 2632	20 May 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3A

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Google fpga no clock domain crossing operations parall Sign in

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Advanced Micro Devices
https://support.xilinx.com › question › question-about-ki...

Question about Kintex Ultrascale GTH Receiver clock domain

Sep 2, 2021 — In my understanding, there are three different clocks, SPIO parallel clock, XCLK, and RXUSRCLK. Phase alignment always(no matter whether the RX ...

Conversion of **parallel** to **serial** and then **serial** ... - Xilinx Support Mar 6, 2015
Clock Domain Crossing data register example - Xilinx Support Jan 19, 2017
More results from support.xilinx.com

Journal of Communications
https://www.jocm.us › opicedfile PDF

A Method of Serial Data Clock Domain Crossing ...

by FS Yan · 2015 · Cited by 4 — parallel-to-serial conversion registers and two 1-bit registers, which do data conversion directly without other registers engaging, based ...

Google Patents
https://patents.google.com › patent

FPGA-based serial signal clock synchronization method ...

FPGA-based serial signal clock synchronization method, serial-to-parallel conversion clock domain accurately, and then convert it into parallel signal through ...

Digilent Forum
https://forum.digilent.com › ... › FPGA

Serial To Parallel Conversion Testing - FPGA

Feb 10, 2015 — Hello Everyone, I actually wrote a code for serial to parallel conversion but when I am trying to test it, I am getting no results.
1 answer · Top answer: Hi, You can generate 49 MHz clock frequency using DCM/PLL and yo...
Missing: domain crossing operations

People also ask

What is clock domain crossing in FPGA?

What is a serial to parallel converter?

What is a high speed serial link SerDes?

What is a clock domain techniques for crossing?

Feedback

AMD
https://docs.amd.com › 2021.2-English › Parallel-to-Serial

Parallel to Serial - 2021.2 English

The Parallel to Serial block takes an input word and splits it into N time-multiplexed output words where N is the ratio of number of input bits to output bits.
Missing: no crossing

AMD
https://www.xilinx.com › archives › books › serialio PDF

High-Speed Serial I/O Made Simple

by A Athavale · Cited by 96 --- ... parallel-to-serial conversion, serial-to- parallel conversion, and clock data recovery. Parallel-to-Serial Conversion. There are two main methods of parallel ...

210 pages

Journal of Communications
https://www.joem.us › ...

A Method of Serial Data Clock Domain Crossing ...

... FPGA/CPLD. This method changes the usage mode of several simple serial-to-parallel and parallel-to-serial converting registers in original design to convert ...

NI Community
https://forums.ni.com › LabVIEW › td-p

Advanced FPGA: Clock Crossing efficiency - NI Community

Jun 3, 2016 --- We have FPGA code which does different operations at several different clock frequencies. We have 8MHz, 10MHz, 50MHz, 80MHz, 128MHz and ...

convert parallel to **serial** - NI Community - National Instruments Jan 13, 2014
Crossing Clock Domains in the **FPGA** Examples - NI Community Nov 16, 2014
Solved: **Parallel** to **serial** convertor using the 74166 in multisim Mar 4, 2023
More results from forums.ni.com

Missing: parallel convert

ResearchGate
https://www.researchgate.net › publication › 28386227...

A Method of Serial Data Clock Domain Crossing ...

This paper designs a high-speed data acquisition system based on a field-programmable gate array (FPGA). The system has the advantages of configurable data ...

Intel
https://www.intel.com › articles › 000080400.html

How do I constrain my clock domain crossing?

It is essential to apply timing constraints to your multibit clock domain crossing. If this bus has a set_false_path constraint then the skew across the bus ...

Related searches

Fpga no clock domain crossing operations parallel...	**gth transceiver user guide**
Fpga no clock domain crossing operations parallel...	**xilinx transceivers**
high-speed serdes design pdf	**xilinx gtx transceiver**
serdes cdr tutorial	

EEVblog
https://www.eevblog.com › forum › picking-a-core-fre...

Picking a "core frequency" for a FPGA

Jun 22, 2020 --- You're not limited to just one clock either, most FPGAs ... clock with DDR serial output ... clocks (besides having clock domain crossing circuitry) ...

UTAR Institutional Repository
http://eprints.utar.edu.my › fyp_CT__2022_LKY PDF

CLOCK DOMAIN CROSSING DESIGN FOR 5-STAGE ...

by KY Leong · 2022 --- It is the device that will convert the incoming parallel data into serial form which can be transmitted on a communication line. UART is ...

126 pages

Forum for Electronics
https://www.edaboard.com › threads › parallel-to-serial-c...

parallel to serial converter

Mar 7, 2008 — Care has to be taken as to see that the shifting is done exactly for eight bits and the ready signal comes every 8th clock cycle. If the ready ...

Missing: domain crossing

Semiconductor Engineering
https://semiengineering.com › ... › Verification

Clock Domain Crossing (CDC)

Clock Domain Crossings in the FPGA World. Published on ... without the cost of FPGAs. Emulation. Special ... The transceiver converts parallel data into serial ...

Linkedin · Microchip USA
7 reactions · 1 month ago

Microchip USA posted on the topic

FPGAs are transforming hardware design with their flexibility and customization options. These devices empower developers to create tailored ...

Reddit · r/FPGA
30+ comments · 6 years ago

Some Simple Clock-Domain Crossing Solutions : r/FPGA

For these two domain crossings, the synthesizer, map, and place and route tools need to know how long of a propagation delay is acceptable.

Missing: operations convert

ResearchGate
https://www.researchgate.net › publication › 34914813...

AXI Based Three 8-bit Parallel Input to One Serial Output ...

AXI Based Three 8-bit Parallel Input to One Serial Output Converter with Priority Management System and Asynchronous Clocks at Input and Output.

CERN Document Server
https://cds.cern.ch › record › files › gefile [PDF]

Development of FPGA-based High-Speed serial links for ...

by S Perrella · Cited by 4 — 2.5 serial to parallel and parallel to serial conversion ... Synchronization clock signals for the serial and parallel domains are generated by ... (XCLK)...

FPGAkey
https://www.fpgakey.com › tutorial › chapter184

Chapter 11: Getting Data In and Out with I/O and SerDes

... Crossing Clock Domains · Chapter 8: The State ... operations in FPGA ... It converts parallel data into a serial stream for transmission and deserializes incoming ...

Electrical Engineering Stack Exchange
https://electronics.stackexchange.com › questions › can...

Can someone give me some ideas concerning the logic of ...

Aug 29, 2017 — ... FPGA are phase- and clock-locked may not be a simple task. ... clock rate is the far end operating ... Just do a straight parallel to serial ...

3 answers · 1 vote: Once I can get the FPGA's clocks to be locked together Rather than do thi...

Missing: domain crossing

Nandland
https://nandland.com › lesson-14-crossing-clock-domains

Crossing Clock Domains in an FPGA

Jun 30, 2022 — Dealing with Metastability and Timing Errors ... Crossing clock domains inside of an FPGA is a common task, but it is one that many digital ...

EEVblog
https://www.eevblog.com › forum › microcontrollers

Interface FPGA woth laptop

Jun 23, 2016 — ... parallel bus. Cypress ... Using an FPGA UART also solves quite a few clock domain crossing issues. ... So, use a off-the-self USB-to-serial ...

Microchip Technology
https://ww1.microchip.com › FPGA › UserGuide PDF

PolarFire FPGA and PolarFire SoC FPGA User I/O ...

I/O gearing handles serial-to-parallel and parallel-to-serial conversion of multiple FPGA fabric signals to and from a single device I/O based on user clock ...

AMD
https://docs.amd.com › en-US › Coding-Shift-Registers-a

Coding Shift Registers and Delay Lines - 2023.2 English

No Clock and Unconstrained Internal Endpoints · Generated ... Limiting Synchronous Clock Domain Crossing Paths ... Serial or parallel output. AMD devices contain ...

ZipCPU
https://zipcpu.com › blog › 2017/10/20 › cdc

Some Simple Clock-Domain Crossing Solutions

Oct 20, 2017 — In many ways, metastability is the big boogeyman within FPGA design. It is hard to see when desk-checking a design, it doesn't show up on ...

Катедра Радиокомуникации и видеотехнологии
http://rcvt.tu-sofia.bg › ICEST2008_148 PDF

A Simple FPGA/PLL Based Protocol Converter for Serial ...

In full mode of operation the converter accepts serial data ... word from internal register to output parallel/serial ... [2] Cadence technical paper, "Clock domain ...

Justia
https://patents.justia.com › patent

Field programmable gate array with external phase-locked loop

In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

Analog Devices
https://www.analog.com › technical-articles PDF

JESD204B Survival Guide

The standard describes a multigigabit serial data link between converter(s) and a receiver, commonly a device such as an FPGA or ASIC. In this original version ...

BYU ScholarsArchive
https://scholarsarchive.byu.edu › cgi › viewcontent PDF

Synchronization Voter Insertion Algorithms for FPGA ...

by JM Johnson · 2010 · Cited by 16 — The sampling uncertainty inherent in clock domain crossing synchronizers is normally not an issue, but becomes an issue when TMR is used ...

Images

How to implement a Parallel t... — Surf-VHDL

Clock Domain Crossing data r... — Xilinx Support - AMD

fpga - Clock Dividers with Cl... — Electronics Stack Exchange

Feedback

6 more images

More results

Optiver Ex1002
Page 31 of 459

Optiver Ex1002
Page 32 of 459

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L213	6	"8873606".pn. "20180027431"	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 09:11 AM
L214	1	213 AND asic	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 10:32 AM
L215	3	213 AND circuit$1	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 10:32 AM
L216	2	"11575381".pn.	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 10:37 AM
L217	659	discrete near4 circuit SAME MHZ	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 11:02 AM
L218	32	discrete near4 circuit SAME "500" ADJ MHZ	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 11:02 AM
L222	21	programabl$5 WITH timing near4 circuit$1	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 11:03 AM
L223	1	re-programabl$5 WITH timing near4 circuit$1	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 11:04 AM
L224	1	re-programabl$5 WITH timing near4 circuit$1	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 11:04 AM
L225	9	eeprom near5 retimer$1	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 11:04 AM
L226	4	"11018678".pn.	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 11:09 AM
L228	0	213 AND die	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 11:18 AM
L229	9	((("BADIZADEGAN") near3 ("Nima"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 11:20 AM
L230	3	((("HFT") near3 ("SOLUTIONS") near3 ("LLC"))).AS,AANM.	(US-PGPUB; USPAT)	OR	ON	ON	2024/05/16 11:20 AM
L231	46	181 AND (((deserializ$5 OR (serial ADJ parallel)) SAME (serializ$5 OR (parallel ADJ serial))) SAME phase near3 detect$5)	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	OFF	OFF	2024/05/16 11:25 AM

L232	18	((receiv$4 OR recept$5) near4 clock$1) WITH ((transmit$5 OR transmission$5) near2 clock$1) WITH phase near5 detect$6 SAME (serializer$1 OR (serial ADJ parallel) OR "s/p")	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 11:41 AM
L233	63	157 AND pll	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/16 11:41 AM
L234	113	L148 L149	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	OFF	OFF	2024/05/16 11:41 AM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: HFT Solutions, LLC	Confirmation No.: 3228
Application No.	: 17/723,130	
Filed	: April 18, 2022	
For	: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	
TC/A.U.	: 2632	
Examiner	: Kevin Michael Burd	
Docket No.	: 00287-0016	
Customer No.	: 01912	

Please enter the after final amendment.

/K.M.B/ 05/16/2024

RESPONSE TO FINAL OFFICE ACTION DATED FEBRUARY 1, 2024

Via Patent Center
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This is a response to the Final Office Action dated February 1, 2024. A response to the Final Office Action is due May 1, 2024. Applicant submits herewith a petition for a one-month extension of time such that the present Amendment is being timely filed.

Amendments to the claims begin on page **2**.

Remarks begin on page **5**.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/723,130	05/14/2024 04:58:29 PM Z ET	00287-0016

Title of Invention

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3228	FILED BY	Victoria GILMORE
PATENT CENTER #	65524518	AUTHORIZED BY	Keith Barkaus
CUSTOMER #	1912	FILING DATE	04/18/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Nima Badizadegan

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 1051	E20245DG59245381	Victoria GILMORE

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2251	EXTENSION FOR RESPONSE WITHIN FIRST MONTH	88.00	1	88.00
			TOTAL AMOUNT:	$88.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: HFT Solutions, LLC	Confirmation No.: 3228
Application No.	: 17/723,130	
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For	: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	
TC/A.U.	: 2632	
Examiner	: Kevin Michael Burd	
Docket No.	: 00287-0016	
Customer No.	: 01912	

Declaration under 37 C.F.R. § 1.132 of Expert James M. Knox, Ph.D.

I, **James M. Knox**, declare:

1. My name is James M. Knox, Ph.D. and I am the owner of Trisoft, a developer of custom designed electronic hardware/software systems and equipment. I submit this declaration in support of Applicant. Unless otherwise indicated, I have personal knowledge of all the facts set forth herein.

Scope of Assignment

2. I have been asked to provide my opinion regarding the patentability of the attached claims as set forth in Exhibit A hereto in view of the current rejection thereof in the Final Office Action dated February 1, 2024 in the above pending United States patent application.

3. In forming my opinion, I reviewed:

   a. the present application,

   b. the pending claims as set forth in **Exhibit A** hereto,

   c. the prosecution history of the present application, including:

      i. the final office action mailed February 1, 2024; and

ii. The Interview Summary dated February 29, 2024 regarding the February 28, 2024 telephone interview between applicants' representative and the Examiner and Applicant's summary of that interview as included in the response being filed herewith;

4. the prior art identified in the February 1, 2024 Office Action, including:

iii. U.S. Patent No. 8,873,606 to Zhang et al. (US 8,873,606);

iv. U.S. Patent Application Publication No. 2018/0027431 to Cho et al.; and

v. the article *What is an FPGA? – Design Support,* DSL, https://www.dsl-ltd.co.uk/support/fpga/ (attached as **Exhibit C** hereto, which I am informed was identified by the Examiner in the February 28, 2024 telephone interview).

Background and Experience

5. A copy of my Curriculum Vitae is attached as Exhibit B hereto.

6. I received a Bachelor's degree in Electrical Engineering from the University of Texas in 1969, a Master's degree in Computer Science from the University of Texas in 1971, and a Ph.D. in Electrical Engineering from the University of Texas in 1978.

7. At the University of Texas, I studied and took courses in areas relating to computer networking and computer communications. I also studied and took numerous courses dealing with electronics, electronic components, and electrical circuits. I taught Electrical Engineering and Computer Science at the University of Texas, including courses involving the design, use, and programming of microprocessors and embedded microprocessor systems. These courses included the techniques for communicating over memory and I/O channels to remote devices, as well as the design and use of localized components such as A/D converters and digital switches.

8. My work experience in the computer hardware and software design field included the design and implementation of numerous electronic and data communication systems. I designed microprocessors at the transistor circuit level (including designing algorithmic structures within the microprocessor), and developed and implemented their use in land-based, sea-based,

air-based, and deep space applications. I have designed many digital communication networks. I have analyzed and am familiar with the internal components of telecommunication networks (e.g., ISDN) and data networks (e.g., Ethernet networks). I have offered my opinion in several legal cases involving computer and network hardware and software, including microprocessors and custom ASICs,, and have qualified as an expert and testified in court about such technologies.

9. I am currently the owner of a computer technology company called TriSoft, located in Austin, Texas. TriSoft is involved in the research and development of unique electronic systems and components. I consult in projects involving remote power delivery, embedded microprocessor system design, and data communications, to name a very small subset.

10. I am intimately familiar with the subject matter of the present application, namely, field programmable gate array systems generally as well as their use in high-speed applications. I have designed systems and integrated circuits involving a range of such custom chips, including:

- Application Specific Integrated Circuits (ASIC) for the B1 Bomber and other military programs
- Programmable Logic Arrays (PLA) for military submarine and Global Positioning System (GPS) applications
- Field Programable Logic Arrays (FPGA) for prototype and rapid response systems, and for systems requiring field updates. Of particular note, these include:
    - Military Ground Support Equipment (GSE) for the F-22 and F-35 fighter (under contract with Lockheed and Northrup-Gruman)
    - Prototype Air Data and Aircraft Heading Reference System (ADAHRS)
    - Initial design – GAMI PRISM ignition system
    - Prototype replacement for Mitchel/Edo-Aire Autopilot

  Developments included primarily (but not exclusively) Xilinx and AMD FPGA chips, and covered a period roughly from 1993 through 2017. Developmental languages used primarily Verilog and VHDL programming languages (although some work on Xilinx and AMD chips was performed using their own variant language).

The Claimed Invention

11. The pending claims include a single independent claim, claim 1, which is reproduced below:

> 1. A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:
>
> (a) receiving, by a deserializer in a field programmable array, a clock signal;
>
> (b) receiving, by the deserializer, the first serial data stream;
>
> (c) generating, by the deserializer, a receiver side clock signal;
>
> (d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;
>
> (e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;
>
> (f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;
>
> (g) generating, using the phase lock loop, a transmitter side clock signal;
>
> (h) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams;
>
> (i) converting the second plurality of parallel data streams, by a serializer, into a second serial data stream; and
>
> (j) transmitting, from the field programmable gate array system, the second serial data stream,
>
> wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

12. I have also reviewed the dependent claims listed in Exhibit A (but not repeated here).

Claim 1 requires converting "the" same "second plurality of serial data streams" by a "serializer" as are generated by a "computational circuitry

13. As pertinent here, steps (h) and (i) of claim 1 reads in pertinent part:

> "(h) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate **a second plurality of parallel data streams**;
>
> (i) converting **the second plurality of parallel data streams**, by a serializer, into a second serial data stream; and"

(Claim 1, steps (h), (i) (emphasis added)).

14. In my opinion, a POSITA would understand that the "second plurality of parallel data streams" in step (h) must be the same plurality of data streams in step (i). This "second plurality of parallel data streams" must both be generated "by the computational circuitry" and "convert[ed]" "by a serializer" into a second serial data stream.

15. In view of this, the output of the computational circuitry, the "second plurality of parallel data streams", in claim 1 must be the same parallel data streams converted by the serializer, and thus, cannot be further processed before being provided to the serializer as suggested by the Examiner. In my opinion, a POSITA would understand that if a "parallel data stream" is further processed, it is not the same "data stream".

16. The specification of the present application supports the view that a "processed stream" is a new stream. It describes the present invention "wherein the computational circuitry is configured to perform a first set of operations on the first plurality of parallel data streams to generate a second plurality of parallel processed data streams having a second amount of data streams;" Paragraph (11). Processing a first plurality of parallel data streams creates a second plurality of parallel processed data streams, where "processed" is just a description of what differentiates the new streams from the previous data streams.

17. There is no limitation on the amount of streams in the second plurality of parallel data streams in claim 1. It can be the same as in the first plurality of parallel data streams or change when processed. Dependent claim 9, "The method of claim 1, wherein the first plurality of data streams has the same number of data streams as the second plurality of data streams", addresses the case where the second amount is the same as the first amount.

18. Since each processing step can generate a new plurality of parallel streams there may be any number of intermediate parallel streams within the computational circuitry. However, the second plurality of parallel streams described in the claim is specifically the output that is delivered to the serializer.

Person of Skill in the Art of the Invention

19. I understand that in order to determine whether a claim is obvious, the level of ordinary skill in the art at the time of the invention must be considered. The present application was filed on April 18, 2022 and claims priority to an application filed February 21, 2019. In my opinion, a person of ordinary skill in the art (hereinafter a "POSITA") at that time would have a bachelor's degree in electrical engineering or related technology and a year of experience programming FPGAs.

The Current Rejection

20. I have reviewed the Office Action dated February 1, 2024 in the present application and understand that the Examiner has rejected claims 1-12 under 35 USC § 103 as allegedly being unpatentable over U.S. Patent No. 8,873,606 to Zhang et al. ("Zhang") in view of U.S. Patent Application Publication No. 2018/0027431 to Cho et al. ("Cho"). The Office Action contends that Zhang allegedly teaches or discloses the entirety of claim 1 except that "the method for processing a first serial data stream uses a field programmable gate array system." Office Action, pg. 3-6. To cure this deficiency, the Office Action relies on the circuit shown in Figure 2 and described in paragraph [0055] of Cho which the Examiner contends allegedly discloses "SERDES 26 may be implemented in a field programmable gate array (FPGA)." Id.

21. For the reasons set forth herein, I do not agree with the Office Action's analysis. I agree that Zhang does not disclose, show or suggest the use of an FPGA. In contrast, Zhang

discloses the use of an application-specific integrated circuit (ASIC). I do not agree that Zhang discloses, shows or suggests the remaining elements of claim 1 and I do not agree that a POSITA would have been motivated to implement the circuit shown in FIG. 6 of Zhang in an FPGA as allegedly taught in Cho.

Overview of Zhang

22. Zhang discloses a specific ASIC to provide a retimer circuit. Retimer circuits are standard devices (commonly used in PCIe systems) used to clean up high-speed serial signals traveling on noisy channels. In particular, retimer circuits are used to recover a signal and drive a new copy with noise and jitter removed.

23. The circuit illustrated in FIG. 6 of Zhang receives a serial input signal, which is amplified via amplifier 202 to provide amplified serial input signal 236 to serial-to-parallel converter 204, which provides N parallel signals (col. 6, l. 30-34, 38-44). The serial-to-parallel converter 204 may sample amplified serial data stream 236 according to receiver clock signal 250 (col. 6, l. 38-40). The N parallel signals are provided to a demux 206 to provide K parallel signals at 240 (col. 6, l. 62-65). The K parallel signals pass through a digital core 208 including FIFO 232 to provide K delayed parallel signals at 242. The digital core 208 may buffer the K parallel signals in FIFO 232 which may have a depth of K (the bit depth of the K parallel signals) (col. 7, l. 21-41). The K delayed parallel signals are delayed according to the FIFO depth and are provided to the transmitter circuit 207 (col. 7, l. 24-28). Specifically, the K delayed parallel signals may be provided to a mux 210 to provide L parallel signals (col. 8, l. 7-9). The L parallel signals are provided to parallel-to-serial converter 212 which converts them into serial output signal 246, which is sent on output signal 248 to a signal line or device. The serial converter 212 is configured to sample the L parallel signals according to the transmitter side clock signal 260 (col. 6, l. 38-40).

Zhang also explains that the digital core 208 may provide for the removal of error correction and packet protocol bits from K parallel signals 240, error correction, and/or bit stuffing as part of processing the second parallel signals 240. (col. 4, l. 36-43). As discussed later in this declaration, a POSITA would understand this circuit in Zhang is a retimer implemented by an ASIC.

24. In my opinion, a POSITA would understand that the purpose of the FIFO 232 in Zhang is to perform clock domain crossing operations between the transmitter side clock, clock 250 and the receiver side clock 260. Clock domain crossing operations are discussed in the specification of the present application and are discussed in further detail below. A POSITA would recognize that they include the buffering operations provided by the FIFO 232 of the digital core 208, which delay the K delayed parallel signals by more than the phase difference between clock 250 and clock 260.

The K parallel data streams 240 output from demux 206 are not the same K delayed parallel data streams 242 that are converted by "serializer" 212

25. I understand that the Examiner is asserting that the K parallel data streams 240 that are output from the demux 206 in Zhang are the "second parallel data streams" of steps (h) and (i) of Claim 1. In my opinion, a POSITA would understand that the K parallel data streams 240 are different data streams than the K delayed parallel data streams 242 that are provided to the transmitter circuit 207, which the Examiner characterizes as the "serializer" of claim 1.

26. As a preliminary matter, I note that although both reference numerals 240 and 242 in FIG. 6 are labeled "K"; "K" indicates the "bit width" or number of parallel data streams, and not the actual content of the data stream. Similarly, "N" and "L" also refer to a bit width or number of data streams that are running in parallel where noted. Indeed, Zang explains that the serial-to-parallel converter 204 is configured to "convert amplified analog serial input signal 236 to an N number of first parallel signals 238. Similarly, Zhang explains that the demux 206 converts "N

first parallel signals to a K number of second parallel signals 240. Zhang also explains " ...the FIFO 232 having a FIFO depth of K (i.e., the bit width of second parallel signals 240) ..." Zhang, Col. 20, ll. 21-24. Further, inclusion of the "/" through the arrows under the reference symbols "N", "K" and "L" in FIG. 6, for example designates these symbols as being representative of the number of streams or signals. This slash is a standard notation for a bus width, defined by IEEE Std. 315-1975 and ANSI Y32.2-1975 clause 3.1.2.3. I understand that this issue was discussed during the telephone interview of February 28, 2024 and the Examiner agreed that the letter "K" in FIG. 6 designates a number of parallel signals.

27. In my opinion, a POSITA reading Zhang would understand that the K parallel data streams 240 output from the demux 206 are **further processed** by the Digital Core 208 including the FIFO 232, to generate a new set of K delayed parallel data streams 242. As is discussed above, the core 208 includes at least a FIFO, which processes the data in order to retime it as it is transferred from the receiver clock side of the transceiver 200 to the transmitter clock side.

28. In particular, in Zhang, the digital core 208 receives K parallel signals 240 and generates a new set of parallel signals 242—called "delayed second parallel signals" (col. 7 lines 26-27)—delayed by the FIFO 232 in a clock domain crossing operation (col. 7 lines 20-27). The delayed second parallel signals 242, not the second parallel signals 240, are then provided to the serializer 207 (col. 8 lines 8-9).

29. In my opinion, a POSITA would understand that the K parallel data streams 240 output by demux 206 (which the Examiner alleges corresponds to the "computational circuitry" of claim 1) are different data streams than the K delayed parallel data signals 242 that are the input of mux 210 of the transmitter 207 (which the Examiner alleges corresponds to the "serializer" of claim 1).

30. Since the K delayed parallel data signals 242 and the K parallel data signal 240 are different data streams, the K parallel data signals 240 generated by the demux 206 **are not the same** K delayed parallel data streams 242 provided to the transmitter circuit 207 that the examiner identifies as the "serializer" in claim 1.

31. Thus, in my opinion, a POSITA would understand that, given the examiner's identification of K parallel data signals 240 as the second parallel data streams, Zhang does not disclose "converting **the second plurality of parallel data streams**, by a serializer, into a second serial data stream," since the K parallel data signals 240 in FIG. 6 of Zhang are not even provided to the transmitter circuit 207 which the Examiner contends is the "serializer" of claim 1. Nor are the K parallel data signals 240 provided to the parallel to serial converter 212.

FIFO 232 in the Digital Core 208 of Zhang Performs "Clock Domain Crossing Operations"

32. I understand, during a telephone interview that took place on November 14, 2023, the Examiner indicated that he was unclear of the meaning of the term "clock domain crossing operations." In the subsequent Interview Summary dated November 15, 2023, the Examiner indicated that "the term clock domain crossing operations was not defined in the claim and [he] was unsure what the scope of the wherein clause limitation of claim 1 is." The Examiner further noted it was unclear to him "which operations were excluded."

33. In an Amendment filed January 23, 2024, Applicant provided the following definition of "clock domain crossing operations" as used in claim 1 as follows:

> With respect to the Examiner's concerns regarding the scope of the term "clock domain crossing operations" in claim 1, Applicant notes that, as used in claim 1, ***"clock domain crossing operations" are operations on the data used to pass the data between clock domains that add latency above and beyond the phase difference between the transmitter side clock signal and the receiver side clock signal.***

> Support for this explanation can be found at least in Paragraph [0291] of the present application which discusses examples of clock domain crossing circuits, which use clock domain crossing operations, including "an asynchronous FIFO" such as the FIFO 232 used in Zhang, for example. Such an asynchronous FIFO includes operations (e.g. a memory write, a memory read, and a synchronization operation) that add latency associated with a synchronizer above and beyond the phase difference between the transmitter side clock signal and the receiver side clock signal.

January 23, 2024 Response, at 6 (*emphasis added*).

34. Applicant further noted in the January 23, 2024 Amendment that the above definition was based on the specification of the present application. In particular, Applicant noted that support for this explanation can be found at least in Paragraph [0291] of the present application which discusses examples of clock domain crossing circuits, which perform clock domain crossing operations, including "an asynchronous FIFO" such as the FIFO 232 used in Zhang, for example. Such an asynchronous FIFO includes operations (e.g. a memory write, a memory read, and a synchronization operation) that add latency associated with a synchronizer above and beyond the phase difference between the transmitter side clock signal and the receiver side clock signal.

35. I have reviewed Paragraph [0291] and agree with Applicant that it discusses exemplary clock domain crossing circuits which I understand perform clock domain crossing operations. I also agree with Applicant that this portion of the present specification identifies "an asynchronous FIFO" as an example of a clock domain crossing circuit, which I understand performs clock domain crossing operations.

36. The Applicant pointed out that the FIFO 232 of Zhang is an asynchronous FIFO. I agree with the Applicant's characterization of the FIFO 232 in Zhang as an asynchronous FIFO, which is also an example of a clock domain crossing circuit. The Applicant further pointed out the "an asynchronous FIFO includes operations (e.g. a memory write, a memory read, and a synchronization operation) that add latency associated with a synchronizer above and beyond the

phase difference between the transmitter side clock signal and the receiver side clock signal." I agree with this position as well.

37. In my opinion, a POSITA reviewing the specification of the present application, including Paragraph [0291] would understand and agree with the description of the term "clock domain crossing operations" as used in claim 1 proffered by Applicant in the January 23, 2023 Amendment .

38. My opinion is based both on the description of this term provided in the present application and my experience in the industry. In my experience, clock domain crossing operations are a broad category of operations that delay data to safely pass said data from one clock domain to another. A clock domain crossing typically uses memory reads and writes to pass data between the clock domains and uses synchronizers to indicate the presence of data. These operations add latency above and beyond the phase difference between the two clocks.

39. Further, in my opinion, FIFO 232 of Zhang meets this definition. As an initial matter, as noted above, the specification of the present application explicitly lists "an asynchronous FIFO" as an example of a clock domain crossing circuit, which performs clock domain crossing operations. Thus, at the very least, the "clock domain crossing operations" recited in claim 1, include operations performed by a FIFO. Further, the FIFO 232 described in Zhang performs operations that fall under the definition of "clock domain crossing operations" proffered by Applicant and described in the specification at Paragraph [0291] for example. FIFO 232 has a write clock that is in a separate clock domain than the read clock. FIFO 232 buffers signals (col. 7 lines 21-25), resulting in a delayed version of those signals. The buffering is done to tolerate a phase offset between the clock signals (col. 13 lines 23-34) while avoiding errors. Since the clock phases are no more than 360 degrees apart, the phase difference between the transmitter and

receiver side clock signal results in a delay equal to a fractional clock cycle. However, the FIFO 232 is a buffer that holds multiple cycles of data at a time, resulting in a delay of more than one clock cycle. The FIFO 232 passes data between clock domains (col. 13 lines 24-25), and by buffering data, adds latency above and beyond the phase difference, delaying the data going through the digital core 208 (col. 7 lines 24-25). Thus, the operation of the FIFO in Zhang is consistent with the definition of a clock domain crossing operations discussed above.

A POSITA would not be motivated to Implement the ASIC circuitry of Zhang In A FPGA as taught in Cho

40. I understand the February 1, 2024 Office Action recognizes that "Zhang does not disclose the method for processing a first serial data stream us[ing] a field programmable gate array system". Feb. 1 O.A. at 6. To rectify this fatal deficiency, the Examiner asserts it would be obvious to "implement the circuit of Zheng on an FPGA as taught by Cho". (*Id.* at 7). The Examiner's alleged motivation was that "[t]he use of FPGA to reduce the size of the circuit and improve energy efficiency of the circuit is well known." (*Id.*)

41. I understand that during the February 28, 2024 Interview, the Examiner referred to the article *What is an FPGA? – Design Support*, DSL, https://www.dsl-ltd.co.uk/support/fpga/ (attached as Exhibit A and identified in an Information Disclosure Statement that I understand will be submitted herewith) as allegedly supporting the motivation to implement the circuit of Zhang in an FPGA. This article states that "FPGA require a smaller board space and can be more energy efficient ***than the equivalent discrete circuit***". Ex. A at 2 (emphasis added).

42. In my opinion, the article cited by the Examiner fails to provide the motivation for the modification suggested by the Examiner, and, in fact, teaches away from the modification suggested by the Examiner.

43. The nature of the circuit and the operating speeds stated in the Zhang make clear that the circuit discussed therein is an ASIC and **not a discrete circuit**. Zhang describes a circuit that receives a stream at 10 Gbps which is parallelized to 20 parallel signals at 500 MHz (col. 1 lines 38-39 and col. 4 lines 12-16). Zhang discloses the low latency channel having a 4-bit signal at 2.5 GHz (col. 10 lines 46-48). As would have been well known to a POSITA at the time of the invention, a 500 MHz or higher clock rate is unrealistic for discrete circuits.

44. A POSITA at the time of the invention would understand that the alleged advantage of FPGA's over discrete circuits set forth in the article relied on by the Examiner is not relevant with respect to modifying Zhang, which is ***not a discrete circuit***.

45. In my opinion. a POSITA would understand that there is no motivation to implement the ASIC of Zhang using an FPGA like Cho. Indeed, a POSITA would be discouraged from such a combination based on the inapplicability of the relative features of an FPGA for the problem addressed by Zhang. When compared to an ASIC implementation, an FPGA implementation of a circuit is (by nature) larger, slower, has greater unit cost and consumes more power than the ASIC.[1] The one advantage that FPGAs offer, field-programmability, is irrelevant to the retimer circuit provided by Zhang. The ASIC disclosed in Zhang offers configuration options relevant to its dedicated function as a retimer (col. 4 lines 37-40, col. 10 lines 44-45), such that additional programmability would be superfluous. Retimer circuits simply do not need field programmability such that production ASICs suit the purpose far better and are typically smaller, faster, less expensive and consume less power.

46. Zhang teaches a specific ASIC design for a retimer circuitry, as identifiable by a POSITA. As noted above, retimer circuits are standard devices (commonly used in PCIe systems)

[1] "What is an FPGA? – Design Support," section on "Disadvantages." URL: https://www.dsl-ltd.co.uk/support/fpga

used to clean up high-speed serial signals traveling on noisy channels, and are devices that recover a signal and drive a new copy with noise and jitter removed.[2] Further, as is explained above, Zhang explains that the digital core 208 may provide for the removal of error correction and packet protocol bits from K parallel signals 240, error correction, and/or bit stuffing. According to figure 6, the circuit in Zhang accepts a serial data stream on an input wire 234, passes it through a FIFO to time the data to a new clock 260, and outputs it on an output wire 248. The low-latency path in Zhang explicitly does no processing other than using the FIFO 218 to retime the data. This architecture identifies the circuit in Zhang as a retimer circuit.

47. A POSITA at the time of the invention would understand that the use of an ASIC for such circuitry makes perfect sense. Due to the speed at which they operate and the fact that they are standard building blocks for larger circuits that have high-volume demand, retimers are commonly implemented as ASICs. Zhang describes a circuit that receives a stream at 10 Gbps which is parallelized to 20 parallel signals at 500 MHz (col. 1 lines 38-39 and col. 4 lines 12-16). 500 MHz is a very high clock rate for a design implemented in an FPGA, but achievable. Furthermore, Zhang discloses the low latency channel having a 4-bit signal at 2.5 GHz (col 10 lines 46-48), which is far beyond the capabilities of any FPGA such that the circuit of Zhang cannot be implemented by an FPGA as suggested by the Examiner. For example, the Xilinx Virtex UltraScale+ FPGA, the state of the art FPGA at the time of the invention, was capable of operating at an interface clock frequency of up to 511 MHz.[3]. The nature of the circuit and the operating speeds stated in the patent indicate that Zhang is disclosing an ASIC and that implementation of

[2] "Solving PCIe Latency with Retimers and Elastic Buffers." Section on "Retimer architecture," see figure 4. URL: https://www.edn.com/a-short-primer-on-pcie-latency-and-its-optimization-with-retimers/

[3] Table 57 on page 54-55 of "Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics (DS923)". URL: https://docs.amd.com/v/u/en-US/ds923-virtex-ultrascale-plus

the circuit of Zhang in FPGA would offer no benefit and is likely technically impractical (if not impossible) due to the speed limitations of FPGAs at the time of the invention.

48. As explained above, due to the operating speed, the volume, increased size, increased power consumption and the lack of a need for field-programmability, using an FPGA to implement the retimer circuitry of Zhang makes no sense and is not possible in view of the speed limitations of FPGA's.

49. Indeed, *What is an FPGA* itself makes clear that "Due to the increased flexibility of an FPGA it will be **less energy efficient** and **slower than** either CPLDs or **ASICs**". (Ex. A at 2 (emphasis added)). A POSITA at the time of the invention would reach this same conclusion. The retimer circuit described by Zhang needs to run faster than an FPGA allows such that it **cannot** be implemented by an FPGA as the Examiner suggests, and certainly would not benefit from the use of an FPGA. The circuit described by Zhang already allows enough configurability such that a field-programmable device would be superfluous.

50. A POSITA at the time of the invention would understand that the use of the FPGA instead of the ASIC would not "reduce the size of the circuit" and would not "improve energy efficiency," as suggested by the Examiner.

51. To the contrary such a modification, if it were technically possible, which it is not, would take up more space and consume more power, generating additional cooling problems, such that a POSITA would not be motivated to make such a change.

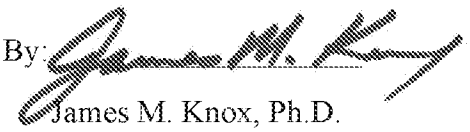
52. Nothing in Zhang suggests a need for any additional flexibility that would make additional configuration and reprogramming options provided by an FPGA useful or desirable beyond the programable options already available in Zhang. Zhang already offers significant programmatic control, including the ability to control the second demux ratio (col. 9 lines 36-40)

and the ability to control the depth of the FIFOs (col. 10 lines 24-26). These options allow the user to control the functioning of the retimer programmatically without the use of an FPGA and the problems that come with it such that use of an FPGA, even if technically feasible, which it is not, would provide no benefits but offer significant drawbacks.

I hereby declare that all the statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements are made with knowledge that willful false statements and the like so made punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code.

Respectfully Submitted,

Dated: May 14, 2024

By: 

James M. Knox, Ph.D.

EXHIBIT A

PENDING CLAIMS IN U.S. Serial No. 17/723,130

LISTING OF CLAIMS:

1. (Currently Amended) A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:

(a) receiving, by a deserializer in a field programmable array, a clock signal;

(b) receiving, by the deserializer, the first serial data stream;

(c) generating, by the deserializer, a receiver side clock signal;

(d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;

(e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;

(f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;

(g) generating, using the phase lock loop, a transmitter side clock signal;

(h) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams;

(i) converting the second plurality of parallel data streams, by a serializer, into a second serial data stream; and

(j) transmitting, from the field programmable gate array system, the second serial data stream, ~~derived from the second plurality of parallel data streams;~~

wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

2. (Original) The method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the set of operations are associated with a trading algorithm.

3. (Original) The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.

4. (Original) The method of claim 1, wherein the set of operations includes at least one of the following:

(i) an arithmetic operation;

(ii) a logical operation;

(iii) a pipeline operation; and

(iv) a memory access operation.

5. (Original) The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed prior to step (g).

6. (Original) The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed after step (g).

7. (Original) The method of claim 1, wherein all of the set of operations performed in step (h) are performed after step (g).

8. (Previously Presented) The method of claim 1, wherein step (g) further comprises:

(k) generating, by the phase lock loop, a feedback clock signal associated with the transmitter side clock signal by performing the following steps until a first output of a phase detector of the field programmable gate array system is below a first threshold level:

(1) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal;

(2) generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal;

(3) transmitting, from the phase detector to a phase controller of the field programmable gate array system, the first output;

(4) determining, by the phase controller, interim adjustment information based on the first output; and

(5) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information;

wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information,

wherein steps (1) through (5) are repeated until the first output of the phase detector is below the first threshold level, and

wherein the transmitter side clock signal is associated with the second clock signal.

9. (Currently Amended) The method of claim 1, wherein the first plurality of parallel data streams has the same number of data streams as the second plurality of parallel data streams.

10. (Original) The method of claim 1, wherein the first plurality of data streams and the second plurality of data streams comprise one of the following:

(i) eight (8) data streams;

(ii) ten (10) data streams;

(iii) sixteen (16) data streams;

(iv) twenty (20) data streams;

(v) thirty-two (32) data streams;

(vi) forty (40) data streams;

(vii) sixty-four (64) data streams;

(viii) eighty (80) data streams;

(ix) one hundred twenty-eight (128) data streams; and

(x) one hundred sixty (160) data streams.

11. (Original) The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and phase.

12. (Original) The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and different phases.

EXHIBIT B

TriSoft/CyberSearch
1300 Koenig Lane West
Austin, Texas 78756
(512) 385-0316

Education

BSEE, Electrical Engineering, University of Texas, 1969
MA, Computer Sciences, University of Texas, 1971
PhD, Electrical Engineering, University of Texas, 1978

Clearance: SECRET

Experience

- Owner, CyberSearch, Austin, Texas, 1976-present
- Chief Engineer, Chief Technology Officer, L-3Com/AVISYS, Austin, TX, 2004-2007
- Owner, TriSoft, System Development Engineer, Austin, Texas, 1984-present
- Faculty, Dept. of Electrical Engineering, University of Texas, 1992-1996
- Partner, TriSoft, System Development Engineer, Austin, Texas, 1982-1984
- System Programmer, Design Engineer, University of Texas, Department of Computer Sciences, Austin, Texas, 1970-1974
- System Programmer Analyst, Design Engineer, University of Texas, Austin, Texas, 1969-1978.
- System Programmer, Electronics Research Center, University of Texas, Austin, Texas, 1968-1969
- Computer Programmer, Bureau of Engineering Research, Austin, Texas, 1965-1968

Fields of Experience

- Development of embedded-processor data collection systems. [University of Texas]
- Development of embedded-processor real-world interface system for assisted living environments. [National Institute of Health (NIH)]
- Senior lecturer on the design and analysis of computer hardware and software, with emphasis on embedded and real-time microprocessor applications. [University of Texas]
- Implementation of several embedded realtime operating systems, including MS-1700 [University of Texas] and multiprocessor system MSOS [Tracor]
- Customization of operating systems such as Digital Research CP/M-68K for Tandy and Apple (Macintosh) systems, VAX-VMS and RSX/RT [University of Texas]
- Development of numerous microprocessor-based automated test equipment (ATE) systems. [Tracor, University of Texas]

- Design of graphic analysis algorithms for image enhancement, developed computerized analysis of cellular photomicroscopy images. [University of Texas]
- Secure LAN and other telecommunications, both military and commercial, provided analysis of MC68HC11 security limitations for financial network certification. [GTE, Intellect Australia, General Electric]
- Extensive experience in aircraft protection systems, threat-adaptive countermeasures systems and electronic warfare, including multiprocessor embedded system design and fault tolerant systems. [Tracor, Meccanicá L'Elettronicá Servomeccanismi (MES), Tokimec, BAE Systems, Avisys, L-3]
- Development of electronic publishing and database design for scientific journals. [Applied Mechanics Reviews, ASME]
- Development of inflight microprocessor-based tracking system for airline reservation, ticketing and data collection. [People's Express]
- Expert witness in cases involving electronic or computer systems, hardware or software.
- Development of RF communications and wireless security devices.

Publications

Knox, External Design Specifications for The University of Texas at Austin IMPORT/EXPORT System: TSD-11, The University of Texas, Austin, Texas, 1970.

Knox, The IMPORT 1700 Remote Communications Package, The University of Texas, Austin, Texas, 1971.

Knox, The MIS 1700 Operating System, The University of Texas, Austin, Texas, 1971.

Knox, A Multiprogrammed Operating System for a Partially Dedicated CDC-1700 Computer System, Master's Thesis, The University of Texas, Austin, Texas, 1971.

Knox and Diller, "Computer Analysis of Volumetric Changes During Cellular Freezing-Thawing", Cryobiology, 14, 1977.

Knox and Diller, "Volumetric Changes Induced in Living Cells During Freezing and Thawing", Advances in Biomedical Engineering, ASME, N.Y., 1978.

Knox, Schwartz, and Diller, "Computerized Measurement of Cellular Volume Changes Occurring During Cryopreservation", Cryobiology, 15, 1978.

Knox, Computer Measurement and Analysis of Cell Freezing, Doctoral Dissertation, The University of Texas, Austin, Texas, 1978.

Juhasz and Knox, AKWAS, Applied Mechanical Reviews, Vol. 32, 1978.

Juhasz, Knox, et al., "Author and Key Word in Alphabetic Sequence", Mechanical Engineering, Vol. 102, No. 7, July 1980.

Knox and Schwartz, "Volumetric Changes in Cells During Freezing and Thawing", Journal of Biomechanical Engineering, Vol. 102, No. 2.

Juhasz and Knox, AKWAS-II, Applied Mechanics Reviews, Vol. 32, 1979. (later volumes produced 1980, 1981, 1982).

Diller and Knox, "Automatic Computer Analysis of Cell Size Changes During Cryomicroscope Freezing: A Biased Trident Convolution Mask Technique", Cryo-Letters 4, 77-92, 1983.

Knox, "Micro's and Mainframes -- The Data Connection", paper presented to ASME and IEEE, San Antonio, Texas, September, 1987.

Prior Testimony

Simple Air, Inc. v. Google, Inc. et al., No. 2:14-cv-011, No. 2:13-cv-937 (E.D. Tex. 2014)

Mirror Worlds Technologies LLC v. Apple et al., No. 6:13-cv-00419 (E.D. Tex. 2013)

Data Treasury v. Fiserv Inc. et al, No. 2:13-cv-00431 (E.D. Tex. 2013)

Freescale Semiconductor, Inc. v. Media Tek, Inc., No. 1:12-cv-00603 (W.D. Tex. 2012)

Freescale Semiconductor, Inc. v. Media Tek, Inc., Inv. No. 337-TA-882 (ITC 2012)

Network-1 Technologies v. Alcatel-Lucent USA Inc. et al, No. 6:11-cv-492 (E.D. Tex. 2011)

SimpleAir, Inc. v. Microsoft Corp., No. 2:11-cv-00416 (E.D. Tex. 2011)

Freescale Semiconductor, Inc. v. Zoran Corp. et al., No. 1:11-cv-00472 (W.D. Tex. 2011)

Freescale Semiconductor, Inc. v. Zoran Corp. et. al., Inv. No. 337-TA-786 (ITC 2011)

Cisco Systems, Inc. v. MOSAID Tech., Inc., No. 1:10-cv-00687 (D. Del. 2010)

Have also written reports, declarations, been deposed or testified in numerous aviation investigation cases from 2009 to the present, including analysis of high-speed and real-time electronic systems [List available by request.]

Other Interests

- Aircraft Pilot (ASEL, Commercial, Instrument rated)
- Director, former Chairman, and former President of Angel Flight, Texas and South Central

- Director, Grace Flight of America
- Member - Institute of Electrical and Electronic Engineers (IEEE)
- Member - Aircraft Owners and Pilots Association (AOPA)
- Member - Association of Old Crows (AOC Military association)
- Member - Experimental Aircraft Association (EAA)

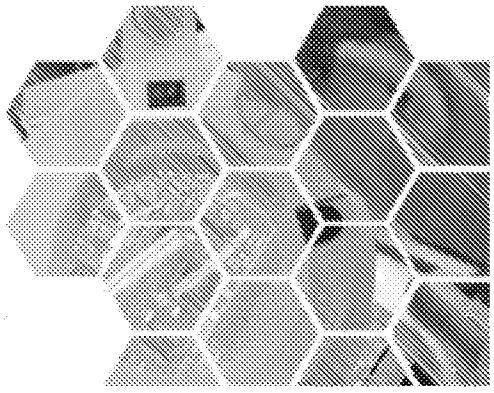
EXHIBIT C

[*What is an FPGA? – Design Support*, DSL, https://www.dsl-ltd.co.uk/support/fpga/]

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What is an FPGA? – Design Support

Introduction



A **field-programmable gate array** (FPGA) is an integrated circuit designed to have its operation configured subsequent to manufacturing, assembly and even deployment of a product of which it forms a part.

FPGAs contain programmable logic blocks, that are capable of performing **many different operations** from simple logic gates to complex functions, and memory blocks.

These blocks can then be connected using a hierarchy of reconfigurable interconnects.

The combination of these elements allows the FPGA to perform in many varied applications.

Advantages

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FPGA are more flexible than a Complex Programmable Logic Device (CPLD) as they, generally, include a greater amount of both logic blocks and programmable interconnects.

FPGA have a lower associated development cost than an ASIC. Whilst an ASIC can perform the same operations as an FPGA and are specific to the application, they cannot be reprogrammed.

FPGA will have a lower time-to-market than an ASIC and also will have a lower non-recurring engineering (NRE) cost.

Disadvantages

Due to the increased flexibility of an FPGA it will be less energy efficient and slower than either CPLDs or ASICs.

They are also be more complex to design than CPLDs. Not only due to their increased size but, due to the greater timing delays that the additional interconnect routes can add, it is more difficult to achieve the required interface signal timings for correct operation.

Historically CPLDs included internal non-volatile flash memory to load the configuration at power on, whilst FPGAs used external devices. FPGA are now available with this functionality, however.

The unit cost of FPGA is greater than that of both CPLD and ASIC.

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- > Fault Fixing Process
- > FAQs
- > What is... ? (Glossary)
- > Application Notes
- > Buyers Guide
- > Acronym & Description

- > Delivery Policy
- > Privacy Policy
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Digital Marketing Agency

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: HFT Solutions, LLC	Confirmation No.: 3228
Application No.	: 17/723,130	
Filed	: April 18, 2022	
For	: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	
TC/A.U.	: 2632	
Examiner	: Kevin Michael Burd	
Docket No.	: 00287-0016	
Customer No.	: 01912	

RESPONSE TO FINAL OFFICE ACTION DATED FEBRUARY 1, 2024

Via Patent Center
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This is a response to the Final Office Action dated February 1, 2024. A response to the Final Office Action is due May 1, 2024. Applicant submits herewith a petition for a one-month extension of time such that the present Amendment is being timely filed.

Amendments to the claims begin on page **2**.

Remarks begin on page **5**.

LISTING OF THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:

(a) receiving, by a deserializer in a field programmable array, a clock signal;

(b) receiving, by the deserializer, the first serial data stream;

(c) generating, by the deserializer, a receiver side clock signal;

(d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;

(e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;

(f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;

(g) generating, using the phase lock loop, a transmitter side clock signal;

(h) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams;

(i) converting the second plurality of parallel data streams, by a serializer, into a second serial data stream; and

(j) transmitting, from the field programmable gate array system, the second serial data stream, ~~derived from the second plurality of parallel data streams;~~

wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

2. (Original) The method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the set of operations are associated with a trading algorithm.

3. (Original) The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.

4. (Original) The method of claim 1, wherein the set of operations includes at least one of the following:

(i) an arithmetic operation;

(ii) a logical operation;

(iii) a pipeline operation; and

(iv) a memory access operation.

5. (Original) The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed prior to step (g).

6. (Original) The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed after step (g).

7. (Original) The method of claim 1, wherein all of the set of operations performed in step (h) are performed after step (g).

8. (Previously Presented) The method of claim 1, wherein step (g) further comprises:

(k) generating, by the phase lock loop, a feedback clock signal associated with the transmitter side clock signal by performing the following steps until a first output of a phase detector of the field programmable gate array system is below a first threshold level:

(1) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal;

(2) generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal;

(3) transmitting, from the phase detector to a phase controller of the field programmable gate array system, the first output;

(4) determining, by the phase controller, interim adjustment information based on the first output; and

(5) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information;

wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information,

wherein steps (1) through (5) are repeated until the first output of the phase detector is below the first threshold level, and

wherein the transmitter side clock signal is associated with the second clock signal.

9. (Currently Amended) The method of claim 1, wherein the first plurality of parallel data streams has the same number of data streams as the second plurality of parallel data streams.

10. (Original) The method of claim 1, wherein the first plurality of data streams and the second plurality of data streams comprise one of the following:

(i) eight (8) data streams;

(ii) ten (10) data streams;

(iii) sixteen (16) data streams;

(iv) twenty (20) data streams;

(v) thirty-two (32) data streams;

(vi) forty (40) data streams;

(vii) sixty-four (64) data streams;

(viii) eighty (80) data streams;

(ix) one hundred twenty-eight (128) data streams; and

(x) one hundred sixty (160) data streams.

11. (Original) The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and phase.

12. (Original) The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and different phases.

REMARKS

This is a response to the Final Office Action dated February 1, 2024. Claims 1-12 are pending in the present application with claim 1, in independent form. Applicant has amended claims 1 and 9 herein to further clarify the subject matter thereof. Applicant submits that no new matter has been added by this amendment.

A. Interview Summary

Applicant appreciates the courtesy extended to Applicant's representatives, Keith J. Barkaus (Reg. No. 51,431), Charles R. Macedo (Reg. No. 32,781) and Thomas E. Hart (Reg. No. 81,259) during the telephone interview of February 28, 2024.

During the interview, Applicant's representatives clarified the Examiner's current obviousness rejection based on Zhang et al. (US 8873606) in view of Cho et al (US 2018/0027431).

The Examiner confirmed that the following markup of FIG. 6 of Zhang accurately reflected the Examiner's application of Zhang to the claims of the present application as presented in the final office action:

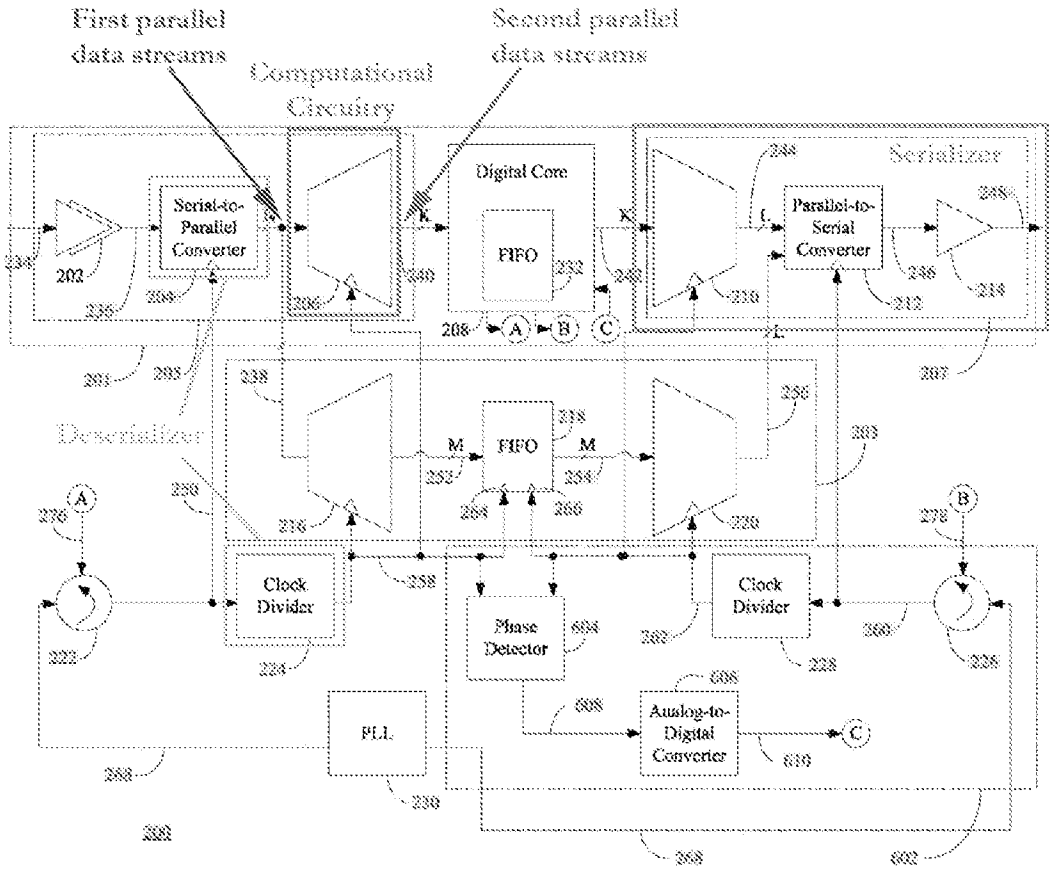


FIG. 6

Applicant's representatives noted that they do not agree with this application of Zhang as presented by the Examiner.

Applicant's representatives explained that under the Examiner's application of Zhang to claim 1, Zhang does not disclose all the features of claim 1. In particular, Zhang does not disclose the limitations of claim 1(i) ("converting the second plurality of parallel data streams, by a serializer, into a second serial data stream").

Applicant's representatives noted that the Final Office Action contends that the claimed "second plurality of parallel data streams" corresponds to the K parallel data streams output from the demux 206 as shown at line 240 in FIG. 6 of Zhang. As indicated in FIG. 6, these data streams are input into the Digital Core 208, including the FIFO 232, which provides an output that is a new and modified set of K parallel data streams as indicated by line 242, based on processing by the Core 208 and including delay and alignment provided by FIFO 232. These modified K parallel data streams are input into mux 210 which the Examiner contends is part of the serializer 207.

The Examiner acknowledged that "K" as used in FIG. 6 refers to the number of data streams and that the K parallel data streams indicated at 242 were processed in the Digital Core 208, and therefore reflected different information and data from the K parallel data streams indicated at 240.

The Examiner asserted that no limitations of claim 1 prevent any type of additional processing from taking place on the second plurality of data streams between generation by the computational circuitry and conversion by the serializer. Applicant's representatives explained that in claim 1(i), "the second plurality of parallel data streams" generated by the computational circuitry is "converted by the serializer", and therefore, if modified by the Digital Core 208 before being converted, would not meet the limitation of claim 1.

Applicant's representatives and the Examiner disagreed as to whether, for purposes of claim 1, "the second plurality of data streams" "convert[ed] ... by a serializer" must be the same "second plurality of data streams" referenced in 1(h) as being "generate[d]" "by the computational circuitry". Applicant's representatives noted that the recitation of "a second plurality of parallel data streams" in claim 1(h) provided antecedent basis for "the second plurality of parallel data streams" in claim 1(i). Thus, Applicant's representatives confirmed that the second plurality of data streams recited by claim 1(i) must be the same second plurality of data streams recited by claim 1(h).

Given the Examiner's recognition that the K parallel data streams indicated at 242 have been modified by the Digital Core 208 and differ from the K parallel data streams indicated at 240 that are the output of demux 206 which the Examiner contends corresponds to the "computational circuitry", Zhang does not disclose the limitations of claim 1(i).

In response to the arguments raised by Applicant's representatives, the Examiner suggested that the computational circuitry of Zhang may include the K parallel data streams indicated at 240 as well as the Digital Core 208. Applicant's representatives noted that this application of Zhang to claim 1 would fail, as claim 1 specifically recites, that the "method does not use clock domain crossing operations that delay processing of the first set of parallel data streams." Applicant's representatives explained that Digital Core 208 explicitly includes a "FIFO", which performs clock domain crossing operations.

In response, the Examiner questioned whether "clock domain crossing operations" had been sufficiently defined. Applicant's Representatives note that in its January 23, 2024 Response to the October 26, 2023 Office Action ("Oct. 26 O.A."), Applicant clarifies the meaning of this term as described by Paragraph [0291] of the specification. For ease of reference, Applicant was referring specifically to the following paragraph from the January 23, 2024 Response:

> With respect to the Examiner's concerns regarding the scope of the term "clock domain crossing operations" in claim 1, Applicant notes that, as used in claim 1, ***"clock domain crossing operations" are operations on the data used to pass the data between clock domains that add latency above and beyond the phase difference between the transmitter side clock signal and the receiver side clock signal.*** Support for this explanation can be found at least in Paragraph [0291] of the present application which discusses examples of clock domain crossing circuits, which use clock domain crossing operations, including "an asynchronous FIFO" such as the FIFO 232 used in Zhang, for example. Such an asynchronous FIFO includes operations (e.g. a memory write, a memory read, and a synchronization operation) that add latency associated with a synchronizer above and beyond the phase difference between the transmitter side clock signal and the receiver side clock signal.
>
> January 23, 2024 Response, at 6 (emphasis added).

Applicant further noted that, FIFO 232 of Zhang, meets this definition and matches the example of a clock domain crossing circuity discussed in Paragraph [0291].

Applicant also discussed the Examiner's proposed modification of Zhang in view of Cho and the lack of support for the alleged motivation to combine.

Applicant's representatives and the Examiner agreed, as stated in the prior office action, that "Zhang does not disclose the method for processing a first serial data stream us[ing] a field programmable gate array system". (Oct. 26 O.A. at 4). The Examiner's alleged motivation to modify Zhang to include the FPGA of Cho was that "[t]he use of FPGA to reduce the size of the circuit and improve energy efficiency of the circuit is well known." *Id.* Applicant's representatives explained during the interview that Zhang taught an application-specific integrated circuit (ASIC), and the proposed modification to replace the ASIC chip from Zhang with an FPGA as allegedly taught in Cho would require more space and use more power than the ASIC. Accordingly, the Applicant's Attorney explained that use of the FPGA instead of the ASIC would not "reduce the size of the circuit" and would not "improve energy efficiency," as suggested by the Examiner. Thus, there is no motivation to modify Zhang in view of Cho.

In response, the Examiner indicated that he was relying on a Google Search result to identify the alleged advantages of FPGAs mentioned in the Office Action. In particular, the Examiner pointed to a statement from the article *What is an FPGA? – Design Support*, DSL, https://www.dsl-ltd.co.uk/support/fpga/ (attached as Exhibit A and identified in an IDS being submitted herewith), which stated that "FPGA require a smaller board space and can be more energy efficient ***than the equivalent discrete circuit***". Ex. A at 2 (*emphasis added*). Applicant's Representatives explained that the ASIC discloses in Zhang is not an "equivalent discrete circuit". Applicant's Representatives also pointed out the reference relied on by the Examiner explained that "Due to the increased flexibility of an FPGA it will ***be less energy efficient and slower than*** either CPLDs or ***ASICs***". Ex. A at 2 (emphasis added). Accordingly, Applicant explained that the motivation suggested by the examiner was contrary to the understanding of a POSITA at the time of the invention such that a POSITA would not have been motivated to modify Zhang to include the FPGA allegedly taught by Cho.

Applicant's representatives also informed Examiner that other support contradicted the Examiner's proposed rationale. For ease of reference, the additional support referenced in the call is also being identified and submitted in an IDS submitted herewith.

Applicant's representatives explained that a POSITA at the time of the invention would not be motivated to replace a single purpose ASIC (like Zhang) with a programmable FPGA. Contrary to the Examiner's stated motivation, an FPGA would be larger and consume more power than an ASIC (e.g., the power for the programmable logic in an FPGA replacing the fixed circuitry

in an ASIC). Further, an FPGA would also add significant cost associated with programming the FPGA to perform the same functions that the ASIC would be preconfigured to perform in Zhang.

The Examiner requested that Applicant formalize Applicant's arguments in writing for the Examiner's review. In the Examiner's interview summary, the Examiner also suggested that Applicant should provide "declarations or affidavits or other evidence" to support this argument. Applicant has done so in the below remarks.

B. Amendments to Claim 1

Claim 1 has been amended to recite:

> A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:
>
> (a) receiving, by a deserializer in a field programmable array, a clock signal;
>
> (b) receiving, by the deserializer, the first serial data stream;
>
> (c) generating, by the deserializer, a receiver side clock signal;
>
> (d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;
>
> (e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;
>
> (f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;
>
> (g) generating, using the phase lock loop, a transmitter side clock signal;
>
> (h) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams;
>
> (i) converting the second plurality of parallel data streams, by a serializer, into a second serial data stream; and
>
> (j) transmitting, from the field programmable gate array system, the second serial data stream,
>
> wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

C. Declaration Under 37 C.F.R. § 1.132

Submitted herewith is a Declaration under 37 C.F.R. § 1.132 by James M. Knox, PhD. in support of the patentability of the claims pending before the Examiner in this case, hereinafter referred to as "Dr. Knox Decl."

D. Rejections of the Claims under 35 USC § 103

In the February 1 Final Office Action, the Examiner rejected claims 1-12 under 35 USC § 103 as allegedly being unpatentable over Zhang et al. (US 8,873,606) in view of Cho et al (US 2018/0027431). The Office Action contends that Zhang allegedly teaches or discloses the entirety of claim 1 except for "the method for processing a first serial data stream uses a field programmable gate array system." Office Action, pg. 3-6. To cure this deficiency, the Office Action relies on the circuit shown in Figure 2 and paragraph [0055] of Cho which allegedly discloses "the SERDES 26 may be implemented in a field programmable gate array (FPGA)." *Id.* Applicant respectfully disagrees.

1. Overview of Zhang

Zhang generally relates to a transceiver that reduces latency. (*See* Zhang, Abstract.) More specifically, FIG. 6 of Zhang, which the Examiner relies on to reject the claims of the present application, illustrates a retimer circuit which is a common circuit used to clean up high speed serial signals and eliminate or reduce noise. (Dr. Knox Decl. at ¶ 22). As noted above and explained during the interview, the particular circuit illustrated in FIG. 6 is an application-specific integrated circuit (ASIC). (*Id.* at ¶ 43).

Dr. Knox explains the operation of the circuit of FIG. 6 as follows::

> The circuit illustrated in FIG. 6 of Zhang receives a serial input signal, which is amplified via amplifier 202 to provide amplified serial input signal 236 to serial-to-parallel converter 204, which provides N parallel signals (col. 6, l. 30-34, 38-44). The serial-to-parallel converter 204 may sample amplified serial data stream 236 according to receiver clock signal 250 (col. 6, l. 38-40). The N parallel signals are provided to a demux 206 to provide K parallel signals at 240 (col. 6, l. 62-65). ***The K parallel signals pass through a digital core 208 including FIFO 232 to provide K delayed parallel signals at 242***. The digital core 208 may buffer the K parallel signals in FIFO 232 which may have a depth of K (the bit depth of the K parallel signals) (col. 7, l. 21-41). The K delayed parallel signals are delayed according to the FIFO depth and are provided to the transmitter circuit 207 (col. 7, l. 24-28). Specifically, the K delayed parallel signals may be provided to a mux 210 to provide L parallel signals (col. 8, l. 7-9). The L parallel signals are provided to parallel to serial converter 212 which converts them into serial output signal 246, which is sent on output signal 248 to a signal line or device. The serial converter 212 is configured to sample the L parallel signals according to the transmitter side clock signal 260 (col. 6, l. 38-40). Zhang also explains that the digital core 208 may provide for the removal of error correction and packet protocol bits from K parallel signals 240, error correction, and/or bit stuffing as part of processing the

> second parallel signals 240. (col. 4, l. 36-43). As discussed later in this declaration, a POSITA would understand this circuit in Zhang is a retimer implemented by an ASIC.

(Dr. Knox Decl., ¶ 23 (*emphasis added*))

2. Zhang does not disclose "converting the second plurality of parallel data streams, by a serializer, into a second serial data stream;"

Amended claim 1 requires, among other things, "converting the second plurality of parallel data streams, by a serializer, into a second serial data stream." In step (h), "a second plurality of parallel data streams" is generated by the computational circuitry. Thus, claim 1, on its face requires that the "second plurality of parallel data streams" generated by the "computational circuitry' be the same "second plurality of parallel data streams" converted by the serializer in the second data stream.

This interpretation of claim 1 is consistent with the law of antecedent basis for claim construction, "**the** second plurality of parallel data streams" converted in step (i) by "a serializer", must be the same as "**a** second plurality of parallel data streams" generated by "the computational circuity" in step (h). *See, e.g., Tech. Consumer Prods. v. Lighting Sci. Grp. Corp.*, 955 F.3d 16, 22 (Fed. Cir. 2020) (reversing PTAB for misapplying antecedent basis; "No other heat sink is specified in the claim. Consequently, 'the heat sink' that is used in the calculation of the height-to-diameter ratio is the same heat sink that is annularly coupled to the heat spreader."); *Ex parte Hisashi Futaki,* Appeal 2024-00825 (PTAB March 5, 2024); *Cisco Systems, Inc. v. WSOU Investments, LLC,* 2021 Pat. App. Lexis 7252, IPR2021-00961, Paper 10 (PTAB Dec. 6, 2021) (Routine Op.) (denying institution of IPR; "Because the former limitation refers to 'a service name' and the latter limitation refers to "the service name," those limitations together require a service connection request message that includes the same 'service name of the remote connected services layer' that is used to establish the service connection.").

Dr. Knox also confirms that a POSITA would have this same understanding of claim 1. Dr. Knox notes that "a POSITA would understand that the 'second plurality of parallel data streams' in step (h) must be the same plurality of data streams in step (i). This 'second plurality of parallel data streams' must both be generated 'by the computational circuitry' and 'convert[ed]' 'by a serializer' into a second serial data stream." (*Id.* at ¶ 14).

In contrast, the Final Office Action contends that different parallel data streams correspond to the "second plurality of parallel data streams" in steps (h) and (i). The Office Action contends that the claim does not preclude further processing of the "second plurality of parallel data streams" between generation by the computation circuitry in step (h) and the conversion by a serializer in step (i). This is incorrect and contrary to the plain meaning of the language in claim 1 as is set forth above and supported by Dr. Knox.

In claim 1, the same "second set of parallel data streams" generated by the computational circuitry in step (h) must be converted by a serializer in step (i). As Dr. Knox explains, and as the Examiner recognized in the telephone interview, the K parallel data streams labeled 240 that are outputted by demux 206 (which the Examiner identifies as his "computational circuitry" for purposes of the claim) are different data streams than the K parallel data streams labeled 242 that are the input of mux 210 portion of 207 (identified by the Examiner as a "serializer"). (*Id.*, at ¶¶ 25-27).

Dr. Knox further explains that the K parallel data streams shown by line 240 in FIG. 6 of Zhang generated by the demux 206 **are not the same** K parallel data streams indicated at 242, which are converted by the circuitry 207 (the alleged "a serializer"). (*Id.* at, ¶¶ 26, 31). Indeed, the Examiner acknowledged during the February 28 Interview and Dr. Knox confirms in his Declaration, that the K parallel data streams output from the demux 206 at line 240 are **further processed** by the Digital Core 208, including the FIFO 232, to generate a new set of K parallel data streams shown at line 242. (*Id.* at, ¶¶ 27-28). As Dr. Knox further explains, while the bit width of the parallel data streams remains as "K" (a fixed integer, e.g., 2, 4, 6, 8, etc.) each of the K data streams are different as a result of the additional processing by the Digital Core 208, including FIFO 232. (*Id.*). As Dr. Knox establishes, a POSITA, at the time of the invention, reviewing the specification and drawings of Zhang would not conclude that a modified set of parallel data streams (such as the K parallel data streams shown at line 242) are the same as an unmodified set of parallel data streams (such as the K parallel data streams shown at line 240). (*Id.* at, ¶¶ 29).

Accordingly, Zhang does not disclose, show or suggest "converting the second plurality of parallel data streams, by a serializer, into a second serial data stream," as is required by amended claim 1. Cho also fails to disclose this features such that Applicant respectfully submits that claim 1 and the claims depending therefrom, including claims 2-12 are patentable over the cited art.

3. FIFO 232 in the Digital Core of Zhang uses "clock domain crossing operations that delay processing of the first set of parallel data streams".

In response to the arguments raised by Applicant's representatives during the February 28, 2024 Interview, the Examiner suggested that the K parallel data streams indicated at 240 as well as the Digital Core 208 may correspond to the "computational circuitry" of claim 1 such that the K parallel data streams at 242 correspond to the second plurality of parallel data streams generated by the computational circuitry. While Applicant does not agree with this interpretation of Zhang, even under this interpretation, the prior art fails to disclose, show or suggest all of the features of claim 1.

Claim 1 requires, among other things, that the "method does not use clock domain crossing operations that delay processing of the first set of parallel data streams." As explained during the Interview, and confirmed by Dr. Knox, Digital Core 208 includes a "FIFO" 232, which performs clock domain crossing operations. (*Id.* at, ¶¶ 24, 28 (*citing* Zhang, Col. 7, lines 20-27))

In the January 23, 2024 Response to the October 26, 2023 Office Action ("Oct. 26 O.A."), Applicant defined "clock domain crossing operations" for purposes of the pending claims, as follows and consistent with Paragraph [0291] of the present application:

> With respect to the Examiner's concerns regarding the scope of the term "clock domain crossing operations" in claim 1, Applicant notes that, as used in claim 1, ***"clock domain crossing operations" are operations on the data used to pass the data between clock domains that add latency above and beyond the phase difference between the transmitter side clock signal and the receiver side clock signal.*** Support for this explanation can be found at least in Paragraph [0291] of the present application which discusses examples of clock domain crossing circuits, which use clock domain crossing operations, including "an asynchronous FIFO" such as the FIFO 232 used in Zhang, for example. Such an asynchronous FIFO includes operations (e.g. a memory write, a memory read, and a synchronization operation) that add latency associated with a synchronizer above and beyond the phase difference between the transmitter side clock signal and the receiver side clock signal.
>
> January 23, 2024 Response, at 6 (*emphasis added*).

Dr. Knox confirms that this explanation of clock domain crossing operations is consistent with what a POSITA, at the time of the invention, would understand in view of Paragraph [291] of the present application, as well as the ordinary meaning of such term as understood by a POSITA. (Dr. Knox Decl., ¶¶ 37-38).

Dr. Knox confirms that FIFO 232 included in the Digital Core 208 of Zhang meets this definition and matches the example of a clock domain crossing circuit that performs clock domain crossing operations described in Paragraph [0291]. (*Id.* at ¶ 39). In particular, Dr. Knox explains that "an asynchronous FIFO" is explicitly listed "as an example of a clock domain crossing circuit, which performs clock domain crossing operations. Thus, at the very least, the "clock domain crossing operations" recited in claim 1, include operations performed by a FIFO." (*Id.* at 39). Further, the operation of the FIFO 232 in Zhang is consistent with a clock domain crossing circuit as Dr. Knox explains:

> the FIFO 232 described in Zhang performs operations that fall under the definition of "clock domain crossing operations" proffered by Applicant and described in the specification at Paragraph [0291] for example. FIFO 232 has a write clock that is in a separate clock domain than the read clock. FIFO 232 buffers signals (col. 7 lines 21-25), resulting in a delayed version of those signals. The buffering is done to tolerate a phase offset between the clock signals (col. 13 lines 23-34) while avoiding errors. Since the clock phases are no more than 360 degrees apart, the phase difference between the transmitter and receiver side clock signal results in a delay equal to a fractional clock cycle. However, the FIFO 232 is a buffer that holds multiple cycles of data at a time, resulting in a delay of more than one clock cycle. The FIFO 232 passes data between clock domains (col. 13 lines 24-25), and by buffering data, adds latency above and beyond the phase difference, delaying the data going through the digital core 208 (col. 7 lines 24-25). Thus, the operation of the FIFO in Zhang is consistent with the definition of a clock domain crossing operations discussed above.
>
> (*Id.* at 39).

Accordingly, if Zhang is interpreted such that the Digital Core 208, including the FIFO 232, correspond to the "computational circuitry", Zhang does not disclose all of the features of amended claim 1, since the FIFO 232 performs clock domain crossing operations that delay processing of the first set of parallel data streams, **contrary** to the requirement of claim 1 that no such clock domain crossing operations are used.

4. The Proposed Modification of Zhang to use an FPGA as allegedly taught by Cho would not have been obvious to a POSITA

The Examiner concedes, "Zhang does not disclose the method for processing a first serial data stream us[ing] a field programmable gate array system". (Feb. 1 O.A. at 6). To rectify this fatal deficiency, the Examiner asserts it would be obvious to "implement the circuit of Zheng on

an FPGA as taught by Cho". (*Id.* at 7). The Examiner alleges that one of skill in the art would be motivated to modify Zhang as suggested because "[t]he use of FPGA to reduce the size of the circuit and improve energy efficiency of the circuit is well known." (*Id.*). Applicant respectfully disagrees.

As noted above, during the February 28, 2024 Interview, the Examiner alleged that this motivation to modify Zhang can be found in *What is an FPGA? – Design Support*, DSL, https://www.dsl-ltd.co.uk/support/fpga/ (attached as Exhibit A and identified in an IDS being submitted herewith), which states that "FPGA require a smaller board space and can be more energy efficient ***than the equivalent discrete circuit***". (Ex. A at 2) (emphasis added).

As an initial matter, this portion of this document is not relevant to the modification suggested by the Examiner since, as Dr. Knox explains, Zhang is not a "discrete circuit", but instead is an application-specific integrated circuit (ASIC). (Dr. Knox Decl., ¶ 43). As Dr. Knox explains, "Zhang describes a circuit that receives a stream at 10 Gbps which is parallelized to 20 parallel signals at 500 MHz" (*citing* Zhang, col. 1 lines 38-39 and col. 4 lines 12-16) and that "Zhang discloses the low latency channel having a 4-bit signal at 2.5 GHz" (*citing* Zhang, col. 10 lines 46-48). (*Id.*). Dr. Knox notes that it "would have been well known to a POSITA at the time of the invention, a 500 MHz or higher clock rate is unrealistic for discrete circuits". Thus, as Dr. Knox concludes, "the alleged advantage of FPGA's over discrete circuits set forth in the article relied on by the Examiner is not relevant with respect to modifying Zhang, which is ***not a discrete circuit***." (*Id.* at ¶¶ 43-44 (*emphasis in original*)). Dr. Knox makes clear that the analysis of an FPGA vs. a discrete circuit is irrelevant to the suggested modification of the ASIC in Zhang. (*Id.* at 44).

Indeed, there is no motivation to implement the ASIC of Zhang using an FPGA as allegedly disclosed in Cho. To the contrary, a POSITA would be discouraged from such a combination based on the inapplicability of the relative features of an ASIC and an FPGA for the problem addressed by Zhang. (*Id.* at ¶ 47). Indeed, the speed limitation inherent to FPGA's would likely make the modification suggested by the Examiner fruitless if not impossible. (*Id.*).

As Dr. Knox explains, Zhang teaches a specific ASIC design for a retimer circuit. (*Id.* at ¶ 22). The purpose of this retimer circuit is "to clean up high-speed serial signals traveling on noisy channels. In particular, retimer circuits are used to recover a signal and drive a new copy with

noise and jitter removed." (*Id.* at ¶ 22). A POSITA at the time of the invention would understand that the use of an ASIC for such a circuit makes perfect sense. (*Id.* at ¶ 47).

Further, as Dr. Knox further explains, using an FPGA to implement the retimer circuitry of Zhang makes no sense. (*Id.* at ¶ 48). Indeed, as Dr. Knox notes, the *What is an FPGA* article itself makes clear that the Examiner's proposal makes no sense noting: "Due to the increased flexibility of an FPGA it will be **less energy efficient** and **slower than** either CPLDs or **ASICs**". (*Id.* at ¶ 49; *quoting* Ex. A at 2 (*emphasis added*)). Dr. Knox confirms a POSITA at the time of the invention would reach this same conclusion. (*Id.* at ¶ 49). In particular, Dr. Knox explains, Zhang teaches an application-specific integrated circuit (ASIC), and the proposed modification to implement the ASIC chip from Zhang using an FPGA as taught in Cho would require more space and use more power than the ASIC. (*Id.* at ¶ 45). Accordingly, as Dr. Knox confirms, a POSITA at the time of the invention wound understand that the use of the FPGA instead of the ASIC would not "reduce the size of the circuit" and would not "improve energy efficiency," as suggested by the Examiner. (*Id.* at ¶ 50). To the contrary such a modification would take up more space and consume more power such that a POSITA would not be motivated to make such a change. (*Id.* at ¶ 51). Indeed, the drawbacks of an FPGA compared to an ASIC described above would teach a POSITA not to modify Zhang to include an FPGA such that it would not have been obvious to modify Zhang as allegedly taught by Cho.

Lastly, as Dr. Knox explains, nothing in Zhang suggests a need for any additional flexibility that would make additional programming options provided by an FPGA useful or desirable beyond the programable options already available in Zhang. (*Id.* at ¶ 52). That is, there is no benefit to using an FPGA in place of the ASIC that is taught by Zhang such that it would not have been obvious to modify Zhang as alleged by the Examiner.

The Examiner is respectfully requested to fully consider the Declaration Under 37 CFR 1.132 submitted herewith.

Accordingly, Applicant respectfully submits that claim 1, and the claims depending therefrom, including claims 2 - are patentable over the cited art for at least the reasons discussed above.

5. The Obviousness Type Double Patenting Rejection

The Office Action rejects claims 1-12 based on statutory double patenting in view of claim 8 of U.S. Patent No. 11,575,381. Applicant respectfully requests reconsideration of this rejection.

Claim 8 of U.S. Patent No. 11,575,381 depends on and includes all of the features of claim 1 therein. Claim 1 of the present application requires, among other things, "transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal." In contrast, claim 1 of U.S. Patent No. 11,575,381, on which claim 8 depends, requires "transmitting, from the deserializer to a phase lock loop of the field programmable gate array system **that is not within the field programmable gate array**, the receiver side clock signal." Thus, the claims of the present application are believed to be patentably distinct from the claims of U.S. Patent No. 11,575,381.

Claims 1-12 of the present application are also rejected under obviousness-type double-patenting over one or more claims of U.S. Patent Nos. 11,575,381, 10,931,286, 10,826,502, 11,128,305, 11,502,694, 10,763,865, 10,771,069, 11,018,678 or 11,329,655. (Office Action, pgs. 11-20).

In order to advance prosecution, Applicant submits herewith a terminal disclaimer with respect to U.S. Patent Nos. 11/575,381, 10,931,286, 10,826,502, 11,128,305, 11,502,694, 10,763,865, 10,771,069, 11,018,678 and 11,329,655 to overcome this rejection.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of the claims based on double patenting.

Reference to Related Patents and Co-Pending Applications

The below chart provides information regarding related issued patents and co-pending applications filed by the present Applicant:

	ATTORNEY DOCKET NO.	FILING DATE	STATUS
16/672,076	00287-0007	2019-11-01	Issued USP 10,826,502
16/670,702	00287-0008	2019-10-31	Issued USP 10,771,069
16/888,218	00287-0009	2020-05-29	Issued USP 10,763,865
16/937,314	00287-0011	2020-07-23	Issued USP 10,931,286
16/937,309	00287-0012	2020-07-23	Issued USP 11,018,678
17/248,304	00287-0013	2021-01-19	Issued USP 11,128,305
17/236,577	00287-0014	2021-04-21	Issued USP 11,329,655
17/405,188	00287-0015	2021-08-18	Issued USP 11,502,381
17/723,130	**00287-0016**	**2022-04-18**	**Present Application**
17/723,145	00287-0017	2022-04-18	Issued USP 11,575,381

	ATTORNEY DOCKET NO.	FILING DATE	STATUS
18/067,332	00287-0018	2022-12-16	Docketed New Case - Ready for Examination

The Examiner is invited to review the prosecution history of each of these applications, including the cited references of record and related office actions, as the Examiner deems appropriate.

The Examiner is invited to review the prosecution history of each of these applications, including the cited references of record and related office actions, as the Examiner deems appropriate.

CONCLUSION

In view of the foregoing, Applicant respectfully submits that all pending claims are patentable over the cited art and in condition for allowance. Reconsideration and prompt allowance of this application are both respectfully solicited.

Applicant respectfully asserts that the foregoing constitutes a bona fide response to all outstanding objections and rejections within this Office Action.

This application is in condition for immediate allowance. However, should any issue(s) of a minor nature remain, the Examiner is respectfully requested to telephone the undersigned at telephone number (212) 336-8000 so that the issue(s) might be promptly resolved.

Favorable reconsideration of the present application is respectfully requested.

* * * * * *

Any claim amendment(s), claim(s) added, claim(s) canceled, argument(s), remark(s), and/or any combination(s) thereof made in this response pertain solely to the specific aspects of this specific claimed invention. Further, any claim amendment(s), claim(s) added, claim(s) canceled, argument(s), remark(s), and/or any combination(s) thereof are made without prejudice to or disclaimer of Applicant's right to seek patent protection of any unclaimed subject matter such as, but not limited, to narrower unclaimed subject matter, broader unclaimed subject matter, different unclaimed subject matter, variations of unclaimed subject matter, any combination thereof, and/or any other unclaimed subject matter that may or may not be filed, for example, in any design and/or utility patent application(s) such as, but not limited to, continuation patent

application(s), continuation-in-part patent application(s), and/or divisional patent application(s) and/or any other patent application(s).

Applicant's silence as to any assertion(s) by the Examiner in the Office Action and/or to any certain fact(s) or conclusion(s) that may be implied and/or alleged by objections(s) and/or rejection(s) in the Office Action is not in any way a concession by Applicant that such assertion(s), implication(s), and/or allegation(s) are accurate, and that all requirements for any objection(s) and/or a rejection(s) have been met. Accordingly, Applicant reserves the right to analyze and dispute any such assertion(s), implication(s), and/or allegation(s) in the future.

Respectfully submitted,

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Dated: New York, New York
May 14, 2024

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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/723,130	**05/14/2024 04:58:29 PM Z ET**	**00287-0016**

Title of Invention

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3228	FILED BY	Victoria GILMORE
PATENT CENTER #	65524518	FILING DATE	04/18/2022
CUSTOMER #	1912	FIRST NAMED INVENTOR	Nima Badizadegan
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Keith Barkaus

Documents

TOTAL DOCUMENTS: 5

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
1-ResponsetoFOA.pdf		19	-	475 KB
1-ResponsetoFOA-A.NE.pdf	(1-1)	1	Response After Final Action	103 KB
1-ResponsetoFOA-CLM.pdf	(2-4)	3	Claims	108 KB
1-ResponsetoFOA-REM.pdf	(5-19)	15	Applicant Arguments/Remarks Made in an Amendment	459 KB
2-Knox132Declaration.pdf		30	Affidavit-traversing rejections or objections rule 132	977 KB
3-Extension of Time.pdf		2	Extension of Time	422 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
1-ResponsetoFOA.pdf	0562FD3FC2033FFE568947718CABE163E5F925599E9EB9E2A BE6EC61CD9880C2DBA7348A5247CB2F886DBAB9CA73190A1 F5F5BDF60B0B7DB167F2A5302EDFE6E
1-ResponsetoFOA-A.NE.pdf	C7139EECF40C6E613ABEFC21532924A81F8D25CECB017DED 95CF8240C56F527C17ECB81C9A31A5F92D6AEBAECE82ED4A 7C84B4F7FB112D69B55F388EFBDDA4D9
1-ResponsetoFOA-CLM.pdf	05CCAB8EFBA2962A97E1233CE7023333B575DC474919C53E5 A795603FBB470E55A6447F4F527FBE3A422BAEEB133A1A8449 CE1F5AB991BAC47CCB6B96FB6D866
1-ResponsetoFOA-REM.pdf	8F521EBDAFC86561E06D82FE30DD88E32C20B9E9A88CD560 7F7E170E7760BACA5FE4002EC49F3D6C9D7D96F5F1C7E638E CEEC02444A4CC918BA285373A9A482A
2-Knox132Declaration.pdf	BB5DDC5E225FD92446D5462E1BCDCD987AEE49AE3827045C 81C70C4F11009896F3D8E7D97479F4FD6D3A20E6D4875264C9 B2C73B4F8E57C34FC79705B48B8A1F
3-Extension of Time.pdf	C24C3A02BEEEB2A8A79FD43FD8F754C9BD768EA2D19531B0 2BFCB330D638EA5BB14B92E7CDCC4960B3BE03DF85D1B844 15A13137553E437C382ABCE6448AF730

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/22 (11-23)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number (Optional): 00287-0016

Application Number: 17/723,130

Filed: April 18, 2022

For: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

Art Unit: 2632

Examiner: Kevin Michael BURD

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
☑ One month (37 CFR 1.17(a)(1))	$220	$88	$44	$ 88
☐ Two months (37 CFR 1.17(a)(2))	$640	$256	$128	$
☐ Three months (37 CFR 1.17(a)(3))	$1,480	$592	$296	$
☐ Four months (37 CFR 1.17(a)(4))	$2,320	$928	$464	$
☐ Five months (37 CFR 1.17(a)(5))	$3,160	$1,264	$632	$

☑ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☑ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 011785.

☑ Payment made via USPTO patent electronic filing system.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 51,431.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Keith J. Barkaus/
Signature

May 14, 2024
Date

Keith J. Barkaus
Typed or printed name

212 336 8000
Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of 1 forms are submitted.

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0031. Public burden for this form is estimated to average 6 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.** If filing this completed form by mail, send to: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

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Privacy Act Statement

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Routine uses of the information in this record may include disclosure to:

1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
2) a federal, state, local, or international agency, in response to its request;

3) a contractor of the USPTO having need for the information in order to perform a contract;

4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;

5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;

6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;

7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;

8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));

9) the Office of Personnel Management (OPM) for personnel research purposes; and

10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A PRIOR PATENT

APPLICATION #	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET #
17723130	04/18/2022	Nima Badizadegan	00287-0016

Title of Invention

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

☑ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☑ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent interest
HFT Solutions, LLC	100%
Total	100%

The owner(s) of percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending reference Application Number(s)

Application #	Filing Date

as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the reference application are commonly owned. This agreement runs with any patent granted on the

instant application and is binding upon the grantee, its successors or assigns.
In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said reference application, "as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application," in the event that any such patent granted on the pending reference application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

The owner(s) of percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

Patent #
11575381
10931286
10826502
11128305
11502694
10763865
10771069
11018678
11329655

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.
In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
• expires for failure to pay a maintenance fee;
• is held unenforceable;

- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.



Terminal disclaimer fee under 37 CFR 1.20(d) included with Electronic Terminal Disclaimer request.

Applicant claims the following entity status:
Small

I hereby declare that all statements made herein of my own knowledge are true and that all statemnts made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I certify, in accordance with 37 CFR 1.4(d)(4) that I am: An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Signature	Name	Registration #
/Keith J Barkaus/	Keith Barkaus	51431

---

* Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this certification. See MPEP 324.

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APPROVAL LETTER

APPLICATION #	FILING DATE	APPLICANT/PATENT UNDER REEXAMINATION
17/723,130	04/18/2022	Nima Badizadegan

Title of Invention

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

Electronic terminal disclaimer filed on 05/14/2024

☑ Approved

This patent is subject to a Terminal Disclaimer

Approved / Disapproved by: Electronic Terminal Disclaimer automatically approved

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/723,130	**05/14/2024 04:51:55 PM Z ET**	**00287-0016**

Title of Invention

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3228	FILED BY	Victoria GILMORE
PATENT CENTER #	65523654	FILING DATE	04/18/2022
CUSTOMER #	1912	FIRST NAMED INVENTOR	Nima Badizadegan
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Keith Barkaus

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
petition-request.pdf	3	Terminal Disclaimer-Filed (Electronic)	52 KB
grantLetter.pdf	1	Terminal Disclaimer-Electronic-Approved	19 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
petition-request.pdf	046FE74B5F6D8FD6EB83FBADD17B32F753C3CF563F7738175 E2EB8343FBCD34960C95F43954FD680260747C0E6DFC7B965

Optiver Ex 1002
Page 97 of 459

E876A564549C3D2A97408AD0E8EB18

grantLetter.pdf 227409BC2E31476DFAD700698F6EC1DB55C428D02D08DE5597F1FE899D552BC164A51FFFA3EE1ECFDAB573B5DC595EB3E934705CC9D9649F81DACDAE88AB3200

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/723,130	05/14/2024 04:51:55 PM Z ET	00287-0016

Title of Invention

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3228	FILED BY	Victoria GILMORE
PATENT CENTER #	65523654	AUTHORIZED BY	Keith Barkaus
CUSTOMER #	1912	FILING DATE	04/18/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Nima Badizadegan

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 1051	E20245DG52565135	Keith Barkaus

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2814	STATUTORY DISCLAIMER, INCLUDING TERMINAL DISCLAIMER	170.00	1	170.00
			TOTAL AMOUNT:	$170.00

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PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/723,130	Filing Date 04/18/2022	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	05/14/2024	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 12	Minus	** 33	= 0		x $40 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 4	= 0		x $192 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/ALLYSON PURNELL/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,130	04/18/2022	Nima Badizadegan	00287-0016	3228

1912 7590 02/29/2024

AMSTER, ROTHSTEIN & EBENSTEIN LLP
405 LEXINGTON AVENUE
FLOOR 48
NEW YORK, NY 10174

EXAMINER
BURD, KEVIN MICHAEL

ART UNIT	PAPER NUMBER
2632	

MAIL DATE	DELIVERY MODE
02/29/2024	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Applicant-Initiated Interview Summary	**Application No.** 17/723,130	**Applicant(s)** Badizadegan, Nima		
	Examiner KEVIN M BURD	**Art Unit** 2632	**AIA (First Inventor to File) Status** Yes	**Page** 1 of 2

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
KEVIN M BURD	Primary Examiner	Telephonic
Keith Barkus	Attorney of Record	
Charles Macedo	Attorney of Record	
Thomas Hart	Agent of Record	

Date of Interview: 28 February 2024

Issues Discussed:

35 U.S.C. 103

An agenda was received prior to the interview. The second plurality of parallel data streams was discussed. Applicant indicated that once the K streams are input to the digital core, the core provides an output that is a new and modified set of K parallel data streams and these are input to the serializer. The examiner disagrees that the K plurality is a new set of parallel stream just because they are processed by an element and output as shown in figure 6. They are the same data streams that have been processed. No limitations of the claim prevent any type of additional processing from taking place on these streams. Figure 6 shows the same plurality, K, being input to the serializer. Applicant's representative argues the rationale for combining the references used in the rejections of the claims. The examiner indicated that he found teaching that the main advantages of an FPGA over the equivalent discrete circuit or application specific IC is the ability to easily change its functionality after a product has been designed. In addition FPGA requires smaller board space and can be more energy efficient than the equivalent discrete circuit. Therefore, the examiner felt the rationale was reasonable. The examiner suggests that if applicant feels this is the reasoning for this application to be allowed, Evidence should be provided such as declarations or affidavits or other evidence to support the attorney arguments. No agreement was reached. Applicant will file an appropriate response.

☑ Attachment

/KEVIN M BURD/ Primary Examiner, Art Unit 2632	

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant-Initiated Interview Summary	**Application No.** 17/723,130	**Applicant(s)** Badizadegan, Nima		
	Examiner KEVIN M BURD	**Art Unit** 2632	**AIA (First Inventor to File) Status** Yes	**Page** **2 of 2**

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

From: Keith J. Barkaus
To: Burd, Kevin M.
Cc: Charles R. Macedo; Thomas Hart
Subject: 00287-16 - Interview Agenda For February 29, 2024 Interview in Serial No. 17/723,130
Date: Tuesday, February 27, 2024 5:32:06 PM
Attachments: Interview Agenda (17723130).pdf

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Dear Examiner Burd:

In advance of our telephone interview scheduled for 10 AM ET tomorrow, February 28, 2024, please find attached our proposed Interview Agenda.

Best regards,

Keith J. Barkaus
Reg. No. 51,431
Charles R. Macedo
Registration No.: 32,781
Thomas Hart
Registration No.: 81,259

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: HFT Solutions, LLC	Confirmation No.: 3228
Application No.	: 17/723,130	
Filed	: April 18, 2022	
For	: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	
TC/A.U.	: 2632	
Examiner	: Kevin Michael Burd	
Docket No.	: 00287-0016	
Customer No.	: 01912	

INTERVIEW AGENDA

Via EFS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Examiner Burd:

Thank you for agreeing to an interview with us on **Wednesday, February 28, 2024 at 10:00 a.m. ET.** We are submitting this agenda to identify the areas we would like to discuss with you:

1. We would like to clarify and discuss the current obviousness rejection based on Zheng et al. (US 8,873,606) in view of Cho et al (US 2018/0027431).

For ease of reference, we have included FIG. 6 from Zheng with our understanding of how the Office Action alleges that it reads on the pending claims:

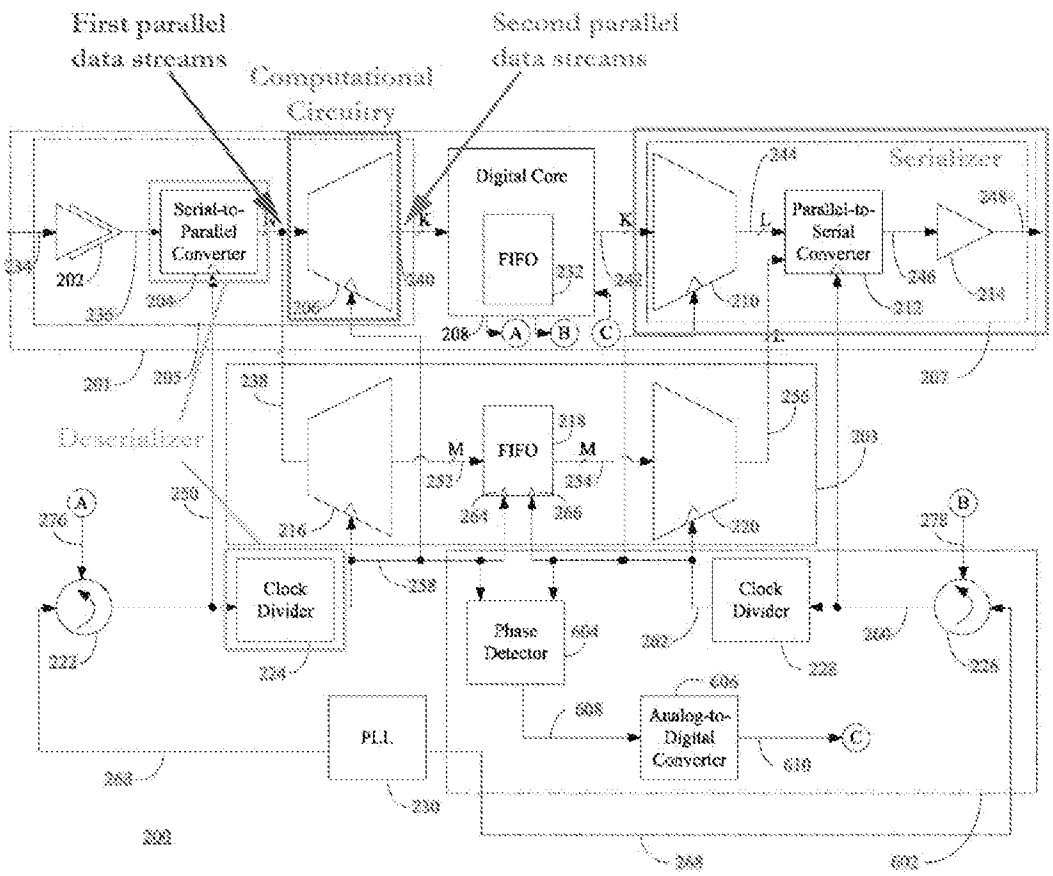


FIG. 6

In the interview, we would like to confirm our understanding of this read.

2. Further, to the extent our understanding of your read is correct, we would like to discuss how the prior art fails to meet the limitations of claim 1(i), including the structures of the prior art that allegedly correspond to the "second plurality of parallel data streams."

The Office Action contends that the claimed "second plurality of parallel data streams" corresponds to the K parallel data streams outputted from the mux 206 as shown at line 240. As indicated in FIG. 6, these data streams are input into the Digital Core 208, including the FIFO 232, which provides an output that is a new and modified set of K parallel data streams as indicated in line 242 based on processing by the Core and further being delayed and aligned by FIFO 232) as the K modified parallel data streams indicate at 242. These modified parallel data streams are input into mux 210 (as part of what is identified in the Office Action as the serializer 207).

Under this interpretation, the alleged "second plurality of parallel data streams," that is, the K parallel data streams at line 240 outputted from mux 206 are not the same data streams as the K modified parallel data streams at line 242 that are input into the mux 210. Thus, the K parallel data streams outputted from mux 206, which the Examiner contends correspond to the "second plurality of parallel data streams" are not "convert[ed]" "by the serializer" as required in step (i).

3. We would also like to discuss your proposed modification of Zheng in view of Cho.

As you correctly state, "Zheng does not disclose the method for processing a first serial data stream us[ing] a field programmable gate array system." Your proposed modification of Zheng is to use SERDES 26 as taught in Cho fig. 2. Your proposed rational is that "[t]he use of FPGA to reduce the size of the circuit and improve energy efficiency of the circuit is well known." The circuit taught in Zheng is an application-specific integrated circuit (ASIC), and specifically a Retimer chip, which receives data in a noisy form, buffers it, and then retransmits it in a cleaner form.

The proposed modification to replace the retimer ASIC chip from Zheng with an FPGA as taught in Cho would require more space and use more power than the ASIC, such that use of the FPGA instead of the ASIC would not "reduce the size of the circuit" and would not "improve energy efficiency," as suggested by the Examiner.

Further, a POSITA at the time of the invention would not be motivated to replace a single purpose ASIC with a programmable FPGA, only to provide the single purpose taught in Zheng as it would not only be larger and consume more power (e.g., the power for the programmable logic in an FPGA replacing the fixed circuitry in an ASIC), but it would also add significant cost associated with programming the FPGA to perform the same functions that the ASIC would be preconfigured to perform in Zheng.

We look forward to speaking with you on Wednesday.

Respectfully submitted,

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Dated: New York, New York
February 27, 2024

By: /Keith J. Barkaus /
Keith J. Barkaus
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Registration No.: 81,259

ATTACHMENT 1

Pending Independent Claim

1. A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:

(a) receiving, by a deserializer in a field programmable array, a clock signal;
(b) receiving, by the deserializer, the first serial data stream;
(c) generating, by the deserializer, a receiver side clock signal;
(d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;
(e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;
(f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;
(g) generating, using the phase lock loop, a transmitter side clock signal;
(h) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams;

(i) converting the second plurality of parallel data streams, by a serializer, into a second serial data stream; and

(j) transmitting, from the field programmable gate array system, the second serial data stream,

wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,130	04/18/2022	Nima Badizadegan	00287-0016	3228

1912 7590 02/01/2024

AMSTER, ROTHSTEIN & EBENSTEIN LLP
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EXAMINER
BURD, KEVIN MICHAEL

ART UNIT	PAPER NUMBER
2632	

MAIL DATE	DELIVERY MODE
02/01/2024	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 17/723,130	Applicant(s) Badizadegan, Nima	
	Examiner KEVIN M BURD	Art Unit 2632	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 1/23/2024.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-12 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-12 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

1. This office action, in response to the amendment filed 1/23/2024, is a final office action.

Response to Amendment and Arguments

2. Claim 1 is amended to recite the limitation of "converting the second plurality of parallel data streams, by a serializer, into a second serial data stream". Applicant states Zhang does not disclose, show or suggest performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams or converting the second plurality of parallel data streams, by a serializer, into a second serial data stream on page 5 of the remarks. The examiner disagrees. Zhang discloses the transceiver shown in figure 6. Zhang discloses demux 206 receives the first plurality of parallel streams from S/P 204 and generates a second plurality of parallel streams K. Digital core processes those streams and outputs K streams. Column 4, lines 17-43 also discloses digital core 112 may generate delayed and optionally processed versions of parallel signals. Therefore, computational circuitry performs a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams. Zhang further discloses K streams are input to mux 210. Further processing of these K streams is conducted and a serial data stream is generated for serial output signal 246

or signal 248. Therefore, Zhang discloses converting the second plurality of parallel data streams, by a serializer, into a second serial data stream.

Applicant states in Zhang, under the examiner's interpretation, this second set of parallel data stream is provided to the FIFO 232 and then to multiplexer 210 which provides a third set of parallel data streams, designated as L, that are provided to serializer 212. Thus, in Zhang, if K is considered the second plurality of parallel data streams, it is not converted into a second serial data stream as is required by amended claim 1 in pages 5-6. The examiner disagrees. Figure 6 of Zhang shows the converting of the second plurality of parallel data streams, by a serializer, into a second serial data stream. Amended claim 1 does not exclude additional processing of the second parallel data streams that is used in the process of converting the second plurality of parallel data streams, by a serializer, into a second serial data stream and therefore, the processing of the K streams to a serial stream meets the claimed limitations. In addition, block 207 of figure 6 of Zhang can be labelled a serializer. This serializer (block 207) receives the K parallel streams and converts the K parallel streams into a serial output signal 248. This serializer (block 207) will carry out the "converting the second plurality of parallel data streams, by a serializer, into a second serial data stream".

As stated in the interview summary, Zhang does not use clock domain operations that delay processing of the first set of parallel data streams. For example, Zhang does not utilize a plurality of serial FIFO buffers in FIFO buffer 232 of figure 6. Since a plurality of FIFO buffers are not utilized, Zhang does not use the clock domain crossing operations that delay processing of a set of parallel data streams that would be present

in the second or third or more FIFO buffers if a plurality of FIFO buffers were taught in Zhang.

The double patenting rejections are not addressed in the response received 1/23/2024. The double patenting rejections are maintained for the reasons stated in the rejections below.

For these reasons, the rejections of the claims are stated below.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis (i.e., changing from AIA to pre-AIA) for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-12 are rejected under 35 U.S.C. 103 as being unpatentable over Zheng et al (US 8,873,606) in view of Cho et al (US 2018/0027431).

Regarding claim 1, Zheng discloses a method for processing a first serial data stream **(Figure 6: input 234)**, using a system **(Figure 6)**, to generate a second serial data stream **(Figure 6L output 248)**, wherein the method comprises the steps of:

(a) receiving, by a deserializer, a clock signal **(Figure 6: serial to parallel converter 204 received clock 250.)**;

(b) receiving, by the deserializer, the first serial data stream **(Figure 6: serial to parallel converter 204 receives the serial data stream.)**;

(c) generating, by the deserializer, a receiver side clock signal **(Figure 6: The serializer comprises at least serial to parallel converter 204 and clock divider 224. Clock divider 224 generates a clock 258.)**;

(d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams **(Figure 6: The serializer comprises at least serial to parallel converter 204 converts a serial stream to parallel streams.)**;

(e) transmitting, from the deserializer to computational circuitry, the first plurality of parallel data streams **(Figure 6: The serializer comprises at least serial to parallel converter 204. The parallel streams are transmitted to demux 206 and then to digital core 208.)**;

(f) transmitting, from the deserializer to a phase lock loop, the receiver side clock signal **(Figure 6: The serializer comprises at least serial to parallel converter 204 and clock divider 224. Clock divider 224 generates a clock 258. Clock 258 is transmitted to phase detector 604.)**;

(g) generating, using the phase lock loop, a transmitter side clock signal **(Figure 6: the phase lock loop comprises PLL 230, element 226 and clock divider 228 and generates clock 262.)**;

(h) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams **(Figure 6: demux 206 receives the first plurality of parallel streams from S/P 204 and generates a second plurality of parallel streams K. Digital core processes those streams. Column 4, lines 17-43: Digital core 112 may generate delayed and optionally processed versions of parallel signals.)**;

(i) converting the second plurality of parallel data streams, by a serializer, into a second serial data stream **(Figure 6: block 207: receives the K parallel data streams and outputs the serial output signal 248.)** and

(j) transmitting, from the system, the second serial data stream, derived from the second plurality of parallel data streams **(figure 6: parallel to serial converter 212 will convert the parallel streams to a serial stream. The serial stream is transmitted on line 246 and then output from the system.)**,

wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams **(Zheng does not disclose using clock domain crossing operations in figure 6.)**.

Zheng does not disclose the method for processing a first serial data stream uses a field programmable gate array system.

Cho discloses the circuit of figure 2. Figure 2 discloses the use of SERDES 26. Paragraph 0055 discloses the SERDES 26 may be implemented in a field

programmable gate array (FPGA). The use of FPGA to reduce the size of the circuit and to improve energy efficiency of the circuit is well known. For these reasons, it would have been obvious for one of ordinary skill in the art before the effective filing date of the claimed invention to implement the circuit of Zheng on an FPGA as taught by Cho.

Regarding claim 2, the combination can process any data content that is received in the circuit. In addition, the data content does not require steps to be performed and therefore doesn't limit the claims in terms of scope. The set of operations is associated with buffering and processing data. These sets can be associated with any type of algorithm including a trading algorithm so that the data is buffered and processed properly to then carry out subsequent steps.

Regarding claim 3, the combination can process any data content that is received in the circuit. In addition, the data content does not require steps to be performed and therefore doesn't limit the claims in terms of scope.

Regarding claim 4, the combination discloses wherein the set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation **(Zheng: Figure 6: demux 206 receives the first plurality of parallel streams from S/P 204 and generates a second plurality of parallel streams K. Digital core processes those streams. Column 4, lines 17-43: Digital core 112 may generate delayed and optionally processed versions of parallel signals.)**.

Regarding claims 5-7, the combination discloses the steps as stated above. Figure 6 of Zheng does not show the order of the steps that are carried out. However, it would have been obvious for one of ordinary skill in the art before the effective filing

date of the claimed invention to carry out the steps in the most efficient manner available. Attempting the steps in each possible order will determine which order is the most efficient and effective. It would have been obvious to try each of these orders of the steps to achieve this goal. The number of possible orders are few and the results would reduce power consumption and improve the operation of the system.

Regarding claim 8, the combination discloses wherein step (g) further comprises:

(i) generating, by the phase lock loop, a feedback clock signal associated with the transmitter side clock signal by performing the following steps until a first output of a phase detector of the system is below a first threshold level **(Zheng: figure 8: shows a flowchart providing example steps for phase aligning a divided transmitter clock with a divided receiver clock signal.)**:

(1) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal **(Zheng: figure 6: phase interpolators receive clock signals and output adjusted clock signals.)**;

(2) generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal **(Zheng: figure 8: detect a phase difference between the first clock and the second clock 806.)**;

(3) transmitting, from the phase detector to a phase controller of the system, the first output **(Zheng: figure 8: transmit a phase difference to a digital core in response to detecting the phase difference 808.)**;

(4) determining, by the phase controller, interim adjustment information based on the first output; and (5) transmitting, from the phase controller to the adjustable

oscillator, the interim adjustment information **(Zheng: figure 8: receive a control signal from the digital core, the control signal being generated by using at least the phase difference signal 810.)**;

wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information **(Zheng: figure 6: phase adjust, by the second phase interpolator, the second clock signal according to the control signal 812.)**, wherein steps (1) through (5) are repeated until the first output of the phase detector is below the first threshold level, and wherein the transmitter side clock signal is associated with the second clock signal **(Zheng: the steps of figure 8 will be repeated when a phase difference is detected. The precision for determining if a phase difference has occurred will be the threshold so that when the phase difference is below that threshold, the adjustments will be stopped.)**.

Regarding claim 9, the combination discloses wherein the first plurality of data streams has the same number of data streams as the second plurality of data streams **(Zheng: Figure 6: K parallel streams are input to and output from the digital core 208).**

Regarding claim 10, the combination discloses wherein the first plurality of data streams and the second plurality of data streams comprise one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams **(Zheng: column 4, lines 4-6: N parallel data streams where N is any integer greater than or**

equal to two. This any integer will include the numbers of parallel streams listed above.).

Regarding claims 11 and 12, the combination discloses wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and phase and wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and different phases **(Zheng: abstract: a delay locked loop may be used to phase align the transmitter clock of the transceiver with the receiver clock of the transceiver to compensate for a limited phase offset between these clocks. Therefore, when aligned the clocks have the same phase and if the clocks are not aligned, the clocks need to be aligned to correct for the different phases.)**.

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process... may obtain a patent therefor..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the claims that are directed to the same invention so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

4. Claim 8 is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 8 of prior U.S. Patent No. 11/575,381. This is a statutory double patenting rejection.

Regarding claim 8, the difference between the instant claim 8 and the reference claim 8 is the reference discloses a step generating a second clock signal and generating a transmitter side clock derived from the second clock signal. The instant claim 1 discloses generating a transmitter side clock signal and claim 8 discloses generating the second clock signal. Claim 8 of the instant and of the reference discloses the same steps. Claim 8 of the instant recites the transmitter side clock signal is associated with the second clock signal. Since the invention of claim 8 of the instant application is the same invention as the invention of claim 8 of the reference, the statutory rejection of claim 8 is applied.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.

Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The filing of a terminal disclaimer by itself is not a complete reply to a nonstatutory double patenting (NSDP) rejection. A complete reply requires that the terminal disclaimer be accompanied by a reply requesting reconsideration of the prior Office action. Even where the NSDP rejection is provisional the reply must be complete. See MPEP § 804, subsection I.B.1. For a reply to a non-final Office action, see 37 CFR 1.111(a). For a reply to final Office action, see 37 CFR 1.113(c). A request for reconsideration while not provided for in 37 CFR 1.113(c) may be filed after final for consideration. See MPEP §§ 706.07(e) and 714.13.

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The actual filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25,

PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/apply/applying-online/eterminal-disclaimer.

5. Claims 1-7 and 9-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-7 and 9-12 of U.S. Patent No. 11,575,381. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader. Claims 1-7 and 9-12 of the instant application correspond to claims 1-7 and 9-12 of the reference.

6. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 12-14, 18-20 and 22 of U.S. Patent No. 10,826,502. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 and 12 of the reference.

Claim 2 of the instant application correspond to claim 22 of the reference.

Claim 3 of the instant application correspond to claim 23 of the reference.

Claim 4 of the instant application correspond to claim 1 of the reference.

Claim 5 of the instant application correspond to claim 18 of the reference.

Claim 6 of the instant application correspond to claim 19 of the reference.

Claim 7 of the instant application correspond to claim 20 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 13 of the reference.

Claim 10 of the instant application correspond to claim 14 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

7. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 10-12, 16-18 and 20 of U.S. Patent No. 10,931,286. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 and 10 of the reference.

Claim 2 of the instant application correspond to claim 20 of the reference.

Claim 3 of the instant application correspond to claim 20 of the reference.

Claim 4 of the instant application correspond to claim 1 of the reference.

Claim 5 of the instant application correspond to claim 16 of the reference.

Claim 6 of the instant application correspond to claim 17 of the reference.

Claim 7 of the instant application correspond to claim 18 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 11 of the reference.

Claim 10 of the instant application correspond to claim 12 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

8. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 4, 5, 8-10 and 20 of U.S. Patent No. 11,128,305. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 of the reference.

Claim 2 of the instant application correspond to claim 20 of the reference.

Claim 3 of the instant application correspond to claim 20 of the reference.

Claim 4 of the instant application correspond to claim 8 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 9 of the reference.

Claim 10 of the instant application correspond to claim 10 of the reference.

Claim 11 of the instant application correspond to claim 4 of the reference.

Claim 12 of the instant application correspond to claim 5 of the reference.

The reference does not disclose the limitations of claims 5-7. However, it would have been obvious for one of ordinary skill in the art before the effective filing date of

the claimed invention to carry out the steps in the most efficient manner available. Attempting the steps in each possible order will determine which order is the most efficient and effective. It would have been obvious to try each of these orders of the steps to achieve this goal. The number of possible orders are few and the results would reduce power consumption and improve the operation of the system.

9. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 11, 12, 16-18 and 20 of U.S. Patent No. 11,502,694. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 of the reference.

Claim 2 of the instant application correspond to claim 20 of the reference.

Claim 3 of the instant application correspond to claim 20 of the reference.

Claim 4 of the instant application correspond to claim 1 of the reference.

Claim 5 of the instant application correspond to claim 16 of the reference.

Claim 6 of the instant application correspond to claim 17 of the reference.

Claim 7 of the instant application correspond to claim 18 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 11 of the reference.

Claim 10 of the instant application correspond to claim 12 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

10. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 5-7, 19 and 20 of U.S. Patent No. 10,763,865. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 of the reference.

Claim 2 of the instant application correspond to claim 19 of the reference.

Claim 3 of the instant application correspond to claim 20 of the reference.

Claim 4 of the instant application correspond to claim 5 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 6 of the reference.

Claim 10 of the instant application correspond to claim 7 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

The reference does not disclose the limitations of claims 5-7. However, it would have been obvious for one of ordinary skill in the art before the effective filing date of the claimed invention to carry out the steps in the most efficient manner available. Attempting the steps in each possible order will determine which order is the most efficient and effective. It would have been obvious to try each of these orders of the steps to achieve this goal. The number of possible orders are few and the results would reduce power consumption and improve the operation of the system.

11. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 5-7, 19 and 20 of U.S. Patent No. 10,771,069. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 of the reference.

Claim 2 of the instant application correspond to claim 21 of the reference.

Claim 3 of the instant application correspond to claim 21 of the reference.

Claim 4 of the instant application correspond to claim 6 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 7 of the reference.

Claim 10 of the instant application correspond to claim 8 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

The reference does not disclose the limitations of claims 5-7. However, it would have been obvious for one of ordinary skill in the art before the effective filing date of the claimed invention to carry out the steps in the most efficient manner available. Attempting the steps in each possible order will determine which order is the most efficient and effective. It would have been obvious to try each of these orders of the steps to achieve this goal. The number of possible orders are few and the results would reduce power consumption and improve the operation of the system.

12. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 6-8, 21 and 22 of U.S. Patent No. 11,018,678. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 of the reference.

Claim 2 of the instant application correspond to claim 21 of the reference.

Claim 3 of the instant application correspond to claim 22 of the reference.

Claim 4 of the instant application correspond to claim 6 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 7 of the reference.

Claim 10 of the instant application correspond to claim 8 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

The reference does not disclose the limitations of claims 5-7. However, it would have been obvious for one of ordinary skill in the art before the effective filing date of the claimed invention to carry out the steps in the most efficient manner available. Attempting the steps in each possible order will determine which order is the most efficient and effective. It would have been obvious to try each of these orders of the steps to achieve this goal. The number of possible orders are few and the results would reduce power consumption and improve the operation of the system.

13. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 11, 12, 16-18 and 20 of U.S. Patent No. 11,329,655. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 of the reference.

Claim 2 of the instant application correspond to claim 24 of the reference.

Claim 3 of the instant application correspond to claim 25 of the reference.

Claim 4 of the instant application correspond to claim 7 of the reference.

Claim 5 of the instant application correspond to claim 13 of the reference.

Claim 6 of the instant application correspond to claim 14 of the reference.

Claim 7 of the instant application correspond to claim 15 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 8 of the reference.

Claim 10 of the instant application correspond to claim 9 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. BURD whose telephone number is (571)272-3008. The examiner can normally be reached 9:30 - 5:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and

https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KEVIN M BURD/
Primary Examiner, Art Unit 2632
1/31/2024

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,130	Badizadegan, Nima
	Examiner	Art Unit
	KEVIN M BURD	2632

CPC - Searched*		
Symbol	**Date**	**Examiner**
H03L7/085;	10/24/2023	KMB
H03K19/1774	10/24/2023	KMB
H04B 1/40	10/24/2023	KMB
H03M 9/00	10/24/2023	KMB
G06F13/4291	10/24/2023	KMB
H03L7/085;	01/31/2024	KMB
H03K19/1774	01/31/2024	KMB
H04B 1/40	01/31/2024	KMB
H03M 9/00	01/31/2024	KMB
G06F13/4291	01/31/2024	KMB

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**
	10/24/2023	KMB

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
375	219		
375	219		

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,130	Badizadegan, Nima
	Examiner	**Art Unit**
	KEVIN M BURD	2632

Search Notes		
Search Notes	**Date**	**Examiner**
search search	10/24/2023	KMB
inventor name search	10/24/2023	KMB
NPL (google) search	10/24/2023	KMB
updated inventor name search	01/31/2024	KMB

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L181	35596	(375/219.ccls.) (H03I7/085.cpc.) (g06f13/4291.cpc.) (H03M9/00.cpc.) (H04b1/40.cpc.) (H03k19/1774.cpc.)	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	OFF	OFF	2023/10/23 04:27 PM
L182	46	181 AND (((deserializ$5 OR (serial ADJ parallel)) SAME (serializ$5 OR (parallel ADJ serial))) SAME phase near3 detect$5)	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	OFF	OFF	2023/10/23 04:27 PM
L200	2	"8873606".pn.	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2024/01/30 03:37 PM
L201	46	181 AND (((deserializ$5 OR (serial ADJ parallel)) SAME (serializ$5 OR (parallel ADJ serial))) SAME phase near3 detect$5)	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	OFF	OFF	2024/01/31 02:30 PM
L202	9	((("BADIZADEGAN") near3 ("Nima"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2024/01/31 02:30 PM
L203	3	((("HFT") near3 ("SOLUTIONS") near3 ("LLC"))).AS,AANM.	(USPAT)	OR	ON	ON	2024/01/31 02:30 PM
L204	3	((("HFT") near3 ("SOLUTIONS") near3 ("LLC"))).AS,AANM.	(US-PGPUB; USPAT)	OR	ON	ON	2024/01/31 02:30 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/723,130	**01/23/2024 01:04:49 PM Z ET**	**00287-0016**

Title of Invention

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3228	FILED BY	Victoria GILMORE
PATENT CENTER #	64051958	FILING DATE	04/18/2022
CUSTOMER #	1912	FIRST NAMED INVENTOR	Nima Badizadegan
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Keith Barkaus

Documents

TOTAL DOCUMENTS: 3

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
1-ResponsetoNFOA.pdf		8	-	136 KB
1-ResponsetoNFOA-A...pdf	(1-1)	1	Amendment/Request for Reconsideration-After Non-Final Rejection	102 KB
1-ResponsetoNFOA-CLM.pdf	(2-4)	3	Claims	106 KB
1-ResponsetoNFOA-REM.pdf	(5-8)	4	Applicant Arguments/Remarks Made in an Amendment	126 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
1-ResponsetoNFOA.pdf	59060849D658F40D57FF0723F55F1199265724DBA839594AAA F9369F073861716 8C62377D40675FDABAFF480EDDE6753BE6 F20D1D16C5047548C6A12E882BAA5
1-ResponsetoNFOA-A....pdf	E9A06152867FA8C9A3F0D0731202DAF41C239A9A23F8D904C 70EE694011F991B0A916A2DA661AA86CB84824A55934500F35 68E8697D440AD513C5501B70CB96E
1-ResponsetoNFOA-CLM.pdf	D80A0414CA9F346142B6AC249AF1B4A59074F0D59F09D7ECD FD5E28BBA5D8AE6056EF040DD850ABCF46258167B77F55EE6 6AF267C36C94BA072EFC75C3CC0412
1-ResponsetoNFOA-REM.pdf	1D13F5449E6265EA413B487476C930F7822EB5EAFAF1F20666 1818053719C1C0985A14DBD6A0111499E7676C4EB716128792 D9C0534EACE7167DB455C62B16AE

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	: 17/723,130	Confirmation No. 3228
Applicant	: HFT Solutions, LLC	
Filing Date	: April 18, 2022	
Title	: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	
Examiner	: Kevin Michael Burd	
Group A.U.	: 2632	
Docket No.	: 00287-0016	
Customer No.	: 1912	

AMENDMENT IN RESPONSE TO OFFICE ACTION DATED

Sir:

This is a response to the Office Action dated October 26, 2023. A response to the Office Action is due January 26, 2024 such that the present Amendment is being timely filed.

Amendments to the claims begin on page **2**.

Remarks begin on page **5**.

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:

(a) receiving, by a deserializer in a field programmable array, a clock signal;

(b) receiving, by the deserializer, the first serial data stream;

(c) generating, by the deserializer, a receiver side clock signal;

(d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;

(e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;

(f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;

(g) generating, using the phase lock loop, a transmitter side clock signal;

(h) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams; [[and]]

(i) converting the second plurality of parallel data streams, by a serializer, into a second serial data stream; and

(j) transmitting, from the field programmable gate array system, the second serial data stream,

wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

2. (Original) The method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the set of operations are associated with a trading algorithm.

3. (Original) The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.

4. (Original) The method of claim 1, wherein the set of operations includes at least one of the following:

(i) an arithmetic operation;

(ii) a logical operation;

(iii) a pipeline operation; and

(iv) a memory access operation.

5. (Original) The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed prior to step (g).

6. (Original) The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed after step (g).

7. (Original) The method of claim 1, wherein all of the set of operations performed in step (h) are performed after step (g).

8. (Currently Amended) The method of claim 1, wherein step (g) further comprises:

[[(i)]] (k) generating, by the phase lock loop, a feedback clock signal associated with the transmitter side clock signal by performing the following steps until a first output of a phase detector of the field programmable gate array system is below a first threshold level:

(1) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal;

(2) generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal;

(3) transmitting, from the phase detector to a phase controller of the field programmable gate array system, the first output;

(4) determining, by the phase controller, interim adjustment information based on the first output; and

(5) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information;

wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information,

wherein steps (1) through (5) are repeated until the first output of the phase detector is below the first threshold level, and

wherein the transmitter side clock signal is associated with the second clock signal.

9. (Original) The method of claim 1, wherein the first plurality of data streams has the same number of data streams as the second plurality of data streams.

10. (Original) The method of claim 1, wherein the first plurality of data streams and the second plurality of data streams comprise one of the following:

(i) eight (8) data streams;

(ii) ten (10) data streams;

(iii) sixteen (16) data streams;

(iv) twenty (20) data streams;

(v) thirty-two (32) data streams;

(vi) forty (40) data streams;

(vii) sixty-four (64) data streams;

(viii) eighty (80) data streams;

(ix) one hundred twenty-eight (128) data streams; and

(x) one hundred sixty (160) data streams.

11. (Original) The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and phase.

12. (Original) The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and different phases.

REMARKS

This is a response to the Office Action dated October 26, 2023. Claims 1-12 are pending in the present application with claim 1, in independent form. Applicant has amended claims 1 and 8, herein, to further clarify the features thereof and address formal matters. No new matter has been added.

Claims 1-12 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 8,873,606 to Zhang et al. ("Zhang") in view of U.S. Patent Application Publication No. 2018/0027431 to Cho et al. ("Cho"), Applicant respectfully requests reconsideration of this rejection.

Applicant appreciates the courtesy extended to Applicant's undersigned attorney and Charles R. Macedo during the telephone interview of November 14, 2023. During the interview, Applicant's attorneys noted that the Zhang reference shows FIFO 232, which is part of the digital core 208, and is also a clock domain crossing circuit that delays processing of parallel signals. Thus, Zhang uses clock domain crossing operations in contrast to the requirement in claim 1 that "the method does not use clock domain crossing operations that delay processing of the first set of parallel data streams."

The Examiner noted that the demux 206 generates the second set of parallel streams in Zhang and does not use clock domain crossing operations to do so. The Examiner also noted that the term "clock domain crossing operations" is not defined in the claims such that the Examiner was "unsure what the scope of the wherein clause of claim 1 is." Interview Summary, p. 2. The Examiner noted that it was unclear "which operations were excluded." *Id.* No agreement was reached during the telephone interview.

Applicant respectfully submits that Zhang does not disclose, show or suggest "performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams," and "converting the second plurality of parallel data streams, by a serializer, into a second serial data stream," as is required by amended claim 1.

The Examiner contends that the output of the demux 206, designated as K in FIG. 6, corresponds to the "second plurality of parallel data streams." However, in Zhang, under the examiner's interpretation, this second set of parallel data streams is provided to the FIFO 232 and then to the multiplexer 210 which provides a third set of parallel data streams, designated as

L, that are provided to the serializer 212. Thus, in Zhang, if K is considered "the second plurality of parallel data streams," it is not converted "into a second serial data stream," as is required by amended claim 1.

For this reason alone, amended claim 1 is believed to be patentable over the cited art.

With respect to the Examiner's concerns regarding the scope of the term "clock domain crossing operations" in claim 1, Applicant notes that, as used in claim 1, "clock domain crossing operations" are operations on the data used to pass the data between clock domains that add latency above and beyond the phase difference between the transmitter side clock signal and the receiver side clock signal. Support for this explanation can be found at least in Paragraph [0291] of the present application which discusses examples of clock domain crossing circuits, which use clock domain crossing operations, including "an asynchronous FIFO" such as the FIFO 232 used in Zhang, for example. Such an asynchronous FIFO includes operations (*e.g.* a memory write, a memory read, and a synchronization operation) that add latency associated with a synchronizer above and beyond the phase difference between the transmitter side clock signal and the receiver side clock signal.

Cho fails to address the shortcomings of Zhang discussed above.

Accordingly, Applicant respectfully submits that claim 1, and the claims depending therefrom, including claims 2-12, are patentable over the cited art for at least the reasons discussed above.

In light of the remarks and amendments herein, Applicant respectfully submits that claims 1-12 are patentable over the prior art and are in condition for allowance.

Reference to Related Patents and Co-Pending Applications

The below chart provides information regarding related issued patents and co-pending applications filed by the present Applicant:

SERIAL NO.	ATTORNEY DOCKET NO.	FILING DATE	STATUS
16/672,076	00287-0007	2019-11-01	Issued USP 10,826,502
16/670,702	00287-0008	2019-10-31	Issued USP 10,771,069
16/888,218	00287-0009	2020-05-29	Issued USP 10,763,865
16/937,314	00287-0011	2020-07-23	Issued USP 10,931,286
16/937,309	00287-0012	2020-07-23	Issued USP 11,018,678

SERIAL NO.	ATTORNEY DOCKET NO.	FILING DATE	STATUS
17/248,304	00287-0013	2021-01-19	Issued USP 11,128,305
17/236,577	00287-0014	2021-04-21	Issued USP 11,329,655
17/405,188	00287-0015	2021-08-18	Issued USP 11,502,381
17/723,130	**00287-0016**	**2022-04-18**	**Present Application**
17/723,145	00287-0017	2022-04-18	Issued USP 11,575,381
18/067,332	00287-0018	2022-12-16	Docketed New Case - Ready for Examination

The Examiner is invited to review the prosecution history of each of these applications, including the cited references of record and related office actions, as the Examiner deems appropriate.

The Examiner is invited to review the prosecution history of each of these applications, including the cited references of record and related office actions, as the Examiner deems appropriate.

CONCLUSION

In view of the foregoing, Applicant respectfully submits that all pending claims are patentable over the cited art and in condition for allowance. Reconsideration and prompt allowance of this application are both respectfully solicited.

Applicant respectfully asserts that the foregoing constitutes a bona fide response to all outstanding objections and rejections within this Office Action.

This application is in condition for immediate allowance. However, should any issue(s) of a minor nature remain, the Examiner is respectfully requested to telephone the undersigned at telephone number (212) 336-8000 so that the issue(s) might be promptly resolved.

Favorable reconsideration of the present application is respectfully requested.

* * * * * *

Any claim amendment(s), claim(s) added, claim(s) canceled, argument(s), remark(s), and/or any combination(s) thereof made in this response pertain solely to the specific aspects of this specific claimed invention. Further, any claim amendment(s), claim(s) added, claim(s) canceled, argument(s), remark(s), and/or any combination(s) thereof are made without prejudice

to or disclaimer of Applicant's right to seek patent protection of any unclaimed subject matter such as, but not limited, to narrower unclaimed subject matter, broader unclaimed subject matter, different unclaimed subject matter, variations of unclaimed subject matter, any combination thereof, and/or any other unclaimed subject matter that may or may not be filed, for example, in any design and/or utility patent application(s) such as, but not limited to, continuation patent application(s), continuation-in-part patent application(s), and/or divisional patent application(s) and/or any other patent application(s).

Applicant's silence as to any assertion(s) by the Examiner in the Office Action and/or to any certain fact(s) or conclusion(s) that may be implied and/or alleged by objections(s) and/or rejection(s) in the Office Action is not in any way a concession by Applicant that such assertion(s), implication(s), and/or allegation(s) are accurate, and that all requirements for any objection(s) and/or a rejection(s) have been met. Accordingly, Applicant reserves the right to analyze and dispute any such assertion(s), implication(s), and/or allegation(s) in the future.

Respectfully submitted,

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405 Lexington Avenue
New York, NY 10174
(212) 336-8000

Dated: New York, New York
January 23, 2024

By: /Keith J. Barkaus/
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Registration No.: 51,431
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Registration No.: 32,781

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/723,130	Filing Date 04/18/2022	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	01/23/2024	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 12	Minus	** 20	= 0		x $40 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $192 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/JACKIE A WHITE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
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☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	01/23/2024	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 33	Minus	** 29	= 4		x $40 =	160
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 4	= 0		x $192 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	160

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/JACKIE A WHITE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,130	04/18/2022	Nima Badizadegan	00287-0016	3228

1912 7590 11/15/2023

AMSTER, ROTHSTEIN & EBENSTEIN LLP
405 LEXINGTON AVENUE
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NEW YORK, NY 10174

EXAMINER
BURD, KEVIN MICHAEL

ART UNIT	PAPER NUMBER
2632	

MAIL DATE	DELIVERY MODE
11/15/2023	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Applicant-Initiated Interview Summary	**Application No.** 17/723,130	**Applicant(s)** Badizadegan, Nima		
	Examiner KEVIN M BURD	**Art Unit** 2632	**AIA (First Inventor to File) Status** Yes	**Page** 1 of 2

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
KEVIN M BURD	Primary Examiner	Telephonic
Keith Barkus	Attorney of Record	
Charles Macedo	Attorney of Record	

Date of Interview: 14 November 2023

Issues Discussed:

35 U.S.C. 103

An agenda was received prior to the interview. The previous rejection of claim 1 was discussed. Applicant indicated that Zhang et al (US 8,873,606) discloses the digital core 208 and FIFO buffer 232 that delays the parallel signals and receives both the read clock and write clock and thus must be a clock domain crossing circuit. The examiner indicated that the previous rejection of the claims indicated the demux 206 generates the second set of parallel data streams. The FIFO 232 will perform operations on the second set of parallel data streams and not the first set of parallel data streams. Claim 1 recites said method does not use clock domain crossing operations that delays processing of the first set of parallel data streams. The examiner indicated that the term clock domain crossing operations was not defined in the claim and was unsure what the scope of the wherein clause limitation of claim 1 is. It was unclear to the examiner which operations were excluded. The examiner indicated an example that the reference does not use a plurality of serial FIFO buffers in FIFO buffer 232 of figure 6 of Zhang. Though Zhang discloses using the FIFO 232, Zhang does not use the clock domain crossing operations that delay processing of a set of parallel data streams of these second and third serial FIFO buffers which would delay processing of the parallel streams further. Applicant's representative indicated they will form a response and contact the examiner to discuss that proposed amendment. The previous double patenting rejections were briefly discussed.
No agreement was reached.

☑ Attachment

/KEVIN M BURD/ Primary Examiner, Art Unit 2632	

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a

non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	: 17/723,130	Confirmation No. 3228
Applicant	: HFT Solutions, LLC	
Filing Date	: April 18, 2022	
Title	: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	
Examiner	: Kevin Michael Burd	
Group A.U.	: 2632	
Docket No.	: 00287-16	
Customer No.	: 1912	

INTERVIEW AGENDA

VIA EFS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Examiner Burd:

In advance of the telephone interview scheduled for November 14, 2023 at 3:15 PM ET in regard to the above-identified application, Applicant respectfully requests that the Examiner consider the following agenda.

Claims 1-12 have been rejected as allegedly being unpatentable over U.S. Patent No. 8,873,606 to Zheng in view of U.S. Patent Application Publication No 2018/0027431 to Cho et al. ("Cho"). Applicant respectfully disagrees.

The Examiner refers to FIG. 6 of Zheng as allegedly disclosing most of the features of claim 1, including that "said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams." Office Action, p. 4. This is incorrect.

FIG. 6 of Zheng shows the FIFO 232, which is part of the digital core 208, and is also a clock domain crossing circuit that delays processing of parallel signals.

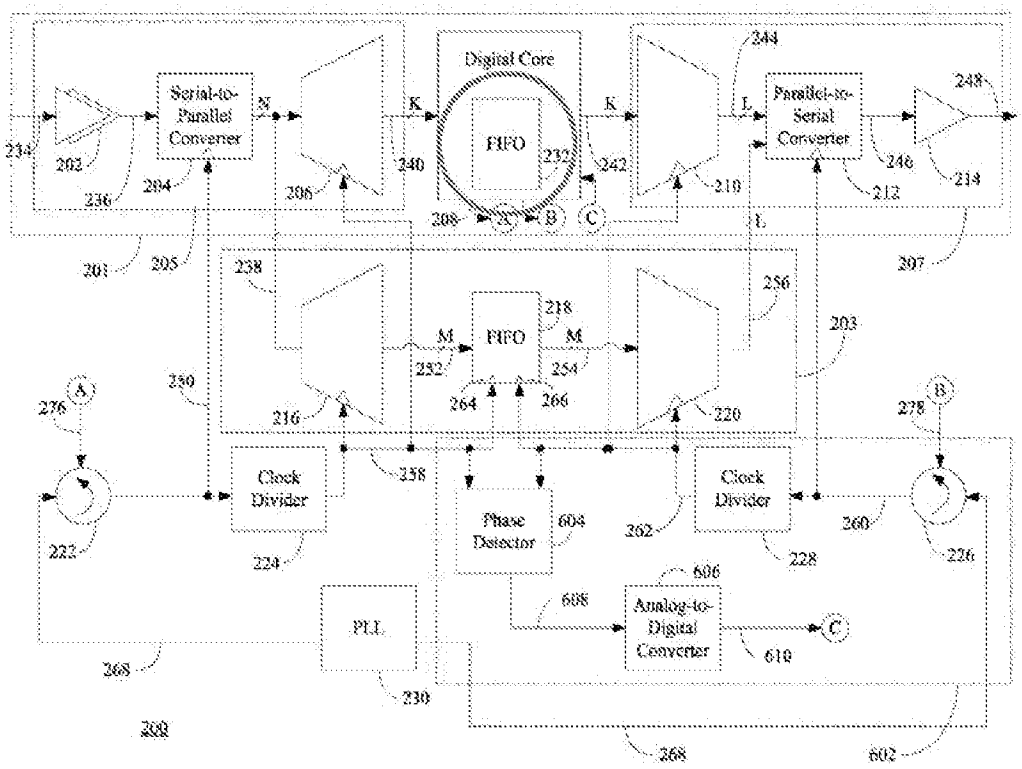


FIG. 6

Indeed, Zheng explicitly states that "[d]igital core 208 may buffer K second parallel signals 240 in **a FIFO 232**..." and that "[d]igital core 208 may generate a **delayed version of second parallel signals 240** (depicted as signals 242) according to the FIFO depth and provide **delayed second parallel signals 242 to transmitter circuit 207** of first communication channel 201." Zheng, Col 7, lines 21-28.

Zheng further explains that the FIFO 232 in FIG. 6 "generally can tolerate a large phase offset between the write clock used to write data to the FIFO and the read clock used to read data

from the FIFO due to the slower speeds at which they operate is connected to." Zheng, Col. 13, lines 23-27. Thus, Zheng discloses that the FIFO 232 is provided with both the read clock and the write clock, and thus, must be a domain crossing circuit. Indeed, the present application explicitly identifies a FIFO, such as FIFO 232, as an example of a domain crossing circuit. See Paragraph [0291] ("The clock domain crossing circuit 112 may be an asynchronous FIFO…").

Accordingly, Zheng explicitly discloses the use of domain crossing operations, contrary to the requirements of claim 1.

Applicant's undersigned attorney looks forward to discussing this issue further during the telephone interview.

Respectfully submitted,

AMSTER, ROTHSTEIN & EBENSTEIN LLP
Attorneys for Applicant
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Dated: New York, New York
November 14, 2023

By: /Keith J. Barkaus/
Keith J. Barkaus
Registration No.: 51,431
Charles R. Macedo
Registration No.: 32,781

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/723,130	04/18/2022	Nima Badizadegan	00287-0016	3228

1912 7590 10/26/2023

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NEW YORK, NY 10174

EXAMINER
BURD, KEVIN MICHAEL

ART UNIT	PAPER NUMBER
2632	

MAIL DATE	DELIVERY MODE
10/26/2023	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 17/723,130	Applicant(s) Badizadegan, Nima	
	Examiner KEVIN M BURD	Art Unit 2632	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 4/18/2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-12 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-12 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 4/18/2022 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis (i.e., changing from AIA to pre-AIA) for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-12 are rejected under 35 U.S.C. 103 as being unpatentable over Zheng et al (US 8,873,606) in view of Cho et al (US 2018/0027431).

Regarding claim 1, Zheng discloses a method for processing a first serial data stream **(Figure 6: input 234)**, using a system **(Figure 6)**, to generate a second serial data stream **(Figure 6L output 248)**, wherein the method comprises the steps of:

(a) receiving, by a deserializer, a clock signal **(Figure 6: serial to parallel converter 204 received clock 250.)**;

(b) receiving, by the deserializer, the first serial data stream **(Figure 6: serial to parallel converter 204 receives the serial data stream.)**;

(c) generating, by the deserializer, a receiver side clock signal **(Figure 6: The serializer comprises at least serial to parallel converter 204 and clock divider 224. Clock divider 224 generates a clock 258.)**;

(d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams **(Figure 6: The serializer comprises at least serial to parallel converter 204 converts a serial stream to parallel streams.)**;

(e) transmitting, from the deserializer to computational circuitry, the first plurality of parallel data streams **(Figure 6: The serializer comprises at least serial to parallel converter 204. The parallel streams are transmitted to demux 206 and then to digital core 208.)**;

(f) transmitting, from the deserializer to a phase lock loop, the receiver side clock signal **(Figure 6: The serializer comprises at least serial to parallel converter 204 and clock divider 224. Clock divider 224 generates a clock 258. Clock 258 is transmitted to phase detector 604.)**;

(g) generating, using the phase lock loop, a transmitter side clock signal **(Figure 6: the phase lock loop comprises PLL 230, element 226 and clock divider 228 and generates clock 262.)**;

(h) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams **(Figure 6: demux 206 receives the first plurality of parallel streams from S/P 204 and generates a second plurality of parallel streams K.**

Digital core processes those streams. Column 4, lines 17-43: Digital core 112 may generate delayed and optionally processed versions of parallel signals.); and

(i) transmitting, from the system, the second serial data stream, derived from the second plurality of parallel data streams **(figure 6: parallel to serial converter 212 will convert the parallel streams to a serial stream. The serial stream is transmitted on line 246 and then output from the system.)**,

wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams **(Zheng does not disclose using clock domain crossing operations in figure 6.)**.

Zheng does not disclose the method for processing a first serial data stream uses a field programmable gate array system.

Cho discloses the circuit of figure 2. Figure 2 discloses the use of SERDES 26. Paragraph 0055 discloses the SERDES 26 may be implemented in a field programmable gate array (FPGA). The use of FPGA to reduce the size of the circuit and to improve energy efficiency of the circuit is well known. For these reasons, it would have been obvious for one of ordinary skill in the art before the effective filing date of the claimed invention to implement the circuit of Zheng on an FPGA as taught by Cho.

Regarding claim 2, the combination can process any data content that is received in the circuit. In addition, the data content does not require steps to be performed and therefore doesn't limit the claims in terms of scope. The set of operations is associated with buffering and processing data. These sets can be associated with any type of algorithm including a trading algorithm so that the data is buffered and processed properly to then carry out subsequent steps.

Regarding claim 3, the combination can process any data content that is received in the circuit. In addition, the data content does not require steps to be performed and therefore doesn't limit the claims in terms of scope.

Regarding claim 4, the combination discloses wherein the set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation **(Zheng: Figure 6: demux 206 receives the first plurality of parallel streams from S/P 204 and generates a second plurality of parallel streams K. Digital core processes those streams. Column 4, lines 17-43: Digital core 112 may generate delayed and optionally processed versions of parallel signals.)**.

Regarding claims 5-7, the combination discloses the steps as stated above. Figure 6 of Zheng does not show the order of the steps that are carried out. However, it would have been obvious for one of ordinary skill in the art before the effective filing date of the claimed invention to carry out the steps in the most efficient manner available. Attempting the steps in each possible order will determine which order is the most efficient and effective. It would have been obvious to try each of these orders of the steps to achieve this goal. The number of possible orders are few and the results would reduce power consumption and improve the operation of the system.

Regarding claim 8, the combination discloses wherein step (g) further comprises:

(i) generating, by the phase lock loop, a feedback clock signal associated with the transmitter side clock signal by performing the following steps until a first output of a phase detector of the system is below a first threshold level **(Zheng: figure 8: shows a**

flowchart providing example steps for phase aligning a divided transmitter clock with a divided receiver clock signal.):

(1) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal **(Zheng: figure 6: phase interpolators receive clock signals and output adjusted clock signals.)**;

(2) generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal **(Zheng: figure 8: detect a phase difference between the first clock and the second clock 806.)**;

(3) transmitting, from the phase detector to a phase controller of the system, the first output **(Zheng: figure 8: transmit a phase difference to a digital core in response to detecting the phase difference 808.)**;

(4) determining, by the phase controller, interim adjustment information based on the first output; and (5) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information **(Zheng: figure 8: receive a control signal from the digital core, the control signal being generated by using at least the phase difference signal 810.)**;

wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information **(Zheng: figure 6: phase adjust, by the second phase interpolator, the second clock signal according to the control signal 812.)**, wherein steps (1) through (5) are repeated until the first output of the phase detector is below the first threshold level, and wherein the transmitter side clock signal is associated with the second clock signal **(Zheng: the steps of figure 8 will be repeated when a phase**

difference is detected. The precision for determining if a phase difference has occurred will be the threshold so that when the phase difference is below that threshold, the adjustments will be stopped.).

Regarding claim 9, the combination discloses wherein the first plurality of data streams has the same number of data streams as the second plurality of data streams **(Zheng: Figure 6: K parallel streams are input to and output from the digital core 208).**

Regarding claim 10, the combination discloses wherein the first plurality of data streams and the second plurality of data streams comprise one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams **(Zheng: column 4, lines 4-6: N parallel data streams where N is any integer greater than or equal to two. This any integer will include the numbers of parallel streams listed above.)**.

Regarding claims 11 and 12, the combination discloses wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and phase and wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and different phases **(Zheng: abstract: a delay locked loop may be used to phase align the transmitter clock of the transceiver with the receiver clock of the transceiver to compensate for a limited phase offset between these**

clocks. Therefore, when aligned the clocks have the same phase and if the clocks are not aligned, the clocks need to be aligned to correct for the different phases.).

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process... may obtain a patent therefor..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the claims that are directed to the same invention so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

2. Claim 8 is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 8 of prior U.S. Patent No. 11/575,381. This is a statutory double patenting rejection.

Regarding claim 8, the difference between the instant claim 8 and the reference claim 8 is the reference discloses a step generating a second clock signal and generating a transmitter side clock derived from the second clock signal. The instant claim 1 discloses generating a transmitter side clock signal and claim 8 discloses

generating the second clock signal. Claim 8 of the instant and of the reference discloses the same steps. Claim 8 of the instant recites the transmitter side clock signal is associated with the second clock signal. Since the invention of claim 8 of the instant application is the same invention as the invention of claim 8 of the reference, the statutory rejection of claim 8 is applied.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See

MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The filing of a terminal disclaimer by itself is not a complete reply to a nonstatutory double patenting (NSDP) rejection. A complete reply requires that the terminal disclaimer be accompanied by a reply requesting reconsideration of the prior Office action. Even where the NSDP rejection is provisional the reply must be complete. See MPEP § 804, subsection I.B.1. For a reply to a non-final Office action, see 37 CFR 1.111(a). For a reply to final Office action, see 37 CFR 1.113(c). A request for reconsideration while not provided for in 37 CFR 1.113(c) may be filed after final for consideration. See MPEP §§ 706.07(e) and 714.13.

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The actual filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/apply/applying-online/eterminal-disclaimer.

3. Claims 1-7 and 9-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-7 and 9-12 of U.S. Patent No. 11,575,381.

Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader. Claims 1-7 and 9-12 of the instant application correspond to claims 1-7 and 9-12 of the reference.

4. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 12-14, 18-20 and 22 of U.S. Patent No. 10,826,502. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 and 12 of the reference.

Claim 2 of the instant application correspond to claim 22 of the reference.

Claim 3 of the instant application correspond to claim 23 of the reference.

Claim 4 of the instant application correspond to claim 1 of the reference.

Claim 5 of the instant application correspond to claim 18 of the reference.

Claim 6 of the instant application correspond to claim 19 of the reference.

Claim 7 of the instant application correspond to claim 20 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 13 of the reference.

Claim 10 of the instant application correspond to claim 14 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

5. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 10-12, 16-18 and 20 of U.S. Patent No. 10,931,286. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 and 10 of the reference.

Claim 2 of the instant application correspond to claim 20 of the reference.

Claim 3 of the instant application correspond to claim 20 of the reference.

Claim 4 of the instant application correspond to claim 1 of the reference.

Claim 5 of the instant application correspond to claim 16 of the reference.

Claim 6 of the instant application correspond to claim 17 of the reference.

Claim 7 of the instant application correspond to claim 18 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 11 of the reference.

Claim 10 of the instant application correspond to claim 12 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

6. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 4, 5, 8-10 and 20 of U.S. Patent No. 11,128,305. Although

the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 of the reference.

Claim 2 of the instant application correspond to claim 20 of the reference.

Claim 3 of the instant application correspond to claim 20 of the reference.

Claim 4 of the instant application correspond to claim 8 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 9 of the reference.

Claim 10 of the instant application correspond to claim 10 of the reference.

Claim 11 of the instant application correspond to claim 4 of the reference.

Claim 12 of the instant application correspond to claim 5 of the reference.

The reference does not disclose the limitations of claims 5-7. However, it would have been obvious for one of ordinary skill in the art before the effective filing date of the claimed invention to carry out the steps in the most efficient manner available. Attempting the steps in each possible order will determine which order is the most efficient and effective. It would have been obvious to try each of these orders of the steps to achieve this goal. The number of possible orders are few and the results would reduce power consumption and improve the operation of the system.

7. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 11, 12, 16-18 and 20 of U.S. Patent No. 11,502,694.

Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 of the reference.

Claim 2 of the instant application correspond to claim 20 of the reference.

Claim 3 of the instant application correspond to claim 20 of the reference.

Claim 4 of the instant application correspond to claim 1 of the reference.

Claim 5 of the instant application correspond to claim 16 of the reference.

Claim 6 of the instant application correspond to claim 17 of the reference.

Claim 7 of the instant application correspond to claim 18 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 11 of the reference.

Claim 10 of the instant application correspond to claim 12 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

8. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 5-7, 19 and 20 of U.S. Patent No. 10,763,865. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 of the reference.

Claim 2 of the instant application correspond to claim 19 of the reference.

Claim 3 of the instant application correspond to claim 20 of the reference.

Claim 4 of the instant application correspond to claim 5 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 6 of the reference.

Claim 10 of the instant application correspond to claim 7 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

The reference does not disclose the limitations of claims 5-7. However, it would have been obvious for one of ordinary skill in the art before the effective filing date of the claimed invention to carry out the steps in the most efficient manner available. Attempting the steps in each possible order will determine which order is the most efficient and effective. It would have been obvious to try each of these orders of the steps to achieve this goal. The number of possible orders are few and the results would reduce power consumption and improve the operation of the system.

9. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 5-7, 19 and 20 of U.S. Patent No. 10,771,069. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 of the reference.

Claim 2 of the instant application correspond to claim 21 of the reference.

Claim 3 of the instant application correspond to claim 21 of the reference.

Claim 4 of the instant application correspond to claim 6 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 7 of the reference.

Claim 10 of the instant application correspond to claim 8 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

The reference does not disclose the limitations of claims 5-7. However, it would have been obvious for one of ordinary skill in the art before the effective filing date of the claimed invention to carry out the steps in the most efficient manner available. Attempting the steps in each possible order will determine which order is the most efficient and effective. It would have been obvious to try each of these orders of the steps to achieve this goal. The number of possible orders are few and the results would reduce power consumption and improve the operation of the system.

10. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 6-8, 21 and 22 of U.S. Patent No. 11,018,678. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 of the reference.

Claim 2 of the instant application correspond to claim 21 of the reference.

Claim 3 of the instant application correspond to claim 22 of the reference.

Claim 4 of the instant application correspond to claim 6 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 7 of the reference.

Claim 10 of the instant application correspond to claim 8 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

The reference does not disclose the limitations of claims 5-7. However, it would have been obvious for one of ordinary skill in the art before the effective filing date of the claimed invention to carry out the steps in the most efficient manner available. Attempting the steps in each possible order will determine which order is the most efficient and effective. It would have been obvious to try each of these orders of the steps to achieve this goal. The number of possible orders are few and the results would reduce power consumption and improve the operation of the system.

11. Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3, 11, 12, 16-18 and 20 of U.S. Patent No. 11,329,655. Although the claims at issue are not identical, they are not patentably distinct from each other because the reference discloses each of the limitations of the reference. The reference discloses additional limitations not recited in the reference. The more specific anticipates the broader.

Claim 1 of the instant application correspond to claim 1 of the reference.

Claim 2 of the instant application correspond to claim 24 of the reference.

Claim 3 of the instant application correspond to claim 25 of the reference.

Claim 4 of the instant application correspond to claim 7 of the reference.

Claim 5 of the instant application correspond to claim 13 of the reference.

Claim 6 of the instant application correspond to claim 14 of the reference.

Claim 7 of the instant application correspond to claim 15 of the reference.

Claim 8 of the instant application correspond to claim 1 of the reference.

Claim 9 of the instant application correspond to claim 8 of the reference.

Claim 10 of the instant application correspond to claim 9 of the reference.

Claim 11 of the instant application correspond to claim 2 of the reference.

Claim 12 of the instant application correspond to claim 3 of the reference.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. BURD whose telephone number is (571)272-3008. The examiner can normally be reached 9:30 - 5:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/KEVIN M BURD/
Primary Examiner, Art Unit 2632
10/24/2023

Notice of References Cited	Application/Control No. 17/723,130	Applicant(s)/Patent Under Reexamination Badizadegan, Nima	
	Examiner KEVIN M BURD	Art Unit 2632	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-8873606-B2	10-2014	Zhang; Heng	H03D3/006	375/295
*	B	US-20180027431-A1	01-2018	CHO; Youngman	H04W24/04	455/424
*	C	US-11575381-B1	02-2023	Badizadegan; Nima	H04L7/0331	1/1
*	D	US-10826502-B1	11-2020	Badizadegan; Nima	G06F30/34	1/1
*	E	US-10771069-B1	09-2020	Badizadegan; Nima	H03M9/00	1/1
*	F	US-10931286-B1	02-2021	Badizadegan; Nima	H03L7/085	1/1
*	G	US-11128305-B1	09-2021	Badizadegan; Nima	H03L7/0812	1/1
*	H	US-10763865-B1	09-2020	Badizadegan; Nima	G06F13/4291	1/1
*	I	US-11018678-B1	05-2021	Badizadegan; Nima	G06F13/4291	1/1
*	J	US-11329655-B1	05-2022	Badizadegan; Nima	H04B1/40	1/1
*	K	US-11502894-B2	11-2022	Mohan; Mahesh Kumar	H04L41/0654	1/1
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FOREIGN PATENT DOCUMENTS

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,130	Badizadegan, Nima
	Examiner	Art Unit
	KEVIN M BURD	2632

CPC - Searched*		
Symbol	**Date**	**Examiner**
H03L7/085;	10/24/2023	KMB
H03K19/1774	10/24/2023	KMB
H04B 1/40	10/24/2023	KMB
H03M 9/00	10/24/2023	KMB
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US Classification - Searched*			
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Search Notes		
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search search	10/24/2023	KMB
inventor name search	10/24/2023	KMB
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/723,130	Badizadegan, Nima
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by J Song · 2022 · Cited by 3 — Due to the clock asynchrony between the transmitter (Tx) side and the receiver ... The method of getting the signals with arbitrary sampling phase ...

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A high speed serializer/deserializer design

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Synchronic, optical transmission data link integrated with ...

by DSR Romaniuk — phase-locked loop (PLL) and four receiver PLLs per gigabit transceiver block ... • comclk – input side correlation clock signal. • clkout – output side correlation ...

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https://www.freepatentsonline.com › ...

Clock phase alignment - Xilinx, Inc.

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Field programmable gate array with external phase-locked ...

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by T Grob · 2010 · Cited by 1 — DDR uses rising and falling edges for sampling, so the clock speed can be halved compared to SDR. At the receiver side the signal of the data channels is.

Imperial College London
http://www.ee.ic.ac.uk › teaching › E2_experiment PDF

Cyclone V Device Handbook Volume 2: Transceivers

Jan 28, 2016 — the input of the byte deserializer is twice the FPGA fabric–receiver interface clock frequency. ... interface clock and the read side clock of the ...

Forum for Electronics
https://www.edaboard.com › threads › page-2

Trouble getting started with a Spartan-6 | Page 2

Feb 1, 2012 — I am currently clocking the FPGA with the original clock at X MHz. To do the deserialization do I need to use the output clocks of the ADC (part ...

More results

Bibliographic Data

Application No: 17/723,130

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /KEVIN M BURD/ Examiner's Signature | Initials

Title: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
04/18/2022	375	2632	00287-0016
RULE			

APPLICANTS

HFT Solutions, LLC, New Canaan, CT,

INVENTORS

Nima Badizadegan, Salem, NH, UNITED STATES

CONTINUING DATA

This application is a CON of 17236577 04/21/2021 PAT 11329655

17236577 is a CON of 16937309 07/23/2020 PAT 11018678

16937309 is a CON of 16888218 05/29/2020 PAT 10763865

16888218 is a CON of 16670702 10/31/2019 PAT 10771069

16670702 has PRO of 62808404 02/21/2019

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

04/20/2022

** SMALL ENTITY **

STATE OR COUNTRY

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ADDRESS

AMSTER, ROTHSTEIN & EBENSTEIN LLP
405 LEXINGTON AVENUE
FLOOR 48
NEW YORK, NY 10174
UNITED STATES

FILING FEE RECEIVED

$1,040

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L155	673	deserializ$6 WITH transmit$6 SAME clock SAME parallel	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/02/14 03:31 PM
L156	194	155 AND pll SAME serial	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/02/14 03:31 PM
L157	63	156 AND side near3 clock$4	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/02/14 03:32 PM
L158	63	157 AND pll	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/02/14 03:34 PM
L159	2	"10763865".pn.	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 01:12 PM
L160	10	"10763865".pn. "11018678".pn. "11329655".pn.	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 01:13 PM
L161	10	"10763865".pn. "11018678".pn. "11329655".pn.	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 01:13 PM
L162	2	"7668524".pn.	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 01:25 PM
L163	24279	deserializ$6 WITH serializ$5	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 02:13 PM
L164	215	163 SAME phase near5 detect$6	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 02:13 PM
L165	414	((receiv$4 OR recept$5) near4 clock$1) WITH (transmit$5 OR transmission$5) near2 clock$1 WITH phase near5 detect$6	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 02:51 PM
L166	414	((receiv$4 OR recept$5) near4 clock$1) WITH ((transmit$5 OR transmission$5) near2 clock$1) WITH phase near5 detect$6	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 02:51 PM
L167	64	((receiv$4 OR recept$5) near4 clock$1) WITH ((transmit$5 OR transmission$5) near2 clock$1) WITH phase near5 detect$6 AND (serializer$1 OR (serial	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 02:52 PM

		ADJ parallel) OR "s/p")					
L168	18	((receiv$4 OR recept$5) near4 clock$1) WITH ((transmit$5 OR transmission$5) near2 clock$1) WITH phase near5 detect$6 SAME (serializer$1 OR (serial ADJ parallel) OR "s/p")	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 02:52 PM
L169	1739	fpga SAME serdes	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 03:15 PM
L170	1249	169 AND @ad<"20190221"	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 03:15 PM
L171	978	169 AND @pd<"20180221"	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 03:16 PM
L172	978	169 AND @pd<"20180220"	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 03:16 PM
L173	1194	fpga WITH serdes	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 03:16 PM
L174	640	173 AND @pd<"20180220"	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 03:17 PM
L175	0	fpga AND "20140126613"	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 03:18 PM
L176	2	programmable AND "20140126613"	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 03:18 PM
L177	3	"11502694".pn.	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 04:01 PM
L178	9	((("BADIZADEGAN") near3 ("Nima"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 04:04 PM
L179	3	((("HFT") near3 ("SOLUTIONS") near3 ("LLC"))).AS,AANM.	(USPAT)	OR	ON	ON	2023/10/23 04:24 PM
L180	1	"10771069".pn.	(USPAT)	OR	ON	ON	2023/10/23 04:25 PM
L181	35596	(375/219.ccls.) (H03I7/085.cpc.) (g06f13/4291.cpc.) (H03M9/00.cpc.) (H04b1/40.cpc.) (H03k19/1774.cpc.)	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	OFF	OFF	2023/10/23 04:27 PM
L182	46	181 AND (((deserializ$5 OR (serial ADJ parallel)) SAME	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	OFF	OFF	2023/10/23 04:27 PM

		(serializ$5 OR (parallel ADJ serial))) SAME phase near3 detect$5)					
L183	4	"11093674".pn. "10160226502"	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 04:41 PM
L184	7	"11093674".pn. "20160226502"	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/23 04:42 PM
L185	5	("10564666" OR "7945803" OR "8996906" OR "9000801" OR "9954530").pn.	(US-PGPUB; USPAT)	OR	ON	ON	2023/10/23 04:44 PM
L186	13	("10037568" OR "10169814" OR "10411720" OR "20190025413" OR "4068188" OR "4745372" OR "6675306" OR "7080345" OR "7084709" OR "7333570" OR "8467418" OR "9001951" OR "9330740").pn.	(US-PGPUB; USPAT)	OR	ON	ON	2023/10/23 04:45 PM
L187	0	"8873606".pn. AND domain	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/24 10:58 AM
L188	1	"8873606".pn. AND K	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/24 11:35 AM
L189	2	"8873606".pn. AND N	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/24 11:38 AM
L190	2	"8873606".pn. AND phase	(US-PGPUB; USPAT; EPO; JPO; DERWENT)	OR	ON	ON	2023/10/24 11:41 AM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17723130
Filing Date	2022-04-18
First Named Inventor	Nima Badizadegan
Art Unit	2632
Examiner Name	BURD, Kevin Michael
Attorney Docket Number	00287-0016

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7945803	B2	2011-05-17	Anthony Mark Jones et al.	
	2	8996906	B1	2015-03-31	Kent R. Townley et al.	
	3	9000801	B1	2015-04-07	Christopher D. Ebeling et al.	
	4	9954530	B2	2018-04-24	Christopher D. Ebeling et al.	
	5	10564666	B2	2020-02-18	Ross MORGAN et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2426164	GB	A	2006-11-15	AGILENT TECHNOLOGIES, INC.		
	2	2572463	GB	B	2020-12-16	CIRRUS LOGIC INTERNATIONAL SEMICONDUCTOR LTD.		

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	U.S. Provisional Patent Application No. 62/649,783 filed March 29, 2018.	

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Attorney Docket Number	00287-0016

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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Signature	/Keith J. Barkaus/	Date (YYYY-MM-DD)	2022-10-03
Name/Print	Keith J. Barkaus	Registration Number	51,431

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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(Not for submission under 37 CFR 1.99)

Application Number	17723130
Filing Date	2022-04-18
First Named Inventor	Nima Badizadegan
Art Unit	2632
Examiner Name	BURD, Kevin Michael
Attorney Docket Number	00287-0016

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/K.M.B/	1	11093674	B2	2021-08-17	Sameh W. Asaad et al.	

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/K.M.B/	1	20160226502	A1	2016-08-04	Joseph D. Cali et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Examiner Name	BURD, Kevin Michael
	Attorney Docket Number	00287-0016

/K.M.B/	1	10G Ethernet PCS/PMA, v6.0; LogiCORE IP Product Guide; Vivado Design Suite, PG068 February 4, 2021 (XILINX)	☐
/K.M.B/	2	Images of trading system on an FPGA (Video feed click synch) 4/20/2018	☐
/K.M.B/	3	Intel UG-01125 - "SDI II Intel FPGA IP User Guide", Updated for Intel® Quartus® Prime Design Suite: 21.4, IP Version: 19.2.0 (Version: 2022.02.16)	☐
/K.M.B/	4	(Sidler et al.) "Scalable 10 Gbps TCP/IP Stack Architecture for Reconfigurable Hardware"; 2015 IEEE 23rd Annual International Symposium on Field-Programmable Custom Computing Machines; Downloaded on September 18, 2023	☐
/K.M.B/	5	Xilinx UG 576 - "UltraScale Architecture GTH Transceivers" User Guide (Xilinx) UG576 (v1.7.1) August 18, 2021	☐
/K.M.B/	6	Xilinx UG 885 - "VC707 Evaluation Board for the Virtex-7 FPGA" (Xilinx) User Guide, UG885 (v1.8) February 20, 2019	☐
/K.M.B/	7	Xilinx XAPP 591 (v1.0); Authors: Bob Feng, et al; "Implementing Triple-Rate SDI Pass-Through Using an All-Digital VCXO Replacement Technique in Virtex-6 FPGAs"; July 27, 2012	☐
/K.M.B/	8	Xilinx XAPP1276, David Taylor et al., "All Digital VCXO Replacement Using a Gigabit Transceiver Fractional PLL", (v1.2.1) January 28, 2022	☐

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Keith J. Barkaus/	Date (YYYY-MM-DD)	2023-10-04
Name/Print	Keith J. Barkaus	Registration Number	51,431

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	17723130
Filing Date	2022-04-18
First Named Inventor	Nima Badizadegan
Art Unit	2632
Examiner Name	
Attorney Docket Number	00287-0016

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	10037568	B2	2018-07-31	Taylor et al.	
	2	10169814	B2	2019-01-01	Parsons et al.	
	3	4068188	A	1978-01-10	Yokoyama	
	4	4745372	A	1988-05-17	Miwa	
	5	8467418	B2	2013-06-18	Aweya et al.	
	6	7333570	B2	2008-02-19	Aung et al.	
	7	7080345	B1	2006-07-18	Iotov	
	8	9330740	B1	2016-05-03	Baeckler et al.	

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	9	9001951	B1	2015-04-07	Kumpulainen	
	10	10411720	B2	2019-09-10	Lenzen et al.	
	11	6675306	B1	2004-01-06	Baxter	
	12	7084709	B1	2006-08-01	Leong, et al.	

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	1	20190025413	A1	2019-01-24	Liu et al.	

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	1	XILINX, "7 Series FPGAs GTX/GTH Transceivers - User Guide," Page 26, available at https://www.xilinx.com/support/documentation/user_guides/ug476_7Series_Transceivers.pdf (August 14, 2018).	
	2	SARAH HARRIS, "Timing & Synchronization," Harvey Mudd College Engineering Department, Page 24, available at https://cseweb.ucsd.edu/classes/wi06/cse291-b/slide/let4/timingint.pdf (January 31, 2006).	
	3	SAM PALERMO, "ECEN 720 High-Speed Links: Circuits and Systems - Lab 5," Texas A&M University, Page 5, available at: http://ece.tamu.edu/~spalermo/ecen689/ECEN720_lab5_2017.pdf (2017).	
	4	ALTERA, "Stratix V Device Handbook," Volume 2: Transceivers, Intel, Page 13, available at: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-v/stx5_xcvr.pdf (February 15, 2017).	
	5	STACKEXCHANGE, "Phase Frequency Detector in PLL," StackExchange, available at: https://electronics.stackexchange.com/questions/301402/phase-frequency-detector-in-pll (April 24, 2017).	
	6	IEEE STANDARDS ASSOCIATION, "IEEE Standards for Ethernet," IEEE 802.3-2018, Section 4, Clauses 49 and 51, Section 6, Clauses 82 and 83, available at: https://standards.ieee.org/standard/802_3-2018.html (August 31, 2018).	
	7	SLOBODAN MILIJEVIC, "The basics of synchronized Ethernet," EE Times-Asia, available at: https://www.microsemi.com/document-portal/doc_view/126475-the-basics-of-synchronized-ethernet-synce.	
	8	MACIEJ LIPINSKI, et al., "White Rabbit: a PTP Application for Robust Sub-nanosecond Synchronization," 2011 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control and Communication, Munich, Pages 25-30, available at: http://white-rabbit.web.cern.ch/documents/White_Rabbit-a_PTP_application_for_robust_sub-nanosecond_synchronization.pdf (2011).	
	9	FLOYD M. GARDNER, "Phaselock Techniques," Third Edition, Wiley-Interscience, Chapters 1, 4, 9, 10, 11, 13, and 17 (2005).	
	10	JENS TWIEFEL, et al., "Digital signal processing for an adaptive phase-locked loop controller," Proceedings of SPIE - The International Society for Optical Engineering, Volume 6926 (April 2008).	
	11	CHEN YAO, "Time to Digital Converter used in ALL digital PLL," Master of Science Thesis In System-on-Chip Design, Stockholm (August 2011).	

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	12	BEHZAD RAZAVI, "A CIRCUIT FOR ALL SEASONS: The StrongARM Latch," IEEE Solid-State Circuits Magazine (Spring 2015).
	13	PING LU, et al., "A 2-D GRO Vernier Time-to-Digital Converter with Large Input Range and Small Latency," Lund University - EIT Department, University of Toronto, IEEE Radio Frequency Integrated Circuits Symposium (2013).
	14	CHRISTIAN LEBER, et al. "High Frequency Trading Acceleration using FPGAs," University of Heidelberg, International Conference on Field Programmable Logic and Applications, Germany (2011).
	15	INTERNATIONAL TELECOMMUNICATION UNION, "Timing and synchronization aspects in packet networks," ITU-T, G.8261/Y.1361, International Telecommunication Union (May 2006).
	16	INTERNATIONAL TELECOMMUNICATION UNION, "Distribution of timing information through packet networks," ITU-T, G.8264/Y.1364, International Telecommunication Union (August 2017).
	17	IEEE STANDARDS ASSOCIATION, "IEEE Standards for Ethernet," IEEE 802.3-2018, Section 4, Figure 52-4, page 634 (2018)

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Examiner Signature	/KEVIN M BURD/	Date Considered	10/23/2023

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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Keith J. Barkaus/	Date (YYYY-MM-DD)	2022-06-02
Name/Print	Keith J. Barkaus	Registration Number	51,431

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/723,130	**10/04/2023 05:35:21 PM ET**	**00287-0016**

Title of Invention

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3228	FILED BY	Victoria Gilmore
PATENT CENTER #	62930706	FILING DATE	04/18/2022
CUSTOMER #	1912	FIRST NAMED INVENTOR	Nima Badizadegan
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Keith Barkaus

Documents

TOTAL DOCUMENTS: 9

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
1-IDS.pdf	4	Information Disclosure Statement (IDS) Form (SB08)	599 KB
NPL1-10GEthernetPCS.pdf	138	Non Patent Literature	1389 KB
NPL2-videofeedclocksynch.pdf	2	Non Patent Literature	281 KB
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NPL4-Scalable_10Gbps.pdf	8	Non Patent Literature	2066 KB
NPL5-ug576-ultrascale-gth-	518	Non Patent Literature	10187 KB

transceivers.pdf			
NPL6-ug885_VC707_Eval_Bd.pdf	96	Non Patent Literature	5650 KB
NPL7-XILINX-ImplementingTriple-RateSDIPass.pdf	12	Non Patent Literature	1524 KB
NPL8-xapp1276-vcxo.pdf	25	Non Patent Literature	9610 KB

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1-IDS.pdf	CFFBA0BC67BC77742E8F36A9D4DE7C6BE317E09D6AF1F4747F33AEA3C46E47400DFA092825BA53D5F483C1EE10666BE4D44BA7FFFF70EC5179F5631DBD8E951B
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NPL4-Scalable_10Gbps.pdf	DB8C4C5C6E77AAD2347B36A2B829F6E0F28FC24ED73197F42361F848BC07A5AE08A91650191A2FA54EE66E2B5C3C1348969B1038D6F89362E025894B944BC45C
NPL5-ug576-ultrascale-gth-transceivers.pdf	D89D30AA1ABB46786C2B422749E8C95E4CBAD50C5335E71FA8FC1FB9F6E27CE53B010F5BB064426DA925B768BE402C1F15876E8B5C5D1D721AF34587CF0DC45F

NPL6-ug885_VC707_Eval_Bd.pdf	17D1EEC7CEAD43B50DD2A227E5D5E861E0C8912FBE939985A6A39DD76B2F74BAAD1D94B3B9DA62606DF2F182B48BE8DC97F5E2826BA8404C75755E8B55877905
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	1	11093674	B2	2021-08-17	Sameh W. Asaad et al.	

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	1	20160226502	A1	2016-08-04	Joseph D. Cali et al.	

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	1	10G Ethernet PCS/PMA, v6.0; LogiCORE IP Product Guide; Vivado Design Suite, PG068 February 4, 2021 (XILINX)	☐
	2	Images of trading system on an FPGA (Video feed click synch)	☐
	3	Intel UG-01125 - "SDI II Intel FPGA IP User Guide", Updated for Intel® Quartus® Prime Design Suite: 21.4, IP Version: 19.2.0 (Version: 2022.02.16)	☐
	4	(Sidler et al.) "Scalable 10 Gbps TCP/IP Stack Architecture for Reconfigurable Hardware"; 2015 IEEE 23rd Annual International Symposium on Field-Programmable Custom Computing Machines; Downloaded on September 18, 2023	☐
	5	Xilinx UG 576 - "UltraScale Architecture GTH Transceivers" User Guide (Xilinx) UG576 (v1.7.1) August 18, 2021	☐
	6	Xilinx UG 885 - "VC707 Evaluation Board for the Virtex-7 FPGA" (Xilinx) User Guide, UG885 (v1.8) February 20, 2019	☐
	7	Xilinx XAPP 591 (v1.0); Authors: Bob Feng, et al; "Implementing Triple-Rate SDI Pass-Through Using an All-Digital VCXO Replacement Technique in Virtex-6 FPGAs"; July 27, 2012	☐
	8	Xilinx XAPP1276, David Taylor et al., "All Digital VCXO Replacement Using a Gigabit Transceiver Fractional PLL", (v1.2.1) January 28, 2022	☐

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Name/Print	Keith J. Barkaus	Registration Number	51,431

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(Not for submission under 37 CFR 1.99)

Application Number	17723130
Filing Date	2022-04-18
First Named Inventor	Nima Badizadegan
Art Unit	2632
Examiner Name	BURD, Kevin Michael
Attorney Docket Number	00287-0016

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	2	8996906	B1	2015-03-31	Kent R. Townley et al.	
	3	9000801	B1	2015-04-07	Christopher D. Ebeling et al.	
	4	9954530	B2	2018-04-24	Christopher D. Ebeling et al.	
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Examiner Name	BURD, Kevin Michael
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	1	2426164	GB	A	2006-11-15	AGILENT TECHNOLOGIES, INC.		
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	First Named Inventor	Nima Badizadegan
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	Examiner Name	BURD, Kevin Michael
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H04L 7/00 (2006.01)

(52) UK CL (Edition X):
H4P PPF

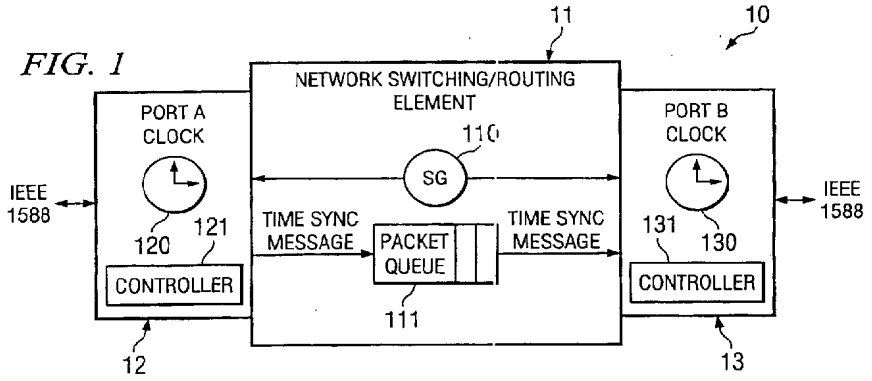
(56) Documents Cited:
GB 2418113 A GB 2300789 A
EP 1657619 A2 US 5812749 A
US 20040073718 A1

(58) Field of Search:
UK CL (Edition X) H4P
INT CL G06F, H04J, H04L
Other: EPODOC, WPI

(54) Abstract Title: **Network time synchronisation using a determination of network element transit times**

(57) By equipping receiving devices in a network with syncbronizable clocks it is possible to periodically send an "impulse" signal that is received by all of the clocks at the same (or relatively the same) instant of time. The accuracy of the impulse clock need not be high, only that its signal reach all the clocks approximately at the same time. In one embodiment, a transmitting device, upon receipt of the synchronizing impulse signal, sends a packet of data bearing the sending device's epoch time-stamp to a receiving device. The data packet makes its way through the network element to the receiving device and the time-stamp is used by the receiving device to calculate the difference between the epoch time of the receiver and the epoch time of the sender. Effectively, this procedure removes the unknown network element transit times from the equation and allows the devices to operate in a synchronized manner.

FIG. 1



GB 2 426 164 A

FIG. 1

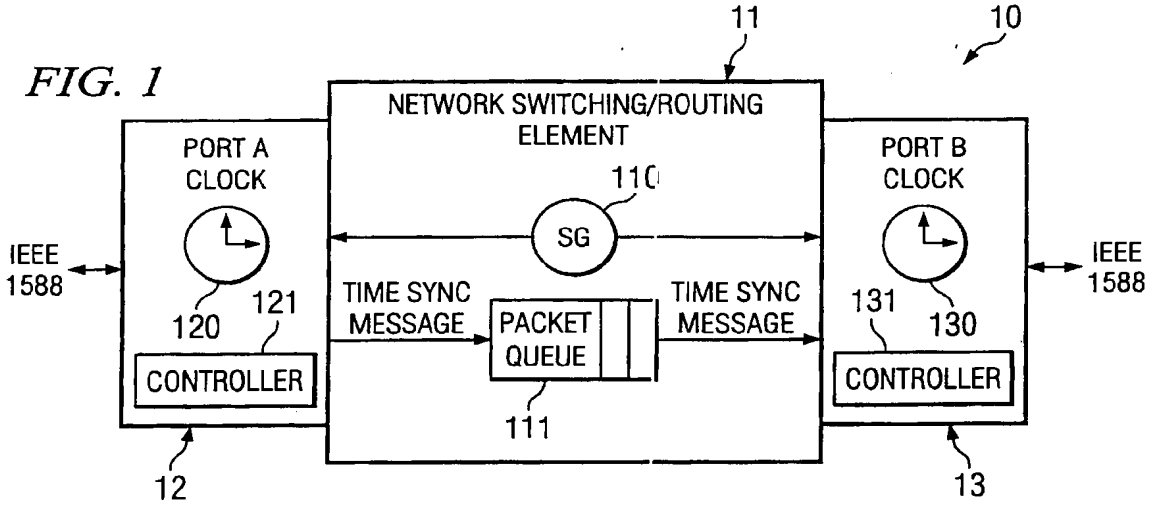


FIG. 2A

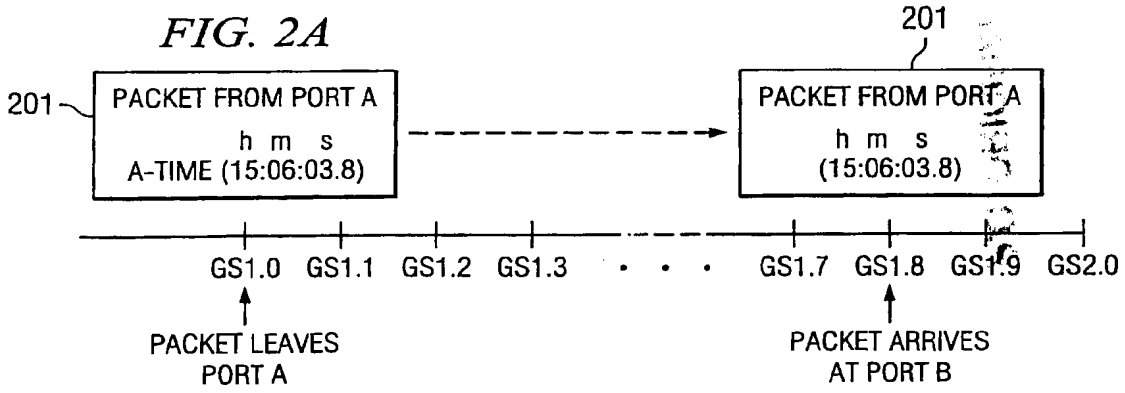


FIG. 2B

	h m s
ARRIVAL TIME (AS SEEN BY PORT B)	15:06:05.2
TRANSIT TIME (AS CALCULATED BY PORT B)	0.8
SENDING TIME (AS CALCULATED BY PORT B)	15:06:04.4
ACTUAL SENDING TIME (CONTAINED IN PACKET)	15:06:03.8
DIFFERENCE (AS CALCULATED BY PORT B)	+.6

FIG. 3A

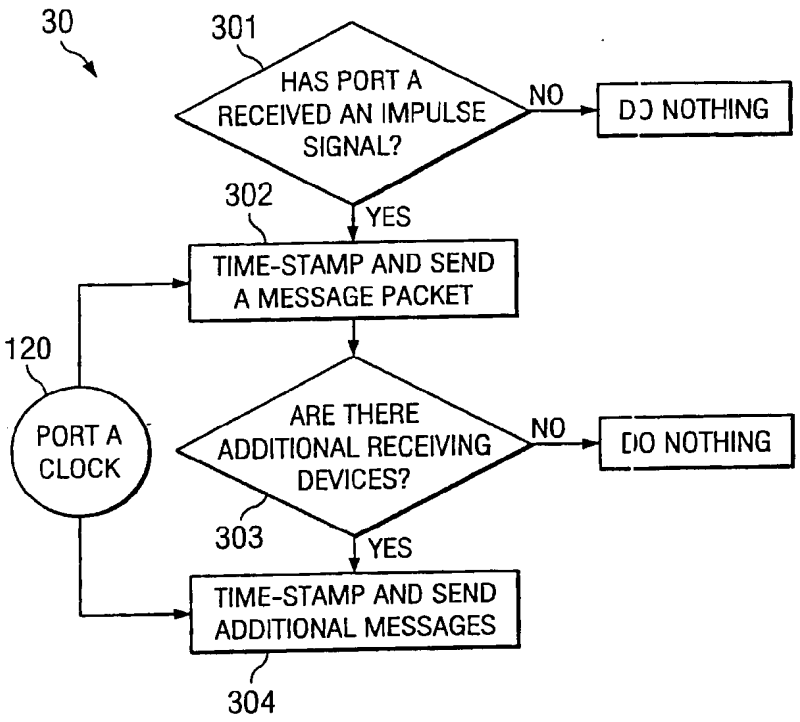
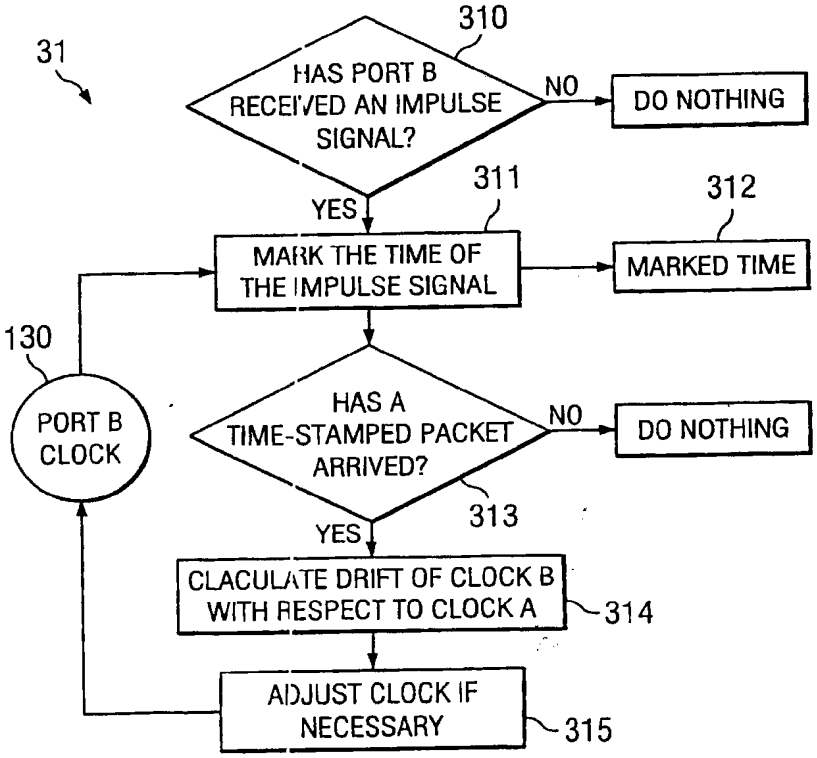

30
301
HAS PORT A RECEIVED AN IMPULSE SIGNAL?
NO
DO NOTHING
302
YES
TIME-STAMP AND SEND A MESSAGE PACKET
120
PORT A CLOCK
ARE THERE ADDITIONAL RECEIVING DEVICES?
NO
DO NOTHING
303
YES
TIME-STAMP AND SEND ADDITIONAL MESSAGES
304

FIG. 3B


31
310
HAS PORT B RECEIVED AN IMPULSE SIGNAL?
NO
DO NOTHING
YES
311
MARK THE TIME OF THE IMPULSE SIGNAL
312
MARKED TIME
130
PORT B CLOCK
HAS A TIME-STAMPED PACKET ARRIVED?
NO
DO NOTHING
313
YES
CLACULATE DRIFT OF CLOCK B WITH RESPECT TO CLOCK A
314
ADJUST CLOCK IF NECESSARY
315

SYSTEMS AND METHODS FOR SYNCHRONIZING TIME ACROSS NETWORKS

TECHNICAL FIELD

[0001] This invention relates to time synchronization and more particularly to systems and methods for synchronizing time across networks.

BACKGROUND OF THE INVENTION

[0002] Achieving time synchronization in computer networking environments is a challenging task. Different elements in a network, such as PCs/workstations/servers, routers/switches, and even VoIP phones, use NTP (Network Time Protocol), to get their epoch time for synchronization purposes. The accuracy of NTP time is in the order of tens of milliseconds. In many cases this is sufficient. In process automation, however, requirements are more rigid, and the requirement for time synchronization between networked devices is in the order of sub-microsecond accuracy.

[0003] This accuracy could be accomplished using the GPS system but the availability of the GPS signal is not assured at all locations due to the requirement of an antenna with a clear sight of the sky (to approximately 50 nsec.). In network performance measurement applications, where the one-way packet delay is measured, the accuracy has to be in the order of sub-milliseconds. Thus, deploying GPS at certain points of a network to perform network measurement is feasible except that, as discussed above, GPS signals are not available at all locations of the network.

[0004] In recent years the process automation industry has started deploying the IEEE 1588 standard to perform time synchronization between various devices. IEEE 1588 in its current form is limited to a very small network, typically a LAN segment. In order for IEEE 1588 to be deployed across wide area networks, significant investment in the network elements is required. For process automation there are a few companies that specialize in making switches that avoid delay in propagating the IEEE 1588 synchronization messages. However other manufactures, specifically router manufactures, find it economically difficult to deploy some of the solutions the IEEE 1588 standard proposes for dealing with queuing delays within the network elements.

[0005] There are two methods in IEEE 1588 to avoid delays at the network switching routing elements. One method is to use a boundary clock and another is to utilize high priority messages. Using the boundary clock, some of the messages carry timestamps i.e., the epoch time of the devices that are trying to synchronize their clocks. This protocol works well if the communication between such devices is symmetrical with respect to delay.

[0006] A problem arises when the path becomes asymmetrical, as when switching/routing network elements add unpredictable delays. Under such a system, the sending device (device A) is a master clock and will synchronize device B's (receiver device) clock. To avoid queuing at the switch/router, the IEEE 1588 messages have to be diverted at the MAC/PHY layer. The boundary clock first synchronizes with the device A clock as a slave, and then device A clock becomes the master clock to device B, which will then synchronize it's clock to the boundary clock. This solution requires modification of the MAC/PHY chip as well as requiring a single clock to manage all possible ports. This could be done with some effort on a switch/router with bus architecture. However, doing this on a switch/router with crossbar architecture is, at best, challenging. Therefore for the foreseeable future it is doubtful if such changes will be implemented in the switching network because of complexity and cost. However, in situations, such as process automation where the cost of the switches is much higher (and the consumer's economic return is higher) than it is for the Internet, there may be freedom to implement these schemes, but in data networks synchronizing clocks remains a problem.

BRIEF SUMMARY OF THE INVENTION

[0007] By equipping receiving devices in a network with synchronizable clocks it is possible to periodically send an "impulse" signal that is received by all of the clocks at the same (or relatively the same) instant of time. The accuracy of the impulse clock need not be high, only that its signal reach all the clocks approximately at the same time. In one embodiment, a transmitting device, upon receipt of the synchronizing impulse signal, sends a packet of data bearing the sending device's epoch time-stamp to a receiving device. The data packet makes its way through the network to the receiving device and the time-stamp is used by the receiving device to calculate the difference between the epoch time of the receiver and the epoch time of the sender. Effectively, this procedure removes the unknown network transit times from the equation and allows the devices to operate in a synchronized manner.

BRIEF DESCRIPTION OF THE DRAWING

[0008] FIGURE 1 shows one embodiment of the inventive concept having two device clocks that must be synchronized;

[0009] FIGURES 2A and 2B show an illustration of the calculations made for clock synchronization; and

[0010] FIGURES 3A and 3B show one embodiment of a process for establishing clock synchronization.

DETAILED DESCRIPTION OF THE INVENTION

[0011] FIGURE 1 shows one embodiment 10 of the inventive concept having two device clocks 120, 130 in devices 12 and 13, respectively, that are to be synchronized. It is assumed that clocks 120 and 130, as will be seen, are capable of receiving a sync signal, either via a wire, optically (either via air or in fiber), or wireless technologies of various frequencies/wave lengths and modulation schemes (such as, for example, 802.11, Bluetooth, TV RF), or via vibrations, such as impulses, etc. The sync (timing control) signal is not a signal that actually synchronizes the clocks directly as is done in GPS systems where the GPS sends an impulse every one second that is followed via a different channel (RS 232) with a value i.e., epoch time for alignment purposes, but rather the sync signal indicates that a specific event has occurred. Based on this specific event the clock to be synchronized will know how far it has wondered from the time of a system masters clock.

[0012] A Sync Generator (SG), such as SG 110, is used to provide the sync signal. SG 110 could be a part of switch/router element 11 or it could reside outside of the element. SG 110 signals an event periodically. The sync signal could be generated at each clock location based upon another event, such as a received signal and each clock then "counts" down from that signal and creates its own sync pulse.

[0013] Clocks 120 and 130 (and any other clocks to be synchronized) could either reside on a linecard of the router/switch or could be inside a Smart Gigabit Interface Converters (GBIC) or at any other location. The clocks outside the switch/router domain may synchronize with the rest of the world using IEEE 1588. Any switch/router port clock, for example, the master port clock could act as a SG. It should be noted that the SG could be one of the Smart

GBIC clocks if the clocks that are to be synchronized are inside Smart GBICs. The SG could be an infrared strobe device that the clocks could receive via infrared receivers, or the impulse could be sound or vibration. The frequency of the SG signals will depend upon the synchronization accuracy desired, but as will be discussed, the stability of the SG itself is not an issue. In the switch/router implementation, the SG could be a backplane clock with its signal propagated to the switch/router ports. The frequency of the SG signal could be approximately 1 second but could be more often, if desired.

[0014] One key aspect is that all of the clocks associated with a specific switch/router must receive the SG signal at approximately the same instant. In some cases it is possible to permanently adjust (tune) the delay of the impulse so that it will arrive at all devices at the same time. However, some delays in propagation in the range of a few nanoseconds could be tolerated.

[0015] If desired, the system could be used as a distributed 1588 boundary clock arrangement since such device would have a low latency/low jitter short-distance communication path that sends 1-bit on a periodic basis. All receivers would be able to timestamp these "sync events". An important aspect of such a distribution system is that the communication path for the 1-bit impulse signal is low jitter. In such a system a remote 1588 master is directly connected via wire or fiber to the smart GBIC which is a slave to the remote master. The remote GBIC synchronizes its clock to the remote master using normal 1588 messages. The remote GBIC sees the sync event (impulse) and timestamps it. Because this clock is synced to the master, this timestamp is essentially the same value that the master would record if the master was close enough to also see the sync event. All local clocks that also see the sync event would generate a local timestamp with the assumption that the sync event is essentially simultaneously received by all local clocks (within the sync accuracy of concern). The slave GBIC then communicates its timestamp to all local clocks that also saw the same sync event. This communication can be high jitter and is assumed to go through the network element. All local clocks receiving this message can then adjust their local clock to track the slave GBIC.

[0016] In operation, as shown in FIGURE 1, let's assume that the port A (12) clock 120 is the master and must synchronize the port B (13) clock 130. The process begins by port A sending a time sync message (TSM) i.e., a message with port A's epoch time-stamp imbedded therein to port B. The time-stamp is put on and the message is sent immediately upon port A

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receiving the SG signal from SG source 110. The TSM could be delayed by the switch/router, for example, in packet queue 111, without causing difficulty because all the slave clocks, as will be seen, will "know" when the packet is sent and will know the epoch time of the sending port, because such time is carried by the TSM.

[0017] The packet sent with port A's time-stamp, for example, under control of controller (12), will be captured at port B (13), as well as at all other ports in which clocks are to be synchronized. Since port B knows when the packet started out (because it started when port A received the same SG signal as did port B) and since the packet has the time-stamp of port A on it, port B, upon receipt of the packet, can determine how far ahead (or behind) port B's clock is from port A's clock when the packet arrives at port B.

[0018] FIGURE 2A illustrates this such that packet 201 is sent from port A at port A's epoch time of, say, 15:06:03.8. It takes eight measures (in this case tenths of a second) to arrive at port B. When the TSM arrives, port B marks its own epoch time of, say 15:06:05.2.

[0019] FIGURE 2B shows the calculations made at port B, for example, by controller 131, FIGURE 1, to determine how far port B's clock is from port A's clock. Thus, as shown, the actual time of arrival of packet 201 is 15:06:05.2 as seen by clock 130 (port B). The transit time is 0.8 which is counted by port B (for example, by controller 131) from the SG signal which come to port B at the same instant it came to port A, which is the time the TMS was sent from port A. The sending time (as calculated by port B) is 15:06:04.4. The actual sending time (as contained in packet 201) is 15:06:03.8. Thus, port B can calculated that clock 130 at port B is running 0.6 faster than is clock 120 at port A.

[0020] Note that while it is anticipated that one packet be sent exactly when the SG signal arrives, it could be on any "tick" thereafter provided that the receiving port knows which tick it is sent on (this could be in the time code within the packet message if desired or could be a system requirement) and provided the message arrives before the next SG signal arrives at port B. Also note that messages could go out to different ports on different "ticks" again provided the receiving port knows which "tick" is being used.

[0021] In a situation when there are multiple slave clocks (multiple ports) port A would most likely send an individual message to each slave clock, since broadcasting or multicasting may not be possible if ports are on separate subnets.

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[0022] In the Smart SGBIC implementation, all SGBICs could be daisy chained via an external wire. A dedicated Smart GBIC could provide the SG signal as well as the master clock signal to all Smart GBICs by sending Time Sync Message as UDP packets.

[0023] In the situation where the SG is within the router/switch device, and the SGBICs are deployed in it's ports, structure for sending the sync pulse to the slave SGBICs is required. This could be achieved by sending the signal down one of the existing tracks on a normal GBIC/SFP socket. For instance, the signal loss output from the GBIC to the host is an open collector signal that is pulled up on the host board. When the GBIC indicates a signal loss condition, it lets the voltage level be pulled up by the resistor, creating logic 1. If the received signal is fine, the GBIC or SFP pulls the signal down to a low voltage to represent logic 0. If the host were to modulate the level of the voltage on the pull-up resistor, a suitable equipped S-GBIC could detect this modulation. However an unmodified GBIC or SFP would not detect this variation and the normal signal loss functionality would not be interfered with.

[0024] If the SG signal were to be thought of as an impulse then this "impulse" could be externally created or could be derived from statistical measurements of packets that are sent from the master to the slave(s). By synchronizing all clocks to the same frequency and phase using statistical measurements then impulses could be derived (for example one second impulses) that every port notices at the same time.

[0025] FIGURE 3A shows one embodiment 30 of a process at a master port for beginning synchronization. Process 301 waits for an SG impulse to be received. When the SG impulse signal is received, process 302, in conjunction with port A clock 120, time-stamps and sends a message packet to port B. Processes 303 and 304 send packets to other devices if required. These signals could be an sequential SG pulses or could be "offset" by a number of "focus" within the same SG pulse.

[0026] FIGURE 3B shows one embodiment 31 of a process at slave port B for finishing the synchronization. Process 310 waits for port B to receive an impulse signal. When such a signal has been received, process 311 marks the time, of the impulse signal as maintained by clock 130. This "time" is the epoch time of port B as now captured by process 312.

[0027] Process 313 determines when a time-stamped message has been received from the master-port and records the time of the arrival using its own epoch time. Then, as

shown in FIGURE 2B, process 314 calculates the drift of clock B with respect to clock A. Process 305 makes any adjustment necessary to clock B to correct for the draft.

[0028] The accuracy of the synchronization depends upon the interval between the impulse signals and the receipt of a message with the time-stamp from port A. The slave clocks will each drift compared to the master with the rate of drift being controlled by its own nature. Since each slave clock adjusts its own drift after learning how much it has drifted. It is possible to make each clock adjustment individual to the port such that the adjustment might be made all at one time or over a period of time. The adjustment could be made using the rate of drift, as measured between SG impulses, to determine how much should be corrected at any one time. This eliminates the need for a big adjustment on any cycle.

[0029] Although the present invention and advantages thereof have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

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CLAIMS

What is claimed is:

1. A network synchronization system comprising:

network sending and receiving devices each adapted to receive a timing control signal at substantially the same time;

a controller at a sending device, said controller operable for placing a time-stamp on a message to be sent from said sending device to a receiving device through a network at a known fixed time in relation to receipt of said timing control signal, said time-stamp being the epoch time of said sending device; and

a controller at said receiving device operable for determining from a received one of said messages the difference between the epoch time of said receiving device and the epoch time of said sending device based upon said time-stamped epoch time and the transit time calculated from said known fixed time from receipt of said timing control signal at said receiving device.

2. The system of claim 1 wherein said known fixed time is immediately upon receipt of said time control signal by said sending device.

3. The system of claim 1 wherein said known fixed time is an offset from said receipt of said time control signal.

4. The system of claim 1 wherein said sending device sends a message to a plurality of receiving devices, each said message bearing a time-stamp of the epoch time of said sending device; and wherein each said message is sent at a different known offset from said receipt of said time control signal.

5. The system of claim 1 further comprising:

a clock at said receiving device; and

wherein said controller provides a drift calculation for adjusting the drift of said receiving device clock, said drift calculation based upon said determined epoch time difference.

6. The system of claim 1 wherein said timing control signal is transmitted to said clocks by a mechanism selected from the list consisting of:

wireless RF, cabled wiring, sound, vibration, and light.

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7. The system of claim 1 wherein said timing control signal is generated by a mechanism selected from the list comprising:

electronic counter, local oscillator, phase locked loop, frequency generator, and GPS receiver.

8. The system of claim 1 wherein said timing control signal is periodic.

9. The system of claim 8 wherein said period is one second.

10. A method for synchronizing clocks in spaced apart network elements, said method comprising:

sending an impulse to a plurality of said clocks, said impulse arriving at said clocks substantially at the same time;

upon receipt of said impulse at one of said clocks sending a message through a network device to at least one target clock, said message having the epoch time of said sending clock; and

calculating at said target clock, upon receipt of said message at a target clock using the epoch time of said sending clock, as contained in said time-stamp, the difference between the epoch time of said target clock and the epoch time of said sending clock.

11. The method of claim 10 wherein said calculating comprises:

comparing the epoch time of said target clock to the epoch time of said sending clock; and

adjusting for network transit time of said message bearing said time-stamp.

12. The method of claim 11 wherein said adjusting comprises:

counting the time elapsed from receipt of said impulse until the time said message arrives at said target clock.

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13. The method of claim 12 further comprising:

upon receipt of said impulse at said sending clock for also sending messages through said network device to a plurality of additional target clocks, each aid message having the epoch time of said sending clock; and

calculating at each of said additional target clocks, upon receipt of said message at said target clocks using the epoch time of said sending clock, as contained in said time-stamp, the difference between the epoch time of each said additional target clock and the epoch time of said sending clock.

14. The method of claim 12 wherein said timing control signal is transmitted to said clocks by a mechanism selected from the list consisting of:

wireless RF, cabled wiring, sound, vibration, and light.

15. The method of claim 12 wherein said timing control signal is generated by a mechanism selected from the list comprising:

electronic counter, local oscillator, phase locked loop, frequency generator, and GPS receiver.

16. The method of claim 11 wherein said timing control signal is periodic.

17. The method of claim 16 wherein said period is one second.

18. A port circuit for use in a network, said circuit comprising:

a controller for determining from a received time-stamped messages from a sending port the difference between the epoch time of said port and the epoch time of said sending port based upon said time-stamped epoch time and the transit time calculated from a known fixed time from receipt of a timing control signal received concurrently at both said port and said sending port.

19. The port circuit of claim 18 further comprising:

a clock having an drift; and wherein said controller further comprises;

means for adjusting said clock drift based upon said determined time difference.

20. The port circuit of claim 18 further comprising:

a clock; and wherein said controller further comprises:

means for synchronizing said clock with a clock in said sending port.

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21. A system for synchronizing clocks in separate ports of network elements, said system comprising:

means for sending an impulse to a plurality of said clocks, said impulse arriving at said clocks substantially at the same time;

means, operative upon receipt of said impulse at one of said clocks, for sending a message through a network to at least one target clock, said message having the epoch time of said sending clock; and

means for calculating at said target clock, upon receipt of said message at a target clock using the epoch time of said sending clock, as contained in said time-stamp, the difference between the epoch time of said target clock and the epoch time of said sending clock.

22. The system of claim 21 wherein said calculating means comprises:

means for comparing the epoch time of said target clock to the epoch time of said sending clock; and

means for adjusting for network transit time of said message bearing said time-stamp.

23. The system of claim 22 wherein said adjusting means comprises:

counting the time elapsed from receipt of said impulse until the time said message arrives at said target clock.

24. The system of claim 21 wherein said impulse generating means comprises, means for generating a signal from the list consisting of:

electronic counter, local oscillator, phase locked loop, frequency generator, and GPS receiver.

25. The system of claim 21 wherein said impulse is periodic.

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26. A distributed boundary clock network comprising:

a master clock;

a plurality of other clocks;

a low-jitter communication path extending among said master clock and said other clocks;

means using 1558 messaging for synchronizing said master clock to one of said other clocks, said one other clock becoming a remote master clock; and

using said low-jitter communication path for distributing a sync signal to all said other clocks, including said remote master clock;

means at said remote master clock for sending a time-stamped message to said other clocks upon receipt of said sync signal; and

means at each said other clocks using said time-stamped message from said remote master clock and the time of said sync signal is received at said other clock for calculating the difference between said other clock and said remote master clock.

27. The distributed boundary clock network of claim 26 wherein said network comprises:

at least one Gigabit Interface Converter.

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The Patent Office

For Innovation

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Application No: GB0607387.8 **Examiner:** Joseph Wellings

Claims searched: 1-25 **Date of search:** 19 July 2006

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
A	-	GB 2300789 A (GEN DATACOMM)
A	-	EP 1657619 A2 (BOSCH)
A	-	US 2004/0073718 A1 (JOHANNESSEN)
A	-	US 5812749 A (FERNANDEZ)
A	-	GB 2418113 A (AGILENT)

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC^{X} :

H4P

Worldwide search of patent documents classified in the following areas of the IPC

G06F; H04J; H04L

The following online and other databases have been used in the preparation of this search report

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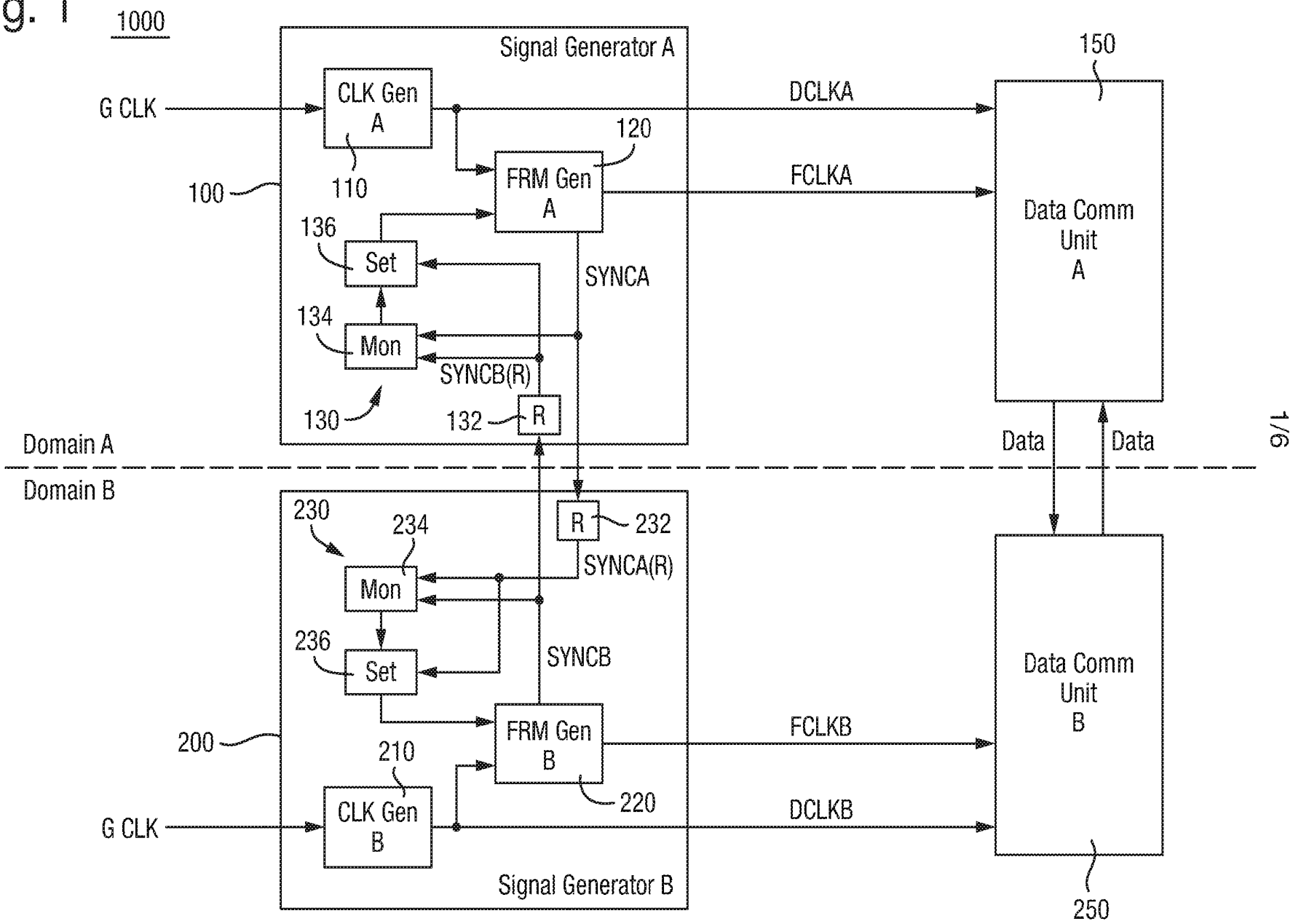
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Fig. 1



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Fig. 2

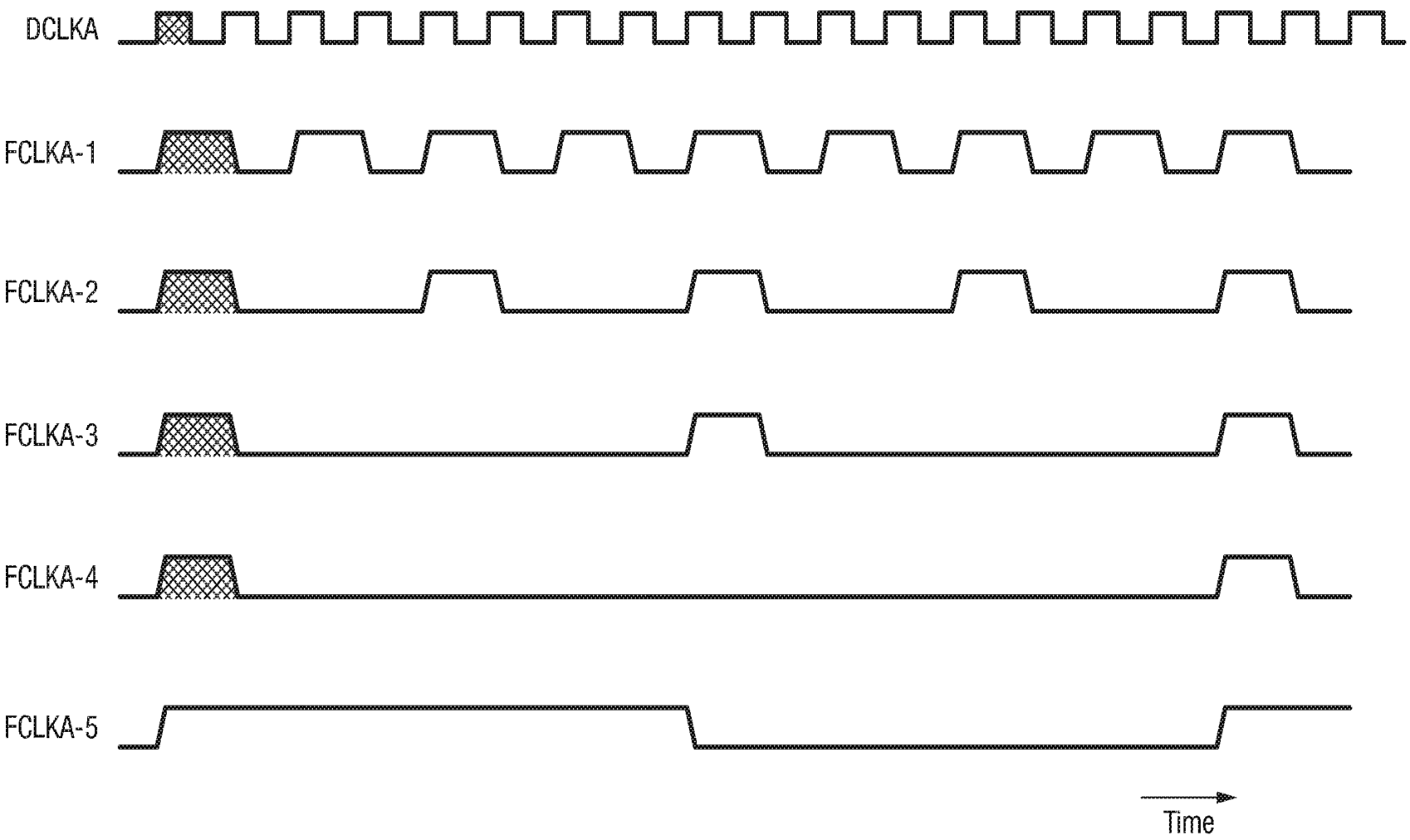
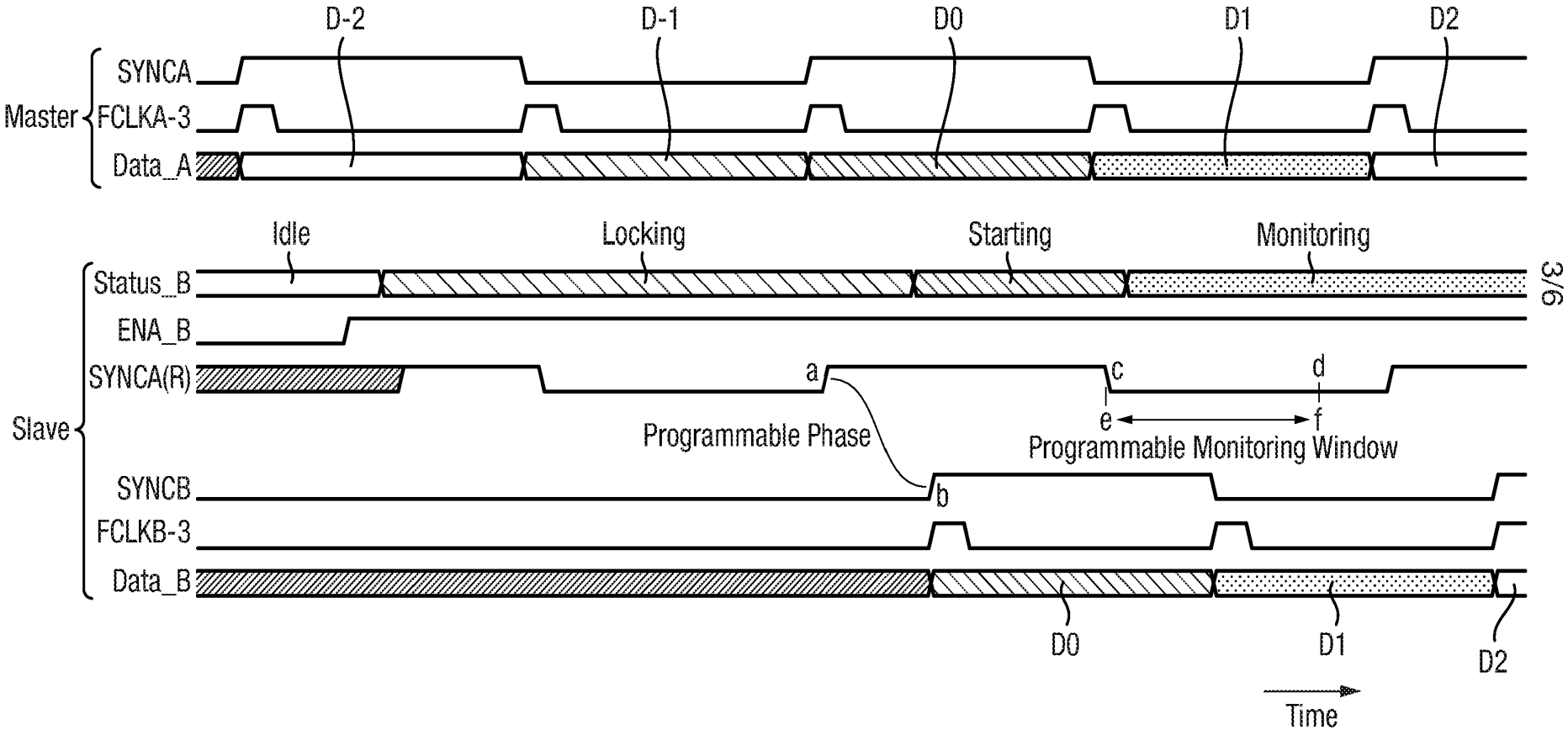
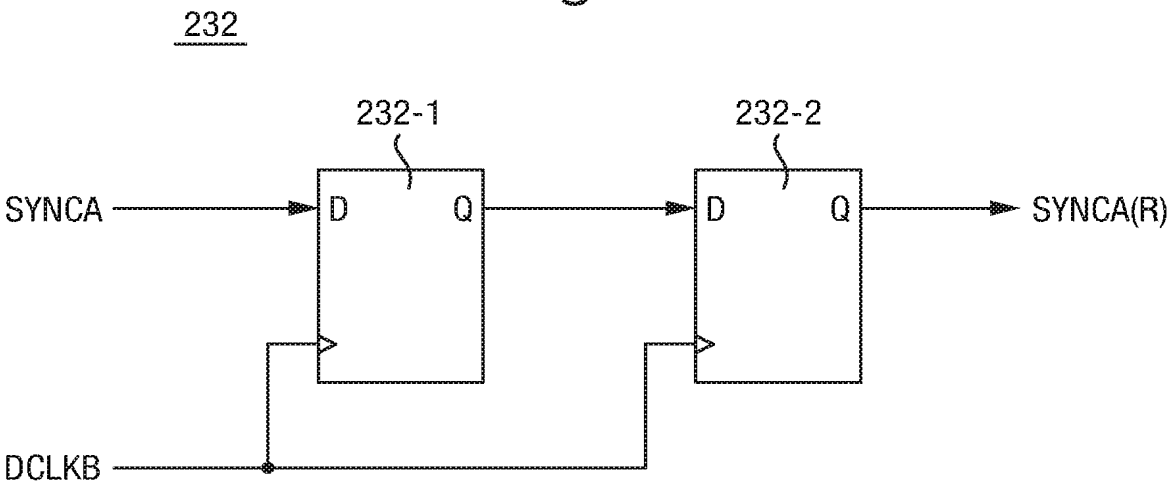


Fig. 3



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Fig. 4



25 10 18

Fig. 7

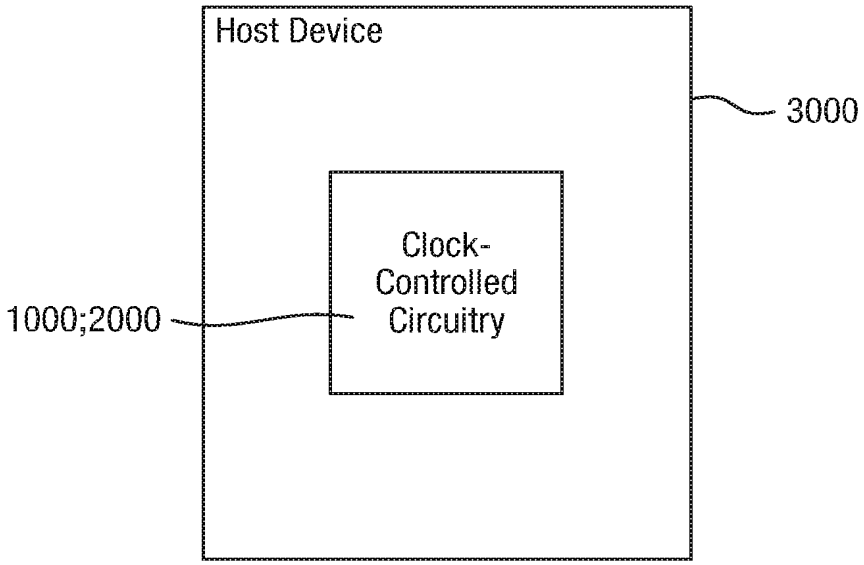
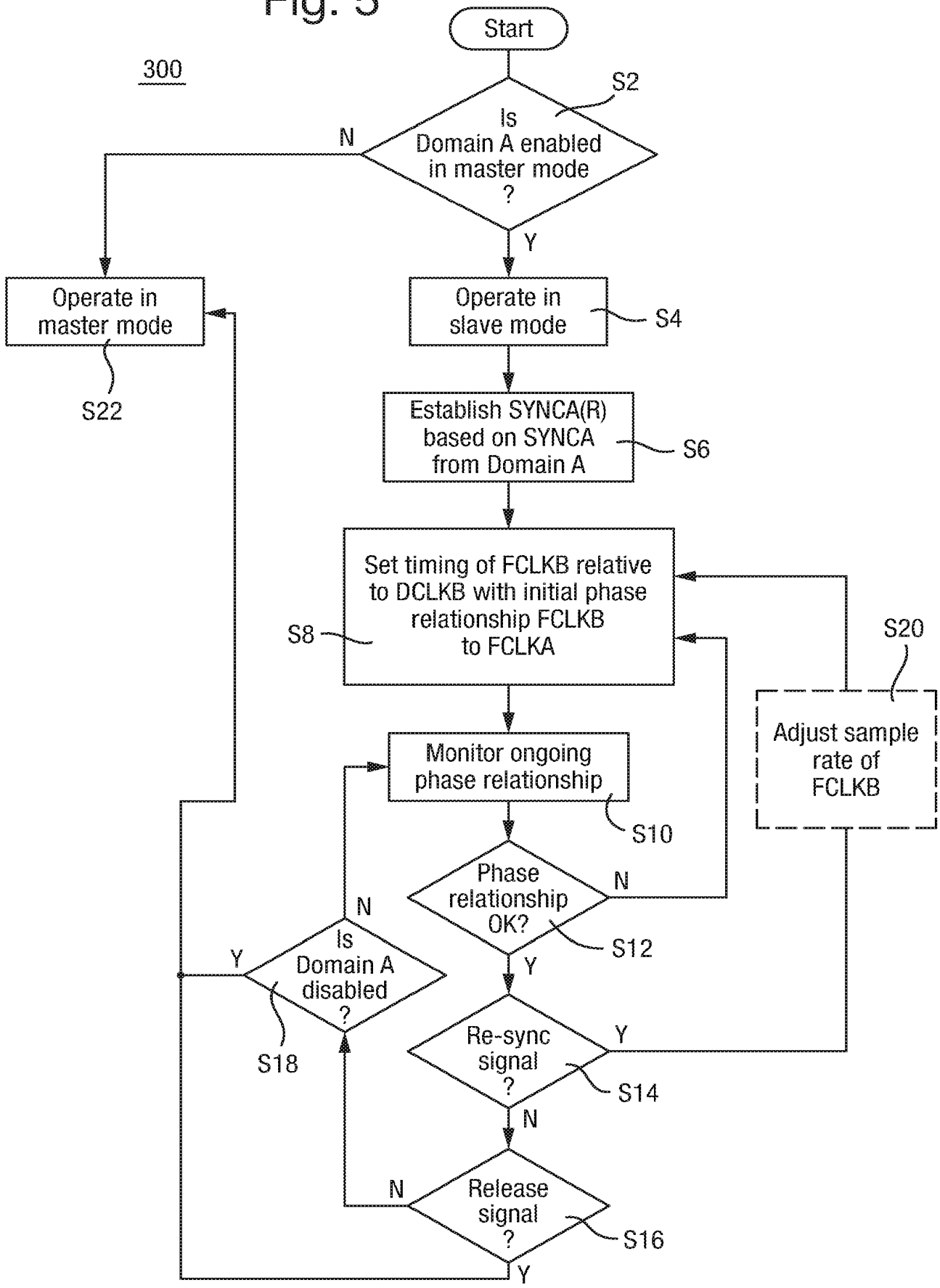
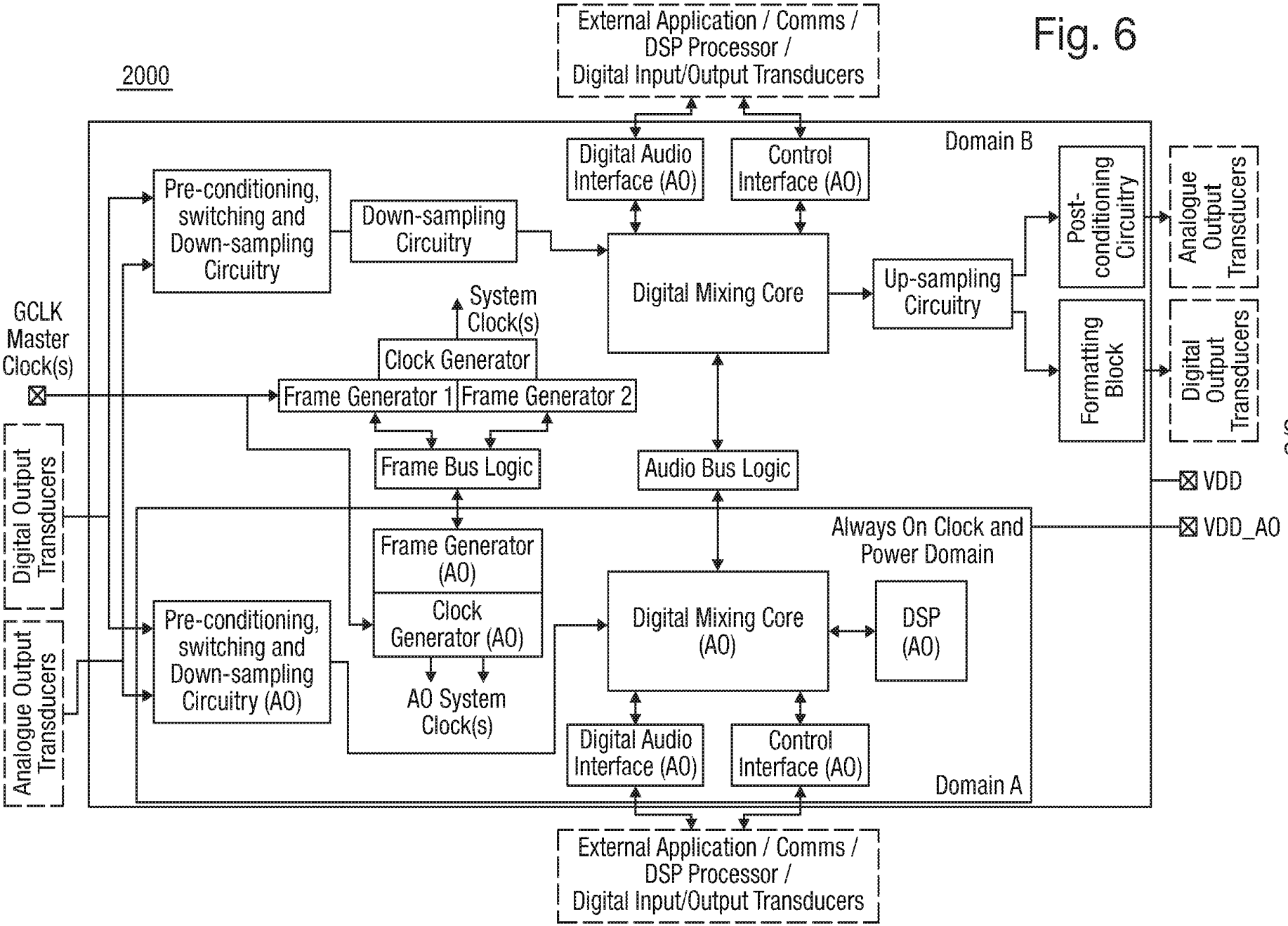


Fig. 5


Start
300
S2
Is Domain A enabled in master mode ?
N
Y
Operate in master mode
S22
Operate in slave mode
S4
Establish SYNCA(R) based on SYNCA from Domain A
S6
Set timing of FCLKB relative to DCLKB with initial phase relationship FCLKB to FCLKA
S8
S20
Adjust sample rate of FCLKB
Monitor ongoing phase relationship
S10
Phase relationship OK?
S12
N
Y
Is Domain A disabled ?
S18
Re-sync signal ?
S14
Release signal ?
S16

25 10 18

Fig. 6


2000
External Application / Comms / DSP Processor / Digital Input/Output Transducers
Domain B
Digital Audio Interface (A0)
Control Interface (A0)
Pre-conditioning, switching and Down-sampling Circuitry
Down-sampling Circuitry
Digital Mixing Core
Up-sampling Circuitry
Post-conditioning Circuitry
Analogue Output Transducers
Formatting Block
Digital Output Transducers
System Clock(s)
Clock Generator
GCLK Master Clock(s)
Frame Generator 1
Frame Generator 2
Frame Bus Logic
Audio Bus Logic
VDD
VDD_AO
Always On Clock and Power Domain
Digital Output Transducers
Frame Generator (A0)
Clock Generator (A0)
Pre-conditioning, switching and Down-sampling Circuitry (A0)
Digital Mixing Core (A0)
DSP (A0)
Analogue Output Transducers
A0 System Clock(s)
Digital Audio Interface (A0)
Control Interface (A0)
Domain A
External Application / Comms / DSP Processor / Digital Input/Output Transducers

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CLOCK-CONTROLLED CIRCUITRY

Technical Field

The present disclosure relates to clock-controlled circuitry, and in particular to the timing of signals between clock domains of such circuitry. Such timing may affect the transfer of data from one such domain to the other.

Background

Clock-controlled circuitry may be organised into a plurality of clock domains, where different clock domains operate based on their own clock signals. The clock signals of such different clock domains may be related in some way – for example, they may be derived ultimately from the same global or master clock signal. However, typically different clock domains have clock signals which have different frequencies and/or phases from one another, or phases and/or frequencies which are only nominally (e.g. to differing accuracies) the same. As such, a relationship between the clock signals of different clock domains may vary over time and may be unpredictable or unreliable. Such an architecture may be described in overview as a Global Asynchronous Locally Synchronous (GALS) architecture. One advantage of a GALS architecture may be that the overall amount of clock-tree balancing required may be reduced as compared to an architecture with only a single clock domain. Also, in a GALS architecture it may be possible to control which domains are on and which are off over time, with the domains then acting as power and clock domains.

Where data is transferred from one clock domain to another, timing between those domains can be important. Where the data is for example audio data, which may be packaged in frames and which may need to be handled in a time-critical manner (such as on a real-time basis), it may be desirable to minimize or reduce group delay or avoid audio artefacts related to clock domain crossing to improve end-user experience.

Clock-controlled circuitry naturally finds wide use. For example, most integrated circuits (ICs) use one or more clock signals to synchronise or otherwise control

different parts of system circuitry. Circuits operating based on clock signals may be considered synchronous circuits. Examples include processing circuits such as audio-processing circuits (which may handle data such as audio data).

Clock-controlled circuitry may therefore be implemented on ICs or systems within a host device, which may be considered an electrical or electronic device. Examples include a portable and/or battery powered host device such as a mobile telephone, an audio player, a video player, a PDA, a mobile computing platform such as a laptop computer or tablet and/or a games device.

Of course, audio data is merely one example type of data where timing issues can be important in relation to clock domain crossing. Other examples may include video or sensor/transducer (e.g. haptics) data. For convenience, however, the example of audio data will be carried forward herein.

Existing clock-controlled circuitry has been found to have shortcomings, in particular when data is passed or streamed from one clock domain to another. It is desirable to provide improved clock-controlled circuitry, in which data (such as audio data) may be transferred from one clock domain to another in an efficient manner.

Summary

According to a first aspect there is provided clock-controlled circuitry organised into at least first and second clock domains, the first clock domain configured to operate based on a first clock signal and the second clock domain configured to operate based on a second clock signal, wherein: the first clock domain comprises a first signal generator operable to generate a first repetitive signal synchronised to the first clock signal; the second clock domain comprises a second signal generator operable to generate a second repetitive signal synchronised to the second clock signal; the first signal generator is operable, when operating in master mode, to output to the second signal generator a first synchronisation signal indicative of a phase of the first repetitive signal; and the second signal generator is operable, when operating in slave mode, to: set a timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is set to have a

phase relationship with the first repetitive signal which then meets a slave specification; and re-set the timing of the second repetitive signal relative to the second clock signal if it is determined that the phase relationship has changed such that it no longer meets the slave specification.

In this way, it is possible to keep the phase relationship within bounds defined by the slave specification, which can be advantageous where interrelated processes are defined by the first and second repetitive signals. For example, it may be that data transfer between the first and second clock domains is governed by the first and second repetitive signals, and in particular the relationship between them. By keeping the phase relationship within bounds defined by the slave specification, it may be that such data transfer can occur without significant errors and with reduced or minimised latency.

The slave specification may be or comprise one or more parameter values, which may define an allowable range of phase differences between the first and second repetitive signals. The slave specification may also define such a phase difference to be achieved when the timing of the second repetitive signal relative to the second clock signal is set.

The second signal generator may be operable to re-set the timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is again set to have a phase relationship with the first repetitive signal which then meets the slave specification.

The second signal generator, or another signal generator of the clock-controlled circuitry, may be operable to monitor the phase relationship between the second repetitive signal and the first repetitive signal after the timing of the second repetitive signal relative to the second clock signal has been set and to determine if that phase relationship has changed such that it no longer meets the slave specification.

By (actively) monitoring the phase relationship, it is possible to detect when the phase relationship no longer meets the slave specification. The other signal generator may for

example be the first signal generator or a central signal generator (such as a control unit) other than the first and second signal generators.

The second signal generator or the other signal generator may be operable to monitor the phase relationship between the second repetitive signal and the first repetitive signal by monitoring a phase relationship between the second repetitive signal and the first synchronisation signal.

The second signal generator or the other signal generator may be operable to monitor the phase relationship between the second repetitive signal and the first repetitive signal by monitoring a phase relationship between the second repetitive signal and a retimed first synchronisation signal being a retimed version of the first synchronisation signal.

The second signal generator or the other signal generator may be operable to monitor the phase relationship between the second repetitive signal and the first repetitive signal by obtaining a count value indicative of the phase relationship by: incrementing a counter between corresponding edges of the second repetitive signal and the first synchronisation signal or retimed first synchronisation signal; or incrementing a counter while the second repetitive signal and the first synchronisation signal or retimed first synchronisation signal have the same value as one another; or incrementing a counter while the second repetitive signal and the first synchronisation signal or retimed first synchronisation signal have different values from one another.

The first synchronisation signal may be part or all of the first repetitive signal, or may be derived from the first repetitive signal. For example, the first repetitive signal may comprise a plurality of component repetitive signals, and the first synchronisation signal may be one of those repetitive signals.

The second signal generator may be operable when operating in slave mode, to receive a release signal, and, if the release signal is received, to transition its operation to free-running mode. The second signal generator may be operable in connection with the transition to free-running mode, to continue generation of the second repetitive signal at its existing timing relative to the second clock signal without taking account of

(i.e. without monitoring) the phase relationship between the second repetitive signal and the first repetitive signal.

The second signal generator may be operable, when operating in slave mode, to receive a re-synch signal indicating a change in the first repetitive signal, and, if the re-synch signal is received, to re-set the timing of the second repetitive signal relative to the second clock signal.

The re-synch signal may indicate a change in a repeating pattern of the first repetitive signal. In such a case, the second signal generator may be operable, if the re-synch signal is received, to re-set the timing of the second repetitive signal relative to the second clock signal based on the re-synch signal and re-configure the second repetitive signal based on the change in the repeating pattern indicated by the re-synch signal.

The second signal generator may be operable, when operating in slave mode, to monitor operation of the first signal generator, and, if the first signal generator is determined to become disabled (e.g. powered down or disconnected), to: transition its operation to master mode; and then continue generation of the second repetitive signal at its existing timing relative to the second clock signal without taking account of the phase relationship between the second repetitive signal and the first repetitive signal. The second signal generator may output a second synchronisation signal indicative of a phase of the second repetitive signal.

The first signal generator may be operable, when re-enabled after being disabled, to: monitor operation of the second signal generator and determine if the second clock control circuit is operating in master mode; and when it is determined that the second clock control circuit is operating in master mode, operate in slave mode.

The first signal generator may be operable, when operating in slave mode, to: set a timing of the first repetitive signal relative to the first clock signal based on the second synchronisation signal so that the first repetitive signal is set to have a phase relationship with the second repetitive signal which then meets the slave specification; and re-set the timing of the first repetitive signal relative to the first clock signal if it is

determined that that phase relationship has changed such that it no longer meets the slave specification.

The first signal generator may be operable to re-set the timing of the first repetitive signal relative to the first clock signal based on the second synchronisation signal so that the first repetitive signal is again set to have a phase relationship with the second repetitive signal which then meets the slave specification.

The first signal generator, or another signal generator of the clock-controlled circuitry, may be operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal after the timing of the first repetitive signal relative to the first clock signal has been set and to determine if that phase relationship has changed such that it no longer meets the slave specification.

The first signal generator or that other signal generator may be operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal by monitoring a phase relationship between the first repetitive signal and the second synchronisation signal.

The first signal generator or that other signal generator may be operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal by monitoring a phase relationship between the first repetitive signal and a retimed second synchronisation signal being a retimed version of the second synchronisation signal.

The first signal generator or that other signal generator may be operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal by obtaining a count value indicative of the phase relationship by: incrementing a counter between corresponding edges of the first repetitive signal and the second synchronisation signal or retimed second synchronisation signal; or incrementing a counter while the first repetitive signal and the second synchronisation signal or retimed second synchronisation signal have the same value as one another; or incrementing a counter while the first repetitive signal and the second synchronisation signal or retimed second synchronisation signal have different values from one another.

The second synchronisation signal may be part or all of the second repetitive signal, or may be derived from the second repetitive signal.

The first signal generator and second signal generator may be operable to generate the first and second clock signals, respectively, based on the same global clock signal. The first and second signal generators may be operable to generate the first and second clock signals with differing degrees of accuracy.

The first repetitive signal may comprise a plurality of different component repetitive signals synchronised with the first clock signal, and/or the second repetitive signal may comprise a plurality of different component repetitive signals synchronised with the second clock signal.

The clock-controlled circuitry may be organised into at least first and second power domains, wherein the first power domain comprises the first clock domain and the second power domain comprises the second clock domain. Such different power domains may be powered on or off (powered up or down, or in normal or low-power mode) independently of one another or at different times from one another.

The first and second power domains may be provided on different IC chips, or they could be provided on the same IC chip. The clock-controlled circuitry may comprise first and second IC chips. The first IC chip may comprise the first power domain and the second IC chip may comprise the second power domain.

The clock-controlled circuitry may comprise a first data communication unit in the first clock domain and configured to operate based on the first clock signal, and a second data communication unit in the second clock domain and configured to operate based on the second clock signal. The first data communication unit may be operable to process a first data signal which is synchronous with the first clock signal, based on the first repetitive signal. The second data communication unit may be configured to process a second data signal which is synchronous with the second clock signal, based on the second repetitive signal. The first and second communication units may be configured to transfer such a data signal between them based on their respective

first and second repetitive signals and via a retiming circuit so that the first data signal becomes the second data signal or *vice versa*.

The data signals may be audio data signals. The clock-controlled circuitry may be clock-controlled audio circuitry. The audio data signals may be organised into frames. The first and second data communication units may be configured to align the frames in their respective audio data signals with their respective repetitive signals.

The clock-controlled circuitry may comprise storage for storing information defining the slave specification. The first signal generator and/or the second signal generator may be configured to set the timing concerned based on the information. The determination that a said phase relationship has changed such that it no longer meets the slave specification may be made based on the information.

The information may comprise parameter values. The first signal generator and/or the second signal generator may be configured to set the timing concerned based on one or more of the parameter values. The determination that a said phase relationship has changed such that it no longer meets the slave specification may be made based on one or more of the parameter values.

The clock-controlled circuitry may comprise a controller operable to store the information in the storage so as to define the slave specification currently in use, optionally based on a user input.

According to a second aspect there is provided a method of controlling clock-controlled circuitry which is organised into at least first and second clock domains, the first clock domain configured to operate based on a first clock signal and the second clock domain configured to operate based on a second clock signal, wherein: the first clock domain comprises a first signal generator operable to generate a first repetitive signal synchronised to the first clock signal; the second clock domain comprises a second signal generator operable to generate a second repetitive signal synchronised to the second clock signal; and the first signal generator is operable, when operating in master mode, to output to the second signal generator a first synchronisation signal indicative of a phase of the first repetitive signal, the method comprising controlling the

second signal generator, when operating in slave mode, to: set a timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is set to have a phase relationship with the first repetitive signal which then meets a slave specification; and re-set the timing of the second repetitive signal relative to the second clock signal if it is determined that the phase relationship has changed such that it no longer meets the slave specification.

According to a third aspect there is provided a computer program which, when executed on a processor of clock-controlled circuitry, causes the clock-controlled circuitry to carry out a control method, wherein: the clock-controlled circuitry is organised into at least first and second clock domains; the first clock domain is configured to operate based on a first clock signal and the second clock domain is configured to operate based on a second clock signal; the first clock domain comprises a first signal generator operable to generate a first repetitive signal synchronised to the first clock signal; the second clock domain comprises a second signal generator operable to generate a second repetitive signal synchronised to the second clock signal; and the first signal generator is operable, when operating in master mode, to output to the second signal generator a first synchronisation signal indicative of a phase of the first repetitive signal, the method comprising controlling the second signal generator, when operating in slave mode, to: set a timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is set to have a phase relationship with the first repetitive signal which then meets a slave specification; and re-set the timing of the second repetitive signal relative to the second clock signal if it is determined that the phase relationship has changed such that it no longer meets the slave specification.

According to a fourth aspect there is provided a computer-readable medium having the computer program of the aforementioned third aspect stored thereon.

As apparent from the above, method aspects corresponding to the apparatus (circuitry) aspects are envisaged. Features of the apparatus aspects may thus have corresponding features in the method aspects. Computer program and storage medium aspects are also envisaged as apparent from the above, and similar comments apply. The present disclosure will be understood accordingly.

Brief Description of Drawings

Reference will now be made, by way of example, to the accompanying drawings, of which:

Figure 1 is a schematic diagram of clock-controlled circuitry embodying the present invention;

Figure 2 is a schematic diagram indicating example frame clock signals;

Figure 3 is a signal diagram useful for understanding operation of the Figure 1 circuitry;

Figure 4 is a schematic diagram of an example implementation of a retiming unit of Figure 1;

Figure 5 is a schematic diagram of a method which may be carried out by the clock-controlled circuitry of Figure 1;

Figure 6 is a schematic diagram of an example detailed implementation of clock-controlled circuitry which corresponds to the Figure 1 clock-controlled circuitry; and

Figure 7 is a schematic diagram of an electrical or electronic device in which the clock-controlled circuitry of Figure 1 or 6 may be deployed.

Detailed Description of Embodiments

Embodiments relate to clock-controlled circuitry and devices/apparatus comprising such circuitry. As will be apparent, such circuitry may find particular use as an IC SoC (System on Chip) in a host device. It will become apparent that circuitry disclosed herein is advantageous in that it enables data such as audio data to cross from one clock domain to another without significant associated power consumption, size/cost (e.g. IC chip area) impact, or delay/latency penalty.

Figure 1 is a schematic diagram of clock-controlled circuitry 1000 embodying the present invention. As indicated, circuitry 1000 is organised into first and second clock domains, denoted Domain A and Domain B, respectively. Thus, various elements and signals in Figure 1 are given the label "A" or "B" to indicate the clock domain which they are associated with. Those labels will however be omitted in the following description where possible for simplicity.

Domain A comprises a signal generator 100 and a data communication unit 150. Similarly, Domain B comprises a signal generator 200 and a data communication unit 250.

As depicted in Figure 1, the signal generators 100 and 200 are both capable of acting in a "master" or "slave" mode. For example, the signal generator 100 may operate in master mode and the signal generator 200 may operate in slave mode, in which case the timing of certain signals generated by the signal generator 200 may be (at least at some point in time) related to or dependent on the timing of certain signals generated by the signal generator 100. Similarly, the signal generator 200 may operate in master mode and the signal generator 100 may operate in slave mode, in which case the timing of certain signals generated by the signal generator 100 may be (at least at some point in time) related to or dependent on the timing of certain signals generated by the signal generator 200.

It will later be explained however that in some arrangements it may be that one of the signal generators 100 and 200 is only capable of operating in master mode, in which case certain elements depicted in Figure 1 need not be provided.

Signal generator 100 comprises a clock generator 110, a frame generator 120 and a relationship controller 130. The relationship controller 130 comprises a retiming unit 132, a monitoring unit 134 and a setting unit 136. Signal generator 200 comprises a clock generator 210, a frame generator 220 and a relationship controller 230. The relationship controller 230 comprises a retiming unit 232, a monitoring unit 234 and a setting unit 236.

The clock generators 110 and 210 operate generally in the same way as one another, in that they receive a common global clock signal GCLK and output respective domain clock signals DCLKA and DCLKB. The clock generators 110 and 210 may however differ from one another in some respects, for example in terms of their precision/accuracy. Thus, it may be that on average the frequencies of the domain clock signals DCLKA and DCLKB are the same as one another, or have some defined

relationship to one another, but that over time the relationship fluctuates. Of course, this is just an example.

The frame generators 120 and 220 also operate generally in the same way as one another, based on their respective domain clock signals DCLKA and DCLKB. Indeed, it will be appreciated that various elements in the clock domains (e.g. in the signal generators 100 and 200) will be controlled by the relevant domain clock signal, or a clock signal derived therefrom, for synchronous operation, however such connections are not shown explicitly to avoid overcomplicating Figure 1.

Focussing on the frame generator 120 by way of example, **Figure 2** is a schematic diagram indicating example frame clock signals FCLKA which the frame generator 120 may output.

In Figure 2, the domain clock signal DCLKA is presented at the top, followed by example frame clock signals FCLKA-1 to FCLKA-5. The frame generator 120 is configured to generate a repetitive signal which is synchronised to the domain clock signal DCLKA, and this repetitive signal could be considered to be FCLKA-1 to FCLKA-5 collectively or indeed any one or more of them. It will be understood that each of FCLKA-1 to FCLKA-5 is an example of a repetitive signal which is synchronised to the domain clock signal DCLKA, and that the number of them and indeed the particular repeating pattern exhibited by them may vary from arrangement to arrangement.

The signals FCLKA-1 to FCLKA-4 have the form of pulse signals, i.e. signals which comprise a regular series of pulses, with the pulse or sample rates differing from one to the next. Merely as examples, signals FCLKA-1 to FCLKA-4 may have 64kHz, 32kHz, 16kHz and 8kHz sample rates, respectively. In the context of audio data, these pulse signals may be considered strobe signals and may be used within their clock domain (i.e. by data communication unit 150) to facilitate routing or sample-rate converting of audio data while maintaining phase between channels.

The number of such strobe signals and their sample rates may for example be programmable or configurable, with the absolute periodicity and absolute time in generation dependent on the domain clock signal DCLKA.

The signal FCLKA-5 has the form of a toggle signal, and in this example toggles between high and low in line with the pulses of signal FCLKA-3. The repetitive signals may thus have the form of pulse signals or toggle signals, or indeed may exhibit any other repetitive pattern.

It will be assumed for convenience of explanation that DCLKB corresponds to DCLKA in that they both have the same nominal (average) frequency, both being generated from the global clock signal GCLK, and that the frame generator 220 generates frame clock signals FCLKB-1 to FCLKB-5 based on DLKCB which are nominally the same as FCLKA-1 to FCLKA-5, respectively. In other arrangements there may be more significant differences between DCLKA and DLKCB, and between the signal(s) which make up FCLKA and FCLKB.

In order to consider how the signal generators 100 and 200 may affect one another, it will be assumed for now that the signal generator 100 operates in master mode and that the signal generator 200 operates in slave mode.

The frame generator 120 outputs a synchronisation signal SYNCA to the signal generator 200. It will be assumed that the signal SYNCA is the same as the signal FLCKA-5, although it could be any other signal (such as another FCLKA signal in Figure 2) which is indicative of a phase of the Domain A frame clock signals FLCKA. The synchronisation signal SYNCA is indicative of a phase of the other frame clock signals FCLKA-1 to FCLKA-4, since it is synchronised with them (all are synchronised with DCLKA). The signals SYNCA and FCLKA-3 are shown as the upper two signals in the signal diagram of **Figure 3**. Each of the signal traces shown in Figure 3 may be considered to show the change in voltage level of the signal concerned over time.

The synchronisation signal SYNCA is received by the retiming unit 232 and retimed to be synchronous to the domain clock signal DCLKB to produce the retimed equivalent signal SYNCA(R). **Figure 4** is a schematic diagram of merely one simple example implementation of the retiming unit 232, in which it comprises a plurality of flip-flops 232-1 and 232-2 connected together in a chain as indicated, and clocked by the domain clock signal DCLKB (i.e. a clock signal of the receiving clock domain, Domain

B). The synchronisation signal SYNCA is received at the D input of the first flip-flop 232-1, the Q output of that flip-flop 232-1 is connected to the D input of the second flip-flop 232-2, and the retimed synchronisation signal SYNCA(R) is output from the Q output of the second flip-flop 232-2 synchronously with the domain clock signal DCLKB. This synchroniser structure is useful for avoiding metastability problems which may arise were only one flip-flop to be used.

Returning to Figure 1, the monitoring unit 234 is connected to receive the retimed signal SYNCA(R) and to control the setting unit 236 (which may also receive the retimed signal SYNCA(R) as shown) to initialise operation of the frame generator 220 based on the retimed signal SYNCA(R). In particular, the frame generator 220 is controlled to output its frame clock signal FCLKB (which is considered in this example to be composed of component frame clock signals FCLKB-1 to FCLKB-5) with a timing linked to the domain clock signal DCLKB such that the frame clock signal FCLKB is set at that time to have a phase relationship with the frame clock signal FCLKA (here, comprising component frame clock signals FCLKA-1 to FCLKA-5) which meets a slave specification. The slave specification may comprise one or more parameters, which may be configurable or programmable, and which define the desired phase relationship.

In more detail, looking at Figure 2, the frame generator 120 is controlled to output its frame clock signal FCLKA with a timing linked to the domain clock signal DCLKA as indicated by the highlighted pulses of the signals DCLKA and FCLKA. That is, the first pulses (highlighted) of the frame clock signals FCLKA-1 to FCLKA-4 and the first rising edge of the toggle signal FCLKA-5 are aligned with (linked to, or triggered by) the highlighted pulse of the signal DCLKA. The frame generator 120 is configured to continue generating the frame clock signal FCLKA with that timing relative to the domain clock signal DCLKA, e.g. by way of a counter triggered by the domain clock signal DCLKA, unless it is reset or its operation is adjusted in some way. The monitoring unit 234 and the setting unit 236 then control the frame generator 220 to link the frame clock signal FCLKB to the domain clock signal DCLKB in a similar way, but such that at that time a phase relationship (an initial phase relationship) between the frame clock signals FCLKA and FCLKB meets the slave specification. The frame generator 220 may then continue to produce the frame clock signals FCLKB to have

the relevant repeating pulse/toggle pattern using, for example, a counter triggered by the domain clock signal DCLKB.

This setting of the phase relationship between the frame clock signals FCLKA and FCLKB can be appreciated by further consideration of Figure 3. The frame generator 220 outputs a synchronisation signal SYNCB, which is assumed here to be the same as the signal FLCKB-5 for consistency with the corresponding synchronisation signal SYCNA. The synchronisation signal SYNCB is indicative of a phase of the other frame clock signals FCLKB-1 to FCLKB-4, since it is synchronised with them (all are synchronised with DCLKB). The signals SYNCB and FCLKB-3 are shown in Figure 3.

As indicated in Figure 3, once the retimed signal SYNCA(R) has been established, e.g. after the retiming unit 232 has been enabled and its operation has stabilised, the frame generator 220 is controlled, based on the retimed signal SYNCA(R), to output the signals SYNCB and FCLKB-3 (amongst others) so that there is a phase difference between corresponding edges of SYNCA(R) and SYNCB which meets the slave specification. This is indicated as being a “programmable phase” in Figure 3 as an example, since this initial phase relationship may be configured by way of a parameter - such as a delay between signal edges - defined in the slave specification.

Because the signal SYNCA(R) is a retimed version of the signal SYNCA, by setting an initial phase relationship between SYNCA(R) and SYNCB effectively an initial phase relationship is also set between SYNCA and SYNCB, and thus also between FCLKA and FCLKB. For example, as can be appreciated from Figure 3, an initial phase relationship is set between FCLKA-3 and FCLKB-3. It will become apparent that it is the relationship between signals FCLKA and FCLKB which affects how data is handled.

The monitoring unit 234 is connected to receive the signals SYNCA(R) and SYNCB as indicated in Figure 1. Based on these signals, and after the timing of the frame clock signal FCLKB has been set relative to the domain clock signal DCLKB as mentioned above, the monitoring unit 234 is configured to monitor the phase relationship between the signals SYNCB and SYNCA(R) (indicative of the relationship between SYNCB and

SYNCA) to determine if that phase relationship has changed such that it no longer meets the slave specification.

This could for example involve detecting whether an edge of the signal SYNCB is within a monitoring window of defined duration and positioned in time relative to the signal SYNCA(R). Such a window is indicated as being a "programmable monitoring window" in Figure 3 as an example, since the window may be configured again by way of a parameter - such as a range of acceptable delays between signal edges - defined in the slave specification. The programmable monitoring window in Figure 3 is defined as beginning at a falling edge of the signal SYNCA(R) and having a defined duration.

Looking at Figure 3, the status of the signal generator 200 is indicated by the signal STATUS_B (not shown in Figure 2). Firstly, the signal generator 200 is in an "idle" state until it is enabled by the rising edge of an enable signal ENA_B (also not shown in Figure 2). The status then becomes "locking" as the signal SYNCA(R) becomes established and the frame clock signal FCLKB is generated with the desired phase relationship set as mentioned above, and "starting" as data transfer across the domain boundary begins (as discussed in more detail below). The status then becomes "monitoring" as the phase relationship between the signals SYNCB and SYNCA(R) is monitored.

In the example in Figure 3, if the corresponding falling edge of the signal SYNCB falls within the programmable monitoring window as shown (the edge is depicted in Figure 3 falling approximately in the middle of the window), then it is determined that the phase relationship continues to meet the slave specification. In that case, the frame generator 220 is allowed to continue generating the frame clock signal FCLKB at its current timing relative to the domain clock signal DCLKB.

If, however, the corresponding falling edge of the signal SYNCB no longer falls within the programmable monitoring window then it is determined that the phase relationship no longer meets the slave specification. This could occur, for example, due to a temporary glitch or failure in e.g. any of the clock generators 110 and 210 and the frame generators 120 and 220 or due to a cosmic event (e.g. an ionizing particle strike). In that case, the monitoring unit 234 and setting unit 236 act to re-set the timing

of the frame clock signal FCLKB relative to the domain clock signal DCLKB (e.g. by reinitialising the frame generator 220, or by adjusting its operation) such that the frame clock signal FCLKB is again set at that time to have a phase relationship with the frame clock signal FCLKA which meets the slave specification.

In this way, the desired phase relationship between the frame clock signal FCLKB and the frame clock signal FCLKA can quickly (e.g. immediately) be re-established. Of course, if the phase relationship is continually monitored (e.g. every falling edge of SYNCB is checked, in the context of the Figure 3 example), then the desired phase relationship between the frame clock signal FCLKB and the frame clock signal FCLKA may be re-established if necessary very quickly. However, in some arrangements it may be acceptable to monitor the phase relationship intermittently, e.g. from time to time, such that the desired phase relationship may be re-established less quickly.

Looking again at Figure 3, when the desired phase relationship between the frame clock signal FCLKB and the frame clock signal FCLKA is established, a data signal DATA_A handled by the data communication unit 150 in Domain A can be transferred to the data communication unit 250 in Domain B as data signal DATA_B, with the frames (D0, D1, D2) of the data signal DATA_A being aligned with (controlled by) the signal FCLKA-3 and the corresponding (received) frames (D0, D1, D2) of the data signal DATA_B being aligned with (controlled by) the signal FCLKB-3. In this respect, it can be seen that the frame clock signals FCLKA and FCLKB may be used by the data communication units 150 and 250 to handle data signals, and in particular their alignment or phase relative to one another.

For example, in some audio applications latency may be of particular importance. For example, there may be relatively strict requirements to move e.g. PCM audio data from one system location to another in the minimal clock or frame cycles possible. This may be to help ensure that there are no notable lags for mobile telephony, contextual awareness or audio/sensor fusion. From Figure 3 it can be seen that the latency between the frame D0 in DATA_A and D0 in DATA_B is less than a single frame length, which constitutes relatively low latency.

As another example, in some audio applications the number of clock cycles per data frame may need to be consistent. In some synchronisation schemes it is acceptable for the frame size to be jittery in the destination clock domain but this may be undesirable or even unacceptable in audio applications in which there are audio converters or audio interfaces that require an exact number of system clocks (domain clock signal cycles) per data frame to ensure a correct audio signal transfer function or correct interfacing with other audio interfaces. The re-establishment of the phase relationship as described above may help ensure such consistency in clock cycles per data frame.

It is thus clear that if the phase relationship were not re-established in the event of a temporary glitch or failure as above, data (e.g. audio samples) could be dropped or repeated as data is transferred to/from either domain and/or other disadvantages as explained above may ensue.

The data communication units 150 and 250 may comprise processing, routing and/or conversion (e.g. digital-to-analogue, or *vice versa*) circuitry. The data communication units 150 and 250 may also be considered to encompass input and/or output transducers, which in the context of audio data may include *inter alia* microphones and speakers.

With the ability to quickly detect a phase relationship outside, or not meeting, the slave specification and re-establish the phase relationship in line with the slave specification as mentioned above, the data signal DATA_B may only suffer loss of one or just a few such frames as compared to the data signal DATA_A as the phase relationship is re-established, which in the context of audio data may be imperceptible to the end-user (e.g. listening to the audio via a speaker).

Another advantage of the present technique is that there is no need for a deep (large) FIFO buffer or similar between the two clock domains to buffer the data signal DATA_A as it crosses the domain boundary to become data signal DATA_B. As mentioned above, the initial phase difference between the signals SYNCA(R) and SYNCB (i.e. effectively between FCLKA and FCLKB), indicated in Figure 3 as a "programmable phase", may be configured so that simple sampling of the data signal DATA_A as it

crosses the clock domain boundary to become data signal DATA_B will be sufficient. For example, retiming circuitry (not shown) such as that described in relation to retiming units 132 and 232 (see the example in Figure 4) may be used.

Also as mentioned above, the size of the monitoring window, indicated in Figure 3 as a "programmable monitoring window", may be configured by way of the slave specification so that an expected range of fluctuation in the phase relationship may be tolerated, within the operational capability of the retiming/synchronising circuitry used to convert the data signal DATA_A to the data signal DATA_B as it crosses the clock domain boundary. The size of the monitoring window and the initial phase difference may be parameters defined in the slave specification.

It will be appreciated that in Figure 3 it is assumed that the direction of data transfer is from Domain A to Domain B, i.e. from data communication unit 150 to data communication unit 250, so that data signal DATA_A becomes data signal DATA_B. In this case, the initial phase difference may be set as in Figure 3 such that the signal SYNCA(R) leads SYNCB (i.e. effectively FCLKA leads FCLKB), allowing the data retiming/synchronising/sampling time to occur. Of course, in another arrangement (not shown in Figure 3) it may be that the direction of data transfer is from Domain B to Domain A, i.e. from data communication unit 250 to data communication unit 150, so that data signal DATA_B becomes data signal DATA_A. In this case, the initial phase difference may be set such that the signal SYNCA(R) lags SYNCB (i.e. effectively FCLKA lags FCLKB), again so that the data retiming/synchronising/sampling has time to occur. Such a situation may occur if there is already a data signal being handled in Domain A when a situation occurs where it is necessary to transfer another data signal from Domain B to Domain A.

The situation may also occur that it is necessary to simultaneously transfer one data signal from Domain A to Domain B, and another data signal from Domain B to Domain A. In that case it may be that multiple pairs of frame generators such as frame generators 120 and 220 are employed. As another example, where the signal generator 100 is operating in master mode and the signal generator 200 is operating in slave mode as described so far, it may be that the component frame clock signals making up frame clock signal FCLKB are organised so that, when the initial phase

difference is set such that the signal SYNCA(R) leads SYNCB (i.e. effectively FCLKA leads FCLKB) as in Figure 3, there is at least one component frame clock signal of FCLKB which is staggered relative to the others so that it appears to lead FCLKA.

Incidentally, although only one frame clock signal FCLKA-3 (and corresponding frame clock signal FCLKB-3) is shown in Figure 3, there may in fact be a plurality of frame clock signals used in each of the clock domains running at different sample/pulse rates (see e.g. Figure 2) with corresponding different data signals (e.g. audio data signals) running at those rates.

Where the signal generator 100 is operating in master mode and the signal generator 200 is operating in slave mode as described so far, it may be that the sample rate adopted in Domain A is changed on-the-fly, i.e. while the signal generator 200 has the "monitoring" status as in Figure 3 with the frame clock signals FCLKA and FCLKB already running with a phase relationship which meets the slave specification. Such a change in sample rate may change the frame clock signal FCLKA so that it is necessary to re-establish the phase relationship between the frame clock signals FCLKA and FCLKB, and potentially also change the format (e.g. sample rate) of the frame clock signal FCLKB. In this case, the signal generator 100 may be configured to send a re-synch signal (not shown) to the signal generator 200 to cause the phase relationship between the frame clock signals FCLKA and FCLKB to be re-established as mentioned above, and potentially to also cause the format (e.g. sample rate) of the frame clock signal FCLKB to be changed accordingly.

As another example, where the signal generator 100 is operating in master mode and the signal generator 200 is operating in slave mode, with the frame clock signals FCLKA and FCLKB already running with a phase relationship which meets the slave specification, it may be that it is no longer necessary for the frame clock signal FCLKB to be slaved (in the sense of continued monitoring) to the frame clock signal FLCKA. This may be indicated for example by a release signal (not shown) received in the signal generator 200 from the signal generator 100 or indeed from a separate control unit (not shown). In such a case, the signal generator 200 may be configured to cease the monitoring of the phase relationship and to allow the frame generator 220 to continue to generate the frame clock signal FCLKB with its current timing relative to the

domain clock signal DCLKB. In this respect, the signal generator 200 may be considered to have transitioned from slave mode to master mode or another free-running mode.

The signal generator 200 may also transition from slave mode to master mode if the signal generator 100 ceases operation for some reason, for example if it is disabled. The signal generator 200 may for example monitor an enable signal (not shown) for the signal generator 100 to determine that is has been disabled, or may for example determine that the signal generator 100 has been disabled if it no longer receives a signal from the signal generator 100 such as the synchronisation signal SYNCA. In such a case, the signal generator 200 may again be configured to cease the monitoring of the phase relationship and to allow the frame generator 220 to continue to generate the frame clock signal FCLKB with its current timing relative to the domain clock signal DCLKB. In this respect, the signal generator 200 may again be considered to have transitioned from slave mode to master mode.

So far, the case where the signal generator 100 is operating in master mode and the signal generator 200 is operating in slave mode has been considered, along with situations where the signal generator 200 may transition from slave mode to master mode. In these cases, it has not been necessary to consider the relationship controller 130, which comprises the retiming unit 132, monitoring unit 134 and setting unit 136. As such, if only such cases are needed the relationship controller 130 need not be provided.

However, it will be appreciated from the above, that there may arise the case where the signal generator 200 is operating in master mode (e.g. because the signal generator 100 has been disabled) and the signal generator 100 is then enabled (e.g. re-enabled).

One possibility is of course that the signal generator 100 starts up in master mode again, and that the signal generator 200 is returned to slave mode, with the phase relationship re-established by way of the relationship controller 230 as described above. However, this may be disadvantageous if a data signal is already being handled by the signal generator 200 with it operating in master mode, since the

retiming of the FCLKB signal(s) relative to the domain clock signal DCLKB may cause a glitch or other disruption in that data signal.

Another possibility is thus for the signal generator 100, which had previously been in master mode before it was disabled (or which had not yet been enabled), to be started up in slave mode. In that case, the relationship controller 130 may be employed analogously to how the relationship controller 230 is employed when the signal generator 200 is in slave mode as described above. This may be understood from Figure 3, but with the signals denoted with "A" swapped for the equivalent signals denoted with "B", and *vice versa*. The above description relating to the signal generator 100 operating in master mode and the signal generator 200 operating in slave mode, including the related transfer of data between the two domains, thus applies here *mutatis mutandis* but with the signal generator 200 operating in master mode and the signal generator 100 operating in slave mode.

For example, once the retimed signal SYNCB(R) has been established, e.g. after the retiming unit 132 has been enabled and its operation has stabilised, the frame generator 120 may be controlled, based on the retimed signal SYNCB(R), to output the signals SYNCA and FCLKA-3 (amongst others) so that there is a phase difference between corresponding edges of SYNCB(R) and SYNCA which meets the or another slave specification. As in Figure 1, the monitoring unit 134 is connected to receive the signals SYNCA(R) and SYNCB. Based on these signals, and after the timing of the frame clock signal FCLKA has been set relative to the domain clock signal DCLKA, the monitoring unit 134 may be configured to monitor the phase relationship between the signals SYNCA and SYNCB(R) (indicative of a relationship between SYNCB and SYNCA) to determine if that phase relationship has changed such that it no longer meets the slave specification concerned. If it is determined that the phase relationship no longer meets the slave specification, the monitoring unit 134 and setting unit 136 may then act to re-set the timing of the frame clock signal FCLKA relative to the domain clock signal DCLKA (e.g. by reinitialising the frame generator 120, or by adjusting its operation) such that the frame clock signal FCLKA is again set at that time to have a phase relationship with the frame clock signal FCLKB which meets the slave specification.

To allow this operation, the relationship controller 130 accordingly needs to be provided. In that case, the signal generators 100 and 200 may be considered to have the same general structure and function as one another.

Looking at the relationship controller 230, as a representative one of the relationship controllers 130 and 230, it will be appreciated that there are a number of ways in which to monitor the master-slave synchronicity, i.e. the phase relationship between the signals SYNCB and SYNCA(R) (effectively between SYNCB and SYNCA, or FCLKB and FCLKA).

For example, if the signals SYNCB and SYNCA(R) are toggle signals as in Figure 3, a counter (e.g. in the monitoring unit 234) can be started when SYNCB and SYNCA(R) are not equal and stopped when they are. If the count falls outside a programmable or configurable value range (whose size represents the size of the monitoring window) it can be determined that the monitoring window has been exceeded (in either direction) – i.e. the phase relationship no longer meets the slave specification. For example, the range may be represented by a single value, and a count value larger than that value (or corresponding to a negative value) may indicate that the monitoring window has been exceeded.

In another example, if the signals SYNCB and SYNCA(R) signals are pulse signals, for example being FCLKB-3 and FCLKA-3(R), where FCLKA-3(R) is a retimed version of FCLKA-3, a counter (e.g. in the monitoring unit 234) can be started on an edge-detection of FCLKA-3(R) and incremented until the corresponding FCLKB-3 edge is detected. Again if the count falls outside a programmable or configurable value range (whose size represents the size of the monitoring window) it can be determined that the monitoring window has been exceeded (in either direction) – i.e. the phase relationship no longer meets the slave specification.

As above, if the monitoring unit 234 determines that the phase relationship no longer meets the slave specification, then the setting unit 236 (which may be a finite state machine) is controlled to cause the frame generator 220 to re-establish the desired phase relationship. This can effectively occur by causing the frame generator 220 to generate the next SYNCB signal (and the related FCLKB signals) with the given phase

relationship ("programmable phase", in Figure 3) after the next appropriate edge of the SYNCA(R) signal, i.e. after the equivalent delay has elapsed.

In these examples, knowing which of the signals SYNCB and SYNCA(R) leads or lags relative to the other allows the associated hardware of the monitoring unit 234 to be minimised, especially if using a counter, as it does not then need to count up an entire frame of clock cycles.

Incidentally, in Figure 1 it has been assumed that the phase-relationship monitoring is carried out in the one of the signal generators 100 and 200 which is in slave mode. However, it would be possible for that monitoring to be carried out outside that signal generator, for example in the one of the signal generators 100 and 200 which is in master mode. For example, looking at Figure 3, when the signal generator 200 is in slave mode the monitoring could be carried out by the monitoring unit 134 using signals SYNCA and SYNCB(R), with the monitoring unit 134 then controlling the setting unit 236 or the frame generator 220 directly. Equally, in some arrangements the functionality of the monitoring and setting units could be provided outside the signal generators (e.g. in a common control unit).

Figure 5 is a schematic diagram of a method 300 which may be carried out by the clock-controlled circuitry 1000, for example by one of the signal generators 100 and 200. For consistency with Figure 3, method 300 as depicted in Figure 5 has been tailored specifically for operation by the signal generator 200 however it could equally be tailored for operation by the signal generator 100 by replacing references to Domain A and its elements with references to Domain B and its elements, and *vice versa*.

Method 300 comprises steps S2 to S22.

In step S2, it is determined whether Domain A (i.e. signal generator 100) is already enabled and in master mode, for example such that it is already generating frame clock signal FCLKA. This determination may be carried out by the signal generator 200 itself, for example based on a signal received from the signal generator 100. In such a case, the data communication unit 150 may already be handling a data signal based on frame clock signal FCLKA.

If signal generator 100 is already enabled and in master mode (S2, YES), the method proceeds to step S4. Otherwise (S2, NO), the method proceeds to step S22.

In step S4, the signal generator 200 determines that it should operate in slave mode and the method proceeds to step S6, in which the signal generator 200 establishes the retimed synchronisation signal SYNCA(R) based on SYNCA received from the signal generator 100.

The method then proceeds to step S8, in which the timing of the frame clock signal FCLKB is set relative to the domain clock signal DCLKB so that there is an initial phase relationship (defined by a slave specification) between the signals SYNCA(R) and SYNCB which translates to an acceptable initial phase relationship between the signals FCLKB and FCLKA.

The method then proceeds to step S10 in which the ongoing phase relationship is monitored. If the phase relationship continues to meet the slave specification (S12, YES), the method proceeds to step S14. Otherwise (S12, NO), the method returns to step S8 where the timing of the frame clock signal FCLKB is re-set relative to the domain clock signal DCLKB so that there is again an intended initial phase relationship (defined by a slave specification) between the signals SYNCA(R) and SYNCB.

In step S14, it is determined whether a re-synch signal has been received by the signal generator 200, for example from the signal generator 100. If a re-synch signal has been received (S14, YES), the method proceeds back to step S8, optionally via step S20 if it is necessary to adjust the sample rate or some other parameter of signal FCLKB based on the re-synch signal. If a re-synch signal has not been received (S14, NO), the method proceeds to step S16.

In step S16, it is determined whether a release signal has been received by the signal generator 200, for example from the signal generator 100. If it has (S14, YES), the method proceeds to step S22. If it has not (S16, NO), the method proceeds to step S18.

In step S18, it is determined whether Domain A (in particular, signal generator 100) has been disabled, for example based on a signal received (or no longer received) from the signal generator 100. If it has (S14, YES), the method proceeds to step S22. If it has not (S16, NO), the method returns to step S10.

In step S22 it is determined that the signal generator 200 of Domain B may operate in master mode, or in a similar free-running mode. In that case, the timing of the frame clock signal FCLKB is set (or is left set) relative to the domain clock signal DCLKB but without needing to consider (or monitor) any phase relationship between FCLKB and any signal from Domain A. The frame clock signal FCLKB may then continue to run with that timing relative to the domain clock signal DCLKB.

Although not shown in Figure 5, at any time the signal generator 200 may be disabled in which case the method 300 may terminate. It will be appreciated that the ordering of certain steps in method 300 is just an example. For example, steps S14 and S16 may occur between steps S8 and S10.

Of course, although only two clock domains are shown in Figure 1, there may be more than two clock domains with for example signal generator 100 operating in master mode and two or more signal generators (equivalent to signal generator 200 but in different clock domains) operating in slave mode in a master-slave relationship with signal generator 100. The present disclosure will be understood accordingly.

The different clock domains may be or be part of different power domains, so that the different domains may be powered on or off independently. For example, in the case of implementation in a host device such as a mobile telephone, it may be desirable to have one power domain operating as an “always on” domain which can react quickly to an external stimulus (such an audio signal picked up by a microphone), and another (e.g. central) power domain which is powered down unless it is “woken up” by the always on domain (perhaps via a higher-level application processor or the like). As another consideration, the different clock and/or power domains may be provided on the same IC chip or on different chips which are connected to one another.

It will be understood that, provided that the two (or more) clock generators share the same root, master or global clock signal (see GCLK in Figure 1) then, under programmatic control, one (or more) frame generator(s) can be slaved to the other frame generator such that their phase is guaranteed or controlled within the bounds of clock-domain-crossing and clock-jitter error. The global clock signal GCLK in Figure 1 may be used directly by the clock generators 110 and 210, or may be provided to them via a clock synthesis circuit such as a PLL (Phase Lock Loop).

By way of summary, in a possible arrangement the start-up of the slaved frame generator(s) is controlled to manage the phase relationship between itself and the master frame generator using a retimed version of a strobe or frame clock signal provided from the master frame generator as a synchronisation signal. Once started, the phase relationship is monitored e.g. in the slaved frame generator(s) to determine whether it moves unexpectedly, i.e. such that the slave specification is no longer met. If it does then the relevant slaved frame generator(s) is resynchronized automatically - re-establishing the master-slave phase relationship. If the master frame generator's sample rate is changed on-the-fly then the slave frame generator is again resynchronized automatically (e.g. on receipt of a re-synch signal). If the master frame generator is disabled the running slave frame generator may automatically become a master frame generator – i.e. no longer monitoring the master-slave phase relationship. If the original frame generator (which had been the master slave generator) is restarted it may by default be slaved to the new master frame generator. This has the benefit of avoiding unnecessary dropped or repeated samples on running data (e.g. audio) channels. At any time, a slaved frame generator may be set to free-run mode (e.g. on receipt of a release signal), i.e. no longer monitoring the master-slave phase relationship. This is akin to being set to master mode.

Figure 6 is a schematic diagram of an example detailed implementation of clock-controlled circuitry 2000 which corresponds to clock-controlled circuitry 1000, useful for better understanding a possible application of the circuitry disclosed herein.

Clock-controlled circuitry 2000 has the form of a SoC, i.e. and IC chip configured for audio processing. The circuitry 2000 is divided into an “always on” (AO) clock and power domain, labelled Domain A for comparison with Figure 1, and a central clock

and power domain, labelled Domain B again for comparison with Figure 1. External connections to input and/or output transducers are shown, along with power (VDD) connections, for both domains.

Both domains are shown having clock and frame generators, corresponding to those in Figure 1. The digital mixing core and DSP in the AO domain (along with the other circuitry in the data path(s) between transducers and e.g. the other domain and/or the external connection to an external application/comms/DSP processor) may thus correspond to the data communication unit 150 in Figure 1, and the digital mixing core in the central domain (along with the other circuitry in the data path between transducers and e.g. the other domain and/or the external connection to an external application/comms/DSP processor) may thus correspond to the data communication unit 250 in Figure 1.

In this regard, the frame generator in the AO domain (Domain A) may generate frame clock signals equivalent to FCLKA in Figure 1, and one or both of the frame generators in the central domain (Domain B) may generate frame clock signals equivalent to FCLKB in Figure 1, for use by the data communication units concerned.

Thus, one typical scenario may be that an audio data stream is first received from the relevant input transducer by the data communication unit circuitry in the AO domain (Domain A) with the frame generator in that domain thus operating in master mode. At that time, the central domain may be powered down, or in a low-power mode. The data may for example be routed to an external application processor via the external connection to the AO domain, which subsequently “wakes up” the central domain, i.e. transitions it into a powered-up or operational mode. Once powered up, one or both of the frame generators in the central domain (Domain B) may be slaved to the frame generator in the AO domain (Domain A), so that an audio data stream may be passed from the digital mixing core of the AO domain to that of the central domain without causing glitches or suffering significant latency. It will be appreciated that the functionality disclosed herein may help enable low latency transfer of such audio between domains, with reduced risk of audio artefacts or similar.

It will already be understood that clock-controlled circuitry considered herein may be implemented in a host device, for example an electrical or electronic device. Examples include a portable and/or battery powered host device such as a mobile telephone, an audio player, a video player, a PDA, a mobile computing platform such as a laptop computer or tablet and/or a games device, for example.

Figure 7 is a schematic diagram of an electrical or electronic device 3000, which may be considered such a host device. Device 3000 comprises clock-controlled circuitry 1000 or 2000 as considered earlier herein, connected to interact with other circuitry (not shown) of the electrical or electronic device 3000.

The skilled person will recognise that some aspects of the above described apparatus (circuitry) and methods may be embodied as processor control code, for example on a non-volatile carrier medium such as a disk, CD- or DVD-ROM, programmed memory such as read only memory (Firmware), or on a data carrier such as an optical or electrical signal carrier. For example, the configuration unit may be implemented as a processor operating based on processor control code.

For some applications, such aspects will be implemented on a DSP (Digital Signal Processor), ASIC (Application Specific Integrated Circuit) or FPGA (Field Programmable Gate Array). Thus the code may comprise conventional program code or microcode or, for example, code for setting up or controlling an ASIC or FPGA. The code may also comprise code for dynamically configuring re-configurable apparatus such as re-programmable logic gate arrays. Similarly, the code may comprise code for a hardware description language such as Verilog TM or VHDL. As the skilled person will appreciate, the code may be distributed between a plurality of coupled components in communication with one another. Where appropriate, such aspects may also be implemented using code running on a field-(re)programmable analogue array or similar device in order to configure analogue hardware.

Some embodiments of the present invention may be arranged as part of an audio processing circuit, for instance an audio circuit (such as a codec or the like) which may be provided in a host device as discussed above. A circuit or circuitry according to an embodiment of the present invention may be implemented as an integrated circuit (IC),

for example on an IC chip. One or more input or output transducers may be connected to the integrated circuit in use.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The word "comprising" does not exclude the presence of elements or steps other than those listed in the claim, "a" or "an" does not exclude a plurality, and a single feature or other unit may fulfil the functions of several units recited in the claims. Any reference numerals or labels in the claims shall not be construed so as to limit their scope.

CLAIMS:

1. Clock-controlled circuitry organised into at least first and second clock domains, the first clock domain configured to operate based on a first clock signal and the second clock domain configured to operate based on a second clock signal, wherein:

the first clock domain comprises a first signal generator operable to generate a first repetitive signal comprising a repeating pattern of pulses synchronised to the first clock signal;

the second clock domain comprises a second signal generator operable to generate a second repetitive signal comprising a repeating pattern of pulses synchronised to the second clock signal;

the first signal generator is operable, when operating in master mode, to output to the second signal generator a first synchronisation signal indicative of a phase of the first repetitive signal, wherein the first synchronisation signal is a pulse signal, and is part or all of the first repetitive signal or derived from the first repetitive signal; and

the second signal generator is operable, when operating in slave mode, to:

set a timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is set to have a phase relationship with the first repetitive signal which then meets a slave specification; and

re-set the timing of the second repetitive signal relative to the second clock signal if it is determined that the phase relationship has changed such that it no longer meets the slave specification,

wherein the second signal generator, or another signal generator of the clock-controlled circuitry, is operable:

to monitor the phase relationship between the second repetitive signal and the first repetitive signal after the timing of the second repetitive signal relative to the second clock signal has been set, by monitoring a phase relationship between corresponding edges of the second repetitive signal and the first synchronisation signal or between corresponding edges of the second repetitive signal and a retimed first synchronisation signal being a retimed version of the first synchronisation signal; and

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to determine if that phase relationship has changed such that it no longer meets the slave specification.

2. The clock-controlled circuitry as claimed in claim 1, wherein the second signal generator is operable to re-set the timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is again set to have a phase relationship with the first repetitive signal which then meets the slave specification.

3. The clock-controlled circuitry as claimed in claim 1 or 2, wherein the first and second repetitive signals comprise regular series of pulses.

4. The clock-controlled circuitry as claimed in any of the preceding claims, wherein the second signal generator or the other signal generator is operable to monitor the phase relationship between the second repetitive signal and the first repetitive signal by obtaining a count value indicative of the phase relationship by:

incrementing a counter between corresponding edges of the second repetitive signal and the first synchronisation signal or retimed first synchronisation signal; or

incrementing a counter while the second repetitive signal and the first synchronisation signal or retimed first synchronisation signal have the same value as one another; or

incrementing a counter while the second repetitive signal and the first synchronisation signal or retimed first synchronisation signal have different values from one another.

5. The clock-controlled circuitry as claimed in any of the preceding claims, wherein the second signal generator is operable:

when operating in slave mode, to receive a release signal, and, if the release signal is received, to transition its operation to free-running mode; and

in connection with the transition to free-running mode, to continue generation of the second repetitive signal at its existing timing relative to the second clock signal without taking account of the phase relationship between the second repetitive signal and the first repetitive signal.

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6. The clock-controlled circuitry as claimed in any of the preceding claims, wherein the second signal generator is operable:

when operating in slave mode, to receive a re-synch signal indicating a change in the first repetitive signal, and, if the re-synch signal is received, to re-set the timing of the second repetitive signal relative to the second clock signal.

7. The clock-controlled circuitry as claimed in claim 6, wherein:

the re-synch signal indicates a change in a repeating pattern of the first repetitive signal; and

the second signal generator is operable, if the re-synch signal is received, to re-set the timing of the second repetitive signal relative to the second clock signal based on the re-synch signal and re-configure the second repetitive signal based on the change in the repeating pattern indicated by the re-synch signal.

8. The clock-controlled circuitry as claimed in any of the preceding claims, wherein the second signal generator is operable, when operating in slave mode, to monitor operation of the first signal generator, and, if the first signal generator is determined to become disabled, to:

transition its operation to master mode; and then

continue generation of the second repetitive signal at its existing timing relative to the second clock signal without taking account of the phase relationship between the second repetitive signal and the first repetitive signal, and output a second synchronisation signal indicative of a phase of the second repetitive signal.

9. The clock-controlled circuitry as claimed in claim 8, wherein the first signal generator is operable, when re-enabled after being disabled, to:

monitor operation of the second signal generator and determine if the second clock control circuit is operating in master mode; and

when it is determined that the second clock control circuit is operating in master mode, operate in slave mode.

10. The clock-controlled circuitry as claimed in claim 9, wherein the first signal generator is operable, when operating in slave mode, to:

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set a timing of the first repetitive signal relative to the first clock signal based on the second synchronisation signal so that the first repetitive signal is set to have a phase relationship with the second repetitive signal which then meets the slave specification; and

re-set the timing of the first repetitive signal relative to the first clock signal if it is determined that that phase relationship has changed such that it no longer meets the slave specification.

11. The clock-controlled circuitry as claimed in claim 10, wherein the first signal generator is operable to re-set the timing of the first repetitive signal relative to the first clock signal based on the second synchronisation signal so that the first repetitive signal is again set to have a phase relationship with the second repetitive signal which then meets the slave specification.

12. The clock-controlled circuitry as claimed in claim 10 or 11, wherein the first signal generator, or another signal generator of the clock-controlled circuitry, is operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal after the timing of the first repetitive signal relative to the first clock signal has been set and to determine if that phase relationship has changed such that it no longer meets the slave specification.

13. The clock-controlled circuitry as claimed in claim 12, wherein the first signal generator or that other signal generator is operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal by monitoring a phase relationship between the first repetitive signal and the second synchronisation signal.

14. The clock-controlled circuitry as claimed in claim 12 or 13, wherein the first signal generator or that other signal generator is operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal by monitoring a phase relationship between the first repetitive signal and a retimed second synchronisation signal being a retimed version of the second synchronisation signal.

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15. The clock-controlled circuitry as claimed in claim 13 or 14, wherein the first signal generator or that other signal generator is operable to monitor the phase relationship between the first repetitive signal and the second repetitive signal by obtaining a count value indicative of the phase relationship by:

incrementing a counter between corresponding edges of the first repetitive signal and the second synchronisation signal or retimed second synchronisation signal; or

incrementing a counter while the first repetitive signal and the second synchronisation signal or retimed second synchronisation signal have the same value as one another; or

incrementing a counter while the first repetitive signal and the second synchronisation signal or retimed second synchronisation signal have different values from one another.

16. The clock-controlled circuitry as claimed in any of claims 8 to 15, wherein the second synchronisation signal is part or all of the second repetitive signal, or is derived from the second repetitive signal.

17. The clock-controlled circuitry as claimed in any of the preceding claims, wherein the first signal generator and second signal generator are operable to generate the first and second clock signals, respectively, based on the same global clock signal.

18. The clock-controlled circuitry as claimed in any of the preceding claims, wherein the first repetitive signal comprises a plurality of different component repetitive signals synchronised with the first clock signal, and/or the second repetitive signal comprises a plurality of different component repetitive signals synchronised with the second clock signal.

19. The clock-controlled circuitry as claimed in any of the preceding claims, organised into at least first and second power domains, wherein the first power domain comprises the first clock domain and the second power domain comprises the second clock domain.

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20. The clock-controlled circuitry as claimed in claim 19, comprising first and second IC chips, wherein the first IC chip comprises the first power domain and the second IC chip comprises the second power domain.

21. The clock-controlled circuitry as claimed in any of the preceding claims, comprising a first data communication unit in the first clock domain and configured to operate based on the first clock signal, and a second data communication unit in the second clock domain and configured to operate based on the second clock signal, wherein:

the first data communication unit is operable to process a first data signal which is synchronous with the first clock signal, based on the first repetitive signal;

the second data communication unit is configured to process a second data signal which is synchronous with the second clock signal, based on the second repetitive signal; and

the first and second communication units are configured to transfer such a data signal between them based on their respective first and second repetitive signals and via a retiming circuit so that the first data signal becomes the second data signal or *vice versa*.

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22. The clock-controlled circuitry as claimed in claim 21, wherein the data signals are audio data signals, and wherein the clock-controlled circuitry is clock-controlled audio circuitry.

23. The clock-controlled circuitry as claimed in claim 22, wherein the audio data signals are organised into frames, and wherein the first and second data communication units are configured to align the frames in their respective audio data signals with their respective repetitive signals.

24. The clock-controlled circuitry as claimed in any of the preceding claims, comprising storage for storing information defining the slave specification, wherein:

the first signal generator and/or the second signal generator is configured to set the timing concerned based on the information; and/or

the determination that a said phase relationship has changed such that it no longer meets the slave specification is made based on the information.

25. The clock-controlled circuitry as claimed in claim 24, wherein the information comprises parameter values, and wherein

the first signal generator and/or the second signal generator is configured to set the timing concerned based on one or more of the parameter values; and/or

the determination that a said phase relationship has changed such that it no longer meets the slave specification is made based on one or more of the parameter values.

26. The clock-controlled circuitry as claimed in claim 24 or 25, comprising a controller operable to store the information in the storage so as to define the slave specification currently in use, optionally based on a user input.

27. The clock-controlled circuitry as claimed in any of the preceding claims, implemented as an integrated circuit.

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28. A method of controlling clock-controlled circuitry which is organised into at least first and second clock domains, the first clock domain configured to operate based on a first clock signal and the second clock domain configured to operate based on a second clock signal, wherein:

the first clock domain comprises a first signal generator operable to generate a first repetitive signal comprising a repeating pattern of pulses synchronised to the first clock signal;

the second clock domain comprises a second signal generator operable to generate a second repetitive signal comprising a repeating pattern of pulses synchronised to the second clock signal; and

the first signal generator is operable, when operating in master mode, to output to the second signal generator a first synchronisation signal indicative of a phase of the first repetitive signal, wherein the first synchronisation signal is a pulse signal, and is part or all of the first repetitive signal or derived from the first repetitive signal,

the method comprising controlling the second signal generator, when operating in slave mode, to:

set a timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive

signal is set to have a phase relationship with the first repetitive signal which then meets a slave specification; and

re-set the timing of the second repetitive signal relative to the second clock signal if it is determined that the phase relationship has changed such that it no longer meets the slave specification,

wherein the second signal generator, or another signal generator of the clock-controlled circuitry, is operable:

to monitor the phase relationship between the second repetitive signal and the first repetitive signal after the timing of the second repetitive signal relative to the second clock signal has been set, by monitoring a phase relationship between corresponding edges of the second repetitive signal and the first synchronisation signal or between corresponding edges of the second repetitive signal and a retimed first synchronisation signal being a retimed version of the first synchronisation signal; and

to determine if that phase relationship has changed such that it no longer meets the slave specification.

29. A computer program which, when executed on a processor of clock-controlled circuitry, causes the clock-controlled circuitry to carry out a control method,

wherein:

the clock-controlled circuitry is organised into at least first and second clock domains;

the first clock domain is configured to operate based on a first clock signal and the second clock domain is configured to operate based on a second clock signal;

the first clock domain comprises a first signal generator operable to generate a first repetitive signal comprising a repeating pattern of pulses synchronised to the first clock signal;

the second clock domain comprises a second signal generator operable to generate a second repetitive signal comprising a repeating pattern of pulses synchronised to the second clock signal; and

the first signal generator is operable, when operating in master mode, to output to the second signal generator a first synchronisation signal indicative of a phase of the first repetitive signal, wherein the first synchronisation signal is a pulse signal, and is part or all of the first repetitive signal or derived from the first repetitive signal,

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the method comprising controlling the second signal generator, when operating in slave mode, to:

set a timing of the second repetitive signal relative to the second clock signal based on the first synchronisation signal so that the second repetitive signal is set to have a phase relationship with the first repetitive signal which then meets a slave specification; and

re-set the timing of the second repetitive signal relative to the second clock signal if it is determined that the phase relationship has changed such that it no longer meets the slave specification,

wherein the second signal generator, or another signal generator of the clock-controlled circuitry, is operable:

to monitor the phase relationship between the second repetitive signal and the first repetitive signal after the timing of the second repetitive signal relative to the second clock signal has been set, by monitoring a phase relationship between corresponding edges of the second repetitive signal and the first synchronisation signal or between corresponding edges of the second repetitive signal and a retimed first synchronisation signal being a retimed version of the first synchronisation signal; and

to determine if that phase relationship has changed such that it no longer meets the slave specification.

30. A computer-readable medium having the computer program of claim 29 stored thereon.

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Electronic Acknowledgement Receipt

EFS ID:	46744944
Application Number:	17723130
International Application Number:	
Confirmation Number:	3228
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	1-IDS.pdf	1282636 e0dd52533cc68bcc00a3c8d32e50091d34269ffd	no	4

Warnings:

Information:					
2	Foreign Reference	FR1-GB2426164A.pdf	633117 75dca957dff4074f1580bbffc4a0de1ef751f5b3	no	16
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3	Foreign Reference	FR2-GB2572463B.pdf	2118668 f4c56691952facf837182ac07b74e62b95e0c426	no	46
Warnings:					
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	17723130
Filing Date	2022-04-18
First Named Inventor	Nima Badizadegan
Art Unit	2632
Examiner Name	
Attorney Docket Number	00287-0016

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	10037568	B2	2018-07-31	Taylor et al.	
	2	10169814	B2	2019-01-01	Parsons et al.	
	3	4068188	A	1978-01-10	Yokoyama	
	4	4745372	A	1988-05-17	Miwa	
	5	8467418	B2	2013-06-18	Aweya et al.	
	6	7333570	B2	2008-02-19	Aung et al.	
	7	7080345	B1	2006-07-18	Iotov	
	8	9330740	B1	2016-05-03	Baeckler et al.	

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	Art Unit	2632
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	Attorney Docket Number	00287-0016

	9	9001951	B1	2015-04-07	Kumpulainen	
	10	10411720	B2	2019-09-10	Lenzen et al.	
	11	6675306	B1	2004-01-06	Baxter	
	12	7084709	B1	2006-08-01	Leong, et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20190025413	A1	2019-01-24	Liu et al.	

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17723130
	Filing Date	2022-04-18
	First Named Inventor	Nima Badizadegan
	Art Unit	2632
	Examiner Name	
	Attorney Docket Number	00287-0016

	1	XILINX, "7 Series FPGAs GTX/GTH Transceivers - User Guide," Page 26, available at https://www.xilinx.com/support/documentation/user_guides/ug476_7Series_Transceivers.pdf (August 14, 2018).	
	2	SARAH HARRIS, "Timing & Synchronization," Harvey Mudd College Engineering Department, Page 24, available at https://cseweb.ucsd.edu/classes/wi06/cse291-b/slide/let4/timingint.pdf (January 31, 2006).	
	3	SAM PALERMO, "ECEN 720 High-Speed Links: Circuits and Systems - Lab 5," Texas A&M University, Page 5, available at: http://ece.tamu.edu/~spalermo/ecen689/ECEN720_lab5_2017.pdf (2017).	
	4	ALTERA, "Stratix V Device Handbook," Volume 2: Transceivers, Intel, Page 13, available at: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-v/stx5_xcvr.pdf (February 15, 2017).	
	5	STACKEXCHANGE, "Phase Frequency Detector in PLL," StackExchange, available at: https://electronics.stackexchange.com/questions/301402/phase-frequency-detector-in-pll (April 24, 2017).	
	6	IEEE STANDARDS ASSOCIATION, "IEEE Standards for Ethernet," IEEE 802.3-2018, Section 4, Clauses 49 and 51, Section 6, Clauses 82 and 83, available at: https://standards.ieee.org/standard/802_3-2018.html (August 31, 2018).	
	7	SLOBODAN MILIJEVIC, "The basics of synchronized Ethernet," EE Times-Asia, available at: https://www.microsemi.com/document-portal/doc_view/126475-the-basics-of-synchronized-ethernet-synce.	
	8	MACIEJ LIPINSKI, et al., "White Rabbit: a PTP Application for Robust Sub-nanosecond Synchronization," 2011 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control and Communication, Munich, Pages 25-30, available at: http://white-rabbit.web.cern.ch/documents/White_Rabbit-a_PTP_application_for_robust_sub-nanosecond_synchronization.pdf (2011).	
	9	FLOYD M. GARDNER, "Phaselock Techniques," Third Edition, Wiley-Interscience, Chapters 1, 4, 9, 10, 11, 13, and 17 (2005).	
	10	JENS TWIEFEL, et al., "Digital signal processing for an adaptive phase-locked loop controller," Proceedings of SPIE - The International Society for Optical Engineering, Volume 6926 (April 2008).	
	11	CHEN YAO, "Time to Digital Converter used in ALL digital PLL," Master of Science Thesis In System-on-Chip Design, Stockholm (August 2011).	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17723130
	Filing Date	2022-04-18
	First Named Inventor	Nima Badizadegan
	Art Unit	2632
	Examiner Name	
	Attorney Docket Number	00287-0016

	12	BEHZAD RAZAVI, "A CIRCUIT FOR ALL SEASONS: The StrongARM Latch," IEEE Solid-State Circuits Magazine (Spring 2015).
	13	PING LU, et al., "A 2-D GRO Vernier Time-to-Digital Converter with Large Input Range and Small Latency," Lund University - EIT Department, University of Toronto, IEEE Radio Frequency Integrated Circuits Symposium (2013).
	14	CHRISTIAN LEBER, et al. "High Frequency Trading Acceleration using FPGAs," University of Heidelberg, International Conference on Field Programmable Logic and Applications, Germany (2011).
	15	INTERNATIONAL TELECOMMUNICATION UNION, "Timing and synchronization aspects in packet networks," ITU-T, G.8261/Y.1361, International Telecommunication Union (May 2006).
	16	INTERNATIONAL TELECOMMUNICATION UNION, "Distribution of timing information through packet networks," ITU-T, G.8264/Y.1364, International Telecommunication Union (August 2017).
	17	IEEE STANDARDS ASSOCIATION, "IEEE Standards for Ethernet," IEEE 802.3-2018, Section 4, Figure 52-4, page 634 (2018)

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17723130
	Filing Date	2022-04-18
	First Named Inventor	Nima Badizadegan
	Art Unit	2632
	Examiner Name	
	Attorney Docket Number	00287-0016

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Keith J. Barkaus/	Date (YYYY-MM-DD)	2022-06-02
Name/Print	Keith J. Barkaus	Registration Number	51,431

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	45861077
Application Number:	17723130
International Application Number:	
Confirmation Number:	3228
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	00287-0016
Receipt Date:	02-JUN-2022
Filing Date:	18-APR-2022
Time Stamp:	15:07:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	1-TransmittalLetter.pdf	125888 1bff78ffa1a18bd72195801ccad8d326f4a7c862	no	3

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	2-IDS.pdf	622164 a8f731a92bb37695be415f4a308ca14ea3122488	no	6
Warnings:					
Information:					
			Total Files Size (in bytes):	748052	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: HFT Solutions, LLC	Confirmation No.: 3228
Application No.	: 17/723,130	
Filed	: April 18, 2022	
For	: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	
TC/A.U.	: 2632	
Examiner	: TBD	
Docket No.	: 00287-0016	
Customer No.	: 01912	

INFORMATION DISCLOSURE STATEMENT LETTER
UNDER 37 CFR § 1.56

Via EFS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant would like to direct the Examiner's attention to the references that are listed on the attached forms PTO/SB/08A. In addition to any copies of Foreign Patent Documents and Non-Patent Literature Documents submitted herewith, Applicant refers the Examiner to the references previously submitted to or cited by the Patent Office during prosecution of U.S. Patent Application No. 17/236,577 filed April 21, 2021, now U.S. Patent No. 11,329,655, U.S. Patent Application No. 16/937,309 filed July 23, 2020, now U.S. Patent No. 11,018,678, U.S. Patent Application No. 16/888,218 filed May 29, 2020, now U.S. Patent No. 10,763,865 and U.S. Patent Application No. 16/670,702 filed October 31, 2019, now U.S. Patent No. 10,771,069 from which the subject application claims priority under 35 U.S.C. § 120. Accordingly, pursuant to 37 C.F.R. § 1.98(d), copies of previously cited or submitted references and Non-Patent Literature Documents are not included with this Information Disclosure Statement.

Reference to Related Patents and Co-Pending Applications

The below chart provides information regarding related issued patents and co-pending applications filed by the present Applicant:

SERIAL NO.	ATTORNEY DOCKET NO.	FILING DATE	STATUS
16/672,076	00287-0007	2019-11-01	Issued USP 10,826,502
16/670,702	00287-0008	2019-10-31	Issued USP 10,771,069
16/888,218	00287-0009	2020-05-29	Issued USP 10,763,865
16/937,314	00287-0011	2020-07-23	Issued USP 10,931,286
16/937,309	00287-0012	2020-07-23	Issued USP 11,018,678
17/248,304	00287-0013	2021-01-19	Issued USP 11,128,305
17/236,577	00287-0014	2021-04-21	Issued USP 11,329,655
17/405,188	00287-0015	2021-08-18	Allowed – Notice of Allowance mailed 2022-05-25
17/723,130	00287-0016	2022-04-18	Present Application
17/723,145	00287-0017	2022-04-18	Docketed New Case - Ready for Examination

The Examiner is invited to review the prosecution history of each of these applications, including the cited references of record and related office actions, as the Examiner deems appropriate.

* * * * *

As provided by 37 C.F.R. § 1.97(g) and (h), no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information, and no inference should be made that the information and references cited are, or are considered to be, material to patentability because they are in this statement. No inference should be made that the information and references cited are prior art merely because they are in the statement.

Since this Information Disclosure Statement is being filed within three months of the filing date and before the mailing date of a first Office Action on the merits in the present application, Applicant believes that no fee is required in connection with the filing of this Statement. Applicant(s) hereby petition(s) that the Information Disclosure Statement be considered. Please charge any fee deficiency or credit any overpayment to Deposit Account No.

01-1785 as needed to ensure consideration of the disclosed information under order no. 00287-0016.

Respectfully submitted

AMSTER, ROTHSTEIN & EBENSTEIN LLP
Attorneys for Applicant
90 Park Avenue
New York, NY 10016
(212) 336-8000

Dated: New York, New York
June 2, 2022

By: /Keith J. Barkaus /
Keith J. Barkaus
Reg. No. 51,431

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/723,130

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	80		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	350		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	400		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	12 minus 20 =	*	x 50 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*	x 240 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			210			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	1040		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/723,130	04/18/2022	2827	1040	00287-0016	12	1

CONFIRMATION NO. 3228

1912
AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

FILING RECEIPT

OC000000133302915

Date Mailed: 04/20/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Nima Badizadegan, Salem, NH;

Applicant(s)

HFT Solutions, LLC, New Canaan, CT;

Power of Attorney: The patent practitioners associated with Customer Number 1912

Domestic Priority data as claimed by applicant

This application is a CON of 17/236,577 04/21/2021 PAT 11329655
which is a CON of 16/937,309 07/23/2020 PAT 11018678
which is a CON of 16/888,218 05/29/2020 PAT 10763865
which is a CON of 16/670,702 10/31/2019 PAT 10771069
which claims benefit of 62/808,404 02/21/2019

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/20/2022

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/723,130**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

**** SMALL ENTITY ****

Title

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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Application Number	
Filing Date	Herewith
First Named Inventor	Nima Badizadegan
Title	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP
Art Unit	
Examiner Name	
Attorney Docket Number	00287-0016

SIGNATURE of Applicant or Patent Practitioner

Signature	/Keith J. Barkaus/	Date (Optional)	2022-04-18
Name	Keith J. Barkaus	Registration Number	51,431
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

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Signature		Date (Optional)	04/04/2022
Name	Corey Horowitz		
Title	Chairman and Chief Executive Officer		

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Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [■] The attached application, or
- [ ] United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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Inventor: Nima Badizadegan Date (Optional) :_____

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FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application No. 17/236,577, filed on April 21, 2021 and entitled FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP, which is a continuation of U.S. Patent Application No. 16/937,309, filed on July 23, 2020 and entitled FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP, which is a continuation of U.S. Patent Applicant No. 16/888,218, filed on May 29, 2020 and entitled "FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP," which in turn is a continuation of U.S. Patent Application No. 16/670,702, filed on October 31, 2019 and entitled "FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP," which claims the benefit of and priority to U.S. Provisional Patent Application No. 62/808,404, filed on February 21, 2019 and entitled FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP, the contents of all of which are incorporated by reference herein in their entirety.

FIELD

[0002] The present invention generally relates to a field programmable gate array system. In embodiments, the present invention generally relates to a field programmable gate array and an external or internal phase controller providing phase matching between a receiver clock and a transmitter clock used in the field programmable gate array.

BACKGROUND

[0003] Field programmable gate arrays (FPGAs) may be used in applications that require fast processing since FPGAs allow for all computations to occur on a single chip that has massive fine-grained parallelism. For example, FPGAs are used in the financial industry in high frequency trading where the rapid processing of the FPGA is desired. One technological problem with FPGAs is that there is a need to synchronize receiving side and transmitting side clock signals within the FPGA.

[0004] The prior art sought to address this problem by including a clock domain crossing circuit in the FPGA. However, these circuits inherently add a delay to the processing that takes place in the FPGA, which is not desirable since high frequency trading may include timestamps that are accurate to the microsecond such that even small delays may present a large problem.

[0005] Synchronous Ethernet systems were designed with the similar goal of synchronizing a transmitter to a receiver. However, since phase alignment in synchronous Ethernet is not necessary, synchronous Ethernet FPGA systems usually do not phase-align the receiver and transmitter sides of a link. The received clock is output from the transceiver to an external clock generation circuit to be used as its frequency reference. As a result, there is no measurement of the internal transmit clock at all by the Ethernet FPGA system.

[0006] While a synchronous Ethernet system with an internal PLL compares the transmit clock to the receive clock, its phase-frequency detector in the internal PLL is configured to measure accurately only the frequency but does not have to measure the phase of the two clocks accurately. In addition, synchronized protocols of the synchronous Ethernet system use simpler control loops that do not have to compensate for a lot of wander or jitter. Accordingly, the phase of the clocks is not treated as important as frequency by the synchronous Ethernet FPGA system. Based on these reasons, synchronous Ethernet FPGA systems do not provide a desirable solution to a technological problem of synchronizing receiving side and transmitting side clock signals within the FPGA.

[0007] Accordingly, a technical problem is presented in FPGAs in that phase synchronization between the receiver side clock and the transmitter side clock will introduce unwanted latency that results in delay of processing. Accordingly, it would be beneficial to provide an FPGA system that avoids these problems and provides sub-microsecond processing with throughput of at least 10 Gbps. In embodiments, the sub-microsecond processing throughput may be: 10-25 Gbps, 22-33 Gbps, 33-45 Gbps, 45-60 Gbps, 60-80 Gbps, 80-120 Gbps, to name a few.

SUMMARY

[0008] An object of the present invention is to address technological challenges that currently exist in phase matching receiver side and transmitter side clocks of a FPGA without introducing unnecessary delay in processing.

[0009] This and other objects shall be addressed by embodiments of the present invention as set forth herein.

[0010] The present invention generally relates to a field programmable gate array system and a method for processing a data stream using a field programmable gate array system. In embodiments, the present invention generally relates to a field programmable gate array and an external or internal phase controller providing phase matching between a receiver clock and a transmitter clock used in the field programmable gate array.

[0011] More particularly, the present invention relates to a field programmable gate array system includes (a) a field programmable gate array comprising (1) a first interface including: (A) a first reference clock pin, wherein said first reference clock pin is configured to receive a first clock signal having a first frequency and a first phase; (B) a second reference clock pin, wherein said second reference clock pin is configured to receive a second clock signal having a second frequency and a second phase; (C) a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream; (D) a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream; (2) a deserializer operationally connected to: (x) the first reference clock pin to receive as a first input the first clock signal and (y) the first plurality of data pins to receive as a second input the first serial data stream, and wherein the deserializer is configured to: (A) convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams, and (B) generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase; and (C) transmit the first plurality of parallel data streams and the first receiver side clock signal within the field programmable gate array; (3) computational circuitry operationally connected to the deserializer to receive the first plurality of parallel data streams and the first receiver side clock signal, wherein the computational circuitry is configured to perform a first set of operations on the first plurality of parallel data streams to generate a second plurality of parallel processed data streams having a second amount of data streams; (4) a serializer operationally connected to: (x) the second reference clock pin to receive as a third input a first wire rate clock signal based on the second clock signal, wherein the first wire rate clock signal has a fourth frequency and a fourth phase; (y) the second plurality of data pins to transmit as a first output the second serial data stream; (z) the computational circuity, wherein the serializer receives the second plurality of parallel processed data streams from the

computational circuity and the serializer transmits to the computational circuitry a first transmitter side clock signal including a fifth frequency and a fifth phase; and wherein the serializer is configured to: (A) convert the second plurality of parallel processed data streams into the second serial data stream; (B) generate the first transmitter side clock signal based on the first wire rate signal, wherein the first transmitter side clock signal has the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency; and (C) transmit the second serial data stream to the second plurality of data pins for transmission off the field programmable gate array; (5) a second interface including: (A) a first clock output pin configured to transmit the first receiver side clock signal, wherein the first clock output pin is operationally connected to the deserializer; and (B) a second clock output pin configured to transmit the first transmitter side clock signal, wherein the second clock output pin is operationally connected to the serializer; and (b) a phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit includes: (1) a phase detector operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array, and wherein the phase detector is configured to compare the third phase of the first receiver side clock signal to the fifth phase of the transmitter side clock signal and to generate a phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the fifth phase of the transmitter side clock signal; (2) a phase controller operationally connected to the phase detector and configured to receive the phase difference indicator signal, and wherein the phase controller is configured to determine adjustment information based on the phase difference indicator signal; and (3) an adjustable oscillator operationally connected to the phase controller and configured to receive the adjustment information as well as operationally connected to the second reference clock pin of the first interface of the field programmable gate array, wherein the adjustable oscillator is configured to generate the second clock signal including the second frequency and the second phase based on the adjustment information and transmit the second clock signal to the second reference clock pin of the first interface of the field programmable gate array; wherein the transmitter side clock signal and the first receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the fifth phase.

[0012] In embodiments, the third frequency corresponds to the first frequency.

[0013] In embodiments, the third phase is not aligned with the first phase.

[0014] In embodiments, the third frequency is different than the first frequency.

[0015] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams. In embodiments, the adjustment information is used to do at least one of the following (i) set a bias to an oscillator; (ii) to set a divider ratio; and (iii) to set a delay.

[0016] In embodiments, the first set of operations includes an arithmetic operation. In embodiments, the first set of operations includes a logical operation. In embodiments, the first set of operations includes a pipeline operation. In embodiments, the first set of operations includes a memory access operation.

[0017] In embodiments, the first amount of data streams is the same as the second amount of data streams.

[0018] In embodiments, the first amount of data streams and the second amount of data streams are equal to eight (8) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to sixteen (16) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to twenty (20) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-two (32) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to forty (40) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to sixty-four (64) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to eighty (80) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to one hundred twenty-eight (128) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to one hundred sixty (160) data streams.

[0019] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer. In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the first amount of data streams and the

second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0020] In embodiments, the field programmable gate array further includes a phase lock loop configured to: receive the second clock signal, as a fourth input, to generate the first wire rate clock signal; and (B) transmit the first wire rate clock signal as the third input, to the serializer.

[0021] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.

[0022] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.

[0023] In embodiments, the fourth frequency is a rational multiple of the second frequency.

[0024] In embodiments, the phase difference indicator signal is a pulse signal.

[0025] In embodiments, the adjustment information indicates a desired phase. In embodiments, the adjustment information indicates a desired frequency. In embodiments, the adjustment information indicates a change in phase. In embodiments, the adjustment information indicates a change in frequency. In embodiments, adjustment information comprises a voltage. In embodiments, adjustment information comprises a digital transmission. In embodiments adjustment information further comprises a digital transmission.

[0026] In some embodiments, the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.

[0027] In embodiments, the trading algorithm includes the steps of: (a) parsing market data; (b) performing mathematical operations at a portion of the market data; and (c) generating order packets using at least an output of (b).

[0028] In embodiments, the first serial data stream includes market data and the second serial stream includes trading data.

[0029] In embodiments, the field programmable gate array includes a transceiver phase locked loop operatively connected between the to the serializer and the first reference clock pin.

[0030] In embodiments, the transceiver phase locked loop operatively connected between the serializer and the first reference clock pin includes a second adjustable oscillator to provide the first wire rate signal.

[0031] In embodiments, a second adjustable oscillator is provided outside of the transceiver phase locked loop and operatively connected to the serializer.

[0032] In embodiments, the second adjustable oscillator is programmable with a desired delay.

[0033] In embodiments, the desired delay is a constant value

[0034] In embodiments, the constant value is zero.

[0035] In embodiments, the adjustment information is provided to the second adjustable oscillator to provide the first wire rate signal.

[0036] The present invention also relates to a field programmable gate array system comprising (a) a field programmable gate array comprising (1) a first interface comprising (A) a first reference clock pin, wherein said first reference clock pin is configured to receive a first clock signal having a first frequency and a first phase; (B) a second reference clock pin, wherein said second reference clock pin is configured to receive a second clock signal having a second frequency and a second phase; (C) a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream; (D) a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream; (2) a deserializer operationally connected to (A) the first reference clock pin to receive as a first input the first clock signal and (B) the first plurality of data pins to receive as a second input the first serial data stream, and wherein the deserializer is configured to (A) convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams, and (B) generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase; and (C) transmit the first plurality of parallel data streams and the first receiver side clock signal within the field programmable gate array; (3) computational circuitry operationally connected to the deserializer to receive the first plurality of parallel data streams and the first receiver side clock signal, wherein the computational circuitry is configured to perform a first set of operations on the first plurality of parallel data

streams to generate a second plurality of parallel processed data streams having a second amount of data streams; (4) a serializer operationally connected to (A) a transceiver phase lock loop to receive as a third input a first wire rate clock signal based on the second clock signal, wherein the first wire rate clock signal has a fourth frequency and a fourth phase; (B) the second plurality of data pins to transmit as a first output the second serial data stream; (C) the computational circuity, wherein the serializer receives the second plurality of parallel processed data streams from the computational circuity and the serializer transmits to the computational circuitry a first transmitter side clock signal including a fifth frequency and a fifth phase; and wherein the serializer is configured to (A) convert the second plurality of parallel processed data streams into the second serial data stream; (B) generate the first transmitter side clock signal based on the first wire rate signal, wherein the first transmitter side clock signal has the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency; and (C) transmit the second serial data stream to the second plurality of data pins for transmission off the field programmable gate array; (5) a second interface comprising (A) a first clock output pin configured to transmit the first receiver side clock signal, wherein the first clock output pin is operationally connected to the deserializer; and (B) a second clock output pin configured to transmit the first transmitter side clock signal, wherein the second clock output pin is operationally connected to the serializer; and (b) a phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises (1) a phase detector operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array, and wherein the phase detector is configured to compare the third phase of the first receiver side clock signal to the fifth phase of the transmitter side clock signal and to generate a phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the fifth phase of the transmitter side clock signal; (2) a phase controller operationally connected to the phase detector and configured to receive the phase difference indicator signal, and wherein the phase controller is configured to determine adjustment information based on the phase difference indicator signal; and (3) an adjustable oscillator operationally connected to the phase controller and configured to receive the adjustment information as well as operationally connected to the second reference clock pin of the first interface of the field programmable gate array, wherein the adjustable oscillator is configured to generate the second clock signal including the second frequency and the second phase based on

the adjustment information and transmit the second clock signal to the second reference clock pin of the first interface of the field programmable gate array, wherein the transmitter side clock signal and the first receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the fifth phase.

[0037] In embodiments, the third frequency corresponds to the first frequency.

[0038] In embodiments, the third phase is not aligned with the first phase.

[0039] In embodiments, the third frequency is different than the first frequency.

[0040] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

[0041] In embodiments, the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

[0042] In embodiments, the first amount of data streams is the same as the second amount of data streams.

[0043] In embodiments, the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

[0044] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

[0045] In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

[0046] In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0047] In embodiments, the transceiver phase lock loop is operationally connected to the second reference clock pin and is configured to: (A) receive the second clock signal, as a fourth

input, to generate the first wire rate clock signal; and (B) transmit the first wire rate clock signal as the third input, to the serializer.

[0048] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.

[0049] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.

[0050] In embodiments, the fourth frequency is a rational multiple of the second frequency.

[0051] In embodiments, the phase difference indicator signal is a pulse signal.

[0052] In embodiments, adjustment information indicates at least one of the following: (A) a desired phase; (B) a desired frequency; (C) a change in phase; and (D) a change in frequency.

[0053] In embodiments, adjustment information comprises a voltage.

[0054] In embodiments, adjustment information comprise a digital transmission.

[0055] In embodiments, the adjustment information is used to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay.

[0056] In embodiments, the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.

[0057] In embodiments, the first serial data stream includes market data and the second serial data stream includes trading data.

[0058] In embodiments, the field programmable gate array system further comprises (a) a fourth plurality of data pins of the first interface, wherein the fourth plurality of data pins is configured to transmit a fourth serial data stream; (b) a second deserializer operationally connected to (i) the first reference clock pin to receive the first clock signal as a third input to the second deserializer, wherein the second deserializer is configured to: (A) receive a third serial data stream; (B) convert the third serial data stream into a third plurality of parallel data streams having a third amount of data streams; (C) generate a second receiver side clock signal based on the first clock signal, wherein the second receiver side clock signal has a sixth frequency and a sixth phase; and (D) transmit within the field programmable gate array to the computational circuitry the third plurality of parallel data streams and the second receiver side clock signal; (ii) the computational

circuitry further configured to (A) receive the third plurality of parallel data streams and the second receiver side clock signal; and (B) generate a fourth plurality of parallel processed data streams having a fourth amount of data streams; (c) a second serializer operationally connected to: (i) the transceiver phase lock loop to receive as a fifth input the first wire rate clock signal based on the second clock signal; and (ii) the fourth plurality of data pins to transmit as a second output the fourth serial data stream, wherein the second serializer is configured to (A) receive the fourth plurality of parallel processed data streams from the computational circuity; (B) convert the fourth plurality of parallel processed data streams into the fourth serial data stream; (C) transmit the fourth serial data stream to the fourth plurality of data pins for transmission off the field programmable gate array; (d) a third clock output pin of the second interface configured to transmit the second receiver side clock signal, wherein the third clock output pin is operationally connected to the second deserializer; and (e) a second phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises: (i) a second phase detector operationally connected to the first clock output pin and the third clock output pin of the second interface of the field programmable gate array, wherein the second phase detector is configured to (A) compare the third phase of the first receiver side clock signal to the sixth phase of the second receiver side clock signal; and (B) generate a second phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the sixth phase of the second receiver side clock signal; (ii) a second phase controller operationally connected to the second phase detector and configured to receive the second phase difference indicator signal, wherein the second phase controller is configured to determine second adjustment information based on the second phase difference indicator signal; and (iii) a delay element operationally connected to the second phase controller and to the second deserializer, wherein the second phase controller sends to the delay element the second adjustment information, wherein the delay element is configured to (A) delay the third serial data stream based on the second adjustment information, and (B) transmit the third serial data stream to the second deserializer, wherein the first receiver side clock signal and the second receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the sixth phase.

[0059] In embodiments, the field programmable gate array system further comprises a third plurality of data pins of the first interface, wherein the delay element is placed on the field programmable gate array and operationally connected to the third plurality of data pins and

wherein the delay element is further configured to (A) receive the third serial data stream via the third plurality of data pins, and (B) transmit the third serial data stream to the second deserializer.

[0060] In embodiments, the field programmable gate array system further comprises a third plurality of data pins of the first interface, wherein (A) the delay element is placed outside of the field programmable gate array, (B) the delay element and the second deserializer are operationally connected to the third plurality of data pins, and (C) the third plurality of data pins is further configured to transmit the third serial data stream from the delay element to the second deserializer.

[0061] The present invention also relates to a method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of (a) receiving, by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream; (b) receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase; (c) transmitting, from the first plurality of data pins of the first interface to a deserializer in the field programmable gate array, the first serial data stream; (d) transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal; (e) generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal; (f) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams; (g) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal; (h) transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams; (i) transmitting, from the deserializer via a first clock output pin on a second interface of the field programmable gate array to a phase detector that is part of the field programmable gate array system and not part of the field programmable gate array, the first receiver side clock signal; (j) generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level: (i) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase; (ii) generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock

signal; (iii) generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase; (iv) transmitting, from the serializer via a second clock output pin of the second interface to the phase detector, the interim transmitter side clock signal; (v) generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal; (vi) transmitting, from the phase detector to a phase controller of the field programmable gate array system which is placed within the field programmable gate array, the first output; (vii) determining, by the phase controller, interim adjustment information based on the first output; and (viii) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information, wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through (viii) are repeated until the first output of the phase detector is below the first threshold level; (k) transmitting, from the serializer to the computational circuitry, first transmitter side clock signal; (l) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams; (m) transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams; (n) converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and (o) transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface, the second serial data stream.

[0062] In embodiments, step (a) is performed before step (b).

[0063] In embodiments, step (b) is performed before step (a).

[0064] In embodiments, step (a) and step (b) are performed contemporaneously.

[0065] In embodiments, step (c) is performed before step (d).

[0066] In embodiments, step (d) is performed before step (c).

[0067] In embodiments, step (c) and step (d) are performed contemporaneously.

[0068] In embodiments, step (e) is performed before step (f).

[0069] In embodiments, step (f) is performed before step (e).

[0070] In embodiments, step (e) and step (f) are performed contemporaneously.

[0071] In embodiments, the second frequency corresponds to the first frequency.

[0072] In embodiments, the second phase is not aligned with the first phase.

[0073] In embodiments, the second frequency is different from the first frequency.

[0074] In embodiments, step (g) is performed before step (h).

[0075] In embodiments, step (h) is performed before step (g).

[0076] In embodiments, step (g) and step (h) are performed contemporaneously.

[0077] In embodiments, the step (i) comprises transmitting, from the deserializer to the phase detector, the first receiver side clock signal via a first zero delay buffer phase lock loop of the field programmable gate array before transmitting the first receiver side clock signal via the first clock output pin of the second interface.

[0078] In embodiments, the third frequency corresponds to the second frequency.

[0079] In embodiments, the third phase is aligned with the second phase.

[0080] In embodiments, a difference between the third phase and the second phase is less than a second threshold level

[0081] In embodiments, the sixth frequency corresponds to the third frequency.

[0082] In embodiments, the sixth phase is not aligned with the third phase prior to the first output of the phase detector being below the first threshold level.

[0083] In embodiments, the step (j)(iv) comprises transmitting, from the serializer to the phase detector, the interim transmitter side clock signal via a second zero delay buffer phase lock loop of the field programmable gate array before transmitting the interim transmitter side clock signal via the second clock output pin of the second interface.

[0084] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

[0085] In embodiments, the first amount of data streams is the same as the second amount of data streams.

[0086] In embodiments, the first amount of data streams and the second amount of data streams is one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen

(16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; and (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

[0087] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

[0088] In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

[0089] In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0090] In embodiments, at least a portion of the first set of operations is performed prior to step (k).

[0091] In embodiments, at least a portion of the first set of operations is performed after step (k).

[0092] In embodiments, all of the first set of operations is performed after step (k).

[0093] In embodiments, the transmission of the second serial data stream from the serializer off the field programmable gate array is transmitted to an input/output module off the field programmable gate array.

[0094] In embodiments, the first serial data stream includes market data and the second serial data stream includes trading data.

[0095] In embodiments, the step of generating the first wire rate clock signal further includes: (a) receiving, from the adjustable oscillator at a transceiver phase lock loop via a second reference clock pin in the first interface, the second clock signal; (b) processing, by the transceiver phase lock loop, the received second clock signal; (c) providing, by the transceiver phase lock loop, the first wire rate clock signal based on the processing of the received clock signal; and (d) transmitting, by the transceiver phase lock loop, the first wire rate clock signal to the serializer.

[0096] In embodiments, a phase lock loop generates the first wire rate clock signal.

[0097] In embodiments, the phase lock loop is on the field programmable gate array.

[0098] In embodiments, the phase lock loop that is part of the field programmable gate array system and not part of the field programmable gate array.

[0099] In embodiments, the step of generating the first wire rate clock signal further includes: (a) processing the second clock signal; (b) providing the first wire rate clock signal based on the processing of the second clock signal; and (c) transmitting, to the serializer, the first wire rate clock signal.

[0100] In embodiments, the sixth frequency corresponds to the third frequency.

[0101] In embodiments, the sixth phase is not aligned with the third phase.

[0102] The present invention also relates to a field programmable gate array system comprising: (a) a field programmable gate array comprising (1) a first interface comprising (A) a first reference clock pin, wherein said first reference clock pin is configured to receive a first clock signal having a first frequency and a first phase; (B) a second reference clock pin, wherein said second reference clock pin is configured to receive a second clock signal having a second frequency and a second phase; (C) a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream; (D) a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream; (2) a deserializer operationally connected to (A) the first reference clock pin to receive as a first input the first clock signal and (B) the first plurality of data pins to receive as a second input the first serial data stream, and wherein the deserializer is configured to (A) convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams; (B) generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase; and (C) transmit the first plurality of parallel data streams and the first receiver side clock signal within the field programmable gate array; (3) computational circuitry operationally connected to the deserializer to receive the first plurality of parallel data streams and the first receiver side clock signal, wherein the computational circuitry is configured to perform a first set of operations on the first plurality of parallel data streams to generate a second plurality of parallel processed data streams having a second amount of data streams; (4) a serializer operationally connected to (A) a transceiver phase lock loop to receive as a third input a first wire rate clock signal based on the second clock signal, wherein the first wire rate clock signal has a fourth frequency and a fourth phase; (B) the second plurality of

data pins to transmit as a first output the second serial data stream; (C) the computational circuity, wherein the serializer receives the second plurality of parallel processed data streams from the computational circuity and the serializer transmits to the computational circuitry a first transmitter side clock signal including a fifth frequency and a fifth phase; and wherein the serializer is configured to (A) convert the second plurality of parallel processed data streams into the second serial data stream; (B) generate the first transmitter side clock signal based on the first wire rate signal, wherein the first transmitter side clock signal has the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency; and (C) transmit the second serial data stream to the second plurality of data pins for transmission off the field programmable gate array; and (b) a phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises (1) a phase detector configured to compare the third phase of the first receiver side clock signal to the fifth phase of the transmitter side clock signal and to generate a phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the fifth phase of the transmitter side clock signal; (2) a phase controller operationally connected to the phase detector and configured to receive the phase difference indicator signal, and wherein the phase controller is configured to determine adjustment information based on the phase difference indicator signal; and (3) a phase lock loop with phase adjustment operationally connected to the phase controller and configured to receive the adjustment information as well as operationally connected to the second reference clock pin of the first interface of the field programmable gate array, wherein the phase lock loop with phase adjustment is configured to generate the second clock signal including the second frequency and the second phase based on the adjustment information and transmit the second clock signal to the second reference clock pin of the first interface of the field programmable gate array, wherein the transmitter side clock signal and the first receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the fifth phase.

[0103] In embodiments, the third frequency corresponds to the first frequency.

[0104] In embodiments, the third phase is not aligned with the first phase.

[0105] In embodiments, the third frequency is different than the first frequency.

[0106] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

[0107] In embodiments, the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

[0108] In embodiments, the first amount of data streams is the same as the second amount of data streams.

[0109] In embodiments, the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

[0110] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

[0111] In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

[0112] In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0113] In embodiments, the transceiver phase lock loop is operationally connected to the second reference clock pin and is configured to (A) receive the second clock signal, as a fourth input, to generate the first wire rate clock signal; and (B) transmit the first wire rate clock signal as the third input, to the serializer.

[0114] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.

[0115] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.

[0116] In embodiments, the fourth frequency is a rational multiple of the second frequency.

[0117] In embodiments, the phase difference indicator signal is a pulse signal.

[0118] In embodiments, adjustment information indicates at least one of the following: (A) a desired phase; (B) a desired frequency; (C) a change in phase; and (D) a change in frequency.

[0119] In embodiments, adjustment information comprises a voltage.

[0120] In embodiments, adjustment information comprise a digital transmission.

[0121] In embodiments, the adjustment information is used to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay.

[0122] In embodiments, the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.

[0123] In embodiments, the first serial data stream includes market data and the second serial data stream includes trading data.

[0124] In embodiments, the field programmable gate array system further comprises: (5) a second interface comprising (A) a first clock output pin configured to transmit the first receiver side clock signal, wherein the first clock output pin is operationally connected to the deserializer; and (B) a second clock output pin configured to transmit the first transmitter side clock signal, wherein the second clock output pin is operationally connected to the serializer; and wherein the phase detector is not on the field programmable gate array and is operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array.

[0125] In embodiments, the field programmable gate array system further comprises (a) a fourth plurality of data pins of the first interface, wherein the fourth plurality of data pins is configured to transmit a fourth serial data stream; (b) a second deserializer operationally connected to: (i) the first reference clock pin to receive the first clock signal as a third input to the second deserializer, wherein the second deserializer is configured to (A) receive a third serial data stream; (B) convert the third serial data stream into a third plurality of parallel data streams having a third amount of data streams; (C) generate a second receiver side clock signal based on the first clock signal, wherein the second receiver side clock signal has a sixth frequency and a sixth phase; and (D) transmit within the field programmable gate array to the computational circuitry the third plurality of parallel data streams and the second receiver side clock signal; (ii) the computational circuitry further configured to (A) receive the third plurality of parallel data streams and the second

receiver side clock signal; and (B) generate a fourth plurality of parallel processed data streams having a fourth amount of data streams; (c) a second serializer operationally connected to: (i) the transceiver phase lock loop to receive as a fifth input the first wire rate clock signal based on the second clock signal; and (ii) the fourth plurality of data pins to transmit as a second output the fourth serial data stream, wherein the second serializer is configured to (A) receive the fourth plurality of parallel processed data streams from the computational circuity; (B) convert the fourth plurality of parallel processed data streams into the fourth serial data stream; (C) transmit the fourth serial data stream to the fourth plurality of data pins for transmission off the field programmable gate array; and (d) a second phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises (i) a second phase detector configured to (A) compare the third phase of the first receiver side clock signal to the sixth phase of the second receiver side clock signal; and (B) generate a second phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the sixth phase of the second receiver side clock signal; (ii) a second phase controller operationally connected to the second phase detector and configured to receive the second phase difference indicator signal, wherein the second phase controller is configured to determine second adjustment information based on the second phase difference indicator signal; and (iii) a delay element operationally connected to the second phase controller and to the second deserializer, wherein the second phase controller sends to the delay element the second adjustment information, wherein the delay element is configured to (A) delay the third serial data stream based on the second adjustment information, and (B) transmit the third serial data stream to the second deserializer, wherein the first receiver side clock signal and the second receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the sixth phase.

[0126] In embodiments, the field programmable gate array system further comprises a third plurality of data pins of the first interface, wherein the delay element is placed on the field programmable gate array and operationally connected to the third plurality of data pins and wherein the delay element is further configured to (A) receive the third serial data stream via the third plurality of data pins, and (B) transmit the third serial data stream to the second deserializer.

[0127] In embodiments, the field programmable gate array system further comprises a third plurality of data pins of the first interface, wherein (A) the delay element is placed outside of the field programmable gate array, (B) the delay element and the second deserializer are

operationally connected to the third plurality of data pins, and (C) the third plurality of data pins is further configured to transmit the third serial data stream from the delay element to the second deserializer.

[0128] In embodiments, the field programmable gate array system further comprises (A) a first clock output pin of a second interface of the field programmable gate array, the first clock output pin being configured to transmit the first receiver side clock signal from the deserializer to the second phase detector; and (B) a third clock output pin of the second interface configured to transmit the second receiver side clock signal from the second deserializer to the second phase detector, wherein the second phase detector is not placed on the field programmable gate array and is operationally connected to the first clock output pin and the third clock output pin of the second interface of the field programmable gate array.

[0129] The present invention also relates to a method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of: (a) receiving, by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream; (b) receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase; (c) transmitting, from the first plurality of data pins of the first interface to a deserializer in the field programmable gate array, the first serial data stream; (d) transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal; (e) generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal; (f) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams; (g) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal; (h) transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams; (i) transmitting, from the deserializer to a phase detector of the field programmable gate array system, the first receiver side clock signal; (j) generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level: (i) generating, by a phase lock loop with phase adjustment in the field programmable gate array system, a second clock signal

having a fourth frequency and a fourth phase; (ii) generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal; (iii) generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase; (iv) transmitting, from the serializer to the phase detector, the interim transmitter side clock signal; (v) generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal; (vi) transmitting, from the phase detector to a phase controller of the field programmable gate array system which is placed within the field programmable gate array, the first output; (vii) determining, by the phase controller, interim adjustment information based on the first output; and (viii) transmitting, from the phase controller to the phase lock loop with phase adjustment, the interim adjustment information; wherein, the phase lock loop with phase adjustment adjusts the second clock signal based on the interim adjustment information and steps (i) through (viii) are repeated until the first output of the phase detector is below the first threshold level; (k) transmitting, from the serializer to the computational circuitry, first transmitter side clock signal; (l) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams; (m) transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams; (n) converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and (o) transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface, the second serial data stream.

[0130] In embodiments, step (a) is performed before step (b).

[0131] In embodiments, step (b) is performed before step (a).

[0132] In embodiments, step (a) and step (b) are performed contemporaneously.

[0133] In embodiments, step (c) is performed before step (d).

[0134] In embodiments, step (d) is performed before step (c).

[0135] In embodiments, step (c) and step (d) are performed contemporaneously.

[0136] In embodiments, step (e) is performed before step (f).

[0137] In embodiments, step (f) is performed before step (e).

[0138] In embodiments, step (e) and step (f) are performed contemporaneously.

[0139] In embodiments, the second frequency corresponds to the first frequency.

[0140] In embodiments, the second phase is not aligned with the first phase.

[0141] In embodiments, the second frequency is different from the first frequency.

[0142] In embodiments, step (g) is performed before step (h).

[0143] In embodiments, step (h) is performed before step (g).

[0144] In embodiments, step (g) and step (h) are performed contemporaneously.

[0145] In embodiments, the phase detector is not placed on the field programmable gate array and the step (i) comprises transmitting, from the deserializer to the phase detector via a first clock output pin on a second interface of the field programmable gate array, the first receiver side clock signal.

[0146] In embodiments, the step (i) further comprises transmitting, from the deserializer to the phase detector, the first receiver side clock signal via a first zero delay buffer phase lock loop of the field programmable gate array before transmitting the first receiver side clock signal via the first clock output pin of the second interface.

[0147] In embodiments, the third frequency corresponds to the second frequency.

[0148] In embodiments, the third phase is aligned with the second phase.

[0149] In embodiments, a difference between the third phase and the second phase is less than a second threshold level

[0150] In embodiments, the sixth frequency corresponds to the third frequency.

[0151] In embodiments, the sixth phase is not aligned with the third phase prior to the first output of the phase detector being below the first threshold level.

[0152] In embodiments, the phase detector is not placed on the field programmable gate array and the step (j)(iv) comprises transmitting, from the serializer to the phase detector via a second clock output pin of the second interface of the field programmable gate array, the interim transmitter side clock signal.

[0153] In embodiments, the step (j)(iv) further comprises transmitting, from the serializer to the phase detector, the interim transmitter side clock signal via a second zero delay buffer phase lock loop of the field programmable gate array before transmitting the interim transmitter side clock signal via the second clock output pin of the second interface.

[0154] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

[0155] In embodiments, the first amount of data streams is the same as the second amount of data streams.

[0156] In embodiments, the first amount of data streams and the second amount of data streams is one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

[0157] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

[0158] In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

[0159] In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0160] In embodiments, at least a portion of the first set of operations is performed prior to step (k).

[0161] In embodiments, at least a portion of the first set of operations is performed after step (k).

[0162] In embodiments, all of the first set of operations is performed after step (k).

[0163] In embodiments, the transmission of the second serial data stream from the serializer off the field programmable gate array is transmitted to an input/output module off the field programmable gate array.

[0164] In embodiments, the first serial data stream includes market data and the second serial data stream includes trading data.

[0165] In embodiments, the step of generating the first wire rate clock signal further includes: (a) receiving, from the phase lock loop with phase adjustment at a transceiver phase lock loop via a second reference clock pin in the first interface, the second clock signal; (b) processing, by the transceiver phase lock loop, the received second clock signal; (c) providing, by the transceiver phase lock loop, the first wire rate clock signal based on the processing of the received clock signal; and (d) transmitting, by the transceiver phase lock loop, the first wire rate clock signal to the serializer.

[0166] In embodiments, a phase lock loop generates the first wire rate clock signal.

[0167] In embodiments, the phase lock loop is on the field programmable gate array.

[0168] In embodiments, the phase lock loop that is part of the field programmable gate array system and not part of the field programmable gate array.

[0169] In embodiments, the step of generating the first wire rate clock signal further includes: (a) processing the second clock signal; (b) providing the first wire rate clock signal based on the processing of the second clock signal; and (c) transmitting, to the serializer, the first wire rate clock signal.

[0170] In embodiments, the sixth frequency corresponds to the third frequency.

[0171] In embodiments, the sixth phase is not aligned with the third phase.

[0172] The present invention also relates to a field programmable gate array system comprising (a) a field programmable gate array comprising (1) a first interface comprising (A) a first reference clock pin, wherein said first reference clock pin is configured to receive a first clock signal having a first frequency and a first phase; (B) a second reference clock pin, wherein said second reference clock pin is configured to receive the first clock signal; (C) a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream; (D) a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream; (2) a deserializer operationally connected to (A) the first reference clock pin to receive as a first input the first clock signal and (B) the first plurality of data pins to receive as a second input the first serial data stream, and wherein the deserializer is

configured to (A) convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams; (B) generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase; and (C) transmit the first plurality of parallel data streams and the first receiver side clock signal within the field programmable gate array; (3) computational circuitry operationally connected to the deserializer to receive the first plurality of parallel data streams and the first receiver side clock signal, wherein the computational circuitry is configured to perform a first set of operations on the first plurality of parallel data streams to generate a second plurality of parallel processed data streams having a second amount of data streams; (4) a serializer operationally connected to (A) an adjustable transceiver phase lock loop to receive as a third input a first wire rate clock signal, wherein the first wire rate clock signal has a fourth frequency and a fourth phase; (B) the second plurality of data pins to transmit as a first output the second serial data stream; (C) the computational circuity, wherein the serializer receives the second plurality of parallel processed data streams from the computational circuity and the serializer transmits to the computational circuitry a first transmitter side clock signal including a fifth frequency and a fifth phase; and wherein the serializer is configured to (A) convert the second plurality of parallel processed data streams into the second serial data stream; (B) generate the first transmitter side clock signal based on the first wire rate signal, wherein the first transmitter side clock signal has the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency; and (C) transmit the second serial data stream to the second plurality of data pins for transmission off the field programmable gate array; and (b) a phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises (1) a phase detector configured to compare the third phase of the first receiver side clock signal to the fifth phase of the transmitter side clock signal and to generate a phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the fifth phase of the transmitter side clock signal; (2) a phase controller operationally connected to the phase detector and configured to receive the phase difference indicator signal, and wherein the phase controller is configured to determine adjustment information based on the phase difference indicator signal; and (3) the adjustable transceiver phase lock loop operationally connected to the phase controller and configured to receive the adjustment information as well as operationally connected to the second reference clock pin of the first interface of the field

programmable gate array, wherein the adjustable transceiver phase lock loop is configured to generate a second clock signal including the second frequency and the second phase based on the first clock signal received via the second reference clock pin and process the second clock signal based on the adjustment information received from the phase controller to generate the first wire rate clock signal, wherein the transmitter side clock signal and the first receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the fifth phase.

[0173] In embodiments, the third frequency corresponds to the first frequency.

[0174] In embodiments, the third phase is not aligned with the first phase.

[0175] In embodiments, the third frequency is different than the first frequency.

[0176] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

[0177] In embodiments, the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

[0178] In embodiments, the first amount of data streams is the same as the second amount of data streams.

[0179] In embodiments, the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

[0180] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

[0181] In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

[0182] In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0183] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.

[0184] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.

[0185] In embodiments, the fourth frequency is a rational multiple of the second frequency.

[0186] In embodiments, the phase difference indicator signal is a pulse signal.

[0187] In embodiments, adjustment information indicates at least one of the following: (A) a desired phase; (B) a desired frequency; (C) a change in phase; and (D) a change in frequency.

[0188] In embodiments, adjustment information comprises a voltage.

[0189] In embodiments, adjustment information comprises a digital transmission.

[0190] In embodiments, the adjustment information is used to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay.

[0191] In embodiments, the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.

[0192] In embodiments, the first serial data stream includes market data and the second serial data stream includes trading data.

[0193] In embodiments, the field programmable gate array system further comprises (5) a second interface comprising (A) a first clock output pin configured to transmit the first receiver side clock signal, wherein the first clock output pin is operationally connected to the deserializer; and (B) a second clock output pin configured to transmit the first transmitter side clock signal, wherein the second clock output pin is operationally connected to the serializer, wherein the phase detector is not on the field programmable gate array and is operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array.

[0194] In embodiments, the field programmable gate array system further comprises (a) a fourth plurality of data pins of the first interface, wherein the fourth plurality of data pins is configured to transmit a fourth serial data stream; (b) a second deserializer operationally connected to: (i) the first reference clock pin to receive the first clock signal as a third input to the second

deserializer, wherein the second deserializer is configured to (A) receive a third serial data stream; (B) convert the third serial data stream into a third plurality of parallel data streams having a third amount of data streams; (C) generate a second receiver side clock signal based on the first clock signal, wherein the second receiver side clock signal has a sixth frequency and a sixth phase; and (D) transmit within the field programmable gate array to the computational circuitry the third plurality of parallel data streams and the second receiver side clock signal; (ii) the computational circuitry further configured to (A) receive the third plurality of parallel data streams and the second receiver side clock signal; and (B) generate a fourth plurality of parallel processed data streams having a fourth amount of data streams; (c) a second serializer operationally connected to: (i) the adjustable transceiver phase lock loop to receive as a fifth input the first wire rate clock signal based on the second clock signal; and (ii) the fourth plurality of data pins to transmit as a second output the fourth serial data stream, wherein the second serializer is configured to (A) receive the fourth plurality of parallel processed data streams from the computational circuity; (B) convert the fourth plurality of parallel processed data streams into the fourth serial data stream; (C) transmit the fourth serial data stream to the fourth plurality of data pins for transmission off the field programmable gate array; and (d) a second phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises (i) a second phase detector configured to (A) compare the third phase of the first receiver side clock signal to the sixth phase of the second receiver side clock signal; and (B) generate a second phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the sixth phase of the second receiver side clock signal; (ii) a second phase controller operationally connected to the second phase detector and configured to receive the second phase difference indicator signal, wherein the second phase controller is configured to determine second adjustment information based on the second phase difference indicator signal; and (iii) a delay element operationally connected to the second phase controller and to the second deserializer, wherein the second phase controller sends to the delay element the second adjustment information, wherein the delay element is configured to (A) delay the third serial data stream based on the second adjustment information, and (B) transmit the third serial data stream to the second deserializer, wherein the first receiver side clock signal and the second receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the sixth phase.

[0195] In embodiments, the field programmable gate array system further comprises a third plurality of data pins of the first interface, wherein the delay element is placed on the field programmable gate array and operationally connected to the third plurality of data pins and wherein the delay element is further configured to (A) receive the third serial data stream via the third plurality of data pins, and (B) transmit the third serial data stream to the second deserializer.

[0196] In embodiments, the field programmable gate array system further comprises a third plurality of data pins of the first interface, wherein (A) the delay element is placed outside of the field programmable gate array, (B) the delay element and the second deserializer are operationally connected to the third plurality of data pins, and (C) the third plurality of data pins is further configured to transmit the third serial data stream from the delay element to the second deserializer.

[0197] In embodiments, the field programmable gate array system further comprises (A) a first clock output pin of a second interface of the field programmable gate array, the first clock output pin being configured to transmit the first receiver side clock signal from the deserializer to the second phase detector; and (B) a third clock output pin of the second interface configured to transmit the second receiver side clock signal from the second deserializer to the second phase detector, wherein the second phase detector is not placed on the field programmable gate array and is operationally connected to the first clock output pin and the third clock output pin of the second interface of the field programmable gate array.

[0198] The present invention also relates to a method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of (a) receiving, by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream; (b) receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase; (c) transmitting, from the first plurality of data pins of the first interface to a deserializer in the field programmable gate array, the first serial data stream; (d) transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal; (e) generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal; (f) converting, by the deserializer, the first serial data stream into a

first plurality of parallel data streams; (g) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal; (h) transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams; (i) transmitting, from the deserializer to a phase detector of the field programmable gate array system, the first receiver side clock signal; (j) generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level: (i) receiving, by an adjustable transceiver phase lock loop via a second reference clock pin in the first interface, the first clock signal to generate a second clock signal having a fourth frequency and a fourth phase; (ii) generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal and interim adjustment information; (iii) generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase; (iv) transmitting, from the serializer to the phase detector, the interim transmitter side clock signal; (v) generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal; (vi) transmitting, from the phase detector to a phase controller of the field programmable gate array system which is placed within the field programmable gate array, the first output; (vii) determining, by the phase controller, the interim adjustment information based on the first output; and (viii) transmitting, from the phase controller to the adjustable transceiver phase lock loop, the interim adjustment information, wherein, the adjustable transceiver phase lock loop adjusts the second clock signal based on the interim adjustment information and steps (i) through (viii) are repeated until the first output of the phase detector is below the first threshold level; (k) transmitting, from the serializer to the computational circuitry, first transmitter side clock signal; (l) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams; (m) transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams; (n) converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and (o) transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface, the second serial data stream.

[0199] In embodiments, step (a) is performed before step (b).

[0200] In embodiments, step (b) is performed before step (a).

[0201] In embodiments, step (a) and step (b) are performed contemporaneously.

[0202] In embodiments, step (c) is performed before step (d).

[0203] In embodiments, step (d) is performed before step (c).

[0204] In embodiments, step (c) and step (d) are performed contemporaneously.

[0205] In embodiments, step (e) is performed before step (f).

[0206] In embodiments, step (f) is performed before step (e).

[0207] In embodiments, step (e) and step (f) are performed contemporaneously.

[0208] In embodiments, the second frequency corresponds to the first frequency.

[0209] In embodiments, the second phase is not aligned with the first phase.

[0210] In embodiments, the second frequency is different from the first frequency.

[0211] In embodiments, step (g) is performed before step (h).

[0212] In embodiments, step (h) is performed before step (g).

[0213] In embodiments, step (g) and step (h) are performed contemporaneously.

[0214] In embodiments, the phase detector is not placed on the field programmable gate array and the step (i) comprises transmitting, from the deserializer to the phase detector via a first clock pin on a second interface of the field programmable gate array, the first receiver side clock signal.

[0215] In embodiments, the step (i) further comprises transmitting, from the deserializer to the phase detector, the first receiver side clock signal via a first zero delay buffer phase lock loop of the field programmable gate array before transmitting the first receiver side clock signal via the first clock output pin of the second interface.

[0216] In embodiments, the third frequency corresponds to the second frequency.

[0217] In embodiments, the third phase is aligned with the second phase.

[0218] In embodiments, a difference between the third phase and the second phase is less than a second threshold level

[0219] In embodiments, the sixth frequency corresponds to the third frequency.

[0220] In embodiments, the sixth phase is not aligned with the third phase prior to the first output of the phase detector being below the first threshold level.

[0221] In embodiments, the phase detector is not placed on the field programmable gate array and the step (j)(iv) comprises transmitting, from the serializer to the phase detector via a second clock output pin of the second interface of the field programmable gate array, the interim transmitter side clock signal.

[0222] In embodiments, the step (j)(iv) further comprises transmitting, from the serializer to the phase detector, the interim transmitter side clock signal via a second zero delay buffer phase lock loop of the field programmable gate array before transmitting the interim transmitter side clock signal via the second clock output pin of the second interface.

[0223] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

[0224] In embodiments, the first amount of data streams is the same as the second amount of data streams.

[0225] In embodiments, the first amount of data streams and the second amount of data streams is one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

[0226] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

[0227] In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

[0228] In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0229] In embodiments, at least a portion of the first set of operations is performed prior to step (k).

[0230] In embodiments, at least a portion of the first set of operations is performed after step (k).

[0231] In embodiments, all of the first set of operations is performed after step (k).

[0232] In embodiments, the transmission of the second serial data stream from the serializer off the field programmable gate array is transmitted to an input/output module off the field programmable gate array.

[0233] In embodiments, the first serial data stream includes market data and the second serial data stream includes trading data.

[0234] In embodiments, the step of generating the first wire rate clock signal further includes: (a) generating, by the adjustable phase lock loop, the second clock signal based on the received first clock signal; (b) processing, by the adjustable transceiver phase lock loop, the second clock signal based on the interim adjustment information received from the phase controller; (c) providing, by the adjustable transceiver phase lock loop, the first wire rate clock signal based on the processing of the second clock signal; and (d) transmitting, by the adjustable transceiver phase lock loop, the first wire rate clock signal to the serializer.

[0235] In embodiments, a phase lock loop generates the first wire rate clock signal.

[0236] In embodiments, the phase lock loop is on the field programmable gate array.

[0237] In embodiments, the phase lock loop that is part of the field programmable gate array system and not part of the field programmable gate array.

[0238] In embodiments, the step of generating the first wire rate clock signal further includes: (a) processing the second clock signal; (b) providing the first wire rate clock signal based on the processing of the second clock signal; and (c) transmitting, to the serializer, the first wire rate clock signal.

[0239] In embodiments, the sixth frequency corresponds to the third frequency.

[0240] In embodiments, the sixth phase is not aligned with the third phase.

BRIEF DESCRIPTION OF THE DRAWINGS

[0241] Exemplary embodiments of the present invention will be described with reference to the accompanying figures, wherein:

[0242] FIG. 1 is a block diagram of a conventional field programmable gate array;

[0243] FIG. 1A is a block diagram of an exemplary transceiver suitable for use in the field programmable gate array of FIG. 1;

[0244] FIG. 1B is an exemplary block diagram of a Clock Domain Crossing Circuit suitable for use in the field programmable gate array of FIG. 1;

[0245] FIG. 1C illustrates exemplary input output waveforms of the Clock Domain Crossing Circuit of the field programmable gate array of FIG. 1;

[0246] FIG. 2A illustrates an example of a phase difference between the receiver side clock and the transmitter side clock of an FPGA in accordance with an exemplary embodiment of the present invention;

[0247] FIG. 2B illustrates an example of a phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an exemplary embodiment of the present invention;

[0248] FIG. 2C illustrates an example of a phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an exemplary embodiment of the present invention;

[0249] FIG. 2D illustrates an example of an inverted phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an exemplary embodiment of the present invention;

[0250] FIG. 3A is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0251] FIG. 3B is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0252] FIG. 3C is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0253] FIG. 3D is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0254] FIG. 3E is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0255] FIG. 3F is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0256] FIG. 4A is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0257] FIG. 4B is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0258] FIG. 4C is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0259] FIG. 5A is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0260] FIG. 5B is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0261] FIG. 5C is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0262] FIG. 5D is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0263] FIG. 5E is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0264] FIG. 5F is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0265] FIG. 6A is an exemplary block diagram of a deserializer suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0266] FIG. 6B is an exemplary circuit diagram of a continuous-time linear equalizer (CTLE) suitable for use in the deserializer of FIG. 6A in accordance with an exemplary embodiment of the present invention;

[0267] FIG. 6C is an exemplary block diagram of a clock and data recovery (CDR) circuit suitable for use in the deserializer of FIG. 6A in accordance with an exemplary embodiment of the present invention;

[0268] FIG. 6D is an exemplary circuit diagram of a decision circuit suitable for use in the deserializer of FIG. 6A in accordance with an embodiment of the present invention;

[0269] FIG. 6E is an exemplary block diagram of a deserializer suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0270] FIG. 7A is an exemplary block diagram of a serializer suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0271] FIG. 7B is an exemplary block diagram of a serializer suitable for use in field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0272] FIG. 8A is an exemplary block diagram of a phase detector suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0273] FIG. 8B is another exemplary block diagram of a phase detector suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0274] FIG. 8C is another exemplary block diagram of a phase detector suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0275] FIG. 8D is another exemplary block diagram of a phase detector suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0276] FIGs 9A-C are flow charts of a process implementing the field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0277] FIGs. 10A-10B are flow charts of a process for generating a transmitter side clock signal in accordance with an exemplary embodiment of the present invention;

[0278] FIG. 11 is a flow chart of a process for generating a wire rate clock signal in accordance with an embodiment of the present invention;

[0279] FIGs 12A-C are flow charts of a process implementing the field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0280] FIGs. 13A-13B are flow charts of a process for generating a transmitter side clock signal in accordance with an exemplary embodiment of the present invention;

[0281] FIG. 14 is a flow chart of a process for generating a wire rate clock signal in accordance with an embodiment of the present invention;

[0282] FIGs 15A-C are flow charts of a process implementing the field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0283] FIGs. 16A-16B are flow charts of a process for generating a transmitter side clock signal in accordance with an exemplary embodiment of the present invention; and

[0284] FIG. 17 is a flow chart of a process for generating a wire rate clock signal in accordance with an exemplary embodiment of the present invention.

DETAILED DESCRIPTION

[0285] The present invention generally relates to a field programmable gate array system. In embodiments, the present invention generally relates to a field programmable gate array and an external or internal phase controller providing phase matching between a receiver clock and a transmitter clock used in the field programmable gate array.

[0286] FIG. 1 illustrates an exemplary schematic of a FPGA 100. Examples of currently available FPGAs include the XCVU3P-2FFVC1517E, Intel 1SG280LH3F55E3VG, Xilinx XCVU9P-2FLGA2104E the Vitrex® Ultrascale, the Vitrex® Ultrascale Plus, the Stratix® V, the

Stratix® 10, XILINX XC3042, the Intel EP4CE6E22C8LN and the Lattice ICE40LP384-SG32, to name a few.

[0287] In embodiments, FPGA 100 may include an FPGA Core 106 and a number of peripheral systems. In embodiments, the FPGA Core 106 includes 4 main components: logic elements, digital signal processor blocks ("DSP blocks"), clock distribution components, and memories, to name a few, and may generally be referred to as the FPGA core, or simply logic core, 106. In embodiments, the peripheral systems may include CPU cores, reconfiguration controllers, security features, hardened logic functions, FPGA transceiver banks 102, hardened high-speed interface accelerators (e.g., PCIe or 100 GbE controllers, to name a few), general-purpose I/O pins, memory interface controllers, larger memories, analog components (e.g., ADCs or DACs to name a few), and 3D-stacked memories (e.g., HBM), to name a few. The FPGA Transceiver banks 102 receive serial data to be processed from outside the FPGA and then transmit serial data out of the FBGA after being processed by internal circuitry of the FPGA 100. Some FPGA's may not include FPGA Transceiver banks.

[0288] In embodiments, data may be received by a receiver side of the transceiver banks 102 in the FPGA 100 at rates such as 10 or 25 Gbps, to name a few. In embodiments, rates may be between a range of 9-25 Gbps, 10-25 Gbps, 22-33 Gbps, 33-45 Gbps, 45-60 Gbps, 60-80Gbps, or 80-120 Gbps, to name a few. An exemplary transceiver (including deserializer 104' and serializer 110') suitable for use in FPGA 100 is shown in FIG. 1A. In embodiments, the input data may be received from I/O module 120. The input data may then be deserialized, using deserializer 104, for example, and parallelized into parallel data streams, such as 16-64 bits wide at $1/16^{th}$ to $1/64^{th}$ of the frequency of the incoming data stream, to name a few. In embodiments, FPGA transceivers may support parallel streams with widths of, for example, 8 bits, 10 bits, 16 bits, 20 bits, 32 bits, 40 bits, 64 bits, 80 bits, 128 bits, and 160 bits (with corresponding clock division), to name a few. In some FPGAs, a physical coding sublayer (PCS) may be used in the transceiver 102. In some FPGAs, the PCS of the transceiver 102 may be bypassed and so that the corresponding PCS functions may be done in the FPGA core 106. After deserialization, data is available for computation in the FPGA logic core 106 where computation is completed. In embodiments, the computation of the data may be computed by receive-side computation 110a of the FPGA core 106. Similarly, data may be computed by the transmit-side computation 110b.

[0289] In embodiments, a REFERENCE CLOCK signal is provided, by Oscillator or Clock Generator 122, to both the deserializer 104 and the serializer 110. The REFERENCE CLOCK signal is received by the serializer 110 via the transceiver PLL 108 (Phase-Locked Loop). The first receiver side clock signal RXCLOCK, however, is different in both frequency and phase from the REFERENCE CLOCK based on the deserialization process that occurs in the deserializer 104. Similarly, the transmitter clock signal TXCLOCK, while based on the REFERNCE CLOCK signal varies in frequency and phase based on processing that occurs in the serializer 110. As a result, the RXCLOCK signal and TXCLOCK signal will be out of phase. A known solution to this issue is the inclusion of the RX to TX clock domain crossing circuit 112. An exemplary Clock Domain Crossing circuit is suitable for use in FPGA 100 is shown as clock domain crossing circuit 112' in connection with FIG. 1B. As is noted above, the inclusion of the RX to TX clock domain crossing circuit 112 creates a technical problem, introducing an inherent delay in the FPGA 100, which is undesirable. The technical problem of an inherent delay is illustrated in FIG. 1C. FIG. 1C illustrates an example of a phase difference between the receiver side clock and the transmitter side clock of the conventional field programmable gate array of FIG. 1.

[0290] Thereafter, the data it transmitted out of the FPGA 100. After all computation (computation by receive-side computation 110a and/or transmit-side computation 110b) and clock domain crossing (by RX to TX clock domain crossing 112) is completed, the data goes back to the transmit side of the FPGA transceiver 102 to be serialized by the serializer 110 out on an output wire. The serializer 110 (e.g., the transmitter) typically runs off a fast clock generated (e.g., 10 Gbps, 25 Gbps, or a range from 10 Gbps to 25 Gbps, or a range from 1Gbps to 100 Gbps, to name a few) by the transceiver phase-locked loop 108 within the transceiver bank 102 from a reference clock signal received by oscillator or clock generator 122.

[0291] The receiver (deserializer 104) and transmitter (serializer 110) of the transceiver 102 operate on different clocks that are independently generated within the transceiver 102. The receiver clock domain is typically generated by a clock and data recovery (CDR) circuit from the incoming data stream. The transmitter clock is typically generated by the transceiver phase-locked loop 108. In conventional FPGAs, phase matching or synchronizing is provided using the clock domain crossing circuit 112 that adjusts the phases of the two clock domains. The clock domain crossing circuit 112 may be an asynchronous FIFO or an asynchronous gearbox, to name a few. In embodiments, domain crossing circuit 112 may be a mesochronous clock crossing circuit. In

embodiments, clock domain crossing circuit 112 may be instantiated within transceiver 102 of FPGA 100, although this structure has a higher latency cost than implementing it in logic fabric 106 of FPGA 100. As discussed above, a significant drawback of the clock domain crossing circuit 112 is that it adds latency related to the phase difference between the clocks plus the latency of the synchronizers used, and does not perform any computation, such that it slows the effective processing speed of FPGA 100.

[0292] FIGS. 2A-2D illustrate example phase differences between the receiver side clock and the transmitter side clock. It will be understood that other examples of phase differences may be present consistent with the teachings of this disclosure. Generally, when the clocks are aligned, the minimum and maximum delays may be used to determine the time available for the computation of data.

[0293] FIG. 2A illustrates an example of a phase difference between the receiver side clock and the transmitter side clock of an FPGA in accordance with an embodiment. FIG. 2A depicts a phase difference when the clocks are under 360 degrees apart. This embodiment results in minimum delay 2106A and maximum delay 2108A, for which data may be computed. The minimum delay 2106A is from the driving clock edge back to itself, as shown in FIG. 2A.

[0294] FIG. 2B illustrates an example of a phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an embodiment. The phase difference depicted in FIG. 2B shows a phase difference with medium delay 2106B and maximum delay 2108B. The example shown in FIG. 2B shows a minimum delay 2106B of 0. However, in practice, while designers may design for the phase difference in FIG. 2B, the phase difference may end up more similar to the phase differences of FIGS. 2A and/or 2C.

[0295] FIG. 2C illustrates an example of a phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an embodiment. FIG. 2C depicts a phase difference with the clocks are over 360 degrees apart. The time between minimum delay 2106C and maximum delay 2108C may allow for more data computations within the phase difference.

[0296] FIG. 2D illustrates an example of an inverted phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an embodiment. This example of an inverted phase difference between minimum delay 2106D and maximum delay 2108D shows that, even inverted, the phase difference would work similarly to the phase detectors of FIGs. 2A-2C.

[0297] FIG. 3A illustrates a block diagram of a field programmable gate array (FPGA) system in accordance with an embodiment of the present disclosure that provides phase control while minimizing latency. In embodiments, the system generally includes FPGA 3100 which preferably includes FPGA transceiver banks 3102. In embodiments, the FPGA transceiver banks 3102 includes deserializer 3104 on the receiver end of FPGA 3100, transceiver PLL 3108, and serializer 3110 on the transmitter end of FPGA 3100. Deserializer 3104 may be similar to the deserializer 3104' and deserializer 3104'' discussed below in connection with FIGS. 6A-6E, the descriptions of which applying herein. Serializer 3110 may be similar to serializer 3110' and serializer 3110'' discussed below in connection with FIGS. 7A and 7B respectively, the descriptions of which applying herein. In embodiments, deserializer 3104 receives a serial data stream from the I/O module 3120 and provides deserialized data to the FPGA core 3106. More specifically, the deserializer 3104 will provide parallel data streams to the FPGA core 3106 for processing. As illustrated, this parallel data is provided to the computational logic 3210 where processing and computation takes place. FIG. 3A illustrates computational logic 3210 as a single element with a receiver side and a transmitting side. In embodiments, the computational logic 3210 may be implemented as a plurality of logic elements. In embodiments, when all computation is complete, the resulting data may be provided to serializer 3110 and then transmitted out of FPGA 3100, preferably via I/O module 3120, for example. In embodiments, the I/O module may be a direct soldered cable, on-chip optics, or an on-board optical transceiver, to name a few. Additionally, the I/O module may be an SFP, a QSFP, a micro QSFP, or a QSFP-DD, to name a few.

[0298] In embodiments, the serializer 3110 and deserializer 3104 (SERDES) circuit(s) may contain two major sections: (1) an analog side whose purpose is signal cleaning, and (2) a digital side which turns the analog signal into bits and converts between parallel and serial data streams. In embodiments, the analog side may include a few different types of amplifiers to provide signal cleaning.

[0299] In embodiments, as shown in FIG. 3A, a PLL with phase adjustment 3300 may be located inside the FPGA 3100 fabric with adjustable feedback dividers, which in turn adjust the frequency of the PLL. Alternatively, the PLL with phase adjustment 3300 may comprise a phase adjuster on the output of the loop, which adjusts the phase of the PLL directly. In embodiments, the same description may apply to adjustable transceiver PLLs 3108 and 5108 respectively

shown in FIGs. 3B and 5B, but the differences are the location of the PLL inside the FPGA (e.g., within the FPGA core 3106 versus outside the FPGA core and within the FPGA transceiver banks 3102, 5102) and the operating frequency.

[0300] As illustrated in FIG. 3A, in embodiments, the first receiver side clock signal RXCLOCK is based on but has a different frequency and phase than the REFERENCE CLOCK signal provided by oscillator 3000 based on the operation of the deserializer 3104, as is discussed above with respect to the serializer 104. In embodiments, the transmitter side clock signal TXCLOCK provided from the serializer 3110 may be provided by transceiver phase locked loop 3108, which is provided inside FPGA 3100, and may be controlled by Phase Lock Loop (PLL) with Phase Adjustment 3300 of the FPGA core 3106. In this manner, the frequency or phase of the transmitter side clock signal TXCLOCK may be adjusted.

[0301] In embodiments, an internal phase controller 3202 is connected to the PLL with Phase Adjustment 3300 and provides control signals to allow for adjustment of the phase of at least the transmitter side clock signal TXCLOCK. The phase of the incoming data, in embodiments, may be adjusted by adjusting the data stream received by I/O module 3120. In embodiments, the internal phase controller 3202 provides control signals based on the phase difference between the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK. In embodiments, the phase difference may be determined using phase detector 3206

[0302] Using the configuration of FIG. 3A, the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK may be sufficiently aligned in phase such that there is no need for the clock domain crossing circuit discussed above, eliminating a technical problem. The technical solution to a technical problem, in embodiments, is shown in the system of FIG. 3A, which provides a wire or a logic path via the controller 3202 and PLL with phase adjustment 3300 to adjust the phase of the transmitter side clock TXCLOCK to correspond to that of the first receiver side clock signal RXCLOCK. Some delays may be introduced in the path including min_delay and max_delay constraints of the wire and components, however, such delays are insignificant compared to the larger delays that are necessarily present when an asynchronous clock domain crossing circuit is used.

[0303] In embodiments, with a phase difference between about 45° and 360°, the min_delay should be set at 0 and the max_delay should be set equal to the time between rising edges on the receive clock signal and transmit clock signal (as shown in FIGs. 2A and 2B). The difference between 45 ° and 360 ° approximates the minimum amount of time required to safely capture data. In embodiments, the formula for the time is as follows:

$$t_{min} = t_{setup} + t_{wire} + t_{clock\text{-}out} + \Delta t_{jitter} + t_{skew}$$

[0304] Referencing the above equation, t_{setup} is the setup time of a flip-flop (i.e., a latch) on FPGA 3100. The t_{wire} is the delay of the, for example, shortest wire (as compared to other wires on the FPGA) on FPGA 3100. In embodiments, the shortest wire is the shortest possible wire. In embodiments, $t_{clock\text{-}out}$ is the clock-to-output time of a flip-flop on the FPGA 3100. In embodiments, Δt_{jitter} is a safety factor for jitter on both clocks. Jitter, for example, is the deviation from true periodicity of a periodic signal from a reference clock. In embodiments, t_{skew} is the skew between clock paths to the two flip-flops on FPGA 3100.

[0305] In embodiments where there is a phase difference with the transmitter clock running less than 45° ahead of the receiver clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, the transmit clock signal may also sample on the opposite edge as the receiving clock signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0306] In embodiments, to avoid instability, the transceiver PLL 3108 preferably runs at the highest bandwidth available from the PLL on the FPGA, while the overall phase locking system including the phase detectors 3206, controller 3202 and PLL with Phase Adjustment 3300 run at a low bandwidth. In embodiments, the highest bandwidth available from the PLL on the FPGA may range between 100 kHz and 10 MHz. In such embodiments, the poles in the on-chip PLLs on the FPGA 3100 are prevented from affecting the gain or phase margin of the overall control loop which may be included in the controller 3202. In embodiments, any loop

filter order may be used in the controller 3202 as long as the bandwidth is low enough to avoid interaction of poles in the control system. In embodiments, a low bandwidth may be, for example, 100Hz- 40kHz, 400Hz and 4khz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. In embodiments, a second-order loop filter may be used in an effort to improve lock time and phase locking error. In embodiments a third-order filter may be used if the second-order filter is stable. In embodiments, a first-order filter is also an option when the second-order filter has stability problems. In embodiments, other order filters may be used, depending on the internal bandwidth of the FPGA 3100.

[0307] In embodiments, where the bandwidth of the controller 3202 is too low, the receiving clock and the transmitter clock may not track each other closely enough to consider them locked. In embodiment, such tracking issues may be solved by adjusting the min and max delay constraints appropriately to provide a cushion for the clocks being away from the expected phase. In embodiments, a PD (Phase Detector) control system may be provided after the loop filter to aid in resolving tracking issues. In embodiments, tracking issues may be addressed by adding some nonlinearity in the transfer function of the filter. Other solutions may also be possible.

[0308] In the embodiment of FIG. 3A, the controller 3202 utilizes a phase-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative (i.e., the derivative component will act against the loop filter, however, some references refer to this as being a positive direction) and less than 1 (so the path straight from the filter dominates). The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. The bandwidth of the standard PLL loop filter, in some embodiments, may range between 400Hz and 4kHz, 4kHz and 10kHz, 100Hz and 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0309] While similar to the embodiment shown in FIG. 3A, in FIG. 3B, an internal phase controller 3202 is directly connected and provides phase control signals to the adjustable transceiver PLL 3108, which is located in the FPGA transceiver banks 3102 and outside the FPGA core 3106. FIG. 3B illustrates a block diagram of an FPGA system in accordance with an embodiment of the present invention that provides phase control while minimizing latency wherein the FPGA 3100 has an acceptable phase-controlled adjustable transceiver PLL 3108. This embodiment uses the phase-controlled transceiver PLL directly to control the phase of TXCLOCK. An acceptable phase-control system must have adjustment gain capable of matching phase transients on the incoming data stream to within the timing margin (t_{min}), meaning that the following inequality must be able to be satisfied:

$$\int_0^\infty \left|\Delta t_{pk}(\omega)[1 - LF(\omega)]\right| d\omega \leq t_{min}$$

[0310] Where $\Delta t_{pk}(\omega)$ is the peak design jitter at that frequency and LF is the transfer function over frequency of the phase locking system consisting of the phase detector 3206, controller 3202, and adjustable transceiver PLL 3108. The transfer function of a phase locked loop relates linearly to the phase control gain at low frequencies, and is given by:

$$LF(\omega) = \frac{K_{APLL}K_{PD}T(\omega)/F(\omega)}{\omega^2 + K_{APLL}K_{PD}T(\omega)/F(\omega)}$$

where K_{APLL} is the phase control gain of adjustable PLL 3108, K_{PD} is the gain of the phase detector 3206, $T(\omega)$ is the transfer function of the PLL controller 3202, and $F(\omega)$ is the transfer function of the feedback network.

[0311] In embodiments, expected functions for $\Delta t_{pk}(\omega)$ may be specified within the protocol specifications for communication protocols used. For example, for 10 Gigabit Ethernet, this is specified in clause 52.8 of the IEEE 802.3 standard.

[0312] In embodiments, the system of FIG. 3B generally includes FPGA 3100 which preferably includes FPGA transceiver banks 3102. In embodiments, the FPGA transceiver banks 3102 includes deserializer 3104 on the receiver end of FPGA 3100, adjustable transceiver PLL 3108, and serializer 3110 on the transmitter end of FPGA 3100. Deserializer 3104 may be similar to the deserializer 3104' and deserializer 3104'' discussed below in connection with

FIGS. 6A-6E, the descriptions of which applying herein. Serializer 3110 may be similar to serializer 3110' and serializer 3110'' discussed below in connection with FIGS. 7A and 7B respectively, the descriptions of which applying herein. In embodiments, deserializer 3104 receives a serial data stream from the I/O module 3120 and provides deserialized data to the FPGA core 3106. More specifically, the deserializer 3104 will provide parallel data streams to the FPGA core 3106 for processing. As illustrated, this parallel data is provided to the computational logic 3210 where processing and computation takes place. FIG. 3B illustrates computational logic 3210 as a single element with a receiver side and a transmitting side. In embodiments, the computational logic 3210 may be implemented as a plurality of logic elements. In embodiments, when all computation is complete, the resulting data may be provided to serializer 3110 and then transmitted out of FPGA 3100, preferably via I/O module 3120, for example. In embodiments, the I/O module may be a direct soldered cable, on-chip optics, or an on-board optical transceiver, to name a few. Additionally, the I/O module may be an SFP, a QSFP, a micro QSFP, or a QSFP-DD, to name a few.

[0313] In embodiments, the serializer 3110 and deserializer 3104 (SERDES) circuit(s) may contain two major sections: (1) an analog side whose purpose is signal cleaning, and (2) a digital side which turns the analog signal into bits and converts between parallel and serial data streams. In embodiments, the analog side may include a few different types of amplifiers in order to provide signal cleaning.

[0314] In embodiments, as shown in FIG. 3B, an adjustable transceiver PLL 3108 may be located inside the FPGA 3100 fabric with adjustable feedback dividers, which in turn adjust the frequency of the PLL. Alternatively, the adjustable transceiver PLL 3108 may comprise a phase adjuster on the output of the loop, which adjusts the phase of the PLL directly. Unlike the PLL with phase adjustment 3300 in FIG. 3A, the adjustable transceiver PLL 3108 in FIG. 3B is located outside the FPGA core 3106 and within the FPGA transceiver banks 3102. The adjustable transceiver PLL 3108 in FIG. 3B may also differ from the PLL with phase adjustment 3300 in FIG. 3A in operating frequency.

[0315] As illustrated in FIG. 3B, in embodiments, the first receiver side clock signal RXCLOCK is based on, but has a different frequency and phase than, the REFERENCE CLOCK signal provided by oscillator 3000 based on the operation of the deserializer 3104, as is discussed

above with respect to the serializer 104. In embodiments, the transmitter side clock signal TXCLOCK provided from the serializer 3110 may be provided by adjustable transceiver phase locked loop 3108. In this manner, the frequency or phase of the transmitter side clock signal TXCLOCK may be adjusted.

[0316] In embodiments, an internal phase controller 3202 is connected to the phase adjustment interface of the phase-controlled transceiver PLL 3108 and provides control signals to allow for adjustment of the phase of at least the transmitter side clock signal TXCLOCK. In embodiments, the phase of the incoming data may be adjusted by adjusting the data stream received by I/O module 3120. In embodiments, the internal phase controller 3202 provides control signals based on the phase difference between the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK. In embodiments, the phase difference may be determined using phase detector 3206.

[0317] Using the configuration of FIG. 3B, the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK may be sufficiently aligned in phase such that there is no need for the clock domain crossing circuit discussed above, eliminating a technical problem. The technical solution to a technical problem, in embodiments, is shown in the system of FIG. 3B, which provides a wire or a logic path via the controller 3202 and adjustable transceiver PLL 3108 to adjust the phase of the transmitter side clock TXCLOCK to correspond to that of the first receiver side clock signal RXCLOCK. Some delays may be introduced in the path including min_delay and max_delay constraints of the wire and components. However, such delays are insignificant compared to the larger delays that are necessarily present when an asynchronous clock domain crossing circuit is used.

[0318] In embodiments, with a phase difference between about 45° and 360°, the min_delay should be set at 0 and the max_delay should be set equal to the time between rising edges on the receive clock signal and transmit clock signal (as shown in FIGs. 2A and 2B). The difference between 45° and 360° approximates the minimum amount of time required to safely capture data. In embodiments, the formula for the time is as follows:

$$t_{min} = t_{setup} + t_{wire} + t_{clock\text{-}out} + \Delta t_{jitter} + t_{skew}$$

[0319] Referencing the above equation, t_{setup} is the setup time of a flip-flop (i.e., a latch) on FPGA 3100. The t_{wire} is the delay of the, for example, shortest wire (as compared to other

wires on the FPGA) on FPGA 3100. In embodiments, the shortest wire is the shortest possible wire. In embodiments, $t_{clock\text{-}out}$ is the clock-to-output time of a flip-flop on the FPGA 3100. In embodiments, Δt_{jitter} is a safety factor for jitter on both clocks. Jitter, for example, is the deviation from true periodicity of a periodic signal from a reference clock. In embodiments, t_{skew} is the skew between clock paths to the two flip-flops on FPGA 3100.

[0320] In embodiments where there is a phase difference with the transmitter clock running less than 45° ahead of the receiver clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, the transmit clock signal may also sample on the opposite edge as the receiving clock signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0321] In the embodiment of FIG. 3B, to avoid instability, the internal PLL of the adjustable transceiver PLL 3108 preferably runs at the highest bandwidth available from the PLL on the FPGA, while the overall phase locking system including the phase detectors 3206 and controller 3202 runs at a low bandwidth. In embodiments, the highest bandwidth available from the PLL on the FPGA may range between 100 kHz and 10 MHz. In such embodiments, the poles in the adjustable transceiver PLL 3108 are prevented from affecting the gain or phase margin of the off-chip PLL which may be included in the controller 3202. In embodiments, any loop filter order may be used in the controller 3202 as long as the bandwidth is low enough to avoid interaction of poles in the control system. In embodiments, a low bandwidth may be, for example, 100Hz- 40kHz, 400Hz and 4khz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. In embodiments, a second-order loop filter may be used in an effort to improve lock time and phase locking error. In embodiments a third-order filter may be used if the second-order filter is stable. In embodiments, a first-order filter is also an option when the second-order filter has stability problems. In embodiments, other order filters may be used, depending on the internal bandwidth of the FPGA 3100.

[0322] In embodiments, where the bandwidth of the controller 3202 is too low, the receiving clock and the transmitter clock may not track each other closely enough to consider them locked. In embodiment, such tracking issues may be solved by adjusting the min and max delay constraints appropriately to provide a cushion for the clocks being away from the expected phase. In embodiments, a PD (Phase Detector) control system may be provided after the loop filter to aid in resolving tracking issues. In embodiments, tracking issues may be addressed by adding some nonlinearity in the transfer function of the filter. Other solutions may also be possible.

[0323] In the embodiment of FIG. 3B, the controller 3202 utilizes a phase-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative (i.e., the derivative component will act against the loop filter, however, some references refer to this as being a positive direction) and less than 1 (so the path straight from the filter dominates). The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. The bandwidth of the standard PLL loop filter, in some embodiments, may range between 400Hz and 4khz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0324] FIG. 3C illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. Like in the embodiment shown in FIG. 3A, a PLL with phase adjustment 3300a located within the FPGA core 3106 is used by the FPGA system in FIG. 3C. Unlike in the embodiment shown in FIG. 3A, however, an additional control loop, comprising a phase detector 3206b, a controller 3202b, and an external delay element 3300b, may be used to allow multiple deserializers 3104a, 3104b and serializers 3110a, 3110b to be aligned. Multiple deserializers and serializers, as opposed to one of each, allow FPGA 3100 to receive more input data and more output data. In such systems, for every additional receiver that needs to be phase-aligned, an additional control loop is required.

[0325] In embodiments, the additional control loop may use a similar method to the control loop for phase aligning a transmitter to the receiver. However, in embodiments, the control loop may use a delay element 3300b on the received data rather than adjusting the frequency or phase of an oscillator. The control loop may also include a deserializer 3104b in the feedback path instead of a transceiver PLL. In such embodiments, the required bandwidth may change or cause different types of nonlinearities. Otherwise, the method for phase-aligning additional receivers generally corresponds to the method used to phase align a transmitter and a receiver, as discussed.

[0326] In embodiments, the external delay element 3300b may have an adjustment range at least as wide as one period of the parallel RX clock. This can be accomplished by using a long delay line or a pair of smaller delay lines with a glitch-free switchover circuit to hide the boundary conditions of the delay lines. In embodiments, the delay element 3300b may be implemented with a digital delay line (e.g., the SY89295U from Micrel), or a voltage-controlled delay element (e.g., the HMC910 from Analog devices).

[0327] In embodiments, the additional controller 3202b utilizes a delay-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative, i.e., the derivative component will act against the loop filter (however, some references refer to this as being a "positive" direction) and less than 1 so that the path straight from the filter dominates. The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. In embodiments, the bandwidth of the standard PLL loop filter may range between 400Hz and 4kHz, 4kHz and 10kHz, 100Hz and 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0328] In the embodiment of FIG. 3C, there are three clocks which should be aligned, and the required timing constraints for passing data from one clock domain to another all follow the same pattern. In embodiments where there is a phase difference between any pair of aligned

clocks with one clock running less than 45 degrees ahead of the other clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, one of the clock signals may also sample on the opposite edge as the signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0329] FIG. 3D illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. Like in the embodiment shown in FIG. 3B, an adjustable transceiver PLL 3108 located within the FPGA transceiver banks 3102 is used by the FPGA system of FIG. 3D. Unlike in the embodiment shown in FIG. 3B, however, an additional control loop similar to the additional control loop in FIG. 3C is used to allow multiple deserializers 3104a, 3104b and serializers 3110a, 3110b to be aligned. In embodiments, the additional control loop may operate in the manner identical to the additional control loop described for FIG. 3C.

[0330] FIG. 3E illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. This embodiment is similar to the embodiment shown in FIG. 3C in almost all aspects, except that the delay element 3300b is internal to the FPGA 3100 in FIG. 3E, unlike the delay element 3300b located outside of the FPGA 3100 in FIG. 3C. In embodiments, the delay element 3300b in FIG. 3E has the same requirements as the external delay element shown in FIG. 3C.

[0331] FIG. 3F illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. This embodiment is similar to the embodiment shown in FIG. 3D in almost all aspects, except that the delay element 3300b is internal to the FPGA 3100 in FIG. 3F, unlike the delay elements 3300b located outside of the FPGA 3100 in FIG. 3D. The delay element 3300b has the same requirements as the external delay element shown in FIG. 3D.

[0332] FIG. 4A is a block diagram of another FPGA system in accordance with an exemplary embodiment of the present invention. The system of FIG. 4A is similar to that of FIG. 3A or 3B, and common components are referred to using the same reference numbers (with a differing first digit to indicate the Figure - e.g., if the first digit of a reference numeral is "3," the reference numeral is located on FIG. 3A or 3B) as in FIGs. 3A and 3B. One difference between the system of FIG. 4A and the system of FIGs. 3A and 3B is that the phase detector 4206 is off-chip, i.e., not of the FPGA 4100. Another difference between the system of FIG. 4A and the system of FIGs. 3A and 3B is that the FPGA 4100 includes zero-delay buffer PLLS 4208a, 4208b. Another difference between the system of FIG. 4A and the system of FIGs. 3A and 3B is that an internal phase controller 4202 is operationally connected to frequency or phase adjustable oscillator 4200, which is outside the FPGA 4100, such that a phase or frequency control signal may be transmitted from the internal phase controller 4202 to transceiver PLL 4108 via the frequency or phase-adjustable oscillator 4200.

[0333] Referring back to FIG. 4A, in embodiments, the system generally includes FPGA 4100 which preferably includes FPGA transceiver banks 4102. In embodiments, the FPGA transceiver banks 4102 includes deserializer 4104 on the receiver end of FPGA 4100, transceiver PLL 4108, and serializer 4110 on the transmitter end of FPGA 4100. Deserializer 4104 may be similar to the deserializer 3014' and deserializer 3104'' discussed below in connection with FIGS. 6A-6E, the descriptions of which applying herein. Serializer 4110 may be similar to serializer 3110' and serializer 3110'' discussed below in connection with FIGS. 7A and 7B respectively, the descriptions of which applying herein. In embodiments, deserializer 4104 receives a serial data stream via a first plurality of data pins of a first interface from the I/O module 4120 and provides deserialized data to the FPGA core 4106. More specifically, the deserializer 4104 will provide parallel data streams to the FPGA core 4106 for processing. As illustrated, this parallel data is provided to receiver side computational element 4210a where processing and computation takes place. The resulting data may then be provided to transmitting side computational element 4210b where additional computation and processing may take place. FIG. 4A illustrates computational logic 4210 as a single element. In embodiments, the computational logic 4210 may be implemented as a plurality of logic elements. In embodiments, computational logic 4210 may also include one or more of the following: RAM blocks or dedicated hardened accelerators. In embodiments, when all computation is complete, the resulting data may be

provided to serializer 4110 and then transmitted out of FPGA 4100, preferably via I/O module 4120, for example. In embodiments, the I/O module 4120 may be a direct soldered cable, on-chip optics, or an on-board optical transceiver, to name a few. I/O Module 4120, may be, for example, a Samtec® I/O Module Firefly® I/O Module, to name a few. Additionally, the I/O module may be designed to meet one or more of the following standards: SFP, a QSFP, a micro QSFP, or a QSFP-DD, to name a few.

[0334] In embodiments, FPGA 4100 may include one or more interfaces, such as pins. By way of example, a first interface of the one or more interfaces, may include a first plurality of pins of FPGA 4100. The first plurality of pins may be used to transmit and/or receive data and/or signals. In embodiments, the first plurality of pins may include a first reference clock pin. The first reference clock pin may be operationally connected to deserializer 4104. In embodiments, the first reference clock pin may also be operationally connected to fixed-frequency oscillator 4000 such that a first clock signal having a first phase and a first phase may be transmitted from fixed-frequency oscillator 4000 to deserializer 4104 via the first reference clock pin. In embodiments, the first clock signal may have a frequency between 50 and 800 MHZ.

[0335] In embodiments, the first plurality of pins may also include a second reference clock pin. The second reference clock pin may, in embodiments, be operationally connected to transceiver PLL 4108. The second reference clock pin, in embodiments, may be operationally connected to frequency or phase adjustable oscillator 4200 such that a second clock signal having a second phase and a second frequency may be transmitted from the frequency or phase-adjustable oscillator 4200 to transceiver PLL 4108 via the second reference clock pin. In embodiments, the second reference clock pin may be operationally connected to serializer 4110 such that the second clock signal may be transmitted from the frequency or phase-adjustable oscillator 4200 to serializer 4110 via the second reference clock pin. In embodiments, the second reference clock pin may also receive a first wire rate clock signal.

[0336] In embodiments, the first plurality of pins may also include a first plurality of data pins. The first plurality of data pins may be operationally connected deserializer 4104. In embodiments, the first plurality of data pins may also be operationally connected to I/O module 4120 such that a first serial data stream may be transmitted from external connection 4122

to deserializer via the I/O module 4120 and the first plurality of data pins. In embodiments, the first serial data stream may range between 10 to 25 GBPS.

[0337] In embodiments, the first plurality of pins may also include a second plurality of data pins. The second plurality of data pins may be operationally connected to serializer 4110. In embodiments, the second plurality of data pins may also be operationally connected to I/O module 4120 such that a second serial data stream may be transmitted from serializer 4110 to the external connection 4122 via the I/O module 4120 and the second plurality of data pins. In embodiments, the second serial data stream may range between 10 to 25 GBPS.

[0338] Although reference is made to separate first reference clock pin, second reference clock pin, first plurality of data pins and second plurality of data pins, in embodiments, each pin may be a fixed-function, fixed-location pin, connected internally through a wire. In embodiments, each pin may be a multiplexed fixed-function pin, connected internally through a multiplexer or crossbar. In embodiments, each pin may be a general purpose I/O pin connected through the FPGA core 4106. In embodiments, one or more pin may be fixed function, fixed location pines, while other pins may me multiplexed fixed function pins and/or a general purpose I/O pin.

[0339] In embodiments, the one or more interfaces may also include at least a second interface. The second interface of the one or more interfaces, may include a second plurality of pins of FPGA 4100. The second plurality of pins may be used to transmit and/or receive data and/or signals. In embodiments, the second plurality of pins may include a first clock output pin. The first clock output pin may be operationally connected to deserializer 4104. In embodiments, the first clock output pin may also be operationally connected to computation logic 4210 such that a first receiver side clock signal is transmitted from the deserializer 4104 to computation logic 4210 via the first clock output pin. Additionally, in some embodiments, the first clock output pin may also be operationally connected to zero-delay buffer PLL 4208a such that the receiver side clock is transmitted from the deserializer 4104 to the zero-delay buffer PLL 4208a via the first clock output pin. In embodiments the first receiver side clock signal may have a frequency ranging between 100-650 MHZ.

[0340] In embodiments, the second plurality of pins may also include a second clock output pin. The second clock output pin may be operationally connected to serializer 4110. In embodiments, the second clock output pin may also be operationally connected to computation

logic 4210 such that a transmitter side clock signal is transmitted from the serializer 4110 to computation logic 4210 via the second clock output pin. Additionally, in some embodiments, the second clock output pin may also be operationally connected to zero-delay buffer PLL 4208b such that the transmitter side clock is transmitted from the serializer 4110 to the zero-delay buffer PLL 4208b via the second clock output pin. In embodiments the transmitter side clock signal may have a frequency ranging between 100-650 MHZ.

[0341] In embodiments, the serializer 4110 and deserializer 4104 (SERDES) circuit(s) may contain two major sections: (a) an analog side whose purpose is signal cleaning, and (2) a digital side which turns the analog signal into bits and converts between parallel and serial data streams. In embodiments, the analog side may include a few different types of amplifiers in order to provide signal cleaning. In embodiments, the adjustable oscillator 4200 may be implemented in a variety of ways. In embodiments, the adjustable oscillator 4200 may be implemented as a voltage controlled oscillator. A voltage controller oscillator may be implemented using a variety of architectures. In embodiments, other types of oscillators may be used including negative-resistance oscillators, Clapp oscillators, Colpitts oscillators, ring oscillators, and varactor-tuned oscillators, to name a few.

[0342] In embodiments, a voltage controller crystal oscillator may be used as the adjustable oscillator 4200, for example, the Si550 from Silicon Labs. In embodiments, a numerically/digitally-controlled oscillator may be used as the adjustable oscillator 4200, which is a digital version of an analog VCO, and may use switched circuit elements or a fixed frequency oscillator and a digital PLL to adjust the frequency.

[0343] In embodiments, the adjustable oscillator 4200 may be implemented with a digital delay line, e.g., the SY89295U from Micrel.

[0344] In embodiments, the adjustable oscillator 4200 may be implemented as a voltage-controlled delay element, e.g., the HMC910 provided by Analog devices.

[0345] As illustrated in FIG. 4A, in embodiments, the first receiver side clock signal RXCLOCK is based on but has a different frequency and phase than the REFERENCE CLOCK signal provided by oscillator 4200 based on the operation of the deserializer 4104, as is discussed above with respect to the serializer 4110. In embodiments, the transmitter side clock signal TXCLOCK provided from the deserializer 4104 may be provided by transceiver phase locked loop

4108, which is provided inside FPGA 4100, and may be controlled by frequency or phase adjustable oscillator 4200, external to FPGA 4100. In this manner, the frequency or phase of the transmitter side clock signal TXCLOCK may be adjusted.

[0346] In embodiments, an internal phase controller 4202 is connected to the frequency or phase adjustable oscillator 4200 and provides control signals to allow for adjustment of the phase of at least the transmitter side clock signal TXCLOCK. The phase of the incoming data, in embodiments, may be adjusted by adjusting the data stream received by I/O module 4120. In embodiments, the internal phase controller 4202 provides control signals based on the phase difference between the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK. In embodiments, the phase difference may be determined using phase detector 4206 and zero-delay buffers, 4208a, 4208b. In embodiments, the zero-delay buffers 4208a, 4208b may be incorporated into the FPGA core 4106 of the FPGA 4100. In embodiments, FPGA core 4106 may not include the zero-delay buffers 4208a, 4208b. In embodiments, zero-delay buffer 4208a may have a reference trace T1 whose length is matched to a length of wire T3 between the I/O pin of FPGA 4100 and external phase detector 4206. Similarly, zero delay buffer 4208b may have a reference trace T2 whose length is matched to a second length of wire T4 between the I/O pin of the FPGA 4100 and the external phase detector 4206. Any length mismatch between reference traces T1 and wire T3 between the I/O pin of the FPGA 4100 and the external phase detector 4206 may introduce a deterministic phase error proportional to the mismatch of the length of the wires. Any length mismatch between reference traces T2 and wire T4 between the I/O pin of the FPGA 4100 and the external phase detector 4206 may introduce a deterministic phase error proportional to the mismatch of the length of the wires.

[0347] In embodiments, the transceiver PLL 4108 may include a second adjustable oscillator. In embodiments, the second adjustable oscillator of the transceiver PLL 4108 may provide the wire rate signal to the serializer 4110 which may be used to provide the transmitter clock signal TX CLOCK. In embodiments, the adjustable oscillator of the transceiver PLL 4108 may be provided outside of the transceiver PLL 4108 and operatively connected to the serializer 4110. In embodiments, where a second adjustable oscillator is provided in the FPGA 4100, the adjustable oscillator 4200 may not be necessary and the output of the controller 4202 may be provided to and used by the second adjustable oscillator to adjust the first wire rate clock signal W.R. CLOCK provided to the serializer 4110 based on the information from the controller. In

embodiments, where the second adjustable oscillator is provided on the FPGA 4100 and the adjustable oscillator 4200 is also provided off the FPGA, the delay of the second adjustable oscillator may be set to a constant value and the controller 4202 may provide instructions to the second adjustable oscillator based on this constant value. In embodiments, the constant value may be zero.

[0348] Using the configuration of FIG. 4A, the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK are sufficiently aligned in phase such that there is no need for the clock domain crossing circuit discussed above, eliminating a technical problem. The technical solution to a technical problem, in embodiments, is shown in the system of FIG. 4A, which provides a wire or a logic path via the controller 4202 and adjustable oscillator 4200 to adjust the phase of the transmitter side clock TMCLOCK to correspond to that of the first receiver side clock signal RXCLOCK. Some delays may be introduced in the path including min_delay and max_delay constraints of the wire and components, however, such delays are insignificant compared to the larger delays that are necessarily present when an asynchronous clock domain crossing circuit is used.

[0349] In embodiments, zero delay buffers 4208a, 4208b may be configured to add a phase offset such that the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK may be provided with any desired fixed phase offset with respect to each other. In such embodiments, any phase difference may be used, depending on the length of the logic path between the clocks and the corresponding delay constraints. In embodiments, with a phase difference between about 45° and 360°, the min_delay should be set at 0 and the max_delay should be set equal to the time between rising edges on the receive clock signal and transmit clock signal (as shown in FIGs. 2A and 2B). The difference between 45° and 360° approximates the minimum amount of time required to safely capture data. In embodiments, the formula for the time is as follows:

$$t_{min} = t_{setup} + t_{wire} + t_{clock\text{-}out} + \Delta t_{jitter} + t_{skew}$$

[0350] Referencing the above equation, t_{setup} is the setup time of a flip-flop (i.e., a latch) on FPGA 4100. The t_{wire} is the delay of the, for example, shortest wire (as compared to other wires on the FPGA) on FPGA 4100. In embodiments, the shortest wire is the shortest possible wire. In embodiments, $t_{clock\text{-}out}$ is the clock-to-output time of a flip-flop on the FPGA 4100. In

embodiments, Δt_{jitter} is a safety factor for jitter on both clocks. Jitter, for example, is the deviation from true periodicity of a periodic signal from a reference clock. In embodiments, t_{skew} is the skew between clock paths to the two flip-flops on FPGA 4100.

[0351] In embodiments where there is a phase difference with the transmitter clock running less than 45 degrees ahead of the receiver clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, the transmit clock signal may also sample on the opposite edge as the receiving clock signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0352] In embodiments, to avoid instability, both the transceiver PLL 4108 and the zero-delay buffer PLL 4208b preferably run at the highest bandwidth available, while the overall phase locking system including the phase detectors 4206, controller 4202 and oscillator 4200 runs at a low bandwidth. In such embodiments, the poles in the on-chip PLLs on the FPGA 4100 are prevented from affecting the gain or phase margin of the off-chip PLL which may be included in the controller 4202. In embodiments, any loop filter order may be used in the controller 4202 as long as the bandwidth is low enough to avoid interaction of poles in the control system. In embodiments, a low bandwidth may be, for example, 100Hz- 40kHz, 400Hz and 4khz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. In embodiments, a second-order loop filter may be used in an effort to improve lock time and phaselocking error. In embodiments a third-order filter may be used if the second-order filter is stable. In embodiments, a first-order filter is also an option when the second-order filter has stability problems. In embodiments, other order filters may be used, depending on the internal bandwidth of the FPGA 4100.

[0353] In embodiments, where the bandwidth of the controller 4202 is too low, the receiving clock and the transmitter clock may not track each other closely enough to consider them locked. In embodiment, such tracking issues may be solved by adjusting the min and max delay constraints appropriately to provide a cushion for the clocks being away from the expected phase. In embodiments, a PD control system may be provided after the loop filter to aid in resolving

tracking issues. In embodiments, tracking issues may be addressed by adding some nonlinearity in the transfer function of the filter. Other solutions may also be possible.

[0354] In the embodiment of FIG. 4A, the controller 4202 utilizes a phase-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative (i.e., the derivative component will act against the loop filter, however, some references refer to this as being a positive direction) and less than 1 (so the path straight from the filter dominates). The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. The bandwidth of the standard PLL loop filter, in some embodiments, may range between 400Hz and 4khz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0355] FIG. 4B illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. Like the embodiment shown in FIG. 4A, the embodiment of FIG. 4B uses a frequency or phase adjustable oscillator 4200a located outside the FPGA 4100. Unlike in the embodiment shown in FIG. 4A, an additional control loop, comprising a phase detector 4206b, a controller 4202b, and an external delay element 4200b, is used in the embodiment of FIG. 4B to allow multiple deserializers 4104a, 4104b and serializers 4110a, 4110b to be aligned. For every additional receiver that needs to be phase-aligned, an additional control loop is required.

[0356] In embodiments, the external delay element 4200b may have an adjustment range at least as wide as one period of the parallel RX clock. This can be accomplished by using a long delay line or a pair of smaller delay lines with a glitch-free switchover circuit to hide the boundary conditions of the delay lines. In embodiments, the delay element 4200b may be implemented with a digital delay line (e.g., the SY89295U from Micrel), or a voltage-controlled delay element (e.g., the HMC910 from Analog devices).

[0357] In embodiments, the additional controller 4202b utilizes a delay-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative, i.e., the derivative component will act against the loop filter (noting, however, that some references refer to this as being a "positive" direction) and less than 1 so that the path straight from the filter dominates. The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. The bandwidth of the standard PLL loop filter, in some embodiments, may range between 400Hz and 4kHz, 4kHz and 10kHz, 100Hz and 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0358] In the embodiment of FIG. 4B, there may be three clocks which should be aligned, and the required timing constraints for passing data from one clock domain to another all follow the same pattern. In embodiments where there is a phase difference between any pair of aligned clocks with one clock running less than 45 degrees ahead of the other clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, one of the clock signals may also sample on the opposite edge as the signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0359] Similar to the system described in connection with FIG. 4A, the system of FIG. 4B may or may not include zero delay buffers 4208a, 4208b, and 4208c. In embodiments, zero-delay buffer 4208a may have a reference trace T1 whose length is matched to a length of wire T4 between the I/O pin of FPGA 4100 and external phase detectors 4206a, 4206b. Similarly, zero delay buffer 4208b may have a reference trace T2 whose length is matched to a second length of wire T5 between the I/O pin of the FPGA 4100 and the external phase detector 4206a. Also, similarly,

zero delay buffer 4208c may have a reference trace T3 whose length is matched to a second length of wire T6 between the I/O pin of the FPGA 4100 and the external phase detector 4206b. Any length mismatch between reference traces T1 and wire T4 between the I/O pin of the FPGA 4100 and the external phase detectors 4206a, 4206b may introduce a deterministic phase error proportional to the mismatch of the length of the wires. Any length mismatch between reference traces T2 and wire T5 between the I/O pin of the FPGA 4100 and the external phase detector 4206a may introduce a deterministic phase error proportional to the mismatch of the length of the wires. Any length mismatch between reference traces T3 and wire T6 between the I/O pin of the FPGA 4100 and the external phase detector 4206b may introduce a deterministic phase error proportional to the mismatch of the length of the wires.

[0360] FIG. 4C illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. This embodiment is similar to the embodiment shown in FIG. 4B in almost all aspects, except that the delay element 4200b is internal to the FPGA 4200b, unlike the delay element 4200b located outside of the FPGA 4100 in FIG. 4B. In embodiments, the delay element 4200b in FIG. 4C has the same requirements as the external delay element shown in FIG. 4B.

[0361] FIG 5A is a block diagram of another FPGA system in accordance with an exemplary embodiment of the present invention. The system of FIG. 5A is similar to that of FIG. 4A, and common components are referred to using the same reference numbers (with a differing first digit to indicate the Figure - e.g., if the first digit of a reference numeral is "4," the reference numeral is located on FIG. 4A) as in FIG. 4A. Like in the system of FIG. 4A, the phase detector 5206 is off-chip, i.e., not of the FPGA 5100, and the FPGA 5100 also includes zero-delay buffer PLLS 5208a, 5208b. On the other hand, the system of FIG. 5A is different from the system of FIG. 4A in that an internal phase controller 5202 is operationally connected to the PLL with phase adjustment 5300 located within the FPGA core 5106, through which the internal phase controller provides phase control to the transceiver PLL 5108.

[0362] FIG. 5A illustrates a block diagram of an FPGA system in accordance with an exemplary embodiment of the present disclosure that provides phase control while minimizing latency. In embodiments, the system generally includes FPGA 5100 which preferably includes FPGA transceiver banks 5102. In embodiments, the FPGA transceiver banks 5102 includes

deserializer 5104 on the receiver end of FPGA 5100, transceiver PLL 5108, and serializer 5110 on the transmitter end of FPGA 5100. Deserializer 5104 may be similar to the deserializer 3104' and deserializer 3104'' discussed below in connection with FIGS. 6A-6E, the descriptions of which applying herein. Serializer 5110 may be similar to serializer 3110' and serializer 3110'' discussed below in connection with FIGS. 7A and 7B respectively, the descriptions of which applying herein. In embodiments, deserializer 5104 receives a serial data stream from the I/O module 5120 and provides deserialized data to the FPGA core 5106. More specifically, the deserializer 5104 will provide parallel data streams to the FPGA core 5106 for processing. As illustrated, this parallel data is provided to the computational logic 5210 where processing and computation takes place. FIG. 5A illustrates computational logic 5210 as a single element with a receiver side and a transmitting side. In embodiments, the computational logic 5210 may be implemented as a plurality of logic elements. In embodiments, when all computation is complete, the resulting data may be provided to serializer 5110 and then transmitted out of FPGA 5100, preferably via I/O module 5120, for example. In embodiments, the I/O module may be a direct soldered cable, on-chip optics, or an on-board optical transceiver, to name a few. Additionally, the I/O module may be an SFP, a QSFP, a micro QSFP, or a QSFP-DD, to name a few.

[0363] In embodiments, the serializer 5110 and deserializer 5104 (SERDES) circuit(s) may contain two major sections: (1) an analog side whose purpose is signal cleaning, and (2) a digital side which turns the analog signal into bits and converts between parallel and serial data streams. In embodiments, the analog side may include a few different types of amplifiers in order to provide signal cleaning.

[0364] In embodiments, as shown in FIG. 5A, a PLL with phase adjustment 5300 may be located inside the FPGA 5100 fabric with adjustable feedback dividers, which in turn adjust the frequency of the PLL. Alternatively, the PLL with phase adjustment 5300 may comprise a phase adjuster on the output of the loop, which adjusts the phase of the PLL directly. In embodiments, the same description may apply to adjustable transceiver PLLs 3108 and 5108 respectively shown in FIGs. 3B and 5B, but the differences are the location of the PLL inside the FPGA (e.g., within the FPGA core 5106 versus outside the FPGA core and within the FPGA transceiver banks 3102, 5102) and the operating frequency.

[0365] As illustrated in FIG. 5A, in embodiments, the first receiver side clock signal RXCLOCK is based on but has a different frequency and phase than the REFERENCE CLOCK signal provided by oscillator 5000 based on the operation of the deserializer 5104, as is discussed above with respect to the serializer 104. In embodiments, the transmitter side clock signal TXCLOCK provided from the serializer 5110 may be provided by transceiver phase locked loop 5108, which is provided inside FPGA 5100, and may be controlled by PLL with Phase Adjustment 5300 of the FPGA core 5106. In this manner, the frequency or phase of the transmitter side clock signal TXCLOCK may be adjusted.

[0366] As illustrated in FIG. 5A, in embodiments, the first receiver side clock signal RXCLOCK is based on but has a different frequency and phase than the REFERENCE CLOCK signal provided by oscillator 5000 based on the operation of the deserializer 5104, as is discussed above with respect to the serializer 104. In embodiments, the transmitter side clock signal TXCLOCK provided from the serializer 5110 may be provided by transceiver phase locked loop 5108, which is provided inside FPGA 5100, and may be controlled by a PLL with Phase Adjustment 5300 of the FPGA core 5106. In this manner, the frequency or phase of the transmitter side clock signal TXCLOCK may be adjusted.

[0367] In embodiments, an internal phase controller 5202 is connected to the PLL with Phase Adjustment 5300 and provides control signals to allow for adjustment of the phase of at least the transmitter side clock signal TXCLOCK. In embodiments, the phase of the incoming data may be adjusted by adjusting the data stream received by I/O module 5120. In embodiments, the phase difference may be determined using phase detector 5206 which is external to the FPGA. In embodiments, with a phase difference between about 45° and 360°, the min_delay should be set at 0 and the max_delay should be set equal to the time between rising edges on the receive clock signal and transmit clock signal (as shown in FIGs. 2A and 2B). The difference between 45° and 360° approximates the minimum amount of time required to safely capture data. In embodiments, the formula for the time is as follows:

$$t_{min} = t_{setup} + t_{wire} + t_{clock\text{-}out} + \Delta t_{jitter} + t_{skew}$$

[0368] Referencing the above equation, t_{setup} is the setup time of a flip-flop (i.e., a latch) on FPGA 3100. The t_{wire} is the delay of the, for example, shortest wire (as compared to other wires on the FPGA) on FPGA 3100. In embodiments, the shortest wire is the shortest possible

wire. In embodiments, $t_{clock\text{-}out}$ is the clock-to-output time of a flip-flop on the FPGA 3100. In embodiments, Δt_{jitter} is a safety factor for jitter on both clocks. Jitter, for example, is the deviation from true periodicity of a periodic signal from a reference clock. In embodiments, t_{skew} is the skew between clock paths to the two flip-flops on FPGA 3100.

[0369] In embodiments where there is a phase difference with the transmitter clock running less than 45 degrees ahead of the receiver clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, the transmit clock signal may also sample on the opposite edge as the receiving clock signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0370] In the embodiment of FIG. 5A, both the transceiver PLL 5108 and the zero-delay buffer PLL 5208b preferably run at the highest bandwidth available from the PLL on the FPGA, while the overall phase locking system including the phase detectors 5206, controller 5202 and PLL with Phase Adjustment 5300 runs at a low bandwidth. In such embodiments, the poles in the adjustable transceiver PLL 5108 are prevented from affecting the gain or phase margin of the off-chip PLL which may be included in the controller 5202. In embodiments, the highest bandwidth available from the PLL on the FPGA may range between 100 kHz and 10 MHz. In embodiments, any loop filter order may be used in the controller 5202 as long as the bandwidth is low enough to avoid interaction of poles in the control system. In embodiments, a low bandwidth may be, for example, 100Hz- 40kHz, 400Hz and 4kHz, 4kHz and 10kHz, 100Hz and 40kHz, 0Hz and 100Hz, to name a few. In embodiments, a second-order loop filter may be used in an effort to improve lock time and phaselocking error. In embodiments a third-order filter may be used if the second-order filter is stable. In embodiments, a first-order filter is also an option when the second-order filter has stability problems. In embodiments, other order filters may be used, depending on the internal bandwidth of the FPGA 5100.

[0371] In embodiments, the one or more interfaces may also include at least a second interface. The second interface of the one or more interfaces, may include a second plurality of pins of FPGA 5100. The second plurality of pins may be used to transmit and/or receive data and/or signals. In embodiments, the second plurality of pins may include a first clock output pin. The first clock output pin may be operationally connected to deserializer 5104. In embodiments, the first clock output pin may also be operationally connected to computation logic 5210 such that a first receiver side clock signal is transmitted from the deserializer 5104 to computation logic 5210 via the first clock output pin. Additionally, in some embodiments, the first clock output pin may also be operationally connected to zero-delay buffer PLL 5208a such that the receiver side clock is transmitted from the deserializer 5104 to the zero-delay buffer PLL 5208a via the first clock output pin. In embodiments the first receiver side clock signal may have a frequency ranging between 100-650 MHZ.

[0372] In embodiments, the second plurality of pins may also include a second clock output pin. The second clock output pin may be operationally connected to the serializer 5110. In embodiments, the second clock output pin may also be operationally connected to computation logic 5210 such that a transmitter side clock signal is transmitted from the serializer 5110 to computation logic 5210 via the second clock output pin. Additionally, in some embodiments, the second clock output pin may also be operationally connected to zero-delay buffer PLL 5208b such that the transmitter side clock is transmitted from the serializer 5110 to the zero-delay buffer PLL 5208b via the second clock output pin. In embodiments the transmitter side clock signal may have a frequency ranging between 100-650 MHZ.

[0373] The PLL with internal phase adjustment 5300 may be similar to the PLL 3300 in FIG. 3A. It is a component of the FPGA core fabric 5106 which generates a clock of adjustable phase and frequency.

[0374] In embodiments, where the bandwidth of the controller 5202 is too low, the receiving clock and the transmitter clock may not track each other closely enough to consider them locked. In embodiment, such tracking issues may be solved by adjusting the min and max delay constraints appropriately to provide a cushion for the clocks being away from the expected phase. In embodiments, a PD (Phase Detector) control system may be provided after the loop filter to aid in resolving tracking issues. In embodiments, tracking issues may be addressed by

adding some nonlinearity in the transfer function of the filter. Other solutions may also be possible.

[0375] In the embodiment of FIG. 5A, the controller 5202 utilizes a phase-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative (i.e., the derivative component will act against the loop filter, however, some references refer to this as being a positive direction) and less than 1 (so the path straight from the filter dominates). The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. The bandwidth of the standard PLL loop filter, in some embodiments, may range between 400Hz and 4khz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0376] FIG 5B is a block diagram of another FPGA system in accordance with an exemplary embodiment of the present invention. Unlike in the embodiment shown in FIG. 5A, an internal phase controller 5202 in the system of FIG. 5B is directly connected and provides phase control signals to the adjustable transceiver PLL 5108, which is located in the FPGA transceiver banks 5102 and outside the FPGA core 5106.

[0377] FIG. 5B illustrates a block diagram of an FPGA system in accordance with an embodiment of the present disclosure that provides phase control while minimizing latency wherein the FPGA has an acceptable phase-controlled transceiver PLL 5108. This embodiment uses the phase-controlled transceiver PLL directly to control the phase of TXCLOCK. An acceptable phase-control system must have adjustment gain capable of matching phase transients on the incoming data stream to within the timing margin ($t_{\min}$), satisfying the following inequality:

$$\int_0^{\infty} \left|\Delta t_{pk}(\omega)[1 - LF(\omega)]\right| d\omega \leq t_{min}$$

[0378] Where $\Delta t_{pk}(\omega)$ is the peak design jitter at that frequency and LF is the transfer function over frequency of the phase locking system consisting of the phase detector 5206, controller 5202, and PLL 5108. Expected functions for $\Delta t_{pk}(\omega)$ are specified within the protocol specifications for communication protocols used. For 10 Gigabit Ethernet, this is specified in clause 52.8 of the IEEE 802.3 standard.

[0379] In embodiments, the system of FIG. 5B generally includes FPGA 5100 which preferably includes FPGA transceiver banks 5102. In embodiments, the FPGA transceiver banks 5102 includes deserializer 5104 on the receiver end of FPGA 5100, transceiver PLL 5108, and serializer 5110 on the transmitter end of FPGA 5100. Deserializer 5104 may be similar to the deserializer 3104' and deserializer 3104'' discussed below in connection with FIGS. 6A-6E, the descriptions of which applying herein. Serializer 5110 may be similar to serializer 3110' and serializer 3110'' discussed below in connection with FIGS. 7A and 7B respectively, the descriptions of which applying herein. In embodiments, deserializer 5104 receives a serial data stream from the I/O module 5120 and provides deserialized data to the FPGA core 5106. More specifically, the deserializer 5104 will provide parallel data streams to the FPGA core 5106 for processing. As illustrated, this parallel data is provided to the computational logic 5210 where processing and computation takes place. FIG. 5B illustrates computational logic 5210 as a single element with a receiver side and a transmitting side. In embodiments, the computational logic 5210 may be implemented as a plurality of logic elements. In embodiments, when all computation is complete, the resulting data may be provided to serializer 5110 and then transmitted out of FPGA 5100, preferably via I/O module 5120, for example. In embodiments, the I/O module may be a direct soldered cable, on-chip optics, or an on-board optical transceiver, to name a few. Additionally, the I/O module may be an SFP, a QSFP, a micro QSFP, or a QSFP-DD, to name a few.

[0380] In embodiments, the serializer 5110 and deserializer 5104 (SERDES) circuit(s) may contain two major sections: (1) an analog side whose purpose is signal cleaning, and (2) a digital side which turns the analog signal into bits and converts between parallel and serial data streams. In embodiments, the analog side may include a few different types of amplifiers in order to provide signal cleaning.

[0381] In embodiments, as shown in FIG. 5B, an adjustable transceiver PLL 5108 may be located inside the FPGA 5100 fabric with adjustable feedback dividers, which in turn adjust the frequency of the PLL. Alternatively, the adjustable transceiver PLL 5108 may comprise a phase adjuster on the output of the loop, which adjusts the phase of the PLL directly. Unlike the PLL with phase adjustment 5300 in FIG. 5A, the adjustable transceiver PLL 5108 in FIG. 5B is located outside the FPGA core 5106 and within the FPGA transceiver banks 5102. The adjustable transceiver PLL 5108 in FIG. 5B may also differ from the PLL with phase adjustment 5300 in FIG. 5A in operating frequency.

[0382] As illustrated in FIG. 5B, in embodiments, the first receiver side clock signal RXCLOCK is based on, but has a different frequency and phase than, the REFERENCE CLOCK signal provided by oscillator 5000 based on the operation of the deserializer 5104, as is discussed above with respect to the serializer 104. In embodiments, the transmitter side clock signal TXCLOCK provided from the serializer 5110 may be provided by adjustable transceiver phase locked loop 5108. In this manner, the frequency or phase of the transmitter side clock signal TXCLOCK may be adjusted.

[0383] In embodiments, an internal phase controller 5202 is connected to the phase adjustment interface of the phase-controlled transceiver PLL 5108 and provides control signals to allow for adjustment of the phase of at least the transmitter side clock signal TXCLOCK. The phase of the incoming data, in embodiments, may be adjusted by adjusting the data stream received by I/O module 5120. In embodiments, the internal phase controller 5202 provides control signals based on the phase difference between the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK. In embodiments, the phase difference may be determined using phase detector 5206.

[0384] Using the configuration of FIG. 5B, the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK may be sufficiently aligned in phase such that there is no need for the clock domain crossing circuit discussed above, eliminating a technical problem. The technical solution to a technical problem, in embodiments, is shown in the system of FIG. 5B, which provides a wire or a logic path via the controller 5202 and adjustable transceiver PLL 5108 to adjust the phase of the transmitter side clock TXCLOCK to correspond to that of the first receiver side clock signal RXCLOCK. Some delays may be introduced in the path including

min_delay and max_delay constraints of the wire and components, however, such delays are insignificant compared to the larger delays that are necessarily present when an asynchronous clock domain crossing circuit is used.

[0385] In embodiments, with a phase difference between about 45° and 360°, the min_delay should be set at 0 and the max_delay should be set equal to the time between rising edges on the receive clock signal and transmit clock signal (as shown in FIGs. 2A and 2B). The difference between 45° and 360° approximates the minimum amount of time required to safely capture data. In embodiments, the formula for the time is as follows:

$$t_{min} = t_{setup} + t_{wire} + t_{clock\text{-}out} + \Delta t_{jitter} + t_{skew}$$

[0386] Referencing the above equation, t_{setup} is the setup time of a flip-flop (i.e., a latch) on FPGA 5100. The t_{wire} is the delay of the, for example, shortest wire (as compared to other wires on the FPGA) on FPGA 5100. In embodiments, the shortest wire is the shortest possible wire. In embodiments, $t_{clock\text{-}out}$ is the clock-to-output time of a flip-flop on the FPGA 5100. In embodiments, Δt_{jitter} is a safety factor for jitter on both clocks. Jitter, for example, is the deviation from true periodicity of a periodic signal from a reference clock. In embodiments, t_{skew} is the skew between clock paths to the two flip-flops on FPGA 5100.

[0387] In embodiments where there is a phase difference with the transmitter clock running less than 45° ahead of the receiver clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, the transmit clock signal may also sample on the opposite edge as the receiving clock signal launch edge, but cases are symmetric**.** In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0388] In the embodiment of FIG. 5B, both the transceiver PLL 5108 and the zero-delay buffer PLL 5208b preferably run at the highest bandwidth available from the PLL on the FPGA, while the overall phase locking system including the phase detectors 5206 and controller 5202 runs at a low bandwidth. In such embodiments, the poles in the adjustable transceiver PLL 5108

are prevented from affecting the gain or phase margin of the off-chip PLL which may be included in the controller 5202. In embodiments, the highest bandwidth available from the PLL on the FPGA may range between 100 kHz and 10 MHz. In embodiments, any loop filter order may be used in the controller 5202 as long as the bandwidth is low enough to avoid interaction of poles in the control system. In embodiments, a low bandwidth may be, for example, 100Hz-40kHz, 400Hz and 4kHz, 4kHz and 10kHz, 100Hz and 40kHz, 0Hz and 100Hz, to name a few. In embodiments, a second-order loop filter may be used in an effort to improve lock time and phaselocking error. In embodiments a third-order filter may be used if the second-order filter is stable. In embodiments, a first-order filter is also an option when the second-order filter has stability problems. In embodiments, other order filters may be used, depending on the internal bandwidth of the FPGA 5100.

[0389] In embodiments, the one or more interfaces may also include at least a second interface. The second interface of the one or more interfaces, may include a second plurality of pins of FPGA 5100. The second plurality of pins may be used to transmit and/or receive data and/or signals. In embodiments, the second plurality of pins may include a first clock output pin. The first clock output pin may be operationally connected to deserializer 5104. In embodiments, the first clock output pin may also be operationally connected to computation logic 5210 such that a first receiver side clock signal is transmitted from the deserializer 5104 to computation logic 5210 via the first clock output pin. Additionally, in some embodiments, the first clock output pin may also be operationally connected to zero-delay buffer PLL 5208a such that the receiver side clock is transmitted from the deserializer 5104 to the zero-delay buffer PLL 5208a via the first clock output pin. In embodiments the first receiver side clock signal may have a frequency ranging between 100-650 MHz.

[0390] In embodiments, the second plurality of pins may also include a second clock output pin. The second clock output pin may be operationally connected to serializer 5110. In embodiments, the second clock output pin may also be operationally connected to computation logic 5210 such that a transmitter side clock signal is transmitted from the serializer 5110 to computation logic 5210 via the second clock output pin. Additionally, in some embodiments, the second clock output pin may also be operationally connected to zero-delay buffer PLL 5208b such that the transmitter side clock is transmitted from the serializer 5110 to the zero-delay buffer

PLL 5208b via the second clock output pin. In embodiments the transmitter side clock signal may have a frequency ranging between 100-650 MHz.

[0391] In embodiments, where the bandwidth of the controller 5202 is too low, the receiving clock and the transmitter clock may not track each other closely enough to consider them locked. In embodiment, such tracking issues may be solved by adjusting the min and max delay constraints appropriately to provide a cushion for the clocks being away from the expected phase. In embodiments, a PD (Phase Detector) control system may be provided after the loop filter to aid in resolving tracking issues. In embodiments, tracking issues may be addressed by adding some nonlinearity in the transfer function of the filter. Other solutions may also be possible.

[0392] In the embodiment of FIG. 5B, the controller 5202 utilizes a phase-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative (i.e., the derivative component will act against the loop filter, however, some references refer to this as being a positive direction) and less than 1 (so the path straight from the filter dominates). The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. The bandwidth of the standard PLL loop filter, in some embodiments, may range between 400Hz and 4khz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0393] FIG. 5C illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. Like the embodiment shown in FIG. 5A, a PLL with phase adjustment 5300a located within the FPGA core 5106 is used by the FPGA system in FIG. 5C. Unlike in the embodiment shown in FIG. 5A, an additional control loop, comprising a phase detector 5206b, a controller 5202b, and an external delay element 5300b, is used to allow multiple deserializers 5104a, 5104b and serializers 5110a, 5110b to be aligned. For every additional receiver that needs to be phase-aligned, an additional control loop is required.

[0394] In embodiments, the external delay element 5300b may have an adjustment range at least as wide as one period of the parallel RX clock. This can be accomplished by using a long delay line or a pair of smaller delay lines with a glitch-free switchover circuit to hide the boundary conditions of the delay lines. In embodiments, the delay element 5200b may be implemented with a digital delay line (e.g., the SY89295U from Micrel), or a voltage-controlled delay element (e.g., the HMC910 from Analog devices).

[0395] In embodiments, the additional controller 5202b utilizes a delay-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative, i.e., the derivative component will act against the loop filter (noting, however, that some references refer to this as being a "positive" direction) and less than 1 so the path straight from the filter dominates. The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. In embodiments, the bandwidth of the standard PLL loop filter may range between 400Hz and 4kHz, 4kHz and 10kHz, 100Hz and 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0396] Similar to the system described in connection with FIG. 5A, the system of FIG. 5C may or may not include zero delay buffers 5208a, 5208b, and 5208c. In embodiments, zero-delay buffer 5208a may have a reference trace T1 whose length is matched to a length of wire T4 between the I/O pin of FPGA 4100 and external phase detectors 5206a, 5206b. Similarly, zero delay buffer 5208b may have a reference trace T2 whose length is matched to a second length of wire T5 between the I/O pin of the FPGA 5100 and the external phase detector 5206a. Also, similarly, zero delay buffer 5208c may have a reference trace T3 whose length is matched to a second length of wire T6 between the I/O pin of the FPGA 5100 and the external phase detector 5206b. Any length mismatch between reference traces T1 and wire T4 between the I/O pin of the FPGA 5100 and the external phase detectors 5206a, 5206b may introduce a deterministic phase error proportional to the mismatch of the length of the wires. Any length mismatch between reference traces T2 and wire T5 between the I/O pin of the FPGA 5100 and the external phase detector 5206a

may introduce a deterministic phase error proportional to the mismatch of the length of the wires. Any length mismatch between reference traces T3 and wire T6 between the I/O pin of the FPGA 5100 and the external phase detector 5206b may introduce a deterministic phase error proportional to the mismatch of the length of the wires.

[0397] In the embodiment of FIG. 5C, there may be three clocks which should be aligned, and the required timing constraints for passing data from one clock domain to another all follow the same pattern. In embodiments where there is a phase difference between any pair of aligned clocks with one clock running less than 45 degrees ahead of the other clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, one of the clock signals may also sample on the opposite edge as the signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0398] FIG. 5D illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. Like in the embodiment shown in FIG. 5B, an adjustable transceiver PLL 5108 located within the FPGA transceiver banks 5102 is used by the FPGA system of FIG. 3D. Unlike in the embodiment shown in FIG. 5B, an additional control loop similar to the additional control loop in FIG. 5C is used to allow multiple deserializers 5104a, 5104b and serializers 5110a, 5110b to be aligned. In embodiments, the additional control loop in the embodiment of FIG. 5D operates in the manner identical to the additional control loop described for FIG. 5C.

[0399] FIG. 5E illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. This embodiment is similar to the embodiment shown in FIG. 5C in almost all aspects, except that the delay element 5300b is internal to the FPGA 5100, unlike the delay element 5300b located outside of the FPGA 5100 in FIG. 5C. In embodiments, the delay element 5300b in FIG. 5E has the same requirements as the external delay element 5300b shown in FIG. 5C.

[0400] FIG. 5F illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. This embodiment is similar to the embodiment shown in FIG. 5D in almost all aspects, except that the delay element 5300b is internal to the FPGA 5100, unlike the delay element 5300b located outside of the FPGA 5100 in FIG. 5D. In embodiments, the delay element 5300b in FIG. 5F has the same requirements as the external delay element 5300b shown in FIG. 5D.

[0401] FIG. 6A is an exemplary block diagram of a deserializer suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention. Deserializer 3104', in embodiments, may include an input buffer 6104, a continuous time linear equalizer (CTLE) 6106, a variable gain amplifier (VGA) 6108; voltage adder 6110; decision feedback equalizer (DFE) 6110, clock and data recovery (CDR) 6116, Serial to parallel box 6118, decision circuit 6112, and clock divider 6120. In embodiments, deserializer 3104' may not include one or more of the following components: CTLE 6106, DFE 6114, and/or VGA 6108, to name a few.

[0402] A deserializer circuit accepts a data stream from an input buffer and converts it into a parallel format at a lower bit rate. First, data comes into the chip from the input pins 6102 into an input buffer 6104. In embodiments, the input buffer receives a transmission from an I/O module, such as I/O module 4120. A continuous time linear equalizer (CTLE) 6106 may be used after the input buffer 6104 to improve signal quality by placing a zero near the dominant pole of the transmission medium to cancel the first pole of the system. A variable-gain amplifier (VGA) 6108 may then be used to scale the signal up for further processing. This output is then turned into a binary 0-1 decision by the decision circuit 6112. In embodiments, the decision circuit 6112 includes adder 6110. A decision feedback amplifier may be included to further improve signal integrity by taking the results of the decision circuit, applying a weighting filter, and adding the result to the output from the VGA 6108. When the signal is in the digital domain, a clock and data recovery circuit (CDR) 6116 recovers the phase of the data and create a wire-rate clock that is phase-aligned to the received data. The CDR 6116 may use a reference clock and *a priori* knowledge of the nominal frequency of the data stream to set the frequency of the recovered clock. With a clock aligned to the data stream, which in some embodiments may be a high speed data stream (e.g., 10 Gbps, 25 Gbps, a range from 9-25 Gbps, 10-25 Gbps, 22-33 Gbps, 33-45 Gbps, 45-60 Gbps, 60-80Gbps, 80-120 Gbps, or 1 Gbps-100 Gbps, to name a few) the receiver

can use a clock divider 6120 and a serial-to-parallel circuit 6118 to convert the serial data stream into a lower-frequency than the data stream (e.g., $1/4^{th}$ of the data rate of the high speed data stream or $1/256^{th}$ of the data rate of the high speed data stream, to name a few) parallel data stream.

[0403] In embodiments, a decision feedback equalizer 6114 (DFE) may be provided. In embodiments, the decision feedback equalizer may be a filter that subtracts or adds at least *n* decided bits to cancel inter-symbol interference on the wire. In embodiments, a clock and data recovery circuit may be provided and includes a data phase detector, which may be any of the circuits discussed above, as well as a phase-locked loop circuit.

[0404] FIG. 6B is an exemplary circuit diagram of a continuous-time linear equalizer (CTLE) suitable for use in the deserializer of FIG. 6A in accordance with an exemplary embodiment of the present invention. CTLE 3106", in some embodiments, places a zero to cancel out the dominant pole of the trans mission line for an incoming signal. In embodiments, CTLE 3106" is a linear filter applied at a receiver, in the case of FIG. 6B, input buffer 6104, that attenuates low-frequency signal components and filters off higher frequencies. The CTLE 3106" may be adjusted to optimize the ratio of low frequency attenuation to high frequency amplification. In embodiments, a variable gain amplifier may be provided and used to scale the output of the CTLE to as large of a signal as possible. In embodiments, a decision circuit may also be provided.

[0405] FIG. 6C is an exemplary block diagram of a clock and data recovery (CDR) circuit suitable for use in the deserializer of FIG. 6A in accordance with an embodiment of the present invention. In embodiments, CDR 6116' circuit recovers phase information from an incoming data stream. The data stream, in embodiments, may be received by an alexander phase detector 6302. The CDR 6116' may also obtain frequency information from a reference clock, output. In embodiments, the output may determine whether the recovered clock have the same phase as the recovered data.

[0406] FIG. 6D is an exemplary circuit diagram of a decision circuit 6112' suitable for use in the deserializer of FIG. 6A in accordance with an embodiment of the present invention. FIG. 6D illustrates an exemplary embodiment of such a decision circuit 6112' utilizing a StrongARM sense amplifier. In embodiments, any comparator circuit may be used as a decision circuit.

[0407] FIG. 6E illustrates an exemplary embodiment of deserializer 3104''. In embodiments, the deserializer 3104'' may include a receiver PMA 6512 and receiver PCS 6508.

The receiver PMA 6512 may include receiver buffer 6504, CDR 6516, and serial to parallel box 6118'. In embodiments, the receiver buffer 6504 receives serial differential input data 6502. In embodiments, this data is received by an I/O module, such as the I/O module 4120 of FIG. 4A. In embodiments, the data is then received by the CDR 6516 from the receiver buffer 6504. The CDR, in embodiments, transmits the inputted serial data, a serial clock signal, and a parallel clock signal to the serial to parallel box 6118'. The CDR may also transmits the parallel clock data to the receiver PCS 6508. The serial to parallel box 6118', in embodiments, then converts the serial data into parallel data, transmitting the parallel data to the receiver PCS 6508. The receiver PCS 6508 transmits parallel data to the FPGA Core 4106.

[0408] In addition to the components illustrated in FIG. 6E, deserializer 3104'' may also include or be electrically coupled to a continuous-time linear equalizer (CTLE) (*see* FIG. 6B) which is a pure analog circuit that may be used to correct channel issues. In embodiments, the deserializer 3104'' may include a shift register or demultiplexer with a counter.

[0409] FIG. 7A is an exemplary block diagram of a serializer 3110' suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention. The serializer circuit accepts a clock running at wire rate 4112 (from transceiver PLL 4108) and accepts parallel data (e.g., TX data 7102) to serialize the data. Data is converted from a parallel format to a serial data stream in the parallel to serial box 7104. A feed-forward equalizer (FFE) 7106, which uses the history of bits serialized on the wire to filter out inter-symbol interference, may be included to improve signal integrity. Finally, the serializer outputs the serial data stream to a transmission medium using an output buffer 7114. The serializer also generates a parallel clock (TX Clk 7110), that operates at a lower speed than the data stream (e.g., 100-400 MHz, 100-600 MHz, to name a few), for use by other components using either a simple clock divider 7108 or a more complex clock generation block which can contain dividers and phase shifting elements for aligning multiple transmitters.

[0410] FIG. 7B illustrates an exemplary embodiment of serializer 3110''. As discussed above with respect to FIGs. 4A and 7A, serializer 3110'' receives parallel data streams from the FPGA core 4106 and serializes them for transmission out of the FPGA 4100. In embodiments, serializer 3110'' may include transmitter PCS 7206, clock generation block 7210, and transmitter PMA 7216. In embodiments, transmitter PMA 7216 may include parallel to serial box 7104' and

transmitter buffer 7214. The transmitter PCS 7206 may receive parallel data from FPGA core 4106. In embodiments, the parallel data is then transmitted to the parallel to serial box 7104'. The clock generation block 7210 may receive a wire-rate clock signal 7112. The clock generation block 7210, in embodiments, may split the signal in to a parallel clock signal and serial clock signal, both the parallel and serial signals being transmitted to the parallel to serial box 7104'. The parallel to serial box 7104' may covert the data from parallel to serial, transmitting the serial differential output data 7218 to the transmitter buffer 7214. Then, in embodiments, the transmitter buffer 7214 outputs the serial differential output data 7218.

[0411] In embodiments the serializer 3110'' may be a shift register or a multiplexer with a counter. In embodiments, the serializer 3110'' may include additional components, such as a feed forward equalizer (FFE) which uses the last *n* bits to cancel inter symbol interference on the wire. In embodiments, a buffer amplifier may be included which provides variable gain to allow adjustable voltage swing on the output of the transmitter. In embodiments, a clock divider may be provided. In embodiments, the clock divider may generate a low-speed clock (e.g., 100-400 MHz, 100-600 MHz, to name a few) for the serializer and the PMA/PCS. In embodiments, the clock divider is typically provided using a counter. In embodiments, the clock generation block 7210 might also include a clock phase adjustment circuit to allow multiple transmitter lanes to be phase-aligned.

[0412] Referring to FIGS. 8A-8D, in embodiments, the phase detector 4206 may be an analog, single bit phase detector which may be implemented using a variety of circuit components including (1) an XOR gate; (2) S-R flip-flop; (3) D flip-flop; (4) Edge-triggered JK flip-flop; (5) Gilbert cell multiplier and/or (6) Diode ring mixer, to name a few. FIG. 8A illustrates an exemplary embodiment of a phase detector 3206' that utilizes D flip-flops. FIG. 8B illustrates another exemplary embodiment of a phase detector 3206" that utilizes S-R flip-flops. FIG. 8C is another exemplary block diagram of a phase detector 3206"' suitable for use in the field programmable gate array system of FIG. 4A in accordance with an embodiment of the present invention. FIG. 8D is another exemplary block diagram of a phase detector 3206"" suitable for use in the field programmable gate array system of FIG. 4A in accordance with an embodiment of the present invention. Other than a basic phase detector, a time-to-digital converter (TDC) can be used to detect the phase offset of the clocks. FIG. 8C shows a Vernier TDC and FIG. 8D shows a parallel delay line TDC as examples. The Vernier TDC uses a pair of unequal delay lines to delay

the two signals by varying amounts and uses D-type flip-flops to quantify the phase difference between the two signals at multiple points along the delay line. The parallel delay line TDC uses a set of simple phase detectors with the two input signals delayed by varying amounts to quantify the phase difference between the two signals. In both cases, a decoding circuit is used to translate the results of the individual phase detection elements into a phase offset.

[0413] In embodiments, the phase detector 4206 may be a multi-bit phase detector, sometimes referred to as a time-to digital converter (TDC). In embodiments, such a phase detector may be a counter-based TDC that counts up the time between START and STOP. In embodiments, such a phase detector may be an interpolator TDC in which time measurement may be performed by measuring a voltage difference (e.g., by using a ramp wave and sampling at two points or by charging a capacitor). In embodiments, a phase detector may be a Vernier TDC as shown in FIG. 8C.

[0414] In embodiments the phase detector 4206 may be implemented using a tapped delay line TDC. In embodiments, the phase detector 4206 may be implemented using a metastability-based phase detector. In embodiments, the metastability-based phase detector is similar to a D flip-flop phase detector but includes an averaging filter. In embodiments, a parallel-delay-line TDC may be used to implement the phase detector 4206. FIG. 8D illustrates an example of a parallel-delay-line TDC. In embodiments, the phase detector may be implemented as a pulse-shrinking TDC. Such a pulse-shrinking TDC may generate a pulse and then send it circularly through an engineered delay line to shrink it until it is gone, count the number of times it goes through the pulse-shrinking circuit.

[0415] In embodiments, the phase detector may be implemented as a scrambling TDC. Scrambling TDCs may be implemented with added digital noise shaping to suppress errors. In embodiments, the phase detector 4206 may be implemented as a PLL/DLL-based TDC. In such an embodiment, the phase detector may lock a digital PLL to the incoming feedback signal and record the internal control code.

[0416] In embodiments, all of the phase detector embodiments discussed above may be combined with or connected to a low-pass filter and an analog to digital converter (ADC). In embodiments, other examples of phase detectors may be used consistent with the teachings of this disclosure.

[0417] The pseudo code shown below implements the control loop inside the PLL or DLL controller (e.g., 3202 in FIGs. 3A-3B, 4202 in FIG. 4A, or 5202 in FIGs. 5A-5B) and communicates with the host in accordance with an exemplary embodiment of the present invention. In embodiments, the pseudocode shown below, or a similar pseudocode is run by the FPGA or a soft processor programmed on the FPGA and uses an interrupt- or event-based system to run the control algorithm for either the PLL or DLL paths on the device. The main control loop is triggered on every sample of the internal ADC.

```
Begin:

    Set up peripherals
    Program initial configuration
    Set up for periodic free-running measurement from the TDC
    Wait

On Periodic Interrupt:
    Read TDC code into Window[0]
    ControlCode = DigitalFilter(Window)
    Read MODE pin to Mode

    If Mode = PLL_MODE then:
        Output ControlCode to PLL frequency adjustment interface
    Else:
        Output ControlCode to PLL phase adjustment interface

    Shift Window array by 1
```

[0418] FIGs 9A-C, 10A-B and 11 are flow charts of a process implementing the field programmable gate array system in accordance with an exemplary embodiment of the present invention. In embodiments, the process described in the flow charts of FIGs. 9A-C, 10A-B and 11 may be implemented by the field programmable gate array system shown in FIG. 4A. The field programmable gate array system, including the field programmable gate array and the components thereof, may be similar to the field programmable gate array systems of FIG. 4A, the descriptions of which applying herein.

[0419] The process of FIGs. 9A-9C may begin at step S902. Referring to FIG. 9A, at step S902, a first serial data stream is received by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system. In embodiments, the

first serial data stream may include market data. In embodiments, market data may be price and trade-related data for a financial instrument reported by a trading venue (i.e., a stock exchange).

[0420] At a step S904, a first clock signal having a first frequency and a first phase is received by a first reference clock in in the first interface. In embodiments, step S904 may be performed before step S902. In embodiments step S904 may be performed contemporaneously with step S902.

[0421] The process of FIGs. 9A-9C may continue with a step S906. At step S906, the first plurality of data pins of the first interface may transmit the first serial data stream to a deserializer in the field programmable gate array.

[0422] At a step S908, the first reference clock pin in the first interface may transmit the first clock signal to the deserializer. In embodiments, step S908 may be performed before step S906. In embodiments step S908 may be performed contemporaneously with step S906.

[0423] At a step S910, a first receiver side clock signal may be generated by the deserializer. In embodiments, the first receiver side clock signal may have a second frequency and a second phase. In embodiments, the second frequency is different from the first frequency. In embodiments, the second frequency corresponds to the first frequency. In embodiments, corresponding may refer to the frequencies being the same frequency. In embodiments corresponding may also refer to frequencies being close (e.g., within an acceptable range in the art) to the same frequencies. In embodiments, the first phase and the second phase may not be aligned. In embodiments the first phase and the second phase are aligned. In embodiments, a difference between the first phase and the second phase is below a threshold level. In embodiments, the deserializer generates the first receiver clock signal based at least in part on the first clock signal.

[0424] At a step S912, the first serial data stream received by the deserializer may be converted, by the deserializer, into a first plurality of data streams. In embodiments, the first plurality of data streams may include a first amount of data streams. In embodiments, the first amount of data streams is equal to eight (8) data streams. In embodiments, the first amount of data streams is equal to ten (10) data streams. In embodiments, the first amount of data streams is equal to sixteen (16) data streams. In embodiments, the first amount of data streams is equal to twenty (20) data streams. In embodiments, the first amount of data streams is equal to thirty-two (32)

data streams. In embodiments, the first amount of data streams is equal to forty (40) data streams. In embodiments, the first amount of data streams is equal to sixty-four (64) data streams. In embodiments, the first amount of data streams is equal to eighty (80) data streams. In embodiments, the first amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the first amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the first amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the first amount of data streams is equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the first amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0425] At a step S914, the first receiver side clock signal is transmitted from the deserializer to computational circuitry in the field programmable gate array.

[0426] At a step S916, the first plurality of data streams is transmitted form the deserializer to the computational circuitry. In embodiments, the first plurality of data streams includes a first plurality of data items. In embodiments, step S916 may be performed before step S914. In embodiments step S916 may be performed contemporaneously with step S914.

[0427] At a step S918, the first receiver side clock signal is transmitted from the deserializer via a first clock output pin on a second interface of the field programmable gate array to a phase detector of the field programmable gate array system which is not on the field programmable gate array. In embodiments, the transmission of the first receiver side clock signal is also via a first zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the first clock output pin of the second interface.

[0428] At a step S920, a first transmitter side clock signal is generated by the field programmable gate array system. In embodiments, the first transmitter side clock signal has a third frequency and a third phase. In embodiments, the third frequency corresponds to the second frequency. In embodiments the third phase may be aligned with the second phase. In embodiments, the third phase and the second phase may not be aligned. In embodiments, the third phase and the second phase may have a difference in phases that is less than a second threshold level. In embodiments, the first transmitter side clock signal is generated by performing the following steps until a first output of the phase detector is below a first threshold.

[0429] Referring to FIG. 10A, generating the first transmitter side clock signal may begin at step S1002. At step S1002, a second clock signal is generated by an adjustable oscillator in the field programmable gate array system. In embodiments, the second clock signal may have a fourth frequency and a fourth phase.

[0430] The process of FIGs. 10A-B may continue at a step S1004. At step S1004, a first wire rate clock signal having a fifth phase and a fifth frequency is generated. In embodiments, the generation of the first wire rate clock signal may be based in part on the second clock signal. In embodiments the fifth frequency is a rational multiple of the fourth frequency. In embodiments the fifth frequency is equal to x times the fifth frequency where x is the second amount of data streams. In embodiments the fifth frequency is equal to x times the frequency of the of the transmitter side clock signal where x is half of the second amount of data streams.

[0431] In embodiments, the generation of the first wire rate clock signal may be performed with the following steps. Referring to FIG. 11, at a step S1102, the second clock signal is received from the adjustable oscillator at a transceiver phase lock loop via a second reference clock pin in the first interface. At a step S1104, the second clock signal is processed by the transceiver phase lock loop. As a step S1106, the first wire rate clock signal is provided by the transceiver phase lock look. The providing of the first wire rate clock signal, in embodiments, may be based at least in part on the processing of the received clock signal. Once the first wire rate clock signal is provided, at a step S1108. the first wire rate clock signal is transmitted by the transceiver phase lock loop to a serializer on the field programmable gate array. In embodiments, the first wire rate clock is generated by a phase lock loop. In embodiments, the phase lock loop that generates the first wire rate clock signal is on field programmable gate array. In embodiments, the phase lock loop that generates the first wire rate clock signal is part of the field programmable gate array system and not part of the field programmable gate array.

[0432] In embodiments, the generation of the first wire rate clock signal may include processing the second clock signal. Once the second clock signal is processed, the first wire rate clock signal may be provided. The providing of the first wire rate clock signal, in embodiments, is based at least in part on the processing of the second clock signal. After providing the first wire rate clock signal, in embodiments, the first wire rate clock signal may be transmitted to the serializer.

[0433] Referring back to FIG. 10A, at a step 1006, an interim transmitter side clock signal having a sixth frequency and a sixth phase is generated by the serializer in the field programmable gate array. In embodiments, the sixth frequency corresponds to the third frequency. In embodiments the sixth phase may be aligned with the third phase. In embodiments, the sixth frequency may correspond to the third frequency and the sixth phase may not be aligned with the third phase. In embodiments, the sixth phase and the third phase may not be aligned. In embodiments, the third phase and the sixth phase may have a difference in phases that is less than a second threshold level.

[0434] At a step S1008, the interim transmitter side clock signal is transmitted from the serializer via a second clock output pin of the second interface to the phase detector. In embodiments, the transmission of the interim transmitter side clock is also via a second zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the second clock output in of the second interface.

[0435] The process of FIGs. 10A-10B may continue with at a step S1010. Referring to FIG. 10B, at a step S1010, a first output is generated by the phase detector. The first output, in embodiments, is based at least on a comparison of the first receiver side clock signal and the interim side clock signal. The first output, in embodiments, may include information indicating the phase differences (if there is any) between the first receiver side clock and the interim side clock signal. Additionally, in embodiments, the first output may include information indicating a difference (if there is any) of frequencies between the first receiver side clock signal and the interim side clock signal.

[0436] At a step S1012, the first output may be transmitted from the phase detector to a phase controller of the field programmable gate array system, which may be placed within the field programmable gate array.

[0437] At a step S1014, interim adjustment information is determined by the phase controller. In embodiments, the interim adjustment information may be based at least in part on the first output. For example, the interim adjustment information may indicate necessary adjustments to align the phases of the first receiver side clock signal and the interim side clock signal. As another example, the interim adjustment information may indicate necessary

adjustments to align the frequencies of the first receiver side clock signal and the interim side clock signal.

[0438] At a step S1016, the interim adjustment information is transmitted from the phase controller to the adjustable oscillator. In embodiments, once the interim adjustment information is received, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information. The adjustment of the second clock signal, in embodiments, may change the phase of the second clock signal. In embodiments, the interim adjustment information indicates a desired phase. In embodiments, the interim adjustment information indicates a desired frequency. In embodiments, the interim adjustment information indicates a change in phase. In embodiments, the interim adjustment information indicates a change in frequency. In embodiments, the adjustment information includes a voltage. In embodiments, the adjustment information includes a digital transmission. For example, the adjustment information may be a command over a serial bus (e.g., I2C or SPI) that adjusts a clock divider or phase rotator. As another example, the adjustment information may trigger a set of parallel digital wires for "frequency/phase up," "frequency/phase down," and/or "frequency/phase step." In embodiments, the adjustment of the second clock signal may change the frequency of the second clock signal.

[0439] In embodiments, steps S1002 through steps S 1016 are repeated until the first output of the phase detector is below the first threshold level. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have phases that are aligned. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have frequencies that correspond to one another.

[0440] Referring back to FIG. 9B, once the first output of the phase detector is below a first threshold level, at a step S922, the serializer may transmit the first transmitter side clock signal to the computational circuitry. At a step S924, a first set of operations performed by the computational circuitry on at least a portion of the first plurality of data items to generate a second plurality of data streams. In embodiments, the first operation includes a trading algorithm. In embodiments the trading algorithm may include the parsing the market data. Once the market data is parsed, mathematical operations are performed at a portion of the market data. After the mathematical operations are performed, order packets are generated using at least an output of the mathematical operations. In embodiments, the first set of operations includes at least one of the

following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

[0441] In embodiments, at least a portion of the first set of operations is performed prior to step S922. In embodiments, at least a portion of the first set of operations is performed after step S922. In embodiments all of the first set of operations is performed after step S922.

[0442] In embodiments, the second plurality of data streams may include a second amount of data streams. In embodiments, the second amount of data streams may be the same as the first amount of data streams. In embodiments, the second amount of data streams is equal to eight (8) data streams. In embodiments, the second amount of data streams is equal to ten (10) data streams. In embodiments, the second amount of data streams is equal to sixteen (16) data streams. In embodiments, the second amount of data streams is equal to twenty (20) data streams. In embodiments, the second amount of data streams is equal to thirty-two (32) data streams. In embodiments, the second amount of data streams is equal to forty (40) data streams. In embodiments, the second amount of data streams is equal to sixty-four (64) data streams. In embodiments, the second amount of data streams is equal to eighty (80) data streams. In embodiments, the second amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the second amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the second amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the second amount of data streams is equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the second amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0443] At a step S926, the second plurality of data streams is transmitted from the computational circuitry to the serializer. Once received by the serializer, at a step S928, the serializer converts the second plurality of parallel data streams into the second serial data stream. The second serial data stream, in embodiments, includes trading data. Trading data, for example, may be any data related to purchasing or selling of stocks, commodities, goods, and/or services.

[0444] At a step S930, the second serial data stream may be transmitted from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface. In embodiments, the second serial data stream is transmitted from the serializer on the field programmable gate array to an input/output module of the field gate array system but not on

the field gate array. The second serial data stream may then be transmitted from the input/output module off the field gate array system.

[0445] FIGs 12A-C, 13A-B and 14 are exemplary flow charts of a process implementing the field programmable gate array system in accordance with another exemplary embodiment of the present invention. In embodiments, the process described in the flow charts of FIGs. 12A-C, 13A-B and 14 may be implemented by the field programmable gate array system shown in FIG. 3A or FIG. 5A. The field programmable gate array system, including the field programmable gate array and the components thereof, may be similar to the field programmable gate array systems of FIG. 3A and 5A, the descriptions of which applying herein.

[0446] The process of FIGs. 12A-12C may begin at step S1202. Referring to FIG. 12A, at step S1202, a first serial data stream is received by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system. In embodiments, the first serial data stream may include market data. In embodiments, market data may be price and trade-related data for a financial instrument reported by a trading venue (i.e., a stock exchange).

[0447] At a step S1204, a first clock signal having a first frequency and a first phase is received by a first reference clock in in the first interface. In embodiments, step S1204 may be performed before step S1202. In embodiments, step S1204 may be performed contemporaneously with step S1202.

[0448] The process of FIGs. 12A-12C may continue with a step S1206. At step S1206, the first plurality of data pins of the first interface may transmit the first serial data stream to a deserializer in the field programmable gate array.

[0449] At a step S1208, the first reference clock pin in the first interface may transmit the first clock signal to the deserializer. In embodiments, step S1208 may be performed before step S1206. In embodiments step S1208 may be performed contemporaneously with step S1206.

[0450] At a step S1210, a first receiver side clock signal may be generated by the deserializer. In embodiments, the first receiver side clock signal may have a second frequency and a second phase. In embodiments, the second frequency is different from the first frequency. In embodiments, the second frequency corresponds to the first frequency. In embodiments,

corresponding may refer to the frequencies being the same frequency. In embodiments corresponding may also refer to frequencies being close (e.g., within an acceptable range in the art) to the same frequencies. In embodiments, the first phase and the second phase may not be aligned. In embodiments the first phase and the second phase are aligned. In embodiments, a difference between the first phase and the second phase is below a threshold level. In embodiments, the deserializer generates the first receiver clock signal based at least in part on the first clock signal.

[0451] At a step S1212, the first serial data stream received by the deserializer may be converted, by the deserializer, into a first plurality of data streams. In embodiments, the first plurality of data streams may include a first amount of data streams. In embodiments, the first amount of data streams is equal to eight (8) data streams. In embodiments, the first amount of data streams is equal to ten (10) data streams. In embodiments, the first amount of data streams is equal to sixteen (16) data streams. In embodiments, the first amount of data streams is equal to twenty (20) data streams. In embodiments, the first amount of data streams is equal to thirty-two (32) data streams. In embodiments, the first amount of data streams is equal to forty (40) data streams. In embodiments, the first amount of data streams is equal to sixty-four (64) data streams. In embodiments, the first amount of data streams is equal to eighty (80) data streams. In embodiments, the first amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the first amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the first amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the first amount of data streams is equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the first amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0452] At a step S1214, the first receiver side clock signal is transmitted from the deserializer to computational circuitry in the field programmable gate array.

[0453] At a step S1216, the first plurality of data streams is transmitted form the deserializer to the computational circuitry. In embodiments, the first plurality of data streams includes a first plurality of data items. In embodiments, step S1216 may be performed before step S1214. In embodiments step S1216 may be performed contemporaneously with step S1214.

[0454] At a step S1218, the first receiver side clock signal is transmitted from the deserializer to a phase detector of the field programmable gate array system. The phase detector may or may not be placed on the field programmable gate array. If the phase detector is not on the field programmable gate array, the first receiver side clock signal is transmitted from the deserializer to the phase detector via a first clock output pin on a second interface of the field programmable gate array. In embodiments, the transmission of the first receiver side clock signal to the phase detector may also be via a first zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the first clock output pin of the second interface.

[0455] At a step S1220, a first transmitter side clock signal is generated by the field programmable gate array system. In embodiments, the first transmitter side clock signal has a third frequency and a third phase. In embodiments, the third frequency corresponds to the second frequency. In embodiments the third phase may be aligned with the second phase. In embodiments, the third phase and the second phase may not be aligned. In embodiments, the third phase and the second phase may have a difference in phases that is less than a second threshold level. In embodiments, the first transmitter side clock signal is generated by performing the following steps until a first output of the phase detector is below a first threshold.

[0456] Referring to FIG. 13A, generating the first transmitter side clock signal may begin at step S1302. At step S1302, a second clock signal is generated by a phase lock loop with phase adjustment in the field programmable gate array system. In embodiments, the phase lock loop with phase adjustment is on the field programmable gate array. In embodiments, the phase lock loop with phase adjustment is located within the core of the field programmable gate array. In embodiments, the second clock signal may have a fourth frequency and a fourth phase.

[0457] The process of FIGs. 13A-B may continue at a step S1304. At step S1304, a first wire rate clock signal having a fifth phase and a fifth frequency is generated. In embodiments, the generation of the first wire rate clock signal may be based in part on the second clock signal. In embodiments the fifth frequency is a rational multiple of the fourth frequency. In embodiments the fifth frequency is equal to x times the fifth frequency where x is the second amount of data streams. In embodiments the fifth frequency is equal to x times the frequency of the of the transmitter side clock signal where x may be half of the second amount of data streams.

[0458] In embodiments, the generation of the first wire rate clock signal may be performed with the following steps. Referring to FIG. 14, at a step S1402, the second clock signal is received from the phase lock loop with phase adjustment at a transceiver phase lock loop via a second reference clock pin in the first interface. At a step S1404, the second clock signal is processed by the transceiver phase lock loop. As a step S1406, the first wire rate clock signal is provided by the transceiver phase lock loop. The providing of the first wire rate clock signal, in embodiments, may be based at least in part on the processing of the received second clock signal. Once the first wire rate clock signal is provided, at a step S1408, the first wire rate clock signal is transmitted by the transceiver phase lock loop to a serializer on the field programmable gate array. In embodiments, the first wire rate clock signal is generated by a phase lock loop. In embodiments, the phase lock loop that generates the first wire rate clock signal is on field programmable gate array. In embodiments, the phase lock loop that generates the first wire rate clock signal may be part of the field programmable gate array system and not part of the field programmable gate array.

[0459] In embodiments, the generation of the first wire rate clock signal may include processing the second clock signal. Once the second clock signal is processed, the first wire rate clock signal may be provided. The providing of the first wire rate clock signal, in embodiments, is based at least in part on the processing of the second clock signal. After providing the first wire rate clock signal, in embodiments, the first wire rate clock signal may be transmitted to the serializer.

[0460] Referring back to FIG. 13A, at a step 1306, an interim transmitter side clock signal having a sixth frequency and a sixth phase is generated by the serializer in the field programmable gate array. In embodiments, the sixth frequency corresponds to the third frequency. In embodiments the sixth phase may be aligned with the third phase. In embodiments, the sixth frequency may correspond to the third frequency and the sixth phase may not be aligned with the third phase. In embodiments, the sixth phase and the third phase may not be aligned. In embodiments, the third phase and the sixth phase may have a difference in phases that is less than a second threshold level.

[0461] At a step S1308, the interim transmitter side clock signal is transmitted from the serializer to the phase detector, which may or may not be on the field programmable gate array. If the phase detector is not on the field programmable gate array, the interim transmitter side clock

signal may be transmitted from the serializer to the phase detector via a second clock output pin of the second interface. In embodiments, the interim transmitter side clock signal may also be transmitted via a second zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the second clock output in of the second interface.

[0462] The process of FIGs. 13A-13B may continue with at a step S1310. Referring to FIG. 13B, at a step S1310, a first output is generated by the phase detector. The first output, in embodiments, is based at least on a comparison of the first receiver side clock signal and the interim side clock signal. The first output, in embodiments, may include information indicating the phase differences (if there is any) between the first receiver side clock and the interim side clock signal. Additionally, in embodiments, the first output may include information indicating a difference (if there is any) of frequencies between the first receiver side clock signal and the interim side clock signal.

[0463] At a step S1312, the first output may be transmitted from the phase detector to a phase controller of the field programmable gate array system, which may be placed within the field programmable gate array.

[0464] At a step S1314, interim adjustment information is determined by the phase controller. In embodiments, the interim adjustment information may be based at least in part on the first output. For example, the interim adjustment information may indicate necessary adjustments to align the phases of the first receiver side clock signal and the interim side clock signal. As another example, the interim adjustment information may indicate necessary adjustments to align the frequencies of the first receiver side clock signal and the interim side clock signal.

[0465] At a step S1316, the interim adjustment information is transmitted from the phase controller to the phase lock loop with phase adjustment. In embodiments, once the interim adjustment information is received, the phase lock loop with phase adjustment adjusts the second clock signal based on the interim adjustment information. The adjustment of the second clock signal, in embodiments, may change the phase of the second clock signal. In embodiments, the interim adjustment information indicates a desired phase. In embodiments, the interim adjustment information indicates a desired frequency. In embodiments, the interim adjustment information indicates a change in phase. In embodiments, the interim adjustment information indicates a

change in frequency. In embodiments, the adjustment information includes a voltage. In embodiments, the adjustment information includes a digital transmission. For example, the adjustment information may be a command over a serial bus (e.g., I2C or SPI) that adjusts a clock divider or phase rotator. As another example, the adjustment information may trigger a set of parallel digital wires for "frequency/phase up," "frequency/phase down," and/or "frequency/phase step." In embodiments, the adjustment of the second clock signal may change the frequency of the second clock signal.

[0466] In embodiments, steps S1302 through steps S 1316 are repeated until the first output of the phase detector is below the first threshold level. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have phases that are aligned. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have frequencies that correspond to one another.

[0467] Referring back to FIG. 12B, once the first output of the phase detector is below a first threshold level, at a step S1222, the serializer may transmit the first transmitter side clock signal to the computational circuitry. At a step S1224, a first set of operations performed by the computational circuitry on at least a portion of the first plurality of data items to generate a second plurality of data streams. In embodiments, the first operation includes a trading algorithm. In embodiments the trading algorithm may include the parsing the market data. Once the market data is parsed, mathematical operations are performed at a portion of the market data. After the mathematical operations are performed, order packets are generated using at least an output of the mathematical operations. In embodiments, the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

[0468] In embodiments, at least a portion of the first set of operations is performed prior to step S1222. In embodiments, at least a portion of the first set of operations is performed after step S922. In embodiments all of the first set of operations is performed after step S1222.

[0469] In embodiments, the second plurality of data streams may include a second amount of data streams. In embodiments, the second amount of data streams may be the same as the first amount of data streams. In embodiments, the second amount of data streams is equal to eight (8) data streams. In embodiments, the second amount of data streams is equal to ten (10) data streams.

In embodiments, the second amount of data streams is equal to sixteen (16) data streams. In embodiments, the second amount of data streams is equal to twenty (20) data streams. In embodiments, the second amount of data streams is equal to thirty-two (32) data streams. In embodiments, the second amount of data streams is equal to forty (40) data streams. In embodiments, the second amount of data streams is equal to sixty-four (64) data streams. In embodiments, the second amount of data streams is equal to eighty (80) data streams. In embodiments, the second amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the second amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the second amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the second amount of data streams is equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the second amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0470] At a step S1226, the second plurality of data streams is transmitted from the computational circuitry to the serializer. Once received by the serializer, at a step S1228, the serializer converts the second plurality of parallel data streams into the second serial data stream. The second serial data stream, in embodiments, includes trading data. Trading data, for example, may be any data related to purchasing or selling of stocks, commodities, goods, and/or services.

[0471] At a step S1230, the second serial data stream may be transmitted from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface. In embodiments, the second serial data stream is transmitted from the serializer on the field programmable gate array to an input/output module of the field gate array system but not on the field gate array. The second serial data stream may then be transmitted from the input/output module off the field gate array system.

[0472] FIGs 15A-C, 16A-B and 17 are exemplary flow charts of a process implementing the field programmable gate array system in accordance with yet another embodiment of the present invention. In embodiments, the process described in the flow charts of FIGs. 15A-C, 16A-B and 17 may be implemented by the field programmable gate array system shown in FIG. 3B or FIG. 5B. The field programmable gate array system, including the field programmable gate array and the components thereof, may be similar to the field programmable gate array systems of FIG. 3B and FIG. 5B, the descriptions of which applying herein.

[0473] The process of FIGs. 15A-15C may begin at step S1502. Referring to FIG. 15A, at step S1502, a first serial data stream is received by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system. In embodiments, the first serial data stream may include market data. In embodiments, market data may be price and trade-related data for a financial instrument reported by a trading venue (i.e., a stock exchange).

[0474] At a step S1504, a first clock signal having a first frequency and a first phase is received by a first reference clock pin in the first interface from a fixed frequency oscillator. In embodiments, step S1504 may be performed before step S1502. In embodiments, step S1504 may be performed contemporaneously with step S1502.

[0475] The process of FIGs. 15A-15C may continue with a step S1506. At step S1506, the first plurality of data pins of the first interface may transmit the first serial data stream to a deserializer in the field programmable gate array.

[0476] At a step S1508, the first reference clock pin in the first interface may transmit the first clock signal to the deserializer. In embodiments, step S1508 may be performed before step S1506. In embodiments step S1508 may be performed contemporaneously with step S1506.

[0477] At a step S1510, a first receiver side clock signal may be generated by the deserializer. In embodiments, the first receiver side clock signal may have a second frequency and a second phase. In embodiments, the second frequency is different from the first frequency. In embodiments, the second frequency corresponds to the first frequency. In embodiments, corresponding may refer to the frequencies being the same frequency. In embodiments corresponding may also refer to frequencies being close (e.g., within an acceptable range in the art) to the same frequencies. In embodiments, the first phase and the second phase may not be aligned. In embodiments the first phase and the second phase are aligned. In embodiments, a difference between the first phase and the second phase is below a threshold level. In embodiments, the deserializer generates the first receiver clock signal based at least in part on the first clock signal.

[0478] At a step S1512, the first serial data stream received by the deserializer may be converted, by the deserializer, into a first plurality of data streams. In embodiments, the first plurality of data streams may include a first amount of data streams. In embodiments, the first

amount of data streams is equal to eight (8) data streams. In embodiments, the first amount of data streams is equal to ten (10) data streams. In embodiments, the first amount of data streams is equal to sixteen (16) data streams. In embodiments, the first amount of data streams is equal to twenty (20) data streams. In embodiments, the first amount of data streams is equal to thirty-two (32) data streams. In embodiments, the first amount of data streams is equal to forty (40) data streams. In embodiments, the first amount of data streams is equal to sixty-four (64) data streams. In embodiments, the first amount of data streams is equal to eighty (80) data streams. In embodiments, the first amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the first amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the first amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the first amount of data streams is equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the first amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0479] At a step S1514, the first receiver side clock signal is transmitted from the deserializer to computational circuitry in the field programmable gate array.

[0480] At a step S1516, the first plurality of data streams is transmitted form the deserializer to the computational circuitry. In embodiments, the first plurality of data streams includes a first plurality of data items. In embodiments, step S1516 may be performed before step S1514. In embodiments step S1516 may be performed contemporaneously with step S1514.

[0481] At a step S1518, the first receiver side clock signal is transmitted from the deserializer to a phase detector of the field programmable gate array system, which may or may not be one the field programmable gate array. If the phase detector is not on the field programmable gate array, the first receiver side clock signal may be transmitted from the deserializer to the phase detector via a first clock output pin on a second interface of the field programmable gate array. In embodiments, the first receiver side clock signal may also be transmitted via a first zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the first clock output pin of the second interface.

[0482] At a step S1520, a first transmitter side clock signal is generated by the field programmable gate array system. In embodiments, the first transmitter side clock signal has a third frequency and a third phase. In embodiments, the third frequency corresponds to the second

frequency. In embodiments, the third phase may be aligned with the second phase. In embodiments, the third phase and the second phase may not be aligned. In embodiments, the third phase and the second phase may have a difference in phases that is less than a second threshold level. In embodiments, the first transmitter side clock signal is generated by performing the following steps until a first output of the phase detector is below a first threshold.

[0483] Referring to FIG. 16A, generating the first transmitter side clock signal may begin at step S1602. At step S1602, an adjustable transceiver phase lock loop receives the first clock signal from the fixed frequency oscillator via a second reference clock pin in the first interface. In embodiments, the received first clock signal is used by the adjustable transceiver phase lock loop to generate a second clock signal. In embodiments, the second clock signal may have a fourth frequency and a fourth phase.

[0484] The process of FIGs. 16A-B may continue at a step S1604. At step S1604, a first wire rate clock signal having a fifth phase and a fifth frequency is generated. In embodiments, the generation of the first wire rate clock signal may be based in part on the second clock signal. In embodiments the fifth frequency is a rational multiple of the fourth frequency. In embodiments the fifth frequency is equal to x times the fifth frequency where x is the second amount of data streams. In embodiments the fifth frequency is equal to x times the frequency of the of the transmitter side clock signal where x may be half of the second amount of data streams.

[0485] In embodiments, the generation of the first wire rate clock signal may be performed with the following steps. Referring to FIG. 17, at a step S1702, the second clock signal is generated by the adjustable transceiver phase lock loop based at least in part on the received first clock signal. At a step S1704, the second clock signal is processed by the adjustable transceiver phase lock loop based on the interim adjustment information received from the phase controller (see S1614 and S1616). As a step S1706, the first wire rate clock signal is provided by the adjustable transceiver phase lock look. The providing of the first wire rate clock signal, in embodiments, may be based at least in part on the processing of the second clock signal. Once the first wire rate clock signal is provided, at a step S1708. the first wire rate clock signal is transmitted by the adjustable transceiver phase lock loop to a serializer on the field programmable gate array. In embodiments, the first wire rate clock signal is generated by a phase lock loop. In embodiments, the phase lock loop that generates the first wire rate clock signal is on field programmable gate array. In

embodiments, the phase lock loop that generates the first wire rate clock signal is part of the field programmable gate array system and not part of the field programmable gate array.

[0486] In embodiments, the generation of the first wire rate clock signal may include processing the second clock signal. Once the second clock signal is processed, the first wire rate clock signal may be provided. The providing of the first wire rate clock signal, in embodiments, is based at least in part on the processing of the second clock signal. After providing the first wire rate clock signal, in embodiments, the first wire rate clock signal may be transmitted to the serializer.

[0487] Referring back to FIG. 16A, at a step 1606, an interim transmitter side clock signal having a sixth frequency and a sixth phase is generated by the serializer in the field programmable gate array. In embodiments, the sixth frequency corresponds to the third frequency. In embodiments the sixth phase may be aligned with the third phase. In embodiments, the sixth frequency may correspond to the third frequency and the sixth phase may not be aligned with the third phase. In embodiments, the sixth phase and the third phase may not be aligned. In embodiments, the third phase and the sixth phase may have a difference in phases that is less than a second threshold level.

[0488] At a step S1608, the interim transmitter side clock signal is transmitted from the serializer to the phase detector, which may or may not be on the field programmable gate array. If the phase detector is not on the field programmable gate array, the interim transmitter side clock signal may be transmitted from the serializer to the phase detector via a second clock output pin of the second interface. In embodiments, the interim transmitter side clock signal may also be transmitted a second zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the second clock output in of the second interface.

[0489] The process of FIGs. 16A-16B may continue with at a step S1610. Referring to FIG. 16B, at a step S1610, a first output is generated by the phase detector. The first output, in embodiments, is based at least on a comparison of the first receiver side clock signal and the interim side clock signal. The first output, in embodiments, may include information indicating the phase differences (if there is any) between the first receiver side clock and the interim side clock signal. Additionally, in embodiments, the first output may include information indicating a

difference (if there is any) of frequencies between the first receiver side clock signal and the interim side clock signal.

[0490] At a step S1612, the first output may be transmitted from the phase detector to a phase controller of the field programmable gate array system, which may be placed within the field programmable gate array.

[0491] At a step S1614, interim adjustment information is determined by the phase controller. In embodiments, the interim adjustment information may be based at least in part on the first output. For example, the interim adjustment information may indicate necessary adjustments to align the phases of the first receiver side clock signal and the interim side clock signal. As another example, the interim adjustment information may indicate necessary adjustments to align the frequencies of the first receiver side clock signal and the interim side clock signal.

[0492] At a step S1616, the interim adjustment information is transmitted from the phase controller to the adjustable transceiver phase lock loop. In embodiments, once the interim adjustment information is received, the adjustable transceiver phase lock loop adjusts the second clock signal based on the interim adjustment information. The adjustment of the second clock signal, in embodiments, may change the phase of the second clock signal. In embodiments, the interim adjustment information indicates a desired phase. In embodiments, the interim adjustment information indicates a desired frequency. In embodiments, the interim adjustment information indicates a change in phase. In embodiments, the interim adjustment information indicates a change in frequency. In embodiments, the adjustment information includes a voltage. In embodiments, the adjustment information includes a digital transmission. For example, the adjustment information may be a command over a serial bus (e.g., I2C or SPI) that adjusts a clock divider or phase rotator. As another example, the adjustment information may trigger a set of parallel digital wires for "frequency/phase up," "frequency/phase down," and/or "frequency/phase step." In embodiments, the adjustment of the second clock signal may change the frequency of the second clock signal.

[0493] In embodiments, steps S1602 through steps S 1016 are repeated until the first output of the phase detector is below the first threshold level. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have phases that are

aligned. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have frequencies that correspond to one another.

[0494] Referring back to FIG. 15B, once the first output of the phase detector is below a first threshold level, at a step S1522, the serializer may transmit the first transmitter side clock signal to the computational circuitry. At a step S1524, a first set of operations is performed by the computational circuitry on at least a portion of the first plurality of data items to generate a second plurality of data streams. In embodiments, the first operation includes a trading algorithm. In embodiments the trading algorithm may include the parsing the market data. Once the market data is parsed, mathematical operations are performed at a portion of the market data. After the mathematical operations are performed, order packets are generated using at least an output of the mathematical operations. In embodiments, the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

[0495] In embodiments, at least a portion of the first set of operations is performed prior to step S1522. In embodiments, at least a portion of the first set of operations is performed after step S1522. In embodiments, all of the first set of operations is performed after step S1522.

[0496] In embodiments, the second plurality of data streams may include a second amount of data streams. In embodiments, the second amount of data streams may be the same as the first amount of data streams. In embodiments, the second amount of data streams is equal to eight (8) data streams. In embodiments, the second amount of data streams is equal to ten (10) data streams. In embodiments, the second amount of data streams is equal to sixteen (16) data streams. In embodiments, the second amount of data streams is equal to twenty (20) data streams. In embodiments, the second amount of data streams is equal to thirty-two (32) data streams. In embodiments, the second amount of data streams is equal to forty (40) data streams. In embodiments, the second amount of data streams is equal to sixty-four (64) data streams. In embodiments, the second amount of data streams is equal to eighty (80) data streams. In embodiments, the second amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the second amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the second amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the second amount of data streams is equal to ten

(10) times two (2) to the power of N, where N is an integer. In embodiments the second amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0497] At a step S1526, the second plurality of data streams is transmitted from the computational circuitry to the serializer. Once received by the serializer, at a step S1528, the serializer converts the second plurality of parallel data streams into the second serial data stream. The second serial data stream, in embodiments, includes trading data. Trading data, for example, may be any data related to purchasing or selling of stocks, commodities, goods, and/or services.

[0498] At a step S1530, the second serial data stream may be transmitted from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface. In embodiments, the second serial data stream is transmitted from the serializer on the field programmable gate array to an input/output module of the field gate array system but not on the field gate array. The second serial data stream may then be transmitted from the input/output module off the field gate array system.

EXAMPLES

[0499] The following examples may be used to illustrate embodiments of the present invention. They are meant solely for illustration and not intended to be limiting.

EXAMPLE 1

[0500] In embodiments a trading algorithm may be applied in a crossing auction on an option exchange. In embodiments, a third serial data stream including target price information on a set of options contracts is provided as in input to the FPGA. In embodiments, the first serial stream includes market data includes bid, asks, trades and auction notifications. When an auction is announced, as indicated in the market data, the FPGA compares the announced auction price to its target price. In embodiments, the target price is stored in the FPGA and is provided via the third serial data stream. In embodiments, the target price may be generated using a suitable pricing model, e.g., Black Scholes model. When there is some overlap, the field programmable gate array generates and sends an order at its target price which is transmitted out of the FPGA in the second serial data stream. In embodiments, the target price information on a set of options contracts is streamed into the field programmable gate array as a simple set of triggers in the third serial data stream. The target price information, may include a linearization of the result of the Black Scholes

computation or some other model. The field programmable gate array may implement Black Scholes, and instead receive market data on the underlying a et as a secondary data stream.

EXAMPLE 2

[0501] Another example of a trading algorithm is "signal based". In embodiments, signals refer to a trigger that is activated when certain events happen. In embodiments, a signal may simply track a sale price which changes every time the market information indicates a sale has taken place. In embodiments, a signal may be used as a measure of book pressure to determine whether prices are likely to rise or fall. Some signals may be calculated quickly while others are calculated more slowly because they require more data over a longer period of time. In embodiments, order information may be based on a single signal or based on a plurality of signals. Signals depending on the historical behavior of a financial instrument are programmed into the field programmable gate array. A few simple and well-known examples of a signal here are moving averages of past prices or book pressure signals (looking for an imbalance in the order book). Signal-based trading involves receiving market data on the financial instrument, constructing the order book for that instrument, calculating a predicted price based on a pre-defined collection of signals, and sending an order if the signals indicate that the signal indicates that it is a favorable time to trade. A secondary data stream here could be used to enable or disable signals or to change signal parameter values. In embodiments, the secondary data stream may be omitted. An example of a signal-based trading system might be a system that updates the quotes for a market maker when a set of signals indicates that a large directional move in the price of a stock is coming. The parallel processing advantage shows up here more so than in the first example.

* * * * * * *

[0502] Now that embodiments of the present invention have been shown and described in detail, various modifications and improvements thereon can become readily apparent to those skilled in the art. Accordingly, the exemplary embodiments of the present invention, as set forth above, are intended to be illustrative, not limiting. The spirit and scope of the present invention is to be construed broadly.

CLAIMS

What is claimed is:

1. A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:

(a) receiving, by a deserializer in a field programmable array, a clock signal;

(b) receiving, by the deserializer, the first serial data stream;

(c) generating, by the deserializer, a receiver side clock signal;

(d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;

(e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;

(f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;

(g) generating, using the phase lock loop, a transmitter side clock signal;

(h) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams; and

(i) transmitting, from the field programmable gate array system, the second serial data stream, derived from the second plurality of parallel data streams,

wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

2. The method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the set of operations are associated with a trading algorithm.

3. The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.

4. The method of claim 1, wherein the set of operations includes at least one of the following:

(i) an arithmetic operation;

(ii) a logical operation;

(iii) a pipeline operation; and

(iv) a memory access operation.

5. The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed prior to step (g).

6. The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed after step (g).

7. The method of claim 1, wherein all of the set of operations performed in step (h) are performed after step (g).

8. The method of claim 1, wherein step (g) further comprises:

(i) generating, by the phase lock loop, a feedback clock signal associated with the transmitter side clock signal by performing the following steps until a first output of a phase detector of the field programmable gate array system is below a first threshold level:

(1) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal;

(2) generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal;

(3) transmitting, from the phase detector to a phase controller of the field programmable gate array system, the first output;

(4) determining, by the phase controller, interim adjustment information based on the first output; and

(5) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information;

wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information,

wherein steps (1) through (5) are repeated until the first output of the phase detector is below the first threshold level, and

wherein the transmitter side clock signal is associated with the second clock signal.

9. The method of claim 1, wherein the first plurality of data streams has the same number of data streams as the second plurality of data streams.

10. The method of claim 1, wherein the first plurality of data streams and the second plurality of data streams comprise one of the following:

(i) eight (8) data streams;

(ii) ten (10) data streams;

(iii) sixteen (16) data streams;

(iv) twenty (20) data streams;

(v) thirty-two (32) data streams;

(vi) forty (40) data streams;

(vii) sixty-four (64) data streams;

(viii) eighty (80) data streams;

(ix) one hundred twenty-eight (128) data streams; and

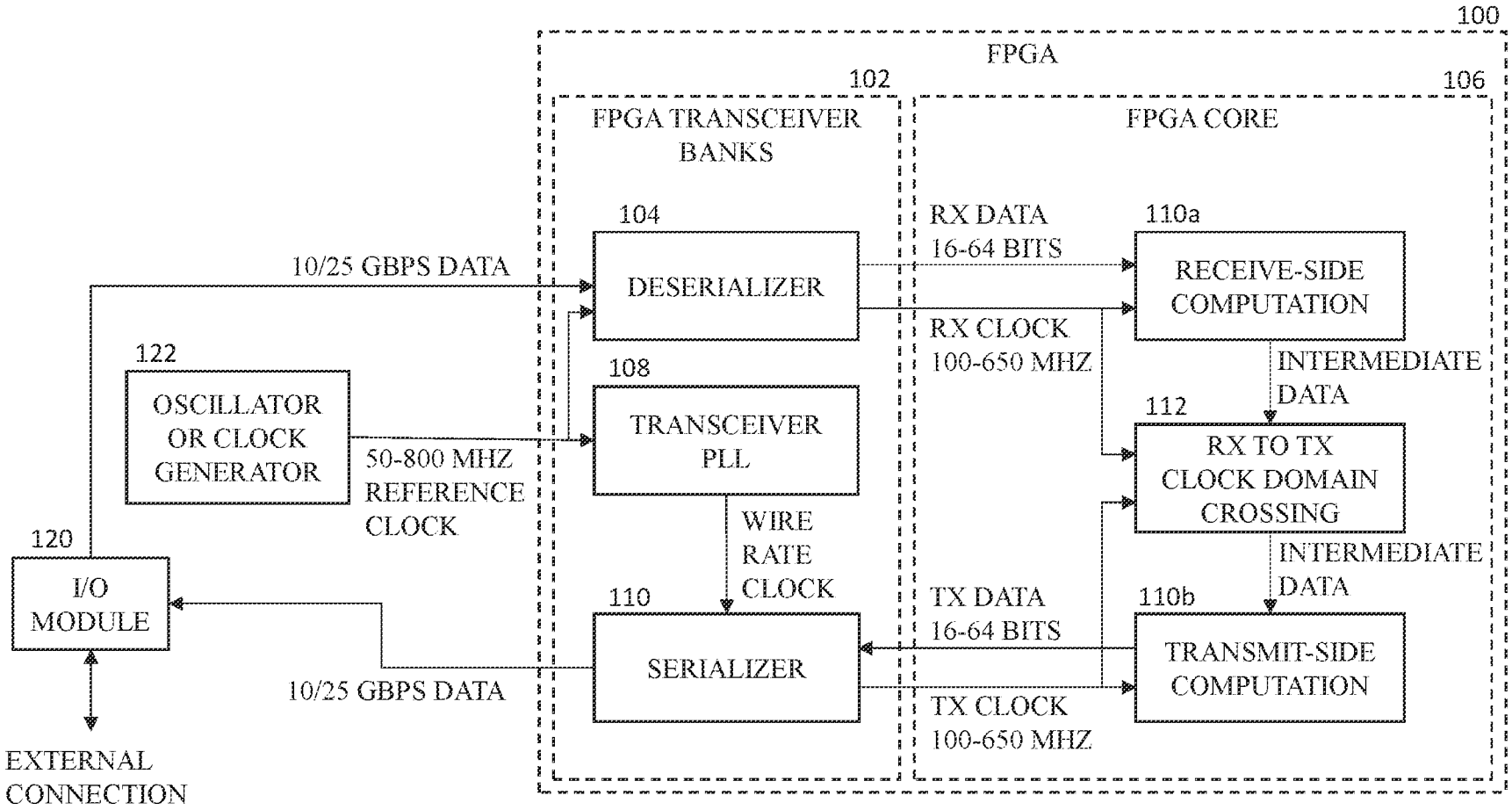
(x) one hundred sixty (160) data streams.

11. The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and phase.

12. The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and different phases.

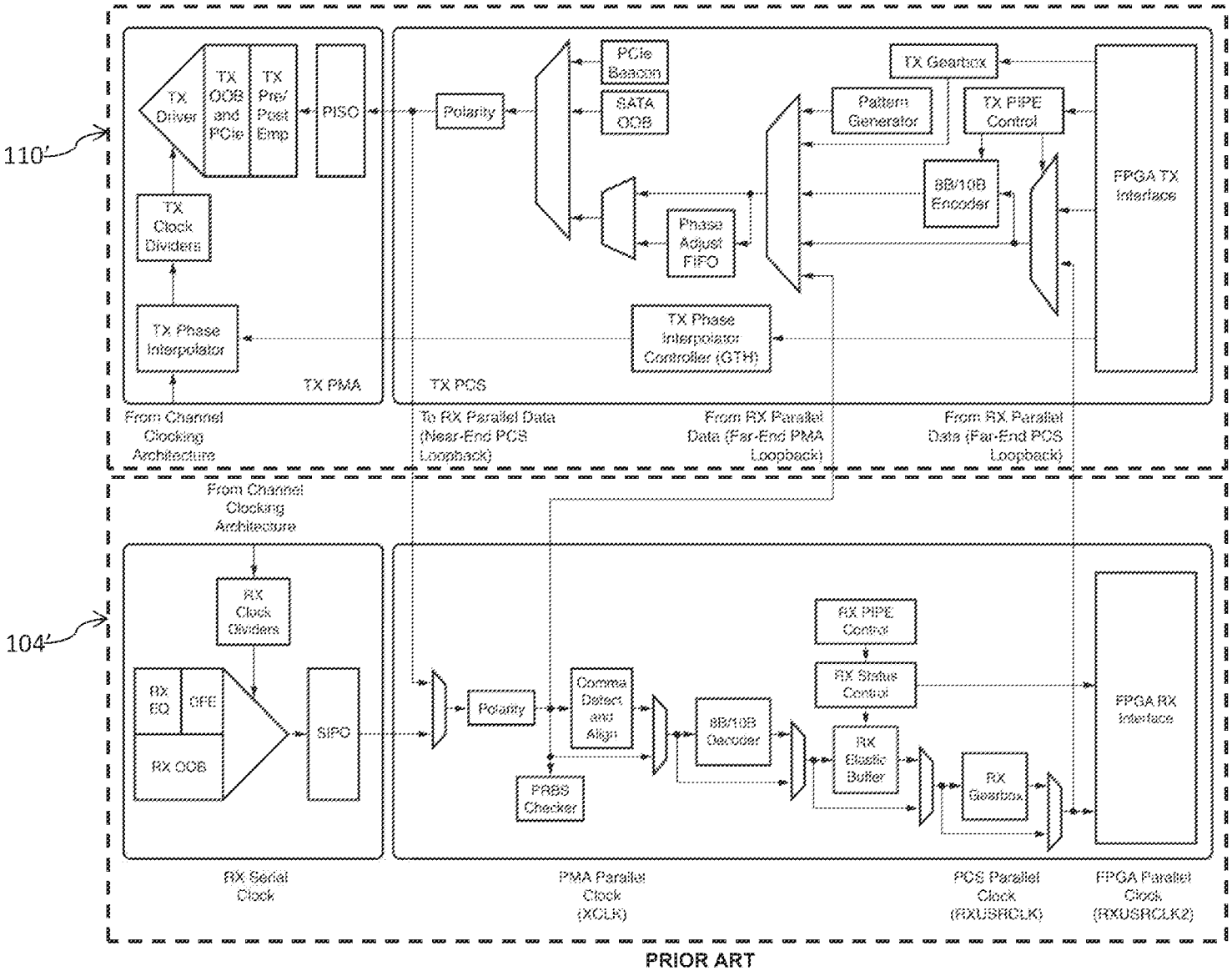
ABSTRACT

The present invention relates to a field programmable gate array system that provides phase control with minimal latency.



PRIOR ART

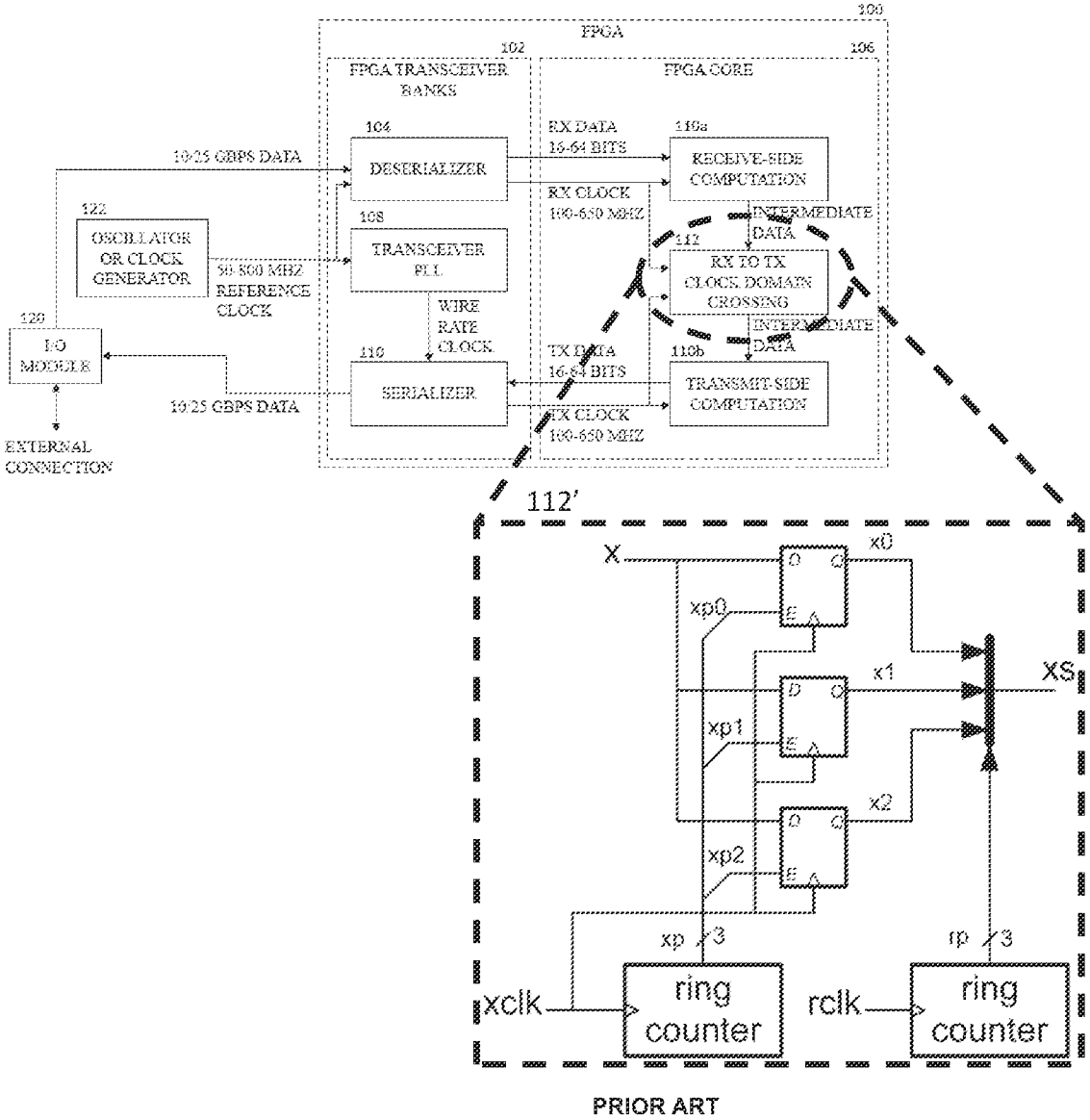
FIG. 1



PRIOR ART

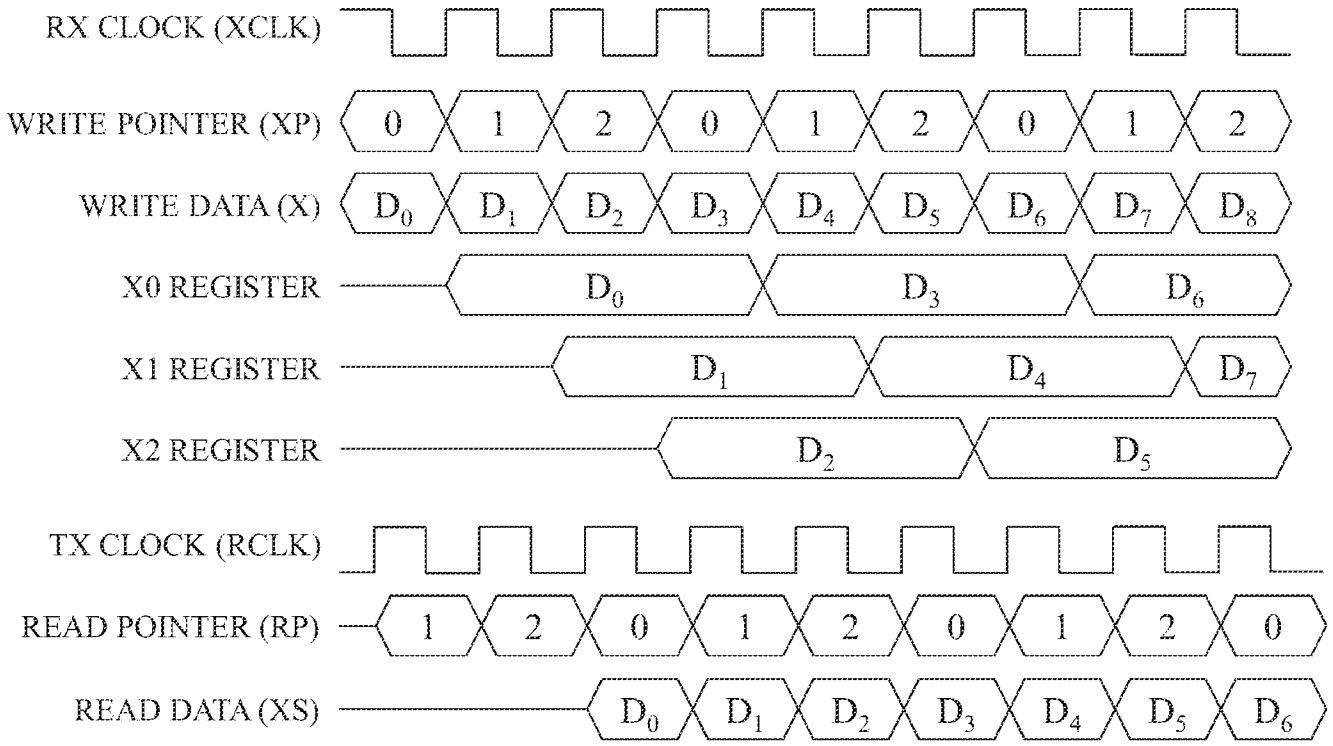
FIG. 1A

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PRIOR ART

FIG. 1B



PRIOR ART

FIG. 1C

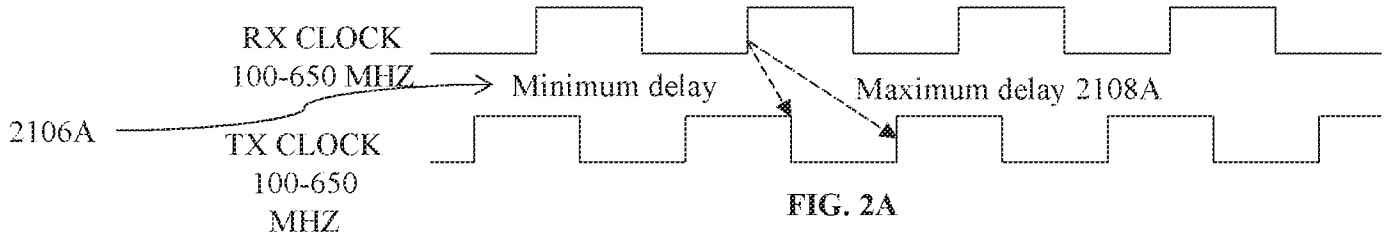


FIG. 2A

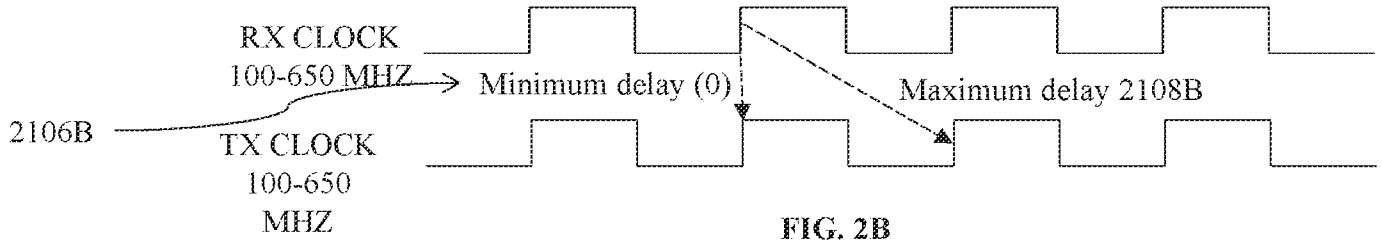


FIG. 2B

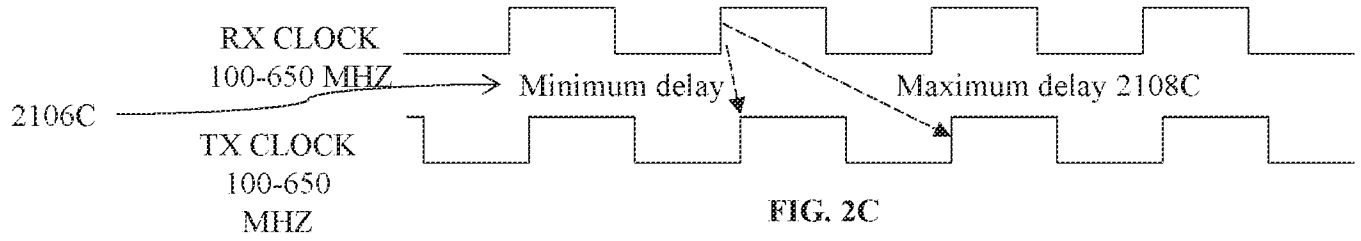


FIG. 2C

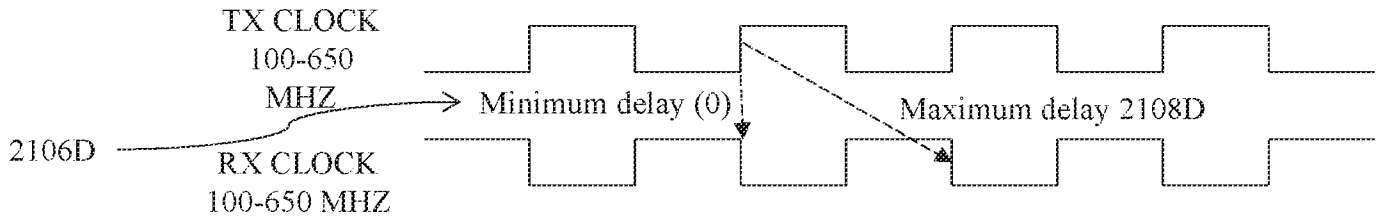


FIG. 2D

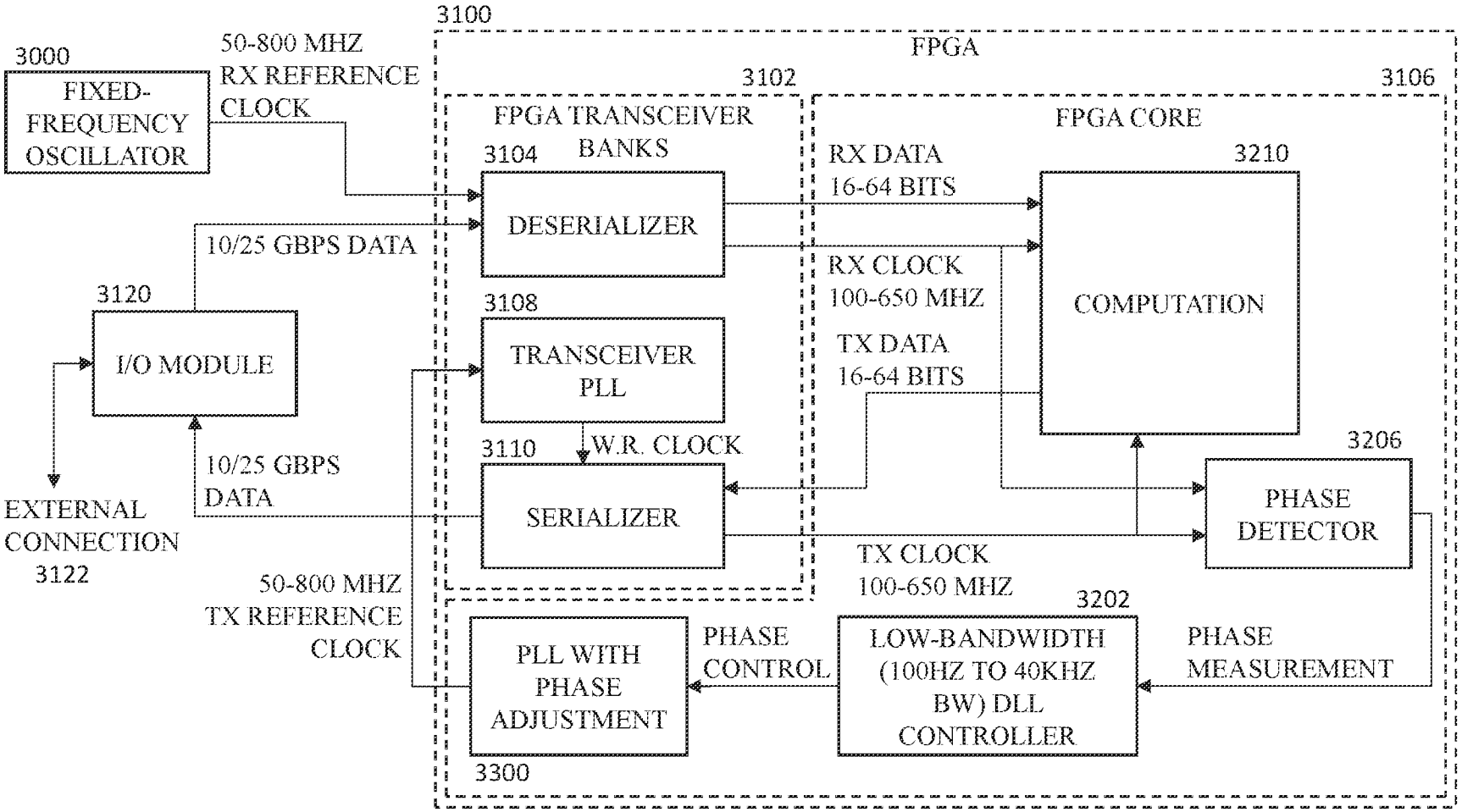

3100
FPGA
3000
FIXED-FREQUENCY OSCILLATOR
50-800 MHZ RX REFERENCE CLOCK
3102
FPGA TRANSCEIVER BANKS
3104
DESERIALIZER
10/25 GBPS DATA
3120
I/O MODULE
3108
TRANSCEIVER PLL
W.R. CLOCK
3110
SERIALIZER
10/25 GBPS DATA
EXTERNAL CONNECTION
3122
50-800 MHZ TX REFERENCE CLOCK
3106
FPGA CORE
RX DATA 16-64 BITS
3210
COMPUTATION
RX CLOCK 100-650 MHZ
TX DATA 16-64 BITS
3206
PHASE DETECTOR
TX CLOCK 100-650 MHZ
3202
LOW-BANDWIDTH (100HZ TO 40KHZ BW) DLL CONTROLLER
PHASE CONTROL
PHASE MEASUREMENT
PLL WITH PHASE ADJUSTMENT
3300

FIG. 3A

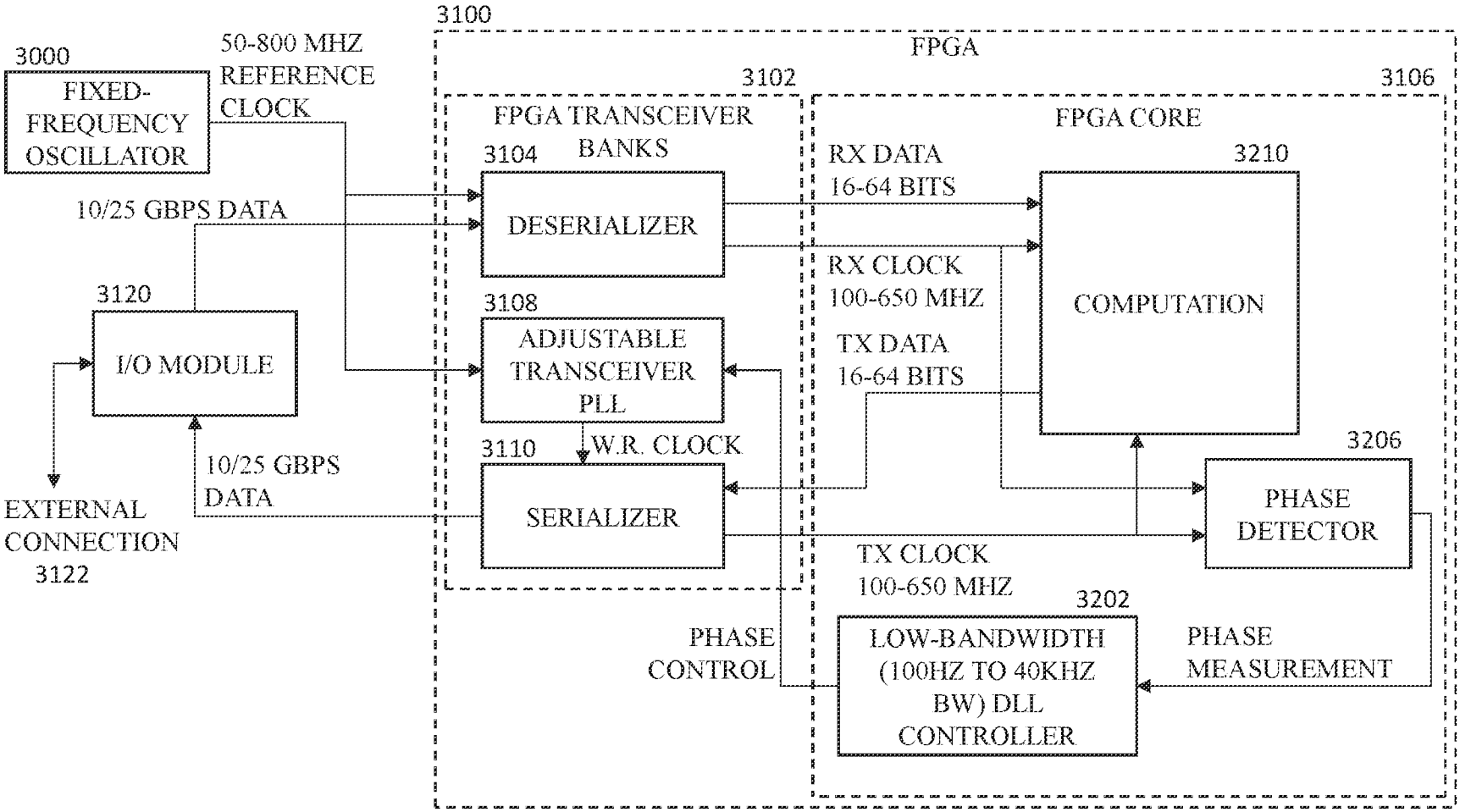

3100
FPGA
3000
FIXED-FREQUENCY OSCILLATOR
50-800 MHZ REFERENCE CLOCK
3102
FPGA TRANSCEIVER BANKS
3104
DESERIALIZER
10/25 GBPS DATA
3120
I/O MODULE
3108
ADJUSTABLE TRANSCEIVER PLL
3110
W.R. CLOCK
SERIALIZER
10/25 GBPS DATA
EXTERNAL CONNECTION
3122
3106
FPGA CORE
RX DATA
16-64 BITS
3210
COMPUTATION
RX CLOCK
100-650 MHZ
TX DATA
16-64 BITS
3206
PHASE DETECTOR
TX CLOCK
100-650 MHZ
3202
LOW-BANDWIDTH (100HZ TO 40KHZ BW) DLL CONTROLLER
PHASE CONTROL
PHASE MEASUREMENT

FIG. 3B

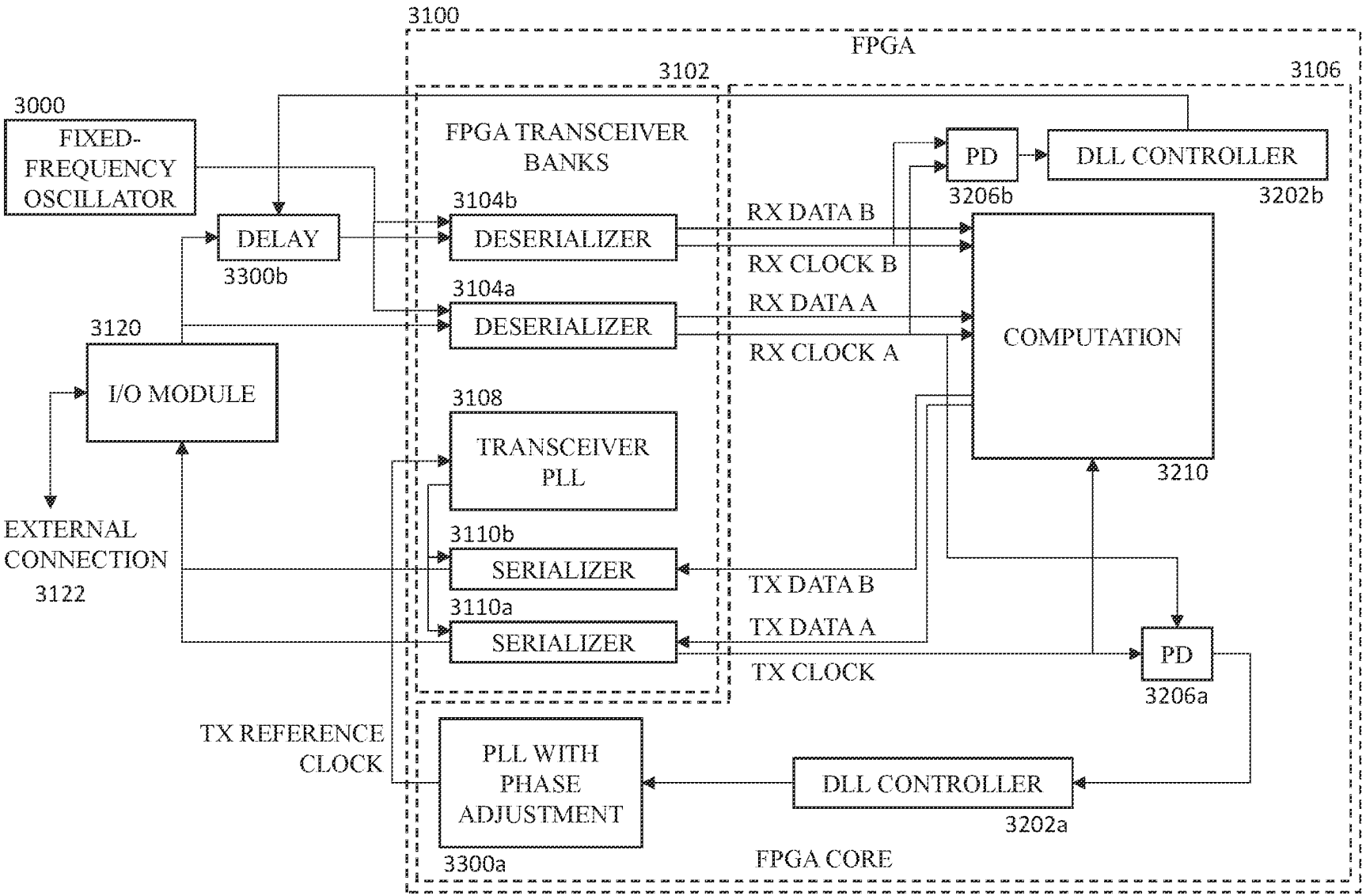

3100
FPGA
3102
3106
3000
FIXED-FREQUENCY OSCILLATOR
FPGA TRANSCEIVER BANKS
PD
3206b
DLL CONTROLLER
3202b
3104b
DELAY
3300b
DESERIALIZER
RX DATA B
RX CLOCK B
3104a
RX DATA A
DESERIALIZER
RX CLOCK A
3120
COMPUTATION
I/O MODULE
3108
TRANSCEIVER PLL
3210
EXTERNAL CONNECTION
3122
3110b
SERIALIZER
TX DATA B
3110a
TX DATA A
SERIALIZER
TX CLOCK
PD
3206a
TX REFERENCE CLOCK
PLL WITH PHASE ADJUSTMENT
DLL CONTROLLER
3202a
3300a
FPGA CORE

FIG. 3C

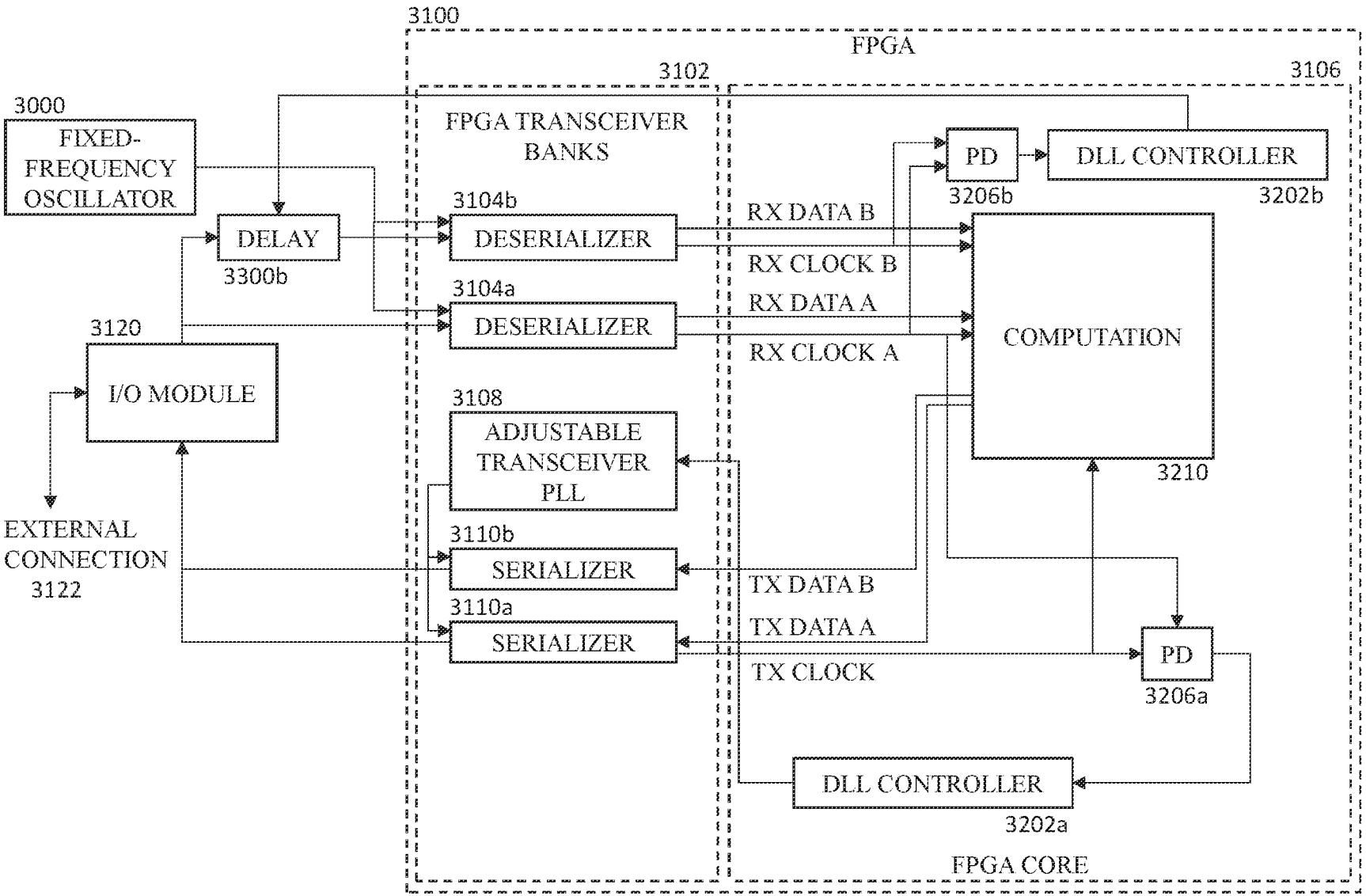

3100
FPGA
3102
3106
3000
FIXED-FREQUENCY OSCILLATOR
FPGA TRANSCEIVER BANKS
PD
3206b
DLL CONTROLLER
3202b
DELAY
3300b
3104b
DESERIALIZER
RX DATA B
RX CLOCK B
3104a
DESERIALIZER
RX DATA A
RX CLOCK A
COMPUTATION
3210
3120
I/O MODULE
3108
ADJUSTABLE TRANSCEIVER PLL
EXTERNAL CONNECTION
3122
3110b
SERIALIZER
TX DATA B
3110a
SERIALIZER
TX DATA A
TX CLOCK
PD
3206a
DLL CONTROLLER
3202a
FPGA CORE

FIG. 3D

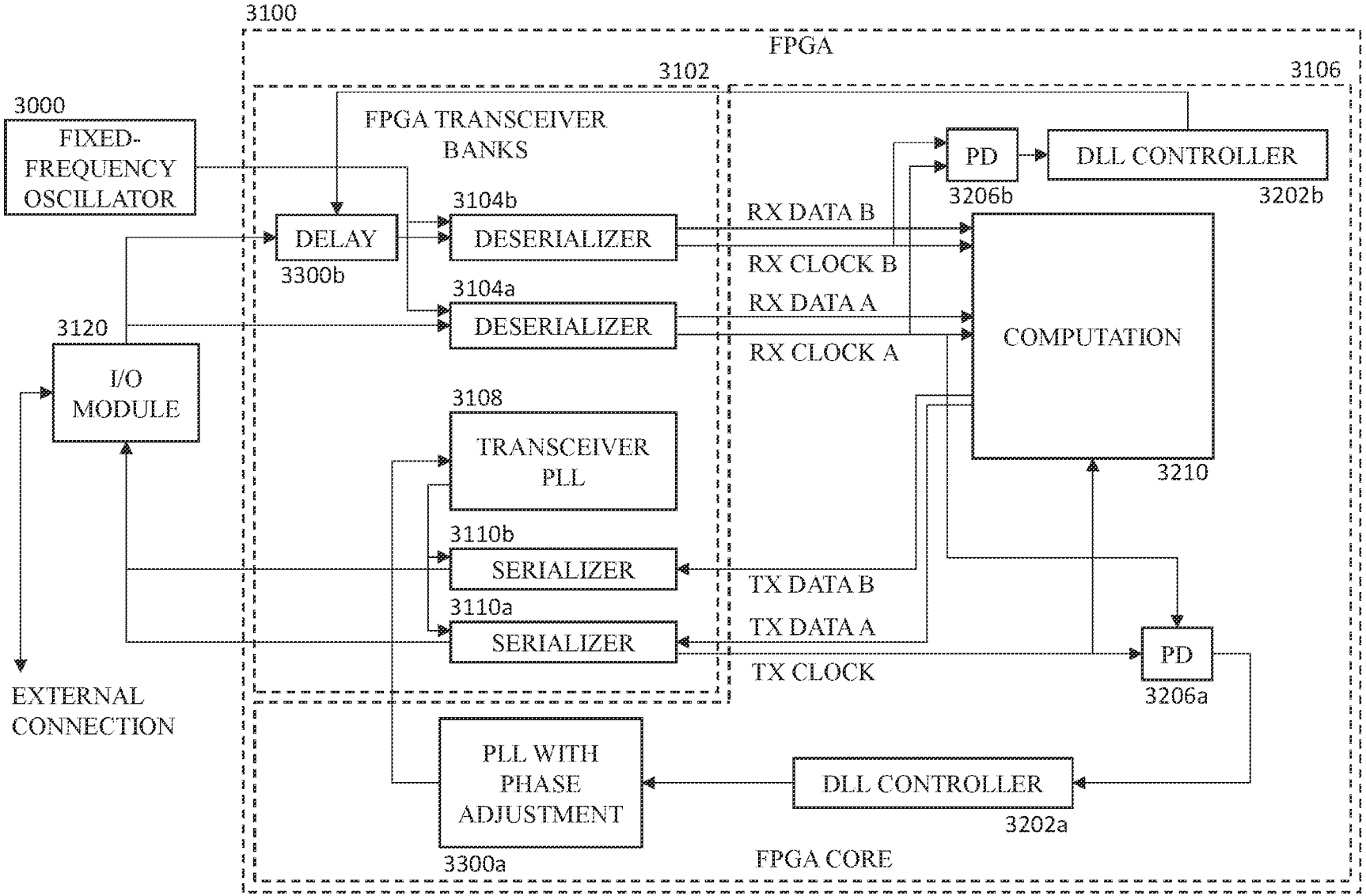

3100
FPGA
3102
3106
3000
FIXED-FREQUENCY OSCILLATOR
FPGA TRANSCEIVER BANKS
PD
3206b
DLL CONTROLLER
3202b
3104b
DELAY
3300b
DESERIALIZER
RX DATA B
RX CLOCK B
3104a
DESERIALIZER
RX DATA A
RX CLOCK A
COMPUTATION
3210
3120
I/O MODULE
3108
TRANSCEIVER PLL
3110b
SERIALIZER
TX DATA B
3110a
SERIALIZER
TX DATA A
TX CLOCK
PD
3206a
EXTERNAL CONNECTION
PLL WITH PHASE ADJUSTMENT
3300a
DLL CONTROLLER
3202a
FPGA CORE

FIG. 3E

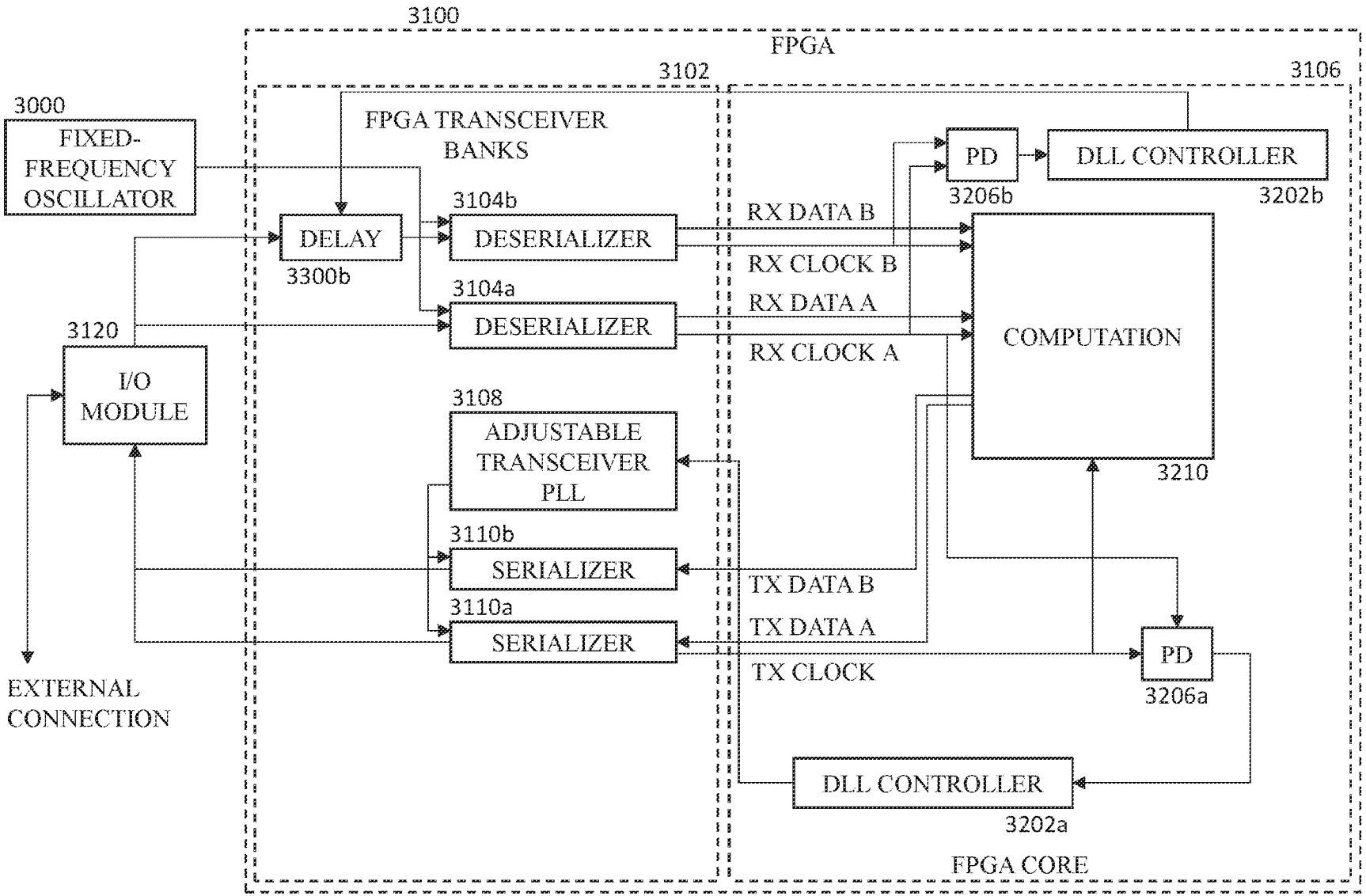

3100
FPGA
3102
3106
3000
FIXED-FREQUENCY OSCILLATOR
FPGA TRANSCEIVER BANKS
DELAY
3300b
3104b
DESERIALIZER
3104a
DESERIALIZER
3120
I/O MODULE
EXTERNAL CONNECTION
3108
ADJUSTABLE TRANSCEIVER PLL
3110b
SERIALIZER
3110a
SERIALIZER
RX DATA B
RX CLOCK B
RX DATA A
RX CLOCK A
TX DATA B
TX DATA A
TX CLOCK
PD
3206b
DLL CONTROLLER
3202b
COMPUTATION
3210
PD
3206a
DLL CONTROLLER
3202a
FPGA CORE

FIG. 3F

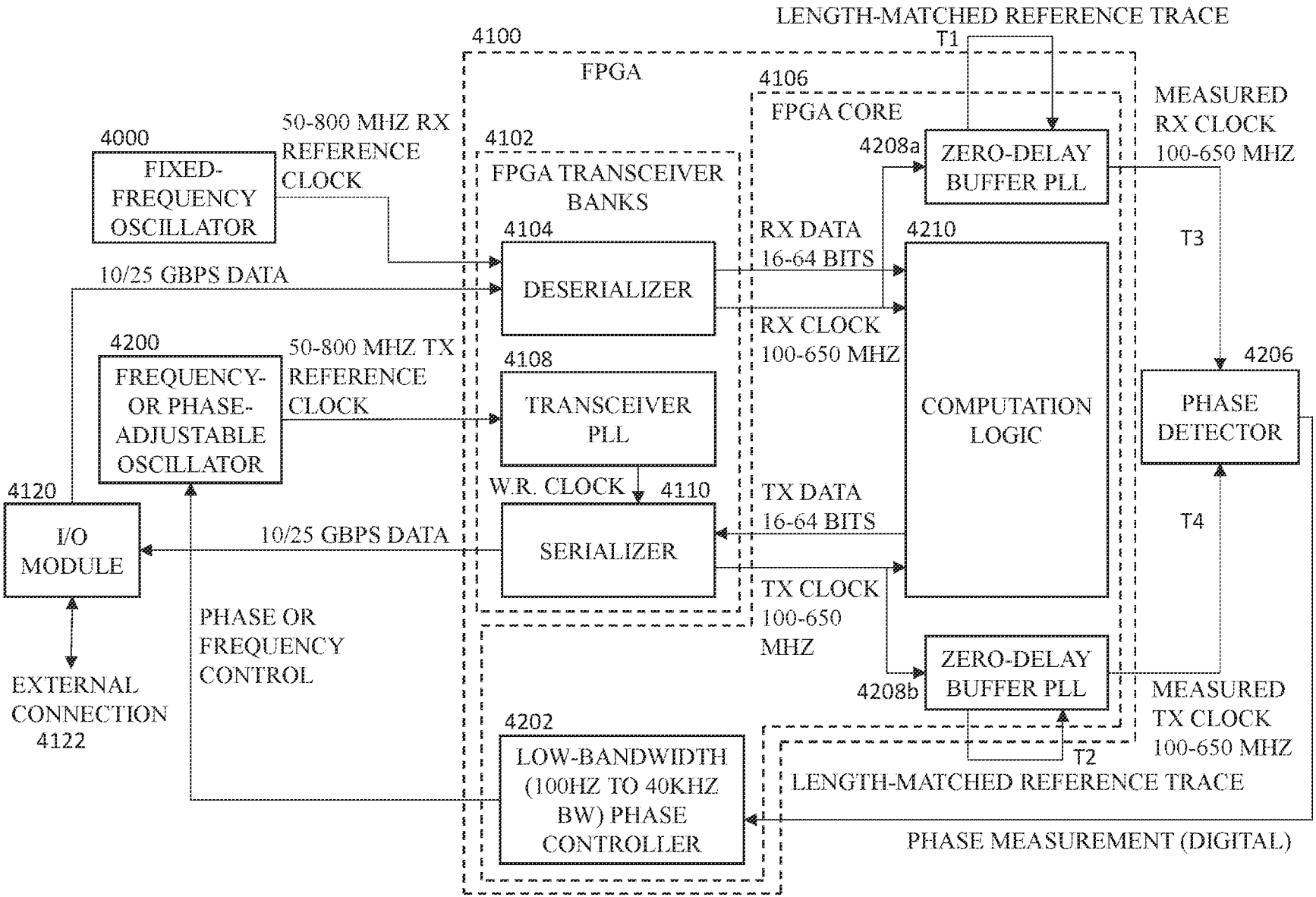

LENGTH-MATCHED REFERENCE TRACE
T1
4100
FPGA
4106
FPGA CORE
MEASURED
RX CLOCK
100-650 MHZ
4000
FIXED-
FREQUENCY
OSCILLATOR
50-800 MHZ RX
REFERENCE
CLOCK
4102
FPGA TRANSCEIVER
BANKS
4208a
ZERO-DELAY
BUFFER PLL
4104
DESERIALIZER
RX DATA
16-64 BITS
4210
T3
10/25 GBPS DATA
RX CLOCK
100-650 MHZ
4200
FREQUENCY-
OR PHASE-
ADJUSTABLE
OSCILLATOR
50-800 MHZ TX
REFERENCE
CLOCK
4108
TRANSCEIVER
PLL
COMPUTATION
LOGIC
4206
PHASE
DETECTOR
W.R. CLOCK
4110
4120
I/O
MODULE
10/25 GBPS DATA
SERIALIZER
TX DATA
16-64 BITS
T4
TX CLOCK
100-650
MHZ
PHASE OR
FREQUENCY
CONTROL
4208b
ZERO-DELAY
BUFFER PLL
MEASURED
TX CLOCK
100-650 MHZ
EXTERNAL
CONNECTION
4122
4202
T2
LENGTH-MATCHED REFERENCE TRACE
LOW-BANDWIDTH
(100HZ TO 40KHZ
BW) PHASE
CONTROLLER
PHASE MEASUREMENT (DIGITAL)

FIG. 4A

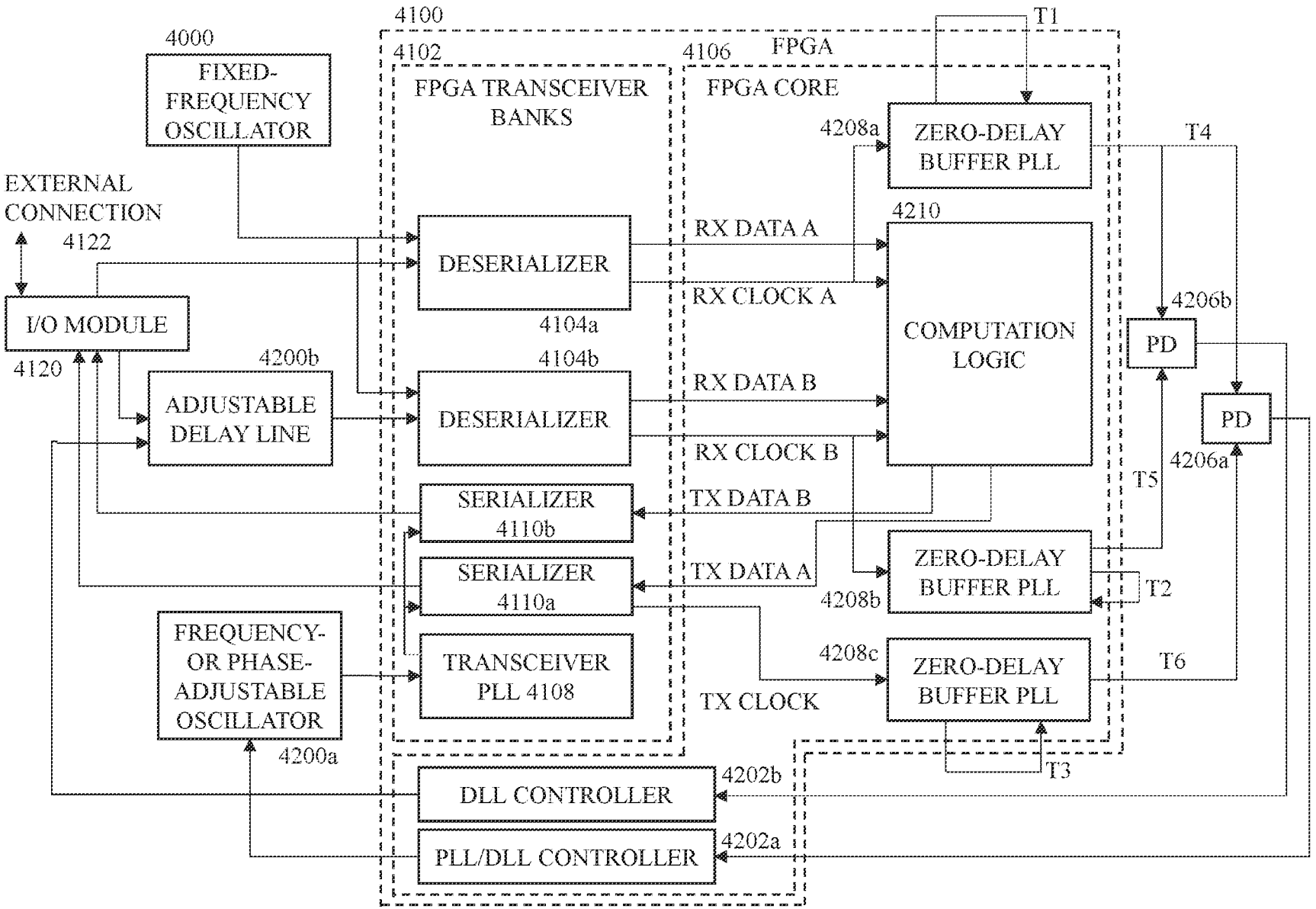

4100
4000
FIXED-FREQUENCY OSCILLATOR
4102
FPGA TRANSCEIVER BANKS
4106
FPGA
FPGA CORE
T1
4208a
ZERO-DELAY BUFFER PLL
T4
EXTERNAL CONNECTION
4122
4210
RX DATA A
DESERIALIZER
RX CLOCK A
4104a
COMPUTATION LOGIC
4206b
PD
I/O MODULE
4120
4200b
4104b
ADJUSTABLE DELAY LINE
RX DATA B
DESERIALIZER
RX CLOCK B
PD
4206a
T5
SERIALIZER 4110b
TX DATA B
SERIALIZER 4110a
TX DATA A
ZERO-DELAY BUFFER PLL
4208b
T2
FREQUENCY- OR PHASE-ADJUSTABLE OSCILLATOR
4200a
TRANSCEIVER PLL 4108
4208c
ZERO-DELAY BUFFER PLL
T6
TX CLOCK
T3
4202b
DLL CONTROLLER
4202a
PLL/DLL CONTROLLER

FIG. 4B

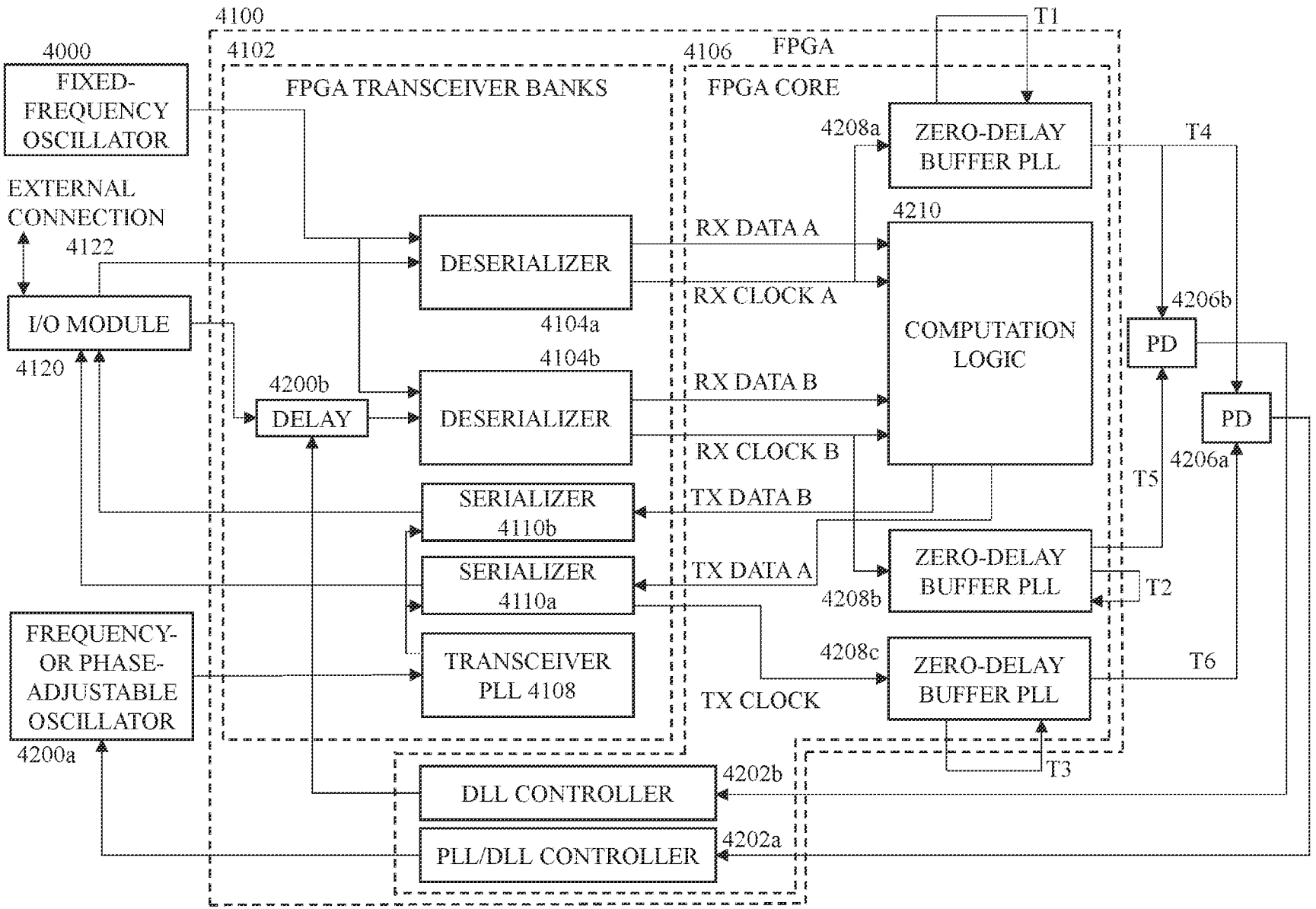

4100
4000
4102
4106
FPGA
FIXED-FREQUENCY OSCILLATOR
FPGA TRANSCEIVER BANKS
FPGA CORE
T1
4208a
ZERO-DELAY BUFFER PLL
T4
EXTERNAL CONNECTION
4122
DESERIALIZER
RX DATA A
4210
RX CLOCK A
4206b
I/O MODULE
4104a
COMPUTATION LOGIC
PD
4120
4104b
4200b
RX DATA B
DELAY
DESERIALIZER
PD
RX CLOCK B
4206a
T5
SERIALIZER 4110b
TX DATA B
SERIALIZER 4110a
TX DATA A
ZERO-DELAY BUFFER PLL
4208b
T2
FREQUENCY- OR PHASE-ADJUSTABLE OSCILLATOR
TRANSCEIVER PLL 4108
4208c
ZERO-DELAY BUFFER PLL
T6
TX CLOCK
4200a
T3
4202b
DLL CONTROLLER
4202a
PLL/DLL CONTROLLER

FIG. 4C

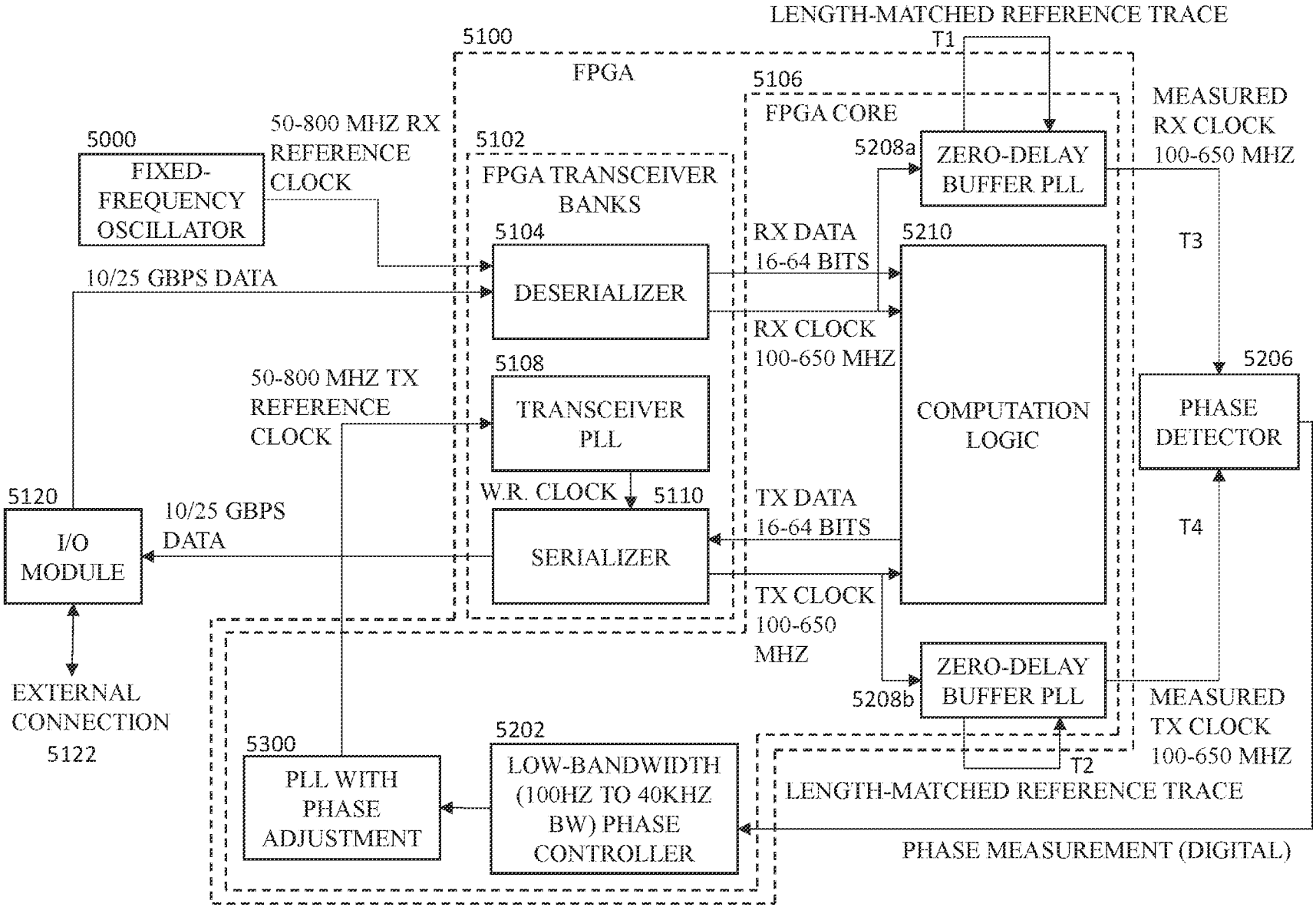

LENGTH-MATCHED REFERENCE TRACE
T1
5100
FPGA
5106
FPGA CORE
MEASURED
RX CLOCK
100-650 MHZ
5000
FIXED-
FREQUENCY
OSCILLATOR
50-800 MHZ RX
REFERENCE
CLOCK
5102
FPGA TRANSCEIVER
BANKS
5208a
ZERO-DELAY
BUFFER PLL
5104
DESERIALIZER
RX DATA
16-64 BITS
5210
T3
10/25 GBPS DATA
RX CLOCK
100-650 MHZ
5206
50-800 MHZ TX
REFERENCE
CLOCK
5108
TRANSCEIVER
PLL
COMPUTATION
LOGIC
PHASE
DETECTOR
5120
I/O
MODULE
10/25 GBPS
DATA
W.R. CLOCK
5110
SERIALIZER
TX DATA
16-64 BITS
T4
TX CLOCK
100-650
MHZ
ZERO-DELAY
BUFFER PLL
5208b
EXTERNAL
CONNECTION
5122
MEASURED
TX CLOCK
100-650 MHZ
5202
5300
T2
LENGTH-MATCHED REFERENCE TRACE
PLL WITH
PHASE
ADJUSTMENT
LOW-BANDWIDTH
(100HZ TO 40KHZ
BW) PHASE
CONTROLLER
PHASE MEASUREMENT (DIGITAL)

FIG. 5A

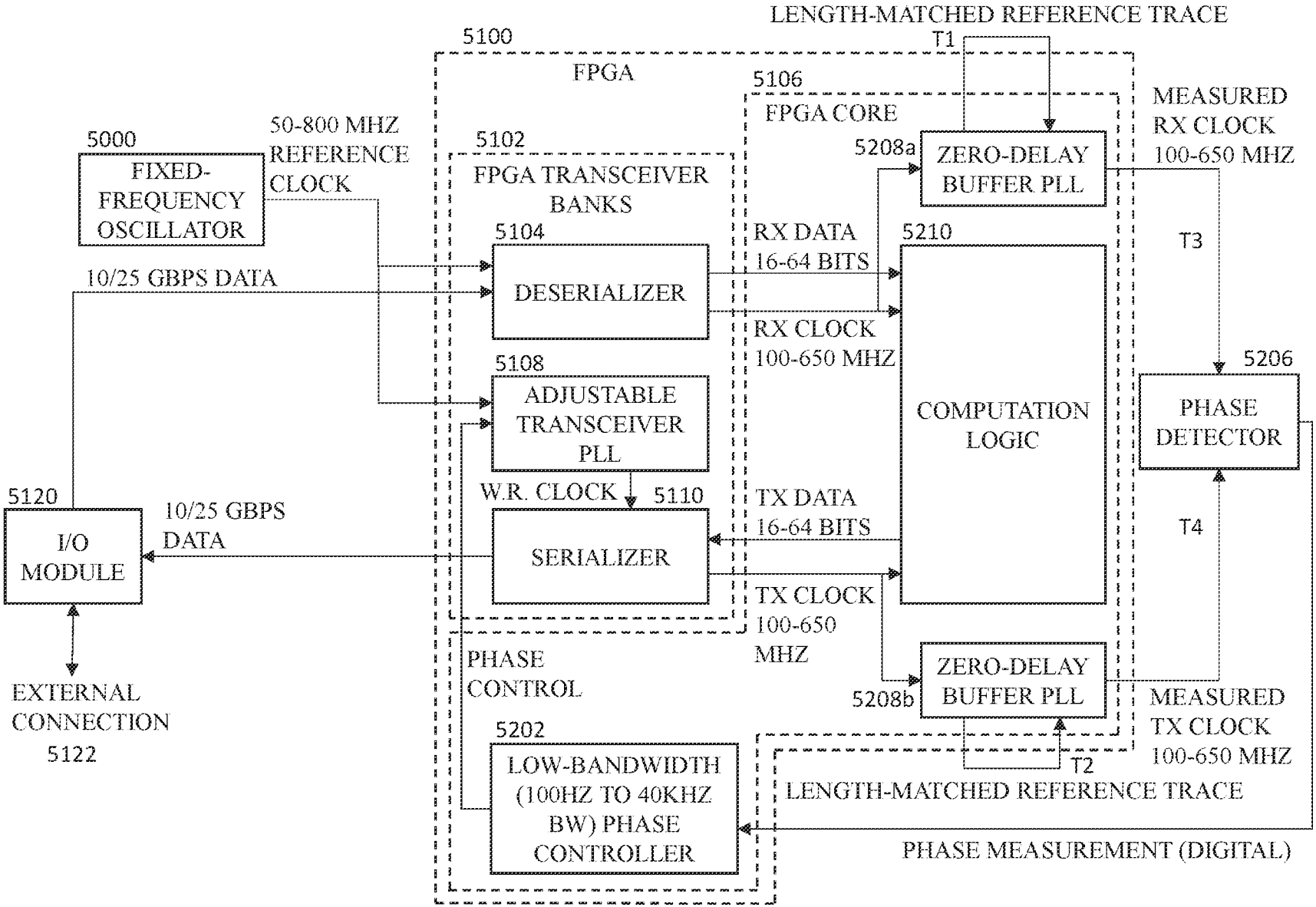

LENGTH-MATCHED REFERENCE TRACE
T1
5100
FPGA
5106
FPGA CORE
MEASURED
RX CLOCK
100-650 MHZ
5000
FIXED-
FREQUENCY
OSCILLATOR
50-800 MHZ
REFERENCE
CLOCK
5102
FPGA TRANSCEIVER
BANKS
5208a
ZERO-DELAY
BUFFER PLL
5104
DESERIALIZER
RX DATA
16-64 BITS
5210
T3
10/25 GBPS DATA
RX CLOCK
100-650 MHZ
5108
ADJUSTABLE
TRANSCEIVER
PLL
5206
PHASE
DETECTOR
COMPUTATION
LOGIC
5120
I/O
MODULE
10/25 GBPS
DATA
W.R. CLOCK
5110
SERIALIZER
TX DATA
16-64 BITS
T4
TX CLOCK
100-650
MHZ
PHASE
CONTROL
ZERO-DELAY
BUFFER PLL
5208b
MEASURED
TX CLOCK
100-650 MHZ
EXTERNAL
CONNECTION
5122
5202
LOW-BANDWIDTH
(100HZ TO 40KHZ
BW) PHASE
CONTROLLER
T2
LENGTH-MATCHED REFERENCE TRACE
PHASE MEASUREMENT (DIGITAL)

FIG. 5B

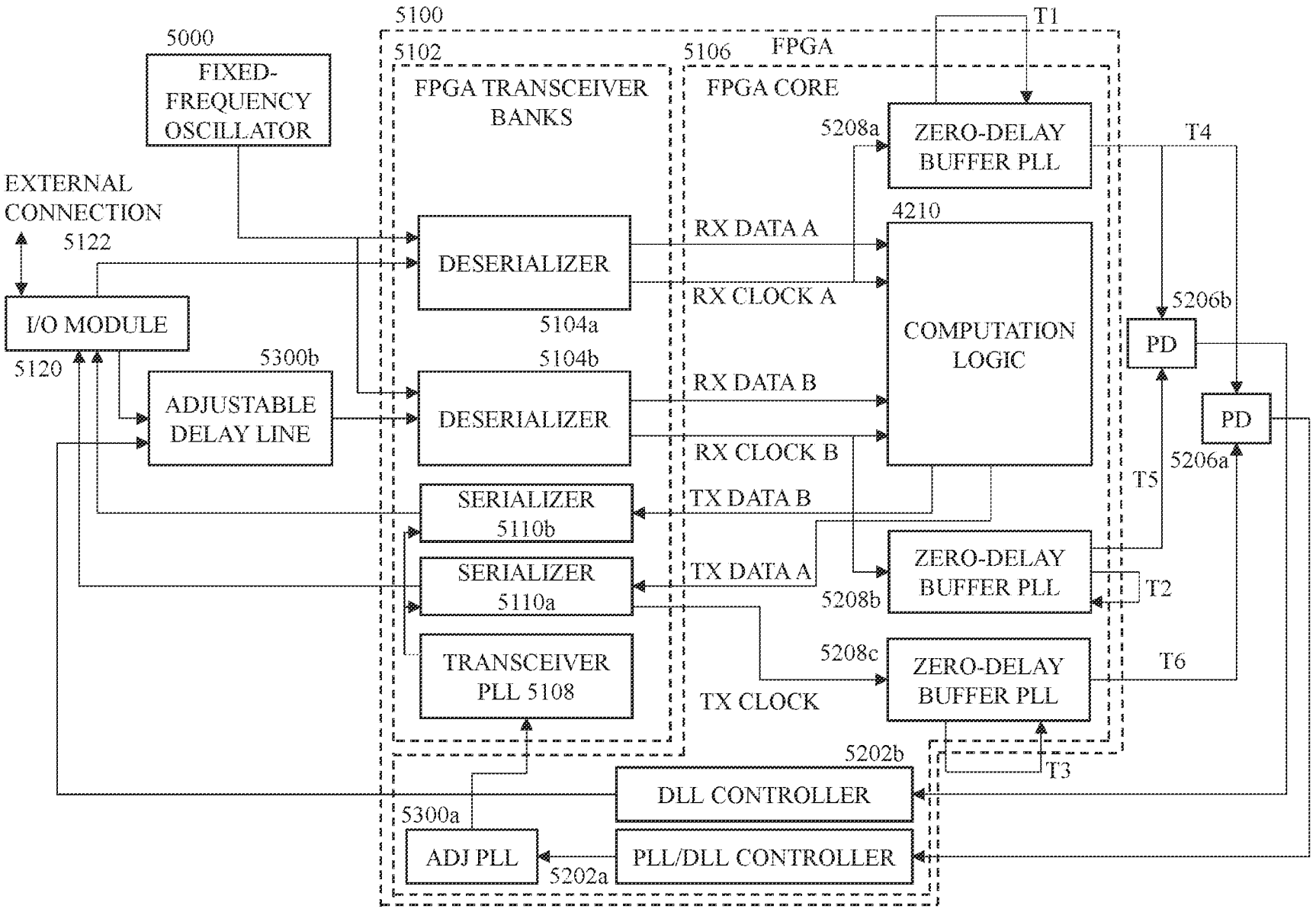

5100
T1
5000
5102
5106
FPGA
FIXED-FREQUENCY OSCILLATOR
FPGA TRANSCEIVER BANKS
FPGA CORE
5208a
ZERO-DELAY BUFFER PLL
T4
EXTERNAL CONNECTION
5122
4210
RX DATA A
DESERIALIZER
RX CLOCK A
5206b
I/O MODULE
5104a
COMPUTATION LOGIC
PD
5120
5300b
5104b
RX DATA B
ADJUSTABLE DELAY LINE
DESERIALIZER
PD
RX CLOCK B
5206a
T5
SERIALIZER 5110b
TX DATA B
SERIALIZER 5110a
TX DATA A
ZERO-DELAY BUFFER PLL
5208b
T2
5208c
TRANSCEIVER PLL 5108
ZERO-DELAY BUFFER PLL
T6
TX CLOCK
5202b
T3
DLL CONTROLLER
5300a
ADJ PLL
PLL/DLL CONTROLLER
5202a

FIG. 5C

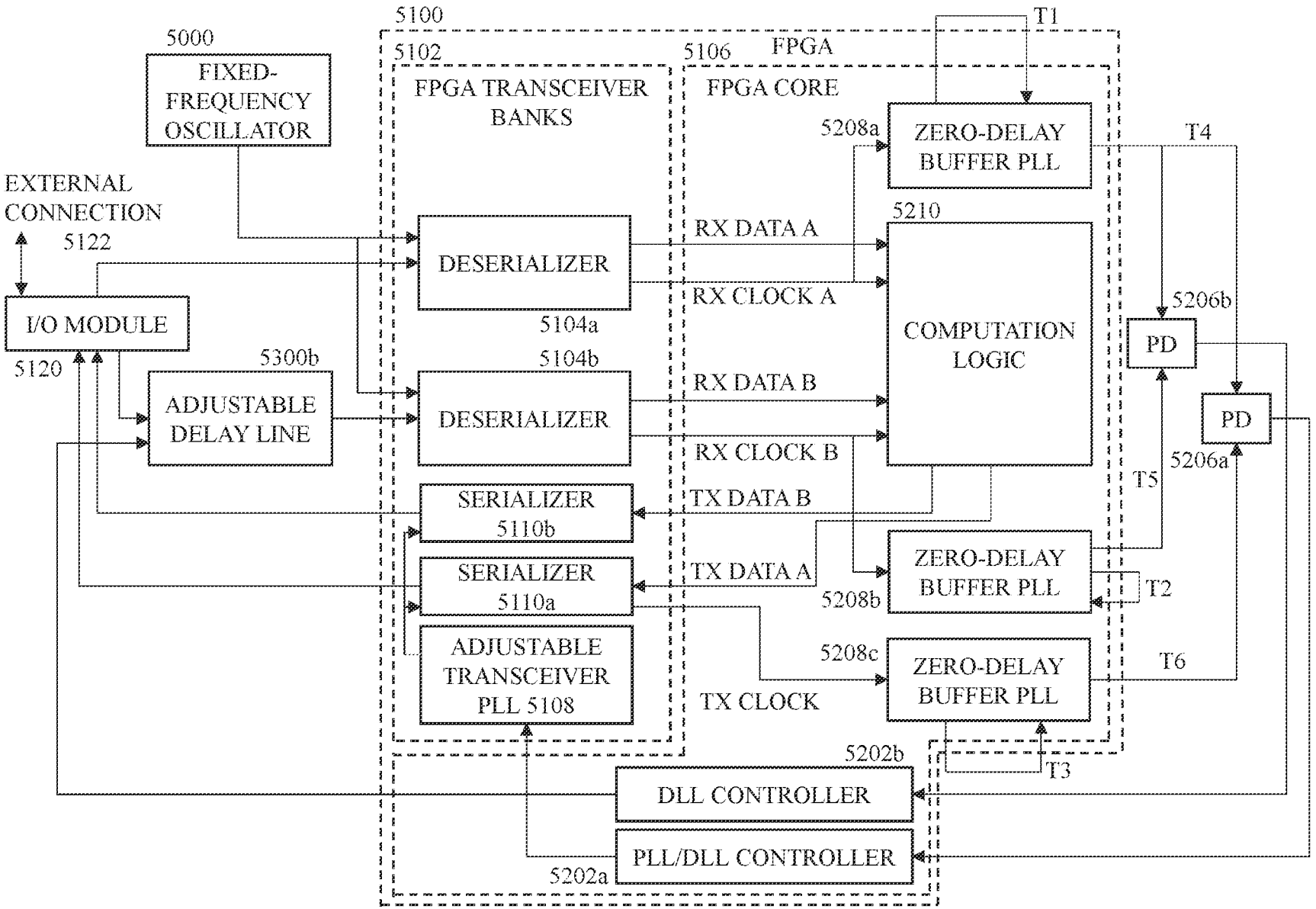

5100
T1
5000
FIXED-FREQUENCY OSCILLATOR
5102
FPGA TRANSCEIVER BANKS
5106
FPGA
FPGA CORE
5208a
ZERO-DELAY BUFFER PLL
T4
EXTERNAL CONNECTION
5122
5210
RX DATA A
DESERIALIZER
RX CLOCK A
5206b
I/O MODULE
5104a
COMPUTATION LOGIC
PD
5120
5300b
5104b
RX DATA B
ADJUSTABLE DELAY LINE
DESERIALIZER
PD
RX CLOCK B
5206a
T5
SERIALIZER 5110b
TX DATA B
SERIALIZER 5110a
TX DATA A
ZERO-DELAY BUFFER PLL
5208b
T2
ADJUSTABLE TRANSCEIVER PLL 5108
5208c
ZERO-DELAY BUFFER PLL
T6
TX CLOCK
5202b
T3
DLL CONTROLLER
PLL/DLL CONTROLLER
5202a

FIG. 5D

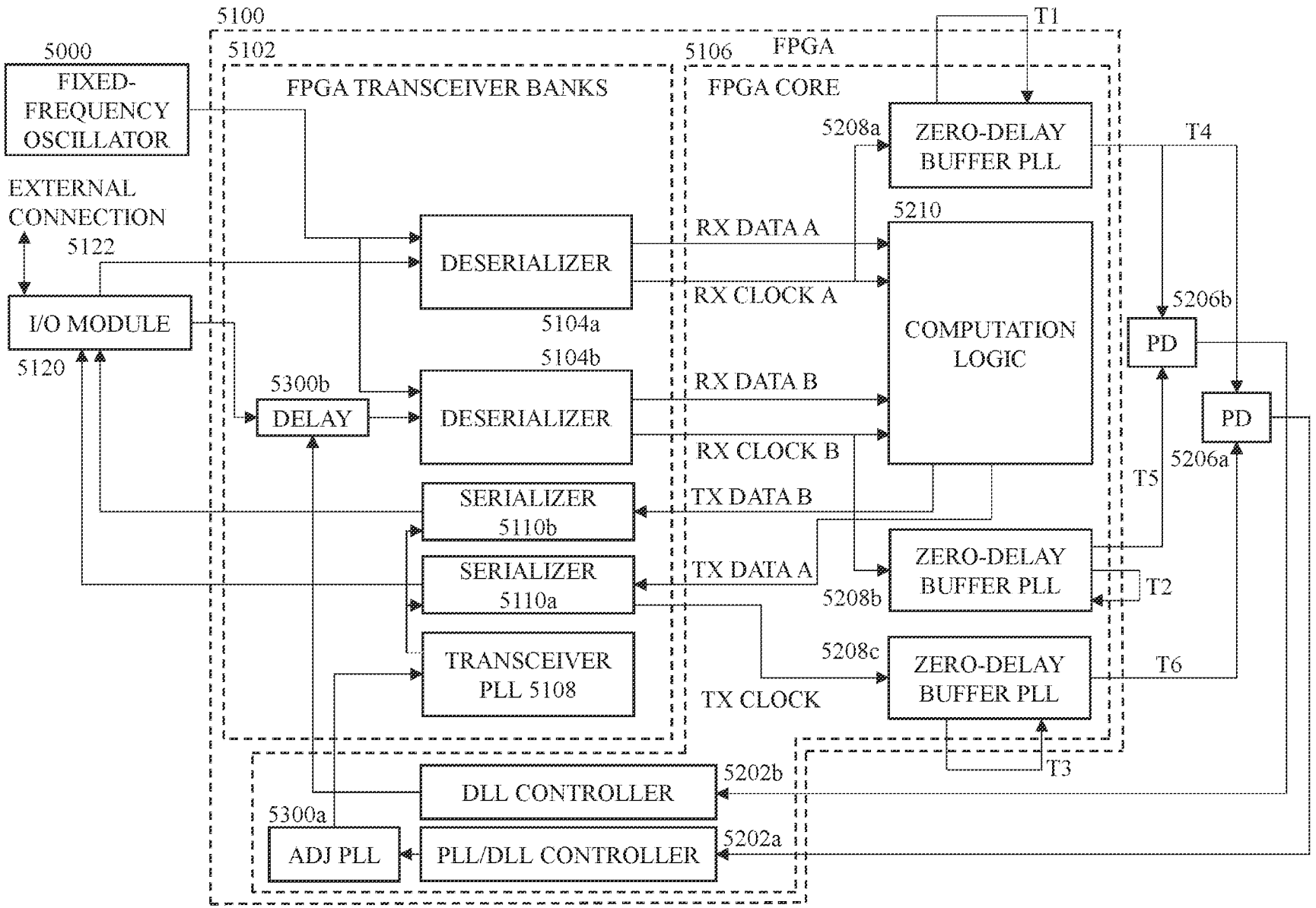

5100
5000
5102
5106
FPGA
FIXED-FREQUENCY OSCILLATOR
FPGA TRANSCEIVER BANKS
FPGA CORE
T1
5208a
ZERO-DELAY BUFFER PLL
T4
EXTERNAL CONNECTION
5122
DESERIALIZER
RX DATA A
5210
RX CLOCK A
COMPUTATION LOGIC
5206b
I/O MODULE
5104a
PD
5120
5104b
5300b
RX DATA B
DELAY
DESERIALIZER
PD
RX CLOCK B
5206a
T5
SERIALIZER 5110b
TX DATA B
SERIALIZER 5110a
TX DATA A
ZERO-DELAY BUFFER PLL
5208b
T2
TRANSCEIVER PLL 5108
5208c
ZERO-DELAY BUFFER PLL
T6
TX CLOCK
T3
5202b
DLL CONTROLLER
5300a
ADJ PLL
PLL/DLL CONTROLLER
5202a

FIG. 5E

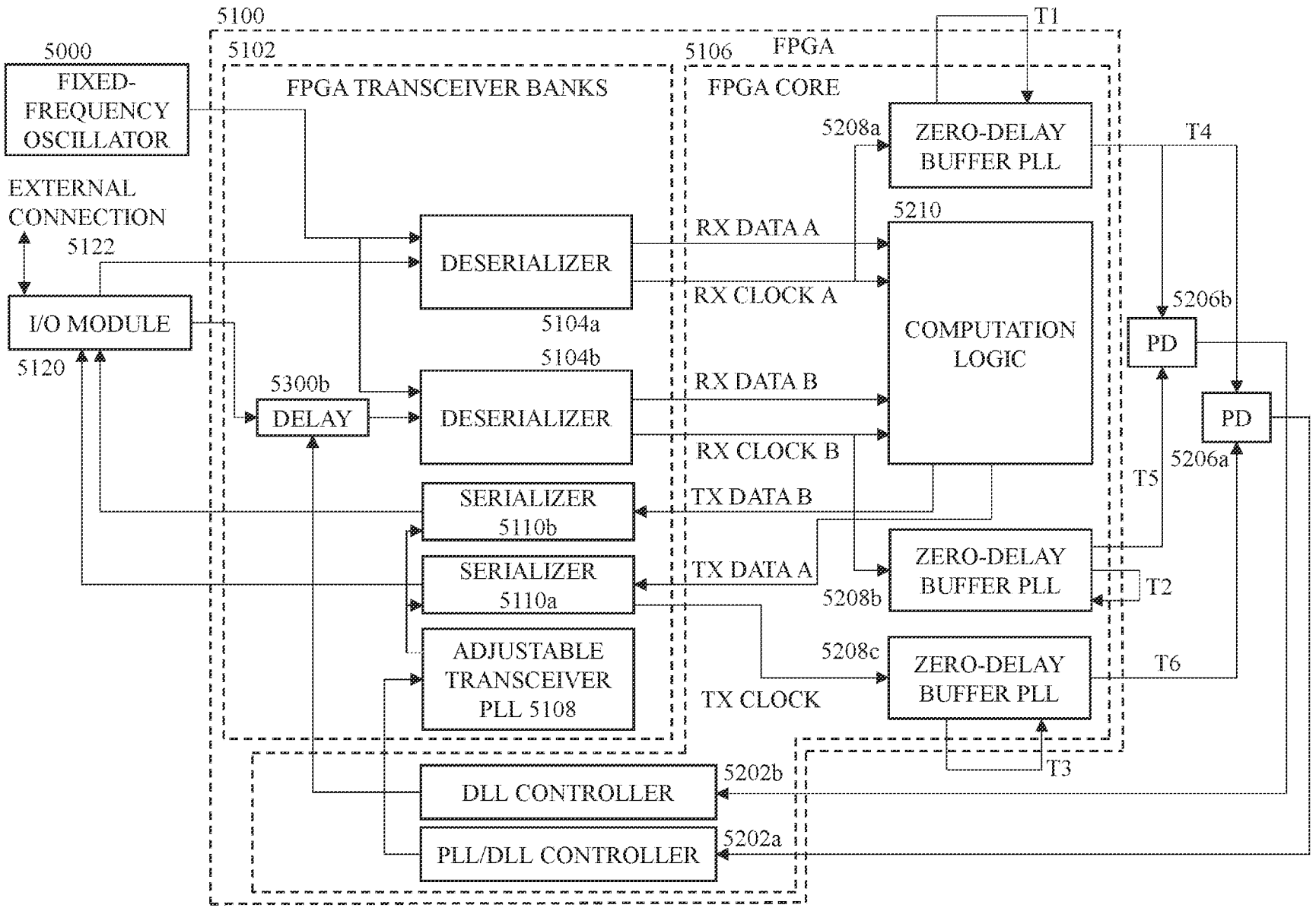

5100
5102
FPGA TRANSCEIVER BANKS
5106
FPGA
FPGA CORE
T1
5000
FIXED-FREQUENCY OSCILLATOR
EXTERNAL CONNECTION
5122
I/O MODULE
5120
DESERIALIZER
5104a
5104b
DESERIALIZER
5300b
DELAY
SERIALIZER 5110b
SERIALIZER 5110a
ADJUSTABLE TRANSCEIVER PLL 5108
RX DATA A
RX CLOCK A
RX DATA B
RX CLOCK B
TX DATA B
TX DATA A
TX CLOCK
5208a
ZERO-DELAY BUFFER PLL
5210
COMPUTATION LOGIC
5208b
ZERO-DELAY BUFFER PLL
5208c
ZERO-DELAY BUFFER PLL
T4
5206b
PD
5206a
PD
T5
T2
T6
T3
5202b
DLL CONTROLLER
5202a
PLL/DLL CONTROLLER

FIG. 5F

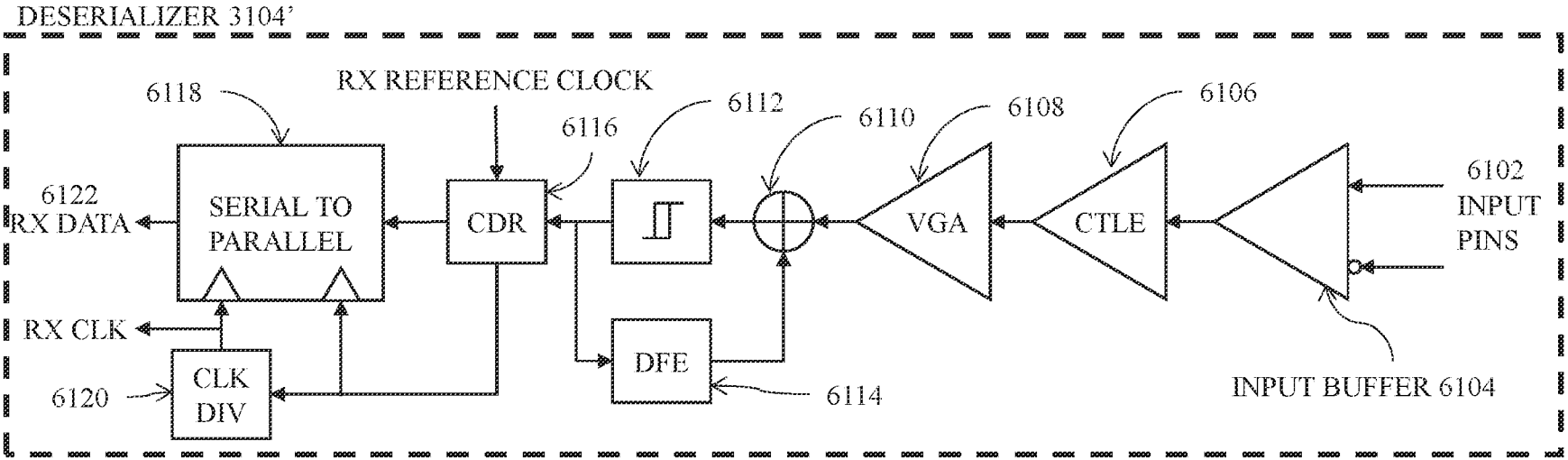

DESERIALIZER 3104'
6118
RX REFERENCE CLOCK
6116
6112
6110
6108
6106
6122
RX DATA
SERIAL TO
PARALLEL
CDR
VGA
CTLE
6102
INPUT
PINS
RX CLK
DFE
6120
CLK
DIV
6114
INPUT BUFFER 6104

FIG. 6A

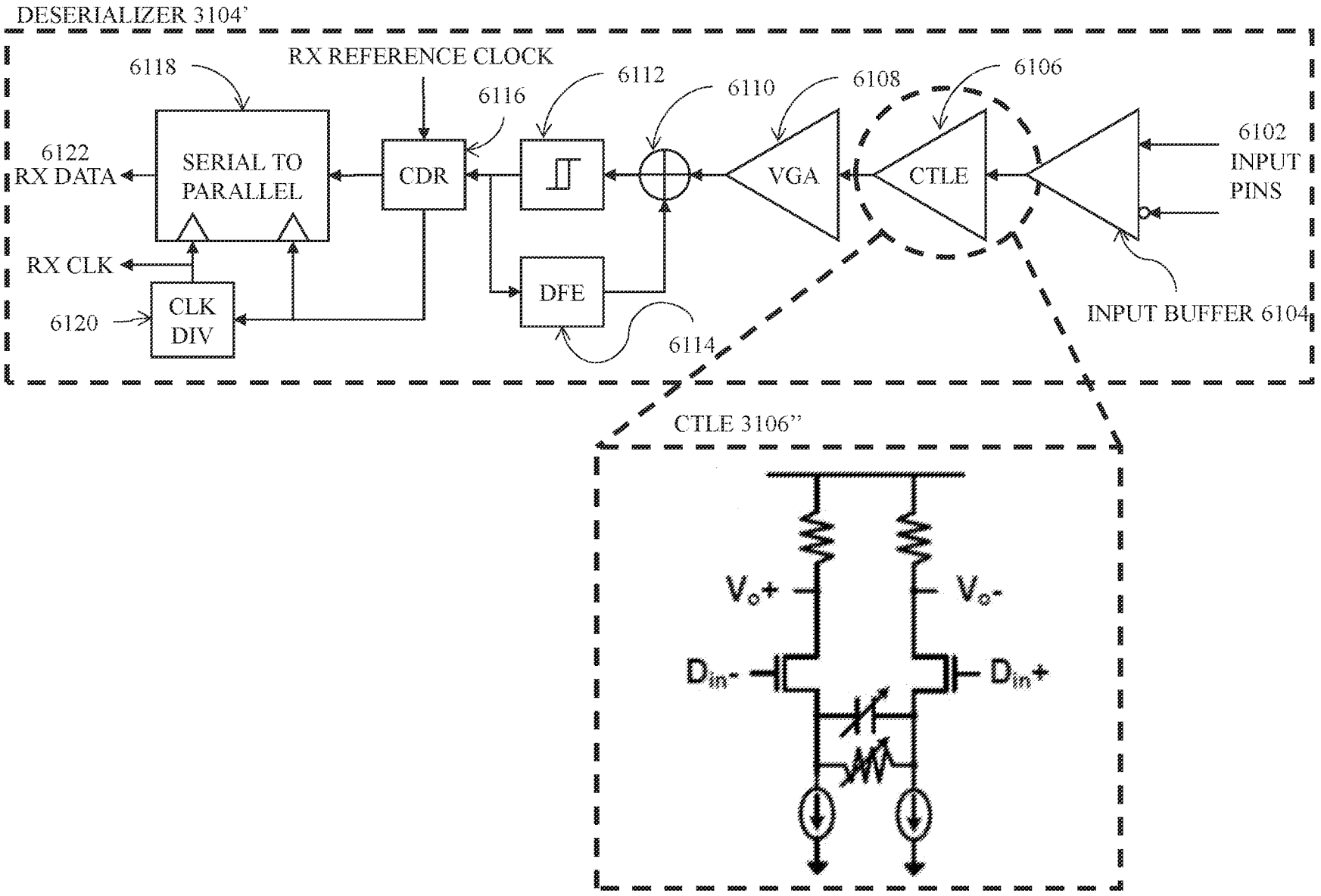

DESERIALIZER 3104'
6118
RX REFERENCE CLOCK
6116
6112
6110
6108
6106
6102
INPUT
PINS
6122
RX DATA
SERIAL TO
PARALLEL
CDR
VGA
CTLE
RX CLK
DFE
INPUT BUFFER 6104
6120
CLK
DIV
6114
CTLE 3106''
Vo+
Vo-
Din-
Din+

FIG. 6B

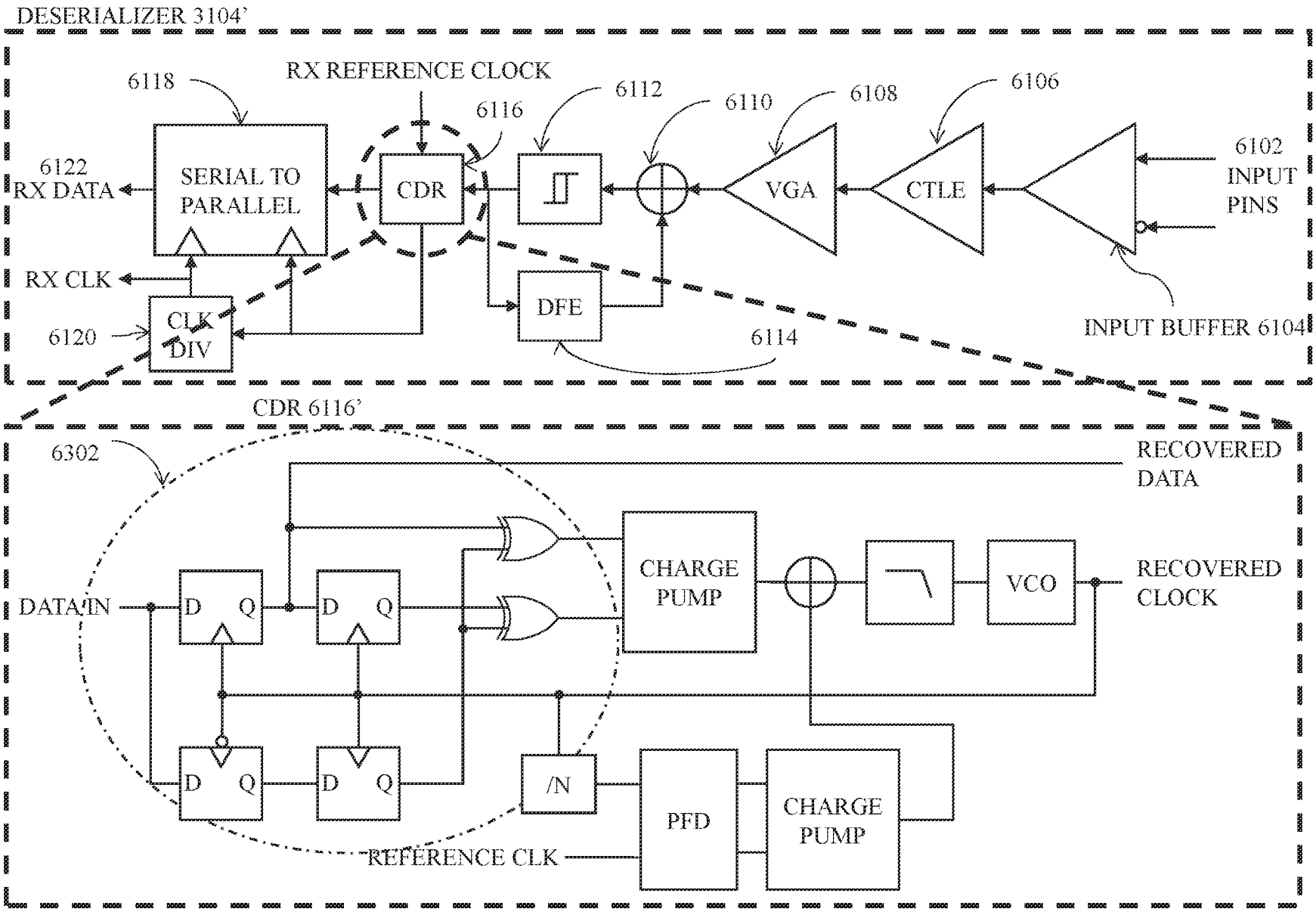

DESERIALIZER 3104'
6118
RX REFERENCE CLOCK
6116
6112
6110
6108
6106
6102
INPUT
PINS
6122
RX DATA
SERIAL TO
PARALLEL
CDR
VGA
CTLE
RX CLK
DFE
CLK
DIV
6120
6114
INPUT BUFFER 6104
CDR 6116'
6302
RECOVERED
DATA
CHARGE
PUMP
VCO
RECOVERED
CLOCK
DATA IN
D
Q
/N
PFD
CHARGE
PUMP
REFERENCE CLK

FIG. 6C

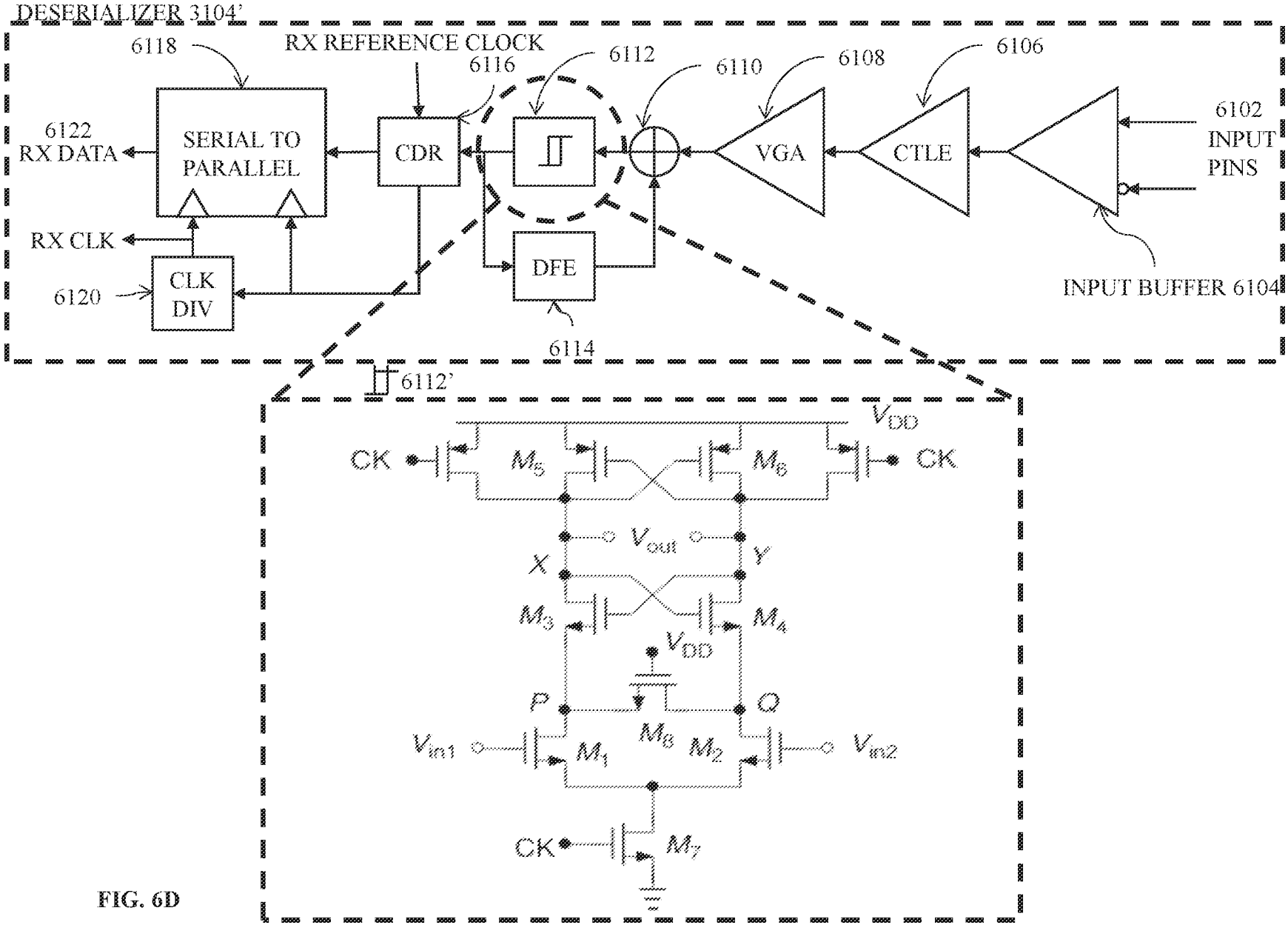

DESERIALIZER 3104'
6118
RX REFERENCE CLOCK
6116
6112
6110
6108
6106
6122
RX DATA
SERIAL TO PARALLEL
CDR
VGA
CTLE
6102
INPUT PINS
RX CLK
CLK DIV
6120
DFE
INPUT BUFFER 6104
6114
6112'
V_{DD}
CK
M_5
M_6
CK
V_{out}
X
Y
M_3
M_4
V_{DD}
P
Q
V_{in1}
M_1
M_8
M_2
V_{in2}
CK
M_7

FIG. 6D

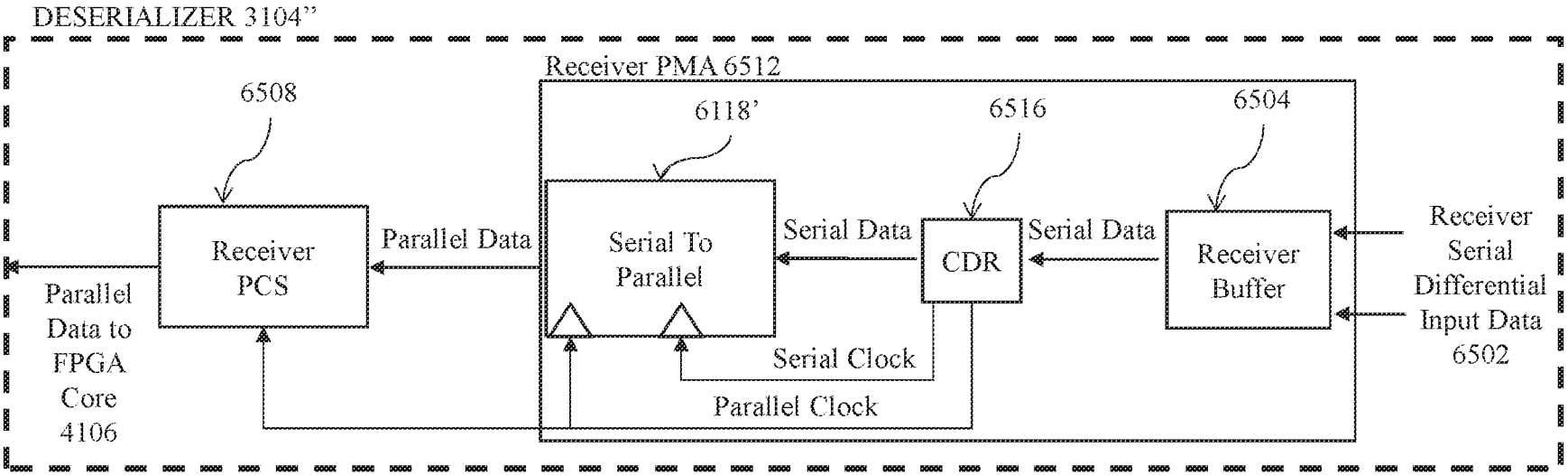

DESERIALIZER 3104"
Receiver PMA 6512
6508
6118'
6516
6504
Receiver PCS
Parallel Data
Serial To Parallel
Serial Data
CDR
Serial Data
Receiver Buffer
Receiver Serial Differential Input Data 6502
Parallel Data to FPGA Core 4106
Serial Clock
Parallel Clock

FIG. 6E

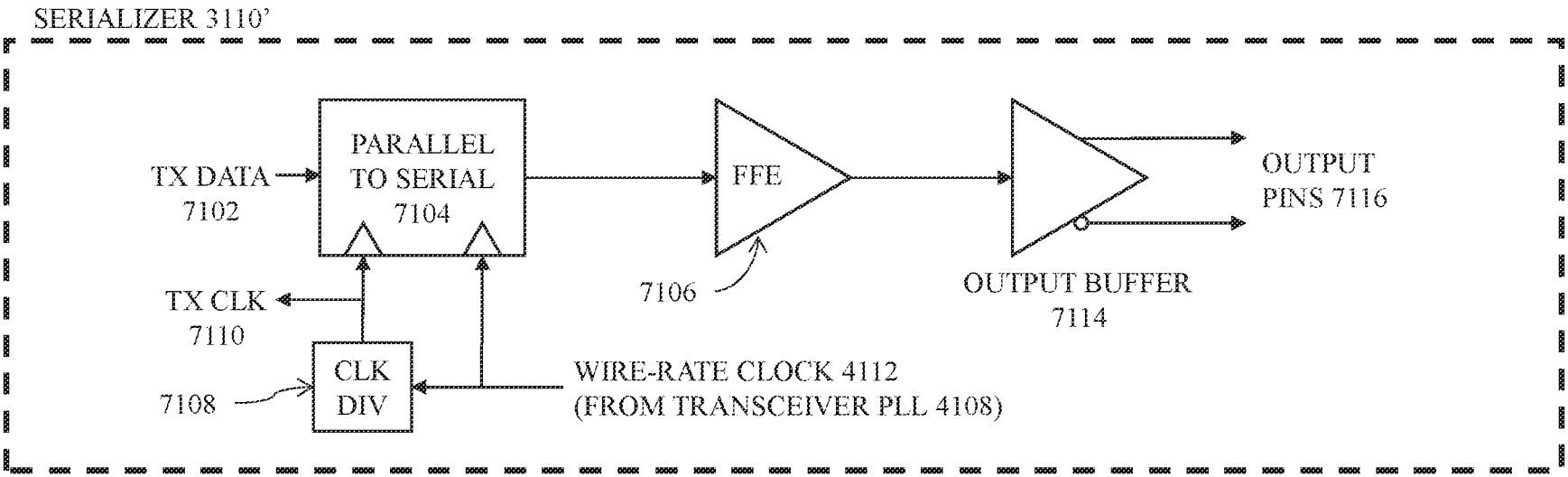

SERIALIZER 3110'
TX DATA
7102
PARALLEL
TO SERIAL
7104
FFE
7106
OUTPUT BUFFER
7114
OUTPUT
PINS 7116
TX CLK
7110
7108
CLK
DIV
WIRE-RATE CLOCK 4112
(FROM TRANSCEIVER PLL 4108)

FIG. 7A

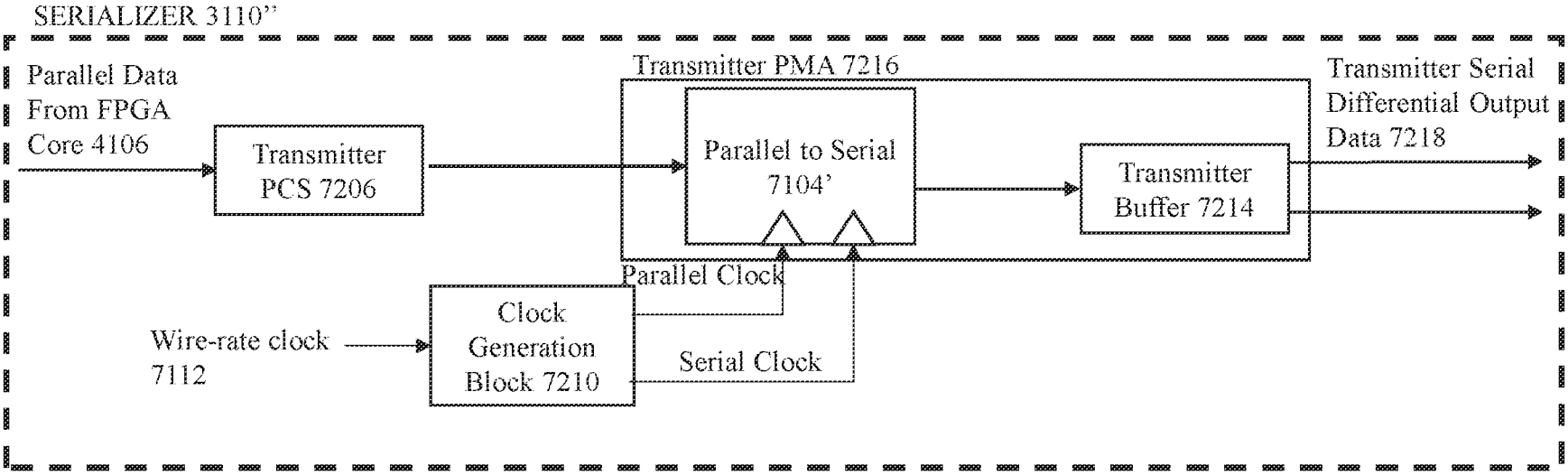

SERIALIZER 3110''
Parallel Data
From FPGA
Core 4106
Transmitter
PCS 7206
Transmitter PMA 7216
Parallel to Serial
7104'
Transmitter
Buffer 7214
Transmitter Serial
Differential Output
Data 7218
Parallel Clock
Wire-rate clock
7112
Clock
Generation
Block 7210
Serial Clock

FIG. 7B

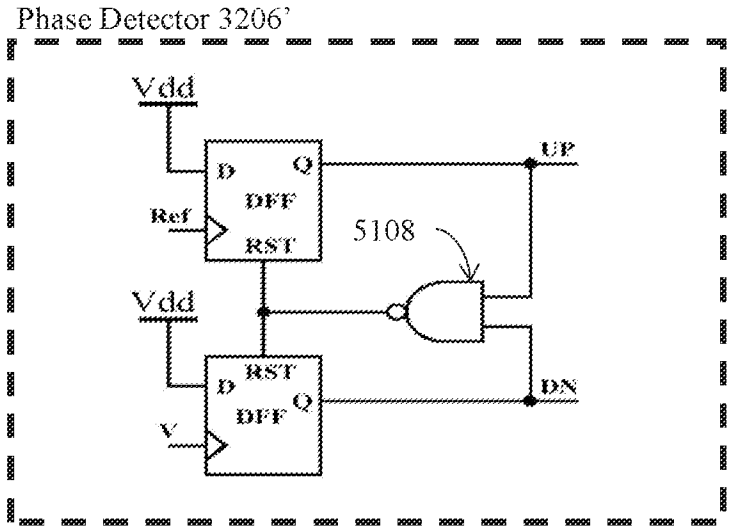

Phase Detector 3206'
Vdd
D
Q
DFF
RST
Ref
UP
5108
Vdd
RST
D
DFF
Q
V
DN

FIG. 8A

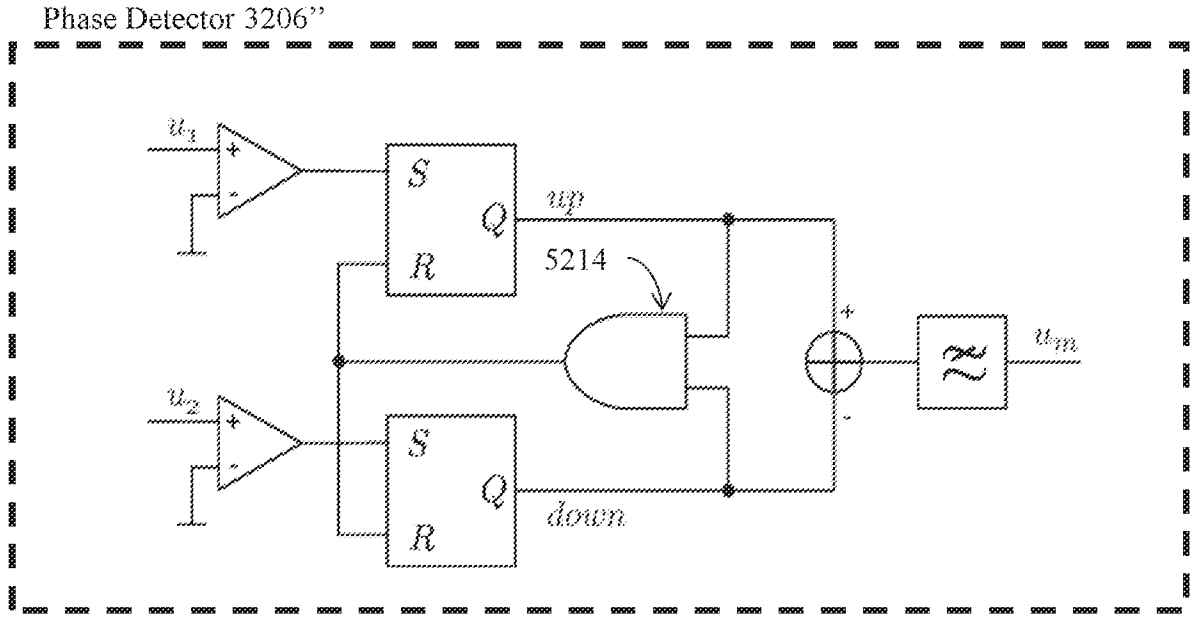
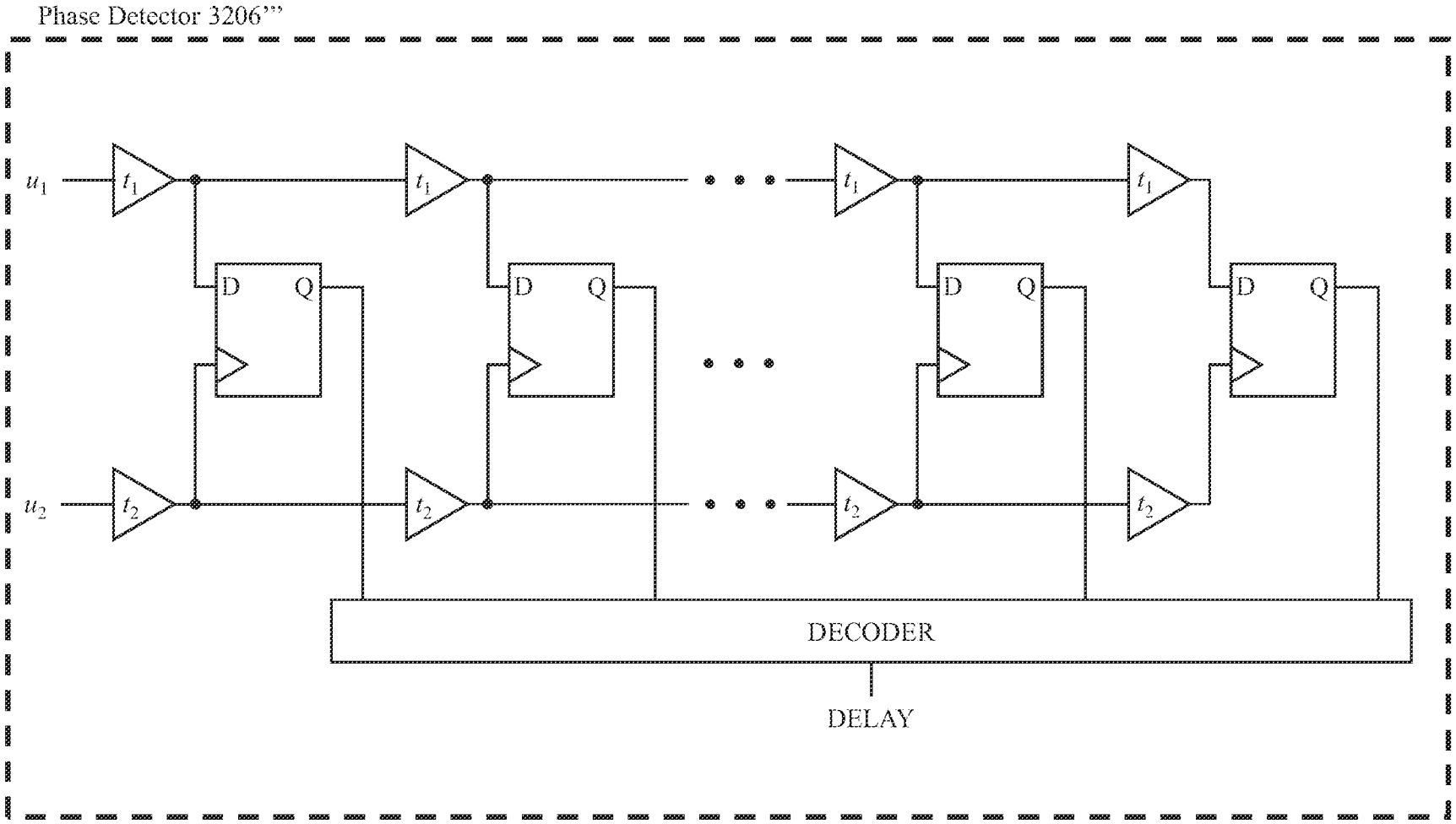

Phase Detector 3206''
u_1
+
-
S
Q
R
up
5214
u_2
+
-
S
Q
R
down
+
-
≈
u_m

FIG. 8B



PRIOR ART

FIG. 8C

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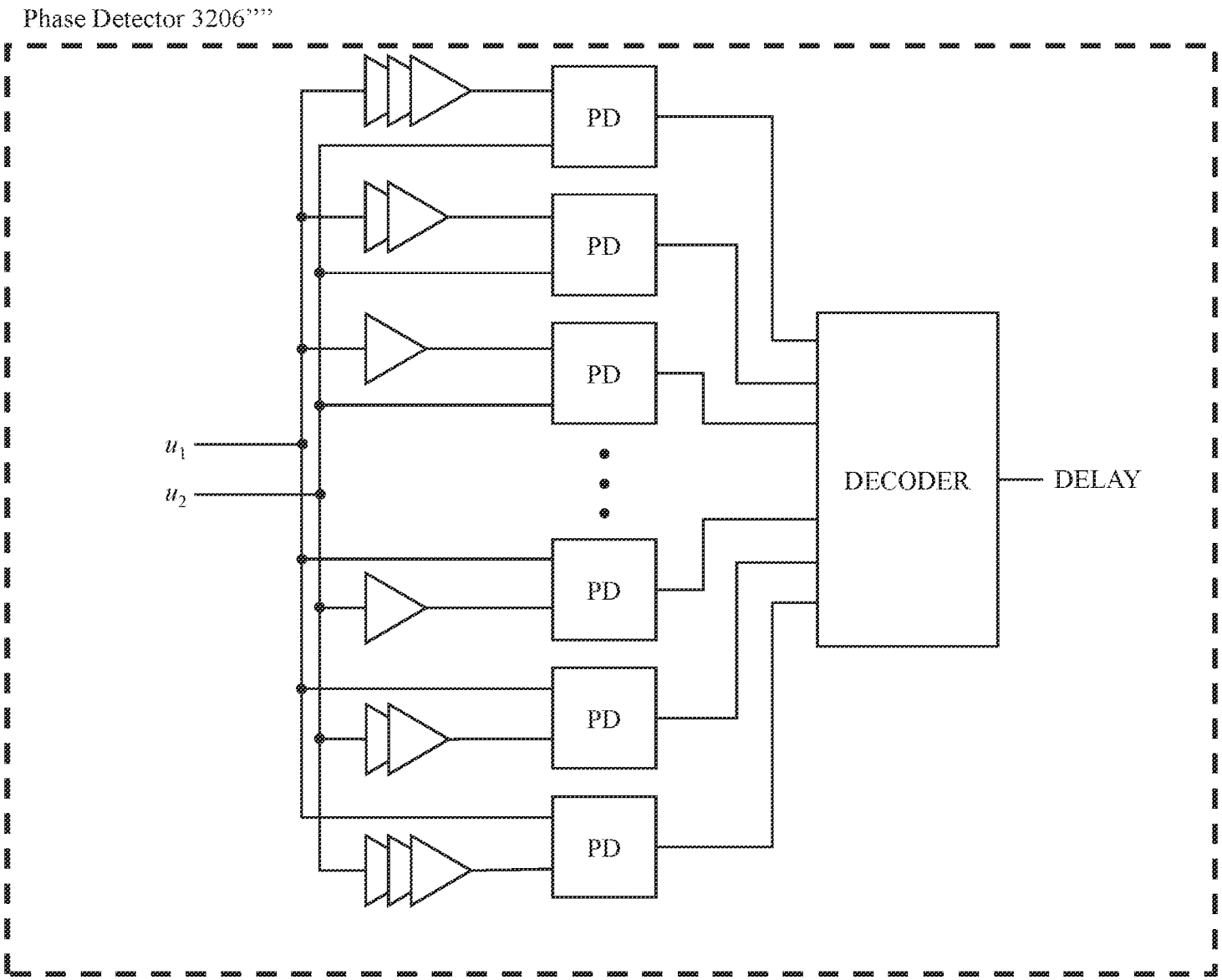


FIG. 8D

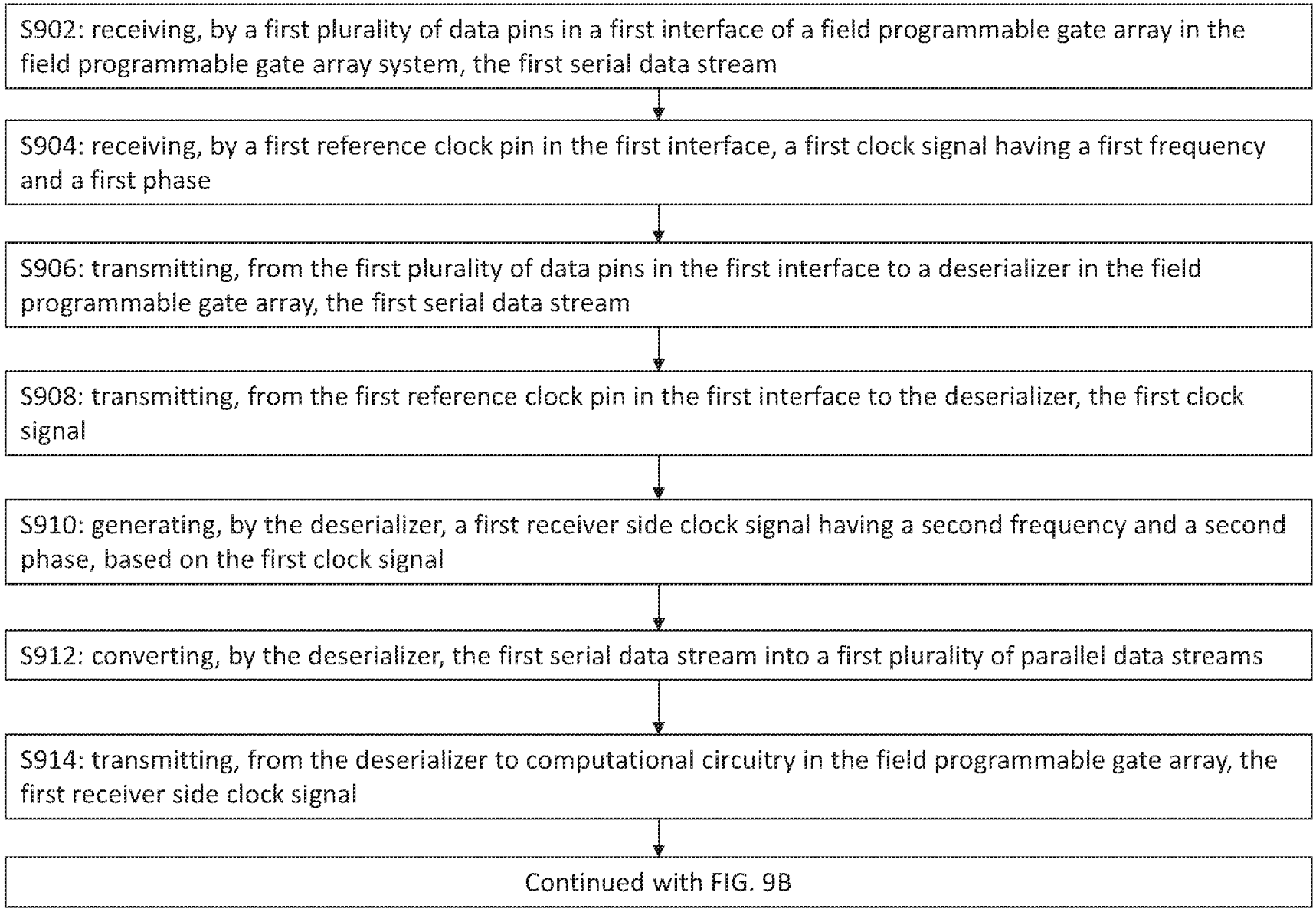

S902: receiving, by a first plurality of data pins in a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream
S904: receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase
S906: transmitting, from the first plurality of data pins in the first interface to a deserializer in the field programmable gate array, the first serial data stream
S908: transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal
S910: generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal
S912: converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams
S914: transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal
Continued with FIG. 9B

FIG. 9A

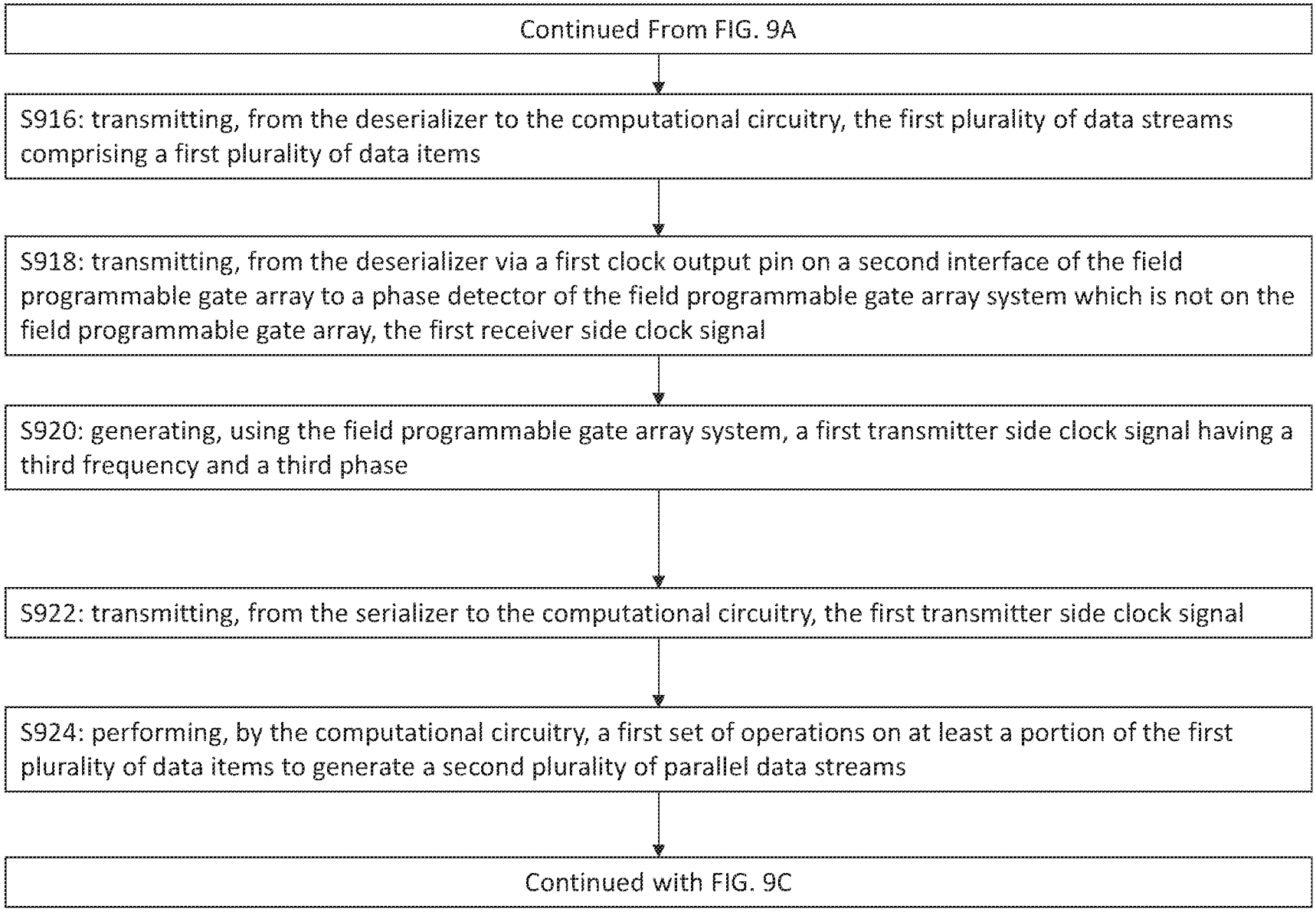

Continued From FIG. 9A
S916: transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items
S918: transmitting, from the deserializer via a first clock output pin on a second interface of the field programmable gate array to a phase detector of the field programmable gate array system which is not on the field programmable gate array, the first receiver side clock signal
S920: generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase
S922: transmitting, from the serializer to the computational circuitry, the first transmitter side clock signal
S924: performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams
Continued with FIG. 9C

FIG. 9B

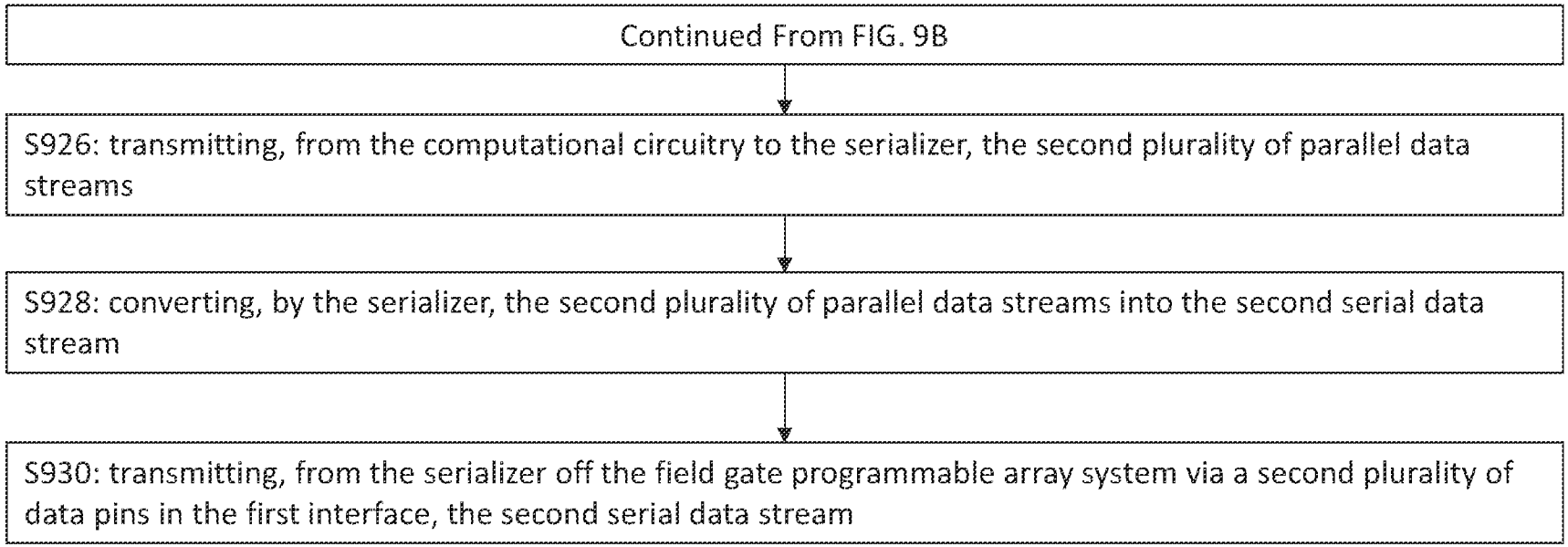

Continued From FIG. 9B
S926: transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams
S928: converting, by the serializer, the second plurality of parallel data streams into the second serial data stream
S930: transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins in the first interface, the second serial data stream

FIG. 9C

S920: generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level

S1002: generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase

S1004: generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal

S1006: generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase

S1008: transmitting, from the serializer via a second clock output pin in the second interface to the phase detector, the interim transmitter side clock signal

Continued with FIG. 10B

FIG. 10A

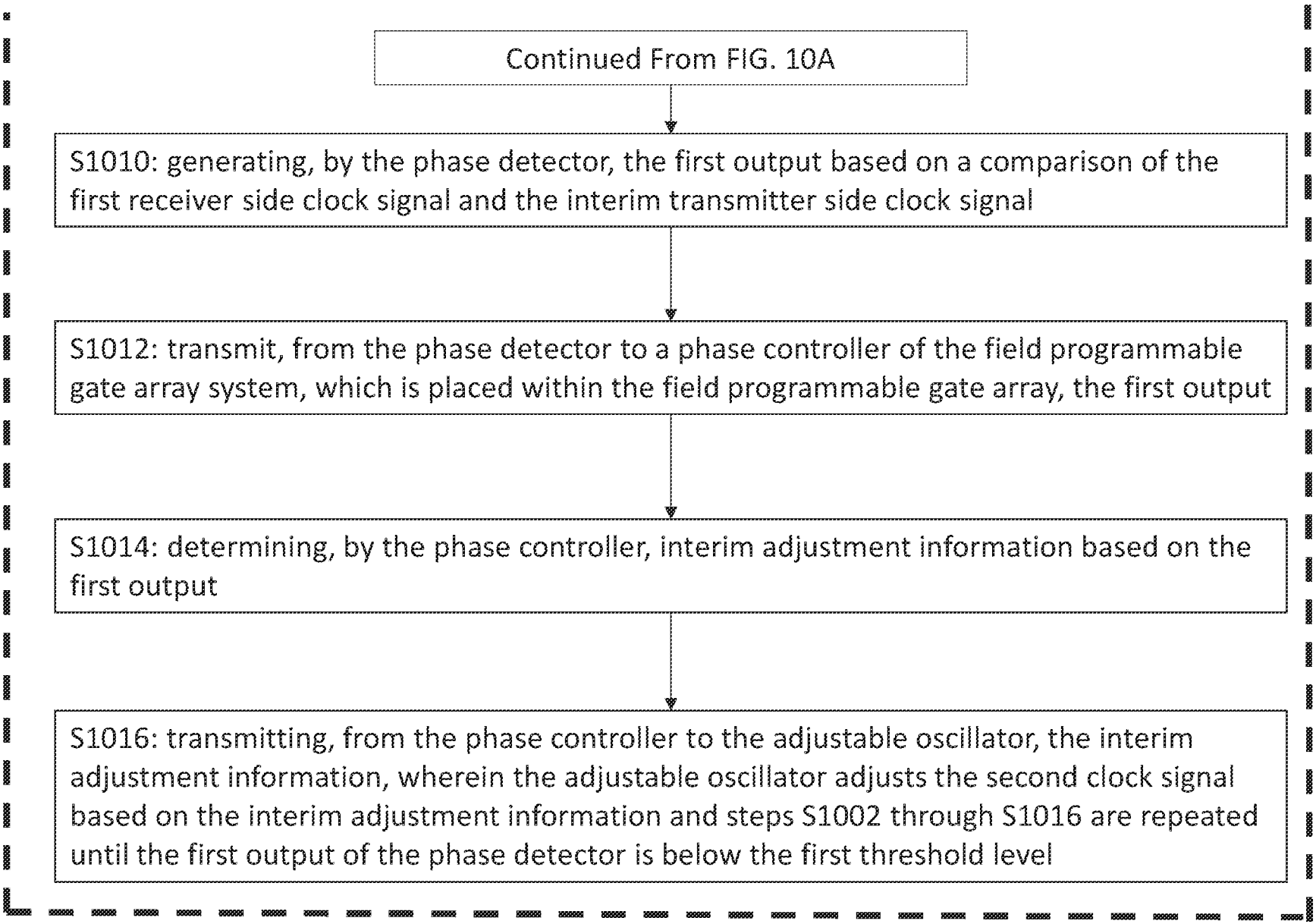

Continued From FIG. 10A
S1010: generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal
S1012: transmit, from the phase detector to a phase controller of the field programmable gate array system, which is placed within the field programmable gate array, the first output
S1014: determining, by the phase controller, interim adjustment information based on the first output
S1016: transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information, wherein the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps S1002 through S1016 are repeated until the first output of the phase detector is below the first threshold level

FIG. 10B

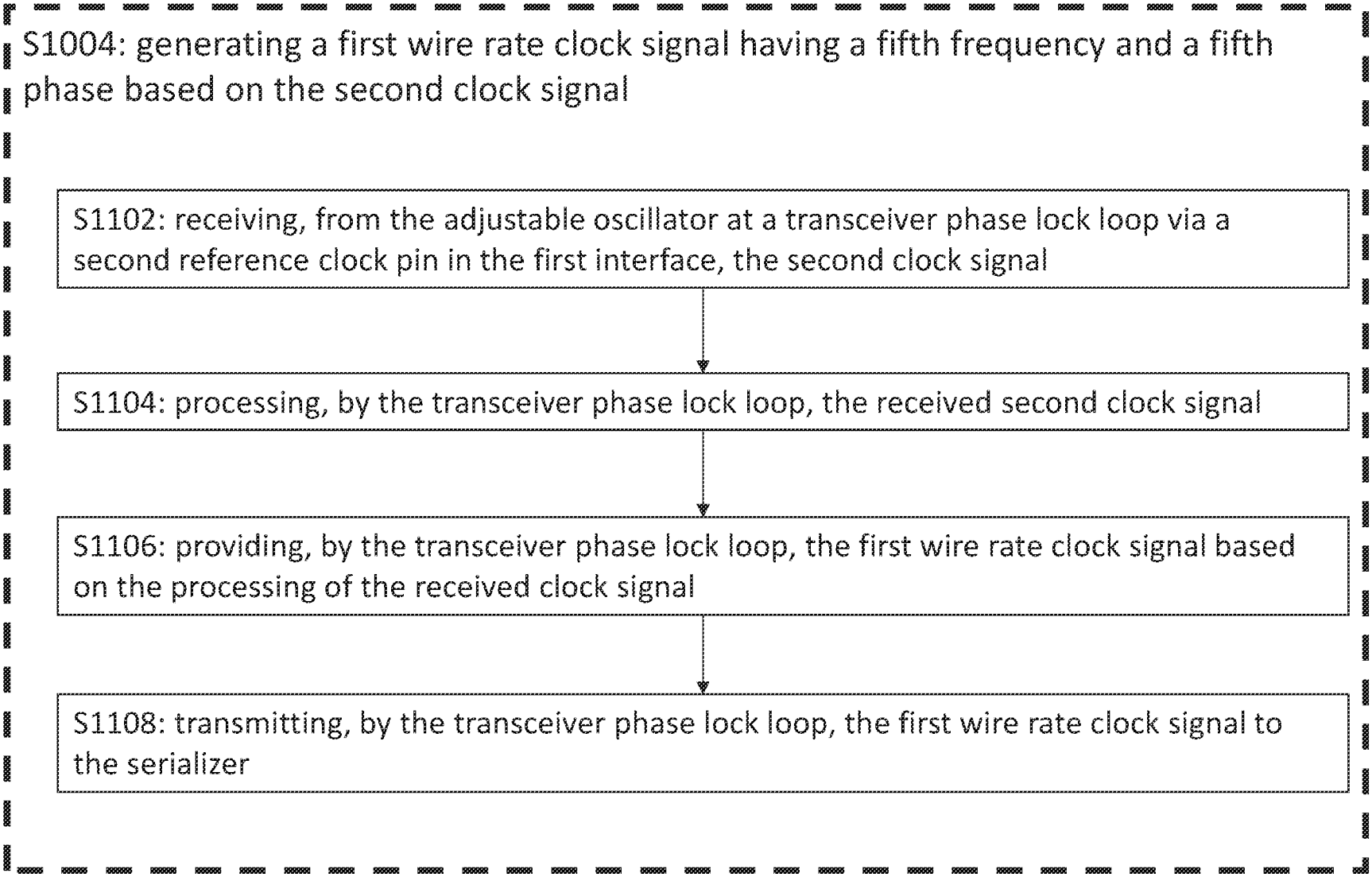

S1004: generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal
S1102: receiving, from the adjustable oscillator at a transceiver phase lock loop via a second reference clock pin in the first interface, the second clock signal
S1104: processing, by the transceiver phase lock loop, the received second clock signal
S1106: providing, by the transceiver phase lock loop, the first wire rate clock signal based on the processing of the received clock signal
S1108: transmitting, by the transceiver phase lock loop, the first wire rate clock signal to the serializer

FIG. 11

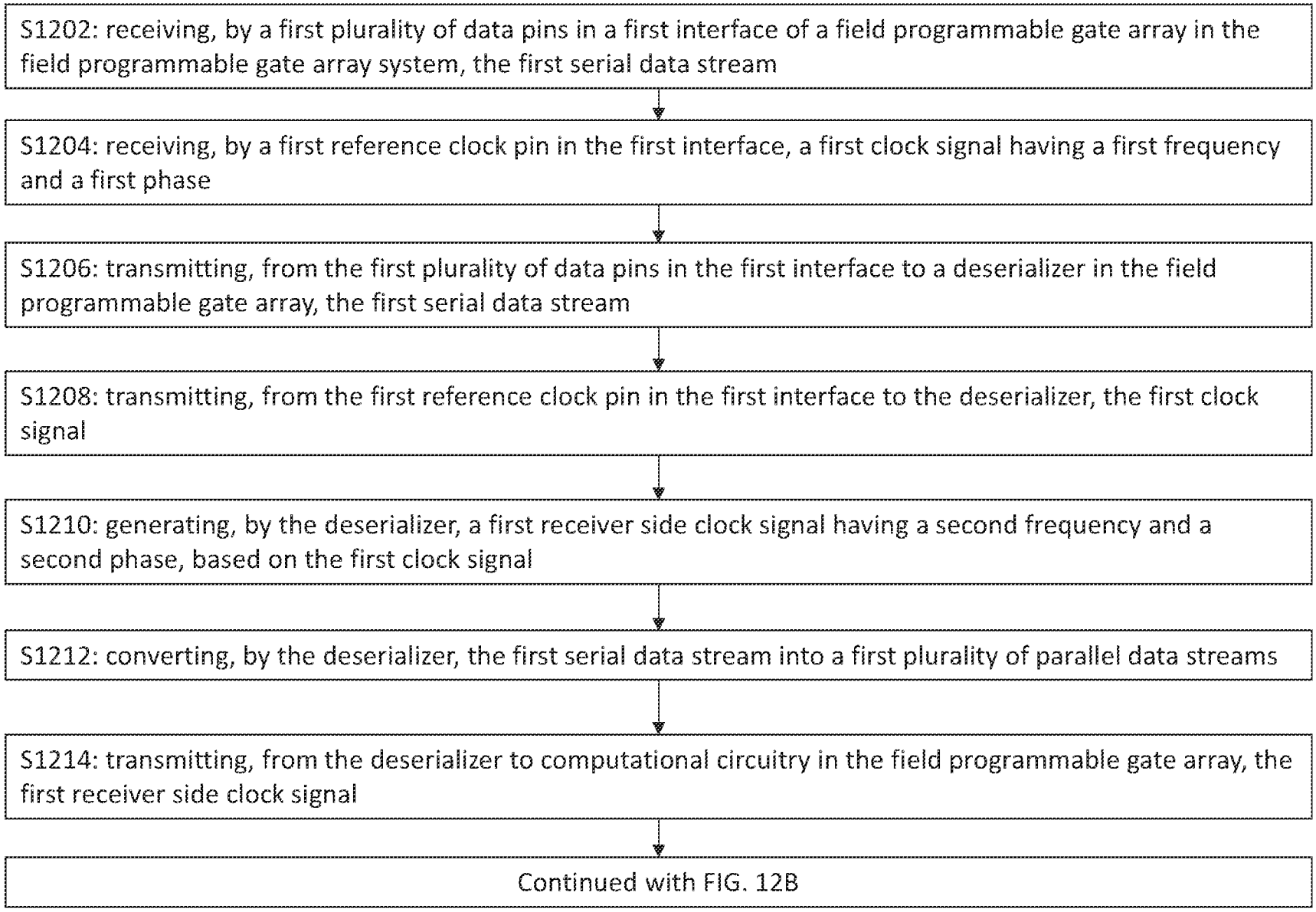

S1202: receiving, by a first plurality of data pins in a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream
S1204: receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase
S1206: transmitting, from the first plurality of data pins in the first interface to a deserializer in the field programmable gate array, the first serial data stream
S1208: transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal
S1210: generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal
S1212: converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams
S1214: transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal
Continued with FIG. 12B

FIG. 12A

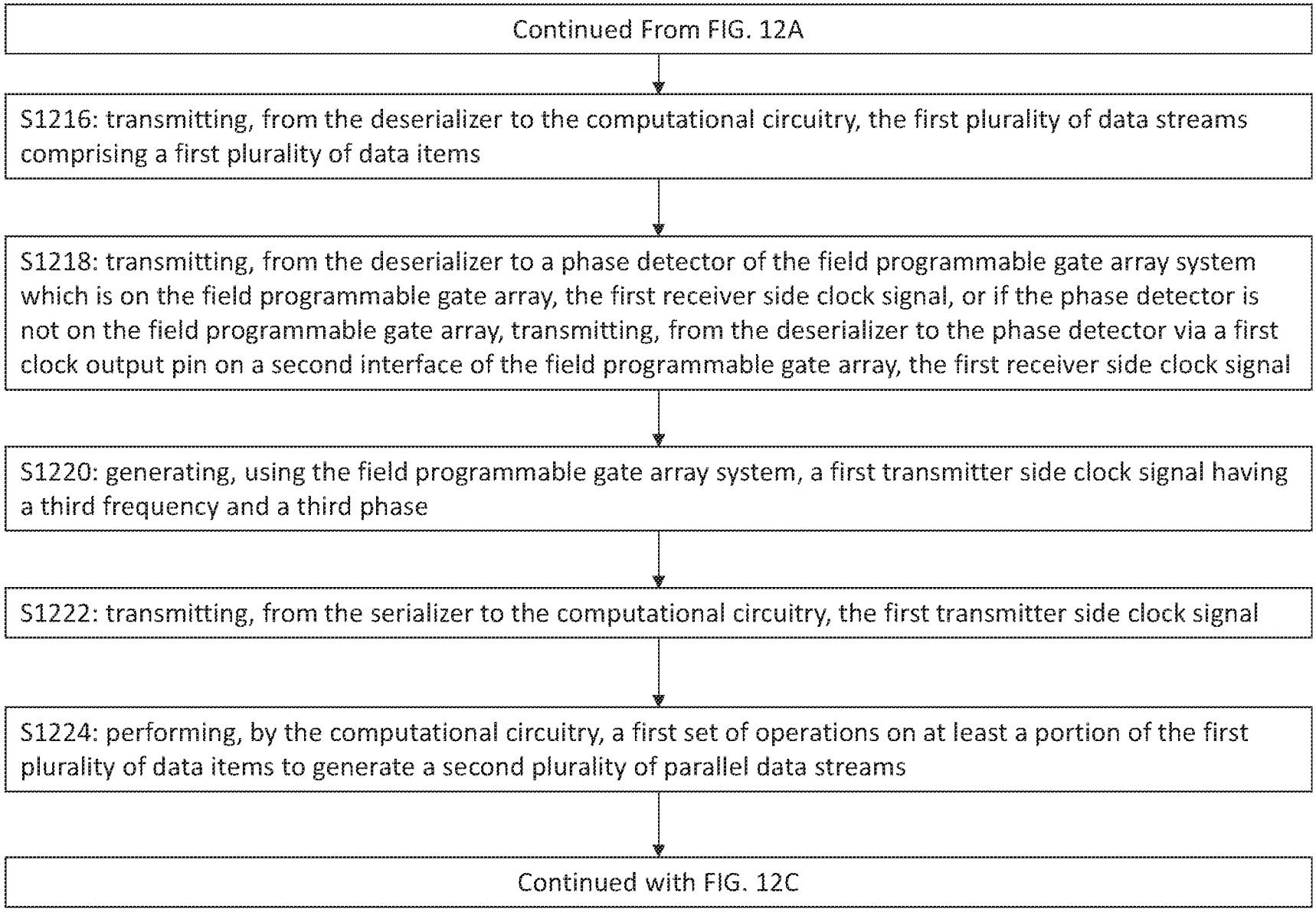

Continued From FIG. 12A
S1216: transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items
S1218: transmitting, from the deserializer to a phase detector of the field programmable gate array system which is on the field programmable gate array, the first receiver side clock signal, or if the phase detector is not on the field programmable gate array, transmitting, from the deserializer to the phase detector via a first clock output pin on a second interface of the field programmable gate array, the first receiver side clock signal
S1220: generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase
S1222: transmitting, from the serializer to the computational circuitry, the first transmitter side clock signal
S1224: performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams
Continued with FIG. 12C

FIG. 12B

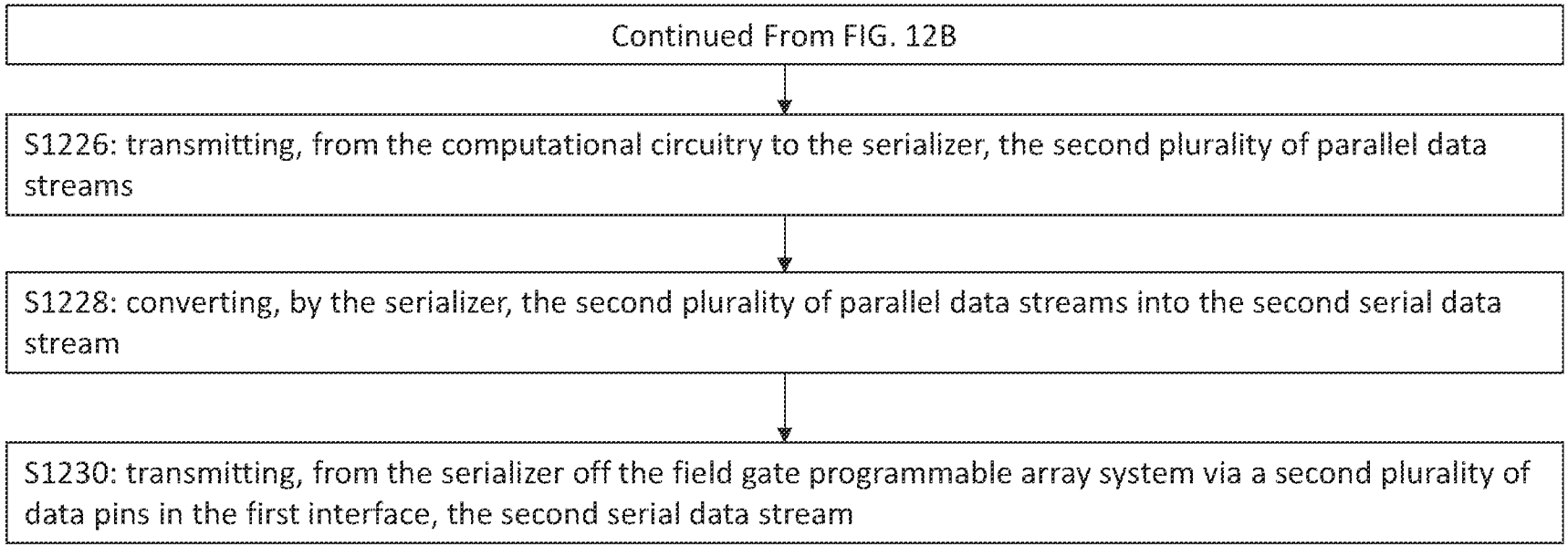

Continued From FIG. 12B
S1226: transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams
S1228: converting, by the serializer, the second plurality of parallel data streams into the second serial data stream
S1230: transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins in the first interface, the second serial data stream

FIG. 12C

S1220: generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level

S1302: generating, by a phase lock loop with phase adjustment in the field programmable gate array system which is on the field programmable gate array, a second clock signal having a fourth frequency and a fourth phase

S1304: generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal

S1306: generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase

S1308: transmitting, from the serializer to the phase detector which is on the field programmable gate array, the interim transmitter side clock signal, or if the phase detector is not on the field programmable gate array, transmitting, from the serializer to the phase detector via a second clock output pin in the second interface, the interim transmitter side clock

Continued with FIG. 13B

FIG. 13A

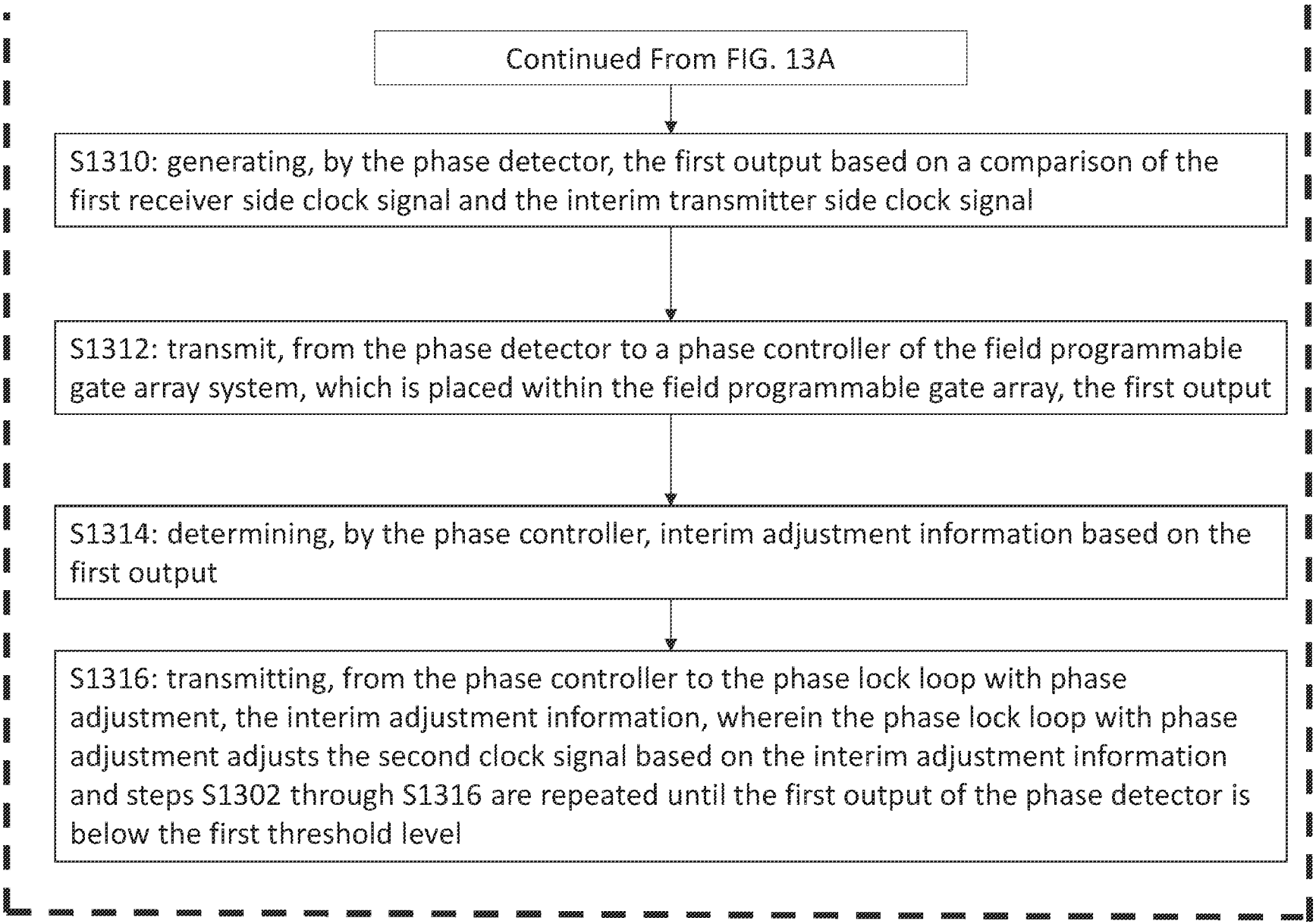

Continued From FIG. 13A
S1310: generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal
S1312: transmit, from the phase detector to a phase controller of the field programmable gate array system, which is placed within the field programmable gate array, the first output
S1314: determining, by the phase controller, interim adjustment information based on the first output
S1316: transmitting, from the phase controller to the phase lock loop with phase adjustment, the interim adjustment information, wherein the phase lock loop with phase adjustment adjusts the second clock signal based on the interim adjustment information and steps S1302 through S1316 are repeated until the first output of the phase detector is below the first threshold level

FIG. 13B

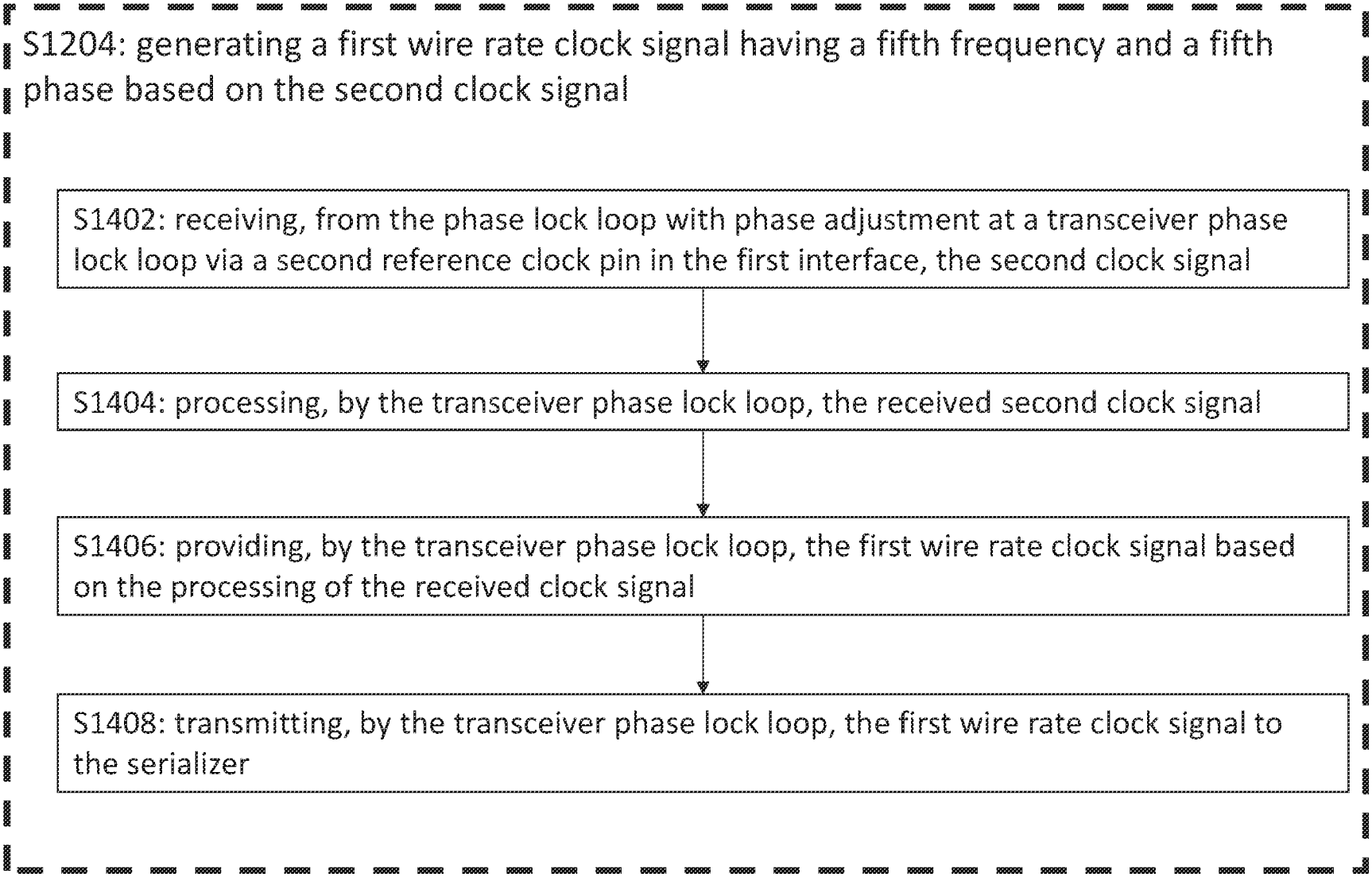

S1204: generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal
S1402: receiving, from the phase lock loop with phase adjustment at a transceiver phase lock loop via a second reference clock pin in the first interface, the second clock signal
S1404: processing, by the transceiver phase lock loop, the received second clock signal
S1406: providing, by the transceiver phase lock loop, the first wire rate clock signal based on the processing of the received clock signal
S1408: transmitting, by the transceiver phase lock loop, the first wire rate clock signal to the serializer

FIG. 14

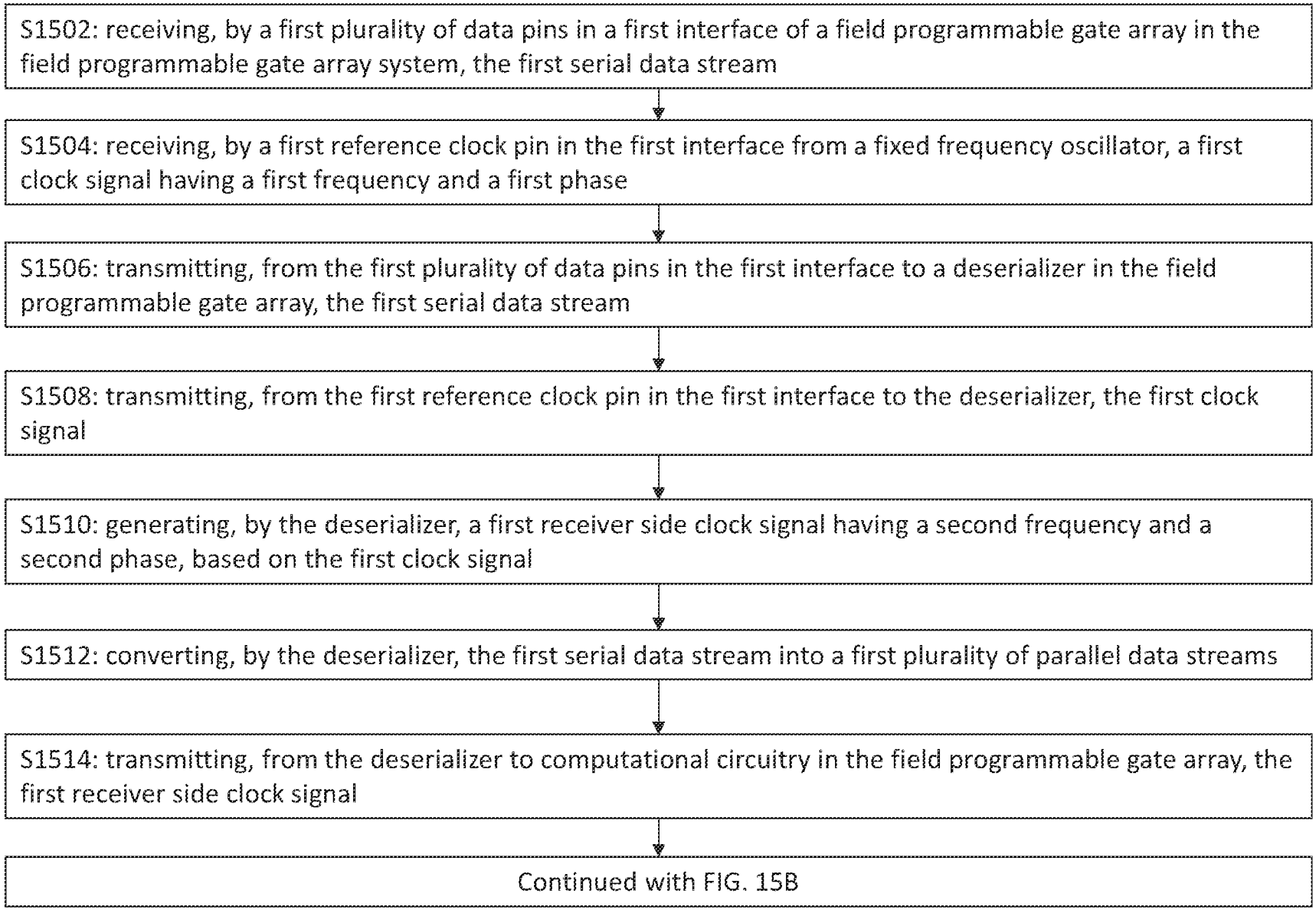

S1502: receiving, by a first plurality of data pins in a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream
S1504: receiving, by a first reference clock pin in the first interface from a fixed frequency oscillator, a first clock signal having a first frequency and a first phase
S1506: transmitting, from the first plurality of data pins in the first interface to a deserializer in the field programmable gate array, the first serial data stream
S1508: transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal
S1510: generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal
S1512: converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams
S1514: transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal
Continued with FIG. 15B

FIG. 15A

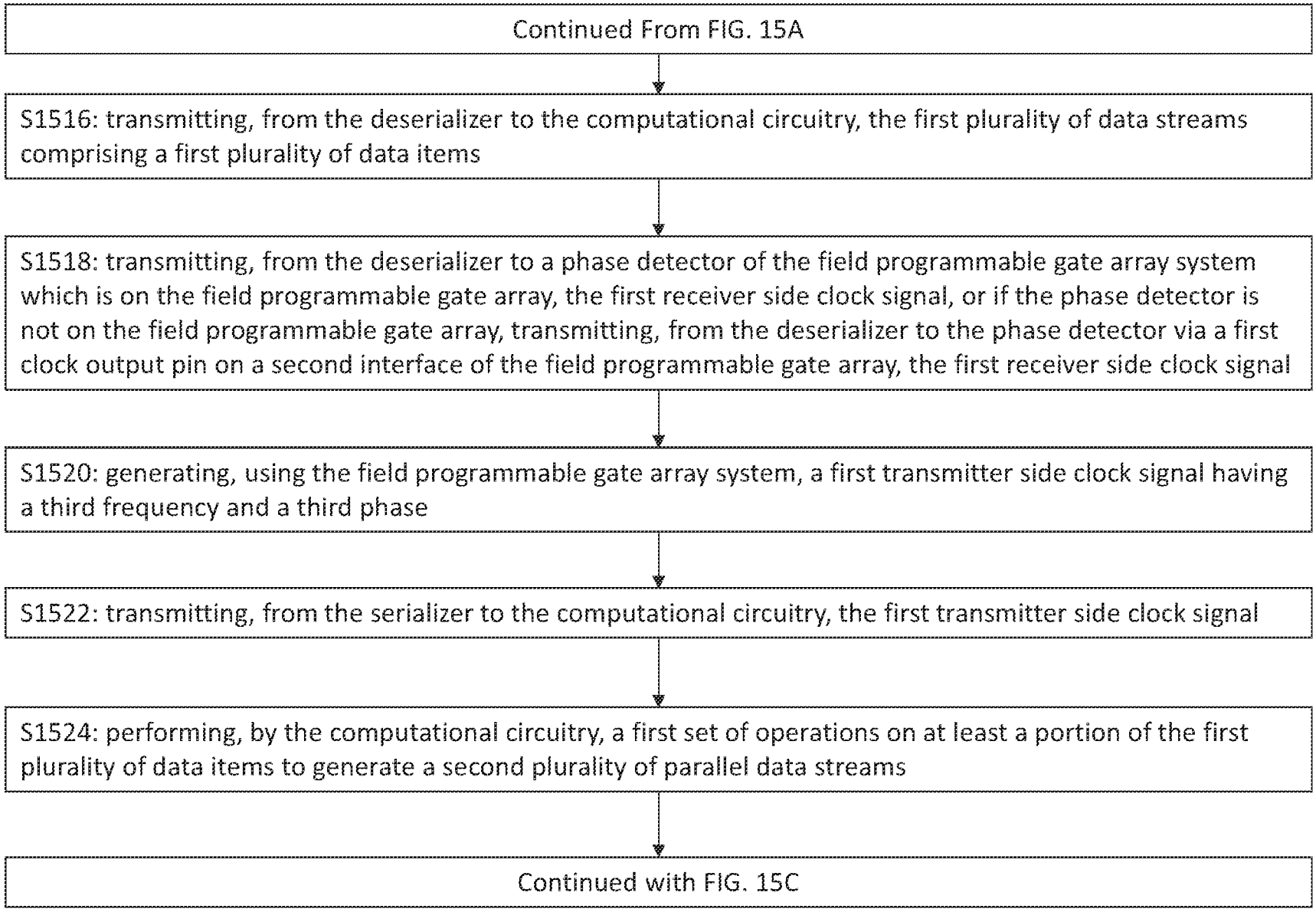

Continued From FIG. 15A
S1516: transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items
S1518: transmitting, from the deserializer to a phase detector of the field programmable gate array system which is on the field programmable gate array, the first receiver side clock signal, or if the phase detector is not on the field programmable gate array, transmitting, from the deserializer to the phase detector via a first clock output pin on a second interface of the field programmable gate array, the first receiver side clock signal
S1520: generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase
S1522: transmitting, from the serializer to the computational circuitry, the first transmitter side clock signal
S1524: performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams
Continued with FIG. 15C

FIG. 15B

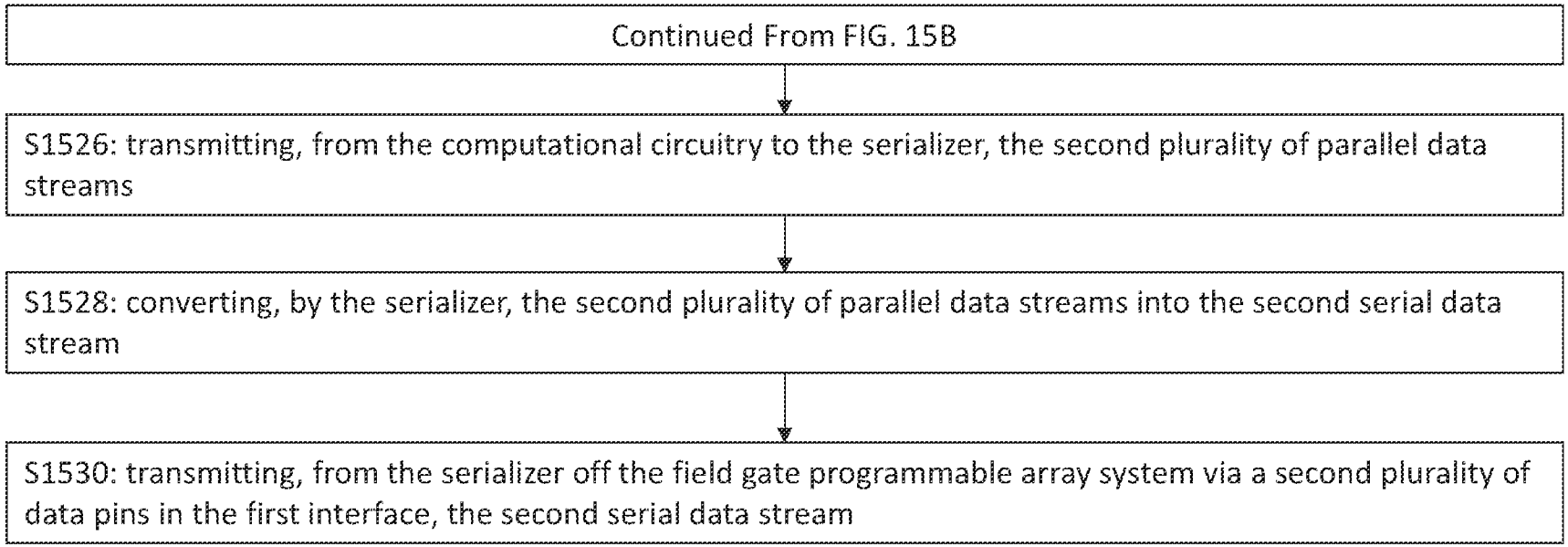

Continued From FIG. 15B
S1526: transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams
S1528: converting, by the serializer, the second plurality of parallel data streams into the second serial data stream
S1530: transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins in the first interface, the second serial data stream

FIG. 15C

S1520: generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level

S1602: receiving, from the fixed frequency oscillator at an adjustable transceiver phase lock loop via a second reference clock pin in the first interface, the first clock signal to generate a second clock signal having a fourth frequency and a fourth phase

S1604: generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal and the interim adjustment information from the phase controller

S1606: generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase

S1608: transmitting, from the serializer to the phase detector which is on the field programmable gate array, the interim transmitter side clock signal, or if the phase detector is not on the field programmable gate array, transmitting, from the serializer to the phase detector via a second clock output pin in the second interface, the interim transmitter side clock signal

Continued with FIG. 16B

FIG. 16A

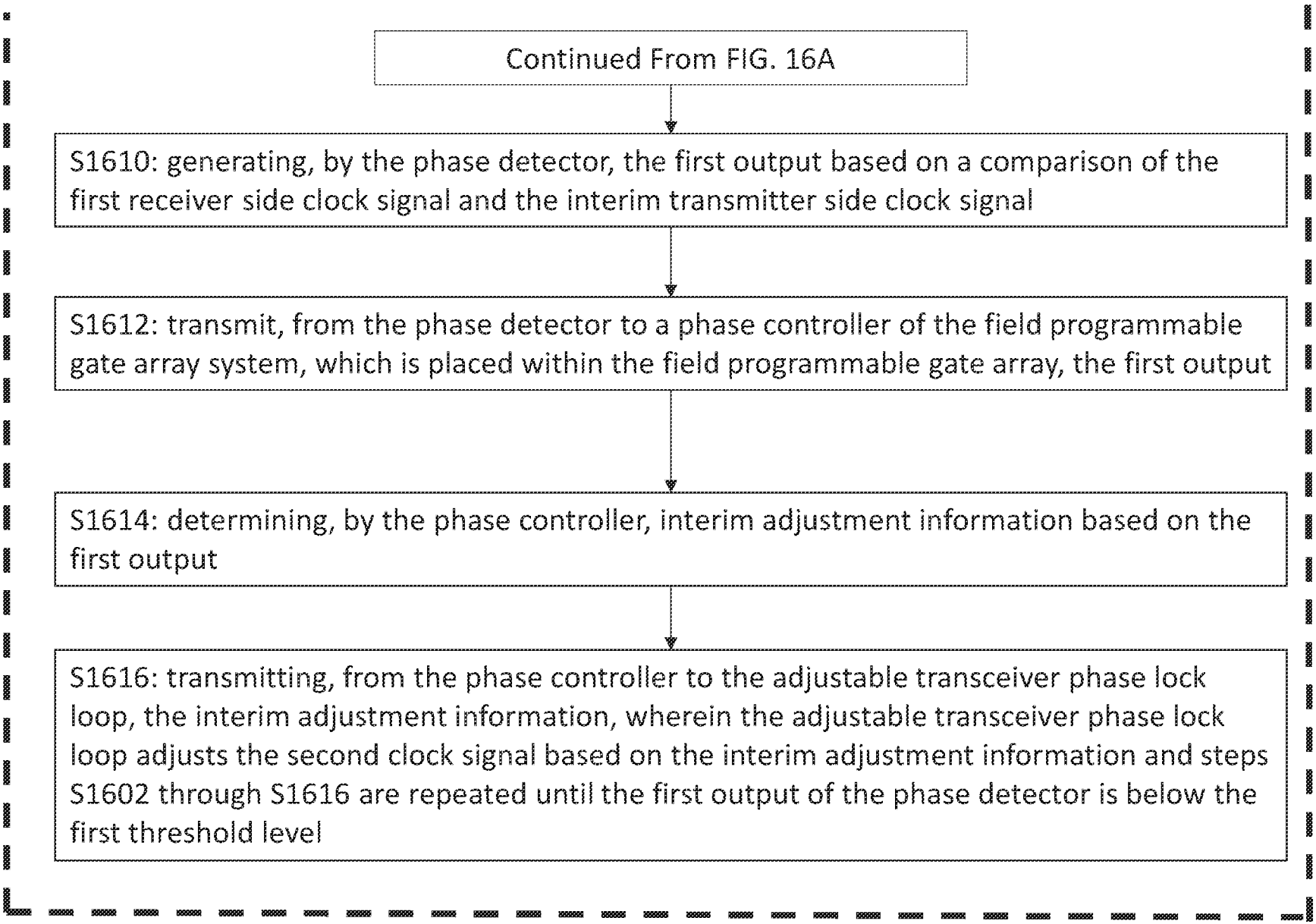

Continued From FIG. 16A
S1610: generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal
S1612: transmit, from the phase detector to a phase controller of the field programmable gate array system, which is placed within the field programmable gate array, the first output
S1614: determining, by the phase controller, interim adjustment information based on the first output
S1616: transmitting, from the phase controller to the adjustable transceiver phase lock loop, the interim adjustment information, wherein the adjustable transceiver phase lock loop adjusts the second clock signal based on the interim adjustment information and steps S1602 through S1616 are repeated until the first output of the phase detector is below the first threshold level

FIG. 16B

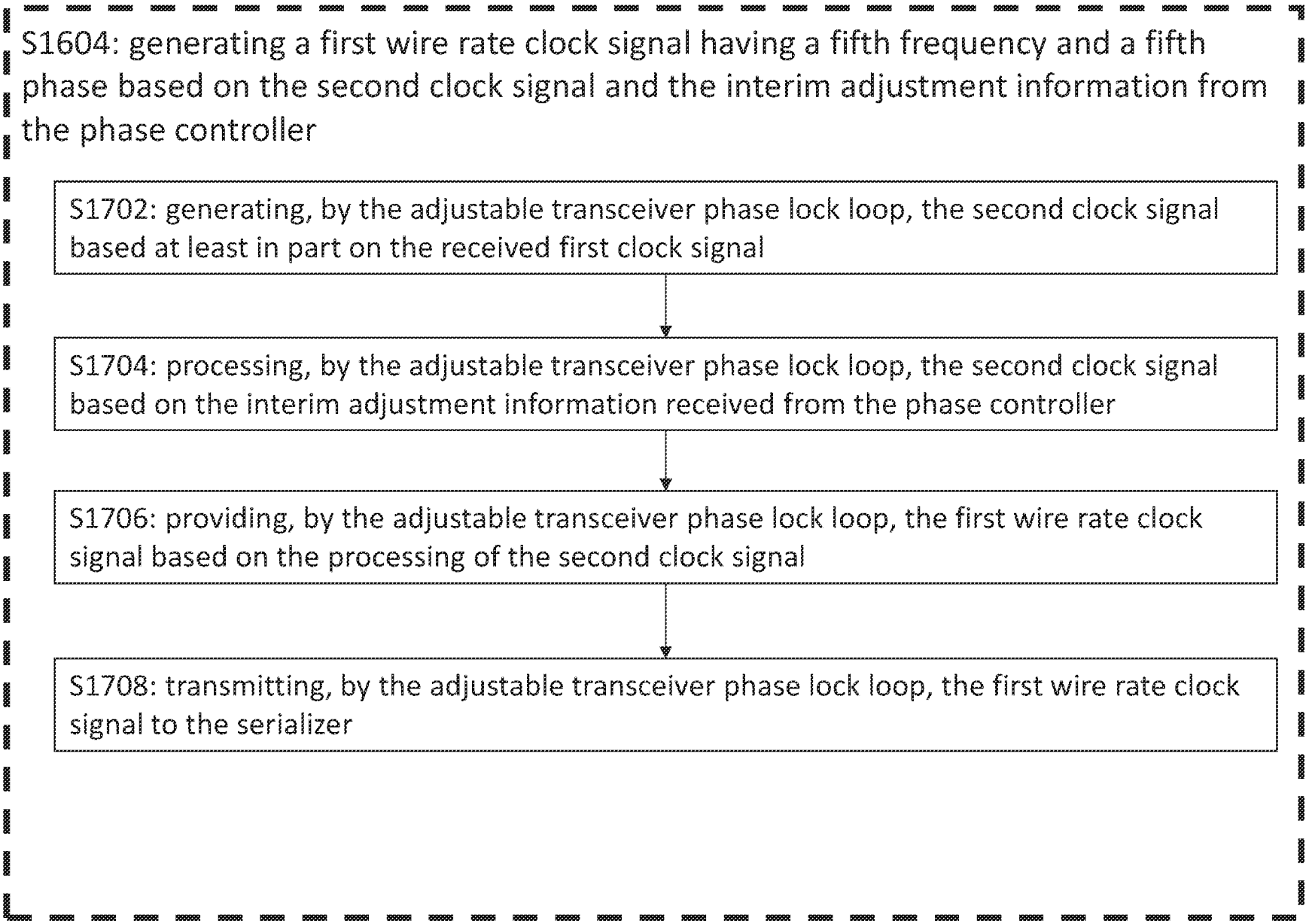

S1604: generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal and the interim adjustment information from the phase controller
S1702: generating, by the adjustable transceiver phase lock loop, the second clock signal based at least in part on the received first clock signal
S1704: processing, by the adjustable transceiver phase lock loop, the second clock signal based on the interim adjustment information received from the phase controller
S1706: providing, by the adjustable transceiver phase lock loop, the first wire rate clock signal based on the processing of the second clock signal
S1708: transmitting, by the adjustable transceiver phase lock loop, the first wire rate clock signal to the serializer

FIG. 17

PTO/SB/35 (07-09)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
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NONPUBLICATION REQUEST UNDER 35 U.S.C. 122(b)(2)(B)(i)

First Named Inventor	Nima Badizadegan
Title	FIELD PROGRAMMABLE GATE ARRAY WITH
Attorney Docket Number	00287-0016

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

/Keith J. Barkaus/ — Signature

2022-04-18 — Date

Keith J. Barkaus — Typed or printed name

51,431 — Registration Number, if applicable

212-336-8000 — Telephone Number

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

This collection of information is required by 37 CFR 1.213(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Filer:	Keith J. Barkaus/Victoria Gilmore
Attorney Docket Number:	00287-0016

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	80	80
UTILITY SEARCH FEE	2111	1	350	350
UTILITY EXAMINATION FEE	2311	1	400	400
Pages:				
UTILITY APPL SIZE FEE PER 50 SHEETS >100	2081	1	210	210
Claims:				
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1040**

Electronic Acknowledgement Receipt

EFS ID:	45498553
Application Number:	17723130
International Application Number:	
Confirmation Number:	3228
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	00287-0016
Receipt Date:	18-APR-2022
Filing Date:	
Time Stamp:	17:37:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

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Payment Type	CARD
Payment was successfully received in RAM	$1040
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	WebADS.pdf	192331 138e26c149a1b92a0fd334537ffa09c15440342e	no	8
Warnings:					
Information:					
2	Power of Attorney	1-PowerofAtty.pdf	347829 c9d927b2ecde34222f0dcf77500558ed5b64b8e4	no	2
Warnings:					
Information:					
3	Oath or Declaration filed	2-Declaration.pdf	157360 75ed7b6f11b5ccf5fd555e0db8081e4992c41060	no	1
Warnings:					
Information:					
4		3-Specification.pdf	473148 d9c7a6a8ab2c172508694f74923a7bba25643a19	yes	105

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Specification	1	101
Claims	102	104
Abstract	105	105

Warnings:					
Information:					
5	Drawings-only black and white line drawings	4-Figures.pdf	1159540 d276e458855e40689608f5c12049f9175c5b3d37	no	47

Warnings:					
Information:					
6	Nonpublication request from applicant	5-NonPublicationRqst.pdf	205823 9cc97da4ce3fe73c760560565fa58a0975eec5cf	no	2
Warnings:					
Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	46917 ba716f7470051d35e4bdff79481a431e0980cea8	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2582948		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00287-0016
	Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1

Legal Name				
Prefix	**Given Name**	**Middle Name**	**Family Name**	**Suffix**
	Nima		Badizadegan	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Salem	**State/Province**	NH	**Country of Residence** i	US

Mailing Address of Inventor:

Address 1	61 Kelly Rd.		
Address 2			
City	Salem	**State/Province**	NH
Postal Code	03079	**Country** i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	1912		
Email Address	ptodocket@arelaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP		
Attorney Docket Number	00287-0016	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	47	**Suggested Figure for Publication (if any)**	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00287-0016
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Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☒ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	1912		

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	
					Remove
Registration Number					
Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	
					Remove
Registration Number					

Additional Representative Information blocks may be generated within this form by selecting the **Add** button.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00287-0016
	Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove

Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	17236577	2021-04-21

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17236577	Continuation of	16937309	2020-07-23	11018678	2021-05-25

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16937309	Continuation of	16888218	2020-05-29	10763865	2020-09-01

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16888218	Continuation of	16670702	2019-10-31	10771069	2020-09-08

Prior Application Status	Pending	Remove

Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16670702	Claims benefit of provisional	62808404	2019-02-21

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00287-0016
	Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00287-0016
	Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00287-0016
	Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	HFT Solutions, LLC

Mailing Address Information For Applicant:

Address 1	65 Locust Avenue		
Address 2			
City	New Canaan	**State/Province**	CT
Country[i]	US	Postal Code	06840
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00287-0016
	Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	00287-0016
	Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e. g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Keith J. Barkaus/			Date (YYYY-MM-DD)	
First Name	Keith J.	Last Name	Barkaus	Registration Number	51431

Additional Signature may be generated within this form by selecting the Add button.