

Benjamin Carrion Schaefer

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EDUCATION

MBA , McGill University, Canada	2008 - 2010
Ph.D. , Reconfigurable Computing, The University of Birmingham, UK	1999 - 2003
M.Sc. , Microelectronics, Birmingham City University, UK	1998 - 1999
B.Eng. , Electronic Engineering, Universidad Politecnica, Madrid, Spain	1993 - 1997

EMPLOYMENT HISTORY

Assistant Dean Graduate Student Success , School of Engineering, UTD	2023 - present
Associate Professor , ECE dept., The University of Texas at Dallas	2022 - present
Assistant Professor , ECE dept., The University of Texas at Dallas	2016 - 2022
Assistant Professor , EIE dept., The Hong Kong Polytechnic University	2012 - 2016
Researcher , NEC Corp. Central R&D Laboratories, Japan	2007 - 2012
Postdoc , Seoul National University, Korea	2005 - 2007
Postdoc , University of California Los Angeles, USA	2003 - 2004

RESEARCH INTERESTS

Reconfigurable Computing, FPGAs, Electronic Design Automation (EDA), High-Level Synthesis (HLS), Hardware Security, Low-power design, Approximate Computing.

PROFESSIONAL RECOGNITIONS AND HONORS

GOMACTech 2025 Best Poster Award, 2025
35th Great Lakes Symposium on VLSI (GLSVLSI) best poster award, 2025
Winner of faculty 3 minute talk (f3mt) UT Dallas Jonsson School of Engineering, 2024
MVP Career Service Faculty Award UT Dallas Jonsson School of Engineering, 2023
UT Dallas Erik Jonsson School of Engineering dean's fellow, 2022-2023
32nd Great Lakes Symposium on VLSI (GLSVLSI) best paper award, 2022
UT Dallas Erik Jonsson School of Engineering & Computer Science best teacher award, 2022
34th Int'l Conference on VLSI Design (VLSID) Naresh Malipeddy honorable mention award, 2021
Best program committee member in GLSVLSI symposium, 2018
Hack at DAC competition, third place, 2017
Brain Korean 21 (BK21) scholarship, Seoul, Korea, 2005
Interdisciplinary Research Fund scholarship, University of Birmingham, UK, 1999
M.Sc. Birmingham City University, UK, awarded with distinction, 1999
GFTN Gesellschaft zur Förderung technischen Nachwuchses, Darmstadt, Germany, 1998

SCHOLARLY AND PROFESSIONAL SERVICE ACTIVITIES

Service within the University	
Member, CE Graduate Committee	2025 - 2026
Member, Search Committee	2024 - 2025
Member, Search Committee	2023 - 2024
Member, University Committee on Student Technology Requirements	2022 - 2023
Member, Search Committee	2022 - 2023
Member, CE Graduate Committee	2020 - 2021

Member, University Library Committee	2020 - 2021
Member, CE Graduate Committee	2019 - 2020
Member, University Library Committee	2019 - 2020
Member, Undergraduate Teaching Committee	2018 - 2019
Member, Search Committee	2018 - 2019
Member, Search Committee	2017 - 2018
Member, Undergraduate Teaching Committee	2016 - 2017

Journal Editorial Activities

Associate Editor, IEEE Transaction on Computer-Aided Design (TCAD)	2025-present
Associate Editor, IEEE Transaction on Sustainable Computing	2022-present
Associate Editor, Integration, The VLSI Journal (Elsevier)	2014 - 2022

Conference Organization, Executive Committee, Track chair

Track Chair, IEEE Design Automation and Test Europe (DATE)	2027
Track Chair, IEEE Design Automation and Test Europe (DATE)	2026
Track Chair, Innovative Applications of Artificial Intelligence (IAAI)	2026
General Chair , IEEE International Conference on Computer Design (ICCD)	2025
TPC Chair, IEEE International Conference on Computer Design (ICCD)	2024
Track Chair, IEEE Design Automation and Test Europe (DATE)	2025
General Chair , IEEE Dallas Circuits and Systems Conference (DCAS)	2024
Track Chair, ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)	2024
Track Chair (EDA), IEEE International Conference on Computer Design (ICCD)	2023
Technical Program co-Chair, IEEE Dallas Circuits and Systems Conference (DCAS)	2023
Track Chair (EDA), IEEE International Conference on Computer Design (ICCD)	2022
Workshop co-chair, 7th Workshop on Approximate Computing (AxC22)	2022
Special Sessions Chair, IEEE Dallas Circuits and Systems Conference (DCAS)	2022
Track co-Chair, ACM/IEEE International Conference on CAD (ICCAD)	2021
Track Chair, ACM/IEEE Design Automation Conference (DAC)	2021
Track Chair, ACM Great Lakes Symposium on VLSI (GLSVLSI)	2021
Track Chair, ACM/IEEE Design Automation Conference (DAC)	2020
Track Chair, ACM Great Lakes Symposium on VLSI (GLSVLSI)	2020
Track Chair, ACM/IEEE Design Automation Conference (DAC)	2019
Track Chair, ACM Great Lakes Symposium on VLSI (GLSVLSI)	2019
Local Arrangement Chair, IEEE Midwest Symposium on Circuits and Systems (MWSCAS)	2019
General Chair , ESLsyn conference, co-located with DAC	2014

Member of the Technical Program Committee

IEEE Conference on Field Programmable Technology (FPT)	2026
IEEE Conference on Field Programmable Gate Arrays (FPL)	2026
IEEE Reconfigurable Architectures Workshop (RAW)	2026
IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)	2026
IEEE Design Automation Conference (DAC)	2026
ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)	2026
ACM/IEEE International Conference on Computer Aided Design (ICCAD)	2025
IEEE Conference on Field Programmable Gate Arrays (FPL)	2025
IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)	2025
IEEE Design Automation Conference (DAC)	2025
IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)	2024
IEEE Design Automation and Test Europe (DATE)	2024
ACM Great Lakes Symposium on VLSI (GLSVLSI)	2023
ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)	2023
ACM/IEEE International Conference on Computer Aided Design (ICCAD)(student competition)	2022

IEEE Conference on Field Programmable Gate Arrays (FPL)	2022
IEEE Application-Specific Systems, Architectures and Processors (ASAP)	2022
ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)	2022
IEEE International Conference on Computer Design (ICCD)	2021
IEEE Transaction on Computers. TPC for special issue on Compiler Optimizations for FPGAs	2021
ACM/IEEE International Conference on Computer Aided Design (ICCAD)	2021
IEEE Application-Specific Systems, Architectures and Processors (ASAP)	2021
ACM/IEEE Design Automation Conference (DAC)	2021
IEEE Design Automation and Test Europe (DATE)	2021
IEEE Conference on Field Programmable Gate Arrays (FPL)	2021
ACM Great Lakes Symposium on VLSI (GLSVLSI)	2021
ACM/IEEE International Conference on Computer Aided Design (ICCAD)	2020
IEEE Application-Specific Systems, Architectures and Processors (ASAP)	2020
ACM/IEEE Design Automation Conference (DAC)	2020
IEEE Design Automation and Test Europe (DATE)	2020
IEEE Conference on Field Programmable Gate Arrays (FPL)	2020
ACM Great Lakes Symposium on VLSI (GLSVLSI)	2020
ACM/IEEE International Conference on Computer Aided Design (ICCAD)	2019
IEEE Application-Specific Systems, Architectures and Processors (ASAP)	2019
ACM/IEEE Design Automation Conference (DAC)	2019
ACM/IEEE Design Automation and Test Europe (DATE)	2019
IEEE Conference on Field Programmable Gate Arrays (FPL)	2019
ACM Great Lakes Symposium on VLSI (GLSVLSI)	2019
IEEE Conference on Field Programmable Gate Arrays (FPL)	2018
ACM Great Lakes Symposium on VLSI (GLSVLSI)	2018
ACM/IEEE Design Automation Conference (DAC)	2018
IEEE Conference on Field Programmable Gate Arrays (FPL)	2018
ACM Great Lakes Symposium on VLSI (GLSVLSI)	2018
ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)	2017
IEEE Conference on Field Programmable Gate Arrays (FPL)	2017
ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)	2016
Electronic System Level Synthesis Conference (ESLSyn)	2015
ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)	2015
Electronic System Level Synthesis Conference (ESLSyn)	2014
Electronic System Level Synthesis Conference (ESLSyn)	2013

NSF Reviewer

NSF Reviewer	2026
NSF Reviewer	2025
NSF Reviewer	2024
NSF Reviewer	2022
NSF Reviewer	2021
NSF Reviewer	2021
NSF Reviewer	2019

External PhD Reviewer

City University, HKSAR	2024
Columbia University, USA	2022
Universidad Politecnica de Madrid, Spain	2021
Universidad Politecnica de Madrid, Spain	2020
Visvesvaraya Technological University (VTU), India	2018

ACHIEVEMENTS IN ORIGINAL INVESTIGATION

Total: 154 Publications (3 Books, 3 Book chapters, 41 Journals, and 106 Conferences)
First author: 40 Publications (3 Books, 1 Book chapter, 19 Journals, and 17 Conferences)

Books

- [B4] **B. Carrion Schaefer**. *High-Level Synthesis Made Easy (Second Edition)*. 2nd. highX Technologies, 2026, pp. 1–183. URL: <http://www.hlsbook.com>.
- [B4] **B. Carrion Schaefer**. *High-Level Synthesis : Applications*. 1st. highX Technologies, 2025, pp. 1–98. URL: <http://www.hlsbook.com>.
- [B4] **B. Carrion Schaefer**. *High-Level Synthesis Made Easy*. 1st. highX Technologies, 2023, pp. 1–135. URL: <http://www.hlsbook.com>.

Book Chapters

- [BC4] Srinivas Katkoori and Sheikh Ariful Islam. *Source Code Obfuscation of Behavioral IPs: Challenges and Solutions, chapter 3*. 2020.
- [BC4] Wim Vanderbauwhede and Khaled Benkrid. *High-Level Synthesis: From Algorithm to Digital Circuit, chapter 7*. 2013.
- [BC4] Philippe Coussy and Adam Morawiec. *High-Level Synthesis: From Algorithm to Digital Circuit*. 2008.

Journals

- [J43] **B. Carrion Schafer** and Baharealsadat Parchamdar. “Approximate Computing in High-Level Synthesis: From Survey to Practical Implementation”. In: *ACM Computing Surveys* (Dec. 2025), pp. 1–20.
- [J43] **B. Carrion Schafer** and Chaitali G. Sathe. “From High-Level Synthesis Lite to High-Level Synthesis Full: Unlocking HLS tool Limitations”. In: *ACM Transactions on Design Automation of Electronic Systems (TODAES)* (Nov. 2025), pp. 1–16.
- [J43] Tejinder Kaur, Jose Luis Olvera-Cervantes, **B. Carrion Schafer** and Alonso Corona-Chavez. “Identification of lyophilized avocado powder adulteration using the cavity perturbation technique at microwave frequencies”. In: *Journal of Microwave Power and Electromagnetic Energy* 0.0 (2024), pp. 1–14.
- [J43] Qilin Si and **B. Carrion Schafer**. “MOSAIC: Maximizing ResOurce Sharing in Behavioral Application SpecIfic ProCessors”. In: *Elsevier Microprocessors and Microsystems (MICPRO)* 65 (2024), pp. 1–10.
- [J43] Md. Imtiaz Rashid and **B. Carrion Schafer**. “Robust and Efficient RTL to C Compiler Optimized for High-Level Synthesis”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 42.11 (Nov. 2024), pp. 1–9.
- [J43] T. Kaur, A. Gamez, J.L. Olvera, **B. Carrion Schaefer**, and A. Corona-Chavez. “I-TAINTED: Identification of Turmeric Adulteration using the Cavity Perturbation Technique and Technology optimized Machine Learning”. In: *IEEE Access* (2023), pp. 1–11.
- [J43] Md. Imtiaz Rashid and **B. Carrion Schafer**. “Fast and Inexpensive High-Level Synthesis Design Space Exploration : Machine Learning to the Rescue”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 42.11 (Nov. 2023), pp. 3939–3950.

- [J43] Q. Si, P. Chowdhury, R. Sreekumar, and **B. Carrion Schafer**. “Application Specific Approximate Behavioral Processor”. In: *IEEE Transactions on Sustainable Computing* (2022), pp. 1–15.
- [J43] P. Goswami, **B. Carrion Schafer** and D. Bhatia. “Machine Learning Based Fast and Accurate High Level Synthesis Design Space Exploration: From Graph to Synthesis”. In: *Integration* 88 (2022), pp. 116–124.
- [J43] Z. Wang and **B. Carrion Schafer**. “Learning from the Past: Efficient High-Level Synthesis Design Space Exploration for FPGAs”. In: *ACM Transactions on Design Automation of Electronic Systems (TODAES)* 27.4 (July 2022), pp. 1–23.
- [J43] Z. Wang, F. Lau, and **B. Carrion Schafer**. “SSSL: Secure Search Space Locking of Behavioral IPs”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2021), pp. 1–10.
- [J43] Q. Si, S. Shetty, and **B. Carrion Schafer**. “Building Complete Heterogeneous Systems-on-Chip in C: From Hardware Accelerators to CPUs”. In: *MDPI Electronics* (2021), pp. 1–15.
- [J43] P. Chowdhury and **B. Carrion Schafer**. “Leveraging Automatic High-Level Synthesis Resource Sharing to maximize Dynamical Voltage Overscaling with Error Control”. In: *ACM Transactions on Design Automation of Electronic Systems (TODAES)* (Sept. 2021), pp. 1–13.
- [J43] A. Yadav, S. Xu, **B. Carrion Schafer**, and A. Davoudi. “Hardware-assisted Simulation of Voltage-behind-reactance Models of Electric Machines on FPGA”. In: *IEEE Transactions on Energy Conversion* (2020), pp. 1–10.
- [J43] S. Liu, F. Lau, and **B. Carrion Schafer**. “Predictive Compositional Method to Design and Re-optimize Complex Behavioral Dataflows”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2020), pp. 1–12.
- [J43] **B. Carrion Schafer** and Z. Wang. “High-Level Synthesis Design Space Exploration: Past, Present and Future”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2020), pp. 1–12.
- [J43] Siyuan Xu, Shuangnan Liu, Yidi Liu, Anushree Mahapatra, Mónica Villaverde, Felix Moreno, and **B. Carrion Schafer**. “Design space exploration of heterogeneous MPSoCs with variable number of hardware accelerators”. In: *Microprocessors and Microsystems* 65 (2019), pp. 169–179.
- [J43] S. Xu and **B. Carrion Schafer**. “Toward Self-Tunable Approximate Computing”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 27.4 (Apr. 2019), pp. 778–789.
- [J43] David Aledo, **B. Carrion Schafer**, and Felix Moreno. “VHDL vs. SystemC: Design of Highly Parameterizable Artificial Neural Networks”. In: *IEICE Transactions on Information and Systems* E102.D.3 (2019), pp. 512–521.
- [J43] A. Mahapatra and **B. Carrion Schafer**. “VeriIntel2C: Abstracting RTL to C to maximize High-Level Synthesis Design Space Exploration”. In: *Integration* 64 (2019), pp. 1–12.
- [J43] John N. Randall, James H. G. Owen, Joseph Lake, Rahul Saini, Ehud Fuchs, Mohammad Mahdavi, S. O. Reza Moheimani, and **B. Carrion Schafer**. “Highly parallel scanning tunneling microscope based hydrogen depassivation lithography”. In: *Journal of Vacuum Science & Technology B* 36.6 (2018), 06JL05.
- [J43] Anushree Mahapatra, Yidi Liu, and **B. Carrion Schafer**. “Accelerating cycle-accurate system-level simulations through behavioral templates”. In: *Integration* 62 (2018), pp. 282–291.

- [J43] S. Xu and **B. Carrion Schafer**. “Exposing Approximate Computing Optimizations at Different Levels: From Behavioral to Gate-Level”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 25.11 (Nov. 2017), pp. 3077–3088.
- [J43] N. Veeranna and **B. Carrion Schafer**. “S3CBench: Synthesizable Security SystemC Benchmarks for High-Level Synthesis”. In: *J. Hardware and Systems Security* 1.2 (2017), pp. 103–113.
- [J43] N. Veeranna and **B. Carrion Schafer**. “Trust Filter: Runtime Hardware Trojan Detection in Behavioral MPSoCs”. In: *J. Hardware and Systems Security* 1.1 (2017), pp. 56–67.
- [J43] **B. Carrion Schafer**. “Parallel High-Level Synthesis Design Space Exploration for Behavioral IPs of Exact Latencies”. In: *ACM Trans. Des. Autom. Electron. Syst.* 22.4 (May 2017).
- [J43] **B. Carrion Schafer**. “Enabling High-Level Synthesis Resource Sharing Design Space Exploration in FPGAs Through Automatic Internal Bitwidth Adjustments”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 36.1 (Jan. 2017), pp. 97–105.
- [J43] N. Veeranna and **B. Carrion Schafer**. “Hardware Trojan Detection in Behavioral Intellectual Properties (IP’s) Using Property Checking Techniques”. In: *IEEE Transactions on Emerging Topics in Computing* 5.4 (Oct. 2017), pp. 576–585.
- [J43] **B. Carrion Schafer**. “Probabilistic Multi-knob High-Level Synthesis Design Space Exploration Acceleration”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 35.3 (Mar. 2016), pp. 394–406.
- [J43] **B. Carrion Schafer**. “Tunable Multiprocess Mapping on Coarse-Grain Reconfigurable Architectures With Dynamic Frequency Control”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 24.1 (Jan. 2016), pp. 324–328.
- [J43] **B. Carrion Schafer**. “Source Code Error Detection in High-Level Synthesis Functional Verification”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 24.1 (Jan. 2016), pp. 301–312.
- [J43] **B. Carrion Schafer**. “Hierarchical High-Level Synthesis Design Space Exploration with Incremental Exploration Support”. In: *IEEE Embedded Systems Letters* 7.2 (June 2015), pp. 51–54.
- [J43] **B. Carrion Schafer** and A. Mahapatra. “S2CBench: Synthesizable SystemC Benchmark Suite for High-Level Synthesis”. In: *IEEE Embedded Systems Letters* 6.3 (Sept. 2014), pp. 53–56.
- [J43] **B. Carrion Schafer** and K. Wakabayashi. “Machine learning predictive modelling high-level synthesis design space exploration”. In: *IET Computers Digital Techniques* 6.3 (May 2012), pp. 153–159.
- [J43] **B. Carrion Schafer** and K. Wakabayashi. “Divide and Conquer High-level Synthesis Design Space Exploration”. In: *ACM Transactions on Design Automation of Electronic Systems (TODAES)* 17.3 (July 2012), 29:1–29:19.
- [J43] **B. Carrion Schafer** and K. Wakabayashi. “Precision tunable RTL macro-modelling cycle-accurate power estimation”. In: *IET Computers Digital Techniques* 5.2 (Mar. 2011), pp. 95–103.
- [J43] **Benjamin Carrion Schafer** and Majid Sarrafzadeh. “Semi-Automatic Control Unit Generation for Complex VLSI Designs”. In: *IPSJ Transactions on System LSI Design Methodology* 5.4 (2010), pp. 234–243.

- [J43] **Benjamin Carrion Schafer**, Yusuke Iguchi, Wataru Takahashi, Shingo Nagatani, and Kazutoshi Wakabayashi. “Fixed Point Data Type Modeling for High Level Synthesis”. In: *IEICE Transactions on Electronics* E93.C.3 (2010), pp. 361–368.
- [J43] **B. Carrion Schafer** and K. Wakabayashi. “Design Space Exploration Acceleration Through Operation Clustering”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 29.1 (Jan. 2010), pp. 153–157.
- [J43] **B. Carrion Schafer** and T. Kim. “Autonomous temperature control technique in VLSI circuits through logic replication”. In: *IET Computers Digital Techniques* 3.1 (Jan. 2009), pp. 62–71.
- [J43] **B. Carrion Schafer** and T. Kim. “Hotspots Elimination and Temperature Flattening in VLSI Circuits”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 16.11 (Nov. 2008), pp. 1475–1487.
- [J43] **B. Carrion Schafer**, Steven F. Quigley, and Andrew H.C. Chan. “Acceleration of the Discrete Element Method (DEM) on a reconfigurable co-processor”. In: *Computers and Structures* 82.20 (2004), pp. 1707–1718.

Conference Papers

- [C107] Baharealsadat Parchamdar and **B. Carrion Schafer**. “Breaking Behavioral IPs Design Space Lock”. In: *Great Lakes Symposium on VLSI (Best Poster Award)*. GLSVLSI’25. Association for Computing Machinery, 2025, pp. 1–6.
- [C107] Sabrina Ahmed, Khaza Anuarul Hoque and **B. Carrion Schafer**. “Robust and Fault-Aware Design for Resilient Edge Computing AI Accelerators”. In: *Great Lakes Symposium on VLSI*. GLSVLSI’25. Association for Computing Machinery, 2025, pp. 1–6.
- [C107] Victoria Gammenthaler and **B. Carrion Schafer**. “Improving the Quality of the High-Level Synthesis Estimation Results through Multi-Level Predictive Models”. In: *Great Lakes Symposium on VLSI*. GLSVLSI’25. Association for Computing Machinery, 2025, pp. 1–6.
- [C107] C.G. Sathe, Y. Makris, **B. Carrion Schafer**. “FREEDOM: FPGA-based Hardware Redaction Emulator”. In: *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM 2025)*. 2025, pp. 1–5.
- [C107] C.G. Sathe, Y. Makris, **B. Carrion Schafer**. “FPGA-based Hardware Redaction Bitstream Fuzzing Attack”. In: *IEEE Dallas Circuits and Systems (DCAS)*. 2025, pp. 1–5.
- [C107] C.G. Sathe, A. Fowler, C. Sechen, **B. Carrion Schafer**, Y. Makris, M. Zaman and R. Narumi. “What to Redact? Guidelines for Cost-Effective Hardware Intellectual Property Protection (Best Poster Award)”. In: *GOMACTech*. 2025, pp. 1–4.
- [C107] B. Parchamdar and **B. Carrion Schafer**. “ADVISOR: Approximate Computing-friendly High-Level Synthesis Design Space Explorer”. In: *ACM/IEEE Design Automation Conference (DAC)*. June 2025, pp. 1–6.
- [C107] M. Imtiaz Rashid and **B. Carrion Schafer**. “Making Legacy Hardware Robust against Side Channel Attacks via High-Level Synthesis”. In: *Asia and South Pacific Design Automation (ASP-DAC)*. Jan. 2025, pp. 1–6.
- [C107] C.G. Sathe, Y. Makris, and **B. Carrion Schafer**. “Efficient and Secure Cloud-based Split Logic Synthesis”. In: *Asia and South Pacific Design Automation (ASP-DAC)*. Jan. 2025, pp. 1–6.
- [C107] Q. Si and **B. Carrion Schafer**. “HAMMER: Hardware-aware Runtime Program Execution Acceleration through runtime reconfigurable CGRAs”. In: *Asia and South Pacific Design Automation (ASP-DAC)*. Jan. 2025, pp. 1–6.

- [C107] M. Imtiaz Rashid and **B. Carrion Schafer**. “VeriPy: A Python-Powered Framework for Parsing Verilog HDL and High-Level Behavioral Analysis of Hardware”. In: *IEEE Dallas Circuits and Systems (DCAS)*. Apr. 2024, pp. 1–6.
- [C107] B. Parchamdar and **B. Carrion Schafer**. “Investigating the Effect of Hyper-Parameter Settings on Simulated Annealing-based High-Level Synthesis Design Space Exploration”. In: *IEEE Dallas Circuits and Systems (DCAS)*. Apr. 2024, pp. 1–5.
- [C107] B. Parchamdar and **B. Carrion Schafer**. “Finding Bugs in RTL Descriptions: High-Level Synthesis to the Rescue”. In: *ACM/IEEE Design Automation Conference (DAC)*. June 2024, pp. 1–6.
- [C107] S. Shetty and **B. Carrion Schafer**. “Facilitating the Design of complete System-on-Chip through High-Level Synthesis”. In: *GOMACTech*. 2024, pp. 1–4.
- [C107] S. Yu and **B. Carrion Schafer**. “Temperature Control through dynamic Approximation”. In: *GOMACTech*. 2024, pp. 1–4.
- [C107] **B. Carrion Schafer** and C.G. Sathe. “Circumventing Restrictions in commercial High-Level Synthesis Tools”. In: *Design, Automation, and Test in Europe (DATE)*. Mar. 2024, pp. 1–2.
- [C107] Qilin Si and **B. Carrion Schafer**. “PEPA: Performance Enhancement of Embedded Processors through HW Accelerator Resource Sharing”. In: *Great Lakes Symposium on VLSI. GLSVLSI’23*. Association for Computing Machinery, 2023, pp. 1–6.
- [C107] Qilin Si and **B. Carrion Schafer**. “ADVICE: Automatic Design and Optimization of Behavioral Application Specific Processors”. In: *Great Lakes Symposium on VLSI. GLSVLSI’23*. Association for Computing Machinery, 2023, pp. 1–6.
- [C107] Md Imtiaz Rashid, A.H. Torabi and **B. Carrion Schafer**. “CERTIFY: Automatic Measuring the Quality of High-Level Synthesis”. In: *IEEE International Symposium on Circuits and Systems (ISCAS)*. May 2023, pp. 1–5.
- [C107] Md. Imtiaz and **B. Carrion Schafer**. “MIRROR: Maximizing the Re-usability of RTL through RTL to C Compiler”. In: *Design, Automation, and Test in Europe (DATE)*. Mar. 2023, pp. 1–6.
- [C107] C.G. Sathe, Y. Makris, and **B. Carrion Schafer**. “MANTIS: Machine Learning-Based Approximate Modeling of Redacted Integrated Circuits”. In: *Design, Automation, and Test in Europe (DATE)*. Mar. 2023, pp. 1–6.
- [C107] A. Hossein Md I. Rashid and **B. Carrion Schafer**. “Automatic Modernization of Hardware Assets”. In: *GOMACTech*. 2023, pp. 1–5.
- [C107] C. Sathe Md I. Rashid and **B. Carrion Schafer**. “ROPE: Re-usability Lock of Behavioral Intellectual Property”. In: *GOMACTech*. 2023, pp. 1–5.
- [C107] Prattay Chowdhury, Jorge Castro Godinez, and **B. Carrion Schafer**. “Approximating HW Accelerators through Partial Extractions onto shared Artificial Neural Networks”. In: *Asia and South Pacific Design Automation (ASP-DAC)*. Jan. 2023, pp. 1–6.
- [C107] P. Chowdhury, C.G. Sathe, **B. Carrion Schafer**. “Predictive Model Attack for Embedded FPGA Logic Locking”. In: *International Symposium on Low Power Electronics and Design (ISLPED)*. ISLPED ’22. ACM/IEEE, 2022, pp. 1–6.
- [C107] C.G. Sathe, Y. Makris and **B. Carrion Schafer**. “Investigating the Effect of different eFPGAs fabrics on Logic Locking through HW Redaction”. In: *Dallas Circuits and Systems Conference (DCAS)*. DCAS’22. IEEE, 2022, pp. 1–6.

- [C107] Q. Si and **B. Carrion Schafer**. “Optimizing Behavioral Near On-Chip Memory Computing Systems”. In: *International Conference on Application-specific Systems, Architectures and Processors (ASAP)*. ASAP’22. IEEE, 2022, pp. 1–7.
- [C107] Md Imtiaz Rashid and **B. Carrion Schafer**. “Fast Parallel High-Level Synthesis Design Space Explorer: Targeting FPGAs to accelerate ASIC Exploration”. In: *Great Lakes Symposium on VLSI (Best Paper Award)*. GLSVLSI ’22. Association for Computing Machinery, 2022, pp. 1–6.
- [C107] Md Imtiaz Rashid, Qilin Si and **B. Carrion Schafer**. “Modernizing Hardware Circuits through High-Level Synthesis”. In: *IEEE International Symposium on Circuits and Systems (ISCAS)*. May 2022, pp. 1–5.
- [C107] **B. Carrion Schafer**. “Hotspot Mitigation through Multi-Row Thermal-aware Re-Placement of Logic Cells based on High-Level Synthesis Scheduling”. In: *Asia and South Pacific Design Automation (ASP-DAC)*. Jan. 2022, pp. 1–6.
- [C107] Md Imtiaz Rashid and **B. Carrion Schafer**. “Improving the Quality of Hardware Accelerators through automatic Behavioral Input Language Conversion in HLS”. In: *Asia and South Pacific Design Automation (ASP-DAC)*. Jan. 2022, pp. 1–6.
- [C107] Z. Wang, S. O. Mohammed, Y. Makris and **B. Carrion Schafer**. “Functional Locking through Omission: From HLS to Obfuscated Design”. In: *IEEE 39th International Conference on Computer Design (ICCD)*. Nov. 2021, pp. 1–8.
- [C107] P. Chowdhury and **B. Carrion Schafer**. “ADAPT: ANN-Controlled System-Level Runtime Adaptable APproximate CompuTing”. In: *IEEE 39th International Conference on Computer Design (ICCD)*. Nov. 2021, pp. 1–4. (invited paper).
- [C107] Prattay Chowdhury and **B. Carrion Schafer**. “BEACON : BEst Approximations for Complete BehaviOral HeterogeNeous SoCs”. In: *International Symposium on Low Power Electronics and Design (ISLPED)*. ISLPED ’21. ACM/IEEE, 2021, pp. 1–6.
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- [C107] Z. Wang and **B. Carrion Schafer**. “Machine Learning to Set Meta-Heuristic Specific Parameters for High-Level Synthesis Design Space Exploration”. In: *ACM/IEEE Design Automation Conference (DAC)*. July 2020, pp. 1–6.
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- [C107] Z. Wang, J. Chen, and **B. Carrion Schafer**. “Efficient and Robust High-Level Synthesis Design Space Exploration through offline Micro-kernels Pre-characterization,” in: *Design, Automation Test in Europe Conference Exhibition (DATE)*. Mar. 2020, pp. 1–6.
- [C107] Bo Hu, Mustafa Shihab, William Swartz, Yiorgos Makris, **B. Carrion Schafer**, and Carl Sechen. “OAn Efficient MILP-Based Aging-Aware Floorplanner for Multi-Context Coarse-Grained Runtime Reconfigurable FPGAs”. In: *2020 Design, Automation Test in Europe Conference Exhibition (DATE)*. Mar. 2020, pp. 1–6.
- [C107] S. Xu and **B. Carrion Schafer**. “On the Design of High Performance HW Accelerator through High-level Synthesis Scheduling Approximations”. In: *Design, Automation Test in Europe Conference Exhibition (DATE)*. Mar. 2020, pp. 1–6.
- [C107] Bo Hu, Mustafa Shihab, William Swartz, Yiorgos **B. Carrion Schafer** Makris, and Carl Sechen. “Extending the Lifetime of Coarse-grained Runtime Reconfigurable FPGAs by Balancing Processing Element Usage,” in: *International Conference on Field-Programmable Technology (FPT)*. Dec. 2019.
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- [C107] S. Xu and **B. Carrion Schafer**. “Low Power Design of Runtime Reconfigurable FPGAs through Contexts Approximations”. In: *IEEE 37th International Conference on Computer Design (ICCD)*. Nov. 2019.
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- [C107] S. Xu and **B. Carrion Schafer**. “Autonomous Temperature Management through Selective Control of Exact-Approximate Tiles”. In: *IEEE 36th International Conference on Computer Design (ICCD)*. Oct. 2018, pp. 346–349.
- [C107] F. N. Taher, M. Kishani, and **B. Carrion Schafer**. “Design and Optimization of Reliable Hardware Accelerators: Leveraging the Advantages of High-Level Synthesis”. In: *IEEE 24th International Symposium on On-Line Testing And Robust System Design (IOLTS)*. July 2018, pp. 232–235.
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- [C107] Farah Naz Taher, Joseph Callenes-Sloan, and **B. Carrion Schafer**. “A Machine Learning Based Hard Fault Recuperation Model for Approximate Hardware Accelerators”. In: *55th Annual Design Automation Conference. DAC ’18*. San Francisco, California: Association for Computing Machinery, 2018.
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- [C107] Y. Liu, M. Villaverde, F. Moreno, and **B. Carrion Schafer**. “Characterization and optimization of behavioral hardware accelerators in heterogeneous MPSoCs”. In: *12th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*. July 2017, pp. 1–8.
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- [C107] Yidi Liu and **B. Carrion Schafer**. “Adaptive combined macro and micro-exploration of concurrent applications mapped on shared bus Reconfigurable SoC”. In: *Electronic System Level Synthesis Conference (ESLsyn)*. June 2015, pp. 11–16.
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- [C107] Y. Liu and **B. Carrion Schafer**. “HW acceleration of multiple applications on a single FPGA”. In: *International Conference on Field-Programmable Technology (FPT)*. Dec. 2014, pp. 284–285.
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- [C107] A. Mahapatra and **B. Carrion Schafer**. “Machine-learning based simulated annealer method for high level synthesis design space exploration”. In: *Proceedings of the 2014 Electronic System Level Synthesis Conference (ESLsyn)*. May 2014, pp. 1–6.
- [C107] **B. Carrion Schafer**. “Allocation of FPGA DSP-macros in multi-process high-level synthesis systems”. In: *19th Asia and South Pacific Design Automation Conference (ASP-DAC)*. Jan. 2014, pp. 616–621.
- [C107] **B. Carrion Schafer**. “Automatic partitioning of behavioral descriptions for high-level synthesis with multiple internal throughputs”. In: *Electronic System Level Synthesis Conference (ESLsyn)*. May 2013, pp. 1–6.

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- [C107] **B. Carrion Schafer**, Y. Lee, and T. Kim. “Temperature-Aware Compilation for VLIWProcessors”. In: *13th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2007)*. Aug. 2007, pp. 426–431.
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- [C107] **B. Carrion Schafer**, S. F. Quigley, and A. H. C. Chan. “Numeric Modeling of the Mechanical interaction between non-biological particles using reconfigurable computing”. In: *9th Annual conference of the Association for Computational Mechanics in Engineering (ACME)*. 2001, pp. 53–56.

Patents

- [P2] **B. Carrion Schafer**. *Method and Apparatus for Incremental Design Space Exploration*. U.S. Patent 8,977,996 B2.
- [P2] **B. Carrion Schafer**. *Method and Apparatus for Design Space Exploration*. JP Patent 2012-522281.

RESEARCH IMPACT AND CITATIONS

h-index (Google Scholar January 2025): 26
i10-index (Google Scholar January 2025): 45
Citations (Google Scholar January 2025): 2402

SOFTWARE ARTIFACTS RELEASED

FREEDOM: FPGA-based Hardware Redaction Emulator

Hardware redaction emulation framework that allows to quickly prototype ASIC+eFPGA designs onto a single low-cost FPGA. The emulator is available at <https://github.com/chaitalisathe/FREEDOM>. The framework only requires a Terasic DE1-SoC standard board.

DSE2Frame: DSE Explorer Framework

DSEFrame is a QT-based open source development framework to create and visualize High-Level Synthesis (HLS) design space exploration results. The development framework is freely available online at <https://github.com/DARCLabHao/DSEframe>.

S2CBench: Synthesizable SystemC Benchmark Suite

S2CBench is collection of over 20 SystemC benchmarks from different domain that comply with the latest Accelera's SystemC synthesizable subset. The benchmark suite is freely available online at <https://sourceforge.net/projects/s2cbench/> from where it has been downloaded over 1,000 times.

S3CBench: Security Synthesizable SystemC Benchmark Suite

S3CBench is the extension of the S2CBench benchmarks instrumented with malicious alterations a.k.a. Hardware Trojan that when triggered lead to deviation of the benchmark from its original intended behavior . The benchmark suite is freely available online at <https://sourceforge.net/projects/s3cbench/> from where it has been downloaded over 300 times.

UNIVERSITY COURSES TAUGHT

At the University of Texas at Dallas

Year	Semester	Code	Type	Title, Credits, Students
2025	Fall	EEDG/CE6370	Grad/elec	Reconfigurable Systems, 3, 48
2024	Fall	EEDG/CE6370	Grad/elec	Reconfigurable Systems, 3, 43
2024	Summer	EE/CE4304	Under/core	Computer Architecture, 3, 14
2023	Fall	EEDG/CE6304	Grad/core	Computer Architecture, 3, 60
2023	Fall	EEDG/CE6370	Grad/elec	Reconfigurable Systems, 3, 48
2023	Summer	EE/CE4304	Under/core	Computer Architecture, 3, 16
2022	Fall	EE/CE4307	Under/core	Embedded Systems, 3, 37
2022	Fall	EEDG/CE6304	Grad/core	Computer Architecture, 3, 55
2022	Summer	EE/CE4304	Under/core	Computer Architecture, 3, 10
2022	Spring	EE/CE4307	Under/core	Embedded Systems, 3, 60
2021	Fall	EEDG/CE6331	Grad/elec	High-Level Synthesis, 3, 8
2021	Fall	EEDG/CE6304	Grad/core	Computer Architecture, 3, 60
2021	Spring	EE/CE4307	Under/core	Embedded Systems, 3, 55
2020	Spring	EEDG7V81	Grad/elec	High-Level Synthesis, 3, 7
2020	Fall	EEDG/CE6304	Grad/core	Computer Architecture, 3, 43
2020	Spring	EE/CE4307	Under/core	Embedded Systems 3, 60
2019	Fall	EEDG7V81	Grad/elec	High-Level Synthesis, 3, 7
2019	Fall	EEDG/CE6304	Grad/core	Computer Architecture, 3, 43
2019	Spring	EE/CE4307	Under/core	Embedded Systems, 3, 49
2018	Fall	EEDG7V81	Grad/elec	High-Level Synthesis, 3, 15
2018	Fall	EEDG6304	Grad/core	Computer Architecture, 3, 13
2018	Spring	EEDG6304	Grad/core	Computer Architecture, 3, 13
2018	Spring	EE/CE4370	Under/core	Embedded Systems, 3, 43
2017	Fall	EEDG/CE6304	Grad/core	Computer Architecture, 3, 16
2017	Spring	EEDG/CE6304	Grad/core	Computer Architecture, 3, 16

At the Hong Kong Polytechnic University

Year	Semester	Code	Type	Title, Credits, Students
2016	Spring	EIE4110	Under/elect	VLSI&CAD, 3, 31
2015	Fall	EIE511	Grad/elect	VLSI System design,3, 15
2014	Spring	EIE4110	Under/elect	VLSI&CAD, 3, 63
2014	Spring	EIE3361	Under/core	Computer Fund, 3, 62
2014	Fall	EIE511	Grad/elect	VLSI System design, 3, 26
2014	Fall	EIE2105	Under/core	Digital Design, 3, 28
2014	Spring	EIE4110	Under/elect	VLSI&CAD, 3, 29
2014	Spring	EIE3361	Under/core	Computer Fund, 3, 74
2013	Fall	EIE2105	Under/elect	Digital Design, 3, 35
2013	Spring	EIE305	Under/elect	Digital Circuits, 3, 18
2013	Spring	EIE361	Under/core	Computer Fund, 3, 56
2013	Spring	EIE410	Under/elect	VLSI&CAD, 3, 22

STUDENT SUPERVISION SUMMARY

Ph.D. students currently supervised:	6
M.S. students currently supervised:	3
Ph.D. students graduated:	15
M.S. students graduated:	20
Undergraduate researchers supervised:	9
High School Students supervised:	3

GRADUATE STUDENTS CURRENTLY SUPERVISED

Doctoral Students

Ph.D. Candidate	Research Area	Years
Sabrina Ahmed	Sustainable HW Design	2023–present
Victoria Gammenthaler	Hardware Security	2024–present
Daksith Chandrasekera	LLM-based EDA	2025–present
Salam Kadhim Al-Khammasi	LLM-based VLSI System Generation	2026–present
Adam Kayyal	LLM-based Design Optimization	2026–present
Emmanuel Llanes	TBD (starting in fall)	2026–present

Master Students

MS	Research Area	Years
Mark Ivey	Efficient LLM implementations on FPGAs	2025–present
Sathwik Sudhindranath	Complex DSP applications on FPGAs	2026–present
Samarth Nandeesh	Custom FPGA fabrics for HLS generated Designs	2026–present

GRADUATE STUDENTS PREVIOUSLY SUPERVISED

Doctoral Advisement/Direction

Name	Year	Dissertation (compact)	Job
Baharealsadat Parchamdar	2026	HLS optimization/applications	–
Chaitali Sathe	2025	HW IP security attacks/defense	–
Md Imtiaz Rashid	2024	HLS circuit modernization	Univ. of Florida (Postdoc)
Qilin Si	2023	Behavioral processors	NVIDIA
Prattay Chowdhury	2022	Approximate computing systems	Qualcomm
Zi Wang	2021	HLS design space search	Cadence
Bo Hu	2021	Thermal/security HLS design	Apple
Jianqi Chen	2020	HLS security/low-power design	Cirrus Logic
Anjana Balachandran	2020	Fault-tolerant circuits	Huawei
Zhiqi Zhu	2020	Fault-tolerant accelerators	Nubis Comm.
Farah Naz Taher	2019	HW fault detection/mitigation	Raytheon
Siyuan Xu	2019	Robust approximate computing	MathWorks
Shuangnan Liu	2019	Behavioral dataflow design	Cadence
Ansuhree Mahapatra	2018	RTL abstraction for HLS	ASTRI
Nandeesh Veeranna	2017	BIP protection	NTU (Postdoc)

Masters Advisement/Direction

Name	Year	Dissertation (short)	Job After Graduation
Adam Kayyal	2026	Synthesis-aware HLS DSE	UT Dallas (PhD), USA
Valliyappan Senthilkumar	2023	ANN optimization HW/SW	Marvell Tech., USA
Amir H. Torabi	2023	HLS quality estimation	UT Dallas (PhD), USA
Santosh Shetty	2020	Behavioral SoC generation	AMD, India
Akshay R. Krisnani	2020	CNN in-situ training	Intel, USA
Yiheng Gao	2020	HLS design space search	Nokia, USA
Rohit Sreekumar	2020	Bespoke processors	Amazon, USA
Himanshu Patra	2019	HLS language conversion	Intel, USA
Maheswaran R. Babu	2019	FPGA diversity accel.	Intel, USA
Mihir Shah	2018	Partial reconfig. architecture	Varex Imaging, USA
Monica Gowda	2018	HLS exploration	MicroChip, USA
Vinay Dasandi	2018	Bitwidth optimization	Delphi, USA
Songseok Choi	2018	FPGA acceleration automation	SK Hynix, Korea
Susmitha Gogineni	2017	OpenCL accel.	Texas Instruments, USA
Siyuan Xu	2015	SoC design exploration	PhD, UT Dallas
Zhendong Gao	2015	FPGA voice viz.	PCCW, Hong Kong
Jieshi Chen	2015	(not specified)	DJI, China
Yidi Liu	2015	Parallel HW acceleration	Huawei
Yu Li	2014	FPGA gaming console	ZTE, China
Xiaotong Li	2014	HW Trojan detection	TCL, China

VISITING GRADUATE STUDENTS SUPERVISED

Takafumi Miyazaki (Visiting from Ritsumeikan University, Japan)	09/2018-10/2018
Shuangnan Liu (Visiting from Hong Kong Polytechnic University, HKSAR)	09/2017-12/2018
Nandeesh Veeranna (Visiting from Hong Kong Polytechnic University, HKSAR)	04/2017-07/2017
Monica Villaverde (Visiting from Universidad Politecnica de Madrid, Spain)	01/2017-04/2017

UNDERGRADUATE AND HIGH SCHOOL STUDENTS SUPERVISED

Undergraduate Students

Juan Diego Rosero Rodriguez	Spring 2026
Omar Abiola Abioye	Spring 2025
Shruthigna Chandupatla	Spring 2024
Axel Gamez (Qualcomm Research Award Recipient)	Fall 2022
Preston T. Glenn	Summer and Fall 2021
Kimberly Klein (Qualcomm Research Award Recipient)	Spring 2021
Michael Nelson	Fall and Spring 2017/2018
Rodolfo Martinez	Summer 2018
Ryota Watanabe	Summer 2018
Kristen Nguyen	Summer 2018
Sean Kennedy	Summer 2018

High School Students

Ishaan Javali	Summer 2019
Alondra Ramos	Summer 2018
Natasha Trayers	Summer 2018

KEYNOTES, INVITED TALKS AND SHORT COURSES TAUGHT

B. Carrion Schaefer, “Fast and Efficient Domain Specific Hardware Design”, The University of Houston, USA, August, 2024.

B. Carrion Schaefer, “C-based VLSI Design: Making Hardware Design Easier”, Hiroshima City University, Japan, July, 2024.

B. Carrion Schaefer, “Career Development: Hiring and Promotion”, DAC Early Career Workshop, San Francisco, USA, June, 2024.

B. Carrion Schaefer and Jeff Roane, “HLS Adoption and Key Technologies: Rethinking the use of High-Level Synthesis: From FPGA Prototyping to ASIC Design”, Cadence Lunch and Learn, Dallas, USA, August, 2023.

B. Carrion Schaefer, “Techniques for Finding Security Vulnerabilities in SoCs”, ACM/IEEE Design Automation Conference (DAC), San Francisco, USA, June, 2018.

B. Carrion Schafer, “Behavioral IPs Micro-architectural Diversity and its Applications”, ESLSyn, San Francisco, Co-located with DAC, June 2015,

B. Carrion Schaefer and J.H. Anderson, “FPGA high-level synthesis: from software to programmable hardware”, tutorial delivered at the ACM/IEEE Asia-South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan, January 2015.

A. Mahapatra and **B. Carrion Schaefer**, “S2CBench:Synthesizable SystemC Benchmark Suite for HighLevel Synthesis”, 20th meeting of the North American SystemC Users Group,San Francisco, June, 2014.

B. Carrion Schaefer, “The ESL Hotspot - Where Software and Hardware Meet”, Design Automation Conference (DAC), 10th annual ESL Symposium, San Francisco, (invited panelist), 2012.

B. Carrion Schaefer, “High-Level Synthesis Production Deployment: Are We Ready?”, Design Automation Conference (DAC), San Francisco, (invited speaker), 2012.

B. Carrion Schaefer, “Challenges and Opportunities of Behavioral Level SoC Design”, ESLSyn, Co-located with DAC, San Francisco, (Keynote speaker), 2012.

GRANTS, CONTRACTS, GIFTS AND DONATIONS

Sponsor Type	Total Funding (\$)	My Share (\$)
U.S. Federal (NSF, ONR, AFRL/AFWERX)	3,347,139	1,211,799
Industry (Boeing, Huawei, Texas Instruments)	224,000	107,000
International Government (NATO, HK UGC, NSFC China)	443,000	134,333
University / Internal (JSRI)	20,000	10,000
Equipment / Software Grants	25,000	25,000
Total	4,059,139	1,488,132

Office of Naval Research (ONR), Self-aware Computing Through AI (Sole PI). 2025-2027
Total amount : \$169,729

NSF, Advancing Innovation in Master of Science and Engineering Scholars Career Development (co-PI w. PI Pearson, UTD). 2025-2030
Total amount : \$2,000,000

NSF CHEST I/UCRC, Investigating the Weaknesses of IP Protection through eFPGA-based Hardware Redaction (PI w. co-PI Makris). Continuation grant. 2024-2025
Total amount : \$75,000

NSF, Collaborative Research: DESC: Type I: SEEDED: Sustainability-aware Reliable and Reusable AI Hardware Design (co-PI w. PI Hoque, University of Missouri). 2023-2026
Total amount : \$600,000
Amount UTD: \$260,00

NSF CHEST I/UCRC, Investigating the Weaknesses of IP Protection through eFPGA-based Hardware Redaction (PI w. co-PI Makris). 2023-2024
Total amount : \$65,000

Jonsson School Research Initiative (JSRI), UTD, Methods for Practical Design for Trust of Complex System-on-Chip (PI w. Co-PI Wong) 2023-2024
Total amount : \$20,000

NSF CHEST I/UCRC,CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming(co-PI w. PI-Makris and Sechen). Continuation grant 2022-2023
Total amount : \$125,000

NSF CHEST I/UCRC,CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming(co-PI w. PI-Makris and Sechen). Continuation grant 2021-2022
Total amount : \$125,000

AFWERX, Microelectronics Challenge Phase III (lead-PI w. Makris and Sechen) 2020
Total amount : \$200,000

NSF CHEST I/UCRC,CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming(co-PI w. PI-Makris and Sechen) 2020-2021
Total amount : \$100,000

Boeing/AFRL (co-PI w. PI-Makris and Sechen) 2020
Total amount : \$150,000

AFWERX, Microelectronics Challenge Phase II (lead-PI w. Makris and Sechen) 2019
Total amount : \$88,410

NATO, Nerve Agent Detection, (co-PI w. PI-Llamas and Mung) 2019-2022
Total amount : \$236,000

Huawei USA, Based Band SoC Approximate Computing (Sole PI) 2018
Total amount : \$60,000

Texas Instruments (Sole PI) 2018
Total amount : \$14,000

NEC Corporation, Software Grant (CyberWorkBench Software license donation) 2017
Value: \$10,000

Altera Equipment Grant (Arria SoC and DE1 FPGA Boards) 2017
Value: \$7,000

Xilinx Equipment Grant (Virtex-5 and Zynq FPGA Boards) 2017
Total amount : \$8,000

Early Career Scheme, University Grant Council, Hong Kong (Sole PI) 2014
Total amount : HKD \$677,000 (\$87,000)

National Natural Science Foundation of China (co-PI w. PI-Lau and Ho) 2014
Total amount : RMB \$750,000 (\$120,000)

PROFESSIONAL MEMBERSHIPS AND LICENSES

IEEE Senior Member since 2010