

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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OPTIVER US LLC and OPTIVER TRADING US LLC,  
Petitioners

v.

HFT SOLUTIONS, LLC,  
Patent Owner.

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Case No. IPR2026-00383  
U.S. Patent No. 12,107,587

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**Unopposed Motion for Leave to File**

**Corrected Petition and Corrected Expert Testimony**

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## I. INTRODUCTION

Petitioners respectfully seek leave to file a corrected petition and a corrected expert declaration in this proceeding. These corrections are clerical or typographical errors, and it is self-evident that the errors are inadvertent. Indeed, Patent Owner reviewed the redlines of these proposed corrections and confirmed it will not oppose Optiver's corrections as "all edits appear to be formatting, grammatical, and cleric edits rather than anything substantive."<sup>1</sup>

No new substance is added, and there are no material changes to the analyses presented in the Petition. The errors are readily apparent, Petitioners diligently sought correction, correction would neither prejudice Patent Owner nor negatively impact this proceeding, and Patent Owner does not oppose this request. Accordingly, pursuant to 37 C.F.R. § 42.104(c), Petitioner's Motion should be granted.

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<sup>1</sup> Petitioners emailed counsel for Patent Owner on June 8, 2026 to confirm whether counsel will represent Patent Owner in this proceeding and to convey Petitioners' intent to seek the corrections at issue. On June 9, 2026, counsel for Patent Owner confirmed representation, and requested Petitioners for the proposed corrections. On the same day, Petitioners provided Patent Owner with redlines of all proposed corrections. On June 11, 2026, Patent Owner confirmed "all edits appear to be formatting, grammatical, and cleric edits rather than anything substantive," and as such it will not oppose Optiver's corrections.

## II. FACTUAL BACKGROUND

On June 2, 2026, Petitioners filed a Petition requesting *inter partes* review of U.S. Patent No. 12,107,587. Subsequent to filing the Petition, Petitioner noticed typographical and clerical errors in the Petition and the accompanying Declaration of Dr. Ben Carrion-Schaefer, and further the absence of Dr. Benjamin Carrion-Schaefer's CV in the filings. On June 8, 2026, Petitioners promptly contacted the Board administrative staff to inquire on recommendations for correcting the errors and was advised to communicate with Patent Owner. On the same day, the Petition was accorded a filing date by the Board. After confirmation that Patent Owner does not oppose Petitioners' corrections, on June 11, 2026, Petitioners contacted the Board via email seeking permission to file the corrective documents. On June 18, 2026, the Board authorized filing this Motion.

Petitioners now moves the Board for leave to file the corrected Petition to make the corrections noted below.<sup>2</sup>

| Page(s) | Current                                                 | Correction                                                                                                                                                                                 |
|---------|---------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ix      | There are no other administrative proceedings at issue. | There are no other administrative proceedings at issue. <b>Petitioners have filed or intend to file petitions for inter partes review regarding four additional patents—U.S. Pat. Nos.</b> |

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<sup>2</sup> In addition, Petitioners intend to update the word count after corrections and execute the signature lines with lead counsel's signature on the date of filing.

| Page(s) | Current                                                                                                                                                                                                                     | Correction                                                                                                                                                                                                                 |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|         |                                                                                                                                                                                                                             | 10,763,865 (IPR2026-00384);<br>11,018,678 (IPR2026-00385);<br>10,771,069 (IPR2026-00386); and<br>11,329,655 (IPR2026-00387)—in<br>the same patent family as the '587<br>patent.                                            |
| 1       | <b>Giordano</b> , the primary reference for Grounds <b>1, and 3–5</b> , teaches aligning clock signals for serialization/deserialization (“SER/DES”) processes with a deterministic, fixed phase difference. Ex. 1005, 197. | <b>Giordano</b> , the primary reference for Grounds <b>1 and 3–9</b> , teaches aligning clock signals for serialization/deserialization (“SER/DES”) processes with a deterministic, fixed phase difference. Ex. 1005, 197. |
| 1       | <b>Tetzlaff and Lee</b> , both Xilinx patents, <b>discloses</b> these phase alignment specifics.                                                                                                                            | <b>Tetzlaff and Lee</b> , both Xilinx patents, <b>disclose</b> these phase alignment specifics.                                                                                                                            |
| 8       | Virtex-UG explains that GTP transceivers <b>are</b> include dual-transceiver tiles, allowing two transceivers (one receiver and one transmitter) to share a single PLL, precisely how Giordano describes the Virtex-5 FPGA. | Virtex-UG explains that GTP transceivers include dual-transceiver tiles, allowing two transceivers (one receiver and one transmitter) to share a single PLL, precisely how Giordano describes the Virtex-5 FPGA.           |
| 16      | Virtex-UG, by incorporation, <b>become</b> part of the disclosures of Giordano.                                                                                                                                             | Virtex-UG, by incorporation, <b>becomes</b> part of the disclosures of Giordano.                                                                                                                                           |
| 20      | Ex. 1005, 195–196, <b>5</b> ; Ex. 1003, ¶147.                                                                                                                                                                               | Ex. 1005, 195–196; Ex. 1003, ¶147.                                                                                                                                                                                         |
| 33      | Since the DLL phase detector “controls” the DLL delay line, interim components and signals for such control, including the claimed “phase controller,” <b>is</b>                                                            | Since the DLL phase detector “controls” the DLL delay line, interim components and signals for such control, including the claimed “phase controller,” <b>are</b>                                                          |

| Page(s)                        | Current                                                                                                                                                                  | Correction                                                                                                                                                                          |
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|                                | necessarily disclosed by Tetzlaff's DLL.                                                                                                                                 | necessarily disclosed by Tetzlaff's DLL.                                                                                                                                            |
| 34                             | As discussed in [8.d], Tetzlaff's DLL <b>disclose</b> the "phase controller."                                                                                            | As discussed in [8.d], Tetzlaff's DLL <b>discloses</b> the "phase controller."                                                                                                      |
| 36                             | Since the DLL phase detector "controls" the DLL delay line, interim components and signals for such control <b>is</b> necessarily disclosed by Tetzlaff's DLL.           | Since the DLL phase detector "controls" the DLL delay line, interim components and signals for such control <b>are</b> necessarily disclosed by Tetzlaff's DLL.                     |
| 39                             | Giordano discloses using 8b/10b encoding, where the SIPO deserializes incoming stream into 10-bit parallel words, which are then outputted as 8-bit parallel data words. | Giordano discloses using 8b/10b encoding, where the SIPO deserializes <b>the</b> incoming stream into 10-bit parallel words, which are then outputted as 8-bit parallel data words. |
| 40, 56                         | In addition, Tetzlaff discloses that "PLL acts to maintain a selectable phase offset between the <b>synthesize</b> clock and the reference clock."                       | In addition, Tetzlaff discloses that "PLL acts to maintain a selectable phase offset between the <b>synthesized</b> clock and the reference clock."                                 |
| 42, 58, 59, 70, 71, 72, 73, 74 | <b>Prior Art</b> Overview                                                                                                                                                | Overview                                                                                                                                                                            |
| 44, 58                         | Raymond <b>emphasized</b> the importance of minimizing latency in communication devices, particularly for financial trading.                                             | Raymond <b>emphasizes</b> the importance of minimizing latency in communication devices, particularly for financial trading.                                                        |
| 68                             | As discussed in [8.b] and [8.e], Lee's Digital Delay Line 208 discloses the "adjustable oscillator," its output the "second clock signal," and Synthesizer               | As discussed in [8.b] and [8.e], Lee's Digital Delay Line 208 discloses the "adjustable oscillator," its output <b>discloses</b> the "second clock signal," and                     |

| Page(s) | Current                                                                                                                                                                                                                                             | Correction                                                                                                                                                                                                                                                                  |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|         | Control Block 214 output discloses “interim adjustment information.”<br><br>Lee discloses Digital Delay Line 208 can modify the frequency and phase of the output signal OscClk based on the control signal from the Synthesizer Control Block 214. | Synthesizer Control Block 214 output discloses “interim adjustment information.”<br><br>Lee discloses <b>that</b> Digital Delay Line 208 can modify the frequency and phase of the output signal OscClk based on the control signal from the Synthesizer Control Block 214. |
| 70, 72  | Motivation to combine Giordano and Lee is detailed in Ground 4. Section VI.D.1 ( <b>Ground 4 Prior Art</b> Overview).                                                                                                                               | Motivation to combine Giordano and Lee is detailed in Ground 4. Section VI.D.1 ( <b>Ground 4, Overview</b> ).                                                                                                                                                               |
| 70      | A POSITA would have been motivated to look to Raymond to combine with Giordano and Lee, for the same reasons to combine Raymond with Giordano and Tetzlaff. Section VI.A.1 ( <b>Ground 1 Prior Art</b> Overview).                                   | A POSITA would have been motivated to look to Raymond to combine with Giordano and Lee, for the same reasons to combine Raymond with Giordano and Tetzlaff. Section VI.C ( <b>Ground 3, Overview</b> ).                                                                     |
| 73      | A POSITA would have been motivated to look to Virtex-UG to combine with Giordano and Lee, for the same reasons to combine Virtex-UG with Giordano and Tetzlaff. Section VI.F.1 ( <b>Ground 6 Prior Art</b> Overview).                               | A POSITA would have been motivated to look to Virtex-UG to combine with Giordano and Lee, for the same reasons to combine Virtex-UG with Giordano and Tetzlaff. Section VI.F.1 ( <b>Ground 6, Overview</b> ).                                                               |
| 73      | Motivations to combine Giordano, Tetzlaff, and Virtex-UG are detailed in Ground 6. Section VI.F.1 ( <b>Ground 6 Prior Art</b> Overview).                                                                                                            | Motivations to combine Giordano, Tetzlaff, and Virtex-UG are detailed in Ground 6. Section VI.F.1 ( <b>Ground 6, Overview</b> ).                                                                                                                                            |
| 74      | Motivations to combine Giordano, Lee, and Virtex-UG are detailed                                                                                                                                                                                    | Motivations to combine Giordano, Lee, and Virtex-UG are detailed                                                                                                                                                                                                            |

| Page(s) | Current                                                                                                                                                                                                                     | Correction                                                                                                                                                                                                          |
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|         | in Ground 7. Section VI.G.1<br>( <b>Ground 7 Prior Art</b> Overview).                                                                                                                                                       | in Ground 7. Section VI.G.1<br>( <b>Ground 7</b> , Overview).                                                                                                                                                       |
| 74      | A POSITA would have been motivated to look to Raymond to combine with Giordano, Lee, and Virtex-UG, for the same reasons to combine Raymond with Giordano and Lee. Section VI.E.1<br>( <b>Ground 5 Prior Art</b> Overview). | A POSITA would have been motivated to look to Raymond to combine with Giordano, Lee, and Virtex-UG, for the same reasons to combine Raymond with Giordano and Lee. Section VI.E.1<br>( <b>Ground 5</b> , Overview). |

In addition, Petitioners moves the Board for leave to file the corrected Declaration of Dr. Benjamin Carrion-Schaefer to make the corrections noted below, in red:

| Page(s) | Current                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Correction                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NA      | -                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | <b>Addition of Dr. Benjamin Carrion-Schaefer's CV as Appendix A</b>                                                                                                                                                                                                                                                                                                                                                                                                    |
| 40      | I was asked to provide my opinions regarding whether the Challenged Claims of the '587 patent would have been obvious to one of ordinary skill in the art at the time of the claimed invention for claims 1 and 4–12 by Giordano in view of Tetzlaff (Ground 1), claims 1–12 by Raymond in view of Tetzlaff (Ground 2), <b>claims 2–3</b> by Giordano in view of Tetzlaff further in view of Raymond (Ground 3), claims 1 and 4–12 by Giordano in view of Lee (Ground | I was asked to provide my opinions regarding whether the Challenged Claims of the '587 patent would have been obvious to one of ordinary skill in the art at the time of the claimed invention for claims 1 and 4–12 by Giordano in view of Tetzlaff (Ground 1), claims 1–12 by Raymond in view of Tetzlaff (Ground 2), <b>claims 1–12</b> by Giordano in view of Tetzlaff further in view of Raymond (Ground 3), claims 1 and 4–12 by Giordano in view of Lee (Ground |

| Page(s) | Current                                                                                                                                                                                                                                                                                                                                                                                      | Correction                                                                                                                                                                                                                                                                                                                                                                                                                        |
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|         | 4), and claims 2–3 by Giordano in view of Lee further in view of Raymond (Ground 5).                                                                                                                                                                                                                                                                                                         | 4), claims 1–12 by Giordano in view of Lee further in view of Raymond (Ground 5), claims 1 and 4–12 by Giordano in view of Tetzlaff further in view of Virtex-UG (Ground 6), claims 1 and 4–12 by Giordano in view of Lee further in view of Virtex-UG (Ground 7), claims 1–12 by Giordano in view of Tetzlaff, Virtex-UG, and Raymond (Ground 8), and claims 1–12 by Giordano in view of Lee, Virtex-UG, and Raymond (Ground 9). |
| 41      | I understand words or terms should be given their ordinary and accepted meaning unless it appears that the inventor <b>wase</b> using them to mean something else or something more specific.                                                                                                                                                                                                | I understand words or terms should be given their ordinary and accepted meaning unless it appears that the inventor <b>was</b> using them to mean something else or something more specific.                                                                                                                                                                                                                                      |
| 49      | Virtex-UG was neither cited nor considered during prosecution of the ' <b>865</b> patent.                                                                                                                                                                                                                                                                                                    | Virtex-UG was neither cited nor considered during prosecution of the ' <b>587</b> patent.                                                                                                                                                                                                                                                                                                                                         |
| 55      | The fundamental building blocks at issue in this proceeding—serializers/deserializers (SERDES), phase-locked loops (PLLs), delay-locked loops (DLLs), clock and data recovery (CDR) circuits, and phase alignment mechanisms—were all well-understood, standardized components that had been available in commercial FPGA devices for many years prior to the priority date. Commercial user | The fundamental building blocks at issue in this proceeding—serializers/deserializers (SERDES), phase-locked loops (PLLs), delay-locked loops (DLLs), clock and data recovery (CDR) circuits, and phase alignment mechanisms—were all well-understood, standardized components that had been available in commercial FPGA devices for many years prior to the priority date. Commercial                                           |

| Page(s) | Current                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Correction                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|         | guides, such as Virtex-5 RocketIO GTP Transceiver User Guide (“Virtex-UG”), <b>documents</b> many of these features.                                                                                                                                                                                                                                                                                                                                                                                                                                        | user guides, such as Virtex-5 RocketIO GTP Transceiver User Guide (“Virtex-UG”), <b>document</b> many of these features.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 57–58   | Lee’s implementation achieves “PLL-like operation while using components that are all digital.” Ex. 1008, 4:42–43. Lee’s circuit was specifically designed for implementation in types of <b>FPGAs</b> like Xilinx FPGAs. Ex. 1008, 7:18–35.                                                                                                                                                                                                                                                                                                                | Lee’s implementation achieves “PLL-like operation while using components that are all digital.” Ex. 1008, 4:42–43. Lee’s circuit was specifically designed for implementation in types of <b>FPGAs</b> like Xilinx FPGAs. Ex. 1008, 7:18–35.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 64      | I have analyzed all Challenged Claims of the ’587 patent, and it is my opinion that claims 1 and 4–12 are rendered obvious by Giordano in view of Tetzlaff (Ground 1), claims 1–12 are rendered obvious by Raymond in view of Tetzlaff (Ground 2), <b>claims 2–3</b> are rendered obvious by Giordano in view of Tetzlaff further in view of Raymond (Ground 3), claims 1 and 4–12 are rendered obvious by Giordano in view of Lee (Ground 4), and <b>claims 2–3</b> are rendered obvious by Giordano in view of Lee further in view of Raymond (Ground 5). | I have analyzed all Challenged Claims of the ’587 patent, and it is my opinion that claims 1 and 4–12 are rendered obvious by Giordano in view of Tetzlaff (Ground 1), claims 1–12 are rendered obvious by Raymond in view of Tetzlaff (Ground 2), <b>claims 1–12</b> are rendered obvious by Giordano in view of Tetzlaff further in view of Raymond (Ground 3), claims 1 and 4–12 are rendered obvious by Giordano in view of Lee (Ground 4), <b>claims 1–12</b> are rendered obvious by Giordano in view of Lee further in view of Raymond (Ground 5), <b>claims 1 and 4–12 are rendered obvious by Giordano in view of Tetzlaff further in view of Virtex-UG (Ground 6), claims 1 and 4–12 are rendered obvious by Giordano in view of Lee further in view of Virtex-UG (Ground 7), claims 1–12 are rendered obvious by Giordano in view of Tetzlaff,</b> |

| Page(s)  | Current                                                                                                                                                                                            | Correction                                                                                                                                                                                          |
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|          |                                                                                                                                                                                                    | Virtex-UG, and Raymond (Ground 8), and claims 1–12 are rendered obvious by Giordano in view of Lee, Virtex-UG, and Raymond (Ground 9).                                                              |
| 73       | Virtex-UG, by incorporation, <b>become</b> part of the disclosures of Giordano.                                                                                                                    | Virtex-UG, by incorporation, <b>becomes</b> part of the disclosures of Giordano.                                                                                                                    |
| 97       | As I discussed in element [8.b above], the synthesized clock 314 discloses the “second clock signal.” Tetzlaff’s DLL/PLL discloses this limitation [8.i].                                          | As I discussed in element [8.b] above, the synthesized clock 314 discloses the “second clock signal.” Tetzlaff’s DLL/PLL discloses this limitation [8.i].                                           |
| 101, 121 | In addition, Tetzlaff discloses that “PLL acts to maintain a selectable phase offset between the <b>synthesize</b> clock and the reference clock.”                                                 | In addition, Tetzlaff discloses that “PLL acts to maintain a selectable phase offset between the <b>synthesized</b> clock and the reference clock.”                                                 |
| 103      | The annotated image below, Figure 2 of Raymond modified in light of the teachings of Tetzlaff, depicts the modifications to Raymond and insertion of <b>Tetzlaf</b> according to this combination: | The annotated image below, Figure 2 of Raymond modified in light of the teachings of Tetzlaff, depicts the modifications to Raymond and insertion of <b>Tetzlaff</b> according to this combination: |
| 109      | Raymond’s transceiver 16 and Input SERDES 208 together disclose the claimed “deserializer,” both which receive incoming a physical layer serial signal 12.                                         | Raymond’s transceiver 16 and Input SERDES 208 together disclose the claimed “deserializer,” both <b>of</b> which receive incoming a physical layer serial signal 12.                                |
| 110      | [1.c] generating, by the deserializer, a receiver side clock signal;                                                                                                                               | [1.c] <b>(c)</b> generating, by the deserializer, a receiver side clock signal;                                                                                                                     |

| Page(s)     | Current                                                                                                                                                                                               | Correction                                                                                                                                                                                                       |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 110         | [1.d] converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;                                                                                  | [1.d] <b>(d)</b> converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;                                                                                  |
| 111         | [1.e] transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;                                              | [1.e] <b>(e)</b> transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;                                              |
| 111,<br>128 | [1.f]: transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;                                                          | [1.f]: <b>(f)</b> transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;                                                          |
| 112,<br>129 | [1.g]: generating, using the phase lock loop, a transmitter side clock signal;                                                                                                                        | [1.g]: <b>(g)</b> generating, using the phase lock loop, a transmitter side clock signal;                                                                                                                        |
| 113         | [1.h]: performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams; | [1.h]: <b>(h)</b> performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams; |
| 113         | [1.i]: converting the second plurality of parallel data streams, by a serializer, into a second serial data stream; and                                                                               | [1.i]: <b>(i)</b> converting the second plurality of parallel data streams, by a serializer, into a second serial data stream; and                                                                               |
| 114         | [1.j]: transmitting, from the field programmable gate array system, the second serial data stream,                                                                                                    | [1.j]: <b>(j)</b> transmitting, from the field programmable gate array system, the second serial data stream,                                                                                                    |
| 119         | Raymond in view of Tetzlaff renders obvious this claim. As I discussed above for claim [1],                                                                                                           | Raymond in view of Tetzlaff renders obvious this claim. As I discussed above for claim [1],                                                                                                                      |

| Page(s) | Current                                                                                                                                                                                                                                             | Correction                                                                                                                                                                                                                                          |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|         | Raymond and Tetzlaff renders obvious claim [1] ( <b>Section IX.A.2.a</b> ).                                                                                                                                                                         | Raymond and Tetzlaff renders obvious claim [1] ( <b>Section IX.B.2.a</b> ).                                                                                                                                                                         |
| 127     | As I described above in <b>Sections IX.A.2.a</b> ., Giordano discloses limitations [1.pre] through [1.e].                                                                                                                                           | As I described above in <b>Section IX.A.2.a</b> ., Giordano discloses limitations [1.pre] through [1.e].                                                                                                                                            |
| 136     | A POSITA would have been motivated to look to Raymond to combine with Giordano and Lee, for the same reasons to combine Raymond with Giordano and Tetzlaff, as I discussed in above in <b>Section IX.A.1</b> ( <b>Ground 1</b> Prior Art Overview). | A POSITA would have been motivated to look to Raymond to combine with Giordano and Lee, for the same reasons to combine Raymond with Giordano and Tetzlaff, as I discussed in above in <b>Section IX.C.1</b> ( <b>Ground 3</b> Prior Art Overview). |
| 136     | As I discussed above in Sections <b>IX.D.2.b–IX.D.2.d</b> (Ground 4, cls. 4–12), Giordano in view of Lee renders obvious claims [1], [4]–[12].                                                                                                      | As I discussed above in Sections <b>IX.D.2.a–IX.D.2.d</b> (Ground 4, cls. <b>1</b> , 4–12), Giordano in view of Lee renders obvious claims [1], [4]–[12].                                                                                           |

The errors are based on incorrect cross-referencing, incomplete or incorrect supporting citations, and minor typographical and clerical errors. The proposed changes correct the errors for clarity.

### III. ARGUMENT

Under 37 C.F.R. § 104(c), “[a] motion may be filed that seeks to correct a clerical or typographical mistake in the petition.” In deciding such motion, the Board may consider the nature of the error; the Petitioner’s diligence in reporting such error; prejudice to the Patent Owner, if any, by allowing the proposed corrections;

and whether the proposed corrections have any impact on the proceeding. *Samsung Electronics Co., Ltd. et al v. Staton Techiya, LLC*, IPR2022-00243, Paper 10 at 2 (P.T.A.B. Feb. 2, 2022); *id.*, Paper 9 at 1–2 (“When ruling on a § 42.104(c) motion, the Board considers various nonexclusive factors such as: ‘(1) the nature of the error, and whether the party requesting relief provides adequate explanation for how the error occurred, including how the error was discovered; (2) the length of time elapsed between learning of the error and bringing the error to [the Board’s] attention; (3) prejudice to the other party, if any, by allowing the proposed corrections; and (4) whether the proposed corrections have any impact on the proceeding.’”) (citing *Ivantis, Inc. v. Glaukos Corp.*, IPR2018-01180, Paper 14 at 9 (P.T.A.B. Dec. 6, 2018)).

Here, Petitioners seek to correct inadvertent errors that do not have material impact to the substantive analysis of the Petition. Correcting the Petition and accompanying expert Declaration do not introduce any new analysis.

**A. The Errors Are Readily Apparent**

Each error is readily apparent from the petition and declaration. For example, the Petition introduces Giordano as the primary reference for Grounds 1, and 3–5, yet other than this single instance, the Petition consistently identifies Giordano as the primary reference for Grounds 1, and 3–9. This includes identification of

challenge and relief requested, which expressly states Giordano as the primary reference for Grounds 1, and 3–9.

Similarly, Dr. Benjamin Carrion-Schaefer’s Declaration includes introductory statements that inadvertently misstated the claims covered by Grounds 3 and 5, and further omitted that his opinions include that for Grounds 6–9. But the actual analysis and related discussions detail his opinions as to the broader scope of claims for Grounds 3 and 5, and further his opinions for Grounds 6–9. As Dr. Carrion-Schaefer’s technical opinions as to these Grounds are already present in his Original Declaration, the correction Petitioners seek is nothing more than addressing clerical errors.

In addition, Petitioners seek to add information inadvertently omitted at the time of filing the Petition. This includes identifying four other *inter partes* review proceedings directed to patents in the same patent family as the ’587 patent, and inclusion of Dr. Benjamin Carrion-Schaefer’s CV. These errors, again, are readily apparent omissions.

Petitioners further identify various misspellings and grammatic errors, which do not affect the substance of the Petition or Declaration, and are apparent from reading of the Petition.

**B. Petitioners Acted Diligently To Correct The Errors**

Petitioners learned of these errors shortly after filing, and reached out to the Board and Patent Owner within a week from filing of the Petition. After obtaining Patent Owner's consent, Petitioners promptly contacted the Board and filed this motion within a week of obtaining the Board's permission to do so, roughly three weeks since filing this Petition.

**C. Correcting The Errors Will Not Prejudice Patent Owner**

Correcting the errors does not add any new analysis and thus will not change the Patent Owner's substantive analysis. As the Patent Owner agrees, the proposed corrections are clerical and grammatical in nature. There is no material change to the substance of the Petition. As such, the correction of the errors does not prejudice Patent Owner's ability to submit a preliminary response, should it choose to do so. Patent Owner indicated that it does not oppose Petitioners' correction of these errors.

**D. Correction Will Not Have Negative Impact**

As discussed above, correcting the errors does not add any new analysis, and will not negatively impact the Board's analysis. Thus the corrections will not materially change the Board's analysis. Rather, the proposed corrections will provide clarity and address clerical and grammatical issues that further benefit the Board's assessment of the Petition.

#### IV. CONCLUSION

For the reasons discussed above, Petitioners respectfully request that the Board grant leave and allow Petitioners to submit a corrected Petition and a corrected Declaration.

DATED: June 22, 2026

Respectfully Submitted,

By: / Brian M. Buroker /

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*Attorneys for Petitioners OPTIVER US LLC  
and OPTIVER TRADING US LLC*

**CERTIFICATE OF SERVICE**

The undersigned certifies service pursuant to 37 C.F.R. §§42.6(e) and 42.105(b) on the Patent Owner electronically on the Patent Owner at the following email addresses:

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