UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

OPTIVER US LLC and OPTIVER TRADING US LLC,
Petitioners

v.

HFT SOLUTIONS, LLC,
Patent Owner.

Case No. IPR2026-00383
U.S. Patent No. 12,107,587

Corrected Petition for *Inter Partes* Review of U.S. Patent No. 12,107,587

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TABLE OF CONTENTS

TABLE OF CONTENTS i
TABLE OF EXHIBITS iv
TABLE OF ABBREVIATIONS v
MANDATORY NOTICES vi
A. Real Parties-in-Interest: 37 C.F.R. §42.8(b)(1) vi
B. Related Matters Under: 37 C.F.R. §42.8(b)(2) vi
1. Current Litigation vi
2. Administrative Proceedings vi
C. Lead and Back-Up Counsel: 37 C.F.R. §42.8(b)(3) vi
D. Service of Information: 37 C.F.R. §42.8(b)(4) viii
I. INTRODUCTION 1
II. REQUIREMENTS OF IPR 2
A. Standing: 37 C.F.R. §42.104(a) 2
B. Identification of Challenge and Relief Requested: 37 C.F.R. §42.104(b) 2
1. R. Giordano and A. Aloisio, *Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs*, 58-1 IEEE Transactions on Nuclear Science 194 (2011) ("Giordano") (Ex. 1005) 4
2. Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 ("Virtex-UG") (Ex. 1009) 4
3. U.S. Pat. No. 7,499,513 ("Tetzlaff") (Ex. 1006) 4
4. U.S. Pat. No. 10,447,463 ("Raymond") (Ex. 1007) 4
5. U.S. Pat. No. 8,788,553 ("Lee") (Ex. 1008) 5
C. Claim Construction: 37 C.F.R. §42.104(b)(3) 5
D. Challenge: 37 C.F.R. §42.104(b)(4) 5
E. Supporting Evidence: 37 C.F.R. §42.104(b)(5) 5
F. Payment of Fees: 37 C.F.R. §§42.103, 42.15(a) 6

III. PERSON OF ORDINARY SKILL IN THE ART ("POSITA") 6
IV. STATE OF THE ART 6
1. Giordano 7
2. Virtex-UG 8
3. Tetzlaff 8
4. Raymond 8
5. Lee 9
V. OVERVIEW OF THE '587 PATENT 9
A. Summary of the File History of the '587 patent 9
VI. GROUNDS FOR UNPATENTABILITY 10
A. Ground 1: Claims 1, 4–12 Are Rendered Obvious by Giordano in View of Tetzlaff 10
1. Overview 10
2. Analysis 16
B. Ground 2: Claims 1–12 Are Rendered Obvious by Raymond in View of Tetzlaff 41
1. Overview 41
2. Analysis 44
C. Ground 3: Claims 1–12 Are Rendered Obvious by Giordano in View of Tetzlaff further in View of Raymond 57
1. Overview 57
2. Analysis 58
D. Ground 4: Claims 1, 4–12 Are Rendered Obvious by Giordano in View of Lee 58
1. Overview 58
2. Analysis 60
E. Ground 5: Claims 1–12 Are Rendered Obvious by Giordano in View of Lee further in View of Raymond 69
1. Overview 69
2. Analysis 69

F. Ground 6: Claims 1, 4–12 Are Rendered Obvious by Giordano in View of Tetzlaff further in View of Virtex-UG 70

1. Overview 70

2. Analysis 71

G. Ground 7: Claims 1, 4–12 Are Rendered Obvious by Giordano in View of Lee further in View of Virtex-UG 71

1. Overview 71

2. Analysis 72

H. Ground 8: Claims 1–12 Are Rendered Obvious by Giordano in View of Tetzlaff, Virtex-UG, and Raymond 72

1. Overview 72

2. Analysis 73

I. Ground 9: Claims 1–12 Are Rendered Obvious by Giordano in View of Lee, Virtex-UG, and Raymond 73

1. Overview 73

2. Analysis 74

VII. CONCLUSION 74

APPENDIX: CHALLENGED CLAIM LISTING 77

TABLE OF EXHIBITS

Exhibit No.	Document
1001	U.S. Patent No. 12,107,587 ("the '587 patent")
1002	File History for U.S. Patent No. 12,107,587
1003	Declaration of Benjamin Carrion Schaefer, Ph.D.
1004	Declaration of Carrie Gardner
1005	R. Giordano and A. Aloisio, *Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs*, 58-1 IEEE Transactions on Nuclear Science 194 (2011) [Giordano]
1006	U.S. Pat. No. 7,499,513 [Tetzlaff]
1007	U.S. Pat. No. 10,447,463 [Raymond]
1008	U.S. Pat. No. 8,788,553 [Lee]
1009	Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 [Virtex-UG]
1010	*(intentionally omitted)*
1011	Declaration of Gordon MacPherson
1012	Curriculum Vitae of Benjamin Carrion Schaefer, Ph.D.
1013	Redline of Corrected Petition for Inter Partes Review of U.S. Patent No. 12, 107,587
1014	Redline of Corrected Declaration of Benjamin Carrion Schaefer, Ph.D.

TABLE OF ABBREVIATIONS

Abbreviation	Term
’587 patent	U.S. Pat. No. 12,107,587
AIA	America Invents Act
CDC	Clock Domain Crossing
CDR	Clock and Data Recovery
Challenged Claims	Claims 1–12 of U.S. Pat. No. 12,107,587
DLL	Delay Locked Loop
Ex.	Exhibit
Fig.	Figure
FPGA	Field Programmable Gate Array
Giordano	R. Giordano and A. Aloisio, *Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs*, 58-1 IEEE Transactions on Nuclear Science 194 (2011)
IPR	*inter partes* review
Lee	U.S. Pat. No. 8,788,553
MAC	Media Access Controller
Patent Owner	HFT Solutions, LLC
PCS	Physical Coding Sublayer
Petitioners	Optiver US LLC and Optiver Trading US LLC
PLL	Phase Locked Loop
PMA	Physical Medium Attachment
Raymond	U.S. Pat. No. 10,447,463
Tetzlaff	U.S. Pat. No. 7,499,513
VCO	Voltage Controlled Oscillator
Virtex-UG	Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009
VLSI	Very Large Scale Integration

MANDATORY NOTICES

A. Real Parties-in-Interest: 37 C.F.R. §42.8(b)(1)

Optiver US LLC and Optiver Trading US LLC are the real parties-in-interest. Optiver Services US LLC is a corporate affiliate and services entity supporting Optiver US LLC and Optiver Trading US LLC. The ultimate parent company of all three entities is Optiver Holding BV.

B. Related Matters Under: 37 C.F.R. §42.8(b)(2)

1. Current Litigation

The ’587 patent is presently not subject to any litigation. Petitioners are not aware of any litigation involving the ’587 patent.

2. Administrative Proceedings

There are no other administrative proceedings at issue. Petitioners have filed or intend to file petitions for *inter partes* review regarding four additional patents—U.S. Pat. Nos. 10,763,865 (IPR2026-00384); 11,018,678 (IPR2026-00385); 10,771,069 (IPR2026-00386); and 11,329,655 (IPR2026-00387)—in the same patent family as the ’587 patent.

C. Lead and Back-Up Counsel: 37 C.F.R. §42.8(b)(3)

Petitioners provide the following designation of counsel:

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Petitioners respectfully request authorization to file motions for Brian Rosenthal to appear before the USPTO *pro hac vice*. Mr. Rosenthal is an experienced attorney and is currently serving as lead counsel for Petitioners in an action between Petitioners and Patent Owner.[1] He is familiar with the subject matter at issue in this proceeding. Petitioners intend to file a motion to appear *pro hac vice* under 37 C.F.R. §42.10. Pursuant to 37 C.F.R. §42.10(b), powers of attorney accompany this petition.

[1] Petitioners are currently defending Patent Owner's assertion of U.S. Pat. Nos. 10,931,286; 11,128,305; 11,575,381 in *HFT Solutions, LLC v. Optiver US LLC and Optiver Trading US LLC*, 7:25-cv-415 (W.D. Tex. filed Sept. 8, 2025). These three patents list the same sole inventor (Nima Badizadegan) as the '587 patent but belong to a separate patent family.

D. Service of Information: 37 C.F.R. §42.8(b)(4)

Service of any documents via hand delivery may be made at the mailing address of lead and backup counsel. Petitioners also consent to electronic service, and service via electronic mail may be made at the email addresses provided for the lead and backup counsel.

I. INTRODUCTION

Pursuant to 35 U.S.C. §311, Petitioners seek *inter partes* review of U.S. Pat. No. 12,107,587 (Ex. 1001) and cancellation of claims 1–12 as unpatentable under 35 U.S.C. §103.

The Challenged Claims are directed to an FPGA system that receives and transmits data using synchronized receiver and transmitter clock signals. Ex. 1001, 1:30–34. The alleged invention of the '587 patent is in using an "internal phase-locked loop" for "***phase matching*** receiver side and transmitter side clocks of a FPGA without introducing unnecessary delay in processing." *Id.*, 2:23–26.[2]

Yet the prior art taught these concepts before the '587 patent. **Giordano**, the primary reference for Grounds 1 and 3–9, teaches aligning clock signals for serialization/deserialization ("SER/DES") processes with a deterministic, fixed phase difference. Ex. 1005, 197. Giordano plainly discloses performing everything in claims 1, 4–12 using Xilinx FPGA systems, but lacks certain details in how the phase alignment is achieved. **Tetzlaff** and **Lee**, both Xilinx patents, disclose these phase alignment specifics. Given the programmable nature of FPGAs (which allows users to modify hardware as needed) and Giordano's guidance to seek further specifics of phase alignment, a POSITA would have found it obvious to incorporate

[2] Unless noted otherwise, emphasis added.

the teachings of Tetzlaff or Lee into Giordano's FPGA system. Ex. 1005, 198; Ex. 1006, 9:29–51; 6:27–47, cls. 1, 5; Ex. 1008, 2:35–51, Fig. 2.

Claims 2 and 3 of the '587 patent add only the application of these well-known FPGA systems to financial trading. **Raymond** expressly teaches using FPGA systems and phase matching (as in Giordano, Tetzlaff, and Lee) in high-frequency trading applications. Ex. 1007, 1:18–38. Applying the known FPGA phase matching teachings disclosed in Giordano, Tetzlaff, and Lee to financial-trading applications as suggested by Raymond would have been straightforward and obvious. *See also* Ex. 1001, 1:41–43 ("FPGAs are used in the financial industry").

Because this Petition demonstrates a reasonable likelihood that Petitioners will prevail on at least one challenged claim based on prior art not considered during prosecution, the Board should institute *inter partes* review ("IPR") and cancel claims 1–12 under 35 U.S.C. §103.

II. REQUIREMENTS OF IPR

A. Standing: 37 C.F.R. §42.104(a)

Petitioners certify that the '587 patent is eligible for IPR and that Petitioners are not barred or estopped from requesting an IPR of the Challenged Claims.

B. Identification of Challenge and Relief Requested: 37 C.F.R. §42.104(b)

Petitioners request IPR of claims 1–12 of the '587 patent under AIA 35 U.S.C. §103.

The ’587 patent issued from an application filed April 18, 2022, and claims priority to a provisional application filed February 21, 2019. For purposes of this Petition only, Petitioners do not dispute that the Challenged Claims are entitled to an effective filing date of February 21, 2019.

Petitioners request cancellation of claims 1–12 based on:

Ground	Claims	Basis for Rejection
1	1, 4–12	Obviousness over Giordano in view of Tetzlaff
2	1–12	Obviousness over Raymond in view of Tetzlaff
3	1–12	Obviousness over Giordano in view of Tetzlaff further in view of Raymond
4	1, 4–12	Obviousness over Giordano in view of Lee
5	1–12	Obviousness over Giordano in view of Lee further in view of Raymond
6	1, 4–12	Obviousness over Giordano in view of Tetzlaff further in view of Virtex-UG[3]
7	1, 4–12	Obviousness over Giordano in view of Lee further in view of Virtex-UG
8	1–12	Obviousness over Giordano in view of Tetzlaff, Virtex-UG, and Raymond
9	1–12	Obviousness over Giordano in view of Lee, Virtex-UG, and Raymond

[3] Giordano inherently discloses the features of Virtex-UG, and further incorporates Virtex-UG by reference. Ex. 1003, ¶¶78, 120. If necessary, a POSITA would have been motivated to combine Virtex-UG to all grounds based on Giordano.

1. R. Giordano and A. Aloisio, *Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs*, 58-1 IEEE Transactions on Nuclear Science 194 (2011) ("Giordano") (Ex. 1005)

Giordano was published in IEEE Transactions on Nuclear Science on January 28, 2011. Ex. 1004, ¶¶21–26; *id*., ¶27, 33–34, 37 (citing Ex. 1011). Giordano qualifies as prior art under AIA 35 U.S.C. §102(a)(1). Giordano was not considered during prosecution of the '587 patent.

2. Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 ("Virtex-UG") (Ex. 1009)

Virtex-UG was published on December 3, 2009. Ex. 1004, ¶¶41–47. Virtex-UG qualifies as prior art under AIA 35 U.S.C. § 102(a)(1). Virtex-UG was not considered during prosecution of the '587 patent.

3. U.S. Pat. No. 7,499,513 ("Tetzlaff") (Ex. 1006)

Tetzlaff, titled "Method and Apparatus for Providing Frequency Synthesis and Phase Alignment in an Integrated Circuit," was filed February 2, 2005, and granted March 3, 2009. Tetzlaff qualifies as prior art under AIA 35 U.S.C. §102(a)(1) and §102(a)(2). Tetzlaff was not considered during prosecution of the '587 patent.

4. U.S. Pat. No. 10,447,463 ("Raymond") (Ex. 1007)

Raymond, titled "Device and Method for Ultra-low Latency Communication," claims priority to a provisional application filed July 13, 2017, and an application filed July 13, 2018. Raymond qualifies as prior art under AIA 35

U.S.C. §102(a)(2). Raymond was not considered during prosecution of the '587 patent.

5. U.S. Pat. No. 8,788,553 ("Lee") (Ex. 1008)

Lee, titled "Method and Circuit for Providing Digital Frequency Synthesis," was filed January 28, 2009, and granted July 22, 2014. Lee qualifies as prior art under AIA 35 U.S.C. §102(a)(1) and §102(a)(2). Lee was not considered during prosecution of the '587 patent.

C. Claim Construction: 37 C.F.R. §42.104(b)(3)

Petitioners submit that no construction of any claim term is necessary for the Board to resolve, and the Challenged Claims would have been obvious under any reasonable construction.

D. Challenge: 37 C.F.R. §42.104(b)(4)

Explanation of how the Challenged Claims are unpatentable under the grounds identified above, including where each claim element is found in the prior art, is provided below.

E. Supporting Evidence: 37 C.F.R. §42.104(b)(5)

The supporting exhibits, their relevance to the Challenged Claims, and the specific portions supporting the asserted grounds are identified below. The Petition's technical analysis and grounds are further supported by Declaration of Dr. Benjamin Carrion Schaefer (Ex. 1003). The public availability of the cited prior art

is further supported by Declaration of Carrie Gardner (Ex. 1004), which further includes cites to Declaration of Gordon MacPherson (Ex. 1011).

A List of Exhibits is included pursuant to 37 C.F.R. §42.63(e).

F. Payment of Fees: 37 C.F.R. §§42.103, 42.15(a)

The required fee was submitted. The Office is authorized to charge any fee deficiency, or credit overpayment, to Deposit Account 50-1408, including additional fees related to this Petition.

III. PERSON OF ORDINARY SKILL IN THE ART ("POSITA")

A POSITA, on February 21, 2019, would have a Bachelor's degree in Computer Engineering, Electrical Engineering, or equivalent discipline, and at least three years of academic or industry experience relating to clocking techniques for FPGAs with high-speed transceivers. Educational requirements may be substituted by work experience, and vice versa.

IV. STATE OF THE ART

By February 21, 2019, FPGA-based communication systems were highly developed, and SERDESes, PLLs, DLLs, CDRs, and phase-alignment mechanisms were standard FPGA features. Ex. 1001, 1:41–43; Ex. 1003, ¶88.

Commercial FPGA transceivers implemented integrated serialization and deserialization using parallel-in/serial-out (PISO) and serial-in/parallel-out (SIPO) circuitry. Ex. 1009, 104; Ex. 1003, ¶90. The transceivers interfaced FPGA

programmable logic through user-accessible clock and data interfaces, enabling custom processing of deserialized data. Ex. 1005, 194–95; Ex. 1003, ¶91.

1. Giordano

Giordano presents "a link architecture" using "GTP transceiver" of Xilinx Virtex-5 FPGA. Ex. 1005, 194. Giordano explains that transceivers are implemented as "configurable hard-macros (or 'tiles')," each including a receiver and a transmitter. *Id*. Each receiver and transmitter has a Physical Medium Attachment (PMA) sublayer for serialization (in transmitter PMA) or deserialization (in receiver PMA), and a Physical Coding Sublayer (PCS) for processing data. *Id*.

Giordano also describes an FPGA Fabric with programmable hardware, which can implement user-programmed circuits such as "Comma Detect and Align" circuits and DLLs. *Id*., 197–199. Figure 1 below shows Giordano's architecture:

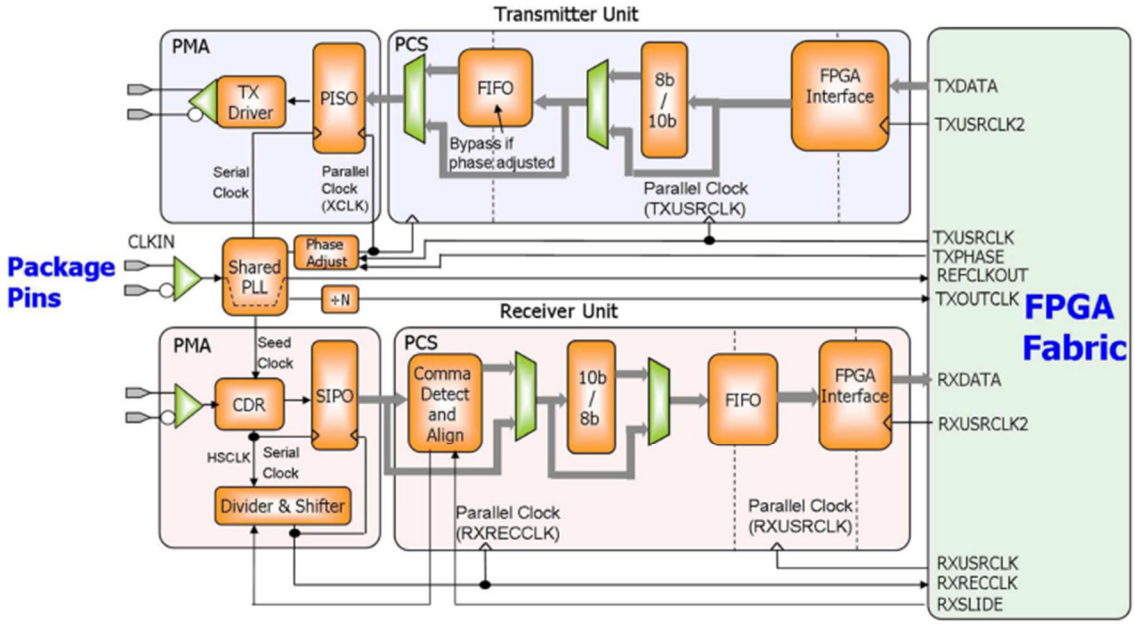


Fig. 1. Simplified block diagram of the GTP transceiver. Half a tile is shown.

2. Virtex-UG

Virtex-UG "shows how to use the RocketIO™ GTP transceivers in Virtex®-5 FPGAs," describing GTP transceivers as configurable transceivers "tightly integrated with the programmable logic resources of the FPGA." Ex. 1009, 17, 23. GTP transceivers support optional features such as 8b/10b encoding, comma alignment, and clock correction, and "fixed latency modes for minimized, deterministic datapath latency." *Id*., 23. Virtex-UG explains that GTP transceivers include dual-transceiver tiles, allowing two transceivers (one receiver and one transmitter) to share a single PLL, precisely how Giordano describes the Virtex-5 FPGA. *Id*., 24; Ex. 1005, 194.

3. Tetzlaff

Tetzlaff (U.S. Pat. No. 7,499,513) explains that FPGAs include arrays of programmable tiles. Ex. 1006, 1:22–26, 1:60–62. Tetzlaff identifies clock skew (*i.e.*, misaligned clock signals) as a problem in synchronous systems. *Id*., 2:9–16. Tetzlaff addresses clock skew by "clock distribution, phase alignment, and frequency synchronization via high speed serial I/O transceivers," using PLLs and DLLs. *Id*., 4:21–26.

4. Raymond

Raymond (U.S. Pat. No. 10,447,463) explains that "[u]ltra-low latency communication is critical" for electronic trading and that trading firms use FPGAs to improve throughput and latency. Ex. 1007, 1:18–24. Raymond discusses

processing incoming financial trading data, exchanged with financial exchanges. *Id*., 4:52–59.

Raymond states that "prefabricated transceivers used to process incoming and outgoing physical layer signals" may be "replaced by low-latency serializer/de-serializer modules" programmed by the FPGA. *Id*., 4:43–47; 9:3–8 ("SerDes module" is "implemented using programmable logic"), 11:65–67.

5. Lee

Lee (U.S. Pat. No. 8,788,553) discloses adjustable PLLs to accommodate different clocks for receivers and transmitters, with capabilities for frequency synthesis and phase shifting. Ex. 1008, 1:12–23. Lee addresses taking advantage of frequency aligned mode and phase aligned mode, separately and together for finer clock management. *Id*., 2:35–55.

V. OVERVIEW OF THE '587 PATENT

A. Summary of the File History of the '587 patent

The '587 patent was filed April 18, 2022. The Examiner rejected original claims 1–12 as obvious over Zhang (U.S. Pat. No. 8,873,606) in view of Cho (U.S. Pat. App. Pub. No. 2018/0027431). Ex. 1002, 154–162.

Applicant amended claim 1 to require "converting the second plurality of parallel data streams, by a serializer, into a second serial data stream," and argued Zhang did not disclose that limitation as Zhang modified the second parallel data

stream into a third parallel data stream before serialization. Ex. 1002, 142–43. Applicant also argued Zhang, by using a FIFO block that is "a clock-domain-crossing circuit that delayed processing of parallel signals," failed to satisfy the claim limitation excluding such circuit. *Id*.

After final rejection, Applicant further amended claims 1 and 9 and continued arguing Zhang failed to disclose the "second plurality of parallel data streams" and "clock domain crossing operations" limitations. *Id*., 76–84.

The Examiner then allowed claims 1–12 as the "second plurality of parallel data streams" should not be altered before conversion into the "second serial data stream," and that Zhang's FIFO buffer performed clock-domain-crossing operations excluded by the claims. *Id*., 14–20.

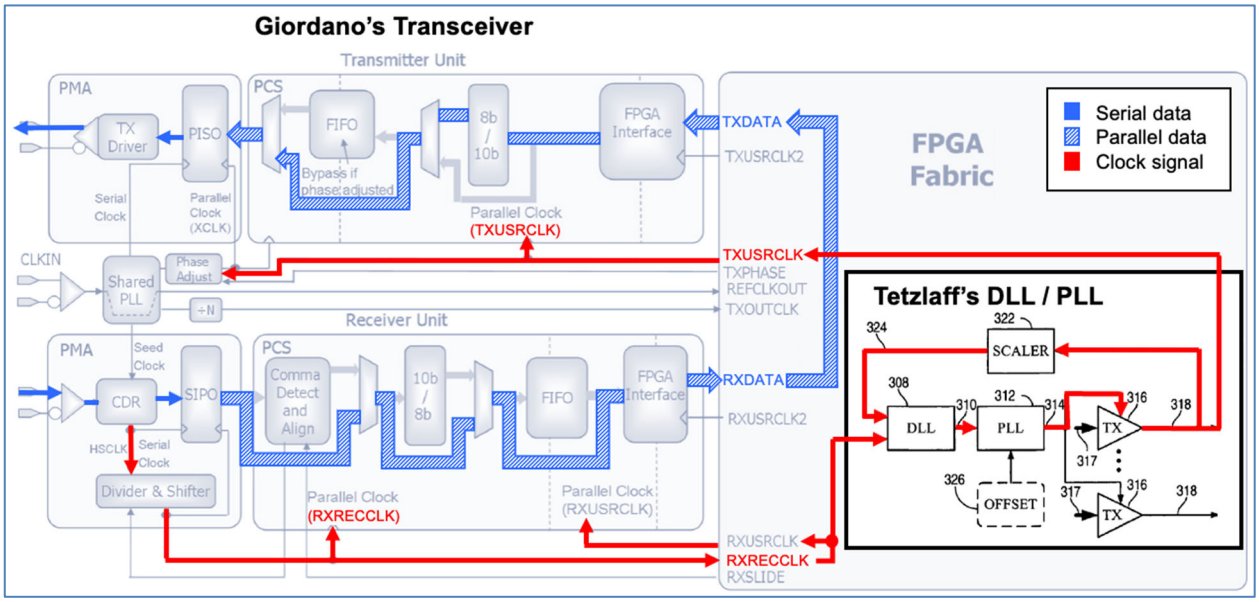
VI. GROUNDS FOR UNPATENTABILITY

A. Ground 1: Claims 1, 4–12 Are Rendered Obvious by Giordano in View of Tetzlaff

1. Overview

Giordano's FPGA comprises two portions—a Xilinx Virtex-5 "RocketIO" GTP transceiver (with separate receiver and transmitter sides) and an FPGA Fabric. Ex. 1005, 195. The GTP transceiver comprises preprogrammed (but with user-configurable operating parameters and settings) hardware commonly referred to as hard-macro tiles. *Id*., 4; Ex. 1003, ¶107. In contrast, the FPGA Fabric comprises user-programmable hardware. Ex. 1003, ¶107.

The image below, based on Figure 1 of Giordano and Figure 3 of Tetzlaff with modifications, depicts this proposed combination:



Giordano's GTP transceiver generates a receiver-side clock signal, RXRECCLK, from a clock extracted from incoming serial data, and provides RXRECCLK to Tetzlaff's DLL/PLL implemented in the FPGA Fabric. Ex. 1003, ¶112. The DLL/PLL block creates a transmitter-side clock signal TXUSRCLK that is phase-matched to RXRECCLK, and sent to the transmitter of the GTP transceiver. *Id*.

a. Motivation to Combine Giordano and Tetzlaff

A POSITA would have been motivated to combine Giordano and Tetzlaff because they address synchronization and phase alignment of clock signals in FPGA transceivers. Ex. 1003, ¶113. Giordano seeks fixed-latency timing synchronization and clock distribution in Xilinx GTP transceivers, while Tetzlaff addresses clock

skew through "clock distribution, phase alignment, and frequency synchronization via high speed serial I/O transceivers." Ex. 1005, 194; Ex. 1006, 2:9–16, 4:24–26.

Giordano identifies the need that Tetzlaff's teachings fulfill. While Giordano's fixed latency architecture achieves deterministic (*i.e.*, fixed) phase relationships between the receiver clock and transmit clock, Giordano identifies gaps for directly using this receiver clock for the transmitter. Ex. 1005, 198; Ex. 1003, ¶115. Giordano states:

> *The clock recovered by the receiver cannot be directly used as a reference clock for the re-transmission. In fact, the internal PLL is shared among the transmitters and receivers in the same tile and at the receiver tile it is already locked to the seed clock. Moreover, the recovered clock might also require to be filtered in order to match the jitter specifications for the GTP reference clock.*

Ex. 1005, 198. Tetzlaff provides precisely such a solution through a DLL/PLL architecture that filters jitter and generates a transmit clock aligned "to the phase of the source clock." Ex. 1006, 9:29–51; 6:27–47, cls. 1, 5.

A POSITA reading Giordano would have naturally consulted Xilinx's own materials (such as Tetzlaff, a Xilinx patent), for a PLL-based phase alignment solution. Giordano repeatedly references the Xilinx RocketIO GTP Transceiver User Guide, and Tetzlaff (a Xilinx patent) expressly incorporates that same guide by reference. Ex. 1005, 194, 197–199; Ex. 1006, 7:25–36.

Incorporating Tetzlaff's DLL/PLL teachings into Giordano would require only programming existing FPGA Fabric logic. Ex. 1003, ¶114.

Giordano demonstrates programming custom hardware in the FPGA Fabric. Giordano implemented a custom Comma Detector and Aligner in the FPGA Fabric because the GTP's built-in comma detector (which is a fixed block inside the transceiver) operated only in unsupported modes. Ex. 1005, 198; Ex. 1003, ¶108. Giordano also discloses implementing DLL blocks "external to the GTP" transceiver, *i.e.*, on the FPGA Fabric. Ex. 1005, Fig. 5; Ex. 1003, ¶108. Implementing Tetzlaff's DLL/PLL in the FPGA Fabric thus represents a straightforward extension of techniques already used in Giordano. Ex. 1003, ¶117.

Such FPGA hardware programming is how the '587 patent suggests implementing its claimed invention, which programs components such as phase detector, phase controller, DLL, and PLL in an "FPGA Core" mirroring Giordano's FPGA Fabric. Ex. 1001, Figs. 3A–F, 4A–C, 5A–F, 26:44–50; Ex. 1003, ¶109.

A POSITA would have had a reasonable expectation of success. Giordano's FPGA implementation was physically tested on Xilinx evaluation boards and used circuit blocks similar to those disclosed in Tetzlaff, including PLLs, DLLs, serializers, and pattern generators which were implemented on the programmable FPGA Fabric as the user intended. Ex. 1005, 195, 197–200; Ex. 1006, 1:23–48; Ex. 1003, ¶119. Because both references rely on the same Xilinx FPGA infrastructure, there would have been high expectations that, through routine FPGA programming, the combination functions as intended. Ex. 1003, ¶119.

b. Features of Virtex-UG are Inherent to Giordano, and Giordano Incorporates Virtex-UG by Reference

Giordano presents a system with the "RocketIO" GTP transceiver of the Xilinx Virtex-5 FPGA family. Ex. 1005, 194, 199. Giordano repeatedly references the RocketIO GTP Transceiver, for example referencing the overall transceiver architecture (*id*., 195) and taking estimated latency values from the RocketIO GTP Transceiver User Guide (*id*., 198). Giordano further describes phase alignment of clock signals, and that "the procedure we follow for activating the alignment circuit is the one suggested in the GTP user's guide." *Id*., 197. A POSITA would have known to reference Xilinx documents on the GTP transceiver to understand the relevant inherent features. Ex. 1003, ¶78. As such, Giordano inherently discloses the features of Virtex-UG. *Id*.

In such a case, the features of the Virtex-UG are necessarily present in Giordano, and it is proper to use extrinsic evidence (such as the Virtex-UG) to understand said features. *See Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1328 (Fed. Cir. 2001) ("[R]ecourse to extrinsic evidence is proper to determine whether a feature, while not explicitly discussed, is necessarily present in a reference. The evidence must make clear that the missing feature is necessarily present, and that it would be so recognized by persons of ordinary skill in the relevant art."); *Sage Prods., LLC v. Stewart*, 133 F.4th 1376, 1385 (Fed. Cir. 2025) ("There was likewise nothing improper in the Board relying on evidence outside of the PAR

to make findings as to what the skilled artisan would understand the PAR to be disclosing."); *Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1345 (Fed. Cir. 2018) ("It is well established that such reliance on extrinsic evidence is proper in an inherency analysis."); *see also In re Haines*, No. 2024-2338, 2025 WL 1403578, at *2 (Fed. Cir. May 15, 2025) (examiner properly used another publication "as evidence to explain why [the prior art's] disclosure of a mass spectrometer implicitly discloses 'obtaining mass spectral channel signals (m/z)'" (cleaned up)).

For the same reasons as above, Giordano incorporates Virtex-UG (Ex. 1009) by reference. Ex. 1005, 197 ("the procedure we follow for activating the alignment circuit is the one suggested in the GTP user's guide."). Virtex-UG, by incorporation, becomes part of the disclosures of Giordano. *Verizon Connect Inc. v. Omega Patents, LLC*, IPR2023-01162, 2024 WL 714951, at *3, 14-15 (P.T.A.B. Feb. 21, 2024) (the incorporated secondary reference's disclosures become part of the primary reference); *Paice LLC v. Ford Motor Co.*, 881 F.3d 894, 906-07 (Fed. Cir. 2018) ("[T]he standard of one reasonably skilled in the art should be used to determine whether the host document describes the material to be incorporated by reference with sufficient particularity.") (citing *Advanced Display Systems, Inc. v. Kent State University*, 212 F.3d 1272 (2000)).

2. Analysis

a. Independent Claim 1

[1.pre]: A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:

To the extent limiting, Giordano discloses [1.pre]. Ex. 1003, ¶122.

Giordano discloses a Xilinx Virtex-5 FPGA that includes "serializer-deserializer (SerDes)." Ex. 1005, 194. Giordano discloses a receiver taking in serial data, and a transmitter sending out processed serial data. Ex. 1003, ¶123; *infra*, [1.b] and [1.i].

[1.a]: (a) receiving, by a deserializer in a field programmable array, a clock signal;

Giordano's Receiver Unit PMA discloses the claimed "deserializer," and HSCLK clock discloses the "clock signal." Ex. 1003, ¶125. Receiver Unit PMA "receives" a signal comprising HSCLK. *Id*.

Giordano discloses the GTP transceiver, which includes separate "Receiver Unit" and "Transmitter Unit." Ex. 1005, 194. Within each receiver- and transmitter-unit are a Physical Medium Attachment ("PMA") and Physical Coding Sublayer ("PCS"). *Id*., 194–195. Giordano points to the PMA sublayer as the component "actually serializing and de-serializing the data," and the PCS layer as "processing" data. *Id*., 194. The Receiver Unit PMA further includes a "Serial In to Parallel

Output (SIPO)" block, which deserializes incoming serial data. *Id*., 195–196; Ex. 1003, ¶126.

Giordano's Receiver Unit PMA has a Clock and Data Recovery ("CDR") block, "which extracts a clock (HSCLK)" from the incoming serial data stream. Ex. 1005, 195.

This mirrors the '587 patent, which describes a deserializer with a receiver PMA. Ex. 1001, 53:31–33, Fig. 6E. This receiver PMA further comprises a CDR block. *Id*. Like Giordano, the CDR block of the '587 patent receives serial data, and extracts a clock signal from the incoming serial data. Ex. 1001, 53:34–48.

[1.b]: (b) receiving, by the deserializer, the first serial data stream;

Giordano's Receiver Unit PMA ("deserializer") has a CDR that receives incoming serial data, which discloses the "first serial data stream." Ex. 1005, 195; Ex. 1003, ¶129.

This mirrors the '587 patent, which describes a receiver PMA with a CDR that receives serial data. Ex. 1001, 53:34–48, Fig. 6E.

[1.c]: (c) generating, by the deserializer, a receiver side clock signal;

Giordano's parallel recovered clock (RXRECCLK) discloses the "receiver side clock signal." Ex. 1003, ¶131.

The CDR in Giordano's Receiver Unit PMA extracts a clock (HSCLK) signal from the incoming serial data. Ex. 1005, 195. HSCLK is then used to "generate a

parallel recovered clock (RXRECCLK)" for the SIPO block and Receiver Unit PCS. *Id*.; Ex. 1003, ¶131. This RXRECCLK discloses the claimed "receiver side clock signal." Ex. 1003, ¶131.

This mirrors the '587 patent, which describes a CDR that receives serial data, and generates clock signals for blocks such as Serial to Parallel and receiver PCS. Ex. 1001, 53:34–48, Fig. 6E.

[1.d]: (d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;

Giordano's SIPO block output discloses the "first plurality of parallel data streams." Ex. 1003, ¶134.

Giordano's Receiver Unit PMA ("deserializer") has a SIPO block that converts incoming serial data ("first serial data stream") to parallel data, which discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶134.

This mirrors the '587 patent, which describes a Serial to Parallel block within the Receiver PMA that "converts the serial data into parallel data, transmitting the parallel data to the receiver PCS." Ex. 1001, 53:44–48, Fig. 6E.

[1.e]: (e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;

Giordano's Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS individually and collectively disclose the "computational circuitry in the [FPGA]." Ex. 1003, ¶137.

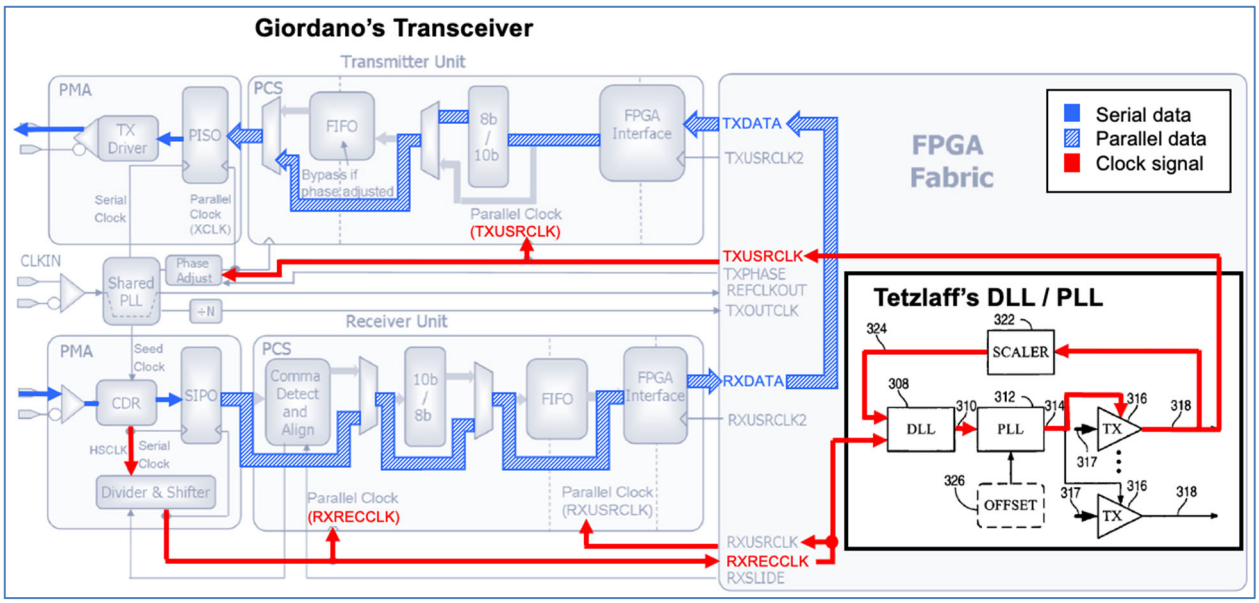
Giordano points to the PCS (both receiver and transmitter sides) as "processing" data, disclosing computational circuitry. Ex. 1005, 194; Ex. 1003, ¶137. Giordano's description that the FPGA Fabric includes "logic" discloses the claimed "computational circuitry in the [FPGA]." Ex. 1005, 195–196; Ex. 1003, ¶137. Giordano discloses that the output of the SIPO block ("first plurality of parallel data streams") is transmitted to the Receiver Unit PCS. Ex. 1005, Fig. 1; Ex. 1003, ¶137.

This mirrors the '587 patent, with figures depicting computational circuitry capable of performing a logical operation as "Computation Logic." Ex. 1001, Figs. 4B–C, 5A–F, cl. 4.

[1.f]: (f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;

Giordano in view of Tetzlaff renders obvious this limitation. Ex. 1003, ¶139.

Tetzlaff's DLL/PLL programmed in Giordano's FPGA Fabric discloses the claimed "phase lock loop." Ex. 1003, ¶140. The combination is depicted below:



Giordano discloses providing RXRECCLK (*i.e.*, "receiver side clock signal") to the Receiver Unit PCS and FPGA Fabric. Ex. 1005, 195; Ex. 1006, Fig. 3; Ex. 1003, ¶141. A POSITA would have understood that FPGA-Fabric blocks, including Tetzlaff's DLL/PLL circuitry, receive RXRECCLK. Ex. 1003, ¶141.

In the proposed combination, the FPGA Fabric creates a clock path from RXRECCLK (*i.e.*, "receiver side clock signal") to TXUSRCLK (*i.e.*, "transmitter side clock signal"), with Tetzlaff's DLL/PLL jitter-filtering and phase-alignment feedback loop between the two clocks. Ex. 1003, ¶144. RXRECCLK is provided to Tetzlaff's DLL/PLL circuitry, which outputs TXUSRCLK and feeds it back for phase matching. *Id*. The result is a clean transmitter-side clock phase matched to the receiver-side clock. Ex. 1005, 198; Ex. 1003, ¶144.

[1.g]: (g) generating, using the phase lock loop, a transmitter side clock signal;

Giordano in view of Tetzlaff renders obvious this limitation. Ex. 1003, ¶145. As discussed in [1.f], Tetzlaff's DLL/PLL discloses the claimed "phase lock loop."

The output of the combined DLL/PLL results in a "transmitter side clock signal" TXUSRCLK. Ex. 1003, ¶145.

[1.h]: (h) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams;

Giordano's processed parallel data exiting the Transmitter Unit PCS into the PMA, *i.e.*, PISO block input, discloses the "second plurality of parallel data streams." Ex. 1005, Fig. 1; Ex. 1003, ¶146.

As to "set of operations," Giordano describes an FPGA Fabric that includes "logic," which discloses this limitation. Ex. 1005, 195–196, 198; Ex. 1003, ¶147. Giordano describes programming a Comma Detector and Aligner in the FPGA Fabric, which performs "comma detection." Ex. 1005, 198; Ex. 1003, ¶147. Giordano's "comma detector looks for commas (*e.g.*, the one included in the K28.5 symbol) and when it finds one it determines how many bit shifts" are "required in order to align the parallel data." Ex. 1005, 198; Ex. 1003, ¶147. A POSITA would have understood this pattern matching operation (to locate comma characters) and computing number of bit shifts for alignment to disclose the claimed "set of operations." Ex. 1003, ¶147.

In addition, Giordano points to the PCS layer (both receiver and transmitter sides) as "processing" data, disclosing the computational circuitry. Ex. 1005, 194; Ex. 1003, ¶148. The PCS layer includes 8b/10b encoding / decoding functions, which require arithmetic calculations hence disclosing "set of operations." Ex. 1005, 197; Ex. 1003, ¶148.

[1.i]: (i) converting the second plurality of parallel data streams, by a serializer, into a second serial data stream; and

Giordano's Transmitter Unit PMA discloses the claimed "serializer." Ex. 1005, 195–196; Ex. 1003, ¶151. The Transmitter PMA includes a Parallel Input to Serial Output ("PISO") block that converts parallel data ("second plurality of parallel data streams") to serial data. Ex. 1005, 195; Ex. 1003, ¶151. The serial data output of PISO discloses the "second serial data stream." Ex. 1003, ¶151.

This mirrors the '587 patent, which describes a serializer with a transmitter PMA with a Parallel to Serial block. Ex. 1001, 54:9–29, Fig. 7B. Like Giordano, this Parallel to Serial block converts the incoming parallel data to serial data. *Id*.

[1.j]: (j) transmitting, from the field programmable gate array system, the second serial data stream,

The Transmitter Unit PMA in Giordano has a TX Driver that sends out serial data, which discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶153.

This mirrors the '587 patent, which describes a Transmitter PMA with a Transmitter Buffer that sends out serial data. Ex. 1001, 54:9–29, Fig. 7B.

[1.k]: wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

Giordano discloses bypassing a First In First Out (FIFO) buffer, a circuit block allowing safe data transfer between different clock domains (*e.g.*, "data transfers between TXUSRCLK domain and the XCLK domain"). Ex. 1005, 195; Ex. 1003, ¶156. A POSITA would have understood FIFO as a clock domain crossing circuit, and Giordano's bypassing of the FIFO block discloses this limitation. Ex. 1003, ¶156.

Giordano discloses bypassing the FIFO buffer by having the two clock domains have "the same phase" and "therefore also the same latency for the data." Ex. 1005, 195; Ex. 1003, ¶157. In the transmitter, Giordano discusses two clocks (XCLK and TXUSRCLK) that are adjusted to have the same frequency and phase. Ex. 1005, 195. The transmitter has a FIFO block for crossing between XCLK and TXUSRCLK clock domains. *Id.*; Ex. 1003, ¶158. Giordano discloses bypassing this FIFO block by using a phase alignment option provided in Xilinx Virtex-5 FPGAs. Ex. 1005, 195; Ex. 1003, ¶158. Through this built-in phase alignment, XCLK and TXUSRCLK are phase aligned, in which "the transmit FIFO is unnecessary and therefore we bypassed it." Ex. 1005, 197.

Virtex-UG further discloses[4] this limitation. Ex. 1003, ¶158. In the receiver, Virtex-UG, which Giordano inherently discloses and incorporates by reference, confirms this FIFO bypass. When receiver clock phase alignment is used, "RXUSRCLK must be driven directly from RXRECCLK using a BUFR regional clock buffer." Ex. 1009, 179 ("Using RX Phase Alignment to Bypass the RX Elastic Buffer"). Due to phase alignment, "SIPO parallel clock phase matches RXUSRCLK phase" and there is "no phase difference between XCLK and RXUSRCLK." *Id*., 180. With no phase difference, the RX Elastic Buffer (which is the FIFO block described in Giordano) is bypassed. This bypass is described in the red arrow below in Figure 7-22 of Virtex-UG:

[4] Unless noted otherwise, the Virtex-UG's disclosures in this Petition are express and also inherent.

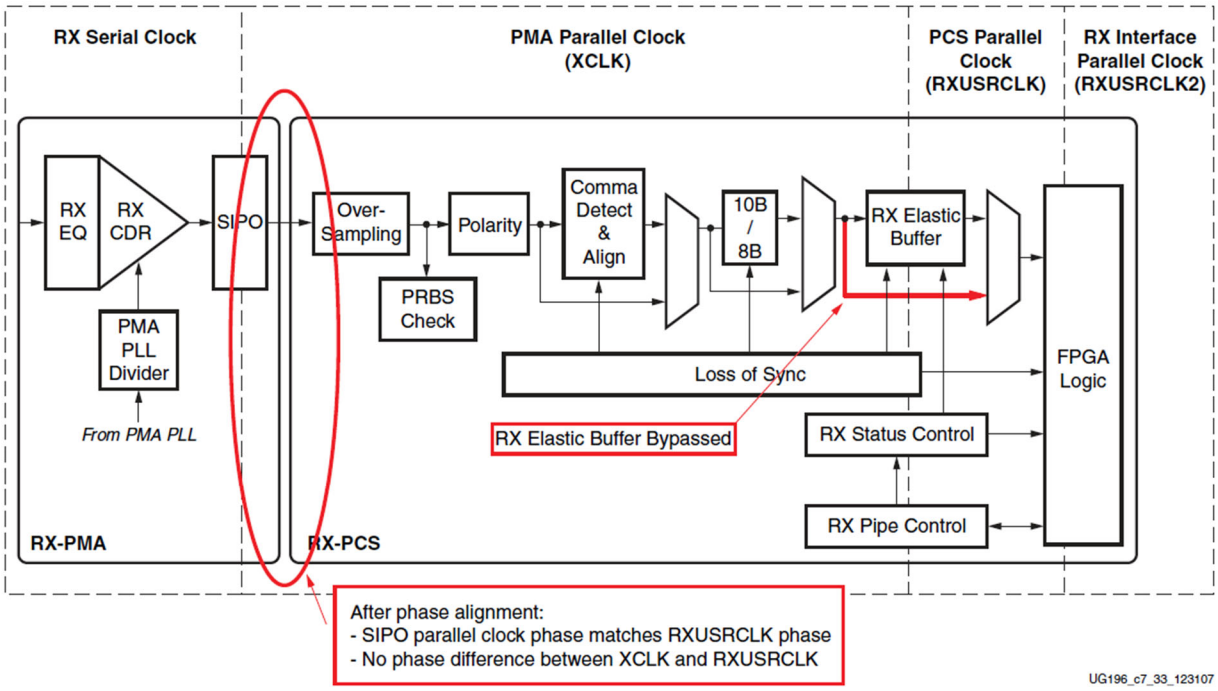


Figure 7-22: **Using Phase Alignment**

The bypass of all clock domain crossing circuits after phase alignment of clock signals, as in Giordano, discloses this limitation. Ex. 1003, ¶159.

b. Claim 4

[4]: The method of claim 1, wherein the set of operations includes at least one of the following:

(i) an arithmetic operation;

(ii) a logical operation;

(iii) a pipeline operation; and

(iv) a memory access operation.

The operations on PCS layers and FPGA Fabric disclose this limitation.

Giordano's Comma Detector and Aligner implemented in the FPGA Fabric performs pattern matching (detecting comma characters in the raw 10-bit data),

comparison (determining the number of bit shifts required), and conditional branching (the even/odd decision logic that either applies RXSLIDE assertions or resets the CDR). Ex. 1005, 198. These are examples of logical operations, which disclose this limitation. Ex. 1003, ¶161.

In addition, Giordano points to the PCS layer (both receiver and transmitter sides) as "processing" data, disclosing the computational circuitry. Ex. 1005, 194; Ex. 1003, ¶161. The PCS layer includes 8b/10b encoding / decoding functions, which require arithmetic calculations hence disclosing this claim. Ex. 1005, 197; Ex. 1003, ¶161.

Tetzlaff discloses that FPGAs may be programmed to include "logic of a user design" including "arithmetic logic." Ex. 1006, 1:28–33. Tetzlaff further discloses "digital signal processing blocks (DSPs)" as a type of programmable tile in the FPGA which are purpose-built hardware for arithmetic operations. Ex. 1006, 1:28–33; Ex. 1003, ¶162. Tetzlaff teaches that the FPGA includes "dedicated random access memory blocks (BRAM)" as one of the programmable tile types, disclosing a memory access operation. Ex. 1006, 1:28–33; Ex. 1003, ¶162.

c. Claims 5–7

[5]: The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed prior to step (g).

[6]: The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed after step (g).

[7]: The method of claim 1, wherein all of the set of operations performed in step (h) are performed after step (g).

Claims 5 through 7 concern the order of step (g) (generating transmitter side clock) and step (h) (performing computational operations). Giordano discloses performing these steps independently because neither depends on completion of the other. Ex. 1003, ¶163. Both steps require the receiver side clock, but otherwise operate separately. Ex. 1003, ¶163.

For step (h), the combination of Giordano and Tetzlaff requires only that the receiver side clock be available before computational operations begin; it is agnostic to whether the transmitter side clock is prepared. In Giordano, the FPGA Fabric receives deserialized parallel data from the GTP receiver and processes it using the receiver-side clock. Ex. 1005, 198 ("recovered clock (RXRECCLK) drives the receive clocks (RXUSRCLK and RXUSRCLK2)."). Thus, the parallel data output from the deserializer into the FPGA Fabric is clocked by RXUSRCLK derived from RXRECCLK. *Id.*; Ex. 1003, ¶164. This processing does not require generation of the transmitter-side clock.

Step (g), by contrast, concerns generating a transmitter-side clock from RXRECCLK. The clock-generation process likewise does not depend on when the FPGA Fabric processes incoming parallel data.

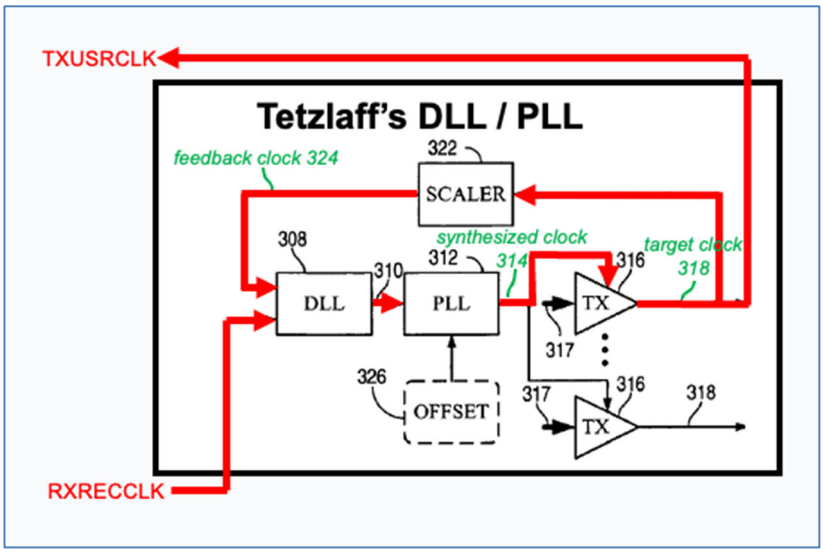
Because the two operations are independent, a POSITA would have found it obvious to perform step (h) before, during, or after step (g). Ex. 1003, ¶165.

d. Claim 8

[8.pre]: 8. The method of claim 1, wherein step (g) further comprises:

[8.a]: (k) generating, by the phase lock loop, a feedback clock signal associated with the transmitter side clock signal by performing the following steps until a first output of a phase detector of the field programmable gate array system is below a first threshold level:

Tetzlaff's DLL/PLL discloses the claimed "phase lock loop." Annotated image of Tetzlaff's DLL/PLL is below:



Tetzlaff's feedback clock 324 discloses the claimed "feedback clock signal." Ex. 1003, ¶168. Tetzlaff discloses that "feedback clock on line 324 may represent

the phase of the target clock on line 318." Ex. 1006, 10:15–23. The target clock 318 is the transmitter side clock signal ("TXUSRCLK"), hence the feedback clock 324 is "associated with" TXUSRCLK. Ex. 1003, ¶172.

Tetzlaff discloses that the "DLL's phase detector controls a delay line," where said delay line modifies the output "until the reference clock signal is synchronized" with the target clock. Ex. 1006, 2:49–55. That phase detector discloses the claimed "phase detector." Ex. 1003, ¶170.

Since the DLL phase detector "controls" the DLL delay line, interim components and signals for control, such as the claimed "first output of a phase detector," are necessarily disclosed by Tetzlaff's DLL. Ex. 1003, ¶181.

Tetzlaff further discloses an iterative process where the DLL repeatedly adjusts delay until the target clock 318 is phase matched with the incoming reference clock, which discloses performing the claimed steps until "first output" is "below a first threshold level." Ex. 1003, ¶169.

Tetzlaff describes this iterative lock acquisition process explicitly, noting that the DLL undergoes "lock acquisition"—defined as "[t]he time in which the DLL is attempting to first synchronize the reference clock signal and skewed clock signal." *Id*., 2:65–3:1. This DLL then "monitors the reference clock signal" and the target clock signal, and "adjusts the amount of [] delay to maintain synchronization." *Id*., 2:56–59. "The time in which the DLL is attempting to maintain synchronization is

referred to as lock maintenance." Ex. 1006, 2:67–3:4. Tetzlaff teaches that this feedback loop operates iteratively until lock is achieved, hence discloses this limitation. Ex. 1003, ¶171.

Tetzlaff's PLL independently reinforces this limitation. Its PLL includes phase-detection circuitry maintaining a selectable phase offset between synthesized and reference clocks using a feedback loop. Ex. 1006, 10:24–33; Fig. 1B. The PLL may add phase adjustment "in addition to or instead of" DLL adjustment. *Id*.

[8.b]: (1) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal;

Tetzlaff's DLL delay line and PLL VCO disclose the claimed "adjustable oscillator." Ex. 1003, ¶174. Tetzlaff's synthesized clock 314 discloses the claimed "second clock signal." *Id*.

Tetzlaff discloses DLLs that include a phase detector that compares the phase of two signals. Ex. 1006, 2:26–55. That "phase detector is then used to detect the associated phase differences and to control the delay line" to phase match the reference and output clocks. Ex. 1006, 2:38–41.

Tetzlaff discloses a charge pump, loop filter, and voltage-controlled oscillator (VCO) within the PLL block. Ex. 1006, 6:27–47; Fig. 1B; Ex. 1003, ¶176. This VCO "or similar variable frequency oscillator" aligns the phases of the synthesized clock with the reference clock. *Id*., 10:24–33.

For the phase matching capabilities, the DLL delay line and PLL VCO are exemplary elements that disclose the claimed "adjustable oscillator." Ex. 1003, ¶177.

Referring to the Tetzlaff image above in [8.a], after the DLL 308 and emanating from PLL 312 is a synthesized clock 314. Ex. 1006, 9:34–51. This synthesized clock 314 discloses the claimed "second clock signal." Ex. 1003, ¶177.

This mirrors the '587 patent, which notes that "the adjustable oscillator [] may be implemented with a digital delay line." Ex. 1001, 39:7–9.

[8.c]: (2) generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal;

As discussed in [8.a] and [8.b], Tetzlaff's DLL/PLL discloses the "phase detector" and "first output," feedback clock 324 discloses the claimed "feedback clock signal," and synthesized clock 314 discloses the "second clock signal."

Tetzlaff's DLL/PLL discloses comparing the phase of the receiver side clock (RXRECCLK) with that of the feedback clock 324, disclosing this limitation. Ex. 1003, ¶179. Tetzlaff discusses that conventional DLLs typically include a delay line and a phase detector, and receives a reference clock signal and drives an output clock signal. Ex. 1006, 2:26–55. "A phase detector is then used to ***detect the associated phase differences*** and to ***control*** the delay line" which allows phase matching between the reference and output clocks. Ex. 1006, 2:38–41. This necessitates

generating a control signal for the delay line. Ex. 1003, ¶179. The DLL/PLL's detection of the phase difference between signals, and using that difference to generate a control signal for the delay line, discloses "generating…the first output." *Id*.

[8.d]: (3) transmitting, from the phase detector to a phase controller of the field programmable gate array system, the first output;

As discussed in [8.a] and [8.c], Tetzlaff's DLL discloses the "phase detector" and "first output."

Tetzlaff's phase adjustments in the DLL/PLL discloses this limitation. Ex. 1003, ¶180.

"A phase detector is then used to detect the associated phase differences and to ***control*** the delay line" which allows phase matching between the reference and output clocks. Ex. 1006, 2:38–41. Since the DLL phase detector "controls" the DLL delay line, interim components and signals for such control, including the claimed "phase controller," are necessarily disclosed by Tetzlaff's DLL. Ex. 1003, ¶181.

Indeed, Tetzlaff discloses that "the actual control mechanism for the DLL can differ" as long as "the DLL monitors" the reference and output clocks, and "adjust the amount of propagation delay to maintain synchronization." Ex. 1006, 2:49–59. Tetzlaff discloses that DLL "signal control is achieved" by its embodiments. *Id*., 4:36–38. This mirrors how the '587 patent suggests programming the FPGA for

"event-based system to run the control algorithm for either the PLL or DLL paths on the device." Ex. 1001, 55:45–55.

Using the detected phase difference to control the DLL delay line discloses "transmitting…the first output" to the "phase controller." Ex. 1003, ¶182.

[8.e]: (4) determining, by the phase controller, interim adjustment information based on the first output; and

As discussed in [8.d], Tetzlaff's DLL discloses the "phase controller."

Tetzlaff's phase adjustments in the DLL/PLL discloses this limitation. Ex. 1003, ¶183.

"A phase detector is then used to detect the associated phase differences and to ***control*** the delay line" which allows phase matching between the reference and output clocks. Ex. 1006, 2:38–41. Since the DLL phase detector "controls" the DLL delay line, interim components and signals for such control, including the claimed "interim adjustment information," are necessarily disclosed by Tetzlaff's DLL. Ex. 1003, ¶184. The control of the DLL delay line to phase match clocks, using information from the phase detector, necessarily requires information for said control, which discloses the "interim adjustment information." *Id*.

Tetzlaff further describes this phase matching process as iterative, noting that "[t]he time in which the DLL is attempting to first synchronize the reference clock signal and skewed clock signal, is referred to as lock acquisition." Ex. 1006, 2:65–

3:4. The iterative process of Tetzlaff discloses the "interim" nature of this "adjustment information." Ex. 1003, ¶185.

[8.f]: (5) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information;

As discussed in [8.b], [8.c], and [8.e], Tetzlaff's DLL delay line and/or PLL VCO disclose the "adjustable oscillator," and DLL discloses the "phase controller" and "interim adjustment information."

Tetzlaff's phase adjustments in the DLL/PLL discloses this limitation. Ex. 1003, ¶187.

Tetzlaff discloses that the DLL's phase detector "control[s]" the delay line to synchronize the reference clock with the feedback signal. Ex. 1006, 2:26–55; Ex. 1003, ¶187. Since the DLL phase detector "controls" the DLL delay line, interim components and signals for such control, including "phase controller" transmitting control-related signals to the "adjustable oscillator," are necessarily disclosed by Tetzlaff's DLL. Ex. 1003, ¶187.

Control of the DLL delay line necessitates sending information to said delay line for such control. Ex. 1003, ¶188. As the DLL delay line discloses the "adjustable oscillator," Tetzlaff's control of the delay line discloses this limitation. Ex. 1003, ¶188.

[8.g]: wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information,

As discussed in [8.b] and [8.e], Tetzlaff's DLL delay line and/or PLL VCO disclose the "adjustable oscillator," synthesized clock 314 discloses the "second clock signal," and DLL discloses the "interim adjustment information."

Referring to the Tetzlaff image above in [8.a], after the DLL 308 and PLL 312 is a synthesized clock 314. Ex. 1006, 9:34–51. As such, Tetzlaff discloses that the DLL delay line and PLL VCO adjust the phase for the signals along the feedback data path, resulting in adjusting the synthesized clock 314. Ex. 1003, ¶190.

Tetzlaff's DLL phase detector "control[s]" the delay line to synchronize the reference clock with the feedback signal. Ex. 1006, 2:26–55; Ex. 1003, ¶191. Since the DLL phase detector "controls" the DLL delay line, interim components and signals for such control are necessarily disclosed by Tetzlaff's DLL. Ex. 1003, ¶191. As such, Tetzlaff's delay line modifying the feedback signal discloses this limitation. *Id*.

Tetzlaff's PLL "acts to maintain a selectable phase offset between the synthesized clock and the reference clock." Ex. 1006, 10:24–33. Tetzlaff discloses that the selectable offset may be added to the synthesized clock "in addition to or instead of the phase adjustment provided by the DLL." *Id*. This phase modification of the feedback signal discloses this limitation. Ex. 1003, ¶192.

[8.h]: wherein steps (1) through (5) are repeated until the first output of the phase detector is below the first threshold level, and

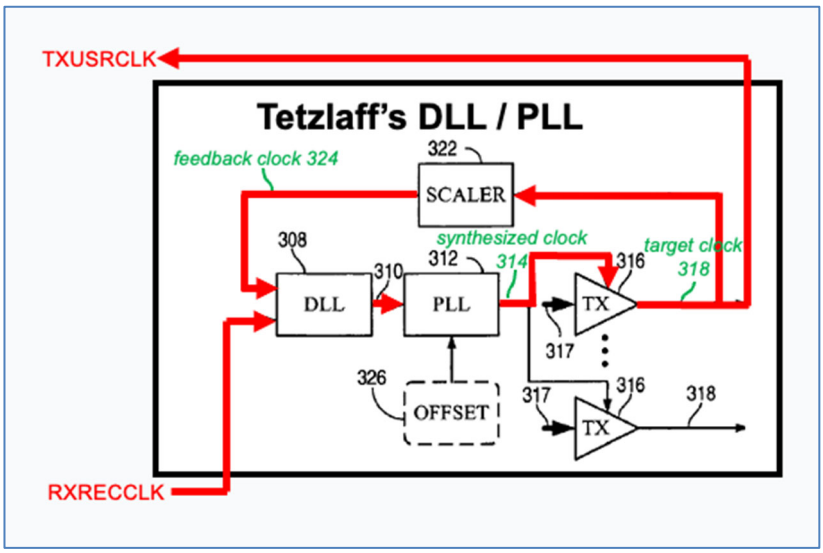
As discussed in [8.a], Tetzlaff's DLL (which includes a phase detector) discloses the "first output." Tetzlaff's DLL/PLL discloses this limitation. Ex. 1003, ¶193.

Tetzlaff discloses the DLL producing the transmit clock "by phase shifting the synthesized clock [] to match the phase of the feedback." Ex. 1006, 10:55–59. Tetzlaff describes this iterative lock acquisition process explicitly, noting that "[t]he time in which the DLL is attempting to first synchronize the reference clock signal and skewed clock signal, is referred to as lock acquisition. The time in which the DLL is attempting to maintain synchronization is referred to as lock maintenance." Ex. 1006, 2:65–3:4. Tetzlaff teaches that this feedback loop operates iteratively until lock is achieved, hence discloses this limitation. Ex. 1003, ¶194.

[8.i]: wherein the transmitter side clock signal is associated with the second clock signal.

As discussed in [8.b], the synthesized clock 314 discloses the "second clock signal."

Tetzlaff's DLL/PLL discloses this limitation. Ex. 1003, ¶195. An annotated image of Tetzlaff's DLL/PLL is below:



The target clock 318 is the transmitter side clock signal (TXUSRCLK). Tetzlaff discloses that the target clock 318 is used to generate the feedback clock 324, which in turn is used to generate the synthesized clock 314. Ex. 1006, 9:61–10:14. This relationship supports that the target clock 318 is "associated with" synthesized clock 314, disclosing this limitation. Ex. 1003, ¶196. The feedback clock 324, synthesized clock 314, and target clock 318 are generated by Tetzlaff's DLL/PLL, mirroring how the '587 patent's "associated" signals—"feedback clock signal," "second clock signal," and "transmitter side clock signal"—are all generated by the claimed "phase lock loop." Ex. 1001, cl. 8; Ex. 1003, ¶196.

e. Claim 9

[9]: The method of claim 1, wherein the first plurality of parallel data streams has the same number of data streams as the second plurality of parallel data streams.

Giordano's use of 8b/10b encoding / decoding discloses this limitation. Ex. 1003, ¶197.

Giordano discloses using 8b/10b encoding, where the SIPO deserializes the incoming stream into 10-bit parallel words, which are then outputted as 8-bit parallel data words. Ex. 1005, 195. On the transmit side, the FPGA fabric supplies 8-bit parallel data words to the GTP, which encodes them using the internal 8b-to-10b encoder before the PISO serializes the resulting 10-bit words. Ex. 1005, 195, 197. A POSITA would have found it obvious to have what is identified as the first plurality of parallel data streams to be the same as the second plurality of parallel data streams, either 8-bits or 10-bits. Ex. 1003, ¶197.

f. Claim 10

[10]: The method of claim 1, wherein the first plurality of data streams and the second plurality of data streams comprise one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

Giordano's use of 8-bit parallel words (eight data streams) and 10-bit parallel words (ten data streams) disclose this limitation. Ex. 1005, 195; Ex. 1003, ¶200.

g. Claim 11

[11]: The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and phase.

Giordano in view of Tetzlaff renders obvious this limitation. Ex. 1003, ¶201. As discussed in claim 1, RXRECCLK discloses the "receiver side clock signal," and TXUSRCLK discloses the "transmitter side clock signal."

As to frequency alignment, Tetzlaff teaches that the PLL synthesizes a clock "having a frequency corresponding to a frequency of the reference clock multiplied by a ratio of selectable integers." Ex. 1006, cl. 8. When a ratio of 1 is selected, the PLL output (*e.g.*, TXUSRCLK) has the same frequency as its reference clock (*e.g.*, RXRECCLK). Ex. 1003, ¶202.

As to phase alignment, both Giordano and Tetzlaff disclose two clocks having the same phase. Giordano states that it uses "the phase alignment circuit, which aligns the phase of XCLK to the one of TXUSRCLK. Since TXUSRCLK is generated with a deterministic phase from the reference clock, this leads to have XCLK, TXUSRCLK and the reference clock running [*i.e.*, RXRECCLK] with a deterministic fixed phase." Ex. 1005, 197. This "deterministic fixed phase" would be understood as a constant difference, including zero (*i.e.*, two signals having the same phase). Ex. 1003, ¶203.

Tetzlaff discloses how DLLs may use a delay line to control the phase difference between two signals, including making the two "synchronized." Ex. 1006, 2:26–41, 2:49–55. In addition, Tetzlaff discloses that "PLL acts to maintain a selectable phase offset between the synthesized clock and the reference clock." Ex. 1006, 10:24–33. This includes "phase shifting the synthesized clock" to "match the phase of the feedback." *Id.*, 10:55–59.

The combination of Giordano and Tetzlaff would therefore be able to generate a TXUSRCLK signal that has the same frequency and phase as RXRECCLK. The combined system therefore renders obvious this limitation. Ex. 1003, ¶204.

h. Claim 12

[12]: The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and different phases.

Giordano in view of Tetzlaff renders obvious this limitation. Ex. 1003, ¶205. As discussed in claim 11, combination of Giordano and Tetzlaff would be able to generate a TXUSRCLK signal that has the same frequency as RXRECCLK.

In addition, the same combination would be able to generate a TXUSRCLK signal that has the same frequency but a different, fixed phase to RXRECCLK. Ex. 1003, ¶205.

Giordano states that it uses "the phase alignment circuit, which aligns the phase of XCLK to the one of TXUSRCLK. Since TXUSRCLK is generated with a deterministic phase from the reference clock, this leads to have XCLK, TXUSRCLK and the reference clock running [*i.e.*, RXRECCLK] with a deterministic fixed phase." Ex. 1005, 197. This includes a non-zero fixed phase difference. Ex. 1003, ¶206.

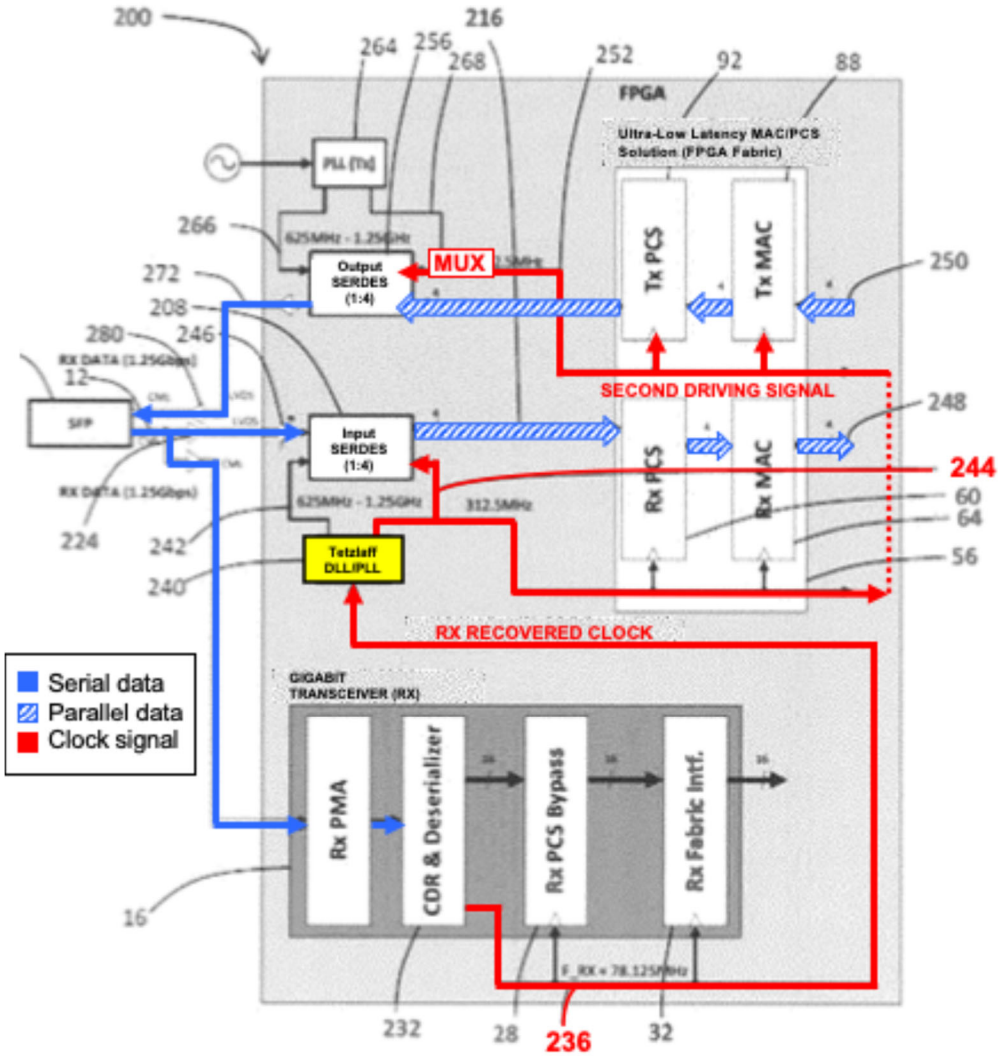
Tetzlaff discloses that the phase shift in the DLL is capable of dynamically compensating for delays with "one of 256 possible phase shifts," and may provide "a selectable quantized delay" of phase. Ex. 1006, 10:59–64.

The combination of Giordano and Tetzlaff would therefore be able to generate a TXUSRCLK signal that has the same frequency yet different phase from RXRECCLK. The combined system therefore renders obvious this limitation. Ex. 1003, ¶207.

B. Ground 2: Claims 1–12 Are Rendered Obvious by Raymond in View of Tetzlaff

1. Overview

The image below, modifying Figure 2 of Raymond in light of teachings from Tetzlaff, depicts the proposed combination:



Raymond's FPGA includes a preprogrammed, fixed transceiver block (RX) (bottom dark box) surrounded by a programmable FPGA (light dark box).

The proposed combination replaces Raymond's receiver-side PLL 240 with Tetzlaff's DLL/PLL (in yellow), which generates the clock signal (second driving signal 244) for both deserializer (Input SERDES) and serializer (Output SERDES). The combination further uses a multiplexer ("MUX") to allow the Output SERDES to select between clocks generated by Tetzlaff's DLL/PLL and Raymond's

transmitter-side PLL 264. Ex. 1003, ¶210. Tetzlaff teaches using a MUX to select an output clock among multiple input clocks. Ex. 1006, Fig. 1B, 6:33–37. Using the FPGA's programmable logic, mirroring how Raymond discloses programming SERDES blocks and wiring its own disclosures, a POSITA would have found it obvious to route the transmitter-side clock from Tetzlaff's DLL/PLL rather than Raymond's PLL 264. Ex. 1007, 8:64–9:8, 11:57–67; Ex. 1003, ¶210.

a. Motivation to Combine Raymond and Tetzlaff

Raymond emphasizes the importance of minimizing latency in communication devices, particularly for financial trading. Ex. 1007 at 1:18–38. Raymond recognizes that higher clock rates reduce latency but also notes that this requires adding a distinct (faster) clock, and additional clock conversions introduce unwanted latency. *Id*., 8:40–50.

A POSITA therefore would have recognized Tetzlaff's DLL/PLL architecture as a solution for synthesizing clocks while maintaining phase alignment and filtering jitter. *Supra*, Section VI.A.1.a.; Ex. 1006 at 4:21–27; Ex. 1003, ¶213.

Raymond repeatedly discusses implementing its invention with Xilinx UltraScale GTY transceivers. Ex. 1007 at 5:48–56, 6:3–8, 8:18–28, 8:51–55. Tetzlaff, a Xilinx patent, also expressly incorporates Xilinx transceivers by reference. Ex. 1006, 7:25–36. A POSITA working with Xilinx transceivers would naturally consult Xilinx materials such as Tetzlaff. Ex. 1003, ¶215.

Incorporating Tetzlaff's DLL/PLL teachings into Raymond would require only routine FPGA programming and configuration of existing transceiver resources. Ex. 1003, ¶217.

Raymond discloses implementing receiver and transmitter SERDES modules and related circuitry using a programmable FPGA. Ex. 1007 at 8:64–9:8 (describing receiving SERDES modules as "being implemented using programmable logic"), 11:57–67; Ex. 1003, ¶218. Implementing Tetzlaff's DLL/PLL in the FPGA Fabric thus represents a straightforward extension of techniques already used in Raymond. Ex. 1003, ¶218.

Such FPGA hardware programming is how the '587 patent suggests implementing its claimed invention. *Supra*, Section VI.A.1.a.

A POSITA would have had a reasonable expectation of success in combining Tetzlaff with Raymond because FPGAs use programmable logic and clock-management resources configurable for desired functions, which could be configured to implement Tetzlaff's DLL/PLL at necessary points in Raymond's clock path. Ex. 1007, 8:64–9:8, 11:57–67; Ex. 1006, 1:23–48; Ex. 1003, ¶218.

2. Analysis

a. Independent Claim 1

[1.pre]: A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:

To the extent limiting, Raymond discloses [1.pre]. Ex. 1003, ¶219.

Raymond discloses "low-latency serializer/de-serializer modules," which disclose this limitation. Ex. 1007, 4:43–51; Ex. 1003, ¶219; *infra*, [1.b] and [1.i] (discussing Raymond's disclosure of first and second serial data streams).

[1.a]: (a) receiving, by a deserializer in a field programmable array, a clock signal;

Raymond's transceiver 16 and Input SERDES 208 together disclose the claimed "deserializer," both of which receive an incoming physical layer serial signal 12. Ex. 1007, 8:64–9:8, 10:34–44. Raymond's CDR 232 recovers a clock signal from this physical layer serial signal 12, and as such this signal comprises the claimed "clock signal." Ex. 1007, 9:52–57, 10:34–44; Ex. 1003, ¶221.

[1.b]: (b) receiving, by the deserializer, the first serial data stream;

Raymond discloses that both transceiver 16 and Input SERDES 208 receive an incoming physical layer serial signal 12, which discloses the claimed "first serial data stream." Ex. 1007, 8:64–9:8, 9:25–28; Ex. 1003, ¶222.

[1.c]: (c) generating, by the deserializer, a receiver side clock signal;

Raymond's recovered clock 236 discloses the claimed "receiver side clock signal." Ex. 1003, ¶223.

Raymond includes a clock recovery module 232 that recovers a synchronizing clock signal from the incoming electrical physical layer serial signal 12 and outputs a recovered clock signal 236. Ex. 1007, 9:52–57, 10:34–44.

[1.d]: (d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;

As discussed in [1.a] and [1.b], Raymond's transceiver 16 and Input SERDES 208 disclose the claimed "deserializer," and the incoming physical layer serial signal 12 discloses "first serial data stream."

Raymond's parallel signal 216, which becomes the incoming data-link layer parallel signal 248, discloses the "first plurality of parallel data streams." Ex. 1003, ¶224.

Raymond's Input SERDES 208 performs deserialization of the incoming electrical physical layer serial signal 12 to output an incoming electrical physical layer parallel signal 216. Ex. 1007, 8:64–9:8. The incoming electrical physical layer parallel signal 216 discloses the claimed "first plurality of parallel data streams." Ex. 1003, ¶225.

[1.e]: (e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;

Raymond's FPGA fabric 56 discloses the claimed "computational circuitry." Ex. 1003, ¶227.

The incoming electrical physical layer parallel signal 216 "is received at the FPGA fabric 56 and processed by the receiving-side PCS module 60 and the receiving-side MAC module 64." Ex. 1007, 11:31–36. The FPGA fabric 56—including the PCS module 60 and MAC module 64—comprises the claimed

"computational circuitry." Ex. 1003, ¶227. The signal may be "further received and processed at a downstream computing unit implementing application-specific algorithms (*e.g.*, electronic trading algorithms)" which "may be implemented within the FPGA fabric 56." Ex. 1007, 7:19–27.

[1.f]: (f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;

Raymond in combination with Tetzlaff renders obvious this limitation. Ex. 1003, ¶228.

Tetzlaff's DLL/PLL discloses the claimed "phase lock loop." Ex. 1003, ¶229.

Raymond discloses that the recovered clock signal 236 (the receiver side clock signal) is fed from the clock recovery module 232 to the receiving-side PLL 240. Ex. 1007, 9:52–66. In the combination of Raymond and Tetzlaff, Tetzlaff's DLL/PLL replaces PLL 240. A POSITA would have understood that clock signal 236 is transmitted to Tetzlaff's DLL/PLL in the proposed combination. Ex. 1003, ¶229.

[1.g]: (g) generating, using the phase lock loop, a transmitter side clock signal;

Raymond in combination with Tetzlaff renders obvious this limitation. Ex. 1003, ¶230.

Tetzlaff's DLL/PLL results in a clock output, which discloses the claimed "transmitter side clock signal."

In the combination of Raymond and Tetzlaff, Tetzlaff's DLL/PLL generates the transmitter-side clock signal from the recovered clock signal 236, and this second driving signal 244 drives Raymond's Output SERDES 256, Tx MAC 88, and Tx PCS 92. Ex. 1003, ¶231.

[1.h]: (h) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams;

Raymond's outgoing parallel signal 252 discloses the claimed "second plurality of parallel data streams." Ex. 1003, ¶233.

The FPGA fabric 56 performs multiple operations on the incoming parallel data. For example, Raymond discloses that data on the transmitting side includes "an outgoing data link layer signal 250 that has been outputted after logical processing (*e.g.*, applying financial trading algorithms)" and "[a] transmitting side PCS module 92 converts the data link layer signal to an outgoing electrical physical layer parallel output signal 252." Ex. 1007, 11:57–63. The applying of financial trading algorithms in Raymond discloses the claimed "set of operations." Ex. 1003, ¶233.

[1.i]: (i) converting the second plurality of parallel data streams, by a serializer, into a second serial data stream; and

As discussed in [1.h], Raymond's outgoing parallel signal 252 discloses the "second plurality of parallel data streams."

Raymond's Output SERDES 256 discloses the claimed "serializer," and the outgoing electrical physical layer serial signal 272 discloses the "second serial data stream." Ex. 1003, ¶235.

The outgoing electrical physical layer parallel signal 252 "is serialized by a transmitting side SerDes module 256 operating in serialization mode." Ex. 1007, 11:63–65. The transmitting-side SerDes module 256 "may output an outgoing electrical physical layer serial signal 272." *Id.*, 11:38–39.

[1.j]: (j) transmitting, from the field programmable gate array system, the second serial data stream,

The outgoing electrical physical layer serial signal 272 output ("second serial data stream") by the Output SERDES 256 "may be converted at transmitting-side converter 280, prior to being received at the SFP 8." Ex. 1007, 11:38–41. The transmission from the FPGA through converter 280 to SFP 8 discloses this limitation. Ex. 1003, ¶236.

[1.k]: wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

Raymond in combination with Tetzlaff renders obvious this limitation. Ex. 1003, ¶237.

In the combination of Raymond and Tetzlaff, the transmitter-side clock is synthesized by Tetzlaff's PLL / DLL from the RX recovered clock signal 236 rather than from an independent clock source. This means the Input SERDES 208 and

Output SERDES 256 operate in a single, phase-coherent clock domain derived from the same recovered clock, eliminating the need for clock domain crossing circuitry between the receiver and transmitter paths. Ex. 1003, ¶237.

Raymond teaches that the "receiving-side driving signals and the transmitting-side driving signals have the same clock frequencies." Ex. 1007, 2:29–31, cl. 6; 12:17–21 ("the transmitting-side phase lock loop 264 may output driving signals 266, 268 having the same clock frequencies as the receiving-side driving signals 242, 244").

Tetzlaff's PLL / DLL feedback architecture ensures phase alignment between the source clock (the recovered clock 236) and the target clocks distributed to the transmitter, because the DLL "align[s] a phase of a feedback clock, which is based on one of the target clocks, to the phase of the source clock." Ex. 1006, cl. 1; 10:15–23. This feedback-based phase alignment ensures that the transmitter operates in phase with the receiver, eliminating the need for elastic buffers or FIFO-based clock domain crossing that would otherwise be required. Ex. 1003, ¶239.

Because the entire data path—from de-serialization through computational processing to serialization—is driven by clocks derived from the single recovered clock signal 236 through Tetzlaff's DLL/PLL, the combined system renders obvious this limitation. Ex. 1003, ¶240.

b. Claim 2

[2]: The method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the set of operations are associated with a trading algorithm.

Raymond expressly identifies electronic trading as a primary application for its ultra-low latency communication device, and describes the incoming and outgoing data streams in terms that correspond directly to market data and order entry data. For example, Raymond discloses incoming and outgoing serial data streams in the context of "financial trading data," which are transmitted to and from "financial exchange." Ex. 1007, 4:52–65.

Indeed, Raymond discloses "market data feed handler" and "market data feed distribution systems" applications, disclosing receiving market data. Ex. 1007, 13:61–64; Ex. 1003, ¶242. Raymond further discloses that the outgoing data link layer signal 250 is "outputted after logical processing (*e.g.*, applying financial trading algorithms)," hence disclosing sending out financial order related data and operations associated with trading algorithms. *Id.* at 11:57–60; Ex. 1003, ¶242.

c. Claim 3

[3]: The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.

As discussed in claim 2, Raymond discloses receiving market data and transmitting the results of applying financial trading algorithms, hence disclosing this limitation. Ex. 1003, ¶243.

d. Claim 4

[4]: The method of claim 1, wherein the set of operations includes at least one of the following:

(i) an arithmetic operation;

(ii) a logical operation;

(iii) a pipeline operation; and

(iv) a memory access operation.

As discussed above in [1.h], Raymond's logical processing (*e.g.*, applying financial trading algorithms) discloses the claimed "set of operations."

Raymond's application of financial trading algorithms involves arithmetic operations, hence discloses this limitation. Ex. 1007, 11:57–60; Ex. 1003, ¶244.

Tetzlaff further discloses this limitation. Section VI.A.2.b (Ground 1, cl. 4).

e. Claims 5–7

[5]: The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed prior to step (g).

[6]: The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed after step (g).

[7]: The method of claim 1, wherein all of the set of operations performed in step (h) are performed after step (g).

Claims 5–7 are directed to the order between step (g) (*i.e.*, generating transmitter side clock) and step (h) (*i.e.*, performing computational operations). The combination of Raymond and Tetzlaff discloses this limitation. Ex. 1003, ¶245. In the combined system, certain receiving-side operations within the computational

circuitry begin processing the incoming parallel data streams before the transmitting-side PLL has generated the transmitter side clock signal.

Raymond discloses that clock recovery and de-serialization on the receiving side operate in parallel: "The recovery of the synchronizing clock signal by the clock recovery module 232 may be carried out in parallel with the de-serialization of the incoming electrical physical layer serial signal 12 by the SerDes module 208." Ex. 1007, 10:7–10. Raymond further discloses that receiving-side operations—PCS decoding, MAC processing, and initial algorithmic processing—are driven by the receiving-side clock and begin as soon as de-serialized data is available. Ex. 1007, 7:19–27; Ex. 1003, ¶246.

Because the two steps may occur in "parallel," a POSITA would have found it obvious to perform the computations in step (h) prior to, during, or after the transmitter-side clock generation of step (g). Ex. 1003, ¶247.

f. Claim 8

Tetzlaff discloses claim 8. Section VI.A.2.d (Ground 1, cl. 8).

g. Claim 9

[9]: The method of claim 1, wherein the first plurality of parallel data streams has the same number of data streams as the second plurality of parallel data streams.

Raymond discloses that "the transmitting-side SerDes module 256 can have the same serialization ratio as the de-serialization ratio of the receiving side SerDes

module 240." Ex. 1007, 12:23–25. The same ratio results in the same parallel data streams, hence rendering this limitation obvious. Ex. 1003, ¶249.

h. Claim 10

[10]: The method of claim 1, wherein the first plurality of data streams and the second plurality of data streams comprise one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

Raymond discloses that "the UltraScale™ GTY from Xilinx™ has internal data buses of 16, 20, 32, 40 or 64 bits, with a minimum bit-width of 16 bits and a minimum de-serialization ratio of 1:16." Ex. 1007, 6:5–8. A POSITA would have understood that the SerDes module 208 could be configured to apply any of these de-serialization ratios depending on the application requirements, and that the serialization ratio of SerDes module 256 would match. Ex. 1003, ¶250.

i. Claim 11

[11]: The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and phase.

Raymond in combination with Tetzlaff renders obvious this limitation. Ex. 1003, ¶251. As discussed in claim 1, in the combination of Raymond and Tetzlaff, recovered clock signal 236 discloses the receiver side clock signal, and the clock output from Tetzlaff's DLL/PLL discloses the transmitter side clock signal.

As to frequency alignment, Raymond discloses that "the receiving-side driving signals and the transmitting-side driving signals have the ***same clock frequencies***." Ex. 1007, 2:29–31, 12:17–25. Raymond further confirms that "transmitting-side phase lock loop 264 may output driving signals 266, 268 having the same clock frequencies as the receiving-side driving signals 242, 244 outputted from the receiving-side phase lock loop 240." *Id*., 12:17–22.

As to phase alignment, Tetzlaff discloses how DLLs may use a delay line to control the phase difference between two signals, including making the two "synchronized." Ex. 1006, 2:26–41, 2:49–55. In addition, Tetzlaff discloses that "PLL acts to maintain a selectable phase offset between the synthesized clock and the reference clock." Ex. 1006, 10:24–33. This includes "phase shifting the synthesized clock" to "match the phase of the feedback." *Id*., 10:55–59.

The combination of Raymond and Tetzlaff would therefore be able to generate a transmitter signal that has the same frequency and phase as the recovered clock signal 236, rendering obvious this limitation. Ex. 1003, ¶254.

j. Claim 12

[12]: The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and different phases.

Raymond in combination with Tetzlaff renders obvious this limitation. Ex. 1003, ¶255. As discussed in claim 11, Raymond discloses that "the receiving-side

driving signals and the transmitting-side driving signals have the ***same clock frequencies.***" Ex. 1007, 2:29–31, 12:17–25.

Raymond expressly discloses an embodiment in which the receiving-side and transmitting-side driving signals are non-synchronized—*i.e.*, have different phases. Ex. 1003, ¶256. Raymond teaches "the receiving-side driving signals are non-synchronized with the transmitting-side driving signals." Ex. 1007, cl. 10; *id*., 12:9–13 ("the transmitting-side phase lock loop 264 can be non-synchronized with the clock signals of the receiving-side phase lock loop 240"). Non-synchronized signals operating at the same frequency necessarily have different phases. Ex. 1003, ¶256.

Tetzlaff independently teaches a mechanism for maintaining a controlled phase offset between the synthesized clock and the reference clock. Tetzlaff teaches that "the PLL acts to maintain a selectable phase offset between the synthesized clock and the reference clock." Ex. 1006, 10:24–33. Tetzlaff further teaches that "[t]he selectable phase offset may be used in addition to or instead of the phase adjustment provided by the DLL 308." *Id*., 10:31–33. A POSITA could configure Tetzlaff's PLL to synthesize a transmitter side clock signal that has the same frequency as the receiver side clock signal but a controlled, different phase. Ex. 1003, ¶257.

C. Ground 3: Claims 1–12 Are Rendered Obvious by Giordano in View of Tetzlaff further in View of Raymond

1. Overview

This proposes using the Giordano and Tetzlaff combination of Ground 1 and further implementing components for financial trading context explicitly disclosed in Raymond.

a. Motivation to Combine Giordano, Tetzlaff, and Raymond

Raymond emphasizes the importance of minimizing latency in communication devices, particularly for financial exchange. Ex. 1007, 1:18–38; Section VI.B.1.a (Motivation to Combine Raymond and Tetzlaff). A POSITA reading Raymond would therefore have recognized that Giordano in view of Tetzlaff offers a solution for synthesizing clock signals at the required frequencies while managing phase alignment and filtering jitter—precisely the clock distribution challenges Raymond identifies. Ex. 1003, ¶262.

A POSITA would have recognized Giordano in view of Tetzlaff as an attractive solution for the PLL functionality depicted in Raymond's system, and would have been motivated to look to Giordano and Tetzlaff to combine with Raymond. Sections VI.A.1.a and VI.B.1.a.

A POSITA would have had a reasonable expectation of success in combining Giordano, Tetzlaff, and Raymond. A POSITA would have recognized that the FPGA's programmable logic and on-chip clock management resources could be

configured to implement the teachings of the three references as needed. Ex. 1003, ¶264.

2. Analysis

a. Claims 1, 4–12

Giordano in view of Tetzlaff renders obvious claims 1, 4–12. Section VI.A.2 (Ground 1, Analysis).

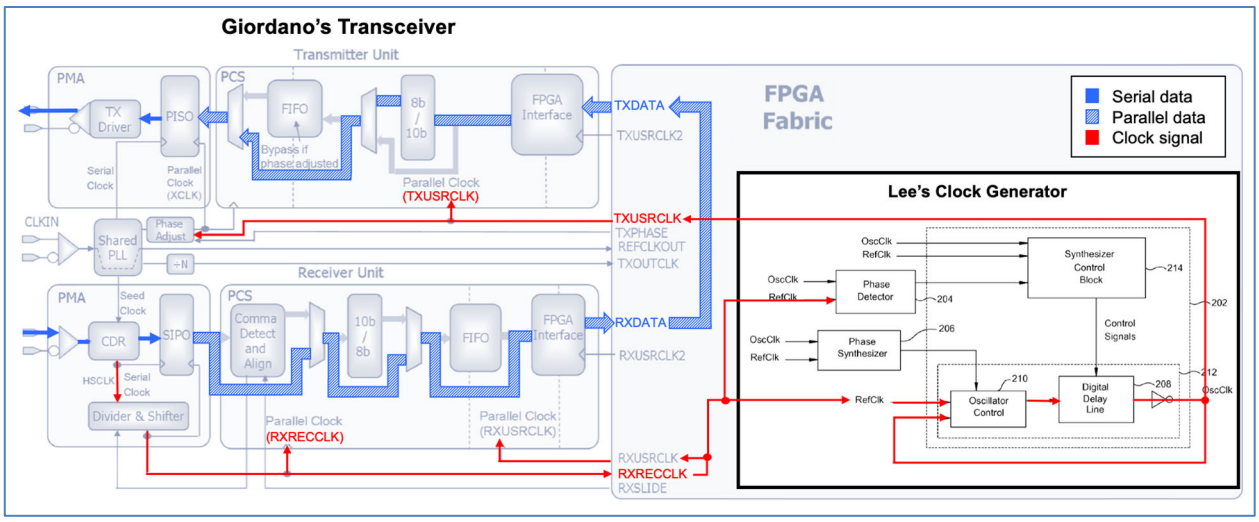
b. Claims 2–3

Raymond discloses claims 2–3. Sections VI.B.2.b–VI.B.2.c (Ground 2, cls. 2–3).

D. Ground 4: Claims 1, 4–12 Are Rendered Obvious by Giordano in View of Lee

1. Overview

The proposed combination is to program Giordano's FPGA Fabric to implement Lee's Clock Generator, as seen below (based on Giordano Figure 1 and Lee Figure 2):



Giordano's GTP transceiver generates a receiver side clock signal, RXRECCLK, from a clock extracted from incoming serial data, and provides RXRECCLK to Lee's Clock Generator implemented in the FPGA Fabric. Ex. 1003, ¶268. The Clock Generator creates a transmitter side clock signal TXUSRCLK that is phase-matched to RXRECCLK and sent to the transmitter of the GTP transceiver. Ex. 1003, ¶268.

a. Motivation to Combine Giordano and Lee

As discussed in Ground 1, Giordano recognizes that a jitter-filtering PLL is beneficial to condition the recovered receiver clock to serve as a transmitter reference clock. Ex. 1005, 198.

Lee discusses solutions for achieving "low output jitter of the frequency aligned mode along with the low phase error of the phase aligned mode." Ex. 1008, 2:35–55. Lee discloses a clock generator that filters jitter and phase matches the output to the input reference clock. Ex. 1008, 2:35–51, Fig. 2.

A POSITA therefore would have recognized Lee's clock generator as a solution for synthesizing clocks while maintaining phase alignment and filtering jitter. Ex. 1003, ¶270.

As with Tetzlaff, a POSITA reading Giordano would have naturally consulted Xilinx's own materials, including Lee, a Xilinx patent within the same Xilinx FPGA infrastructure. Ex. 1005, 194, 197–199; Ex. 1008, Cover.

Incorporating Lee's Clock Generator into Giordano would require only routine FPGA programming and configuration of existing transceiver resources. Ex. 1003, ¶271.

Lee discusses implementing its clock-generating teachings "using components that are all digital." Ex. 1008, 2:35–37, 4:31–35. A POSITA would have understood this to support implementing Lee's teachings on programmable logic, such as on Giordano's FPGA Fabric. Ex. 1003, ¶271.

Such FPGA hardware programming is how the '587 patent suggests implementing its claimed invention. *Supra*, Section VI.A.1.a.

A POSITA would have had a reasonable expectation of success for the same reasons discussed for the Giordano-Tetzlaff combination. *Supra*, Section VI.A.1.a. Because both Giordano and Lee rely on the same Xilinx FPGA infrastructure, and Lee's phase-matching elements can be implemented through routine programming of Giordano's FPGA Fabric, there would have been high expectations that the combination functions as intended. Ex. 1005, 195, 197; Ex. 1003, ¶272.

2. Analysis

a. Independent Claim 1

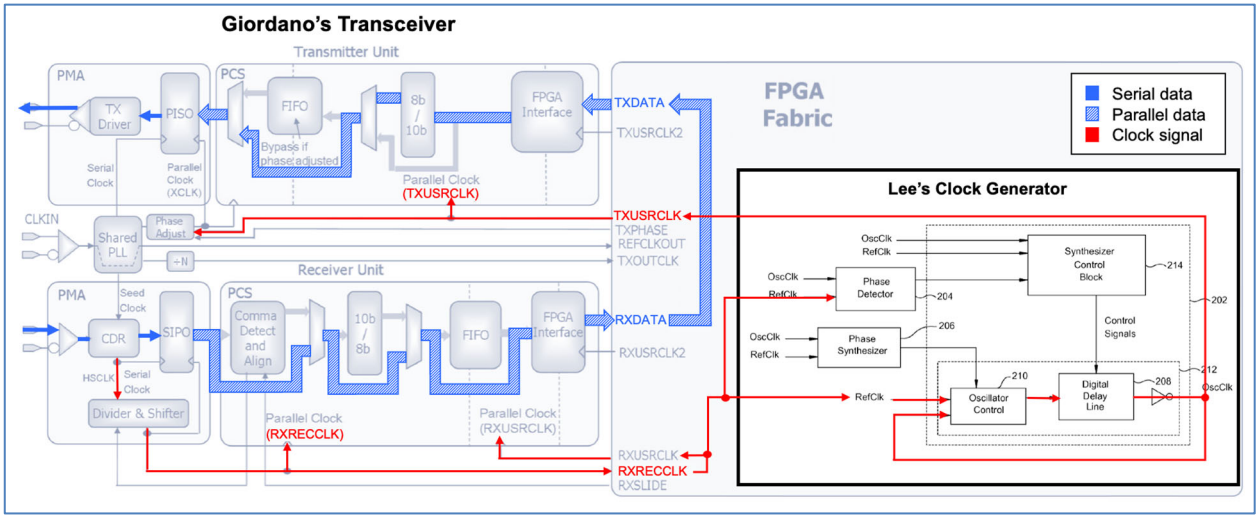
[1.pre] through [1.e]:

Giordano discloses these limitations. Section VI.A.2.a (Ground 1, cl. 1), [1.pre]–[1.e].

[1.f]: (f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;

Giordano in view of Lee renders obvious this limitation. Ex. 1003, ¶274. As discussed in [1.a] and [1.c], the Receiver Unit PMA in Giordano discloses the claimed "deserializer," and the recovered clock signal RXRECCLK from the PMA block discloses "receiver side clock signal."

Lee's Clock Generator programmed in Giordano's FPGA Fabric discloses the claimed "phase lock loop" of the '587 patent. Ex. 1003, ¶275. The combination of Giordano and Lee is depicted in the annotated image below:



Giordano discloses that the recovered RXRECCLK (*i.e.*, "receiver side clock signal") is provided to the FPGA Fabric. Ex. 1005, 195; Ex. 1008, Fig. 2; Ex. 1003, ¶275. A POSITA would have understood this RXRECCLK is transmitted to blocks implemented within the FPGA Fabric, including Lee's Clock Generator. Ex. 1003, ¶275.

A POSITA would have known how to implement Lee's Clock Generator in Giordano's FPGA Fabric. *Supra*, VI.D.1.a (Motivation to Combine Giordano and Lee).

While Giordano already phase-aligns the receiver side clock RXRECCLK and transmitter clock TXUSRCLK (as a result of modifying the receiver side clock), Giordano acknowledges that further jitter cleaning would be necessary to use this receiver side clock RXRECCLK for the transmitter. Ex. 1005, 198; Ex. 1003, ¶276. Lee's teachings provide the solution for this further jitter cleaning. Ex. 1003, ¶276.

In the combination of Giordano and Lee, Giordano's FPGA Fabric is programmed to create a clock signal path from the receiver clock RXRECCLK to the transmitter clock TXUSRCLK, where Lee's jitter-filtering and phase-alignment Clock Generator is inserted between the two clocks. Ex. 1003, ¶277. Giordano's RXRECCLK (*i.e.*, "receiver side clock signal") is transmitted to Lee's Clock Generator. Ex. 1003, ¶277. This generator outputs TXUSRCLK (*i.e.*, "transmitter side clock signal"), which is looped back as input to the Clock Generator for phase matching. Ex. 1003, ¶277. This results in synthesizing a clean transmitter side clock phase matched with the receiver side clock. Ex. 1005, 198; Ex. 1003, ¶277.

[1.g]: (g) generating, using the phase lock loop, a transmitter side clock signal;

Giordano in view of Lee renders obvious this limitation. Ex. 1003, ¶278. The output of Lee's Clock Generator ("phase lock loop") results in a "transmitter side clock signal" TXUSRCLK. Ex. 1003, ¶278.

[1.h] through [1.k]:

Giordano discloses these limitations. Section VI.A.2.a (Ground 1, cl. 1), [1.h]–[1.k].

b. Claims 4–7

Giordano discloses these claims. Section VI.A.2.b–VI.A.2.c (Ground 1, cls. 4–7).

c. Claim 8

[8.pre]: 8. The method of claim 1, wherein step (g) further comprises:

[8.a]: (k) generating, by the phase lock loop, a feedback clock signal associated with the transmitter side clock signal by performing the following steps until a first output of a phase detector of the field programmable gate array system is below a first threshold level:

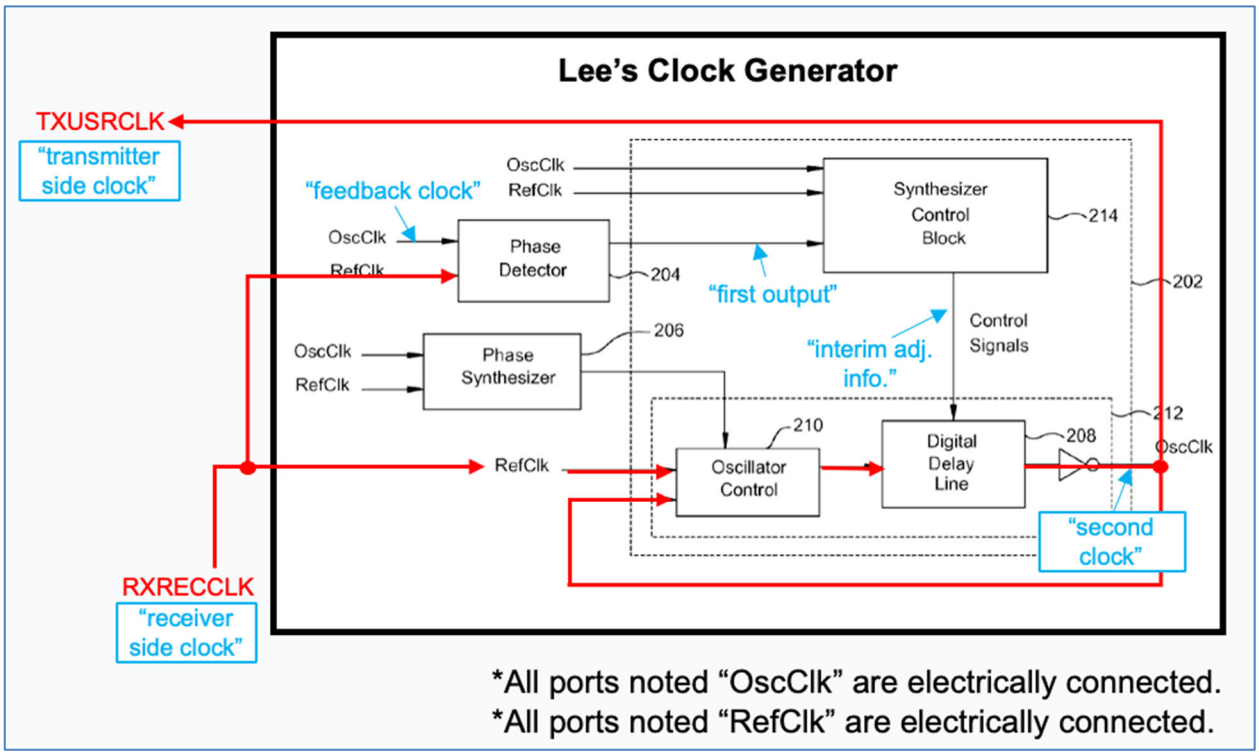
As discussed in [1.f] and [1.g], Lee's Clock Generator discloses the claimed "phase lock loop," which generates the "transmitter side clock signal" TXUSRCLK.

Lee's Phase Detector 204 discloses the claimed "phase detector," and the OscClk input of Phase Detector 204 discloses the "feedback clock signal." Ex. 1003, ¶282. This feedback clock signal is connected to the "transmitter side clock signal"

TXUSRCLK and hence is "associated with" TXUSRCLK (*i.e.*, "transmitter side clock signal").

Lee's Phase Detector 204 compares its two input signals and provides a signal to the Synthesizer Control Block 214 for adjusting the generated clock. Ex. 1008, 3:16–31. This signal to the Synthesizer Control Block 214 discloses the claimed "first output." Ex. 1003, ¶282.

Lee further discloses an iterative process until the two input clocks are aligned (Ex. 1008, 1:30–35, 3:16–24), through the feedback loop depicted in the annotated image below (based on Lee Figure 2):



Ex. 1003, ¶283. A POSITA would have understood the repeated steps to achieve this alignment to disclose this limitation. *Id.*

[8.b]: (1) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal;

Lee's Digital Delay Line 208 discloses the claimed "adjustable oscillator." Ex. 1003, ¶284. Lee's Digital Delay Line 208 output OscClk discloses the claimed "second clock signal." *Id*.

Lee discloses that Digital Delay Line 208 can modify the frequency and phase of the output signal OscClk. Ex. 1008, 2:56–3:24; Ex. 1003, ¶284.

This mirrors the '587 patent, which notes that "the adjustable oscillator [] may be implemented with a digital delay line." Ex. 1001, 39:7–9.

[8.c]: (2) generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal;

As discussed in [8.a] and [8.b], Lee's Phase Detector 204 discloses the claimed "phase detector," its OscClk input discloses the "feedback clock signal," and the signal into Synthesizer Control Block 214 discloses the "first output."

Lee's Phase Detector 204 compares its two input signals (*i.e.*, "feedback clock signal" and "receiver side clock signal") and provides a signal to the Synthesizer Control Block 214 for adjusting the generated clock. Ex. 1008, 3:16–31. This signal to the Synthesizer Control Block 214 discloses the claimed "first output." Ex. 1003, ¶285. The relationships between the aforementioned signals disclose this limitation. *Id*.

[8.d]: (3) transmitting, from the phase detector to a phase controller of the field programmable gate array system, the first output;

As discussed in [8.a] and [8.c], Lee's Phase Detector 204 discloses the claimed "phase detector," and the signal from the Phase Detector 204 into Synthesizer Control Block 214 discloses the "first output."

Lee's Synthesizer Control Block 214 discloses the claimed "phase controller." Ex. 1003, ¶286.

Lee discloses Phase Detector 204 sending a control signal based on the measured phase difference between two signals to Synthesizer Control Block 214. Ex. 1008, 3:16–31; Ex. 1003, ¶286.

[8.e]: (4) determining, by the phase controller, interim adjustment information based on the first output; and

The output of Lee's Synthesizer Control Block 214 ("phase controller") discloses the claimed "interim adjustment information." Ex. 1003, ¶287.

Lee discloses Synthesizer Control Block 214 providing control signals to Digital Delay Line 208 for modifying the output clock signal, disclosing this limitation. Ex. 1008, 3:16–31; Ex. 1003, ¶287. Lee discloses multiple variations of Synthesizer Control Blocks, each disclosing how that block may generate said control signals. *E.g.*, Ex. 1008, Figs. 3–5; Ex. 1003, ¶287.

[8.f]: (5) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information;

As discussed in [8.b], [8.c], and [8.e], Lee's Digital Delay Line 208 discloses the "adjustable oscillator," Synthesizer Control Block 214 discloses the "phase controller," and its output discloses "interim adjustment information."

Lee discloses Synthesizer Control Block 214 sending control signals to Digital Delay Line 208. Ex. 1008, Fig. 2.

[8.g]: wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information,

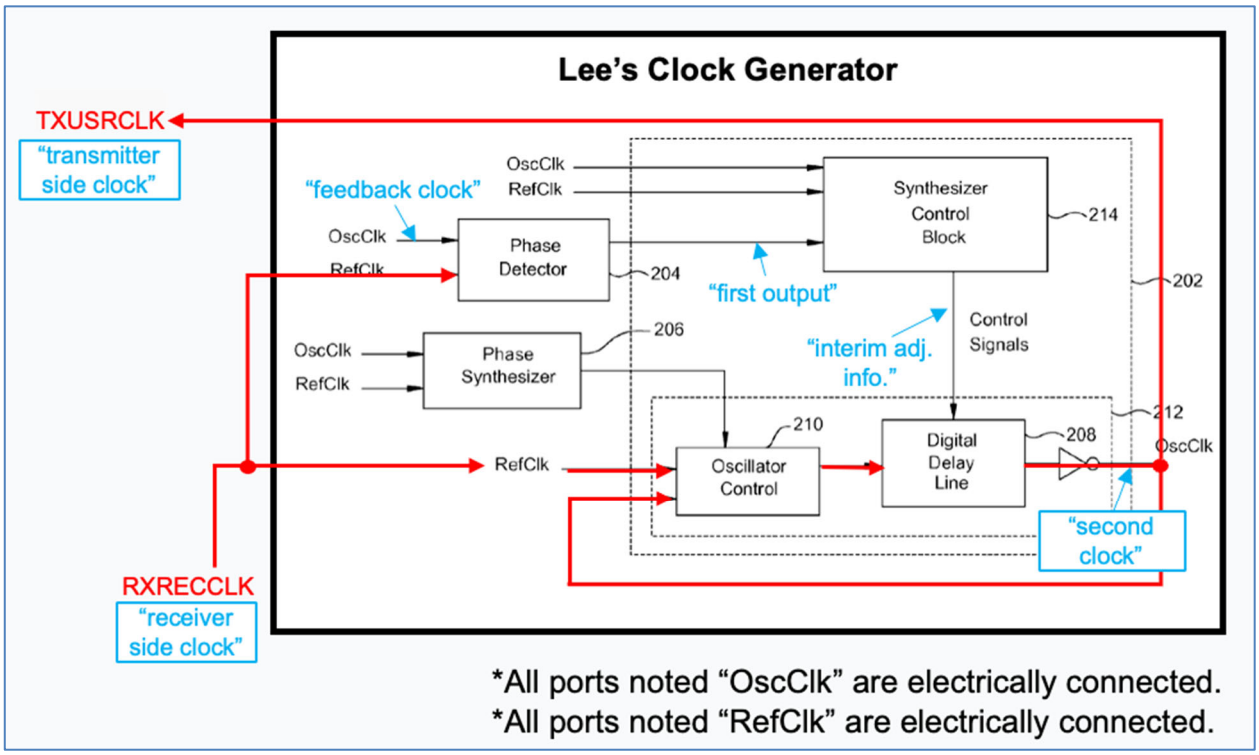
As discussed in [8.b] and [8.e], Lee's Digital Delay Line 208 discloses the "adjustable oscillator," its output discloses the "second clock signal," and Synthesizer Control Block 214 output discloses "interim adjustment information."

Lee discloses that Digital Delay Line 208 can modify the frequency and phase of the output signal OscClk based on the control signal from the Synthesizer Control Block 214. Ex. 1008, 2:56–3:24; Ex. 1003, ¶289.

[8.h]: wherein steps (1) through (5) are repeated until the first output of the phase detector is below the first threshold level, and

Lee's Phase Detector 204 ("phase detector") compares its two input signals and provides a signal ("first output") to the Synthesizer Control Block 214 for adjusting the generated clock. Ex. 1008, 3:16–31; Ex. 1003, ¶290.

Lee further discloses an iterative process until the two input clocks are aligned (Ex. 1008, 1:30–35, 3:16–24), through the feedback loop depicted in the annotated image below (based on Lee Figure 2):



Ex. 1003, ¶290. A POSITA would have understood the repeated steps to achieve this alignment to disclose this limitation. Ex. 1003, ¶290.

[8.i]: wherein the transmitter side clock signal is associated with the second clock signal.

Lee's Digital Delay Line 208 output OscClk ("second clock signal") is connected to the "transmitter side clock signal" TXUSRCLK and hence is "associated with" TXUSRCLK (*i.e.*, "transmitter side clock signal"). Ex. 1003, ¶291.

d. Claims 9–12

Giordano discloses these claims. Sections VI.A.2.e–VI.A.2.h (Ground 1, cls. 9–12).

E. Ground 5: Claims 1–12 Are Rendered Obvious by Giordano in View of Lee further in View of Raymond

1. Overview

This proposes using the Giordano and Lee combination of Ground 4 and further implementing components for financial trading context explicitly disclosed in Raymond.

a. Motivation to Combine Giordano, Lee, and Raymond

Motivation to combine Giordano and Lee is detailed in Ground 4. Section VI.D.1 (Ground 4, Overview).

A POSITA would have been motivated to look to Raymond to combine with Giordano and Lee, for the same reasons to combine Raymond with Giordano and Tetzlaff. Section VI.C (Ground 3, Overview).

2. Analysis

a. Claims 1, 4–12

Giordano in view of Lee renders obvious claims 1, 4–12. Section VI.D.2 (Ground 4, Analysis).

b. Claims 2–3

Raymond discloses claims 2–3. Sections VI.B.2.b–VI.B.2.c (Ground 2, cls. 2–3).

F. Ground 6: Claims 1, 4–12 Are Rendered Obvious by Giordano in View of Tetzlaff further in View of Virtex-UG

1. Overview

This proposes using the Giordano and Tetzlaff combination of Ground 1 and modifying the transceiver and FPGA configurations as necessary based on the teachings of Virtex-UG.

a. Motivation to Combine Giordano, Tetzlaff, and Virtex-UG

While Giordano already inherently discloses and incorporates Virtex-UG, if necessary, a POSITA would have been motivated to look to Virtex-UG to combine with Giordano and Tetzlaff. Giordano repeatedly references the Xilinx RocketIO GTP Transceiver User Guide, and Tetzlaff (a Xilinx patent) expressly incorporates that same guide by reference. Ex. 1005, 194, 197–199; Ex. 1006, 7:25–36. Virtex-UG details how to use, configure, and modify the Virtex-5 FPGA "RocketIO" GTP transceiver. *See generally* Ex. 1009; Ex. 1003, ¶303.

A POSITA reading Virtex-UG would therefore have recognized that its teachings would be helpful in the use, configuration, and modification of the FPGA system based on Giordano in view of Tetzlaff, including for synthesizing clock signals at the required frequencies while managing phase alignment and filtering jitter. Section VI.A.1.a (Motivation to Combine Giordano and Tetzlaff); Ex. 1003, ¶213.

A POSITA would have had a reasonable expectation of success in combining Giordano, Tetzlaff, and Virtex-UG. A POSITA would have recognized that the FPGA's programmable logic and on-chip clock management resources could be configured to implement the teachings of the three references as needed. Ex. 1003, ¶305. Because all references suggest implementations with Xilinx transceiver infrastructure, a POSITA would have had a high expectation that the combination would function as intended. Section VI.A.1.a (Motivation to Combine Giordano and Tetzlaff); Ex. 1003, ¶218.

2. Analysis

a. Claims 1, 4–12

Giordano in view of Tetzlaff and Virtex-UG renders obvious these claims. Section VI.A.2 (Ground 1, Analysis).

G. Ground 7: Claims 1, 4–12 Are Rendered Obvious by Giordano in View of Lee further in View of Virtex-UG

1. Overview

This proposes using the Giordano and Lee combination of Ground 4 and modifying the transceiver and FPGA configurations as necessary based on the teachings of Virtex-UG.

a. Motivation to Combine Giordano, Lee, and Virtex-UG

Motivation to combine Giordano and Lee is detailed in Ground 4. Section VI.D.1 (Ground 4, Overview).

A POSITA would have been motivated to look to Virtex-UG to combine with Giordano and Lee, for the same reasons to combine Virtex-UG with Giordano and Tetzlaff. Section VI.F.1 (Ground 6, Overview).

2. Analysis

a. Claims 1, 4–12

Giordano in view of Lee and Virtex-UG renders obvious these claims. Section VI.D.2 (Ground 4, Analysis).

H. Ground 8: Claims 1–12 Are Rendered Obvious by Giordano in View of Tetzlaff, Virtex-UG, and Raymond

1. Overview

This proposes using the Giordano, Tetzlaff, and Virtex-UG combination of Ground 6 and modifying the FPGA for financial trading applications explicitly disclosed in Raymond.

a. Motivation to Combine Giordano, Tetzlaff, Virtex-UG, and Raymond

Motivations to combine Giordano, Tetzlaff, and Virtex-UG are detailed in Ground 6. Section VI.F.1 (Ground 6, Overview).

A POSITA would have been motivated to look to Raymond to combine with Giordano, Tetzlaff, and Virtex-UG, for the same reasons to combine Raymond with Giordano and Tetzlaff. Section VI.C.1 (Ground 3, Overview).

2. Analysis

a. Claims 1, 4–12

Giordano in view of Tetzlaff and Virtex-UG renders obvious claims 1, 4–12. Section VI.F.2 (Ground 6, Analysis).

b. Claims 2–3

Raymond discloses claims 2–3. Sections VI.B.2.b–VI.B.2.c (Ground 2, cls. 2–3).

I. Ground 9: Claims 1–12 Are Rendered Obvious by Giordano in View of Lee, Virtex-UG, and Raymond

1. Overview

This proposes using the Giordano, Lee, and Virtex-UG combination of Ground 7 and modifying the FPGA for financial trading applications explicitly disclosed in Raymond.

a. Motivation to Combine Giordano, Lee, Virtex-UG, and Raymond

Motivations to combine Giordano, Lee, and Virtex-UG are detailed in Ground 7. Section VI.G.1 (Ground 7, Overview).

A POSITA would have been motivated to look to Raymond to combine with Giordano, Lee, and Virtex-UG, for the same reasons to combine Raymond with Giordano and Lee. Section VI.E.1 (Ground 5, Overview).

2. Analysis

a. Claims 1, 4–12

Giordano in view of Lee and Virtex-UG renders obvious claims 1, 4–12. Section VI.G.2 (Ground 7, Analysis).

b. Claims 2–3

Raymond discloses claims 2–3. Sections VI.B.2.b–VI.B.2.c (Ground 2, cls. 2–3).

VII. CONCLUSION

Petitioners have established a reasonable likelihood that the Challenged Claims are unpatentable. Petitioners therefore respectfully request that IPR be instituted.

DATED: August 3, 2026

Respectfully Submitted,

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CERTIFICATION UNDER 37 C.F.R. §42.24(d)

Under the provisions of 37 C.F.R. §42.24(d), the undersigned attorney hereby certifies that the word count for Sections I–VII of the foregoing Petition for *Inter Partes* Review is 13,940, according to the word count tool in Microsoft Word.

DATED: August 3, 2026

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CERTIFICATE OF SERVICE

The undersigned certifies service pursuant to 37 C.F.R. §§42.6(e) and 42.105(b) on the Patent Owner electronically on the Patent Owner at the following email addresses:

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APPENDIX: CHALLENGED CLAIM LISTING

No.	Limitation
[1.pre]	A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:
[1.a]	receiving, by a deserializer in a field programmable array, a clock signal;
[1.b]	receiving, by the deserializer, the first serial data stream;
[1.c]	generating, by the deserializer, a receiver side clock signal;
[1.d]	converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;
[1.e]	transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;
[1.f]	transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;
[1.g]	generating, using the phase lock loop, a transmitter side clock signal;
[1.h]	performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams;
[1.i]	converting the second plurality of parallel data streams, by a serializer, into a second serial data stream; and
[1.j]	transmitting, from the field programmable gate array system, the second serial data stream,
[1.k]	wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.
[2]	The method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the set of operations are associated with a trading algorithm.
[3]	The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.

No.	Limitation
[4]	The method of claim 1, wherein the set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.
[5]	The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed prior to step (g).
[6]	The method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed after step (g).
[7]	The method of claim 1, wherein all of the set of operations performed in step (h) are performed after step (g).
[8.pre]	The method of claim 1, wherein step (g) further comprises:
[8.a]	(k) generating, by the phase lock loop, a feedback clock signal associated with the transmitter side clock signal by performing the following steps until a first output of a phase detector of the field programmable gate array system is below a first threshold level:
[8.b]	(1) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal;
[8.c]	(2) generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal;
[8.d]	(3) transmitting, from the phase detector to a phase controller of the field programmable gate array system, the first output;
[8.e]	(4) determining, by the phase controller, interim adjustment information based on the first output; and
[8.f]	(5) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information;
[8.g]	wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information,
[8.h]	wherein steps (1) through (5) are repeated until the first output of the phase detector is below the first threshold level, and

No.	Limitation
[8.i]	wherein the transmitter side clock signal is associated with the second clock signal.
[9]	The method of claim 1, wherein the first plurality of parallel data streams has the same number of data streams as the second plurality of parallel data streams.
[10]	The method of claim 1, wherein the first plurality of data streams and the second plurality of data streams comprise one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.
[11]	The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and phase.
[12]	The method of claim 1, wherein the transmitter side clock signal and the receiver side clock signal have the same frequency and different phases.