

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

OPTIVER US LLC and OPTIVER TRADING US LLC,

Petitioners

v.

HFT SOLUTIONS, LLC,

Patent Owner

Case No. IPR2026-00383

Patent No. 12,107,587

PATENT OWNER'S PRELIMINARY RESPONSE

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PATENT OWNER'S EXHIBIT LIST

No.	Description
Ex. 2001	<i>HFT Solutions, LLC, v. Optiver US LLC et al</i> , Case No. 7:25-cv-00415, Dkt. 1 (Sept. 8, 2025, W.D. Tex)
Ex. 2002	Optiver reports strong financial results for 2024, available at https://www.optiver.com/insights/news/optiver-reports-strong-financial-results-for-2024/

I. INTRODUCTION

The present Petition fails to establish a reasonable likelihood of success on the merits for numerous reasons. First, the Petition’s primary reference for all but one ground expressly includes a clock domain crossing circuit, contravening limitation 1.k. Second, the Petition does not actually offer any basis to combine the two references supporting the remaining ground, merely stating two technical aspects of each reference without relating the two in any way.

Because the Petition makes only a token effort to address these fatal issues, the Petition cannot succeed and justifies denial of institution. Together, they make it clear there is no likelihood of success on the merits. Because the Petition does not present any grounds that can be instituted, much less any that present a reasonable likelihood of success, institution should be denied.

II. BACKGROUND

A. Optiver’s Petition

Petitioner Optiver US LLC and Optiver Trading US LLC (“Optiver” or “Petitioner”) challenges claims 1–12 of U.S. Patent No. 12,107,587 (the “’587 Patent”). Petitioner structures its asserted grounds for unpatentability as follows:

- Ground 1: Giordano and Tetzlaff Render Obvious Claims 1, 4-12
- Ground 2: Raymond and Tetzlaff Render Obvious Claims 1-12

- Ground 3: Giordano, Tetzlaff, and Raymond Render Obvious Claims 1-12
- Ground 4: Giordano and Lee Render Obvious Claims 1, 4-12
- Ground 5: Giordano, Lee, and Raymond Render Obvious Claims 1-12
- Ground 6: Giordano, Tetzlaff, and Virtex-UG Render Obvious Claims 1, 4-12
- Ground 7: Giordano, Lee, and Virtex-UG Render Obvious Claims 1, 4-12
- Ground 8: Giordano, Tetzlaff, Virtex-UG, and Raymond Render Obvious Claims 1-12
- Ground 9: Giordano, Lee, Virtex-UG, and Raymond Render Obvious Claims 1-12

Because all challenged dependent claims across all grounds depend from claim 1, this Preliminary Response need only address the Petition's arguments concerning claim 1. If the Petition does not show a reasonable likelihood of prevailing on claim 1, then it cannot prevail on any other challenged claim.

B. Overview of the '587 Patent

At a high level, the '587 Patent is directed to addressing a need for phase control to minimize latency in high-speed FPGA systems. Ex. 1001 at 1:29-34, Abstract. Latency reduction is important "in the financial industry in high frequency trading where the rapid processing of the FPGA is desired." *Id.* at 1:42-43. Contrary to the prior art method of using a clock domain crossing circuit to synchronize clock

signals, which adds delay, the invention teaches a technique that avoids clock domain crossings. *Id.* at 1:47-53.

In particular, the '587 Patent teaches utilizing a phase-locked loop to avoid the need for clock domain crossings. *Id.* 1:29-34. This solution is reflected, for example, in claim 1 of the '587 Patent, which recites:

1. A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:
 - (a) receiving, by a deserializer in a field programmable array, a clock signal;
 - (b) receiving, by the deserializer, the first serial data stream;
 - (c) generating, by the deserializer, a receiver side clock signal;
 - (d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;
 - (e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;
 - (f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system, the receiver side clock signal;
 - (g) generating, using the phase lock loop, a transmitter side clock signal;
 - (h) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams;

- (i) converting the second plurality of parallel data streams, by a serializer, into a second serial data stream; and
 - (j) transmitting, from the field programmable gate array system, the second serial data stream,
- wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

Ex. 1001 at claim 1.

All other challenged claims (2–12) depend from claim 1.

III. Level of Ordinary Skill in the Art

The Petition proposes that a person of ordinary skill in the art in the field of the '587 Patent “would have a bachelor’s degree in Computer Engineering, Electrical Engineering, or equivalent discipline, and at least three years of academic or industry experience relating to clocking techniques for FPGAs with high-speed transceivers.” Paper 1 (“Petition” or “Pet.”) at 6. For purposes of this preliminary response, Patent Owner does not challenge that definition.

IV. THE PETITION DOES NOT DEMONSTRATE A LIKELIHOOD OF SUCCESS ON THE MERITS

Eight of the Petitions grounds rely on a primary reference that expressly discloses a clock domain crossing in contradiction to limitation 1.k. While the Petition concedes this crossing violates the limitation, it is unable to navigate its express inclusion under any theory. The remaining ground fails because its combination is expressly based in hindsight bias offering no reason but the patents own teachings that a POSITA would combine its two references at all, much less in

the manner proposed by the Petition. Because the Petition presents no ground likely to invalidate any claim, institution should be denied.

A. Giordano Uses A Clock Domain Crossing Operation That Delays Processing Of the First Set of Parallel Data Streams

Giordano expressly teaches a clock domain crossing in a manner excluded by limitation 1.k. This crossing cannot be removed, indeed the user manual Optiver cites explains why. Limitation 1.k specifically prohibits the use of a clock domain crossing operation that delays processing the first set of parallel data streams. But Optiver focuses its analysis on removing only one of two clock domain crossings. When attempting to remove the other, Optiver references the wrong user manual which is not prior art and ultimately explains the propose combination is not feasible.

As all claims rely upon claim 1 and each of grounds 1 and 3-9 rely on Giordano in this same way for this limitation¹, they all fail.

1. Giordano Teaches A Clock Domain Crossing

Optiver's analysis of Giordano itself is insufficient to meet this limitation. Optiver focuses on bypassing a First In First Out (FIFO) buffer in the transmitter of Giordano. *See* Paper 1 at 23. But Giordano still teaches the same FIFO buffer on its receiver which processing the data flow.

¹ While Grounds 6-9 presents Virtex-UG as an obviousness reference, they do not present any new argument for why its inclusion would be obvious or at all motivated. *See* Paper 1 at 70-71 (providing no motivation to bypass a receiver side FIFO).

Indeed, the “first set of parallel data streams” does not bypass the receiver side FIFO buffer. This adds delay to the data flow being processed. Giordano’s Figure 1 clearly shows data flowing from the SIPO (the “first set of parallel data streams”) passes through a FIFO buffer before continuing to a FPGA Interface and the FPGA Fabric. Ex. 1005 at 195. Indeed, Section II of Giordano explains data is transmitted from the SIPO (serial in to parallel out) to the Comma Detect and Align block and the data “is then 10b to 8b decoded, if needed, and transferred to a FIFO (also called elastic buffer) in order to enter the RXUSRCLK domain.” *Id.* This is in stark contrast to what Giordano provides regarding the transmitter side FIFO where it explains “[i]n some configurations XCLK and TXUSRCLK have the same frequency and a constant phase offset” so the FIFO may be bypassed. *Id.* Giordano offers no means to bypass the receiver side FIFO. Giordano’s Table 1 confirms this distinction, describing the transmitter FIFO as “bypassed” and thus only having a 4 ns latency or delay, as compared with the receiver side FIFO with 20 ns of latency or delay. *Id.* at 198. As such, Giordano has a FIFO to cross clock domains that adds a 20ns delay to the “first set of parallel data streams” prior to it being processed. This does not meet limitation 1.k.

2. Virtex-UG Does Not Remove the Clock Domain Crossing

The Petition’s reference to Virtex-UG does not rescue Optiver’s failed analysis. Tellingly, while Optiver’s analysis of Giordano ignores its receiver side

FIFO, the analysis of Virtex-UG recognizes the receiver side FIFO violates limitation 1.k. However, the analysis of Virtex-UG offers no basis to bypass Giordano's receiver side FIFO. Such a change to Giordano is not obvious, inherent, express, or even feasible. For these multiple reasons, Virtex-UG does not render this bypass obvious or inherent.

a. Bypassing the Receiver Side FIFO is Not Inherent To Giordano

First, Virtex-UG is not inherent to Giordano. While the Petition states the correct standard, "whether a feature, while not explicitly discussed, is necessarily present in a reference," Paper 1 at 14 citing *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1328 (Fed. Cir. 2001), the Petition cannot show bypassing Giordano's receiver side FIFO is necessarily present. Optiver argues "Giordano presents a system with the 'RocketIO' GTP transceiver of the Xilinx Virtex-5 FPGA family" and notes Giordano follows the procedures of Virtex-UG "for activating the alignment circuit." Paper 1 at 14. But this bears no relation to the cited feature of Virtex-UG, bypassing a receiver side FIFO. Virtex-UG itself provides bypassing this buffer "is an advanced feature" only operable "under certain system-level conditions and data rates." Ex. 1009 at 177. There is no reason an "advanced feature" would necessarily be present in Giordano's presentation of the RocketIO GTP transceiver. Especially when, as noted above, Giordano expressly does not bypass the receiver FIFO.

b. Giordano Does Not Incorporate Ex. 1009

Second, Virtex-UG's teachings are not express in Giordano. Giordano does not incorporate Ex. 1009 by reference. Ex. 1009 is cited by neither Giordano nor Tetzlaff and is not even prior art.

The only place a user manual² is referenced is in a footnote citation. But a footnote citation to a user manual, is not an incorporation by reference. *See Commonwealth Sci. & Indus. Rsch. Organisation v. Buffalo Tech. (USA), Inc.*, 542 F.3d 1363, 1372 (Fed. Cir. 2008) (explaining “[t]he footnote citation in [the host document] could provide justification for combining the reference for obviousness³ purposes, but there is nothing about the reference [] that appears to constitute an incorporation of any or all of the information from the [] reference under the standard set forth in *Advanced Display Systems*.”). Indeed, here Giordano makes only passing reference to two user manuals, a Virtex-5 user manual and an Evaluation Platform User Guide used for testing. Ex. 1005 at 199, 201. Those passing reference never address all of Ex. 1009 or bypassing a reference side buffer. Rather, they reference “[t]he architecture we present in this paper” and “the procedure we follow for activating the alignment circuit.” *Id.* at 194, 197. But passing references that do no

² As explained below, the reference is not even to Ex. 1009.

³ While the Petition mentions it would be obvious to implement Virtex-UG's teachings, “including for synthesizing clock signals at the required frequencies while managing phase alignment and filtering jitter,” there is no motivation directed to bypassing a FIFO buffer in Giordano. *See* Paper 1 at 70; Ex. 1003 at ¶159.

even mention the portion relied upon by the presenting party do not incorporate the reference material. *See Apple Inc. v. Int'l Trade Comm'n*, 725 F.3d 1356, 1362-63 (Fed. Cir. 2013). Giordano only references user manuals for the portions it uses and does not bypass its receiver side FIFO, thus such a technique is not available under incorporation by reference.

Moreover, Ex. 1009 is not cited by Giordano or Tetzlaff. Giordano cites “Virtex-5 FPGA RocketIO GTP Transceiver USER Guide Xilinx, UG196, v. 1.7, 2008.” Ex. 1005 at 201. Ex. 1009 is version 2.1 and has a date on its face of December 3, 2009. Ex. 1009. Ex. 1009 is an entire version and year later than what Giordano cites and the relevant portions regarding TX Buffering and RX Elastic Buffering cited by the Petition were extensively revised and revised in version 2.1. *See* Ex. 1009 at 6. Likewise, Tetzlaff cites an even early version UG204 Dec. 9, 2004. Ex. 1006 at 7:29-31. Because Optiver’s entire basis for alleging Ex. 1009 is inherent or express to Giordano is Giordano’s citation to a different user manual, Ex. 1009 is clearly neither express nor inherent. Similarly, it is not obvious to rely on an entirely user manual than cited in the reference.

c. Ex. 1009 Is Not Prior Art

Further still, Optiver fails to establish Ex. 1009 is even prior art. As Ex. 1009 is not a patent or patent application, the Petition must show that it was publicly available, i.e., that it was “disseminated or otherwise made available to the extent

that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it.” *Kyocera Wireless Corp. v. Int’l Trade Comm’n*, 545 F.3d 1340, 1350 (Fed.Cir.2008). “[T]he burden is on the petitioner to identify with particularity evidence sufficient to establish a reasonable likelihood that the reference was publicly accessible before the critical date of the challenged patent, and therefore that there is a reasonable likelihood that it qualifies as a printed publication.” *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 16 (PTAB Dec. 20, 2019) (precedential). Neither the Petition nor its expert declarations do this.

First, the Petition itself only suggest “Virtex-UG was published on December 3, 2009” and then concludes it qualifies as prior art. Paper 1 at 4. But a publishing date, particularly one supported only by assumption and hearsay, does not establish public availability. That requires dissemination and availability to the correct audience. The Petition never so much as states Ex. 1009 was ever available to public, much less showing such. Without even that much, Optiver cannot show Ex. 1009 is prior art.

Second, Dr. Gardner who is cited only for the notion that Ex. 1009 was published on December 3, 2009, similarly fails to show public availability. While Dr. Gardner declares Ex. 1009 authentic this has nothing to do with public availability. *See* Ex. 1004 at ¶¶41-46. Similarly, paragraph 47, the only portion of

her declaration relating to publication, fails to demonstrate public availability. Dr. Gardner merely reads a date from the user manual and assumes public accessibility based on “standard practice for technology companies.” *Id.* at ¶47. But that date is hearsay and is routinely rejected as a basis for dating documents. *See e.g. ServiceNow, Inc. v. Hewlett-Packard Co.*, Case IPR2015- 00716, slip op. at 17 (PTAB Aug. 26, 2015) (Paper 13) (finding a copyright notice unreliable hearsay for purposes of establishing the date of a printed publication); *Navico Inc. v. Garmin Int'l, Inc.*, No. 216CV00190JRGRSP, 2017 WL 3750252, at *3 (E.D. Tex. July 28, 2017), *report and recommendation adopted*, No. 216CV00190JRGRSP, 2017 WL 3764213 (E.D. Tex. Aug. 29, 2017) (copyright and revision dates insufficient to show date of distribution); *Finjan, Inc. v. Sophos, Inc.*, No. 14-CV-01197-WHO, 2016 WL 2988834, at *26 (N.D. Cal. May 24, 2016) (copyright date and screen shot from decades later showing “Published/distributed” in 1995 insufficient to show date of distribution). Moreover, Dr. Gardner offers no basis for the alleged “standard practice for technology companies to add the release date to User Manuals.” *See Ex. 1004* at ¶47. Her declaration identifies no experience with “technology companies” or their practices regarding user manuals. At best, she notes she has assisted engineers in finding technical materials, but finding technical materials has little to do with establishing when or how they are made available or to whom as the legal standard requires. Because the declaration “authenticates” the wrong user manual

and offers no reliable basis for when or if it was publicly accessible, the Petition cannot show Ex. 1009 is prior art. Because every ground referencing Giordano relies on Ex. 1009 to suggest bypassing the receiver side FIFO, all such grounds fail.

d. The Proposed Combination Violates the Teachings of Ex. 1009

Last, the proposed revision of Giordano according to Ex. 1009 expressly violates Ex. 1009. Ex. 1009 expressly provides either FIFO buffer can only be bypassed “under certain system-level conditions and data rates.” *See* Ex. 1009 at 177. As the Petition acknowledges “RXUSRCLK must be driven directly from RXRECCLK using a BUFR regional clock buffer.” *Id.* But the Petition’s proposed arrangement does not include a BUFR regional clock buffer, instead the RXUSRCLK is RXRECCLK, not driven from it. *See* Paper 1 at 10-11. Indeed, a similar requirement is in place for bypassing the transmit side that “[w]hen the buffer is bypassed, TXUSRCLK must be driven directly from REFCLKOUT using a BUFR regional clock buffer...” Ex. 1009 at 116. But the Petition proposes TXUSRCLK be driven by Tetzlaff’s DLL/PLL from RXRECCLK. Paper 1 at 11; *see also id.* at 61 (providing a similar arrangement of clocks in combination with Lee where TXUSRCLK is driven by Lee’s Clock Generator from RXRECCLK not a BUFR). In short, the proposed combination, while attempting to overcome the RX FIFO in Giordano, breaks his invention’s bypassing of the TX FIFO. As the Petition’s proposed combination of Giordano and Tetzlaff violates the teaching of

what it alleges to be the relevant user manual, a POSITA would not find a combination of the three obvious and would not support bypassing any FIFO

Giordano's express teachings violate limitation 1.k by including a FIFO buffer on the receiver side. Giordano does not rely on Ex. 1009 or any version of that user guide to necessarily require bypassing the FIFO buffer it expressly includes. Moreover, there is no teaching or reason a POSITA would have been motivated to remove the FIFO buffer from Giordano based on Ex. 1009, not the least because it is not prior art. Lastly, the teachings of Ex. 1009 show that the petition's design cannot function as claimed. Because each of Ground 1 and 3-9 rely on Giordano and Virtex-UG in the same way, *see* Paper 1 at 23-25, 58, 63, 69, 71-74, each ground fails.

B. Ground 2 Is Based Entirely on Hindsight

Optiver has no basis whatsoever to add any teachings of Tetzlaff to Raymond. Optiver's apparent guiding motivation, that "clock conversions introduce unwanted latency," finds no solution in Tetzlaff. Nor does reference to a manufacturer motivate any change to Raymond, not the least the key change of putting Tetzlaff's DLL/PLL in the FPGA fabric. Optiver expressly finds that motivation by reviewing '587 Patent, expressly roadmapping. Because this combination is motivated exclusively by hindsight bias, it cannot show any claim is obvious.

1. Optiver's Motivation To Combine Has No Technical Basis

Optiver observes Raymond notes while higher frequency reduces latency it also requires additional clock conversions and “additional clock conversions introduce unwanted latency” and “Tetzlaff’s DLL/PLL architecture [i]s a solution for synthesizing clocks while maintaining phase alignment and filtering jitter.” Paper 1 at 43. But Optiver never connects these concepts to show why the fact that clock conversion introduce latency or higher frequency desires would lead a POSITA to want Tetzlaff’s technique for maintaining phase alignment and filtering jitter⁴. Nor does Optiver’s expert, who simply repeats verbatim the petition. *See* Ex. 1003 at ¶213.

Such a failure to meet the Petition’s burden to provide a motivation to combine alone justifies disregarding the proposed combination. But even considering the alleged problem and Tetzlaff, a POSITA would not find any reason to combine Raymond and Tetzlaff. First, Raymond’s proposed embodiments are the solution to “additional clock conversions” leaving the POSITA no need to consider another solution. Second, Tetzlaff’s DLL/PLL architecture offers Raymond nothing

⁴ While Optiver cites back to its motivation to combine Giordano and Tetzlaff, Giordano expressly notes “the recovered clock might also require to be filtered in order to match the jitter specifications...” Paper 1 at 12. No such statement is made in Raymond and indeed, as noted *infra*, Raymond already teaches a PLL filtering the recovered clock.

new. Because the alleged problem of Raymond is solved in Raymond and Tetzlaff would not even address the solution, there is no motivation to combine.

Raymond explains latency in the PCS and MAC components can be reduced by using a faster clock but, in the prefabricated model provided by Xilinx, this requires an additional clock which mandates clock conversions that themselves add latency. *See* Ex. 1007 at 8:29-50. Specifically, Raymond notes increasing the clock frequency from 78.125 MHz to between 250 and 350 MHz would cut latency by 8 or 10 ns. *Id.* at 8:36-43. But Raymond does not merely leave this as an opportunity for later development, Raymond solves it. Raymond teaches how to increase the clock frequency of the PCS and MAC components into this desired range. The very next paragraph explains that Figure 2 shows “an improved ultra-low latency communication device.” *See id.* at 8:56-58; *see also id.* at 12:42-46. The most notable improvement in latency is the alternate SerDes taught by Raymond which allows a de-serialization ratio less than the minimum ratio of the prefabricated module. *Id.* at 12:66-13:12. This increases the clock driving the PCS and MAC components from 78.125MHz as in figure 1 to 312.5 MHz, a four times increase. *Id.* at 13:5-8. This is exactly what Raymond explains is desired at column 8 cited by Optiver. Because Raymond addresses the problem alleged by Optiver to motivate a combination with Tetzlaff, there is no motivation to include Tetzlaff

Even if there were a need in Raymond to reduce clock conversions or increase frequency, Tetzlaff offers nothing to meet that need. First and foremost, Raymond eliminated those needs by reducing the deserialization ratio and operating all serialized components on a single, higher frequency, clock. Second, the DLL/PLL architecture of Tetzlaff is not a tool for eliminating clock conversions or increasing frequency. Nothing in Tetzlaff or identified by Optiver or even Dr. Schaefer's declaration suggests Tetzlaff's architecture can be used to eliminate clock conversions, address their added latency, or to increased clock frequency mentioned in Raymond. Last, even considering "synthesizing clocks while maintaining phase alignment and filtering jitter" generally, Raymond has no need for Tetzlaff's architecture. Instead, Raymond implements its own phase alignment and jitter control architecture. Raymond teaches "the delay element 246 adjusts a phase of the electrical physical layer serial signal 12" to maintain phase alignment. Ex. 1007 at 10:4-6. This performs the role of Tetzlaff's DLL. Likewise, Raymond already controls jitter using its several PLLs including one to clean the recovered clock 236. *See id.* at Fig. 2. As Optiver can identify no reason to duplicate what Raymond already has, there is no motivation to add Tetzlaff in anyway, much less the way Optiver proposes.

2. Optiver's Combination Would Not Function

Next, while Optiver contends a POSITA would have “require[d] only routine FPGA programming” and would be “a straightforward extension of techniques already used in Raymond,” the combination is non-functional on its face.

In fact, the combination proposed by Optiver creates, without resolving, the very issue that the '587 Patent was intended to solve. Raymond's design assumes that PLL 264 delivers the clocks necessary for the transceiver's transmit operation. It provides phase-aligned clock signals 266 and 268, ensuring no need to cross between clock domains operating in different phases. But Optiver proposes providing non-phase-aligned clock signals 266 and 244, Ex. 1007 at 12:7-9 (PLL 264 is independent of the PLL replaced by Tetzlaff). This would not function. Indeed, Tetzlaff teaches such phase misalignment or skew “can cause sample data systems to malfunction.” Ex. 1006 at 2:17-18. To function the different clock domains of signals 244 and 266 would need to be crossed, adding delay, and violating limitation 1.k. Because, this failing is only glossed over, not addressed, the proposed combination of Raymond and Tetzlaff is not obvious.

Indeed, Optiver suggests that because Raymond mentions Xilinx it would be obvious to implement patents owned by Xilinx, like Tetzlaff. Paper 1 at 43. But this offers no explanation for what from Tetzlaff would be implemented or how. Rather it seems Optiver has offered an incomplete “obvious to try” argument. But such an

argument requires both “a design need or market pressure to solve a problem” and “a finite number of identified predictable solutions.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 402, 127 S. Ct. 1727, 1732, 167 L. Ed. 2d 705 (2007). But, while, as noted above, Optiver has identified a problem, Optiver has made no showing that Tetzlaff offers a solution. At best, it suggests that if a POSITA found an issue in Raymond relating to its reference to Xilinx, Xilinx materials may have been considered. But as explained above, Optiver does not show Tetzlaff would address the Raymond issue. Likewise, that incorporating Tetzlaff would only requires routing experience is irrelevant when there is no reason to make the incorporation.

Further, Optiver suggests because Raymond implements entirely different components “using a programmable FPGA” it is obvious to put Tetzlaff’s DLL/PLL in the FPGA Fabric. Paper 1 at 44. As with the clock conversion and phase alignment, these two concepts have nothing to do with each other. Raymond’s SERDES modules being implemented in a FPGA does not lead a POSITA to place DLLs or PLLs in the FPGA Fabric. Optiver offers no reasoning for placing one module in an FPGA generally motivates placing any other module in the FPGA Fabric specifically. Nor does Optiver’s expert. Ex. 1003 at ¶218 (explaining that a POSITA would have had a reasonable expectation of success in implementing Tetzlaff’s teaching to Raymond, not that anything in Raymond suggests a particular implementation of Tetzlaff). Instead, Optiver expressly invokes hindsight bias

explaining implementing clock circuitry by “FPGA hardware programming is how the ’587 patent suggests implementing its claimed invention.” Paper 1 at 44. Clearly, Optiver has used the ’587 patent as a roadmap to reach the combination of Raymond and Tetzlaff, that does not show the combination would be obvious.

Lastly, Optiver also provides no explanation for its particular implementation of Tetzlaff into Raymond. For example, in addition to inserting Tetzlaff’s DLL/PLL into Raymond, the Petition proposes reversing the direction of a portion of Raymond’s “output driving signal[] 268.” Raymond teaches PLL 264 outputs signal 268 to the FPGA, Ex. 1006 at 12:1-2, but the Petition breaks this clock signal with a MUX and has the FPGA signal driven from the opposite direction, Paper 1 at 42. The Petition offers no explanation for why a POSITA might make these changes, that they are obvious, or are even within the scope of a person’s skill in the art. *See id.* While Dr. Schaefer suggests Tetzlaff “teaches using a MUX to select an output clock among multiple input clocks,” he offers no basis for why Raymond’s PLL would be bypassed at all, much less in this way. No doubt this is because, as explained above, such an arrangement does not work. This does not prove obviousness.

Optiver fails to show the combination of Raymond and Tetzlaff is obvious. Optiver has no motivation to combine, just a problem unrelated to the alleged solution. Optiver’s other arguments are meritless without an underlying motivation

or are expressly based on hindsight. Because there is no basis to combine Raymond and Tetzlaff, much less in the manner proposed by Optiver, ground 2 fails.

V. CONCLUSION

Because of the failures noted above, Patent Owner respectfully asks the Director to find the Petition has failed to establish any likelihood of success on the merits and deny institution.

Date: September 8, 2026

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The undersigned hereby certifies that the above document was served on September 8, 2026 by filing this document through the Patent Trial and Appeal Case Tracking System (PTACTS) as well as delivering a copy via electronic mail upon the following attorneys of record for Petitioner:

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