



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/888,218	09/01/2020	10763865	05301-0009	2004

1912 7590 08/12/2020
AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Nima Badizadegan, New York, NY;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

1912 7590 07/16/2020
AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Keith J. Barkaus	(Typed or printed name)
/Keith J. Barkaus/	(Signature)
July 24, 2020	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/888,218	05/29/2020	Nima Badizadegan	05301-0009	2004

TITLE OF INVENTION: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$500	\$0.00	\$0.00	\$500	10/16/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
BURD, KEVIN MICHAEL	2632	375-219000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Amster, Rothstein & Ebenstein LLP

2

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 01-1785

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Keith J. Barkaus/ Date July 24, 2020
Typed or printed name Keith J. Barkaus Registration No. 51431

Electronic Patent Application Fee Transmittal

Application Number:	16888218			
Filing Date:	29-May-2020			
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP			
First Named Inventor/Applicant Name:	Nima Badizadegan			
Filer:	Keith J. Barkaus/Fabrina Brown			
Attorney Docket Number:	05301-0009			
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	2501	1	500	500

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				500

Electronic Acknowledgement Receipt

EFS ID:	40102730
Application Number:	16888218
International Application Number:	
Confirmation Number:	2004
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Fabrina Brown
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	05301-0009
Receipt Date:	24-JUL-2020
Filing Date:	29-MAY-2020
Time Stamp:	17:49:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 500
RAM confirmation Number	E20207NH49593768
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	1-05301-9IssueFeeTrans.pdf	97326	no	1
			feb2d2b789aff46cd05ba7c7176cfe465364f644		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30765	no	2
			05f421e56a53aa76a60e3a5dbb2cb79ca3dbaa67		
Warnings:					
Information:					
Total Files Size (in bytes):			128091		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

1912 7590 07/16/2020
AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

EXAMINER

BURD, KEVIN MICHAEL

ART UNIT

PAPER NUMBER

2632

DATE MAILED: 07/16/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/888,218	05/29/2020	Nima Badizadegan	05301-0009	2004

TITLE OF INVENTION: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$500	\$0.00	\$0.00	\$500	10/16/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

1912 7590 07/16/2020
AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/888,218	05/29/2020	Nima Badizadegan	05301-0009	2004

TITLE OF INVENTION: FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$500	\$0.00	\$0.00	\$500	10/16/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
BURD, KEVIN MICHAEL	2632	375-219000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/888,218	05/29/2020	Nima Badizadegan	05301-0009	2004
1912 7590 07/16/2020 AMSTER, ROTHSTEIN & EBENSTEIN LLP 90 PARK AVENUE NEW YORK, NY 10016			EXAMINER BURD, KEVIN MICHAEL	
			ART UNIT 2632	PAPER NUMBER
DATE MAILED: 07/16/2020				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/888,218	Applicant(s) Badizadegan, Nima	
	Examiner KEVIN M BURD	Art Unit 2632	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the terminal disclaimer filed 7/8/2020.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-4 and 6-22. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)	5. ☒ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ____.	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material ____.	7. ☐ Other ____.
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date ____.	

/KEVIN M BURD/ Primary Examiner, Art Unit 2632	
---	--

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

The terminal disclaimer has been received and approved on 7/8/2020.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Claim 1, line 49, the phrase "wherein wherein" is replaced with the term "wherein".

Claim 5 was not originally presented. The claims are renumbered due to claim 5 not being originally presented.

Conclusion

Claims 1-4 and 6-22 are allowed.

The following is an examiner's statement of reasons for allowance: Claim 1 recites " wherein the first set of operations does not include clock domain crossing

operations that delays processing of the first set of parallel data streams". Applicant's disclosed prior art, specifically figure 1, discloses the computational circuitry would include the FPGA core 106 which comprises receive-side computation block 110a, transmit-side computation block 110b. Each of these computations blocks are directly coupled to RX to TX clock domain crossing block 112. It is unclear how this computation circuit would function and function properly without block 112. Step (vi) recites transmitting, from the phase detector to a phase controller of the field programmable gate array system which is placed within the field programmable gate array, the first output. This transmitting step does not recite identical subject matter as step (vi) of application 16/672,076 since application 16/672,076 recites the phase controller is not in the field programmable gate array. Since the claims do not recite identical subject matter, a provisional statutory double patenting rejection is not appropriate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. BURD whose telephone number is (571)272-3008. The examiner can normally be reached on 9:30 - 5:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <https://ppair-my.uspto.gov/pair/PrivatePair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KEVIN M BURD/
Primary Examiner, Art Unit 2632
7/8/2020

<i>Examiner-Initiated Interview Summary</i>	Application No. 16/888,218	Applicant(s) Badizadegan, Nima		
	Examiner KEVIN M BURD	Art Unit 2632	AIA (First Inventor to File) Status Yes	Page 1 of 2

All participants (applicant, applicants representative, PTO personnel):

1. KEVIN M BURD (Primary Examiner); Telephonic
2. Keith Barkaus (Attorney of Record); Telephonic

Date of Interview: 07 July 2020

Claims Discussed: 1

Prior Art Discussed: Parent application 16/670,702. Copeniding application 16/672,076.

Issues Discussed:

Double Patenting:

The examiner contacted applicant's representative to notify him of potential provisonal non-statutory double patenting rejections for the claims in view of the parent application 16/670,702 and copending application 16/672,0769. The examiner asked applicant's representative if a terminal disclaimer could be filed to overcome the potential double patenting rejection so a notice of allowability could be issued or if a non-final office action should be mailed which would include the provisional non-statutory double patenting rejection. Applicant's representative indicated a terminal disclaimer would be filed in the next few days. Statutory double patenting issues were discussed. It was agreed that the location of the phase controller will alter the transmitting step (claim 1, step vi in the instant application and 16/672,076) and therefore the claims do not recite identical subject matter. Since claim 1 of the instant application and claims 1 and 12 of 16/672,076 do not recite identical subject matter, a provisional statutory double patenting rejection is not appropriate. A typo in step (I) will be corrected by examiner's amendment. The word "wherein" is recited twice. The second wherein will be deleted.

/KEVIN M BURD/ Primary Examiner, Art Unit 2632	
Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04 Please further see: MPEP 713.04 Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b) 37 CFR § 1.2 Business to be transacted in writing	

U.S. Patent and Trademark Office
PTOL-413/413b (Rev. 01/01/2015)

Interview Summary

Paper No. 20200702

Applicant recordation instructions:It is not necessary for applicant to provide a separate record of the substance of interview
.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

<i>Notice of References Cited</i>	Application/Control No. 16/888,218		Applicant(s)/Patent Under Reexamination Badizadegan, Nima	
	Examiner KEVIN M BURD		Art Unit 2632	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
	A					
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
*	U	US patent application 16/670,702 (Year: 2019)
*	V	US patent application 16/672,076 (Year: 2019)
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 16/888,218	Applicant(s)/Patent Under Reexamination Badizadegan, Nima
	Examiner KEVIN M BURD	Art Unit 2632

CPC - Searched*		
Symbol	Date	Examiner
H03L7/085	07/02/2020	KMB
G06F12/4291; 30/34; 1/08	07/02/2020	KMB
H04B1/403,40,50	07/02/2020	KMB
H03M9/00	07/02/2020	KMB

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
375	219	07/02/2020	KMB

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
inventor name search	07/02/2020	KMB
east search	07/02/2020	KMB

--	--

<i>Search Notes</i> 	Application/Control No. 16/888,218	Applicant(s)/Patent Under Reexamination Badizadegan, Nima
	Examiner KEVIN M BURD	Art Unit 2632

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
375	219	07/02/2020	KMB
H03L	7/085	07/02/2020	KMB
G06F	12/4291; 30/34; 1/08	07/02/2020	KMB
H04B	1/403,40,50	07/02/2020	KMB
H03M	9/00	07/02/2020	KMB

--	--

Issue Classification 	Application/Control No. 16/888,218	Applicant(s)/Patent Under Reexamination Badizadegan, Nima
	Examiner KEVIN M BURD	Art Unit 2632

CPC						
Symbol					Type	Version
H03L	/	7	/	085	F	2013-01-01
G06F	/	13	/	4291	I	2013-01-01
H03M	/	9	/	00	I	2013-01-01
H04B	/	1	/	40	I	2013-01-01
H03K	/	19	/	1774	I	2013-01-01

CPC Combination Sets					
Symbol				Type	Version
/	/	/	/		

NONE (Assistant Examiner) (Date)		Total Claims Allowed: 21	
/KEVIN M BURD/ Primary Examiner, Art Unit 2632 (Primary Examiner) (Date)		07 July 2020 (Date)	O.G. Print Claim(s) 1
			O.G. Print Figure 3A

Issue Classification 	Application/Control No. 16/888,218	Applicant(s)/Patent Under Reexamination Badizadegan, Nima
	Examiner KEVIN M BURD	Art Unit 2632

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H04L	/	7	/ 08
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
375	219

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	21	
/KEVIN M BURD/ Primary Examiner, Art Unit 2632 (Primary Examiner)	07 July 2020 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3A

Issue Classification 	Application/Control No. 16/888,218	Applicant(s)/Patent Under Reexamination Badizadegan, Nima
	Examiner KEVIN M BURD	Art Unit 2632

☐ Claims renumbered in the same order as presented by applicant
 ☐ CPA
 ☒ T.D.
 ☐ R.1.47

CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	11	19	20										
2	2	11	12	20	21										
3	3	12	13	21	22										
4	4	13	14												
5	6	14	15												
6	7	15	16												
7	8	16	17												
8	9	17	18												
9	10	18	19												

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 21	
/KEVIN M BURD/ Primary Examiner, Art Unit 2632 (Primary Examiner) _____ (Date) 07 July 2020		O.G. Print Claim(s) 1	O.G. Print Figure 3A

Bibliographic Data

Application No: 16/888,218

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged:

/KEVIN M BURD/

Examiner's Signature

Initials

Title:

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL
PHASE-LOCKED LOOP

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
05/29/2020	375	2632	05301-0009
RULE			

APPLICANTS

INVENTORS

Nima Badizadegan New York, NY, UNITED STATES

CONTINUING DATA

This application is a CON of 16670702 10/31/2019

16670702 has PRO of 62808404 02/21/2019

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

06/08/2020

**** SMALL ENTITY ****

STATE OR COUNTRY

UNITED STATES

ADDRESS

AMSTER, ROTHSTEIN & EBENSTEIN LLP

90 PARK AVENUE

NEW YORK, NY 10016

UNITED STATES

FILING FEE RECEIVED

\$3,155

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	16888219
Filing Date	2020-05-29
First Named Inventor	Nima Badizadegan
Art Unit	2632
Examiner Name	BURD, Kevin Michael
Attorney Docket Number	05301-0009

U.S.PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1	9330740	B1	2016-05-03	Baeckler et al.			
	2	9001951	B1	2015-04-07	Kumpulainen			
	3	10411720	B2	2019-09-10	Lenzen et al.			
	4	6675306	B1	2004-01-06	Baxter			
If you wish to add additional U.S. Patent citation information please click the Add button.							Add	
U.S.PATENT APPLICATION PUBLICATIONS							Remove	
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1	20190025413	A1	2019-01-24	Liu et al.			
If you wish to add additional U.S. Published Application citation information please click the Add button.							Add	
FOREIGN PATENT DOCUMENTS							Remove	
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²ⁱ	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T ⁵

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16888219
Filing Date	2020-05-29
First Named Inventor	Nima Badizadegan
Art Unit	2632
Examiner Name	BURD, Kevin Michael
Attorney Docket Number	05301-0009

1							
---	--	--	--	--	--	--	--

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	IEEE STANDARDS ASSOCIATION, "IEEE Standards for Ethernet," IEEE 802.3-2018, Section 4, Figure 52-4, page 634 (2018)	

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/KEVIN M BURD/	Date Considered	07/09/2020
--------------------	----------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16888219
Filing Date	2020-05-29
First Named Inventor	Nima Badizadegan
Art Unit	2632
Examiner Name	BURD, Kevin Michael
Attorney Docket Number	05301-0009

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Keith J. Barkaus/	Date (YYYY-MM-DD)	2020-07-08
Name/Print	Keith J. Barkaus	Registration Number	51,431

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	5	("10037568" "10169814" "4068188" "4745372" "8467418").PN.	US-PGPUB; USPAT	OR	OFF	2020/01/21 12:15
S2	17,366	serializ\$5 with deserializ\$	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:15
S3	0	S1 same pll	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:15
S4	0	S1 same phase near3 detect\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:15
S5	18,879	serializ\$5 same deserializ\$	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:15
S6	830	S2 same pll	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:15
S7	30	S6 same phase near3 detect\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:15
S8	0	(BADIZADEGAN near4 NIMA).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:23
S9	0	S2 same pphase adj detect\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:37
S10	100	S2 same phase adj detect\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:37
S11	0	S5 same tranceiver\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:42
S12	2,447	S5 same transceiver\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:42
S14	124,393	deserializ\$5 or (serial adj parallel)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:43

S16	135,860	serializ\$5 or (parallel adj serial)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:44
S17	28,947	S14 same S16	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:44
S18	2,935	S17 same transceiver\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:44
S19	30	S18 same phase near3 detect\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:45
S20	22	S19 not S7	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:45
S21	46,346	(transmit\$1 or transmission or tx) near2 clock\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:58
S22	171,245	(reception or receiv\$5 or RX) near2 clock\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:59
S23	4	S21 near4 S22 near4 input\$5 near4 phase near2 detect\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:59
S24	0	S23 and S17	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/21 13:59
S25	3	((("20130113534") or ("6987823") or ("7668524"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/01/28 10:57
S26	3	S25 and phase near3 detect\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:01
S27	46,389	(transmit\$1 or transmission or tx) near2 clock\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:04
S28	171,368	(reception or receiv\$5 or RX) near2 clock\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:04
S29	4	S27 near4 S28 near4 input\$5 near4 phase near2 detect\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:04
S30	18,906	serializ\$5 same deserializ\$	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:05

S31	0	S29 and S30	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:05
S32	17,392	serializ\$5 with deserializ\$	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:05
S33	832	S32 same pll	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:05
S34	30	S33 same phase near3 detect\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:05
S35	124,543	deserializ\$5 or (serial adj parallel)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:05
S36	136,017	serializ\$5 or (parallel adj serial)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:05
S37	28,981	S35 same S36	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:05
S38	2,938	S37 same transceiver\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:05
S39	30	S38 same phase near3 detect\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:05
S40	22	S39 not S34	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 11:05
S41	3	((("20130113534") or ("6987823") or ("7668524"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/01/28 13:16
S42	2	S41 and pll	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/01/28 13:16
S43	1	"7668524".pn.	US-PGPUB; USPAT	OR	OFF	2020/03/24 10:36
S44	1	"7668524".pn. and "210"	US-PGPUB; USPAT	OR	OFF	2020/03/24 11:25
S45	1	"7668524".pn.	US-PGPUB; USPAT	OR	OFF	2020/03/24 13:38
S46	1	"7668524".pn.	US-PGPUB; USPAT	OR	OFF	2020/04/20 10:48
S47	0	((("BADIZADEGAN") near3 ("Nima"))).INV.	US-PGPUB; USPAT; USOCR;	OR	OFF	2020/04/29 10:32

			EPO; JPO; DERWENT			
S48	7,398	375/219.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:36
S49	3,476	H03I7/085.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:36
S52	2,975	g06f13/4291.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:37
S53	3,008	g06f30/34.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:37
S54	4,767	g06f1/08.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:37
S55	2,267	H03M9/00.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:37
S56	9,500	H04b1/40.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:37
S57	681	H04b1/403.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:37
S58	897	H04b1/50.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:38
S59	34,008	S48 or S49 or S52 or S53 or S54 or S55 or S56 or S57 or S58	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:38
S60	126,684	deserializ\$5 or (serial adj parallel)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:38
S61	138,328	serializ\$5 or (parallel adj serial)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:38
S62	29,531	S60 same S61	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:38
S63	212	S62 same phase near3 detect\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:39

S64	28	S59 and S63	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:39
S65	1,666	clock near4 domain near4 crossing	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:41
S66	98	S59 and S65	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:41
S67	0	S66 and de-skew\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:42
S68	1	S66 and deskew\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:42
S69	509,568	fpga	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:43
S70	657,272	field near2 program\$6 near2 gate\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:43
S71	726,978	S69 or S70	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:43
S72	440	S71 and S65	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:43
S73	0	S72 and ppl	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:44
S74	122	S72 and pll	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:44
S75	115	S72 and phase near3 lock\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:44
S76	136	S74 or S75	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:44
S77	19	S70 and S63	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/04/29 10:48
S78	0	((("Badizadegan") near3 ("Nima"))).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/30 13:41

S79	7,402	375/219.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:43
S80	3,534	H03I7/085.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:43
S81	3,033	g06f13/4291.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:43
S82	3,100	g06f30/34.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:43
S83	4,843	g06f1/08.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:43
S84	2,290	H03M9/00.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:43
S85	9,763	H04b1/40.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:43
S86	693	H04b1/403.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:43
S87	914	H04b1/50.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:43
S88	34,597	S79 or S80 or S81 or S82 or S83 or S84 or S85 or S86 or S87	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:43
S89	128,287	deserializ\$5 or (serial adj parallel)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:48
S90	140,077	serializ\$5 or (parallel adj serial)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:48
S91	29,889	S89 same S90	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:48
S92	213	S91 same phase near3 detect\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:48
S93	28	S88 and S92	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:48

S94	128,287	deserializ\$5 or (serial adj parallel)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:55
S95	140,077	serializ\$5 or (parallel adj serial)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:55
S96	29,889	S94 same S95	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:55
S97	3,057	S96 same transceiver\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:55
S98	30	S97 same phase near3 detect\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:55
S99	5	S98 and fpga	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:56
S100	34,597	S79 or S80 or S81 or S82 or S83 or S84 or S85 or S86 or S87	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:56
S101	1,687	clock near4 domain near4 crossing	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:56
S102	99	S100 and S101	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:56
S103	1	S102 and deskew\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 13:56
S104	527,210	fpga	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 14:06
S105	679,794	field near2 program\$6 near2 gate\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 14:06
S106	751,145	S104 or S105	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 14:06
S107	445	S106 and S101	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 14:06
S108	123	S107 and pll	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 14:06

S109	116	S107 and phase near3 lock\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 14:06
S110	137	S108 or S109	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2020/06/30 14:06

7/2/2020 10:12:35 AM

C:\Users\kburd\Documents\EAST\Workspaces\16888218.wsp

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16888219
	Filing Date	2020-05-29
	First Named Inventor	Nima Badizadegan
	Art Unit	2632
	Examiner Name	BURD, Kevin Michael
	Attorney Docket Number	05301-0009

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	9330740	B1	2016-05-03	Baeckler et al.	
	2	9001951	B1	2015-04-07	Kumpulainen	
	3	10411720	B2	2019-09-10	Lenzen et al.	
	4	6675306	B1	2004-01-06	Baxter	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20190025413	A1	2019-01-24	Liu et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS								Remove
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²ⁱ	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T ⁵

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16888219
Filing Date	2020-05-29
First Named Inventor	Nima Badizadegan
Art Unit	2632
Examiner Name	BURD, Kevin Michael
Attorney Docket Number	05301-0009

1							
---	--	--	--	--	--	--	--

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	IEEE STANDARDS ASSOCIATION, "IEEE Standards for Ethernet," IEEE 802.3-2018, Section 4, Figure 52-4, page 634 (2018)	

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16888219
Filing Date	2020-05-29
First Named Inventor	Nima Badizadegan
Art Unit	2632
Examiner Name	BURD, Kevin Michael
Attorney Docket Number	05301-0009

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Keith J. Barkaus/	Date (YYYY-MM-DD)	2020-07-08
Name/Print	Keith J. Barkaus	Registration Number	51,431

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	39947985
Application Number:	16888218
International Application Number:	
Confirmation Number:	2004
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	05301-0009
Receipt Date:	08-JUL-2020
Filing Date:	29-MAY-2020
Time Stamp:	17:30:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	1-IDS.pdf	1034558	no	4
			9c8a506d059c38f76259aff5a877d976eb9e c0e2		

Warnings:

Information:					
2	Non Patent Literature	2-NPL-8023-2018-jitter.pdf	164763	no	1
			9799f5b926080567cc26b10f744cf85b2967889d		
Warnings:					
Information:					
Total Files Size (in bytes):			1199321		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed		PTO/SB/25 U.S. Patent and Trademark Office Department of Commerce	
Electronic Petition Request	TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION		
Application Number	16888218		
Filing Date	29-May-2020		
First Named Inventor	Nima Badizadegan		
Attorney Docket Number	05301-0009		
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP		
☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action ☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.			
Owner	Percent Interest		
Nima Badizadegan	100%		
The owner(s) of percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending reference Application Number(s)			
16670702 filed on 10/31/2019 16672076 filed on 11/01/2019 as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the reference application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said reference application, "as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application," in the event that any such patent granted on the pending reference application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.			
☒ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.			

☐ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.	
Applicant claims the following fee status: ☒ Small Entity ☐ Micro Entity ☐ Regular Undiscounted	
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.	
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ☒ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application Registration Number <u>51431</u> ☐ A sole inventor ☐ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ☐ A joint inventor; all of whom are signing this request	
Signature	/Keith J. Barkaus/
Name	Keith J. Barkaus

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
 Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	16888218			
Filing Date:	29-May-2020			
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP			
First Named Inventor/Applicant Name:	Nima Badizadegan			
Filer:	Keith J. Barkaus/Victoria Gilmore			
Attorney Docket Number:	05301-0009			
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	2814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				160

Doc Code: DISQ.E.FILE

Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 16888218

Filing Date: 29-May-2020

Applicant/Patent under Reexamination: Badizadegan

Electronic Terminal Disclaimer filed on July 8, 2020

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	39943114
Application Number:	16888218
International Application Number:	
Confirmation Number:	2004
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	05301-0009
Receipt Date:	08-JUL-2020
Filing Date:	29-MAY-2020
Time Stamp:	17:27:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 160
RAM confirmation Number	E202078H27021136
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	36631	no	2
			d250a2c71d4d785dbba3e0ef6168eda7ca611723		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30857	no	2
			8ffc5d7c855a80c588292f42700afea5a65b98ce		
Warnings:					
Information:					
Total Files Size (in bytes):			67488		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/888,218	05/29/2020	Nima Badizadegan	05301-0009	2004

1912 7590 06/12/2020
AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016

EXAMINER

ART UNIT	PAPER NUMBER
2632	

MAIL DATE	DELIVERY MODE
06/12/2020	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<i>Decision Granting Request for Prioritized Examination (Track I)</i>	Application No. 16/888,218	Applicant(s) Badizadegan, Nima	
	Examiner BRIAN W BROWN	Art Unit OPET	AIA (FITF) Status Yes
1. THE REQUEST FILED <u>29 May 2020</u> IS GRANTED . The above-identified application has met the requirements for prioritized examination A. ☒ for an original nonprovisional application (Track I). B. ☐ for an application undergoing continued examination (RCE). 2. The above-identified application will undergo prioritized examination. The application will be accorded special status throughout its entire course of prosecution until one of the following occurs: A. filing a <u>petition for extension of time</u> to extend the time period for filing a reply; B. filing an <u>amendment to amend the application to contain more than four independent claims, more than thirty total claims</u>, or a multiple dependent claim; C. filing a <u>request for continued examination</u> ; D. filing a notice of appeal; E. filing a request for suspension of action; F. mailing of a notice of allowance; G. mailing of a final Office action; H. completion of examination as defined in 37 CFR 41.102; or I. abandonment of the application. Telephone inquiries with regard to this decision should be directed to BRIAN BROWN at (571)272-5338. In his/her absence, calls may be directed to Petition Help Desk at (571) 272-3282.			
/BRIAN W BROWN/ Petitions Examiner, OPET			

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/888,218	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)	RATE(\$)	FEE(\$)	
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	75	N/A		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	330	N/A		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	380	N/A		
TOTAL CLAIMS (37 CFR 1.16(j))	21	minus 20 = *	1	x 50 =	50		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *		x 230 =	0.00		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			200			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
				TOTAL	1035	TOTAL	
* If the difference in column 1 is less than zero, enter "0" in column 2.							
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	x =	=
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	x =	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	x =	=
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	x =	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
16/888,218	05/29/2020	2827	1035	05301-0009	21	1

CONFIRMATION NO. 2004

FILING RECEIPT

1912
AMSTER, ROTHSTEIN & EBENSTEIN LLP
90 PARK AVENUE
NEW YORK, NY 10016



Date Mailed: 06/09/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Nima Badizadegan, New York, NY;

Applicant(s)

Nima Badizadegan, New York, NY;

Power of Attorney: The patent practitioners associated with Customer Number 01912

Domestic Priority data as claimed by applicant

This application is a CON of 16/670,702 10/31/2019
which claims benefit of 62/808,404 02/21/2019

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 06/08/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/888,218**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

**** SMALL ENTITY ****

Title

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	
Filing Date	Herewith
First Named Inventor	Nima Badizadegan
Title	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP
Art Unit	
Examiner Name	
Attorney Docket Number	05301-0009

SIGNATURE of Applicant or Patent Practitioner

Signature	/Keith J. Barkaus/	Date (Optional)	2020-05-29
Name	Keith J. Barkaus	Registration Number	51,431
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.



*Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number

Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)



I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

01912

OR



I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:



The address associated with the above-mentioned Customer Number

OR



The address associated with Customer Number:

OR



Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):



Inventor or Joint Inventor (title not required below)



Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)



Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)



Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

10/27/19

Name

Nima Badizadegan

Title

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.



Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of
Invention

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

As the below named inventor, I hereby declare that:

This declaration
is directed to:



The attached application, or



United States application or PCT international application number _____

filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Nima Badizadegan

Date (Optional): _____

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

ABSTRACT

The present invention relates to a field programmable gate array system that provides phase control with minimal latency.

CLAIMS

What is claimed is:

1. A method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of:

(a) receiving, by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream;

(b) receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase;

(c) transmitting, from the first plurality of data pins of the first interface to a deserializer in the field programmable gate array, the first serial data stream;

(d) transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal;

(e) generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal;

(f) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;

(g) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal;

(h) transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams;

(i) transmitting, from the deserializer via a first clock output pin on a second interface of the field programmable gate array to a phase detector that is part of the field programmable gate array system and not part of the field programmable gate array, the first receiver side clock signal;

(j) generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level:

(i) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase;

(ii) generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal;

(iii) generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase;

(iv) transmitting, from the serializer via a second clock output pin of the second interface to the phase detector, the interim transmitter side clock signal;

(v) generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal;

(vi) transmitting, from the phase detector to a phase controller of the field programmable gate array system which is placed within the field programmable gate array, the first output;

(vii) determining, by the phase controller, interim adjustment information based on the first output; and

(viii) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information, wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through (viii) are repeated until the first output of the phase detector is below the first threshold level;

(k) transmitting, from the serializer to the computational circuitry, first transmitter side clock signal;

(l) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams, wherein wherein the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams;

(m) transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams;

(n) converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and

(o) transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface, the second serial data stream.

2. The method of claim 1, wherein the third frequency corresponds to the first frequency.

3. The method of claim 2, wherein the third phase is not aligned with the first phase.

4. The method of claim 1, wherein the third frequency is different than the first frequency.

6. The method of claim 1, wherein the first set of operations includes at least one of the following:

- (i) an arithmetic operation;
- (ii) a logical operation;
- (iii) a pipeline operation; and
- (iv) a memory access operation.

7. The method of claim 1, wherein the first amount of data streams is the same as the second amount of data streams.

8. The method of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to one of the following:

- (i) eight (8) data streams;
- (ii) ten (10) data streams;
- (iii) sixteen (16) data streams;
- (iv) twenty (20) data streams;
- (v) thirty-two (32) data streams;

- (vi) forty (40) data streams;
- (vii) sixty-four (64) data streams;
- (viii) eighty (80) data streams;
- (ix) one hundred twenty-eight (128) data streams; and
- (x) one hundred sixty (160) data streams.

9. The method of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

10. The method of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

11. The method of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

12. The method of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.

13. The method of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.

14. The method of claim 1, wherein the fourth frequency is a rational multiple of the second frequency.

15. The method of claim 1, wherein the phase difference indicator signal is a pulse signal.

16. The method of claim 1, wherein adjustment information indicates at least one of the following:

- (A) a desired phase;

- (B) a desired frequency;
- (C) a change in phase; and
- (D) a change in frequency.

17. The method of claim 16, wherein adjustment information comprises a voltage.
18. The method of claim 17, wherein adjustment information comprises a digital transmission.
19. The method of claim 1, wherein the adjustment information is used to do at least one of the following:
 - (i) set a bias to an oscillator;
 - (ii) set a divider ratio; and
 - (iii) set a delay.
20. The method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.
21. The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.
22. The method of claim 1, wherein the first clock output pin is operationally connected to the deserializer and the second clock output pin is operationally connected to the serializer; and wherein the phase detector is not on the field programmable gate array and is operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array.

FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP

REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application No. 16/670,702, filed on October 31, 2019 and entitled “FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP,” which claims the benefit of and priority to U.S. Provisional Patent Application No. 62/808,404, filed on February 21, 2019 and entitled FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP, the contents of both of which are incorporated by reference herein in their entirety.

FIELD

[0002] The present invention generally relates to a field programmable gate array system. In embodiments, the present invention generally relates to a field programmable gate array and an external or internal phase controller providing phase matching between a receiver clock and a transmitter clock used in the field programmable gate array.

BACKGROUND

[0003] Field programmable gate arrays (FPGAs) may be used in applications that require fast processing since FPGAs allow for all computations to occur on a single chip that has massive fine-grained parallelism. For example, FPGAs are used in the financial industry in high frequency trading where the rapid processing of the FPGA is desired. One technological problem with FPGAs is that there is a need to synchronize receiving side and transmitting side clock signals within the FPGA.

[0004] The prior art sought to address this problem by including a clock domain crossing circuit in the FPGA. However, these circuits inherently add a delay to the processing that takes place in the FPGA, which is not desirable since high frequency trading may include timestamps that are accurate to the microsecond such that even small delays may present a large problem.

[0005] Synchronous Ethernet systems were designed with the similar goal of synchronizing a transmitter to a receiver. However, since phase alignment in synchronous Ethernet is not necessary, synchronous Ethernet FPGA systems usually do not phase-align the

receiver and transmitter sides of a link. The received clock is output from the transceiver to an external clock generation circuit to be used as its frequency reference. As a result, there is no measurement of the internal transmit clock at all by the Ethernet FPGA system.

[0006] While a synchronous Ethernet system with an internal PLL compares the transmit clock to the receive clock, its phase-frequency detector in the internal PLL is configured to measure accurately only the frequency but does not have to measure the phase of the two clocks accurately. In addition, synchronized protocols of the synchronous Ethernet system use simpler control loops that do not have to compensate for a lot of wander or jitter. Accordingly, the phase of the clocks is not treated as important as frequency by the synchronous Ethernet FPGA system. Based on these reasons, synchronous Ethernet FPGA systems do not provide a desirable solution to a technological problem of synchronizing receiving side and transmitting side clock signals within the FPGA.

[0007] Accordingly, a technical problem is presented in FPGAs in that phase synchronization between the receiver side clock and the transmitter side clock will introduce unwanted latency that results in delay of processing. Accordingly, it would be beneficial to provide an FPGA system that avoids these problems and provides sub-microsecond processing with throughput of at least 10 Gbps. In embodiments, the sub-microsecond processing throughput may be: 10-25 Gbps, 22-33 Gbps, 33-45 Gbps, 45-60 Gbps, 60-80 Gbps, 80-120 Gbps, to name a few.

SUMMARY

[0008] An object of the present invention is to address technological challenges that currently exist in phase matching receiver side and transmitter side clocks of a FPGA without introducing unnecessary delay in processing.

[0009] This and other objects shall be addressed by embodiments of the present invention as set forth herein.

[0010] The present invention generally relates to a field programmable gate array system and a method for processing a data stream using a field programmable gate array system. In embodiments, the present invention generally relates to a field programmable gate array and an

external or internal phase controller providing phase matching between a receiver clock and a transmitter clock used in the field programmable gate array.

[0011] More particularly, the present invention relates to a field programmable gate array system includes (a) a field programmable gate array comprising (1) a first interface including: (A) a first reference clock pin, wherein said first reference clock pin is configured to receive a first clock signal having a first frequency and a first phase; (B) a second reference clock pin, wherein said second reference clock pin is configured to receive a second clock signal having a second frequency and a second phase; (C) a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream; (D) a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream; (2) a deserializer operationally connected to: (x) the first reference clock pin to receive as a first input the first clock signal and (y) the first plurality of data pins to receive as a second input the first serial data stream, and wherein the deserializer is configured to: (A) convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams, and (B) generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase; and (C) transmit the first plurality of parallel data streams and the first receiver side clock signal within the field programmable gate array; (3) computational circuitry operationally connected to the deserializer to receive the first plurality of parallel data streams and the first receiver side clock signal, wherein the computational circuitry is configured to perform a first set of operations on the first plurality of parallel data streams to generate a second plurality of parallel processed data streams having a second amount of data streams; (4) a serializer operationally connected to: (x) the second reference clock pin to receive as a third input a first wire rate clock signal based on the second clock signal, wherein the first wire rate clock signal has a fourth frequency and a fourth phase; (y) the second plurality of data pins to transmit as a first output the second serial data stream; (z) the computational circuitry, wherein the serializer receives the second plurality of parallel processed data streams from the computational circuitry and the serializer transmits to the computational circuitry a first transmitter side clock signal including a fifth frequency and a fifth phase; and wherein the serializer is configured to: (A) convert the second plurality of parallel processed data streams into the second serial data stream; (B) generate the first transmitter side clock signal based on the first wire rate signal, wherein the first transmitter side clock signal has the fifth frequency and the fifth phase,

wherein the fifth frequency is different than and less than the fourth frequency; and (C) transmit the second serial data stream to the second plurality of data pins for transmission off the field programmable gate array; (5) a second interface including: (A) a first clock output pin configured to transmit the first receiver side clock signal, wherein the first clock output pin is operationally connected to the deserializer; and (B) a second clock output pin configured to transmit the first transmitter side clock signal, wherein the second clock output pin is operationally connected to the serializer; and (b) a phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit includes: (1) a phase detector operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array, and wherein the phase detector is configured to compare the third phase of the first receiver side clock signal to the fifth phase of the transmitter side clock signal and to generate a phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the fifth phase of the transmitter side clock signal; (2) a phase controller operationally connected to the phase detector and configured to receive the phase difference indicator signal, and wherein the phase controller is configured to determine adjustment information based on the phase difference indicator signal; and (3) an adjustable oscillator operationally connected to the phase controller and configured to receive the adjustment information as well as operationally connected to the second reference clock pin of the first interface of the field programmable gate array, wherein the adjustable oscillator is configured to generate the second clock signal including the second frequency and the second phase based on the adjustment information and transmit the second clock signal to the second reference clock pin of the first interface of the field programmable gate array; wherein the transmitter side clock signal and the first receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the fifth phase.

[0012] In embodiments, the third frequency corresponds to the first frequency.

[0013] In embodiments, the third phase is not aligned with the first phase.

[0014] In embodiments, the third frequency is different than the first frequency.

[0015] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams. In embodiments, the

adjustment information is used to do at least one of the following (i) set a bias to an oscillator; (ii) to set a divider ratio; and (iii) to set a delay.

[0016] In embodiments, the first set of operations includes an arithmetic operation. In embodiments, the first set of operations includes a logical operation. In embodiments, the first set of operations includes a pipeline operation. In embodiments, the first set of operations includes a memory access operation.

[0017] In embodiments, the first amount of data streams is the same as the second amount of data streams.

[0018] In embodiments, the first amount of data streams and the second amount of data streams are equal to eight (8) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to sixteen (16) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to twenty (20) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-two (32) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to forty (40) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to sixty-four (64) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to eighty (80) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to one hundred twenty-eight (128) data streams. In embodiments, the first amount of data streams and the second amount of data streams are equal to one hundred sixty (160) data streams.

[0019] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N , where N is an integer. In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N , where N is an integer. In embodiments the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N , where N is an integer.

[0020] In embodiments, the field programmable gate array further includes a phase lock loop configured to: receive the second clock signal, as a fourth input, to generate the first wire rate clock signal; and (B) transmit the first wire rate clock signal as the third input, to the serializer.

[0021] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.

[0022] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.

[0023] In embodiments, the fourth frequency is a rational multiple of the second frequency.

[0024] In embodiments, the phase difference indicator signal is a pulse signal.

[0025] In embodiments, the adjustment information indicates a desired phase. In embodiments, the adjustment information indicates a desired frequency. In embodiments, the adjustment information indicates a change in phase. In embodiments, the adjustment information indicates a change in frequency. In embodiments, adjustment information comprises a voltage. In embodiments, adjustment information comprises a digital transmission. In embodiments adjustment information further comprises a digital transmission.

[0026] In some embodiments, the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.

[0027] In embodiments, the trading algorithm includes the steps of: (a) parsing market data; (b) performing mathematical operations at a portion of the market data; and (c) generating order packets using at least an output of (b).

[0028] In embodiments, the first serial data stream includes market data and the second serial stream includes trading data.

[0029] In embodiments, the field programmable gate array includes a transceiver phase locked loop operatively connected between the to the serializer and the first reference clock pin.

[0030] In embodiments, the transceiver phase locked loop operatively connected between the serializer and the first reference clock pin includes a second adjustable oscillator to provide the first wire rate signal.

[0031] In embodiments, a second adjustable oscillator is provided outside of the transceiver phase locked loop and operatively connected to the serializer.

[0032] In embodiments, the second adjustable oscillator is programmable with a desired delay.

[0033] In embodiments, the desired delay is a constant value

[0034] In embodiments, the constant value is zero.

[0035] In embodiments, the adjustment information is provided to the second adjustable oscillator to provide the first wire rate signal.

[0036] The present invention also relates to a field programmable gate array system comprising (a) a field programmable gate array comprising (1) a first interface comprising (A) a first reference clock pin, wherein said first reference clock pin is configured to receive a first clock signal having a first frequency and a first phase; (B) a second reference clock pin, wherein said second reference clock pin is configured to receive a second clock signal having a second frequency and a second phase; (C) a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream; (D) a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream; (2) a deserializer operationally connected to (A) the first reference clock pin to receive as a first input the first clock signal and (B) the first plurality of data pins to receive as a second input the first serial data stream, and wherein the deserializer is configured to (A) convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams, and (B) generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase; and (C) transmit the first plurality of parallel data streams and the first receiver side clock signal within the field programmable gate array; (3) computational circuitry operationally connected to the deserializer to receive the first plurality of parallel data streams and the first receiver side clock signal, wherein the computational circuitry is configured to perform a first set of operations on the first plurality of parallel data streams to generate a second plurality of parallel processed data streams having a second amount of data streams; (4) a serializer operationally connected to (A) a transceiver phase lock loop to receive as a third input a first wire rate clock signal based on the second clock signal, wherein the first wire rate clock signal has a fourth frequency and a fourth phase; (B) the second plurality of

data pins to transmit as a first output the second serial data stream; (C) the computational circuitry, wherein the serializer receives the second plurality of parallel processed data streams from the computational circuitry and the serializer transmits to the computational circuitry a first transmitter side clock signal including a fifth frequency and a fifth phase; and wherein the serializer is configured to (A) convert the second plurality of parallel processed data streams into the second serial data stream; (B) generate the first transmitter side clock signal based on the first wire rate signal, wherein the first transmitter side clock signal has the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency; and (C) transmit the second serial data stream to the second plurality of data pins for transmission off the field programmable gate array; (5) a second interface comprising (A) a first clock output pin configured to transmit the first receiver side clock signal, wherein the first clock output pin is operationally connected to the deserializer; and (B) a second clock output pin configured to transmit the first transmitter side clock signal, wherein the second clock output pin is operationally connected to the serializer; and (b) a phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises (1) a phase detector operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array, and wherein the phase detector is configured to compare the third phase of the first receiver side clock signal to the fifth phase of the transmitter side clock signal and to generate a phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the fifth phase of the transmitter side clock signal; (2) a phase controller operationally connected to the phase detector and configured to receive the phase difference indicator signal, and wherein the phase controller is configured to determine adjustment information based on the phase difference indicator signal; and (3) an adjustable oscillator operationally connected to the phase controller and configured to receive the adjustment information as well as operationally connected to the second reference clock pin of the first interface of the field programmable gate array, wherein the adjustable oscillator is configured to generate the second clock signal including the second frequency and the second phase based on the adjustment information and transmit the second clock signal to the second reference clock pin of the first interface of the field programmable gate array, wherein the transmitter side clock signal and the first receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the fifth phase.

- [0037] In embodiments, the third frequency corresponds to the first frequency.
- [0038] In embodiments, the third phase is not aligned with the first phase.
- [0039] In embodiments, the third frequency is different than the first frequency.
- [0040] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.
- [0041] In embodiments, the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.
- [0042] In embodiments, the first amount of data streams is the same as the second amount of data streams.
- [0043] In embodiments, the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.
- [0044] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N , where N is an integer.
- [0045] In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N , where N is an integer.
- [0046] In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N , where N is an integer.
- [0047] In embodiments, the transceiver phase lock loop is operationally connected to the second reference clock pin and is configured to: (A) receive the second clock signal, as a fourth input, to generate the first wire rate clock signal; and (B) transmit the first wire rate clock signal as the third input, to the serializer.
- [0048] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.

[0049] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.

[0050] In embodiments, the fourth frequency is a rational multiple of the second frequency.

[0051] In embodiments, the phase difference indicator signal is a pulse signal.

[0052] In embodiments, adjustment information indicates at least one of the following: (A) a desired phase; (B) a desired frequency; (C) a change in phase; and (D) a change in frequency.

[0053] In embodiments, adjustment information comprises a voltage.

[0054] In embodiments, adjustment information comprise a digital transmission.

[0055] In embodiments, the adjustment information is used to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay.

[0056] In embodiments, the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.

[0057] In embodiments, the first serial data stream includes market data and the second serial data stream includes trading data.

[0058] In embodiments, the field programmable gate array system further comprises (a) a fourth plurality of data pins of the first interface, wherein the fourth plurality of data pins is configured to transmit a fourth serial data stream; (b) a second deserializer operationally connected to (i) the first reference clock pin to receive the first clock signal as a third input to the second deserializer, wherein the second deserializer is configured to: (A) receive a third serial data stream; (B) convert the third serial data stream into a third plurality of parallel data streams having a third amount of data streams; (C) generate a second receiver side clock signal based on the first clock signal, wherein the second receiver side clock signal has a sixth frequency and a sixth phase; and (D) transmit within the field programmable gate array to the computational circuitry the third plurality of parallel data streams and the second receiver side clock signal; (ii) the computational circuitry further configured to (A) receive the third plurality of parallel data streams and the second receiver side clock signal; and (B) generate a fourth plurality of parallel processed data streams having a fourth amount of data streams; (c) a second serializer operationally connected to: (i) the transceiver phase lock loop to receive as a fifth input the first wire rate clock signal based on the second clock signal; and (ii) the fourth plurality of data pins to transmit as a second output the

fourth serial data stream, wherein the second serializer is configured to (A) receive the fourth plurality of parallel processed data streams from the computational circuitry; (B) convert the fourth plurality of parallel processed data streams into the fourth serial data stream; (C) transmit the fourth serial data stream to the fourth plurality of data pins for transmission off the field programmable gate array; (d) a third clock output pin of the second interface configured to transmit the second receiver side clock signal, wherein the third clock output pin is operationally connected to the second deserializer; and (e) a second phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises: (i) a second phase detector operationally connected to the first clock output pin and the third clock output pin of the second interface of the field programmable gate array, wherein the second phase detector is configured to (A) compare the third phase of the first receiver side clock signal to the sixth phase of the second receiver side clock signal; and (B) generate a second phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the sixth phase of the second receiver side clock signal; (ii) a second phase controller operationally connected to the second phase detector and configured to receive the second phase difference indicator signal, wherein the second phase controller is configured to determine second adjustment information based on the second phase difference indicator signal; and (iii) a delay element operationally connected to the second phase controller and to the second deserializer, wherein the second phase controller sends to the delay element the second adjustment information, wherein the delay element is configured to (A) delay the third serial data stream based on the second adjustment information, and (B) transmit the third serial data stream to the second deserializer, wherein the first receiver side clock signal and the second receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the sixth phase.

[0059] In embodiments, the field programmable gate array system further comprises a third plurality of data pins of the first interface, wherein the delay element is placed on the field programmable gate array and operationally connected to the third plurality of data pins and wherein the delay element is further configured to (A) receive the third serial data stream via the third plurality of data pins, and (B) transmit the third serial data stream to the second deserializer.

[0060] In embodiments, the field programmable gate array system further comprises a third plurality of data pins of the first interface, wherein (A) the delay element is placed outside of the field programmable gate array, (B) the delay element and the second deserializer are

operationally connected to the third plurality of data pins, and (C) the third plurality of data pins is further configured to transmit the third serial data stream from the delay element to the second deserializer.

[0061] The present invention also relates to a method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of (a) receiving, by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream; (b) receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase; (c) transmitting, from the first plurality of data pins of the first interface to a deserializer in the field programmable gate array, the first serial data stream; (d) transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal; (e) generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal; (f) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams; (g) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal; (h) transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams; (i) transmitting, from the deserializer via a first clock output pin on a second interface of the field programmable gate array to a phase detector that is part of the field programmable gate array system and not part of the field programmable gate array, the first receiver side clock signal; (j) generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level: (i) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase; (ii) generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal; (iii) generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase; (iv) transmitting, from the serializer via a second clock output pin of the second interface to the phase detector, the interim transmitter side clock signal; (v) generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal; (vi) transmitting,

from the phase detector to a phase controller of the field programmable gate array system which is placed within the field programmable gate array, the first output; (vii) determining, by the phase controller, interim adjustment information based on the first output; and (viii) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information, wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through (viii) are repeated until the first output of the phase detector is below the first threshold level; (k) transmitting, from the serializer to the computational circuitry, first transmitter side clock signal; (l) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams; (m) transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams; (n) converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and (o) transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface, the second serial data stream.

- [0062] In embodiments, step (a) is performed before step (b).
- [0063] In embodiments, step (b) is performed before step (a).
- [0064] In embodiments, step (a) and step (b) are performed contemporaneously.
- [0065] In embodiments, step (c) is performed before step (d).
- [0066] In embodiments, step (d) is performed before step (c).
- [0067] In embodiments, step (c) and step (d) are performed contemporaneously.
- [0068] In embodiments, step (e) is performed before step (f).
- [0069] In embodiments, step (f) is performed before step (e).
- [0070] In embodiments, step (e) and step (f) are performed contemporaneously.
- [0071] In embodiments, the second frequency corresponds to the first frequency.
- [0072] In embodiments, the second phase is not aligned with the first phase.
- [0073] In embodiments, the second frequency is different from the first frequency.
- [0074] In embodiments, step (g) is performed before step (h).

- [0075] In embodiments, step (h) is performed before step (g).
- [0076] In embodiments, step (g) and step (h) are performed contemporaneously.
- [0077] In embodiments, the step (i) comprises transmitting, from the deserializer to the phase detector, the first receiver side clock signal via a first zero delay buffer phase lock loop of the field programmable gate array before transmitting the first receiver side clock signal via the first clock output pin of the second interface.
- [0078] In embodiments, the third frequency corresponds to the second frequency.
- [0079] In embodiments, the third phase is aligned with the second phase.
- [0080] In embodiments, a difference between the third phase and the second phase is less than a second threshold level
- [0081] In embodiments, the sixth frequency corresponds to the third frequency.
- [0082] In embodiments, the sixth phase is not aligned with the third phase prior to the first output of the phase detector being below the first threshold level.
- [0083] In embodiments, the step (j)(iv) comprises transmitting, from the serializer to the phase detector, the interim transmitter side clock signal via a second zero delay buffer phase lock loop of the field programmable gate array before transmitting the interim transmitter side clock signal via the second clock output pin of the second interface.
- [0084] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.
- [0085] In embodiments, the first amount of data streams is the same as the second amount of data streams.
- [0086] In embodiments, the first amount of data streams and the second amount of data streams is one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; and (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.
- [0087] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

[0088] In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

[0089] In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0090] In embodiments, at least a portion of the first set of operations is performed prior to step (k).

[0091] In embodiments, at least a portion of the first set of operations is performed after step (k).

[0092] In embodiments, all of the first set of operations is performed after step (k).

[0093] In embodiments, the transmission of the second serial data stream from the serializer off the field programmable gate array is transmitted to an input/output module off the field programmable gate array.

[0094] In embodiments, the first serial data stream includes market data and the second serial data stream includes trading data.

[0095] In embodiments, the step of generating the first wire rate clock signal further includes: (a) receiving, from the adjustable oscillator at a transceiver phase lock loop via a second reference clock pin in the first interface, the second clock signal; (b) processing, by the transceiver phase lock loop, the received second clock signal; (c) providing, by the transceiver phase lock loop, the first wire rate clock signal based on the processing of the received clock signal; and (d) transmitting, by the transceiver phase lock loop, the first wire rate clock signal to the serializer.

[0096] In embodiments, a phase lock loop generates the first wire rate clock signal.

[0097] In embodiments, the phase lock loop is on the field programmable gate array.

[0098] In embodiments, the phase lock loop that is part of the field programmable gate array system and not part of the field programmable gate array.

[0099] In embodiments, the step of generating the first wire rate clock signal further includes: (a) processing the second clock signal; (b) providing the first wire rate clock signal based on the processing of the second clock signal; and (c) transmitting, to the serializer, the first wire rate clock signal.

[0100] In embodiments, the sixth frequency corresponds to the third frequency.

[0101] In embodiments, the sixth phase is not aligned with the third phase.

[0102] The present invention also relates to a field programmable gate array system comprising: (a) a field programmable gate array comprising (1) a first interface comprising (A) a first reference clock pin, wherein said first reference clock pin is configured to receive a first clock signal having a first frequency and a first phase; (B) a second reference clock pin, wherein said second reference clock pin is configured to receive a second clock signal having a second frequency and a second phase; (C) a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream; (D) a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream; (2) a deserializer operationally connected to (A) the first reference clock pin to receive as a first input the first clock signal and (B) the first plurality of data pins to receive as a second input the first serial data stream, and wherein the deserializer is configured to (A) convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams; (B) generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase; and (C) transmit the first plurality of parallel data streams and the first receiver side clock signal within the field programmable gate array; (3) computational circuitry operationally connected to the deserializer to receive the first plurality of parallel data streams and the first receiver side clock signal, wherein the computational circuitry is configured to perform a first set of operations on the first plurality of parallel data streams to generate a second plurality of parallel processed data streams having a second amount of data streams; (4) a serializer operationally connected to (A) a transceiver phase lock loop to receive as a third input a first wire rate clock signal based on the second clock signal, wherein the first wire rate clock signal has a fourth frequency and a fourth phase; (B) the second plurality of data pins to transmit as a first output the second serial data stream; (C) the computational circuitry, wherein the serializer receives the second plurality of parallel processed data streams from the computational circuitry and the serializer transmits to the computational circuitry a first transmitter side clock signal including a fifth frequency and a fifth phase; and wherein the serializer is configured to (A) convert the second plurality of parallel processed data streams into the second serial data stream; (B) generate the first transmitter side clock signal based on the first wire rate signal, wherein the first transmitter side clock signal has the fifth frequency and the fifth phase,

wherein the fifth frequency is different than and less than the fourth frequency; and (C) transmit the second serial data stream to the second plurality of data pins for transmission off the field programmable gate array; and (b) a phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises (1) a phase detector configured to compare the third phase of the first receiver side clock signal to the fifth phase of the transmitter side clock signal and to generate a phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the fifth phase of the transmitter side clock signal; (2) a phase controller operationally connected to the phase detector and configured to receive the phase difference indicator signal, and wherein the phase controller is configured to determine adjustment information based on the phase difference indicator signal; and (3) a phase lock loop with phase adjustment operationally connected to the phase controller and configured to receive the adjustment information as well as operationally connected to the second reference clock pin of the first interface of the field programmable gate array, wherein the phase lock loop with phase adjustment is configured to generate the second clock signal including the second frequency and the second phase based on the adjustment information and transmit the second clock signal to the second reference clock pin of the first interface of the field programmable gate array, wherein the transmitter side clock signal and the first receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the fifth phase.

[0103] In embodiments, the third frequency corresponds to the first frequency.

[0104] In embodiments, the third phase is not aligned with the first phase.

[0105] In embodiments, the third frequency is different than the first frequency.

[0106] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

[0107] In embodiments, the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

[0108] In embodiments, the first amount of data streams is the same as the second amount of data streams.

[0109] In embodiments, the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

[0110] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

[0111] In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

[0112] In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0113] In embodiments, the transceiver phase lock loop is operationally connected to the second reference clock pin and is configured to (A) receive the second clock signal, as a fourth input, to generate the first wire rate clock signal; and (B) transmit the first wire rate clock signal as the third input, to the serializer.

[0114] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.

[0115] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.

[0116] In embodiments, the fourth frequency is a rational multiple of the second frequency.

[0117] In embodiments, the phase difference indicator signal is a pulse signal.

[0118] In embodiments, adjustment information indicates at least one of the following: (A) a desired phase; (B) a desired frequency; (C) a change in phase; and (D) a change in frequency.

[0119] In embodiments, adjustment information comprises a voltage.

[0120] In embodiments, adjustment information comprise a digital transmission.

[0121] In embodiments, the adjustment information is used to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay.

[0122] In embodiments, the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.

[0123] In embodiments, the first serial data stream includes market data and the second serial data stream includes trading data.

[0124] In embodiments, the field programmable gate array system further comprises: (5) a second interface comprising (A) a first clock output pin configured to transmit the first receiver side clock signal, wherein the first clock output pin is operationally connected to the deserializer; and (B) a second clock output pin configured to transmit the first transmitter side clock signal, wherein the second clock output pin is operationally connected to the serializer; and wherein the phase detector is not on the field programmable gate array and is operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array.

[0125] In embodiments, the field programmable gate array system further comprises (a) a fourth plurality of data pins of the first interface, wherein the fourth plurality of data pins is configured to transmit a fourth serial data stream; (b) a second deserializer operationally connected to: (i) the first reference clock pin to receive the first clock signal as a third input to the second deserializer, wherein the second deserializer is configured to (A) receive a third serial data stream; (B) convert the third serial data stream into a third plurality of parallel data streams having a third amount of data streams; (C) generate a second receiver side clock signal based on the first clock signal, wherein the second receiver side clock signal has a sixth frequency and a sixth phase; and (D) transmit within the field programmable gate array to the computational circuitry the third plurality of parallel data streams and the second receiver side clock signal; (ii) the computational circuitry further configured to (A) receive the third plurality of parallel data streams and the second receiver side clock signal; and (B) generate a fourth plurality of parallel processed data streams having a fourth amount of data streams; (c) a second serializer operationally connected to: (i) the transceiver phase lock loop to receive as a fifth input the first wire rate clock signal based on the second clock signal; and (ii) the fourth plurality of data pins to transmit as a second output the fourth serial data stream, wherein the second serializer is configured to (A) receive the fourth plurality of parallel processed data streams from the computational circuitry; (B) convert the fourth plurality of parallel processed data streams into the fourth serial data stream; (C) transmit the fourth

serial data stream to the fourth plurality of data pins for transmission off the field programmable gate array; and (d) a second phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises (i) a second phase detector configured to (A) compare the third phase of the first receiver side clock signal to the sixth phase of the second receiver side clock signal; and (B) generate a second phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the sixth phase of the second receiver side clock signal; (ii) a second phase controller operationally connected to the second phase detector and configured to receive the second phase difference indicator signal, wherein the second phase controller is configured to determine second adjustment information based on the second phase difference indicator signal; and (iii) a delay element operationally connected to the second phase controller and to the second deserializer, wherein the second phase controller sends to the delay element the second adjustment information, wherein the delay element is configured to (A) delay the third serial data stream based on the second adjustment information, and (B) transmit the third serial data stream to the second deserializer, wherein the first receiver side clock signal and the second receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the sixth phase.

[0126] In embodiments, the field programmable gate array system further comprises a third plurality of data pins of the first interface, wherein the delay element is placed on the field programmable gate array and operationally connected to the third plurality of data pins and wherein the delay element is further configured to (A) receive the third serial data stream via the third plurality of data pins, and (B) transmit the third serial data stream to the second deserializer.

[0127] In embodiments, the field programmable gate array system further comprises a third plurality of data pins of the first interface, wherein (A) the delay element is placed outside of the field programmable gate array, (B) the delay element and the second deserializer are operationally connected to the third plurality of data pins, and (C) the third plurality of data pins is further configured to transmit the third serial data stream from the delay element to the second deserializer.

[0128] In embodiments, the field programmable gate array system further comprises (A) a first clock output pin of a second interface of the field programmable gate array, the first clock output pin being configured to transmit the first receiver side clock signal from the deserializer to

the second phase detector; and (B) a third clock output pin of the second interface configured to transmit the second receiver side clock signal from the second deserializer to the second phase detector, wherein the second phase detector is not placed on the field programmable gate array and is operationally connected to the first clock output pin and the third clock output pin of the second interface of the field programmable gate array.

[0129] The present invention also relates to a method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of: (a) receiving, by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream; (b) receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase; (c) transmitting, from the first plurality of data pins of the first interface to a deserializer in the field programmable gate array, the first serial data stream; (d) transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal; (e) generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal; (f) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams; (g) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal; (h) transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams; (i) transmitting, from the deserializer to a phase detector of the field programmable gate array system, the first receiver side clock signal; (j) generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level: (i) generating, by a phase lock loop with phase adjustment in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase; (ii) generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal; (iii) generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase; (iv) transmitting, from the serializer to the phase detector, the interim transmitter side clock signal; (v) generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal; (vi)

transmitting, from the phase detector to a phase controller of the field programmable gate array system which is placed within the field programmable gate array, the first output; (vii) determining, by the phase controller, interim adjustment information based on the first output; and (viii) transmitting, from the phase controller to the phase lock loop with phase adjustment, the interim adjustment information; wherein, the phase lock loop with phase adjustment adjusts the second clock signal based on the interim adjustment information and steps (i) through (viii) are repeated until the first output of the phase detector is below the first threshold level; (k) transmitting, from the serializer to the computational circuitry, first transmitter side clock signal; (l) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams; (m) transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams; (n) converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and (o) transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface, the second serial data stream.

- [0130] In embodiments, step (a) is performed before step (b).
- [0131] In embodiments, step (b) is performed before step (a).
- [0132] In embodiments, step (a) and step (b) are performed contemporaneously.
- [0133] In embodiments, step (c) is performed before step (d).
- [0134] In embodiments, step (d) is performed before step (c).
- [0135] In embodiments, step (c) and step (d) are performed contemporaneously.
- [0136] In embodiments, step (e) is performed before step (f).
- [0137] In embodiments, step (f) is performed before step (e).
- [0138] In embodiments, step (e) and step (f) are performed contemporaneously.
- [0139] In embodiments, the second frequency corresponds to the first frequency.
- [0140] In embodiments, the second phase is not aligned with the first phase.
- [0141] In embodiments, the second frequency is different from the first frequency.

- [0142] In embodiments, step (g) is performed before step (h).
- [0143] In embodiments, step (h) is performed before step (g).
- [0144] In embodiments, step (g) and step (h) are performed contemporaneously.
- [0145] In embodiments, the phase detector is not placed on the field programmable gate array and the step (i) comprises transmitting, from the deserializer to the phase detector via a first clock output pin on a second interface of the field programmable gate array, the first receiver side clock signal.
- [0146] In embodiments, the step (i) further comprises transmitting, from the deserializer to the phase detector, the first receiver side clock signal via a first zero delay buffer phase lock loop of the field programmable gate array before transmitting the first receiver side clock signal via the first clock output pin of the second interface.
- [0147] In embodiments, the third frequency corresponds to the second frequency.
- [0148] In embodiments, the third phase is aligned with the second phase.
- [0149] In embodiments, a difference between the third phase and the second phase is less than a second threshold level
- [0150] In embodiments, the sixth frequency corresponds to the third frequency.
- [0151] In embodiments, the sixth phase is not aligned with the third phase prior to the first output of the phase detector being below the first threshold level.
- [0152] In embodiments, the phase detector is not placed on the field programmable gate array and the step (j)(iv) comprises transmitting, from the serializer to the phase detector via a second clock output pin of the second interface of the field programmable gate array, the interim transmitter side clock signal.
- [0153] In embodiments, the step (j)(iv) further comprises transmitting, from the serializer to the phase detector, the interim transmitter side clock signal via a second zero delay buffer phase lock loop of the field programmable gate array before transmitting the interim transmitter side clock signal via the second clock output pin of the second interface.
- [0154] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

[0155] In embodiments, the first amount of data streams is the same as the second amount of data streams.

[0156] In embodiments, the first amount of data streams and the second amount of data streams is one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

[0157] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

[0158] In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

[0159] In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0160] In embodiments, at least a portion of the first set of operations is performed prior to step (k).

[0161] In embodiments, at least a portion of the first set of operations is performed after step (k).

[0162] In embodiments, all of the first set of operations is performed after step (k).

[0163] In embodiments, the transmission of the second serial data stream from the serializer off the field programmable gate array is transmitted to an input/output module off the field programmable gate array.

[0164] In embodiments, the first serial data stream includes market data and the second serial data stream includes trading data.

[0165] In embodiments, the step of generating the first wire rate clock signal further includes: (a) receiving, from the phase lock loop with phase adjustment at a transceiver phase lock loop via a second reference clock pin in the first interface, the second clock signal; (b) processing, by the transceiver phase lock loop, the received second clock signal; (c) providing, by the transceiver phase lock loop, the first wire rate clock signal based on the processing of the received

clock signal; and (d) transmitting, by the transceiver phase lock loop, the first wire rate clock signal to the serializer.

[0166] In embodiments, a phase lock loop generates the first wire rate clock signal.

[0167] In embodiments, the phase lock loop is on the field programmable gate array.

[0168] In embodiments, the phase lock loop that is part of the field programmable gate array system and not part of the field programmable gate array.

[0169] In embodiments, the step of generating the first wire rate clock signal further includes: (a) processing the second clock signal; (b) providing the first wire rate clock signal based on the processing of the second clock signal; and (c) transmitting, to the serializer, the first wire rate clock signal.

[0170] In embodiments, the sixth frequency corresponds to the third frequency.

[0171] In embodiments, the sixth phase is not aligned with the third phase.

[0172] The present invention also relates to a field programmable gate array system comprising (a) a field programmable gate array comprising (1) a first interface comprising (A) a first reference clock pin, wherein said first reference clock pin is configured to receive a first clock signal having a first frequency and a first phase; (B) a second reference clock pin, wherein said second reference clock pin is configured to receive the first clock signal; (C) a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream; (D) a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream; (2) a deserializer operationally connected to (A) the first reference clock pin to receive as a first input the first clock signal and (B) the first plurality of data pins to receive as a second input the first serial data stream, and wherein the deserializer is configured to (A) convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams; (B) generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase; and (C) transmit the first plurality of parallel data streams and the first receiver side clock signal within the field programmable gate array; (3) computational circuitry operationally connected to the deserializer to receive the first plurality of parallel data streams and the first receiver side clock signal, wherein the computational circuitry is configured to perform a first set

of operations on the first plurality of parallel data streams to generate a second plurality of parallel processed data streams having a second amount of data streams; (4) a serializer operationally connected to (A) an adjustable transceiver phase lock loop to receive as a third input a first wire rate clock signal, wherein the first wire rate clock signal has a fourth frequency and a fourth phase; (B) the second plurality of data pins to transmit as a first output the second serial data stream; (C) the computational circuitry, wherein the serializer receives the second plurality of parallel processed data streams from the computational circuitry and the serializer transmits to the computational circuitry a first transmitter side clock signal including a fifth frequency and a fifth phase; and wherein the serializer is configured to (A) convert the second plurality of parallel processed data streams into the second serial data stream; (B) generate the first transmitter side clock signal based on the first wire rate signal, wherein the first transmitter side clock signal has the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency; and (C) transmit the second serial data stream to the second plurality of data pins for transmission off the field programmable gate array; and (b) a phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises (1) a phase detector configured to compare the third phase of the first receiver side clock signal to the fifth phase of the transmitter side clock signal and to generate a phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the fifth phase of the transmitter side clock signal; (2) a phase controller operationally connected to the phase detector and configured to receive the phase difference indicator signal, and wherein the phase controller is configured to determine adjustment information based on the phase difference indicator signal; and (3) the adjustable transceiver phase lock loop operationally connected to the phase controller and configured to receive the adjustment information as well as operationally connected to the second reference clock pin of the first interface of the field programmable gate array, wherein the adjustable transceiver phase lock loop is configured to generate a second clock signal including the second frequency and the second phase based on the first clock signal received via the second reference clock pin and process the second clock signal based on the adjustment information received from the phase controller to generate the first wire rate clock signal, wherein the transmitter side clock signal and the first receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the fifth phase.

- [0173] In embodiments, the third frequency corresponds to the first frequency.
- [0174] In embodiments, the third phase is not aligned with the first phase.
- [0175] In embodiments, the third frequency is different than the first frequency.
- [0176] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.
- [0177] In embodiments, the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.
- [0178] In embodiments, the first amount of data streams is the same as the second amount of data streams.
- [0179] In embodiments, the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.
- [0180] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N , where N is an integer.
- [0181] In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N , where N is an integer.
- [0182] In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N , where N is an integer.
- [0183] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.
- [0184] In embodiments, the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.
- [0185] In embodiments, the fourth frequency is a rational multiple of the second frequency.
- [0186] In embodiments, the phase difference indicator signal is a pulse signal.

[0187] In embodiments, adjustment information indicates at least one of the following: (A) a desired phase; (B) a desired frequency; (C) a change in phase; and (D) a change in frequency.

[0188] In embodiments, adjustment information comprises a voltage.

[0189] In embodiments, adjustment information comprises a digital transmission.

[0190] In embodiments, the adjustment information is used to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay.

[0191] In embodiments, the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.

[0192] In embodiments, the first serial data stream includes market data and the second serial data stream includes trading data.

[0193] In embodiments, the field programmable gate array system further comprises (5) a second interface comprising (A) a first clock output pin configured to transmit the first receiver side clock signal, wherein the first clock output pin is operationally connected to the deserializer; and (B) a second clock output pin configured to transmit the first transmitter side clock signal, wherein the second clock output pin is operationally connected to the serializer, wherein the phase detector is not on the field programmable gate array and is operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array.

[0194] In embodiments, the field programmable gate array system further comprises (a) a fourth plurality of data pins of the first interface, wherein the fourth plurality of data pins is configured to transmit a fourth serial data stream; (b) a second deserializer operationally connected to: (i) the first reference clock pin to receive the first clock signal as a third input to the second deserializer, wherein the second deserializer is configured to (A) receive a third serial data stream; (B) convert the third serial data stream into a third plurality of parallel data streams having a third amount of data streams; (C) generate a second receiver side clock signal based on the first clock signal, wherein the second receiver side clock signal has a sixth frequency and a sixth phase; and (D) transmit within the field programmable gate array to the computational circuitry the third plurality of parallel data streams and the second receiver side clock signal; (ii) the computational circuitry further configured to (A) receive the third plurality of parallel data streams and the second

receiver side clock signal; and (B) generate a fourth plurality of parallel processed data streams having a fourth amount of data streams; (c) a second serializer operationally connected to: (i) the adjustable transceiver phase lock loop to receive as a fifth input the first wire rate clock signal based on the second clock signal; and (ii) the fourth plurality of data pins to transmit as a second output the fourth serial data stream, wherein the second serializer is configured to (A) receive the fourth plurality of parallel processed data streams from the computational circuitry; (B) convert the fourth plurality of parallel processed data streams into the fourth serial data stream; (C) transmit the fourth serial data stream to the fourth plurality of data pins for transmission off the field programmable gate array; and (d) a second phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises (i) a second phase detector configured to (A) compare the third phase of the first receiver side clock signal to the sixth phase of the second receiver side clock signal; and (B) generate a second phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the sixth phase of the second receiver side clock signal; (ii) a second phase controller operationally connected to the second phase detector and configured to receive the second phase difference indicator signal, wherein the second phase controller is configured to determine second adjustment information based on the second phase difference indicator signal; and (iii) a delay element operationally connected to the second phase controller and to the second deserializer, wherein the second phase controller sends to the delay element the second adjustment information, wherein the delay element is configured to (A) delay the third serial data stream based on the second adjustment information, and (B) transmit the third serial data stream to the second deserializer, wherein the first receiver side clock signal and the second receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the sixth phase.

[0195] In embodiments, the field programmable gate array system further comprises a third plurality of data pins of the first interface, wherein the delay element is placed on the field programmable gate array and operationally connected to the third plurality of data pins and wherein the delay element is further configured to (A) receive the third serial data stream via the third plurality of data pins, and (B) transmit the third serial data stream to the second deserializer.

[0196] In embodiments, the field programmable gate array system further comprises a third plurality of data pins of the first interface, wherein (A) the delay element is placed outside of

the field programmable gate array, (B) the delay element and the second deserializer are operationally connected to the third plurality of data pins, and (C) the third plurality of data pins is further configured to transmit the third serial data stream from the delay element to the second deserializer.

[0197] In embodiments, the field programmable gate array system further comprises (A) a first clock output pin of a second interface of the field programmable gate array, the first clock output pin being configured to transmit the first receiver side clock signal from the deserializer to the second phase detector; and (B) a third clock output pin of the second interface configured to transmit the second receiver side clock signal from the second deserializer to the second phase detector, wherein the second phase detector is not placed on the field programmable gate array and is operationally connected to the first clock output pin and the third clock output pin of the second interface of the field programmable gate array.

[0198] The present invention also relates to a method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of (a) receiving, by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream; (b) receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase; (c) transmitting, from the first plurality of data pins of the first interface to a deserializer in the field programmable gate array, the first serial data stream; (d) transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal; (e) generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal; (f) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams; (g) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal; (h) transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams; (i) transmitting, from the deserializer to a phase detector of the field programmable gate array system, the first receiver side clock signal; (j) generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level: (i) receiving, by an adjustable

transceiver phase lock loop via a second reference clock pin in the first interface, the first clock signal to generate a second clock signal having a fourth frequency and a fourth phase; (ii) generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal and interim adjustment information; (iii) generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase; (iv) transmitting, from the serializer to the phase detector, the interim transmitter side clock signal; (v) generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal; (vi) transmitting, from the phase detector to a phase controller of the field programmable gate array system which is placed within the field programmable gate array, the first output; (vii) determining, by the phase controller, the interim adjustment information based on the first output; and (viii) transmitting, from the phase controller to the adjustable transceiver phase lock loop, the interim adjustment information, wherein, the adjustable transceiver phase lock loop adjusts the second clock signal based on the interim adjustment information and steps (i) through (viii) are repeated until the first output of the phase detector is below the first threshold level; (k) transmitting, from the serializer to the computational circuitry, first transmitter side clock signal; (l) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams; (m) transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams; (n) converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and (o) transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface, the second serial data stream.

- [0199] In embodiments, step (a) is performed before step (b).
- [0200] In embodiments, step (b) is performed before step (a).
- [0201] In embodiments, step (a) and step (b) are performed contemporaneously.
- [0202] In embodiments, step (c) is performed before step (d).
- [0203] In embodiments, step (d) is performed before step (c).
- [0204] In embodiments, step (c) and step (d) are performed contemporaneously.

- [0205] In embodiments, step (e) is performed before step (f).
- [0206] In embodiments, step (f) is performed before step (e).
- [0207] In embodiments, step (e) and step (f) are performed contemporaneously.
- [0208] In embodiments, the second frequency corresponds to the first frequency.
- [0209] In embodiments, the second phase is not aligned with the first phase.
- [0210] In embodiments, the second frequency is different from the first frequency.
- [0211] In embodiments, step (g) is performed before step (h).
- [0212] In embodiments, step (h) is performed before step (g).
- [0213] In embodiments, step (g) and step (h) are performed contemporaneously.
- [0214] In embodiments, the phase detector is not placed on the field programmable gate array and the step (i) comprises transmitting, from the deserializer to the phase detector via a first clock pin on a second interface of the field programmable gate array, the first receiver side clock signal.
- [0215] In embodiments, the step (i) further comprises transmitting, from the deserializer to the phase detector, the first receiver side clock signal via a first zero delay buffer phase lock loop of the field programmable gate array before transmitting the first receiver side clock signal via the first clock output pin of the second interface.
- [0216] In embodiments, the third frequency corresponds to the second frequency.
- [0217] In embodiments, the third phase is aligned with the second phase.
- [0218] In embodiments, a difference between the third phase and the second phase is less than a second threshold level
- [0219] In embodiments, the sixth frequency corresponds to the third frequency.
- [0220] In embodiments, the sixth phase is not aligned with the third phase prior to the first output of the phase detector being below the first threshold level.
- [0221] In embodiments, the phase detector is not placed on the field programmable gate array and the step (j)(iv) comprises transmitting, from the serializer to the phase detector via a

second clock output pin of the second interface of the field programmable gate array, the interim transmitter side clock signal.

[0222] In embodiments, the step (j)(iv) further comprises transmitting, from the serializer to the phase detector, the interim transmitter side clock signal via a second zero delay buffer phase lock loop of the field programmable gate array before transmitting the interim transmitter side clock signal via the second clock output pin of the second interface.

[0223] In embodiments, the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

[0224] In embodiments, the first amount of data streams is the same as the second amount of data streams.

[0225] In embodiments, the first amount of data streams and the second amount of data streams is one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

[0226] In embodiments, the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

[0227] In embodiments, the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

[0228] In embodiments, the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0229] In embodiments, at least a portion of the first set of operations is performed prior to step (k).

[0230] In embodiments, at least a portion of the first set of operations is performed after step (k).

[0231] In embodiments, all of the first set of operations is performed after step (k).

[0232] In embodiments, the transmission of the second serial data stream from the serializer off the field programmable gate array is transmitted to an input/output module off the field programmable gate array.

[0233] In embodiments, the first serial data stream includes market data and the second serial data stream includes trading data.

[0234] In embodiments, the step of generating the first wire rate clock signal further includes: (a) generating, by the adjustable phase lock loop, the second clock signal based on the received first clock signal; (b) processing, by the adjustable transceiver phase lock loop, the second clock signal based on the interim adjustment information received from the phase controller; (c) providing, by the adjustable transceiver phase lock loop, the first wire rate clock signal based on the processing of the second clock signal; and (d) transmitting, by the adjustable transceiver phase lock loop, the first wire rate clock signal to the serializer.

[0235] In embodiments, a phase lock loop generates the first wire rate clock signal.

[0236] In embodiments, the phase lock loop is on the field programmable gate array.

[0237] In embodiments, the phase lock loop that is part of the field programmable gate array system and not part of the field programmable gate array.

[0238] In embodiments, the step of generating the first wire rate clock signal further includes: (a) processing the second clock signal; (b) providing the first wire rate clock signal based on the processing of the second clock signal; and (c) transmitting, to the serializer, the first wire rate clock signal.

[0239] In embodiments, the sixth frequency corresponds to the third frequency.

[0240] In embodiments, the sixth phase is not aligned with the third phase.

BRIEF DESCRIPTION OF THE DRAWINGS

[0241] Exemplary embodiments of the present invention will be described with reference to the accompanying figures, wherein:

[0242] FIG. 1 is a block diagram of a conventional field programmable gate array;

[0243] FIG. 1A is a block diagram of an exemplary transceiver suitable for use in the field programmable gate array of FIG. 1;

[0244] FIG. 1B is an exemplary block diagram of a Clock Domain Crossing Circuit suitable for use in the field programmable gate array of FIG. 1;

[0245] FIG. 1C illustrates exemplary input output waveforms of the Clock Domain Crossing Circuit of the field programmable gate array of FIG. 1;

[0246] FIG. 2A illustrates an example of a phase difference between the receiver side clock and the transmitter side clock of an FPGA in accordance with an exemplary embodiment of the present invention;

[0247] FIG. 2B illustrates an example of a phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an exemplary embodiment of the present invention;

[0248] FIG. 2C illustrates an example of a phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an exemplary embodiment of the present invention;

[0249] FIG. 2D illustrates an example of an inverted phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an exemplary embodiment of the present invention;

[0250] FIG. 3A is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0251] FIG. 3B is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0252] FIG. 3C is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0253] FIG. 3D is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0254] FIG. 3E is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0255] FIG. 3F is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0256] FIG. 4A is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0257] FIG. 4B is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0258] FIG. 4C is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0259] FIG. 5A is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0260] FIG. 5B is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0261] FIG. 5C is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0262] FIG. 5D is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0263] FIG. 5E is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0264] FIG. 5F is a block diagram of a field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0265] FIG. 6A is an exemplary block diagram of a deserializer suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0266] FIG. 6B is an exemplary circuit diagram of a continuous-time linear equalizer (CTLE) suitable for use in the deserializer of FIG. 6A in accordance with an exemplary embodiment of the present invention;

[0267] FIG. 6C is an exemplary block diagram of a clock and data recovery (CDR) circuit suitable for use in the deserializer of FIG. 6A in accordance with an exemplary embodiment of the present invention;

[0268] FIG. 6D is an exemplary circuit diagram of a decision circuit suitable for use in the deserializer of FIG. 6A in accordance with an embodiment of the present invention;

[0269] FIG. 6E is an exemplary block diagram of a deserializer suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0270] FIG. 7A is an exemplary block diagram of a serializer suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0271] FIG. 7B is an exemplary block diagram of a serializer suitable for use in field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0272] FIG. 8A is an exemplary block diagram of a phase detector suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0273] FIG. 8B is another exemplary block diagram of a phase detector suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0274] FIG. 8C is another exemplary block diagram of a phase detector suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0275] FIG. 8D is another exemplary block diagram of a phase detector suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention;

[0276] FIGs 9A-C are flow charts of a process implementing the field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0277] FIGs. 10A-10B are flow charts of a process for generating a transmitter side clock signal in accordance with an exemplary embodiment of the present invention;

[0278] FIG. 11 is a flow chart of a process for generating a wire rate clock signal in accordance with an embodiment of the present invention;

[0279] FIGs 12A-C are flow charts of a process implementing the field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0280] FIGs. 13A-13B are flow charts of a process for generating a transmitter side clock signal in accordance with an exemplary embodiment of the present invention;

[0281] FIG. 14 is a flow chart of a process for generating a wire rate clock signal in accordance with an embodiment of the present invention;

[0282] FIGs 15A-C are flow charts of a process implementing the field programmable gate array system in accordance with an exemplary embodiment of the present invention;

[0283] FIGs. 16A-16B are flow charts of a process for generating a transmitter side clock signal in accordance with an exemplary embodiment of the present invention; and

[0284] FIG. 17 is a flow chart of a process for generating a wire rate clock signal in accordance with an exemplary embodiment of the present invention.

DETAILED DESCRIPTION

[0285] The present invention generally relates to a field programmable gate array system. In embodiments, the present invention generally relates to a field programmable gate array and an external or internal phase controller providing phase matching between a receiver clock and a transmitter clock used in the field programmable gate array.

[0286] FIG. 1 illustrates an exemplary schematic of a FPGA 100. Examples of currently available FPGAs include the XCVU3P-2FFVC1517E, Intel 1SG280LH3F55E3VG, Xilinx XCVU9P-2FLGA2104E the Vitrex® Ultrascale, the Vitrex® Ultrascale Plus, the Stratix® V, the Stratix® 10, XILINX XC3042, the Intel EP4CE6E22C8LN and the Lattice ICE40LP384-SG32, to name a few.

[0287] In embodiments, FPGA 100 may include an FPGA Core 106 and a number of peripheral systems. In embodiments, the FPGA Core 106 includes 4 main components: logic elements, digital signal processor blocks (“DSP blocks”), clock distribution components, and memories, to name a few, and may generally be referred to as the FPGA core, or simply logic core, 106. In embodiments, the peripheral systems may include CPU cores, reconfiguration controllers, security features, hardened logic functions, FPGA transceiver banks 102, hardened high-speed interface accelerators (e.g., PCIe or 100 GbE controllers, to name a few), general-purpose I/O pins, memory interface controllers, larger memories, analog components (e.g., ADCs or DACs to name a few), and 3D-stacked memories (e.g., HBM), to name a few. The FPGA Transceiver banks 102 receive serial data to be processed from outside the FPGA and then transmit serial data out of the FBGA after being processed by internal circuitry of the FPGA 100. Some FPGA’s may not include FPGA Transceiver banks.

[0288] In embodiments, data may be received by a receiver side of the transceiver banks 102 in the FPGA 100 at rates such as 10 or 25 Gbps, to name a few. In embodiments, rates may be between a range of 9-25 Gbps, 10-25 Gbps, 22-33 Gbps, 33-45 Gbps, 45-60 Gbps, 60-80Gbps, or 80-120 Gbps, to name a few. An exemplary transceiver (including deserializer 104’ and serializer 110’) suitable for use in FPGA 100 is shown in FIG. 1A. In embodiments, the input data may be received from I/O module 120. The input data may then be deserialized, using deserializer 104, for example, and parallelized into parallel data streams, such as 16-64 bits wide at $1/16^{\text{th}}$ to $1/64^{\text{th}}$ of the frequency of the incoming data stream, to name a few. In embodiments, FPGA transceivers may support parallel streams with widths of, for example, 8 bits, 10 bits, 16 bits, 20 bits, 32 bits, 40 bits, 64 bits, 80 bits, 128 bits, and 160 bits (with corresponding clock division), to name a few. In some FPGAs, a physical coding sublayer (PCS) may be used in the transceiver 102. In some FPGAs, the PCS of the transceiver 102 may be bypassed and so that the corresponding PCS functions may be done in the FPGA core 106. After deserialization, data is available for computation in the FPGA logic core 106 where computation is completed. In embodiments, the computation of the data may be computed by receive-side computation 110a of the FPGA core 106. Similarly, data may be computed by the transmit-side computation 110b.

[0289] In embodiments, a REFERENCE CLOCK signal is provided, by Oscillator or Clock Generator 122, to both the deserializer 104 and the serializer 110. The REFERENCE CLOCK signal is received by the serializer 110 via the transceiver PLL 108 (Phase-Locked Loop).

The first receiver side clock signal RXCLOCK, however, is different in both frequency and phase from the REFERENCE CLOCK based on the deserialization process that occurs in the deserializer 104. Similarly, the transmitter clock signal TXCLOCK, while based on the REFERENCE CLOCK signal varies in frequency and phase based on processing that occurs in the serializer 110. As a result, the RXCLOCK signal and TXCLOCK signal will be out of phase. A known solution to this issue is the inclusion of the RX to TX clock domain crossing circuit 112. An exemplary Clock Domain Crossing circuit is suitable for use in FPGA 100 is shown as clock domain crossing circuit 112' in connection with FIG. 1B. As is noted above, the inclusion of the RX to TX clock domain crossing circuit 112 creates a technical problem, introducing an inherent delay in the FPGA 100, which is undesirable. The technical problem of an inherent delay is illustrated in FIG. 1C. FIG. 1C illustrates an example of a phase difference between the receiver side clock and the transmitter side clock of the conventional field programmable gate array of FIG. 1.

[0290] Thereafter, the data is transmitted out of the FPGA 100. After all computation (computation by receive-side computation 110a and/or transmit-side computation 110b) and clock domain crossing (by RX to TX clock domain crossing 112) is completed, the data goes back to the transmit side of the FPGA transceiver 102 to be serialized by the serializer 110 out on an output wire. The serializer 110 (e.g., the transmitter) typically runs off a fast clock generated (e.g., 10 Gbps, 25 Gbps, or a range from 10 Gbps to 25 Gbps, or a range from 1 Gbps to 100 Gbps, to name a few) by the transceiver phase-locked loop 108 within the transceiver bank 102 from a reference clock signal received by oscillator or clock generator 122.

[0291] The receiver (deserializer 104) and transmitter (serializer 110) of the transceiver 102 operate on different clocks that are independently generated within the transceiver 102. The receiver clock domain is typically generated by a clock and data recovery (CDR) circuit from the incoming data stream. The transmitter clock is typically generated by the transceiver phase-locked loop 108. In conventional FPGAs, phase matching or synchronizing is provided using the clock domain crossing circuit 112 that adjusts the phases of the two clock domains. The clock domain crossing circuit 112 may be an asynchronous FIFO or an asynchronous gearbox, to name a few. In embodiments, domain crossing circuit 112 may be a mesochronous clock crossing circuit. In embodiments, clock domain crossing circuit 112 may be instantiated within transceiver 102 of FPGA 100, although this structure has a higher latency cost than implementing it in logic fabric 106 of FPGA 100. As discussed above, a significant drawback of the clock domain crossing circuit

112 is that it adds latency related to the phase difference between the clocks plus the latency of the synchronizers used, and does not perform any computation, such that it slows the effective processing speed of FPGA 100.

[0292] FIGS. 2A-2D illustrate example phase differences between the receiver side clock and the transmitter side clock. It will be understood that other examples of phase differences may be present consistent with the teachings of this disclosure. Generally, when the clocks are aligned, the minimum and maximum delays may be used to determine the time available for the computation of data.

[0293] FIG. 2A illustrates an example of a phase difference between the receiver side clock and the transmitter side clock of an FPGA in accordance with an embodiment. FIG. 2A depicts a phase difference when the clocks are under 360 degrees apart. This embodiment results in minimum delay 2106A and maximum delay 2108A, for which data may be computed. The minimum delay 2106A is from the driving clock edge back to itself, as shown in FIG. 2A.

[0294] FIG. 2B illustrates an example of a phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an embodiment. The phase difference depicted in FIG. 2B shows a phase difference with medium delay 2106B and maximum delay 2108B. The example shown in FIG. 2B shows a minimum delay 2106B of 0. However, in practice, while designers may design for the phase difference in FIG. 2B, the phase difference may end up more similar to the phase differences of FIGS. 2A and/or 2C.

[0295] FIG. 2C illustrates an example of a phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an embodiment. FIG. 2C depicts a phase difference with the clocks are over 360 degrees apart. The time between minimum delay 2106C and maximum delay 2108C may allow for more data computations within the phase difference.

[0296] FIG. 2D illustrates an example of an inverted phase difference between receiver clock and a transmitter clock of an FPGA in accordance with an embodiment. This example of an inverted phase difference between minimum delay 2106D and maximum delay 2108D shows that, even inverted, the phase difference would work similarly to the phase detectors of FIGs. 2A-2C.

[0297] FIG. 3A illustrates a block diagram of a field programmable gate array (FPGA) system in accordance with an embodiment of the present disclosure that provides phase control

while minimizing latency. In embodiments, the system generally includes FPGA 3100 which preferably includes FPGA transceiver banks 3102. In embodiments, the FPGA transceiver banks 3102 includes deserializer 3104 on the receiver end of FPGA 3100, transceiver PLL 3108, and serializer 3110 on the transmitter end of FPGA 3100. Deserializer 3104 may be similar to the deserializer 3104' and deserializer 3104'' discussed below in connection with FIGS. 6A-6E, the descriptions of which applying herein. Serializer 3110 may be similar to serializer 3110' and serializer 3110'' discussed below in connection with FIGS. 7A and 7B respectively, the descriptions of which applying herein. In embodiments, deserializer 3104 receives a serial data stream from the I/O module 3120 and provides deserialized data to the FPGA core 3106. More specifically, the deserializer 3104 will provide parallel data streams to the FPGA core 3106 for processing. As illustrated, this parallel data is provided to the computational logic 3210 where processing and computation takes place. FIG. 3A illustrates computational logic 3210 as a single element with a receiver side and a transmitting side. In embodiments, the computational logic 3210 may be implemented as a plurality of logic elements. In embodiments, when all computation is complete, the resulting data may be provided to serializer 3110 and then transmitted out of FPGA 3100, preferably via I/O module 3120, for example. In embodiments, the I/O module may be a direct soldered cable, on-chip optics, or an on-board optical transceiver, to name a few. Additionally, the I/O module may be an SFP, a QSFP, a micro QSFP, or a QSFP-DD, to name a few.

[0298] In embodiments, the serializer 3110 and deserializer 3104 (SERDES) circuit(s) may contain two major sections: (1) an analog side whose purpose is signal cleaning, and (2) a digital side which turns the analog signal into bits and converts between parallel and serial data streams. In embodiments, the analog side may include a few different types of amplifiers to provide signal cleaning.

[0299] In embodiments, as shown in FIG. 3A, a PLL with phase adjustment 3300 may be located inside the FPGA 3100 fabric with adjustable feedback dividers, which in turn adjust the frequency of the PLL. Alternatively, the PLL with phase adjustment 3300 may comprise a phase adjuster on the output of the loop, which adjusts the phase of the PLL directly. In embodiments, the same description may apply to adjustable transceiver PLLs 3108 and 5108 respectively shown in FIGs. 3B and 5B, but the differences are the location of the PLL inside the FPGA (e.g.,

within the FPGA core 3106 versus outside the FPGA core and within the FPGA transceiver banks 3102, 5102) and the operating frequency.

[0300] As illustrated in FIG. 3A, in embodiments, the first receiver side clock signal RXCLOCK is based on but has a different frequency and phase than the REFERENCE CLOCK signal provided by oscillator 3000 based on the operation of the deserializer 3104, as is discussed above with respect to the serializer 104. In embodiments, the transmitter side clock signal TXCLOCK provided from the serializer 3110 may be provided by transceiver phase locked loop 3108, which is provided inside FPGA 3100, and may be controlled by Phase Lock Loop (PLL) with Phase Adjustment 3300 of the FPGA core 3106. In this manner, the frequency or phase of the transmitter side clock signal TXCLOCK may be adjusted.

[0301] In embodiments, an internal phase controller 3202 is connected to the PLL with Phase Adjustment 3300 and provides control signals to allow for adjustment of the phase of at least the transmitter side clock signal TXCLOCK. The phase of the incoming data, in embodiments, may be adjusted by adjusting the data stream received by I/O module 3120. In embodiments, the internal phase controller 3202 provides control signals based on the phase difference between the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK. In embodiments, the phase difference may be determined using phase detector 3206

[0302] Using the configuration of FIG. 3A, the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK may be sufficiently aligned in phase such that there is no need for the clock domain crossing circuit discussed above, eliminating a technical problem. The technical solution to a technical problem, in embodiments, is shown in the system of FIG. 3A, which provides a wire or a logic path via the controller 3202 and PLL with phase adjustment 3300 to adjust the phase of the transmitter side clock TXCLOCK to correspond to that of the first receiver side clock signal RXCLOCK. Some delays may be introduced in the path including min_delay and max_delay constraints of the wire and components, however, such delays are insignificant compared to the larger delays that are necessarily present when an asynchronous clock domain crossing circuit is used.

[0303] In embodiments, with a phase difference between about 45° and 360° , the min_delay should be set at 0 and the max_delay should be set equal to the time between rising

edges on the receive clock signal and transmit clock signal (as shown in FIGs. 2A and 2B). The difference between 45 ° and 360 ° approximates the minimum amount of time required to safely capture data. In embodiments, the formula for the time is as follows:

$$t_{\min} = t_{\text{setup}} + t_{\text{wire}} + t_{\text{clock-out}} + \Delta t_{\text{jitter}} + t_{\text{skew}}$$

[0304] Referencing the above equation, t_{setup} is the setup time of a flip-flop (i.e., a latch) on FPGA 3100. The t_{wire} is the delay of the, for example, shortest wire (as compared to other wires on the FPGA) on FPGA 3100. In embodiments, the shortest wire is the shortest possible wire. In embodiments, $t_{\text{clock-out}}$ is the clock-to-output time of a flip-flop on the FPGA 3100. In embodiments, Δt_{jitter} is a safety factor for jitter on both clocks. Jitter, for example, is the deviation from true periodicity of a periodic signal from a reference clock. In embodiments, t_{skew} is the skew between clock paths to the two flip-flops on FPGA 3100.

[0305] In embodiments where there is a phase difference with the transmitter clock running less than 45° ahead of the receiver clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, the transmit clock signal may also sample on the opposite edge as the receiving clock signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0306] In embodiments, to avoid instability, the transceiver PLL 3108 preferably runs at the highest bandwidth available from the PLL on the FPGA, while the overall phase locking system including the phase detectors 3206, controller 3202 and PLL with Phase Adjustment 3300 run at a low bandwidth. In embodiments, the highest bandwidth available from the PLL on the FPGA may range between 100 kHz and 10 MHz. In such embodiments, the poles in the on-chip PLLs on the FPGA 3100 are prevented from affecting the gain or phase margin of the overall control loop which may be included in the controller 3202. In embodiments, any loop filter order may be used in the controller 3202 as long as the bandwidth is low enough to avoid interaction of poles in the control system. In embodiments, a low bandwidth may be, for

example, 100Hz- 40kHz, 400Hz and 4kHz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. In embodiments, a second-order loop filter may be used in an effort to improve lock time and phase locking error. In embodiments a third-order filter may be used if the second-order filter is stable. In embodiments, a first-order filter is also an option when the second-order filter has stability problems. In embodiments, other order filters may be used, depending on the internal bandwidth of the FPGA 3100.

[0307] In embodiments, where the bandwidth of the controller 3202 is too low, the receiving clock and the transmitter clock may not track each other closely enough to consider them locked. In embodiment, such tracking issues may be solved by adjusting the min and max delay constraints appropriately to provide a cushion for the clocks being away from the expected phase. In embodiments, a PD (Phase Detector) control system may be provided after the loop filter to aid in resolving tracking issues. In embodiments, tracking issues may be addressed by adding some nonlinearity in the transfer function of the filter. Other solutions may also be possible.

[0308] In the embodiment of FIG. 3A, the controller 3202 utilizes a phase-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative (i.e., the derivative component will act against the loop filter, however, some references refer to this as being a positive direction) and less than 1 (so the path straight from the filter dominates). The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. The bandwidth of the standard PLL loop filter, in some embodiments, may range between 400Hz and 4kHz, 4kHz and 10kHz, 100Hz and 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0309] While similar to the embodiment shown in FIG. 3A, in FIG. 3B, an internal phase controller 3202 is directly connected and provides phase control signals to the adjustable transceiver PLL 3108, which is located in the FPGA transceiver banks 3102 and outside the FPGA

core 3106. FIG. 3B illustrates a block diagram of an FPGA system in accordance with an embodiment of the present invention that provides phase control while minimizing latency wherein the FPGA 3100 has an acceptable phase-controlled adjustable transceiver PLL 3108. This embodiment uses the phase-controlled transceiver PLL directly to control the phase of TXCLOCK. An acceptable phase-control system must have adjustment gain capable of matching phase transients on the incoming data stream to within the timing margin (t_{min}), meaning that the following inequality must be able to be satisfied:

$$\int_0^{\infty} |\Delta t_{pk}(\omega)[1 - LF(\omega)]| d\omega \leq t_{min}$$

[0310] Where $\Delta t_{pk}(\omega)$ is the peak design jitter at that frequency and LF is the transfer function over frequency of the phase locking system consisting of the phase detector 3206, controller 3202, and adjustable transceiver PLL 3108. The transfer function of a phase locked loop relates linearly to the phase control gain at low frequencies, and is given by:

$$LF(\omega) = \frac{K_{APLL}K_{PD}T(\omega)/F(\omega)}{\omega^2 + K_{APLL}K_{PD}T(\omega)/F(\omega)}$$

where K_{APLL} is the phase control gain of adjustable PLL 3108, K_{PD} is the gain of the phase detector 3206, $T(\omega)$ is the transfer function of the PLL controller 3202, and $F(\omega)$ is the transfer function of the feedback network.

[0311] In embodiments, expected functions for $\Delta t_{pk}(\omega)$ may be specified within the protocol specifications for communication protocols used. For example, for 10 Gigabit Ethernet, this is specified in clause 52.8 of the IEEE 802.3 standard.

[0312] In embodiments, the system of FIG. 3B generally includes FPGA 3100 which preferably includes FPGA transceiver banks 3102. In embodiments, the FPGA transceiver banks 3102 includes deserializer 3104 on the receiver end of FPGA 3100, adjustable transceiver PLL 3108, and serializer 3110 on the transmitter end of FPGA 3100. Deserializer 3104 may be similar to the deserializer 3104' and deserializer 3104'' discussed below in connection with FIGS. 6A-6E, the descriptions of which applying herein. Serializer 3110 may be similar to serializer 3110' and serializer 3110'' discussed below in connection with FIGS. 7A and 7B respectively, the descriptions of which applying herein. In embodiments, deserializer 3104

receives a serial data stream from the I/O module 3120 and provides deserialized data to the FPGA core 3106. More specifically, the deserializer 3104 will provide parallel data streams to the FPGA core 3106 for processing. As illustrated, this parallel data is provided to the computational logic 3210 where processing and computation takes place. FIG. 3B illustrates computational logic 3210 as a single element with a receiver side and a transmitting side. In embodiments, the computational logic 3210 may be implemented as a plurality of logic elements. In embodiments, when all computation is complete, the resulting data may be provided to serializer 3110 and then transmitted out of FPGA 3100, preferably via I/O module 3120, for example. In embodiments, the I/O module may be a direct soldered cable, on-chip optics, or an on-board optical transceiver, to name a few. Additionally, the I/O module may be an SFP, a QSFP, a micro QSFP, or a QSFP-DD, to name a few.

[0313] In embodiments, the serializer 3110 and deserializer 3104 (SERDES) circuit(s) may contain two major sections: (1) an analog side whose purpose is signal cleaning, and (2) a digital side which turns the analog signal into bits and converts between parallel and serial data streams. In embodiments, the analog side may include a few different types of amplifiers in order to provide signal cleaning.

[0314] In embodiments, as shown in FIG. 3B, an adjustable transceiver PLL 3108 may be located inside the FPGA 3100 fabric with adjustable feedback dividers, which in turn adjust the frequency of the PLL. Alternatively, the adjustable transceiver PLL 3108 may comprise a phase adjuster on the output of the loop, which adjusts the phase of the PLL directly. Unlike the PLL with phase adjustment 3300 in FIG. 3A, the adjustable transceiver PLL 3108 in FIG. 3B is located outside the FPGA core 3106 and within the FPGA transceiver banks 3102. The adjustable transceiver PLL 3108 in FIG. 3B may also differ from the PLL with phase adjustment 3300 in FIG. 3A in operating frequency.

[0315] As illustrated in FIG. 3B, in embodiments, the first receiver side clock signal RXCLOCK is based on, but has a different frequency and phase than, the REFERENCE CLOCK signal provided by oscillator 3000 based on the operation of the deserializer 3104, as is discussed above with respect to the serializer 104. In embodiments, the transmitter side clock signal TXCLOCK provided from the serializer 3110 may be provided by adjustable transceiver phase

locked loop 3108. In this manner, the frequency or phase of the transmitter side clock signal TXCLOCK may be adjusted.

[0316] In embodiments, an internal phase controller 3202 is connected to the phase adjustment interface of the phase-controlled transceiver PLL 3108 and provides control signals to allow for adjustment of the phase of at least the transmitter side clock signal TXCLOCK. In embodiments, the phase of the incoming data may be adjusted by adjusting the data stream received by I/O module 3120. In embodiments, the internal phase controller 3202 provides control signals based on the phase difference between the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK. In embodiments, the phase difference may be determined using phase detector 3206.

[0317] Using the configuration of FIG. 3B, the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK may be sufficiently aligned in phase such that there is no need for the clock domain crossing circuit discussed above, eliminating a technical problem. The technical solution to a technical problem, in embodiments, is shown in the system of FIG. 3B, which provides a wire or a logic path via the controller 3202 and adjustable transceiver PLL 3108 to adjust the phase of the transmitter side clock TXCLOCK to correspond to that of the first receiver side clock signal RXCLOCK. Some delays may be introduced in the path including min_delay and max_delay constraints of the wire and components. However, such delays are insignificant compared to the larger delays that are necessarily present when an asynchronous clock domain crossing circuit is used.

[0318] In embodiments, with a phase difference between about 45° and 360°, the min_delay should be set at 0 and the max_delay should be set equal to the time between rising edges on the receive clock signal and transmit clock signal (as shown in FIGs. 2A and 2B). The difference between 45° and 360° approximates the minimum amount of time required to safely capture data. In embodiments, the formula for the time is as follows:

$$t_{\min} = t_{\text{setup}} + t_{\text{wire}} + t_{\text{clock-out}} + \Delta t_{\text{jitter}} + t_{\text{skew}}$$

[0319] Referencing the above equation, t_{setup} is the setup time of a flip-flop (i.e., a latch) on FPGA 3100. The t_{wire} is the delay of the, for example, shortest wire (as compared to other wires on the FPGA) on FPGA 3100. In embodiments, the shortest wire is the shortest possible wire. In embodiments, $t_{\text{clock-out}}$ is the clock-to-output time of a flip-flop on the FPGA 3100. In

embodiments, Δt_{jitter} is a safety factor for jitter on both clocks. Jitter, for example, is the deviation from true periodicity of a periodic signal from a reference clock. In embodiments, t_{skew} is the skew between clock paths to the two flip-flops on FPGA 3100.

[0320] In embodiments where there is a phase difference with the transmitter clock running less than 45° ahead of the receiver clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, the transmit clock signal may also sample on the opposite edge as the receiving clock signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0321] In the embodiment of FIG. 3B, to avoid instability, the internal PLL of the adjustable transceiver PLL 3108 preferably runs at the highest bandwidth available from the PLL on the FPGA, while the overall phase locking system including the phase detectors 3206 and controller 3202 runs at a low bandwidth. In embodiments, the highest bandwidth available from the PLL on the FPGA may range between 100 kHz and 10 MHz. In such embodiments, the poles in the adjustable transceiver PLL 3108 are prevented from affecting the gain or phase margin of the off-chip PLL which may be included in the controller 3202. In embodiments, any loop filter order may be used in the controller 3202 as long as the bandwidth is low enough to avoid interaction of poles in the control system. In embodiments, a low bandwidth may be, for example, 100Hz- 40kHz, 400Hz and 4kHz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. In embodiments, a second-order loop filter may be used in an effort to improve lock time and phase locking error. In embodiments a third-order filter may be used if the second-order filter is stable. In embodiments, a first-order filter is also an option when the second-order filter has stability problems. In embodiments, other order filters may be used, depending on the internal bandwidth of the FPGA 3100.

[0322] In embodiments, where the bandwidth of the controller 3202 is too low, the receiving clock and the transmitter clock may not track each other closely enough to consider

them locked. In embodiment, such tracking issues may be solved by adjusting the min and max delay constraints appropriately to provide a cushion for the clocks being away from the expected phase. In embodiments, a PD (Phase Detector) control system may be provided after the loop filter to aid in resolving tracking issues. In embodiments, tracking issues may be addressed by adding some nonlinearity in the transfer function of the filter. Other solutions may also be possible.

[0323] In the embodiment of FIG. 3B, the controller 3202 utilizes a phase-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative (i.e., the derivative component will act against the loop filter, however, some references refer to this as being a positive direction) and less than 1 (so the path straight from the filter dominates). The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. The bandwidth of the standard PLL loop filter, in some embodiments, may range between 400Hz and 4kHz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0324] FIG. 3C illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. Like in the embodiment shown in FIG. 3A, a PLL with phase adjustment 3300a located within the FPGA core 3106 is used by the FPGA system in FIG. 3C. Unlike in the embodiment shown in FIG. 3A, however, an additional control loop, comprising a phase detector 3206b, a controller 3202b, and an external delay element 3300b, may be used to allow multiple deserializers 3104a, 3104b and serializers 3110a, 3110b to be aligned. Multiple deserializers and serializers, as opposed to one of each, allow FPGA 3100 to receive more input data and more output data. In such systems, for every additional receiver that needs to be phase-aligned, an additional control loop is required.

[0325] In embodiments, the additional control loop may use a similar method to the control loop for phase aligning a transmitter to the receiver. However, in embodiments, the

control loop may use a delay element 3300b on the received data rather than adjusting the frequency or phase of an oscillator. The control loop may also include a deserializer 3104b in the feedback path instead of a transceiver PLL. In such embodiments, the required bandwidth may change or cause different types of nonlinearities. Otherwise, the method for phase-aligning additional receivers generally corresponds to the method used to phase align a transmitter and a receiver, as discussed.

[0326] In embodiments, the external delay element 3300b may have an adjustment range at least as wide as one period of the parallel RX clock. This can be accomplished by using a long delay line or a pair of smaller delay lines with a glitch-free switchover circuit to hide the boundary conditions of the delay lines. In embodiments, the delay element 3300b may be implemented with a digital delay line (e.g., the SY89295U from Micrel), or a voltage-controlled delay element (e.g., the HMC910 from Analog devices).

[0327] In embodiments, the additional controller 3202b utilizes a delay-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative, i.e., the derivative component will act against the loop filter (however, some references refer to this as being a "positive" direction) and less than 1 so that the path straight from the filter dominates. The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. In embodiments, the bandwidth of the standard PLL loop filter may range between 400Hz and 4kHz, 4kHz and 10kHz, 100Hz and 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0328] In the embodiment of FIG. 3C, there are three clocks which should be aligned, and the required timing constraints for passing data from one clock domain to another all follow the same pattern. In embodiments where there is a phase difference between any pair of aligned clocks with one clock running less than 45 degrees ahead of the other clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C).

In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, one of the clock signals may also sample on the opposite edge as the signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0329] FIG. 3D illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. Like in the embodiment shown in FIG. 3B, an adjustable transceiver PLL 3108 located within the FPGA transceiver banks 3102 is used by the FPGA system of FIG. 3D. Unlike in the embodiment shown in FIG. 3B, however, an additional control loop similar to the additional control loop in FIG. 3C is used to allow multiple deserializers 3104a, 3104b and serializers 3110a, 3110b to be aligned. In embodiments, the additional control loop may operate in the manner identical to the additional control loop described for FIG. 3C.

[0330] FIG. 3E illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. This embodiment is similar to the embodiment shown in FIG. 3C in almost all aspects, except that the delay element 3300b is internal to the FPGA 3100 in FIG. 3E, unlike the delay element 3300b located outside of the FPGA 3100 in FIG. 3C. In embodiments, the delay element 3300b in FIG. 3E has the same requirements as the external delay element shown in FIG. 3C.

[0331] FIG. 3F illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. This embodiment is similar to the embodiment shown in FIG. 3D in almost all aspects, except that the delay element 3300b is internal to the FPGA 3100 in FIG. 3F, unlike the delay elements 3300b located outside of the FPGA 3100 in FIG. 3D. The delay element 3300b has the same requirements as the external delay element shown in FIG. 3D.

[0332] FIG. 4A is a block diagram of another FPGA system in accordance with an exemplary embodiment of the present invention. The system of FIG. 4A is similar to that of FIG. 3A or 3B, and common components are referred to using the same reference numbers (with

a differing first digit to indicate the Figure - e.g., if the first digit of a reference numeral is “3,” the reference numeral is located on FIG. 3A or 3B) as in FIGs. 3A and 3B. One difference between the system of FIG. 4A and the system of FIGs. 3A and 3B is that the phase detector 4206 is off-chip, i.e., not of the FPGA 4100. Another difference between the system of FIG. 4A and the system of FIGs. 3A and 3B is that the FPGA 4100 includes zero-delay buffer PLLS 4208a, 4208b. Another difference between the system of FIG. 4A and the system of FIGs. 3A and 3B is that an internal phase controller 4202 is operationally connected to frequency or phase adjustable oscillator 4200, which is outside the FPGA 4100, such that a phase or frequency control signal may be transmitted from the internal phase controller 4202 to transceiver PLL 4108 via the frequency or phase-adjustable oscillator 4200.

[0333] Referring back to FIG. 4A, in embodiments, the system generally includes FPGA 4100 which preferably includes FPGA transceiver banks 4102. In embodiments, the FPGA transceiver banks 4102 includes deserializer 4104 on the receiver end of FPGA 4100, transceiver PLL 4108, and serializer 4110 on the transmitter end of FPGA 4100. Deserializer 4104 may be similar to the deserializer 3014' and deserializer 3104'' discussed below in connection with FIGS. 6A-6E, the descriptions of which applying herein. Serializer 4110 may be similar to serializer 3110' and serializer 3110'' discussed below in connection with FIGS. 7A and 7B respectively, the descriptions of which applying herein. In embodiments, deserializer 4104 receives a serial data stream via a first plurality of data pins of a first interface from the I/O module 4120 and provides deserialized data to the FPGA core 4106. More specifically, the deserializer 4104 will provide parallel data streams to the FPGA core 4106 for processing. As illustrated, this parallel data is provided to receiver side computational element 4210a where processing and computation takes place. The resulting data may then be provided to transmitting side computational element 4210b where additional computation and processing may take place. FIG. 4A illustrates computational logic 4210 as a single element. In embodiments, the computational logic 4210 may be implemented as a plurality of logic elements. In embodiments, computational logic 4210 may also include one or more of the following: RAM blocks or dedicated hardened accelerators. In embodiments, when all computation is complete, the resulting data may be provided to serializer 4110 and then transmitted out of FPGA 4100, preferably via I/O module 4120, for example. In embodiments, the I/O module 4120 may be a direct soldered cable, on-chip optics, or an on-board optical transceiver, to name a few. I/O Module 4120, may be, for example,

a Samtec® I/O Module Firefly® I/O Module, to name a few. Additionally, the I/O module may be designed to meet one or more of the following standards: SFP, a QSFP, a micro QSFP, or a QSFP-DD, to name a few.

[0334] In embodiments, FPGA 4100 may include one or more interfaces, such as pins. By way of example, a first interface of the one or more interfaces, may include a first plurality of pins of FPGA 4100. The first plurality of pins may be used to transmit and/or receive data and/or signals. In embodiments, the first plurality of pins may include a first reference clock pin. The first reference clock pin may be operationally connected to deserializer 4104. In embodiments, the first reference clock pin may also be operationally connected to fixed-frequency oscillator 4000 such that a first clock signal having a first phase and a first phase may be transmitted from fixed-frequency oscillator 4000 to deserializer 4104 via the first reference clock pin. In embodiments, the first clock signal may have a frequency between 50 and 800 MHZ.

[0335] In embodiments, the first plurality of pins may also include a second reference clock pin. The second reference clock pin may, in embodiments, be operationally connected to transceiver PLL 4108. The second reference clock pin, in embodiments, may be operationally connected to frequency or phase adjustable oscillator 4200 such that a second clock signal having a second phase and a second frequency may be transmitted from the frequency or phase-adjustable oscillator 4200 to transceiver PLL 4108 via the second reference clock pin. In embodiments, the second reference clock pin may be operationally connected to serializer 4110 such that the second clock signal may be transmitted from the frequency or phase-adjustable oscillator 4200 to serializer 4110 via the second reference clock pin. In embodiments, the second reference clock pin may also receive a first wire rate clock signal.

[0336] In embodiments, the first plurality of pins may also include a first plurality of data pins. The first plurality of data pins may be operationally connected deserializer 4104. In embodiments, the first plurality of data pins may also be operationally connected to I/O module 4120 such that a first serial data stream may be transmitted from external connection 4122 to deserializer via the I/O module 4120 and the first plurality of data pins. In embodiments, the first serial data stream may range between 10 to 25 GBPS.

[0337] In embodiments, the first plurality of pins may also include a second plurality of data pins. The second plurality of data pins may be operationally connected to serializer 4110. In

embodiments, the second plurality of data pins may also be operationally connected to I/O module 4120 such that a second serial data stream may be transmitted from serializer 4110 to the external connection 4122 via the I/O module 4120 and the second plurality of data pins. In embodiments, the second serial data stream may range between 10 to 25 GBPS.

[0338] Although reference is made to separate first reference clock pin, second reference clock pin, first plurality of data pins and second plurality of data pins, in embodiments, each pin may be a fixed-function, fixed-location pin, connected internally through a wire. In embodiments, each pin may be a multiplexed fixed-function pin, connected internally through a multiplexer or crossbar. In embodiments, each pin may be a general purpose I/O pin connected through the FPGA core 4106. In embodiments, one or more pin may be fixed function, fixed location pins, while other pins may be multiplexed fixed function pins and/or a general purpose I/O pin.

[0339] In embodiments, the one or more interfaces may also include at least a second interface. The second interface of the one or more interfaces, may include a second plurality of pins of FPGA 4100. The second plurality of pins may be used to transmit and/or receive data and/or signals. In embodiments, the second plurality of pins may include a first clock output pin. The first clock output pin may be operationally connected to deserializer 4104. In embodiments, the first clock output pin may also be operationally connected to computation logic 4210 such that a first receiver side clock signal is transmitted from the deserializer 4104 to computation logic 4210 via the first clock output pin. Additionally, in some embodiments, the first clock output pin may also be operationally connected to zero-delay buffer PLL 4208a such that the receiver side clock is transmitted from the deserializer 4104 to the zero-delay buffer PLL 4208a via the first clock output pin. In embodiments the first receiver side clock signal may have a frequency ranging between 100-650 MHZ.

[0340] In embodiments, the second plurality of pins may also include a second clock output pin. The second clock output pin may be operationally connected to serializer 4110. In embodiments, the second clock output pin may also be operationally connected to computation logic 4210 such that a transmitter side clock signal is transmitted from the serializer 4110 to computation logic 4210 via the second clock output pin. Additionally, in some embodiments, the second clock output pin may also be operationally connected to zero-delay buffer PLL 4208b such that the transmitter side clock is transmitted from the serializer 4110 to the zero-delay buffer

PLL 4208b via the second clock output pin. In embodiments the transmitter side clock signal may have a frequency ranging between 100-650 MHZ.

[0341] In embodiments, the serializer 4110 and deserializer 4104 (SERDES) circuit(s) may contain two major sections: (a) an analog side whose purpose is signal cleaning, and (2) a digital side which turns the analog signal into bits and converts between parallel and serial data streams. In embodiments, the analog side may include a few different types of amplifiers in order to provide signal cleaning. In embodiments, the adjustable oscillator 4200 may be implemented in a variety of ways. In embodiments, the adjustable oscillator 4200 may be implemented as a voltage controlled oscillator. A voltage controller oscillator may be implemented using a variety of architectures. In embodiments, other types of oscillators may be used including negative-resistance oscillators, Clapp oscillators, Colpitts oscillators, ring oscillators, and varactor-tuned oscillators, to name a few.

[0342] In embodiments, a voltage controller crystal oscillator may be used as the adjustable oscillator 4200, for example, the Si550 from Silicon Labs. In embodiments, a numerically/digitally-controlled oscillator may be used as the adjustable oscillator 4200, which is a digital version of an analog VCO, and may use switched circuit elements or a fixed frequency oscillator and a digital PLL to adjust the frequency.

[0343] In embodiments, the adjustable oscillator 4200 may be implemented with a digital delay line, e.g., the SY89295U from Micrel.

[0344] In embodiments, the adjustable oscillator 4200 may be implemented as a voltage-controlled delay element, e.g., the HMC910 provided by Analog devices.

[0345] As illustrated in FIG. 4A, in embodiments, the first receiver side clock signal RXCLOCK is based on but has a different frequency and phase than the REFERENCE CLOCK signal provided by oscillator 4200 based on the operation of the deserializer 4104, as is discussed above with respect to the serializer 4110. In embodiments, the transmitter side clock signal TXCLOCK provided from the deserializer 4104 may be provided by transceiver phase locked loop 4108, which is provided inside FPGA 4100, and may be controlled by frequency or phase adjustable oscillator 4200, external to FPGA 4100. In this manner, the frequency or phase of the transmitter side clock signal TXCLOCK may be adjusted.

[0346] In embodiments, an internal phase controller 4202 is connected to the frequency or phase adjustable oscillator 4200 and provides control signals to allow for adjustment of the phase of at least the transmitter side clock signal TXCLOCK. The phase of the incoming data, in embodiments, may be adjusted by adjusting the data stream received by I/O module 4120. In embodiments, the internal phase controller 4202 provides control signals based on the phase difference between the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK. In embodiments, the phase difference may be determined using phase detector 4206 and zero-delay buffers, 4208a, 4208b. In embodiments, the zero-delay buffers 4208a, 4208b may be incorporated into the FPGA core 4106 of the FPGA 4100. In embodiments, FPGA core 4106 may not include the zero-delay buffers 4208a, 4208b. In embodiments, zero-delay buffer 4208a may have a reference trace T1 whose length is matched to a length of wire T3 between the I/O pin of FPGA 4100 and external phase detector 4206. Similarly, zero delay buffer 4208b may have a reference trace T2 whose length is matched to a second length of wire T4 between the I/O pin of the FPGA 4100 and the external phase detector 4206. Any length mismatch between reference traces T1 and wire T3 between the I/O pin of the FPGA 4100 and the external phase detector 4206 may introduce a deterministic phase error proportional to the mismatch of the length of the wires. Any length mismatch between reference traces T2 and wire T4 between the I/O pin of the FPGA 4100 and the external phase detector 4206 may introduce a deterministic phase error proportional to the mismatch of the length of the wires.

[0347] In embodiments, the transceiver PLL 4108 may include a second adjustable oscillator. In embodiments, the second adjustable oscillator of the transceiver PLL 4108 may provide the wire rate signal to the serializer 4110 which may be used to provide the transmitter clock signal TX CLOCK. In embodiments, the adjustable oscillator of the transceiver PLL 4108 may be provided outside of the transceiver PLL 4108 and operatively connected to the serializer 4110. In embodiments, where a second adjustable oscillator is provided in the FPGA 4100, the adjustable oscillator 4200 may not be necessary and the output of the controller 4202 may be provided to and used by the second adjustable oscillator to adjust the first wire rate clock signal W.R. CLOCK provided to the serializer 4110 based on the information from the controller. In embodiments, where the second adjustable oscillator is provided on the FPGA 4100 and the adjustable oscillator 4200 is also provided off the FPGA, the delay of the second adjustable oscillator may be set to a constant value and the controller 4202 may provide instructions to the

second adjustable oscillator based on this constant value. In embodiments, the constant value may be zero.

[0348] Using the configuration of FIG. 4A, the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK are sufficiently aligned in phase such that there is no need for the clock domain crossing circuit discussed above, eliminating a technical problem. The technical solution to a technical problem, in embodiments, is shown in the system of FIG. 4A, which provides a wire or a logic path via the controller 4202 and adjustable oscillator 4200 to adjust the phase of the transmitter side clock TMCLOCK to correspond to that of the first receiver side clock signal RXCLOCK. Some delays may be introduced in the path including min_delay and max_delay constraints of the wire and components, however, such delays are insignificant compared to the larger delays that are necessarily present when an asynchronous clock domain crossing circuit is used.

[0349] In embodiments, zero delay buffers 4208a, 4208b may be configured to add a phase offset such that the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK may be provided with any desired fixed phase offset with respect to each other. In such embodiments, any phase difference may be used, depending on the length of the logic path between the clocks and the corresponding delay constraints. In embodiments, with a phase difference between about 45° and 360°, the min_delay should be set at 0 and the max_delay should be set equal to the time between rising edges on the receive clock signal and transmit clock signal (as shown in FIGs. 2A and 2B). The difference between 45° and 360° approximates the minimum amount of time required to safely capture data. In embodiments, the formula for the time is as follows:

$$t_{\min} = t_{\text{setup}} + t_{\text{wire}} + t_{\text{clock-out}} + \Delta t_{\text{jitter}} + t_{\text{skew}}$$

[0350] Referencing the above equation, t_{setup} is the setup time of a flip-flop (i.e., a latch) on FPGA 4100. The t_{wire} is the delay of the, for example, shortest wire (as compared to other wires on the FPGA) on FPGA 4100. In embodiments, the shortest wire is the shortest possible wire. In embodiments, $t_{\text{clock-out}}$ is the clock-to-output time of a flip-flop on the FPGA 4100. In embodiments, Δt_{jitter} is a safety factor for jitter on both clocks. Jitter, for example, is the deviation from true periodicity of a periodic signal from a reference clock. In embodiments, t_{skew} is the skew between clock paths to the two flip-flops on FPGA 4100.

[0351] In embodiments where there is a phase difference with the transmitter clock running less than 45 degrees ahead of the receiver clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, the transmit clock signal may also sample on the opposite edge as the receiving clock signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0352] In embodiments, to avoid instability, both the transceiver PLL 4108 and the zero-delay buffer PLL 4208b preferably run at the highest bandwidth available, while the overall phase locking system including the phase detectors 4206, controller 4202 and oscillator 4200 runs at a low bandwidth. In such embodiments, the poles in the on-chip PLLs on the FPGA 4100 are prevented from affecting the gain or phase margin of the off-chip PLL which may be included in the controller 4202. In embodiments, any loop filter order may be used in the controller 4202 as long as the bandwidth is low enough to avoid interaction of poles in the control system. In embodiments, a low bandwidth may be, for example, 100Hz- 40kHz, 400Hz and 4kHz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. In embodiments, a second-order loop filter may be used in an effort to improve lock time and phaselocking error. In embodiments a third-order filter may be used if the second-order filter is stable. In embodiments, a first-order filter is also an option when the second-order filter has stability problems. In embodiments, other order filters may be used, depending on the internal bandwidth of the FPGA 4100.

[0353] In embodiments, where the bandwidth of the controller 4202 is too low, the receiving clock and the transmitter clock may not track each other closely enough to consider them locked. In embodiment, such tracking issues may be solved by adjusting the min and max delay constraints appropriately to provide a cushion for the clocks being away from the expected phase. In embodiments, a PD control system may be provided after the loop filter to aid in resolving tracking issues. In embodiments, tracking issues may be addressed by adding some nonlinearity in the transfer function of the filter. Other solutions may also be possible.

[0354] In the embodiment of FIG. 4A, the controller 4202 utilizes a phase-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative (i.e., the derivative component will act against the loop filter, however, some references refer to this as being a positive direction) and less than 1 (so the path straight from the filter dominates). The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. The bandwidth of the standard PLL loop filter, in some embodiments, may range between 400Hz and 4kHz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0355] FIG. 4B illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. Like the embodiment shown in FIG. 4A, the embodiment of FIG. 4B uses a frequency or phase adjustable oscillator 4200a located outside the FPGA 4100. Unlike in the embodiment shown in FIG. 4A, an additional control loop, comprising a phase detector 4206b, a controller 4202b, and an external delay element 4200b, is used in the embodiment of FIG. 4B to allow multiple deserializers 4104a, 4104b and serializers 4110a, 4110b to be aligned. For every additional receiver that needs to be phase-aligned, an additional control loop is required.

[0356] In embodiments, the external delay element 4200b may have an adjustment range at least as wide as one period of the parallel RX clock. This can be accomplished by using a long delay line or a pair of smaller delay lines with a glitch-free switchover circuit to hide the boundary conditions of the delay lines. In embodiments, the delay element 4200b may be implemented with a digital delay line (e.g., the SY89295U from Micrel), or a voltage-controlled delay element (e.g., the HMC910 from Analog devices).

[0357] In embodiments, the additional controller 4202b utilizes a delay-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the

FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative, i.e., the derivative component will act against the loop filter (noting, however, that some references refer to this as being a "positive" direction) and less than 1 so that the path straight from the filter dominates. The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. The bandwidth of the standard PLL loop filter, in some embodiments, may range between 400Hz and 4kHz, 4kHz and 10kHz, 100Hz and 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0358] In the embodiment of FIG. 4B, there may be three clocks which should be aligned, and the required timing constraints for passing data from one clock domain to another all follow the same pattern. In embodiments where there is a phase difference between any pair of aligned clocks with one clock running less than 45 degrees ahead of the other clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, one of the clock signals may also sample on the opposite edge as the signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0359] Similar to the system described in connection with FIG. 4A, the system of FIG. 4B may or may not include zero delay buffers 4208a, 4208b, and 4208c. In embodiments, zero-delay buffer 4208a may have a reference trace T1 whose length is matched to a length of wire T4 between the I/O pin of FPGA 4100 and external phase detectors 4206a, 4206b. Similarly, zero delay buffer 4208b may have a reference trace T2 whose length is matched to a second length of wire T5 between the I/O pin of the FPGA 4100 and the external phase detector 4206a. Also, similarly, zero delay buffer 4208c may have a reference trace T3 whose length is matched to a second length of wire T6 between the I/O pin of the FPGA 4100 and the external phase detector 4206b. Any length mismatch between reference traces T1 and wire T4 between the I/O pin of the FPGA 4100

and the external phase detectors 4206a, 4206b may introduce a deterministic phase error proportional to the mismatch of the length of the wires. Any length mismatch between reference traces T2 and wire T5 between the I/O pin of the FPGA 4100 and the external phase detector 4206a may introduce a deterministic phase error proportional to the mismatch of the length of the wires. Any length mismatch between reference traces T3 and wire T6 between the I/O pin of the FPGA 4100 and the external phase detector 4206b may introduce a deterministic phase error proportional to the mismatch of the length of the wires.

[0360] FIG. 4C illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. This embodiment is similar to the embodiment shown in FIG. 4B in almost all aspects, except that the delay element 4200b is internal to the FPGA 4200b, unlike the delay element 4200b located outside of the FPGA 4100 in FIG. 4B. In embodiments, the delay element 4200b in FIG. 4C has the same requirements as the external delay element shown in FIG. 4B.

[0361] FIG. 5A is a block diagram of another FPGA system in accordance with an exemplary embodiment of the present invention. The system of FIG. 5A is similar to that of FIG. 4A, and common components are referred to using the same reference numbers (with a differing first digit to indicate the Figure - e.g., if the first digit of a reference numeral is "4," the reference numeral is located on FIG. 4A) as in FIG. 4A. Like in the system of FIG. 4A, the phase detector 5206 is off-chip, i.e., not of the FPGA 5100, and the FPGA 5100 also includes zero-delay buffer PLLS 5208a, 5208b. On the other hand, the system of FIG. 5A is different from the system of FIG. 4A in that an internal phase controller 5202 is operationally connected to the PLL with phase adjustment 5300 located within the FPGA core 5106, through which the internal phase controller provides phase control to the transceiver PLL 5108.

[0362] FIG. 5A illustrates a block diagram of an FPGA system in accordance with an exemplary embodiment of the present disclosure that provides phase control while minimizing latency. In embodiments, the system generally includes FPGA 5100 which preferably includes FPGA transceiver banks 5102. In embodiments, the FPGA transceiver banks 5102 includes deserializer 5104 on the receiver end of FPGA 5100, transceiver PLL 5108, and serializer 5110 on the transmitter end of FPGA 5100. Deserializer 5104 may be similar to the deserializer 3104' and deserializer 3104'' discussed below in connection with FIGS. 6A-6E, the descriptions of

which applying herein. Serializer 5110 may be similar to serializer 3110' and serializer 3110'' discussed below in connection with FIGS. 7A and 7B respectively, the descriptions of which applying herein. In embodiments, deserializer 5104 receives a serial data stream from the I/O module 5120 and provides deserialized data to the FPGA core 5106. More specifically, the deserializer 5104 will provide parallel data streams to the FPGA core 5106 for processing. As illustrated, this parallel data is provided to the computational logic 5210 where processing and computation takes place. FIG. 5A illustrates computational logic 5210 as a single element with a receiver side and a transmitting side. In embodiments, the computational logic 5210 may be implemented as a plurality of logic elements. In embodiments, when all computation is complete, the resulting data may be provided to serializer 5110 and then transmitted out of FPGA 5100, preferably via I/O module 5120, for example. In embodiments, the I/O module may be a direct soldered cable, on-chip optics, or an on-board optical transceiver, to name a few. Additionally, the I/O module may be an SFP, a QSFP, a micro QSFP, or a QSFP-DD, to name a few.

[0363] In embodiments, the serializer 5110 and deserializer 5104 (SERDES) circuit(s) may contain two major sections: (1) an analog side whose purpose is signal cleaning, and (2) a digital side which turns the analog signal into bits and converts between parallel and serial data streams. In embodiments, the analog side may include a few different types of amplifiers in order to provide signal cleaning.

[0364] In embodiments, as shown in FIG. 5A, a PLL with phase adjustment 5300 may be located inside the FPGA 5100 fabric with adjustable feedback dividers, which in turn adjust the frequency of the PLL. Alternatively, the PLL with phase adjustment 5300 may comprise a phase adjuster on the output of the loop, which adjusts the phase of the PLL directly. In embodiments, the same description may apply to adjustable transceiver PLLs 3108 and 5108 respectively shown in FIGs. 3B and 5B, but the differences are the location of the PLL inside the FPGA (e.g., within the FPGA core 5106 versus outside the FPGA core and within the FPGA transceiver banks 3102, 5102) and the operating frequency.

[0365] As illustrated in FIG. 5A, in embodiments, the first receiver side clock signal RXCLOCK is based on but has a different frequency and phase than the REFERENCE CLOCK signal provided by oscillator 5000 based on the operation of the deserializer 5104, as is discussed

above with respect to the serializer 104. In embodiments, the transmitter side clock signal TXCLOCK provided from the serializer 5110 may be provided by transceiver phase locked loop 5108, which is provided inside FPGA 5100, and may be controlled by PLL with Phase Adjustment 5300 of the FPGA core 5106. In this manner, the frequency or phase of the transmitter side clock signal TXCLOCK may be adjusted.

[0366] As illustrated in FIG. 5A, in embodiments, the first receiver side clock signal RXCLOCK is based on but has a different frequency and phase than the REFERENCE CLOCK signal provided by oscillator 5000 based on the operation of the deserializer 5104, as is discussed above with respect to the serializer 104. In embodiments, the transmitter side clock signal TXCLOCK provided from the serializer 5110 may be provided by transceiver phase locked loop 5108, which is provided inside FPGA 5100, and may be controlled by a PLL with Phase Adjustment 5300 of the FPGA core 5106. In this manner, the frequency or phase of the transmitter side clock signal TXCLOCK may be adjusted.

[0367] In embodiments, an internal phase controller 5202 is connected to the PLL with Phase Adjustment 5300 and provides control signals to allow for adjustment of the phase of at least the transmitter side clock signal TXCLOCK. In embodiments, the phase of the incoming data may be adjusted by adjusting the data stream received by I/O module 5120. In embodiments, the phase difference may be determined using phase detector 5206 which is external to the FPGA. In embodiments, with a phase difference between about 45° and 360°, the min_delay should be set at 0 and the max_delay should be set equal to the time between rising edges on the receive clock signal and transmit clock signal (as shown in FIGs. 2A and 2B). The difference between 45° and 360° approximates the minimum amount of time required to safely capture data. In embodiments, the formula for the time is as follows:

$$t_{\min} = t_{\text{setup}} + t_{\text{wire}} + t_{\text{clock-out}} + \Delta t_{\text{jitter}} + t_{\text{skew}}$$

[0368] Referencing the above equation, t_{setup} is the setup time of a flip-flop (i.e., a latch) on FPGA 3100. The t_{wire} is the delay of the, for example, shortest wire (as compared to other wires on the FPGA) on FPGA 3100. In embodiments, the shortest wire is the shortest possible wire. In embodiments, $t_{\text{clock-out}}$ is the clock-to-output time of a flip-flop on the FPGA 3100. In embodiments, Δt_{jitter} is a safety factor for jitter on both clocks. Jitter, for example, is the

deviation from true periodicity of a periodic signal from a reference clock. In embodiments, t_{skew} is the skew between clock paths to the two flip-flops on FPGA 3100.

[0369] In embodiments where there is a phase difference with the transmitter clock running less than 45 degrees ahead of the receiver clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, the transmit clock signal may also sample on the opposite edge as the receiving clock signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0370] In the embodiment of FIG. 5A, both the transceiver PLL 5108 and the zero-delay buffer PLL 5208b preferably run at the highest bandwidth available from the PLL on the FPGA, while the overall phase locking system including the phase detectors 5206, controller 5202 and PLL with Phase Adjustment 5300 runs at a low bandwidth. In such embodiments, the poles in the adjustable transceiver PLL 5108 are prevented from affecting the gain or phase margin of the off-chip PLL which may be included in the controller 5202. In embodiments, the highest bandwidth available from the PLL on the FPGA may range between 100 kHz and 10 MHz. In embodiments, any loop filter order may be used in the controller 5202 as long as the bandwidth is low enough to avoid interaction of poles in the control system. In embodiments, a low bandwidth may be, for example, 100Hz- 40kHz, 400Hz and 4kHz, 4kHz and 10kHz, 100Hz and 40kHz, 0Hz and 100Hz, to name a few. In embodiments, a second-order loop filter may be used in an effort to improve lock time and phaselocking error. In embodiments a third-order filter may be used if the second-order filter is stable. In embodiments, a first-order filter is also an option when the second-order filter has stability problems. In embodiments, other order filters may be used, depending on the internal bandwidth of the FPGA 5100.

[0371] In embodiments, the one or more interfaces may also include at least a second interface. The second interface of the one or more interfaces, may include a second plurality of pins of FPGA 5100. The second plurality of pins may be used to transmit and/or receive data

and/or signals. In embodiments, the second plurality of pins may include a first clock output pin. The first clock output pin may be operationally connected to deserializer 5104. In embodiments, the first clock output pin may also be operationally connected to computation logic 5210 such that a first receiver side clock signal is transmitted from the deserializer 5104 to computation logic 5210 via the first clock output pin. Additionally, in some embodiments, the first clock output pin may also be operationally connected to zero-delay buffer PLL 5208a such that the receiver side clock is transmitted from the deserializer 5104 to the zero-delay buffer PLL 5208a via the first clock output pin. In embodiments the first receiver side clock signal may have a frequency ranging between 100-650 MHZ.

[0372] In embodiments, the second plurality of pins may also include a second clock output pin. The second clock output pin may be operationally connected to the serializer 5110. In embodiments, the second clock output pin may also be operationally connected to computation logic 5210 such that a transmitter side clock signal is transmitted from the serializer 5110 to computation logic 5210 via the second clock output pin. Additionally, in some embodiments, the second clock output pin may also be operationally connected to zero-delay buffer PLL 5208b such that the transmitter side clock is transmitted from the serializer 5110 to the zero-delay buffer PLL 5208b via the second clock output pin. In embodiments the transmitter side clock signal may have a frequency ranging between 100-650 MHZ.

[0373] The PLL with internal phase adjustment 5300 may be similar to the PLL 3300 in FIG. 3A. It is a component of the FPGA core fabric 5106 which generates a clock of adjustable phase and frequency.

[0374] In embodiments, where the bandwidth of the controller 5202 is too low, the receiving clock and the transmitter clock may not track each other closely enough to consider them locked. In embodiment, such tracking issues may be solved by adjusting the min and max delay constraints appropriately to provide a cushion for the clocks being away from the expected phase. In embodiments, a PD (Phase Detector) control system may be provided after the loop filter to aid in resolving tracking issues. In embodiments, tracking issues may be addressed by adding some nonlinearity in the transfer function of the filter. Other solutions may also be possible.

[0375] In the embodiment of FIG. 5A, the controller 5202 utilizes a phase-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative (i.e., the derivative component will act against the loop filter, however, some references refer to this as being a positive direction) and less than 1 (so the path straight from the filter dominates). The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. The bandwidth of the standard PLL loop filter, in some embodiments, may range between 400Hz and 4kHz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0376] FIG 5B is a block diagram of another FPGA system in accordance with an exemplary embodiment of the present invention. Unlike in the embodiment shown in FIG. 5A, an internal phase controller 5202 in the system of FIG. 5B is directly connected and provides phase control signals to the adjustable transceiver PLL 5108, which is located in the FPGA transceiver banks 5102 and outside the FPGA core 5106.

[0377] FIG. 5B illustrates a block diagram of an FPGA system in accordance with an embodiment of the present disclosure that provides phase control while minimizing latency wherein the FPGA has an acceptable phase-controlled transceiver PLL 5108. This embodiment uses the phase-controlled transceiver PLL directly to control the phase of TXCLOCK. An acceptable phase-control system must have adjustment gain capable of matching phase transients on the incoming data stream to within the timing margin (t_{min}), satisfying the following inequality:

$$\int_0^{\infty} |\Delta t_{pk}(\omega)[1 - LF(\omega)]| d\omega \leq t_{min}$$

[0378] Where $\Delta t_{pk}(\omega)$ is the peak design jitter at that frequency and LF is the transfer function over frequency of the phase locking system consisting of the phase detector 5206, controller 5202, and PLL 5108. Expected functions for $\Delta t_{pk}(\omega)$ are specified within the protocol

specifications for communication protocols used. For 10 Gigabit Ethernet, this is specified in clause 52.8 of the IEEE 802.3 standard.

[0379] In embodiments, the system of FIG. 5B generally includes FPGA 5100 which preferably includes FPGA transceiver banks 5102. In embodiments, the FPGA transceiver banks 5102 includes deserializer 5104 on the receiver end of FPGA 5100, transceiver PLL 5108, and serializer 5110 on the transmitter end of FPGA 5100. Deserializer 5104 may be similar to the deserializer 3104' and deserializer 3104'' discussed below in connection with FIGS. 6A-6E, the descriptions of which applying herein. Serializer 5110 may be similar to serializer 3110' and serializer 3110'' discussed below in connection with FIGS. 7A and 7B respectively, the descriptions of which applying herein. In embodiments, deserializer 5104 receives a serial data stream from the I/O module 5120 and provides deserialized data to the FPGA core 5106. More specifically, the deserializer 5104 will provide parallel data streams to the FPGA core 5106 for processing. As illustrated, this parallel data is provided to the computational logic 5210 where processing and computation takes place. FIG. 5B illustrates computational logic 5210 as a single element with a receiver side and a transmitting side. In embodiments, the computational logic 5210 may be implemented as a plurality of logic elements. In embodiments, when all computation is complete, the resulting data may be provided to serializer 5110 and then transmitted out of FPGA 5100, preferably via I/O module 5120, for example. In embodiments, the I/O module may be a direct soldered cable, on-chip optics, or an on-board optical transceiver, to name a few. Additionally, the I/O module may be an SFP, a QSFP, a micro QSFP, or a QSFP-DD, to name a few.

[0380] In embodiments, the serializer 5110 and deserializer 5104 (SERDES) circuit(s) may contain two major sections: (1) an analog side whose purpose is signal cleaning, and (2) a digital side which turns the analog signal into bits and converts between parallel and serial data streams. In embodiments, the analog side may include a few different types of amplifiers in order to provide signal cleaning.

[0381] In embodiments, as shown in FIG. 5B, an adjustable transceiver PLL 5108 may be located inside the FPGA 5100 fabric with adjustable feedback dividers, which in turn adjust the frequency of the PLL. Alternatively, the adjustable transceiver PLL 5108 may comprise a phase adjuster on the output of the loop, which adjusts the phase of the PLL directly. Unlike the

PLL with phase adjustment 5300 in FIG. 5A, the adjustable transceiver PLL 5108 in FIG. 5B is located outside the FPGA core 5106 and within the FPGA transceiver banks 5102. The adjustable transceiver PLL 5108 in FIG. 5B may also differ from the PLL with phase adjustment 5300 in FIG. 5A in operating frequency.

[0382] As illustrated in FIG. 5B, in embodiments, the first receiver side clock signal RXCLOCK is based on, but has a different frequency and phase than, the REFERENCE CLOCK signal provided by oscillator 5000 based on the operation of the deserializer 5104, as is discussed above with respect to the serializer 104. In embodiments, the transmitter side clock signal TXCLOCK provided from the serializer 5110 may be provided by adjustable transceiver phase locked loop 5108. In this manner, the frequency or phase of the transmitter side clock signal TXCLOCK may be adjusted.

[0383] In embodiments, an internal phase controller 5202 is connected to the phase adjustment interface of the phase-controlled transceiver PLL 5108 and provides control signals to allow for adjustment of the phase of at least the transmitter side clock signal TXCLOCK. The phase of the incoming data, in embodiments, may be adjusted by adjusting the data stream received by I/O module 5120. In embodiments, the internal phase controller 5202 provides control signals based on the phase difference between the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK. In embodiments, the phase difference may be determined using phase detector 5206.

[0384] Using the configuration of FIG. 5B, the receiver clock signal RXCLOCK and the transmitter clock signal TXCLOCK may be sufficiently aligned in phase such that there is no need for the clock domain crossing circuit discussed above, eliminating a technical problem. The technical solution to a technical problem, in embodiments, is shown in the system of FIG. 5B, which provides a wire or a logic path via the controller 5202 and adjustable transceiver PLL 5108 to adjust the phase of the transmitter side clock TXCLOCK to correspond to that of the first receiver side clock signal RXCLOCK. Some delays may be introduced in the path including min_delay and max_delay constraints of the wire and components, however, such delays are insignificant compared to the larger delays that are necessarily present when an asynchronous clock domain crossing circuit is used.

[0385] In embodiments, with a phase difference between about 45° and 360°, the min_delay should be set at 0 and the max_delay should be set equal to the time between rising edges on the receive clock signal and transmit clock signal (as shown in FIGs. 2A and 2B). The difference between 45° and 360° approximates the minimum amount of time required to safely capture data. In embodiments, the formula for the time is as follows:

$$t_{\min} = t_{\text{setup}} + t_{\text{wire}} + t_{\text{clock-out}} + \Delta t_{\text{jitter}} + t_{\text{skew}}$$

[0386] Referencing the above equation, t_{setup} is the setup time of a flip-flop (i.e., a latch) on FPGA 5100. The t_{wire} is the delay of the, for example, shortest wire (as compared to other wires on the FPGA) on FPGA 5100. In embodiments, the shortest wire is the shortest possible wire. In embodiments, $t_{\text{clock-out}}$ is the clock-to-output time of a flip-flop on the FPGA 5100. In embodiments, Δt_{jitter} is a safety factor for jitter on both clocks. Jitter, for example, is the deviation from true periodicity of a periodic signal from a reference clock. In embodiments, t_{skew} is the skew between clock paths to the two flip-flops on FPGA 5100.

[0387] In embodiments where there is a phase difference with the transmitter clock running less than 45° ahead of the receiver clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, the transmit clock signal may also sample on the opposite edge as the receiving clock signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0388] In the embodiment of FIG. 5B, both the transceiver PLL 5108 and the zero-delay buffer PLL 5208b preferably run at the highest bandwidth available from the PLL on the FPGA, while the overall phase locking system including the phase detectors 5206 and controller 5202 runs at a low bandwidth. In such embodiments, the poles in the adjustable transceiver PLL 5108 are prevented from affecting the gain or phase margin of the off-chip PLL which may be included in the controller 5202. In embodiments, the highest bandwidth available from the PLL on the FPGA may range between 100 kHz and 10 MHz. In embodiments, any loop filter order

may be used in the controller 5202 as long as the bandwidth is low enough to avoid interaction of poles in the control system. In embodiments, a low bandwidth may be, for example, 100Hz-40kHz, 400Hz and 4kHz, 4kHz and 10kHz, 100Hz and 40kHz, 0Hz and 100Hz, to name a few. In embodiments, a second-order loop filter may be used in an effort to improve lock time and phaselocking error. In embodiments a third-order filter may be used if the second-order filter is stable. In embodiments, a first-order filter is also an option when the second-order filter has stability problems. In embodiments, other order filters may be used, depending on the internal bandwidth of the FPGA 5100.

[0389] In embodiments, the one or more interfaces may also include at least a second interface. The second interface of the one or more interfaces, may include a second plurality of pins of FPGA 5100. The second plurality of pins may be used to transmit and/or receive data and/or signals. In embodiments, the second plurality of pins may include a first clock output pin. The first clock output pin may be operationally connected to deserializer 5104. In embodiments, the first clock output pin may also be operationally connected to computation logic 5210 such that a first receiver side clock signal is transmitted from the deserializer 5104 to computation logic 5210 via the first clock output pin. Additionally, in some embodiments, the first clock output pin may also be operationally connected to zero-delay buffer PLL 5208a such that the receiver side clock is transmitted from the deserializer 5104 to the zero-delay buffer PLL 5208a via the first clock output pin. In embodiments the first receiver side clock signal may have a frequency ranging between 100-650 MHz.

[0390] In embodiments, the second plurality of pins may also include a second clock output pin. The second clock output pin may be operationally connected to serializer 5110. In embodiments, the second clock output pin may also be operationally connected to computation logic 5210 such that a transmitter side clock signal is transmitted from the serializer 5110 to computation logic 5210 via the second clock output pin. Additionally, in some embodiments, the second clock output pin may also be operationally connected to zero-delay buffer PLL 5208b such that the transmitter side clock is transmitted from the serializer 5110 to the zero-delay buffer PLL 5208b via the second clock output pin. In embodiments the transmitter side clock signal may have a frequency ranging between 100-650 MHz.

[0391] In embodiments, where the bandwidth of the controller 5202 is too low, the receiving clock and the transmitter clock may not track each other closely enough to consider them locked. In embodiment, such tracking issues may be solved by adjusting the min and max delay constraints appropriately to provide a cushion for the clocks being away from the expected phase. In embodiments, a PD (Phase Detector) control system may be provided after the loop filter to aid in resolving tracking issues. In embodiments, tracking issues may be addressed by adding some nonlinearity in the transfer function of the filter. Other solutions may also be possible.

[0392] In the embodiment of FIG. 5B, the controller 5202 utilizes a phase-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative (i.e., the derivative component will act against the loop filter, however, some references refer to this as being a positive direction) and less than 1 (so the path straight from the filter dominates). The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. The bandwidth of the standard PLL loop filter, in some embodiments, may range between 400Hz and 4kHz, 4kHz and 10kHz, 100hz to 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0393] FIG. 5C illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. Like the embodiment shown in FIG. 5A, a PLL with phase adjustment 5300a located within the FPGA core 5106 is used by the FPGA system in FIG. 5C. Unlike in the embodiment shown in FIG. 5A, an additional control loop, comprising a phase detector 5206b, a controller 5202b, and an external delay element 5300b, is used to allow multiple deserializers 5104a, 5104b and serializers 5110a, 5110b to be aligned. For every additional receiver that needs to be phase-aligned, an additional control loop is required.

[0394] In embodiments, the external delay element 5300b may have an adjustment range at least as wide as one period of the parallel RX clock. This can be accomplished by using a long

delay line or a pair of smaller delay lines with a glitch-free switchover circuit to hide the boundary conditions of the delay lines. In embodiments, the delay element 5200b may be implemented with a digital delay line (e.g., the SY89295U from Micrel), or a voltage-controlled delay element (e.g., the HMC910 from Analog devices).

[0395] In embodiments, the additional controller 5202b utilizes a delay-locked loop. In embodiments, a derivative component may be provided in the loop filter to slow down the control loop when the output value has changed recently and reduces the chance that the PLLs on the FPGA will lose lock. In embodiments, the derivative component's coefficient will be negative, i.e., the derivative component will act against the loop filter (noting, however, that some references refer to this as being a "positive" direction) and less than 1 so the path straight from the filter dominates. The loop filter consists of a standard PLL loop filter with bandwidth between 400 Hz and 40 kHz of up to 4th order plus a derivative component that slows down the loop based on recent changes in the filter value. In embodiments, the bandwidth of the standard PLL loop filter may range between 400Hz and 4kHz, 4kHz and 10kHz, 100Hz and 40kHz, 0Hz and 100Hz, to name a few. The extra derivative component helps to keep the other components in the control system in their linear operating regions. The loop filter is represented by DigitalFilter() in the pseudocode provided below.

[0396] Similar to the system described in connection with FIG. 5A, the system of FIG. 5C may or may not include zero delay buffers 5208a, 5208b, and 5208c. In embodiments, zero-delay buffer 5208a may have a reference trace T1 whose length is matched to a length of wire T4 between the I/O pin of FPGA 4100 and external phase detectors 5206a, 5206b. Similarly, zero delay buffer 5208b may have a reference trace T2 whose length is matched to a second length of wire T5 between the I/O pin of the FPGA 5100 and the external phase detector 5206a. Also, similarly, zero delay buffer 5208c may have a reference trace T3 whose length is matched to a second length of wire T6 between the I/O pin of the FPGA 5100 and the external phase detector 5206b. Any length mismatch between reference traces T1 and wire T4 between the I/O pin of the FPGA 5100 and the external phase detectors 5206a, 5206b may introduce a deterministic phase error proportional to the mismatch of the length of the wires. Any length mismatch between reference traces T2 and wire T5 between the I/O pin of the FPGA 5100 and the external phase detector 5206a may introduce a deterministic phase error proportional to the mismatch of the length of the wires. Any length mismatch between reference traces T3 and wire T6 between the I/O pin of the FPGA

5100 and the external phase detector 5206b may introduce a deterministic phase error proportional to the mismatch of the length of the wires.

[0397] In the embodiment of FIG. 5C, there may be three clocks which should be aligned, and the required timing constraints for passing data from one clock domain to another all follow the same pattern. In embodiments where there is a phase difference between any pair of aligned clocks with one clock running less than 45 degrees ahead of the other clock, metastability may occur unless the clocks are treated as being greater than 360 degrees apart (as seen in FIG. 2C). In such embodiments, the min and max delay are set with the min delay greater than the time difference between rising edges and the max delay less than one full clock cycle plus the min delay. In embodiments, one of the clock signals may also sample on the opposite edge as the signal launch edge, but cases are symmetric. In embodiments, a change from positive to negative edge sampling adds an approximate 180 degrees offset. In embodiments, manufacturer analysis tools may add a reasonable jitter margin to account for times when jitter causes temporary misalignment.

[0398] FIG. 5D illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. Like in the embodiment shown in FIG. 5B, an adjustable transceiver PLL 5108 located within the FPGA transceiver banks 5102 is used by the FPGA system of FIG. 3D. Unlike in the embodiment shown in FIG. 5B, an additional control loop similar to the additional control loop in FIG. 5C is used to allow multiple deserializers 5104a, 5104b and serializers 5110a, 5110b to be aligned. In embodiments, the additional control loop in the embodiment of FIG. 5D operates in the manner identical to the additional control loop described for FIG. 5C.

[0399] FIG. 5E illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. This embodiment is similar to the embodiment shown in FIG. 5C in almost all aspects, except that the delay element 5300b is internal to the FPGA 5100, unlike the delay element 5300b located outside of the FPGA 5100 in FIG. 5C. In embodiments, the delay element 5300b in FIG. 5E has the same requirements as the external delay element 5300b shown in FIG. 5C.

[0400] FIG. 5F illustrates a block diagram of another embodiment of an FPGA system in accordance with an exemplary embodiment of the present invention. This embodiment is similar

to the embodiment shown in FIG. 5D in almost all aspects, except that the delay element 5300b is internal to the FPGA 5100, unlike the delay element 5300b located outside of the FPGA 5100 in FIG. 5D. In embodiments, the delay element 5300b in FIG. 5F has the same requirements as the external delay element 5300b shown in FIG. 5D.

[0401] FIG. 6A is an exemplary block diagram of a deserializer suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention. Deserializer 3104', in embodiments, may include an input buffer 6104, a continuous time linear equalizer (CTLE) 6106, a variable gain amplifier (VGA) 6108; voltage adder 6110; decision feedback equalizer (DFE) 6110, clock and data recovery (CDR) 6116, Serial to parallel box 6118, decision circuit 6112, and clock divider 6120. In embodiments, deserializer 3104' may not include one or more of the following components: CTLE 6106, DFE 6114, and/or VGA 6108, to name a few.

[0402] A deserializer circuit accepts a data stream from an input buffer and converts it into a parallel format at a lower bit rate. First, data comes into the chip from the input pins 6102 into an input buffer 6104. In embodiments, the input buffer receives a transmission from an I/O module, such as I/O module 4120. A continuous time linear equalizer (CTLE) 6106 may be used after the input buffer 6104 to improve signal quality by placing a zero near the dominant pole of the transmission medium to cancel the first pole of the system. A variable-gain amplifier (VGA) 6108 may then be used to scale the signal up for further processing. This output is then turned into a binary 0-1 decision by the decision circuit 6112. In embodiments, the decision circuit 6112 includes adder 6110. A decision feedback amplifier may be included to further improve signal integrity by taking the results of the decision circuit, applying a weighting filter, and adding the result to the output from the VGA 6108. When the signal is in the digital domain, a clock and data recovery circuit (CDR) 6116 recovers the phase of the data and create a wire-rate clock that is phase-aligned to the received data. The CDR 6116 may use a reference clock and *a priori* knowledge of the nominal frequency of the data stream to set the frequency of the recovered clock. With a clock aligned to the data stream, which in some embodiments may be a high speed data stream (e.g., 10 Gbps, 25 Gbps, a range from 9-25 Gbps, 10-25 Gbps, 22-33 Gbps, 33-45 Gbps, 45-60 Gbps, 60-80Gbps, 80-120 Gbps, or 1 Gbps-100 Gbps, to name a few) the receiver can use a clock divider 6120 and a serial-to-parallel circuit 6118 to convert the serial data stream

into a lower-frequency than the data stream (e.g., $1/4^{\text{th}}$ of the data rate of the high speed data stream or $1/256^{\text{th}}$ of the data rate of the high speed data stream, to name a few) parallel data stream.

[0403] In embodiments, a decision feedback equalizer 6114 (DFE) may be provided. In embodiments, the decision feedback equalizer may be a filter that subtracts or adds at least n decided bits to cancel inter-symbol interference on the wire. In embodiments, a clock and data recovery circuit may be provided and includes a data phase detector, which may be any of the circuits discussed above, as well as a phase-locked loop circuit.

[0404] FIG. 6B is an exemplary circuit diagram of a continuous-time linear equalizer (CTLE) suitable for use in the deserializer of FIG. 6A in accordance with an exemplary embodiment of the present invention. CTLE 3106'', in some embodiments, places a zero to cancel out the dominant pole of the transmission line for an incoming signal. In embodiments, CTLE 3106'' is a linear filter applied at a receiver, in the case of FIG. 6B, input buffer 6104, that attenuates low-frequency signal components and filters off higher frequencies. The CTLE 3106'' may be adjusted to optimize the ratio of low frequency attenuation to high frequency amplification. In embodiments, a variable gain amplifier may be provided and used to scale the output of the CTLE to as large of a signal as possible. In embodiments, a decision circuit may also be provided.

[0405] FIG. 6C is an exemplary block diagram of a clock and data recovery (CDR) circuit suitable for use in the deserializer of FIG. 6A in accordance with an embodiment of the present invention. In embodiments, CDR 6116' circuit recovers phase information from an incoming data stream. The data stream, in embodiments, may be received by an alexander phase detector 6302. The CDR 6116' may also obtain frequency information from a reference clock, output. In embodiments, the output may determine whether the recovered clock have the same phase as the recovered data.

[0406] FIG. 6D is an exemplary circuit diagram of a decision circuit 6112' suitable for use in the deserializer of FIG. 6A in accordance with an embodiment of the present invention. FIG. 6D illustrates an exemplary embodiment of such a decision circuit 6112' utilizing a StrongARM sense amplifier. In embodiments, any comparator circuit may be used as a decision circuit.

[0407] FIG. 6E illustrates an exemplary embodiment of deserializer 3104''. In embodiments, the deserializer 3104'' may include a receiver PMA 6512 and receiver PCS 6508. The receiver PMA 6512 may include receiver buffer 6504, CDR 6516, and serial to parallel

box 6118'. In embodiments, the receiver buffer 6504 receives serial differential input data 6502. In embodiments, this data is received by an I/O module, such as the I/O module 4120 of FIG. 4A. In embodiments, the data is then received by the CDR 6516 from the receiver buffer 6504. The CDR, in embodiments, transmits the inputted serial data, a serial clock signal, and a parallel clock signal to the serial to parallel box 6118'. The CDR may also transmits the parallel clock data to the receiver PCS 6508. The serial to parallel box 6118', in embodiments, then converts the serial data into parallel data, transmitting the parallel data to the receiver PCS 6508. The receiver PCS 6508 transmits parallel data to the FPGA Core 4106.

[0408] In addition to the components illustrated in FIG. 6E, deserializer 3104'' may also include or be electrically coupled to a continuous-time linear equalizer (CTLE) (*see* FIG. 6B) which is a pure analog circuit that may be used to correct channel issues. In embodiments, the deserializer 3104'' may include a shift register or demultiplexer with a counter.

[0409] FIG. 7A is an exemplary block diagram of a serializer 3110' suitable for use in the field programmable gate array systems of FIGs. 3A-3F, 4A-4C and 5A-5F in accordance with an exemplary embodiment of the present invention. The serializer circuit accepts a clock running at wire rate 4112 (from transceiver PLL 4108) and accepts parallel data (e.g., TX data 7102) to serialize the data. Data is converted from a parallel format to a serial data stream in the parallel to serial box 7104. A feed-forward equalizer (FFE) 7106, which uses the history of bits serialized on the wire to filter out inter-symbol interference, may be included to improve signal integrity. Finally, the serializer outputs the serial data stream to a transmission medium using an output buffer 7114. The serializer also generates a parallel clock (TX Clk 7110), that operates at a lower speed than the data stream (e.g., 100-400 MHz, 100-600 MHz, to name a few), for use by other components using either a simple clock divider 7108 or a more complex clock generation block which can contain dividers and phase shifting elements for aligning multiple transmitters.

[0410] FIG. 7B illustrates an exemplary embodiment of serializer 3110''. As discussed above with respect to FIGs. 4A and 7A, serializer 3110'' receives parallel data streams from the FPGA core 4106 and serializes them for transmission out of the FPGA 4100. In embodiments, serializer 3110'' may include transmitter PCS 7206, clock generation block 7210, and transmitter PMA 7216. In embodiments, transmitter PMA 7216 may include parallel to serial box 7104' and transmitter buffer 7214. The transmitter PCS 7206 may receive parallel data from FPGA

core 4106. In embodiments, the parallel data is then transmitted to the parallel to serial box 7104'. The clock generation block 7210 may receive a wire-rate clock signal 7112. The clock generation block 7210, in embodiments, may split the signal in to a parallel clock signal and serial clock signal, both the parallel and serial signals being transmitted to the parallel to serial box 7104'. The parallel to serial box 7104' may covert the data from parallel to serial, transmitting the serial differential output data 7218 to the transmitter buffer 7214. Then, in embodiments, the transmitter buffer 7214 outputs the serial differential output data 7218.

[0411] In embodiments the serializer 3110'' may be a shift register or a multiplexer with a counter. In embodiments, the serializer 3110'' may include additional components, such as a feed forward equalizer (FFE) which uses the last n bits to cancel inter symbol interference on the wire. In embodiments, a buffer amplifier may be included which provides variable gain to allow adjustable voltage swing on the output of the transmitter. In embodiments, a clock divider may be provided. In embodiments, the clock divider may generate a low-speed clock (e.g., 100-400 MHz, 100-600 MHz, to name a few) for the serializer and the PMA/PCS. In embodiments, the clock divider is typically provided using a counter. In embodiments, the clock generation block 7210 might also include a clock phase adjustment circuit to allow multiple transmitter lanes to be phase-aligned.

[0412] Referring to FIGS. 8A-8D, in embodiments, the phase detector 4206 may be an analog, single bit phase detector which may be implemented using a variety of circuit components including (1) an XOR gate; (2) S-R flip-flop; (3) D flip-flop; (4) Edge-triggered JK flip-flop; (5) Gilbert cell multiplier and/or (6) Diode ring mixer, to name a few. FIG. 8A illustrates an exemplary embodiment of a phase detector 3206' that utilizes D flip-flops. FIG. 8B illustrates another exemplary embodiment of a phase detector 3206'' that utilizes S-R flip-flops. FIG. 8C is another exemplary block diagram of a phase detector 3206''' suitable for use in the field programmable gate array system of FIG. 4A in accordance with an embodiment of the present invention. FIG. 8D is another exemplary block diagram of a phase detector 3206'''' suitable for use in the field programmable gate array system of FIG. 4A in accordance with an embodiment of the present invention. Other than a basic phase detector, a time-to-digital converter (TDC) can be used to detect the phase offset of the clocks. FIG. 8C shows a Vernier TDC and FIG. 8D shows a parallel delay line TDC as examples. The Vernier TDC uses a pair of unequal delay lines to delay the two signals by varying amounts and uses D-type flip-flops to quantify the phase difference

between the two signals at multiple points along the delay line. The parallel delay line TDC uses a set of simple phase detectors with the two input signals delayed by varying amounts to quantify the phase difference between the two signals. In both cases, a decoding circuit is used to translate the results of the individual phase detection elements into a phase offset.

[0413] In embodiments, the phase detector 4206 may be a multi-bit phase detector, sometimes referred to as a time-to digital converter (TDC). In embodiments, such a phase detector may be a counter-based TDC that counts up the time between START and STOP. In embodiments, such a phase detector may be an interpolator TDC in which time measurement may be performed by measuring a voltage difference (e.g., by using a ramp wave and sampling at two points or by charging a capacitor). In embodiments, a phase detector may be a Vernier TDC as shown in FIG. 8C.

[0414] In embodiments the phase detector 4206 may be implemented using a tapped delay line TDC. In embodiments, the phase detector 4206 may be implemented using a metastability-based phase detector. In embodiments, the metastability-based phase detector is similar to a D flip-flop phase detector but includes an averaging filter. In embodiments, a parallel-delay-line TDC may be used to implement the phase detector 4206. FIG. 8D illustrates an example of a parallel-delay-line TDC. In embodiments, the phase detector may be implemented as a pulse-shrinking TDC. Such a pulse-shrinking TDC may generate a pulse and then send it circularly through an engineered delay line to shrink it until it is gone, count the number of times it goes through the pulse-shrinking circuit.

[0415] In embodiments, the phase detector may be implemented as a scrambling TDC. Scrambling TDCs may be implemented with added digital noise shaping to suppress errors. In embodiments, the phase detector 4206 may be implemented as a PLL/DLL-based TDC. In such an embodiment, the phase detector may lock a digital PLL to the incoming feedback signal and record the internal control code.

[0416] In embodiments, all of the phase detector embodiments discussed above may be combined with or connected to a low-pass filter and an analog to digital converter (ADC). In embodiments, other examples of phase detectors may be used consistent with the teachings of this disclosure.

[0417] The pseudo code shown below implements the control loop inside the PLL or DLL controller (e.g., 3202 in FIGs. 3A-3B, 4202 in FIG. 4A, or 5202 in FIGs. 5A-5B) and communicates with the host in accordance with an exemplary embodiment of the present invention. In embodiments, the pseudocode shown below, or a similar pseudocode is run by the FPGA or a soft processor programmed on the FPGA and uses an interrupt- or event-based system to run the control algorithm for either the PLL or DLL paths on the device. The main control loop is triggered on every sample of the internal ADC.

Begin:

Set up peripherals
 Program initial configuration
 Set up for periodic free-running measurement from the TDC
 Wait

On Periodic Interrupt:

Read TDC code into Window[0]
 ControlCode = DigitalFilter(Window)
 Read MODE pin to Mode

If Mode = PLL_MODE then:

Output ControlCode to PLL frequency adjustment interface

Else:

Output ControlCode to PLL phase adjustment interface

Shift Window array by 1

[0418] FIGs 9A-C, 10A-B and 11 are flow charts of a process implementing the field programmable gate array system in accordance with an exemplary embodiment of the present invention. In embodiments, the process described in the flow charts of FIGs. 9A-C, 10A-B and 11 may be implemented by the field programmable gate array system shown in FIG. 4A. The field programmable gate array system, including the field programmable gate array and the components thereof, may be similar to the field programmable gate array systems of FIG. 4A, the descriptions of which applying herein.

[0419] The process of FIGs. 9A-9C may begin at step S902. Referring to FIG. 9A, at step S902, a first serial data stream is received by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system. In embodiments, the

first serial data stream may include market data. In embodiments, market data may be price and trade-related data for a financial instrument reported by a trading venue (i.e., a stock exchange).

[0420] At a step S904, a first clock signal having a first frequency and a first phase is received by a first reference clock in in the first interface. In embodiments, step S904 may be performed before step S902. In embodiments step S904 may be performed contemporaneously with step S902.

[0421] The process of FIGs. 9A-9C may continue with a step S906. At step S906, the first plurality of data pins of the first interface may transmit the first serial data stream to a deserializer in the field programmable gate array.

[0422] At a step S908, the first reference clock pin in the first interface may transmit the first clock signal to the deserializer. In embodiments, step S908 may be performed before step S906. In embodiments step S908 may be performed contemporaneously with step S906.

[0423] At a step S910, a first receiver side clock signal may be generated by the deserializer. In embodiments, the first receiver side clock signal may have a second frequency and a second phase. In embodiments, the second frequency is different from the first frequency. In embodiments, the second frequency corresponds to the first frequency. In embodiments, corresponding may refer to the frequencies being the same frequency. In embodiments corresponding may also refer to frequencies being close (e.g., within an acceptable range in the art) to the same frequencies. In embodiments, the first phase and the second phase may not be aligned. In embodiments the first phase and the second phase are aligned. In embodiments, a difference between the first phase and the second phase is below a threshold level. In embodiments, the deserializer generates the first receiver clock signal based at least in part on the first clock signal.

[0424] At a step S912, the first serial data stream received by the deserializer may be converted, by the deserializer, into a first plurality of data streams. In embodiments, the first plurality of data streams may include a first amount of data streams. In embodiments, the first amount of data streams is equal to eight (8) data streams. In embodiments, the first amount of data streams is equal to ten (10) data streams. In embodiments, the first amount of data streams is equal to sixteen (16) data streams. In embodiments, the first amount of data streams is equal to twenty (20) data streams. In embodiments, the first amount of data streams is equal to thirty-two (32)

data streams. In embodiments, the first amount of data streams is equal to forty (40) data streams. In embodiments, the first amount of data streams is equal to sixty-four (64) data streams. In embodiments, the first amount of data streams is equal to eighty (80) data streams. In embodiments, the first amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the first amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the first amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the first amount of data streams is equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the first amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0425] At a step S914, the first receiver side clock signal is transmitted from the deserializer to computational circuitry in the field programmable gate array.

[0426] At a step S916, the first plurality of data streams is transmitted from the deserializer to the computational circuitry. In embodiments, the first plurality of data streams includes a first plurality of data items. In embodiments, step S916 may be performed before step S914. In embodiments step S916 may be performed contemporaneously with step S914.

[0427] At a step S918, the first receiver side clock signal is transmitted from the deserializer via a first clock output pin on a second interface of the field programmable gate array to a phase detector of the field programmable gate array system which is not on the field programmable gate array. In embodiments, the transmission of the first receiver side clock signal is also via a first zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the first clock output pin of the second interface.

[0428] At a step S920, a first transmitter side clock signal is generated by the field programmable gate array system. In embodiments, the first transmitter side clock signal has a third frequency and a third phase. In embodiments, the third frequency corresponds to the second frequency. In embodiments the third phase may be aligned with the second phase. In embodiments, the third phase and the second phase may not be aligned. In embodiments, the third phase and the second phase may have a difference in phases that is less than a second threshold level. In embodiments, the first transmitter side clock signal is generated by performing the following steps until a first output of the phase detector is below a first threshold.

[0429] Referring to FIG. 10A, generating the first transmitter side clock signal may begin at step S1002. At step S1002, a second clock signal is generated by an adjustable oscillator in the field programmable gate array system. In embodiments, the second clock signal may have a fourth frequency and a fourth phase.

[0430] The process of FIGs. 10A-B may continue at a step S1004. At step S1004, a first wire rate clock signal having a fifth phase and a fifth frequency is generated. In embodiments, the generation of the first wire rate clock signal may be based in part on the second clock signal. In embodiments the fifth frequency is a rational multiple of the fourth frequency. In embodiments the fifth frequency is equal to x times the fourth frequency where x is the second amount of data streams. In embodiments the fifth frequency is equal to x times the frequency of the of the transmitter side clock signal where x is half of the second amount of data streams.

[0431] In embodiments, the generation of the first wire rate clock signal may be performed with the following steps. Referring to FIG. 11, at a step S1102, the second clock signal is received from the adjustable oscillator at a transceiver phase lock loop via a second reference clock pin in the first interface. At a step S1104, the second clock signal is processed by the transceiver phase lock loop. As a step S1106, the first wire rate clock signal is provided by the transceiver phase lock loop. The providing of the first wire rate clock signal, in embodiments, may be based at least in part on the processing of the received clock signal. Once the first wire rate clock signal is provided, at a step S1108, the first wire rate clock signal is transmitted by the transceiver phase lock loop to a serializer on the field programmable gate array. In embodiments, the first wire rate clock is generated by a phase lock loop. In embodiments, the phase lock loop that generates the first wire rate clock signal is on field programmable gate array. In embodiments, the phase lock loop that generates the first wire rate clock signal is part of the field programmable gate array system and not part of the field programmable gate array.

[0432] In embodiments, the generation of the first wire rate clock signal may include processing the second clock signal. Once the second clock signal is processed, the first wire rate clock signal may be provided. The providing of the first wire rate clock signal, in embodiments, is based at least in part on the processing of the second clock signal. After providing the first wire rate clock signal, in embodiments, the first wire rate clock signal may be transmitted to the serializer.

[0433] Referring back to FIG. 10A, at a step 1006, an interim transmitter side clock signal having a sixth frequency and a sixth phase is generated by the serializer in the field programmable gate array. In embodiments, the sixth frequency corresponds to the third frequency. In embodiments the sixth phase may be aligned with the third phase. In embodiments, the sixth frequency may correspond to the third frequency and the sixth phase may not be aligned with the third phase. In embodiments, the sixth phase and the third phase may not be aligned. In embodiments, the third phase and the sixth phase may have a difference in phases that is less than a second threshold level.

[0434] At a step S1008, the interim transmitter side clock signal is transmitted from the serializer via a second clock output pin of the second interface to the phase detector. In embodiments, the transmission of the interim transmitter side clock is also via a second zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the second clock output in of the second interface.

[0435] The process of FIGs. 10A-10B may continue with at a step S1010. Referring to FIG. 10B, at a step S1010, a first output is generated by the phase detector. The first output, in embodiments, is based at least on a comparison of the first receiver side clock signal and the interim side clock signal. The first output, in embodiments, may include information indicating the phase differences (if there is any) between the first receiver side clock and the interim side clock signal. Additionally, in embodiments, the first output may include information indicating a difference (if there is any) of frequencies between the first receiver side clock signal and the interim side clock signal.

[0436] At a step S1012, the first output may be transmitted from the phase detector to a phase controller of the field programmable gate array system, which may be placed within the field programmable gate array.

[0437] At a step S1014, interim adjustment information is determined by the phase controller. In embodiments, the interim adjustment information may be based at least in part on the first output. For example, the interim adjustment information may indicate necessary adjustments to align the phases of the first receiver side clock signal and the interim side clock signal. As another example, the interim adjustment information may indicate necessary

adjustments to align the frequencies of the first receiver side clock signal and the interim side clock signal.

[0438] At a step S1016, the interim adjustment information is transmitted from the phase controller to the adjustable oscillator. In embodiments, once the interim adjustment information is received, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information. The adjustment of the second clock signal, in embodiments, may change the phase of the second clock signal. In embodiments, the interim adjustment information indicates a desired phase. In embodiments, the interim adjustment information indicates a desired frequency. In embodiments, the interim adjustment information indicates a change in phase. In embodiments, the interim adjustment information indicates a change in frequency. In embodiments, the adjustment information includes a voltage. In embodiments, the adjustment information includes a digital transmission. For example, the adjustment information may be a command over a serial bus (e.g., I2C or SPI) that adjusts a clock divider or phase rotator. As another example, the adjustment information may trigger a set of parallel digital wires for "frequency/phase up," "frequency/phase down," and/or "frequency/phase step." In embodiments, the adjustment of the second clock signal may change the frequency of the second clock signal.

[0439] In embodiments, steps S1002 through steps S 1016 are repeated until the first output of the phase detector is below the first threshold level. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have phases that are aligned. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have frequencies that correspond to one another.

[0440] Referring back to FIG. 9B, once the first output of the phase detector is below a first threshold level, at a step S922, the serializer may transmit the first transmitter side clock signal to the computational circuitry. At a step S924, a first set of operations performed by the computational circuitry on at least a portion of the first plurality of data items to generate a second plurality of data streams. In embodiments, the first operation includes a trading algorithm. In embodiments the trading algorithm may include the parsing the market data. Once the market data is parsed, mathematical operations are performed at a portion of the market data. After the mathematical operations are performed, order packets are generated using at least an output of the mathematical operations. In embodiments, the first set of operations includes at least one of the

following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

[0441] In embodiments, at least a portion of the first set of operations is performed prior to step S922. In embodiments, at least a portion of the first set of operations is performed after step S922. In embodiments all of the first set of operations is performed after step S922.

[0442] In embodiments, the second plurality of data streams may include a second amount of data streams. In embodiments, the second amount of data streams may be the same as the first amount of data streams. In embodiments, the second amount of data streams is equal to eight (8) data streams. In embodiments, the second amount of data streams is equal to ten (10) data streams. In embodiments, the second amount of data streams is equal to sixteen (16) data streams. In embodiments, the second amount of data streams is equal to twenty (20) data streams. In embodiments, the second amount of data streams is equal to thirty-two (32) data streams. In embodiments, the second amount of data streams is equal to forty (40) data streams. In embodiments, the second amount of data streams is equal to sixty-four (64) data streams. In embodiments, the second amount of data streams is equal to eighty (80) data streams. In embodiments, the second amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the second amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the second amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the second amount of data streams is equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the second amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0443] At a step S926, the second plurality of data streams is transmitted from the computational circuitry to the serializer. Once received by the serializer, at a step S928, the serializer converts the second plurality of parallel data streams into the second serial data stream. The second serial data stream, in embodiments, includes trading data. Trading data, for example, may be any data related to purchasing or selling of stocks, commodities, goods, and/or services.

[0444] At a step S930, the second serial data stream may be transmitted from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface. In embodiments, the second serial data stream is transmitted from the serializer on the field programmable gate array to an input/output module of the field gate array system but not on

the field gate array. The second serial data stream may then be transmitted from the input/output module off the field gate array system.

[0445] FIGs 12A-C, 13A-B and 14 are exemplary flow charts of a process implementing the field programmable gate array system in accordance with another exemplary embodiment of the present invention. In embodiments, the process described in the flow charts of FIGs. 12A-C, 13A-B and 14 may be implemented by the field programmable gate array system shown in FIG. 3A or FIG. 5A. The field programmable gate array system, including the field programmable gate array and the components thereof, may be similar to the field programmable gate array systems of FIG. 3A and 5A, the descriptions of which applying herein.

[0446] The process of FIGs. 12A-12C may begin at step S1202. Referring to FIG. 12A, at step S1202, a first serial data stream is received by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system. In embodiments, the first serial data stream may include market data. In embodiments, market data may be price and trade-related data for a financial instrument reported by a trading venue (i.e., a stock exchange).

[0447] At a step S1204, a first clock signal having a first frequency and a first phase is received by a first reference clock in in the first interface. In embodiments, step S1204 may be performed before step S1202. In embodiments, step S1204 may be performed contemporaneously with step S1202.

[0448] The process of FIGs. 12A-12C may continue with a step S1206. At step S1206, the first plurality of data pins of the first interface may transmit the first serial data stream to a deserializer in the field programmable gate array.

[0449] At a step S1208, the first reference clock pin in the first interface may transmit the first clock signal to the deserializer. In embodiments, step S1208 may be performed before step S1206. In embodiments step S1208 may be performed contemporaneously with step S1206.

[0450] At a step S1210, a first receiver side clock signal may be generated by the deserializer. In embodiments, the first receiver side clock signal may have a second frequency and a second phase. In embodiments, the second frequency is different from the first frequency. In embodiments, the second frequency corresponds to the first frequency. In embodiments,

corresponding may refer to the frequencies being the same frequency. In embodiments corresponding may also refer to frequencies being close (e.g., within an acceptable range in the art) to the same frequencies. In embodiments, the first phase and the second phase may not be aligned. In embodiments the first phase and the second phase are aligned. In embodiments, a difference between the first phase and the second phase is below a threshold level. In embodiments, the deserializer generates the first receiver clock signal based at least in part on the first clock signal.

[0451] At a step S1212, the first serial data stream received by the deserializer may be converted, by the deserializer, into a first plurality of data streams. In embodiments, the first plurality of data streams may include a first amount of data streams. In embodiments, the first amount of data streams is equal to eight (8) data streams. In embodiments, the first amount of data streams is equal to ten (10) data streams. In embodiments, the first amount of data streams is equal to sixteen (16) data streams. In embodiments, the first amount of data streams is equal to twenty (20) data streams. In embodiments, the first amount of data streams is equal to thirty-two (32) data streams. In embodiments, the first amount of data streams is equal to forty (40) data streams. In embodiments, the first amount of data streams is equal to sixty-four (64) data streams. In embodiments, the first amount of data streams is equal to eighty (80) data streams. In embodiments, the first amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the first amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the first amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the first amount of data streams is equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the first amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0452] At a step S1214, the first receiver side clock signal is transmitted from the deserializer to computational circuitry in the field programmable gate array.

[0453] At a step S1216, the first plurality of data streams is transmitted from the deserializer to the computational circuitry. In embodiments, the first plurality of data streams includes a first plurality of data items. In embodiments, step S1216 may be performed before step S1214. In embodiments step S1216 may be performed contemporaneously with step S1214.

[0454] At a step S1218, the first receiver side clock signal is transmitted from the deserializer to a phase detector of the field programmable gate array system. The phase detector may or may not be placed on the field programmable gate array. If the phase detector is not on the field programmable gate array, the first receiver side clock signal is transmitted from the deserializer to the phase detector via a first clock output pin on a second interface of the field programmable gate array. In embodiments, the transmission of the first receiver side clock signal to the phase detector may also be via a first zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the first clock output pin of the second interface.

[0455] At a step S1220, a first transmitter side clock signal is generated by the field programmable gate array system. In embodiments, the first transmitter side clock signal has a third frequency and a third phase. In embodiments, the third frequency corresponds to the second frequency. In embodiments the third phase may be aligned with the second phase. In embodiments, the third phase and the second phase may not be aligned. In embodiments, the third phase and the second phase may have a difference in phases that is less than a second threshold level. In embodiments, the first transmitter side clock signal is generated by performing the following steps until a first output of the phase detector is below a first threshold.

[0456] Referring to FIG. 13A, generating the first transmitter side clock signal may begin at step S1302. At step S1302, a second clock signal is generated by a phase lock loop with phase adjustment in the field programmable gate array system. In embodiments, the phase lock loop with phase adjustment is on the field programmable gate array. In embodiments, the phase lock loop with phase adjustment is located within the core of the field programmable gate array. In embodiments, the second clock signal may have a fourth frequency and a fourth phase.

[0457] The process of FIGs. 13A-B may continue at a step S1304. At step S1304, a first wire rate clock signal having a fifth phase and a fifth frequency is generated. In embodiments, the generation of the first wire rate clock signal may be based in part on the second clock signal. In embodiments the fifth frequency is a rational multiple of the fourth frequency. In embodiments the fifth frequency is equal to x times the fourth frequency where x is the second amount of data streams. In embodiments the fifth frequency is equal to x times the frequency of the first transmitter side clock signal where x may be half of the second amount of data streams.

[0458] In embodiments, the generation of the first wire rate clock signal may be performed with the following steps. Referring to FIG. 14, at a step S1402, the second clock signal is received from the phase lock loop with phase adjustment at a transceiver phase lock loop via a second reference clock pin in the first interface. At a step S1404, the second clock signal is processed by the transceiver phase lock loop. As a step S1406, the first wire rate clock signal is provided by the transceiver phase lock loop. The providing of the first wire rate clock signal, in embodiments, may be based at least in part on the processing of the received second clock signal. Once the first wire rate clock signal is provided, at a step S1408, the first wire rate clock signal is transmitted by the transceiver phase lock loop to a serializer on the field programmable gate array. In embodiments, the first wire rate clock signal is generated by a phase lock loop. In embodiments, the phase lock loop that generates the first wire rate clock signal is on field programmable gate array. In embodiments, the phase lock loop that generates the first wire rate clock signal may be part of the field programmable gate array system and not part of the field programmable gate array.

[0459] In embodiments, the generation of the first wire rate clock signal may include processing the second clock signal. Once the second clock signal is processed, the first wire rate clock signal may be provided. The providing of the first wire rate clock signal, in embodiments, is based at least in part on the processing of the second clock signal. After providing the first wire rate clock signal, in embodiments, the first wire rate clock signal may be transmitted to the serializer.

[0460] Referring back to FIG. 13A, at a step 1306, an interim transmitter side clock signal having a sixth frequency and a sixth phase is generated by the serializer in the field programmable gate array. In embodiments, the sixth frequency corresponds to the third frequency. In embodiments the sixth phase may be aligned with the third phase. In embodiments, the sixth frequency may correspond to the third frequency and the sixth phase may not be aligned with the third phase. In embodiments, the sixth phase and the third phase may not be aligned. In embodiments, the third phase and the sixth phase may have a difference in phases that is less than a second threshold level.

[0461] At a step S1308, the interim transmitter side clock signal is transmitted from the serializer to the phase detector, which may or may not be on the field programmable gate array. If the phase detector is not on the field programmable gate array, the interim transmitter side clock

signal may be transmitted from the serializer to the phase detector via a second clock output pin of the second interface. In embodiments, the interim transmitter side clock signal may also be transmitted via a second zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the second clock output in of the second interface.

[0462] The process of FIGs. 13A-13B may continue with at a step S1310. Referring to FIG. 13B, at a step S1310, a first output is generated by the phase detector. The first output, in embodiments, is based at least on a comparison of the first receiver side clock signal and the interim side clock signal. The first output, in embodiments, may include information indicating the phase differences (if there is any) between the first receiver side clock and the interim side clock signal. Additionally, in embodiments, the first output may include information indicating a difference (if there is any) of frequencies between the first receiver side clock signal and the interim side clock signal.

[0463] At a step S1312, the first output may be transmitted from the phase detector to a phase controller of the field programmable gate array system, which may be placed within the field programmable gate array.

[0464] At a step S1314, interim adjustment information is determined by the phase controller. In embodiments, the interim adjustment information may be based at least in part on the first output. For example, the interim adjustment information may indicate necessary adjustments to align the phases of the first receiver side clock signal and the interim side clock signal. As another example, the interim adjustment information may indicate necessary adjustments to align the frequencies of the first receiver side clock signal and the interim side clock signal.

[0465] At a step S1316, the interim adjustment information is transmitted from the phase controller to the phase lock loop with phase adjustment. In embodiments, once the interim adjustment information is received, the phase lock loop with phase adjustment adjusts the second clock signal based on the interim adjustment information. The adjustment of the second clock signal, in embodiments, may change the phase of the second clock signal. In embodiments, the interim adjustment information indicates a desired phase. In embodiments, the interim adjustment information indicates a desired frequency. In embodiments, the interim adjustment information indicates a change in phase. In embodiments, the interim adjustment information indicates a

change in frequency. In embodiments, the adjustment information includes a voltage. In embodiments, the adjustment information includes a digital transmission. For example, the adjustment information may be a command over a serial bus (e.g., I2C or SPI) that adjusts a clock divider or phase rotator. As another example, the adjustment information may trigger a set of parallel digital wires for "frequency/phase up," "frequency/phase down," and/or "frequency/phase step." In embodiments, the adjustment of the second clock signal may change the frequency of the second clock signal.

[0466] In embodiments, steps S1302 through steps S 1316 are repeated until the first output of the phase detector is below the first threshold level. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have phases that are aligned. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have frequencies that correspond to one another.

[0467] Referring back to FIG. 12B, once the first output of the phase detector is below a first threshold level, at a step S1222, the serializer may transmit the first transmitter side clock signal to the computational circuitry. At a step S1224, a first set of operations performed by the computational circuitry on at least a portion of the first plurality of data items to generate a second plurality of data streams. In embodiments, the first operation includes a trading algorithm. In embodiments the trading algorithm may include the parsing the market data. Once the market data is parsed, mathematical operations are performed at a portion of the market data. After the mathematical operations are performed, order packets are generated using at least an output of the mathematical operations. In embodiments, the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

[0468] In embodiments, at least a portion of the first set of operations is performed prior to step S1222. In embodiments, at least a portion of the first set of operations is performed after step S922. In embodiments all of the first set of operations is performed after step S1222.

[0469] In embodiments, the second plurality of data streams may include a second amount of data streams. In embodiments, the second amount of data streams may be the same as the first amount of data streams. In embodiments, the second amount of data streams is equal to eight (8) data streams. In embodiments, the second amount of data streams is equal to ten (10) data streams.

In embodiments, the second amount of data streams is equal to sixteen (16) data streams. In embodiments, the second amount of data streams is equal to twenty (20) data streams. In embodiments, the second amount of data streams is equal to thirty-two (32) data streams. In embodiments, the second amount of data streams is equal to forty (40) data streams. In embodiments, the second amount of data streams is equal to sixty-four (64) data streams. In embodiments, the second amount of data streams is equal to eighty (80) data streams. In embodiments, the second amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the second amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the second amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the second amount of data streams is equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the second amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0470] At a step S1226, the second plurality of data streams is transmitted from the computational circuitry to the serializer. Once received by the serializer, at a step S1228, the serializer converts the second plurality of parallel data streams into the second serial data stream. The second serial data stream, in embodiments, includes trading data. Trading data, for example, may be any data related to purchasing or selling of stocks, commodities, goods, and/or services.

[0471] At a step S1230, the second serial data stream may be transmitted from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface. In embodiments, the second serial data stream is transmitted from the serializer on the field programmable gate array to an input/output module of the field gate array system but not on the field gate array. The second serial data stream may then be transmitted from the input/output module off the field gate array system.

[0472] FIGs 15A-C, 16A-B and 17 are exemplary flow charts of a process implementing the field programmable gate array system in accordance with yet another embodiment of the present invention. In embodiments, the process described in the flow charts of FIGs. 15A-C, 16A-B and 17 may be implemented by the field programmable gate array system shown in FIG. 3B or FIG. 5B. The field programmable gate array system, including the field programmable gate array and the components thereof, may be similar to the field programmable gate array systems of FIG. 3B and FIG. 5B, the descriptions of which applying herein.

[0473] The process of FIGs. 15A-15C may begin at step S1502. Referring to FIG. 15A, at step S1502, a first serial data stream is received by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system. In embodiments, the first serial data stream may include market data. In embodiments, market data may be price and trade-related data for a financial instrument reported by a trading venue (i.e., a stock exchange).

[0474] At a step S1504, a first clock signal having a first frequency and a first phase is received by a first reference clock pin in the first interface from a fixed frequency oscillator. In embodiments, step S1504 may be performed before step S1502. In embodiments, step S1504 may be performed contemporaneously with step S1502.

[0475] The process of FIGs. 15A-15C may continue with a step S1506. At step S1506, the first plurality of data pins of the first interface may transmit the first serial data stream to a deserializer in the field programmable gate array.

[0476] At a step S1508, the first reference clock pin in the first interface may transmit the first clock signal to the deserializer. In embodiments, step S1508 may be performed before step S1506. In embodiments step S1508 may be performed contemporaneously with step S1506.

[0477] At a step S1510, a first receiver side clock signal may be generated by the deserializer. In embodiments, the first receiver side clock signal may have a second frequency and a second phase. In embodiments, the second frequency is different from the first frequency. In embodiments, the second frequency corresponds to the first frequency. In embodiments, corresponding may refer to the frequencies being the same frequency. In embodiments corresponding may also refer to frequencies being close (e.g., within an acceptable range in the art) to the same frequencies. In embodiments, the first phase and the second phase may not be aligned. In embodiments the first phase and the second phase are aligned. In embodiments, a difference between the first phase and the second phase is below a threshold level. In embodiments, the deserializer generates the first receiver clock signal based at least in part on the first clock signal.

[0478] At a step S1512, the first serial data stream received by the deserializer may be converted, by the deserializer, into a first plurality of data streams. In embodiments, the first plurality of data streams may include a first amount of data streams. In embodiments, the first

amount of data streams is equal to eight (8) data streams. In embodiments, the first amount of data streams is equal to ten (10) data streams. In embodiments, the first amount of data streams is equal to sixteen (16) data streams. In embodiments, the first amount of data streams is equal to twenty (20) data streams. In embodiments, the first amount of data streams is equal to thirty-two (32) data streams. In embodiments, the first amount of data streams is equal to forty (40) data streams. In embodiments, the first amount of data streams is equal to sixty-four (64) data streams. In embodiments, the first amount of data streams is equal to eighty (80) data streams. In embodiments, the first amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the first amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the first amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the first amount of data streams is equal to ten (10) times two (2) to the power of N, where N is an integer. In embodiments the first amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0479] At a step S1514, the first receiver side clock signal is transmitted from the deserializer to computational circuitry in the field programmable gate array.

[0480] At a step S1516, the first plurality of data streams is transmitted from the deserializer to the computational circuitry. In embodiments, the first plurality of data streams includes a first plurality of data items. In embodiments, step S1516 may be performed before step S1514. In embodiments step S1516 may be performed contemporaneously with step S1514.

[0481] At a step S1518, the first receiver side clock signal is transmitted from the deserializer to a phase detector of the field programmable gate array system, which may or may not be one the field programmable gate array. If the phase detector is not on the field programmable gate array, the first receiver side clock signal may be transmitted from the deserializer to the phase detector via a first clock output pin on a second interface of the field programmable gate array. In embodiments, the first receiver side clock signal may also be transmitted via a first zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the first clock output pin of the second interface.

[0482] At a step S1520, a first transmitter side clock signal is generated by the field programmable gate array system. In embodiments, the first transmitter side clock signal has a third frequency and a third phase. In embodiments, the third frequency corresponds to the second

frequency. In embodiments, the third phase may be aligned with the second phase. In embodiments, the third phase and the second phase may not be aligned. In embodiments, the third phase and the second phase may have a difference in phases that is less than a second threshold level. In embodiments, the first transmitter side clock signal is generated by performing the following steps until a first output of the phase detector is below a first threshold.

[0483] Referring to FIG. 16A, generating the first transmitter side clock signal may begin at step S1602. At step S1602, an adjustable transceiver phase lock loop receives the first clock signal from the fixed frequency oscillator via a second reference clock pin in the first interface. In embodiments, the received first clock signal is used by the adjustable transceiver phase lock loop to generate a second clock signal. In embodiments, the second clock signal may have a fourth frequency and a fourth phase.

[0484] The process of FIGs. 16A-B may continue at a step S1604. At step S1604, a first wire rate clock signal having a fifth phase and a fifth frequency is generated. In embodiments, the generation of the first wire rate clock signal may be based in part on the second clock signal. In embodiments the fifth frequency is a rational multiple of the fourth frequency. In embodiments the fifth frequency is equal to x times the fourth frequency where x is the second amount of data streams. In embodiments the fifth frequency is equal to x times the frequency of the of the transmitter side clock signal where x may be half of the second amount of data streams.

[0485] In embodiments, the generation of the first wire rate clock signal may be performed with the following steps. Referring to FIG. 17, at a step S1702, the second clock signal is generated by the adjustable transceiver phase lock loop based at least in part on the received first clock signal. At a step S1704, the second clock signal is processed by the adjustable transceiver phase lock loop based on the interim adjustment information received from the phase controller (see S1614 and S1616). As a step S1706, the first wire rate clock signal is provided by the adjustable transceiver phase lock loop. The providing of the first wire rate clock signal, in embodiments, may be based at least in part on the processing of the second clock signal. Once the first wire rate clock signal is provided, at a step S1708, the first wire rate clock signal is transmitted by the adjustable transceiver phase lock loop to a serializer on the field programmable gate array. In embodiments, the first wire rate clock signal is generated by a phase lock loop. In embodiments, the phase lock loop that generates the first wire rate clock signal is on field programmable gate array. In

embodiments, the phase lock loop that generates the first wire rate clock signal is part of the field programmable gate array system and not part of the field programmable gate array.

[0486] In embodiments, the generation of the first wire rate clock signal may include processing the second clock signal. Once the second clock signal is processed, the first wire rate clock signal may be provided. The providing of the first wire rate clock signal, in embodiments, is based at least in part on the processing of the second clock signal. After providing the first wire rate clock signal, in embodiments, the first wire rate clock signal may be transmitted to the serializer.

[0487] Referring back to FIG. 16A, at a step 1606, an interim transmitter side clock signal having a sixth frequency and a sixth phase is generated by the serializer in the field programmable gate array. In embodiments, the sixth frequency corresponds to the third frequency. In embodiments the sixth phase may be aligned with the third phase. In embodiments, the sixth frequency may correspond to the third frequency and the sixth phase may not be aligned with the third phase. In embodiments, the sixth phase and the third phase may not be aligned. In embodiments, the third phase and the sixth phase may have a difference in phases that is less than a second threshold level.

[0488] At a step S1608, the interim transmitter side clock signal is transmitted from the serializer to the phase detector, which may or may not be on the field programmable gate array. If the phase detector is not on the field programmable gate array, the interim transmitter side clock signal may be transmitted from the serializer to the phase detector via a second clock output pin of the second interface. In embodiments, the interim transmitter side clock signal may also be transmitted a second zero delay buffer phase lock loop of the field programmable gate array before being transmitted via the second clock output in of the second interface.

[0489] The process of FIGs. 16A-16B may continue with at a step S1610. Referring to FIG. 16B, at a step S1610, a first output is generated by the phase detector. The first output, in embodiments, is based at least on a comparison of the first receiver side clock signal and the interim side clock signal. The first output, in embodiments, may include information indicating the phase differences (if there is any) between the first receiver side clock and the interim side clock signal. Additionally, in embodiments, the first output may include information indicating a

difference (if there is any) of frequencies between the first receiver side clock signal and the interim side clock signal.

[0490] At a step S1612, the first output may be transmitted from the phase detector to a phase controller of the field programmable gate array system, which may be placed within the field programmable gate array.

[0491] At a step S1614, interim adjustment information is determined by the phase controller. In embodiments, the interim adjustment information may be based at least in part on the first output. For example, the interim adjustment information may indicate necessary adjustments to align the phases of the first receiver side clock signal and the interim side clock signal. As another example, the interim adjustment information may indicate necessary adjustments to align the frequencies of the first receiver side clock signal and the interim side clock signal.

[0492] At a step S1616, the interim adjustment information is transmitted from the phase controller to the adjustable transceiver phase lock loop. In embodiments, once the interim adjustment information is received, the adjustable transceiver phase lock loop adjusts the second clock signal based on the interim adjustment information. The adjustment of the second clock signal, in embodiments, may change the phase of the second clock signal. In embodiments, the interim adjustment information indicates a desired phase. In embodiments, the interim adjustment information indicates a desired frequency. In embodiments, the interim adjustment information indicates a change in phase. In embodiments, the interim adjustment information indicates a change in frequency. In embodiments, the adjustment information includes a voltage. In embodiments, the adjustment information includes a digital transmission. For example, the adjustment information may be a command over a serial bus (e.g., I2C or SPI) that adjusts a clock divider or phase rotator. As another example, the adjustment information may trigger a set of parallel digital wires for "frequency/phase up," "frequency/phase down," and/or "frequency/phase step." In embodiments, the adjustment of the second clock signal may change the frequency of the second clock signal.

[0493] In embodiments, steps S1602 through steps S 1016 are repeated until the first output of the phase detector is below the first threshold level. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have phases that are

aligned. This threshold level may indicate that the first receiver side clock signal and the interim transmitter side clock signal have frequencies that correspond to one another.

[0494] Referring back to FIG. 15B, once the first output of the phase detector is below a first threshold level, at a step S1522, the serializer may transmit the first transmitter side clock signal to the computational circuitry. At a step S1524, a first set of operations is performed by the computational circuitry on at least a portion of the first plurality of data items to generate a second plurality of data streams. In embodiments, the first operation includes a trading algorithm. In embodiments the trading algorithm may include the parsing the market data. Once the market data is parsed, mathematical operations are performed at a portion of the market data. After the mathematical operations are performed, order packets are generated using at least an output of the mathematical operations. In embodiments, the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

[0495] In embodiments, at least a portion of the first set of operations is performed prior to step S1522. In embodiments, at least a portion of the first set of operations is performed after step S1522. In embodiments, all of the first set of operations is performed after step S1522.

[0496] In embodiments, the second plurality of data streams may include a second amount of data streams. In embodiments, the second amount of data streams may be the same as the first amount of data streams. In embodiments, the second amount of data streams is equal to eight (8) data streams. In embodiments, the second amount of data streams is equal to ten (10) data streams. In embodiments, the second amount of data streams is equal to sixteen (16) data streams. In embodiments, the second amount of data streams is equal to twenty (20) data streams. In embodiments, the second amount of data streams is equal to thirty-two (32) data streams. In embodiments, the second amount of data streams is equal to forty (40) data streams. In embodiments, the second amount of data streams is equal to sixty-four (64) data streams. In embodiments, the second amount of data streams is equal to eighty (80) data streams. In embodiments, the second amount of data streams is equal to one hundred twenty-eight (128) data streams. In embodiments, the second amount of data streams is equal to one hundred sixty (160) data streams. In embodiments, the second amount of data streams is equal to two (2) to the power of N, where N is an integer. In embodiments, the second amount of data streams is equal to ten

(10) times two (2) to the power of N, where N is an integer. In embodiments the second amount of data streams is equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

[0497] At a step S1526, the second plurality of data streams is transmitted from the computational circuitry to the serializer. Once received by the serializer, at a step S1528, the serializer converts the second plurality of parallel data streams into the second serial data stream. The second serial data stream, in embodiments, includes trading data. Trading data, for example, may be any data related to purchasing or selling of stocks, commodities, goods, and/or services.

[0498] At a step S1530, the second serial data stream may be transmitted from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface. In embodiments, the second serial data stream is transmitted from the serializer on the field programmable gate array to an input/output module of the field gate array system but not on the field gate array. The second serial data stream may then be transmitted from the input/output module off the field gate array system.

EXAMPLES

[0499] The following examples may be used to illustrate embodiments of the present invention. They are meant solely for illustration and not intended to be limiting.

EXAMPLE 1

[0500] In embodiments a trading algorithm may be applied in a crossing auction on an option exchange. In embodiments, a third serial data stream including target price information on a set of options contracts is provided as an input to the FPGA. In embodiments, the first serial stream includes market data includes bid, asks, trades and auction notifications. When an auction is announced, as indicated in the market data, the FPGA compares the announced auction price to its target price. In embodiments, the target price is stored in the FPGA and is provided via the third serial data stream. In embodiments, the target price may be generated using a suitable pricing model, e.g., Black Scholes model. When there is some overlap, the field programmable gate array generates and sends an order at its target price which is transmitted out of the FPGA in the second serial data stream. In embodiments, the target price information on a set of options contracts is streamed into the field programmable gate array as a simple set of triggers in the third serial data stream. The target price information, may include a linearization of the result of the Black Scholes

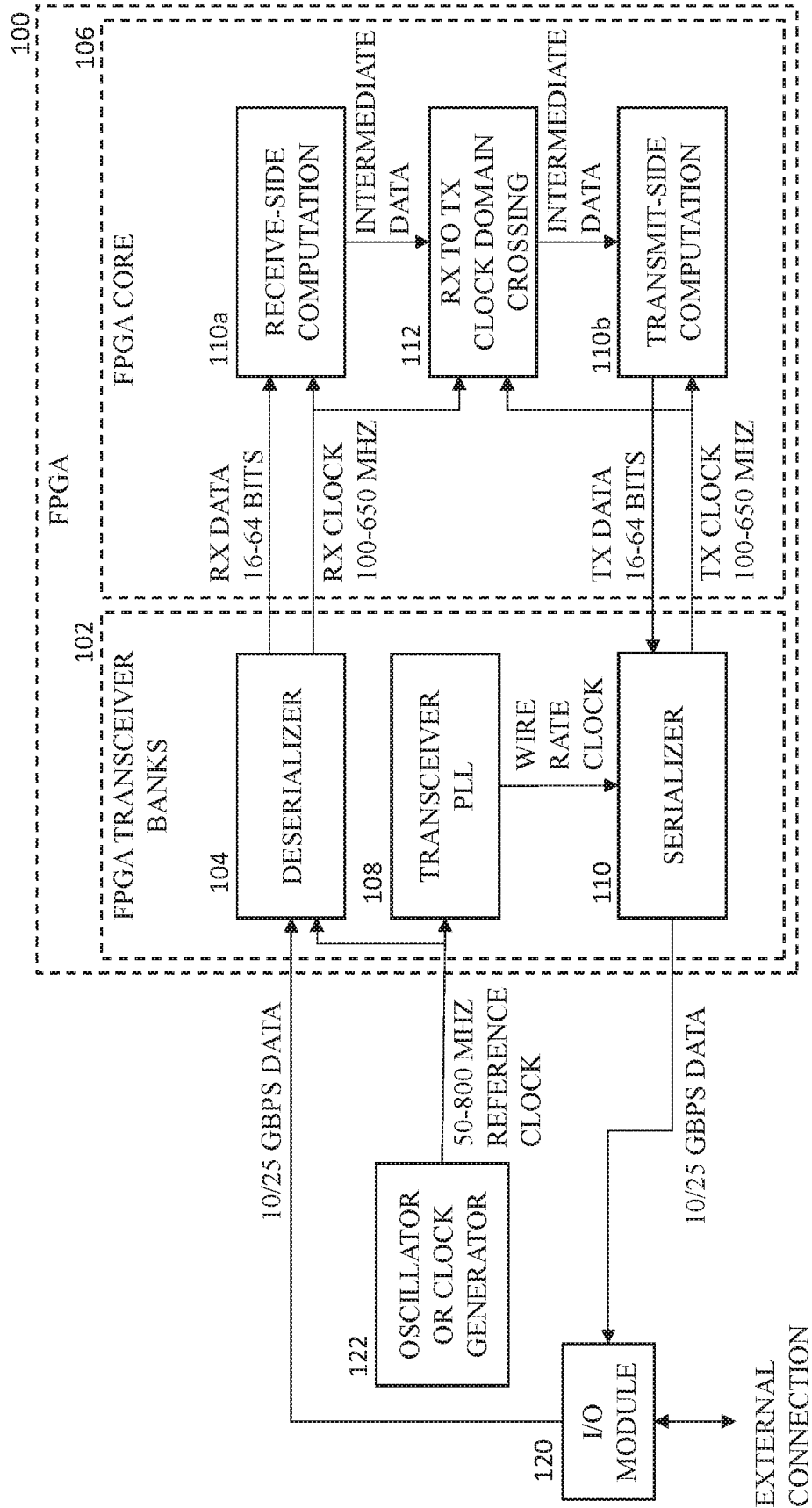
computation or some other model. The field programmable gate array may implement Black Scholes, and instead receive market data on the underlying asset as a secondary data stream.

EXAMPLE 2

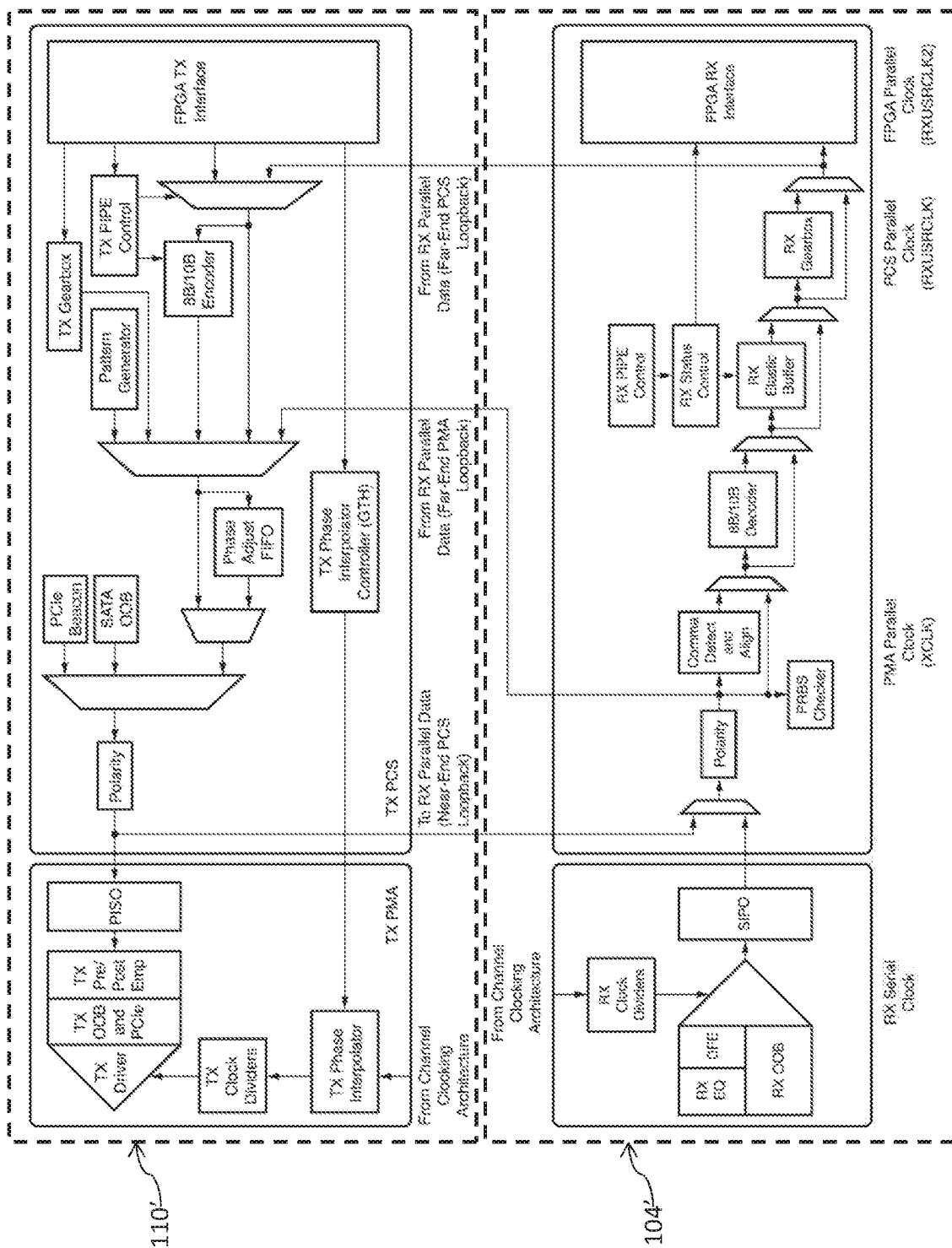
[0501] Another example of a trading algorithm is "signal based". In embodiments, signals refer to a trigger that is activated when certain events happen. In embodiments, a signal may simply track a sale price which changes every time the market information indicates a sale has taken place. In embodiments, a signal may be used as a measure of book pressure to determine whether prices are likely to rise or fall. Some signals may be calculated quickly while others are calculated more slowly because they require more data over a longer period of time. In embodiments, order information may be based on a single signal or based on a plurality of signals. Signals depending on the historical behavior of a financial instrument are programmed into the field programmable gate array. A few simple and well-known examples of a signal here are moving averages of past prices or book pressure signals (looking for an imbalance in the order book). Signal-based trading involves receiving market data on the financial instrument, constructing the order book for that instrument, calculating a predicted price based on a pre-defined collection of signals, and sending an order if the signals indicate that the signal indicates that it is a favorable time to trade. A secondary data stream here could be used to enable or disable signals or to change signal parameter values. In embodiments, the secondary data stream may be omitted. An example of a signal-based trading system might be a system that updates the quotes for a market maker when a set of signals indicates that a large directional move in the price of a stock is coming. The parallel processing advantage shows up here more so than in the first example.

* * * * *

[0502] Now that embodiments of the present invention have been shown and described in detail, various modifications and improvements thereon can become readily apparent to those skilled in the art. Accordingly, the exemplary embodiments of the present invention, as set forth above, are intended to be illustrative, not limiting. The spirit and scope of the present invention is to be construed broadly.



PRIOR ART
FIG. 1



PRIOR ART

FIG. 1A

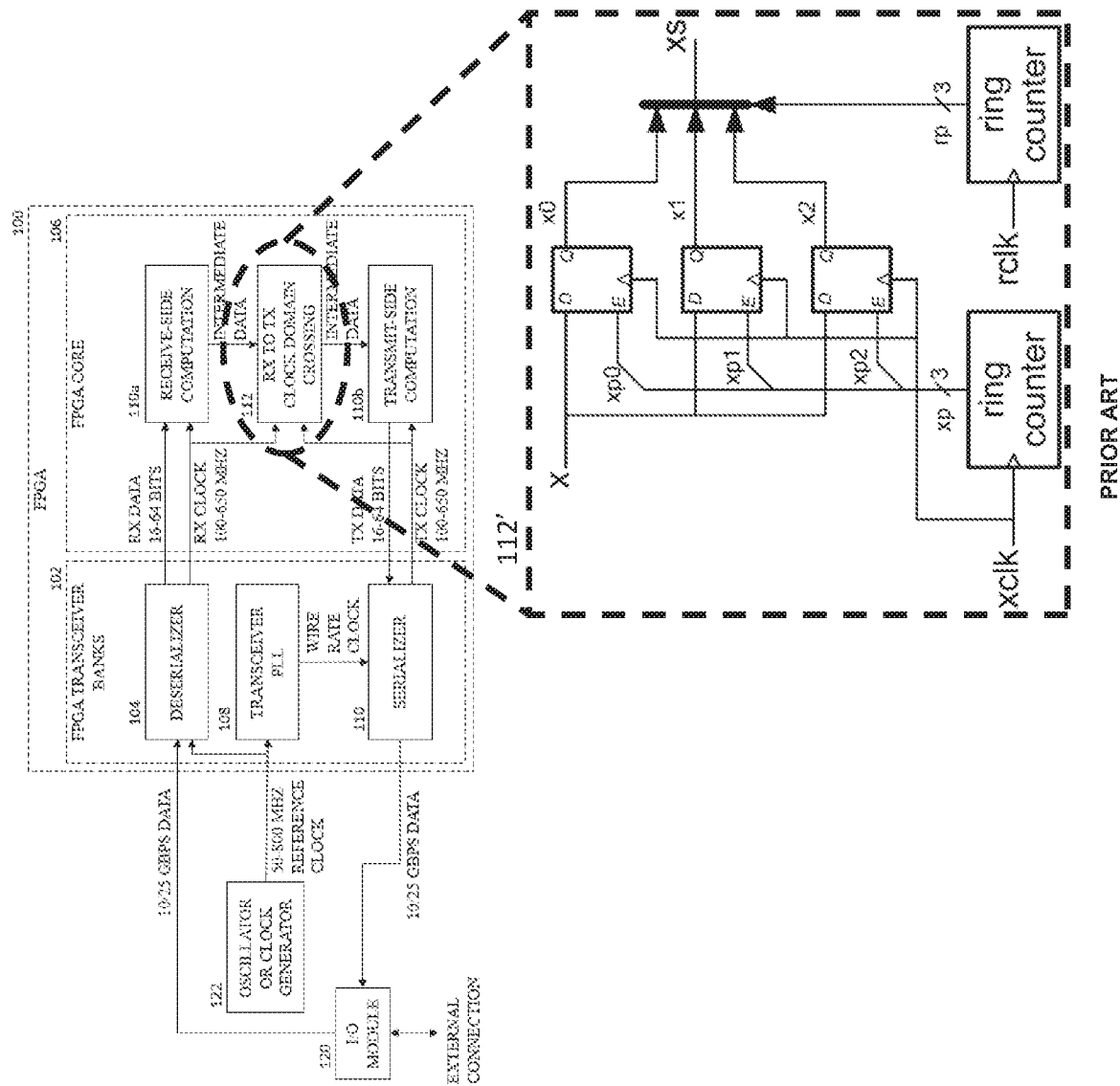
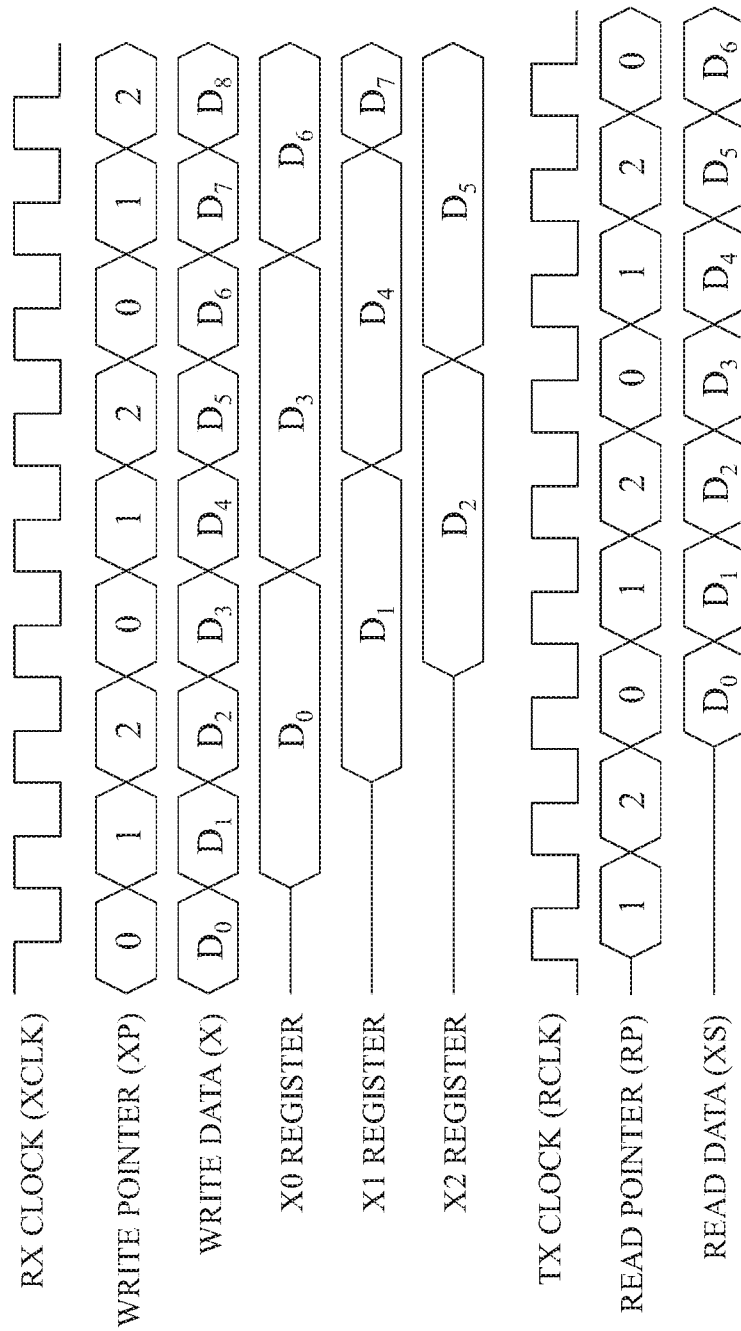


FIG. 1B



PRIOR ART

FIG. 1C

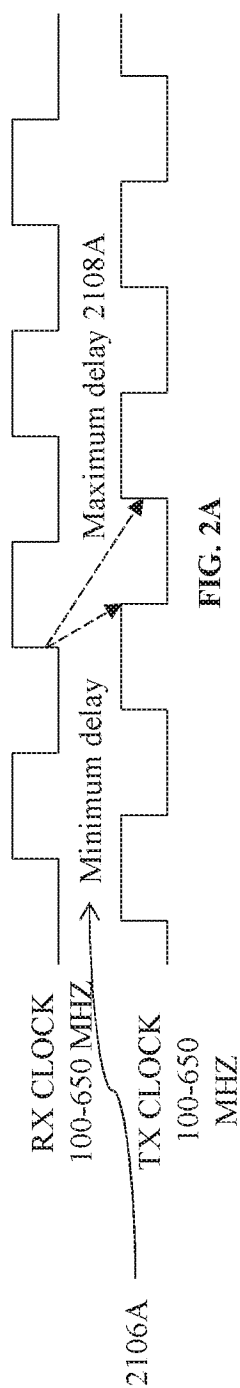


FIG. 2A

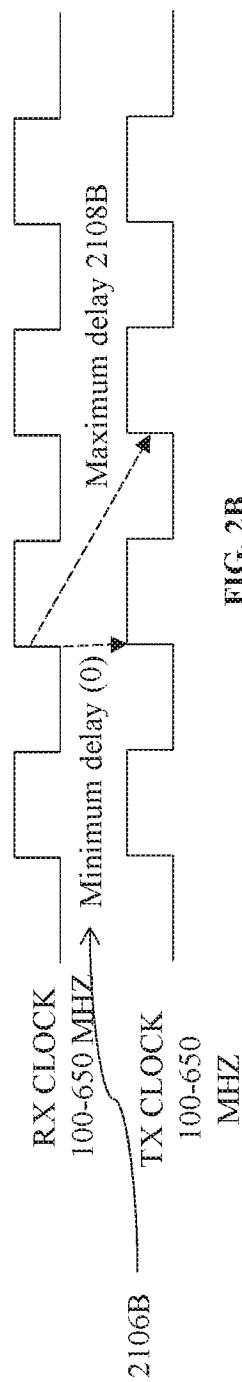


FIG. 2B

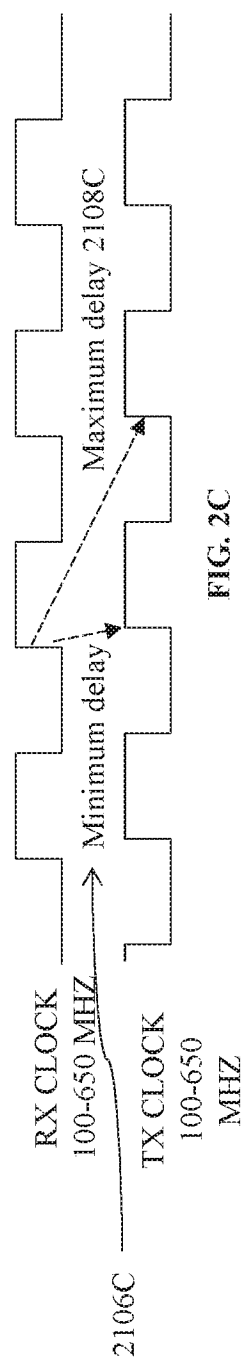


FIG. 2C

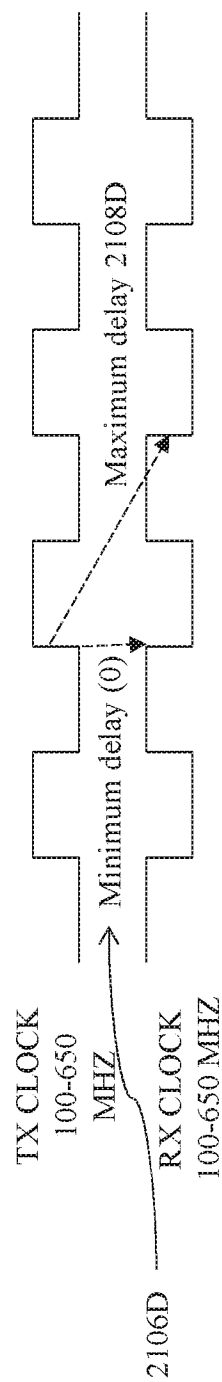


FIG. 2D

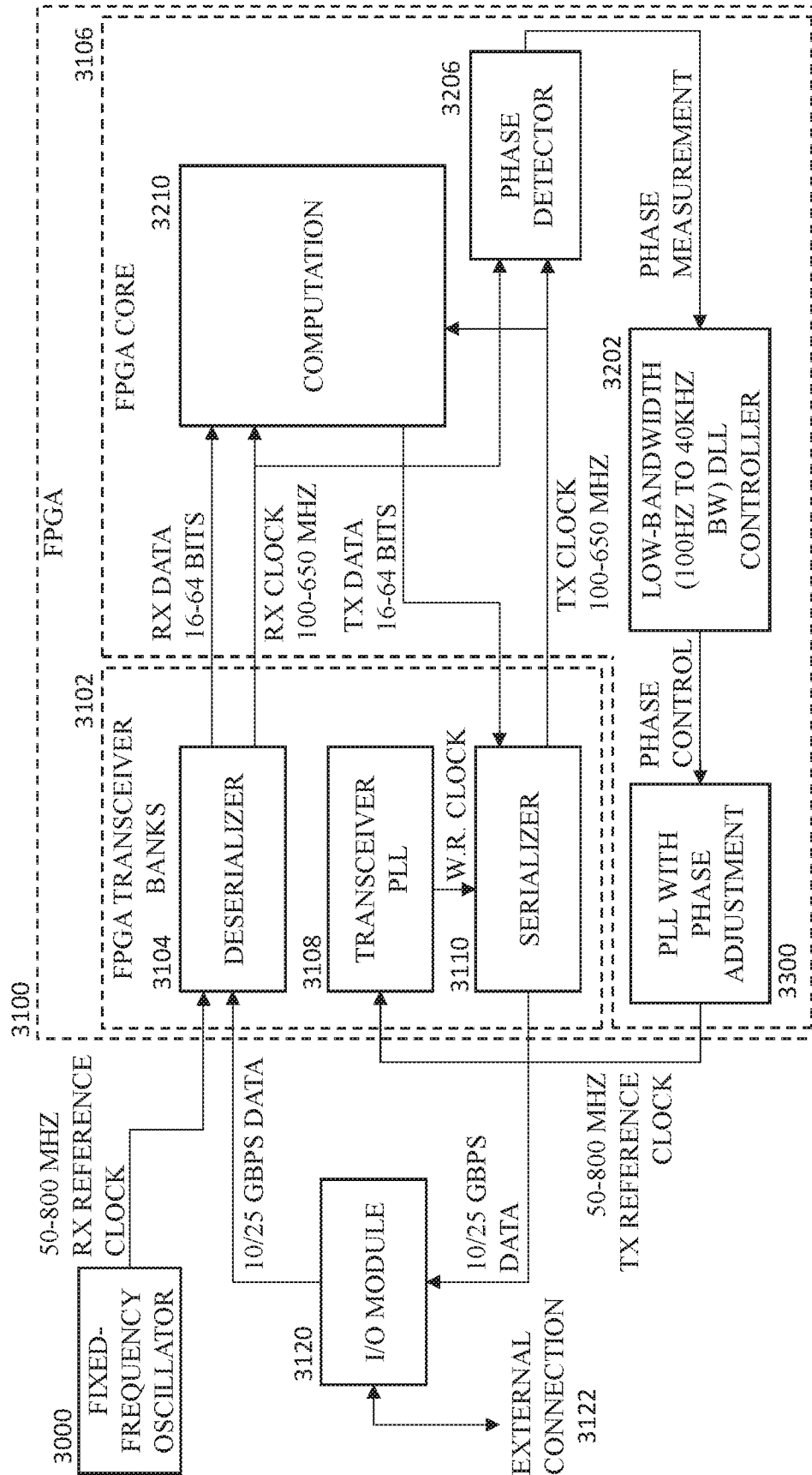


FIG. 3A

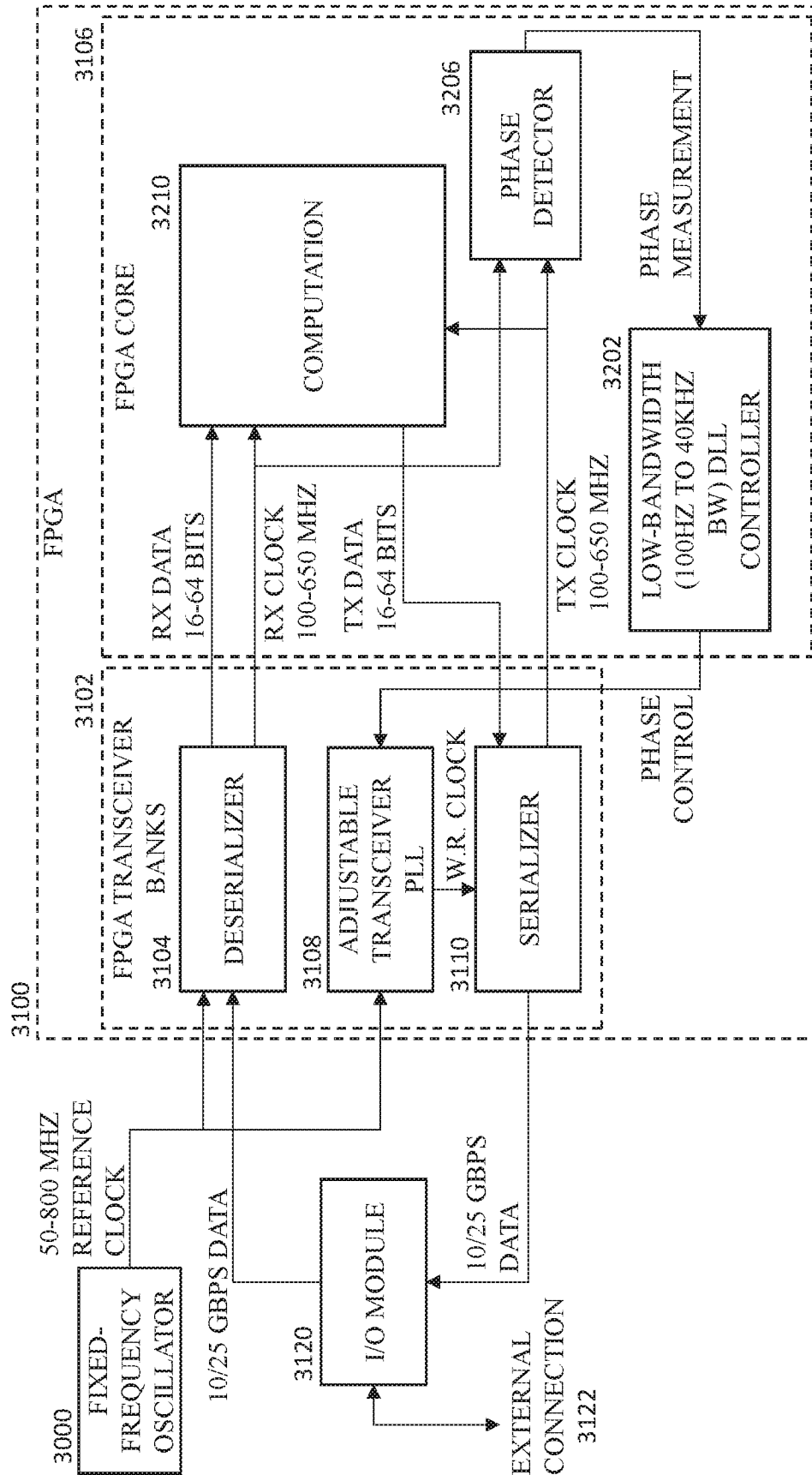


FIG. 3B

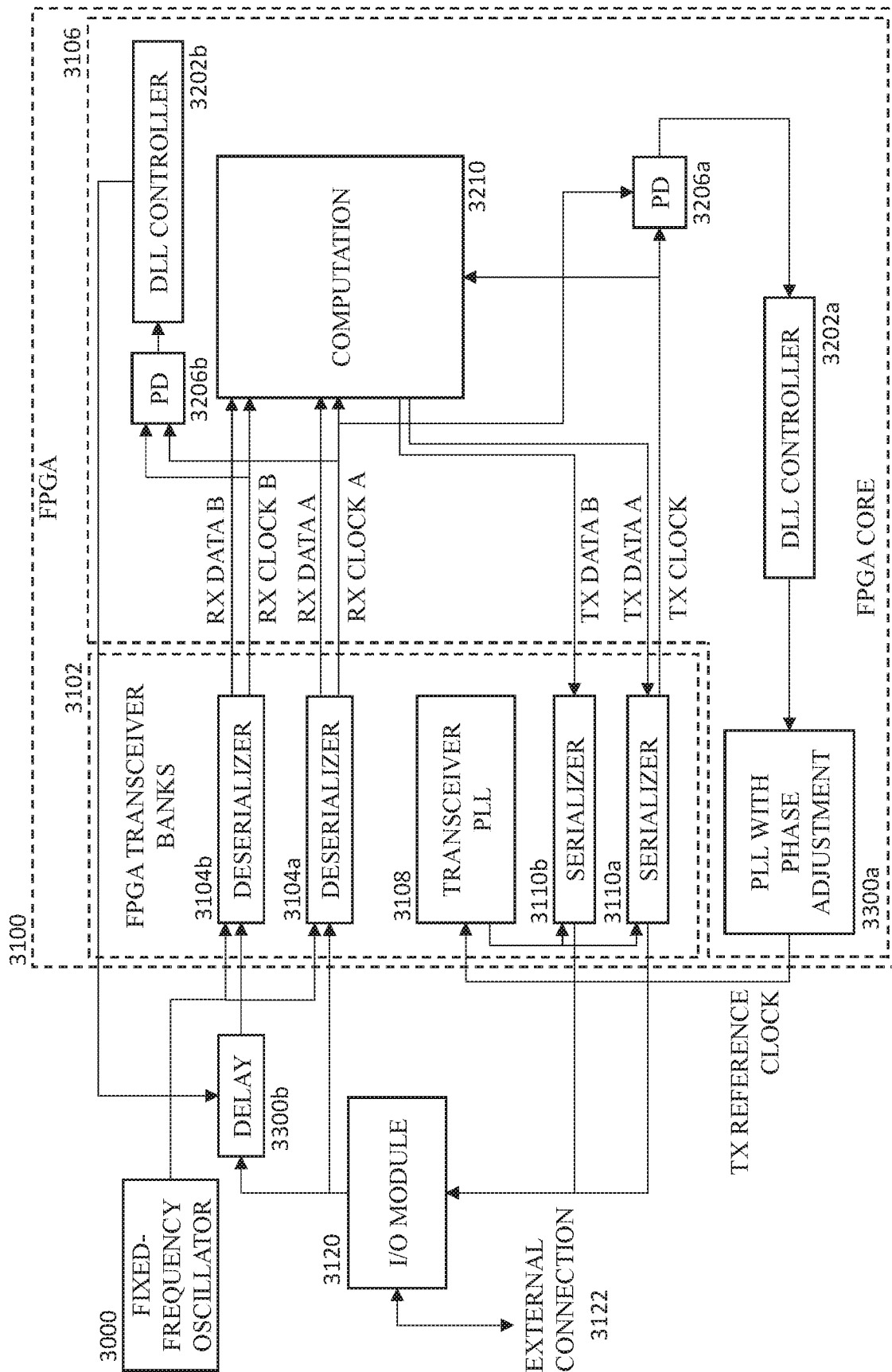


FIG. 3C

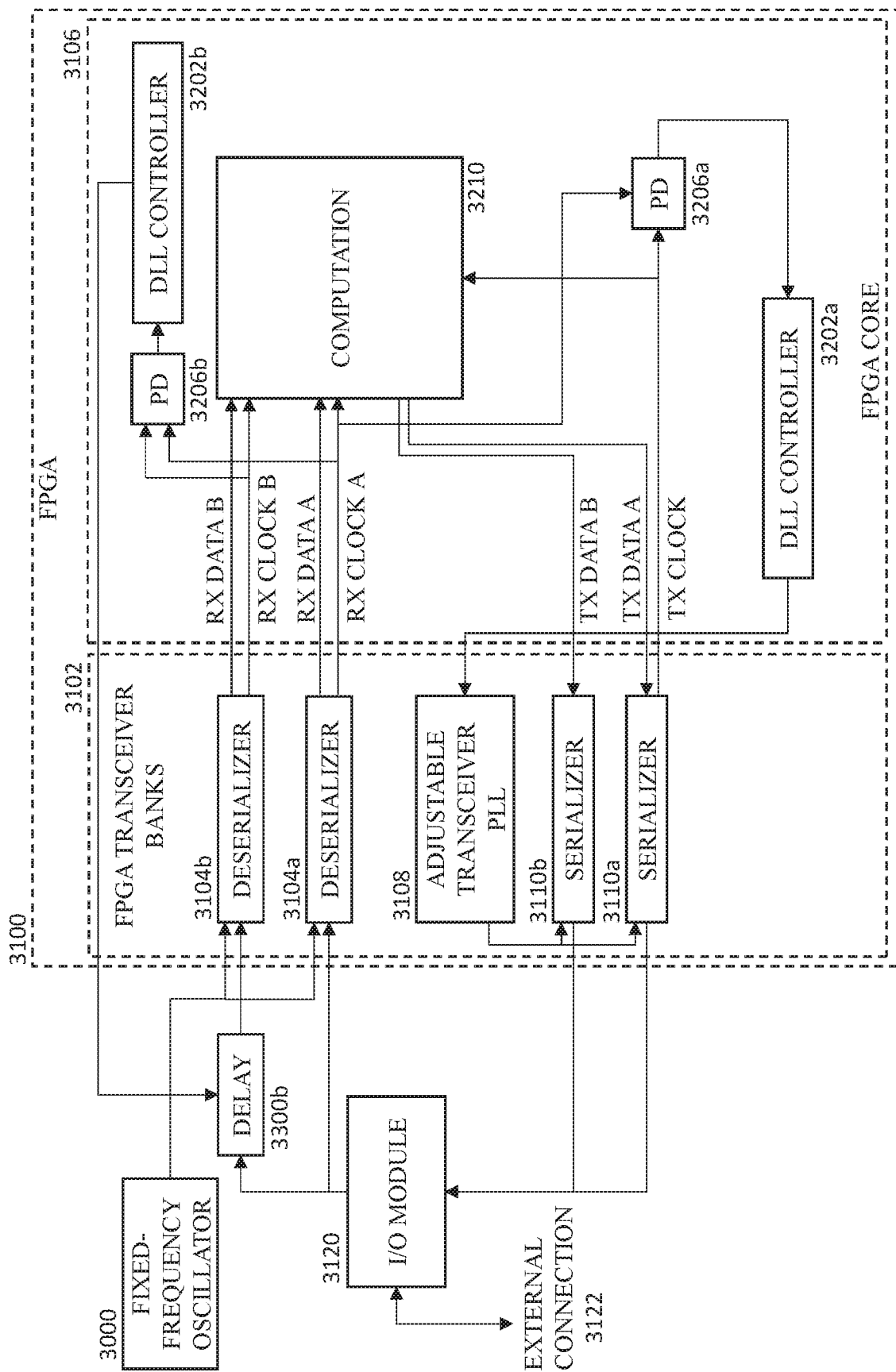


FIG. 3D

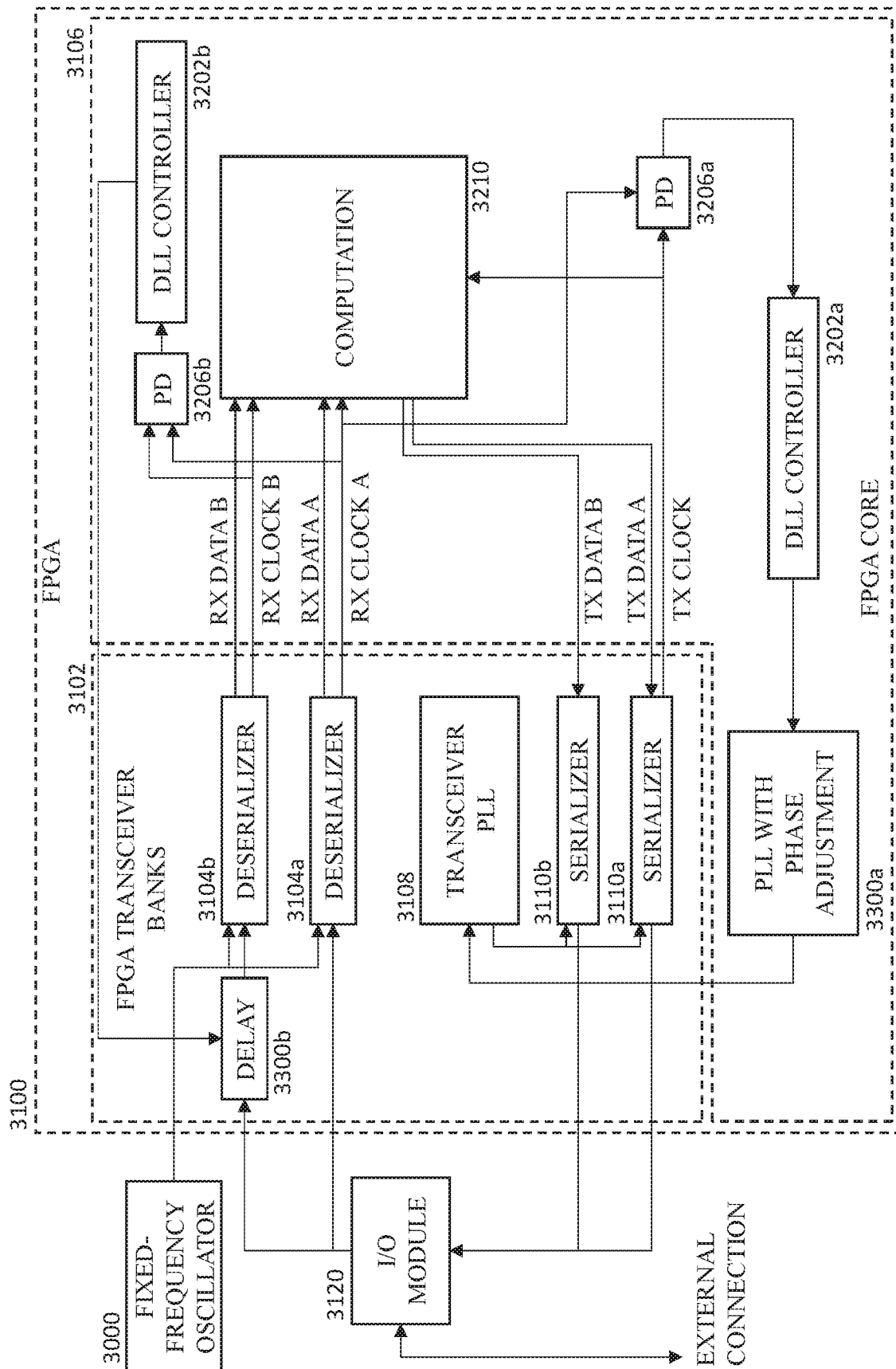


FIG. 3E

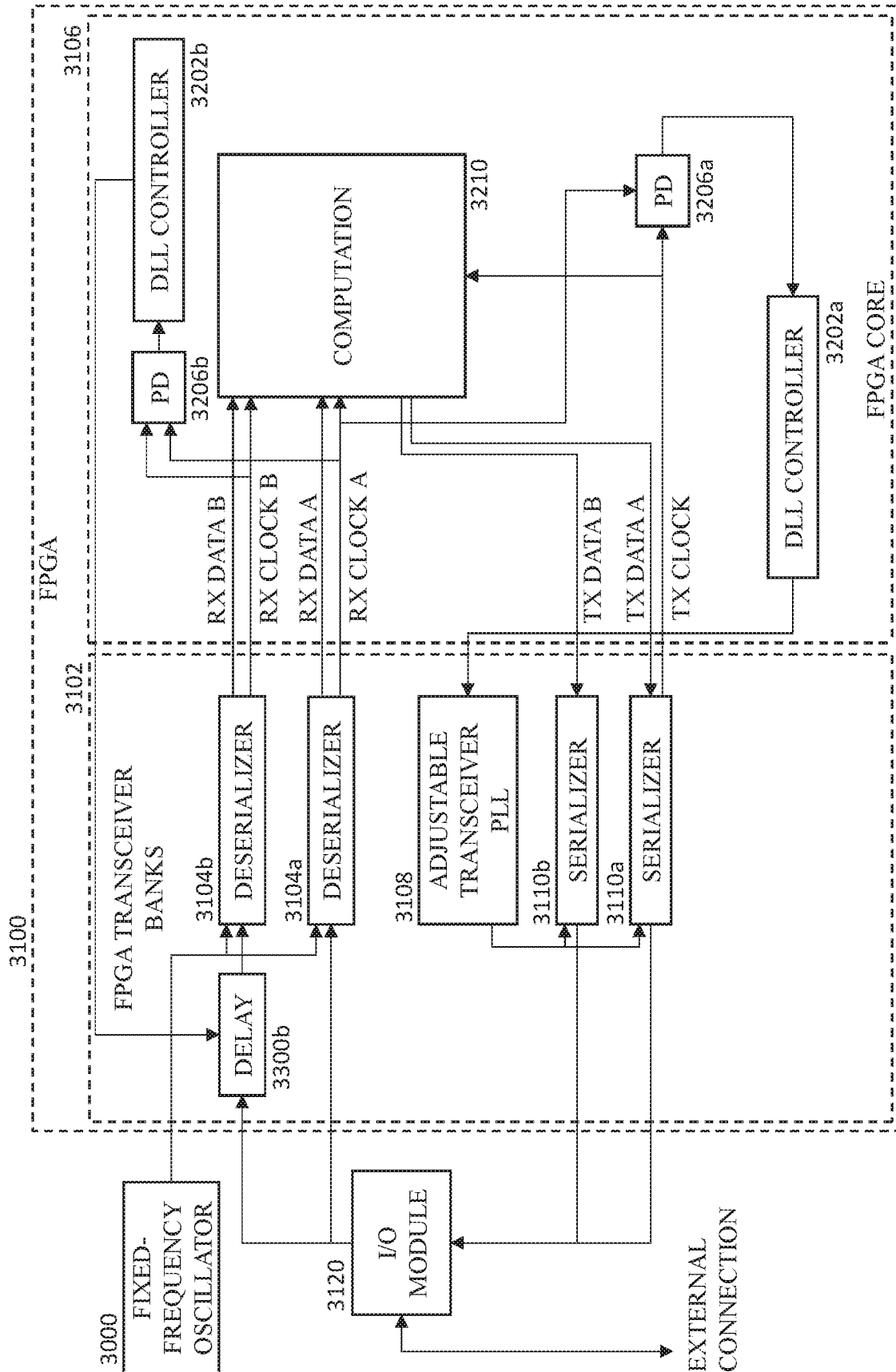


FIG. 3F

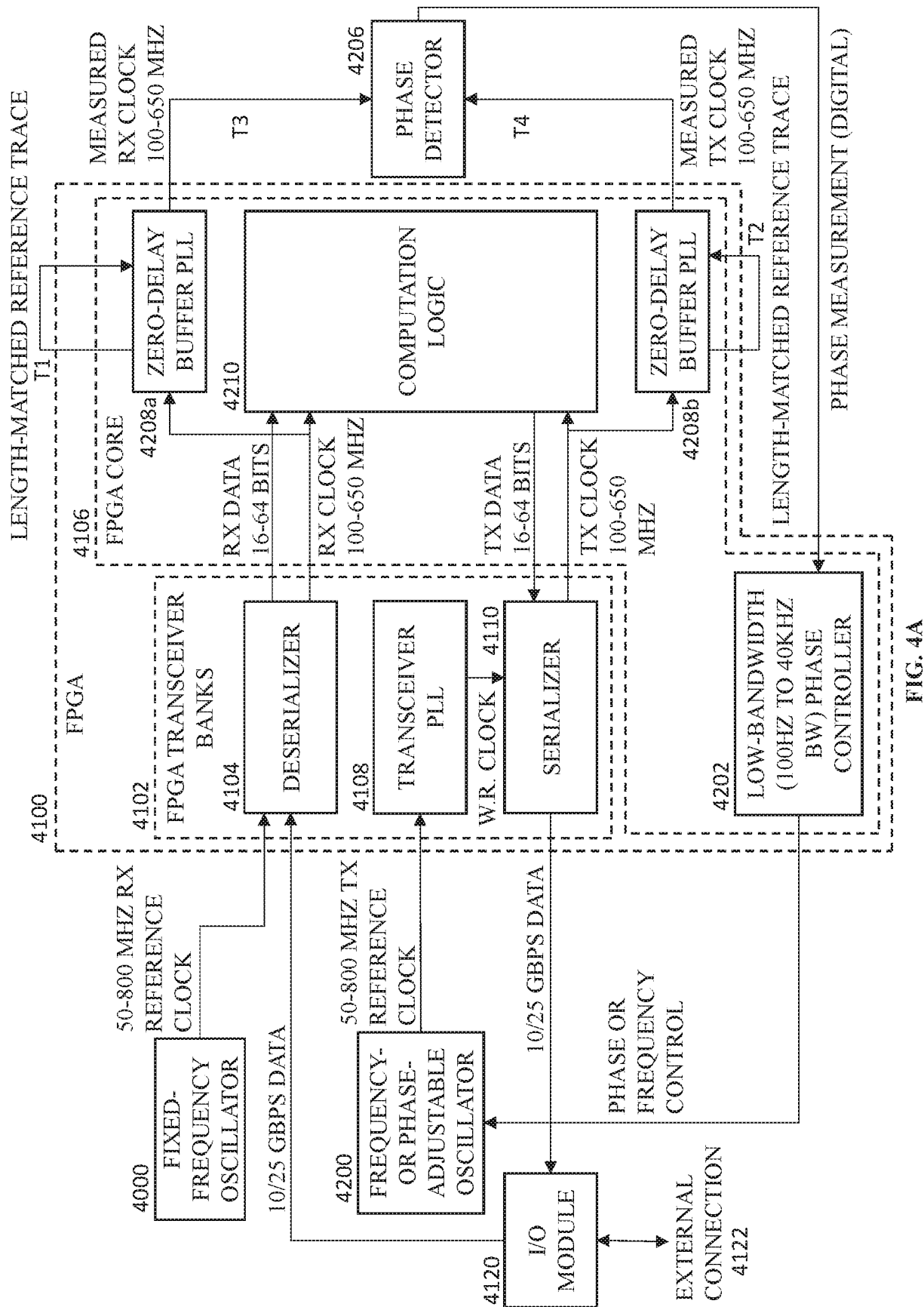


FIG. 4A

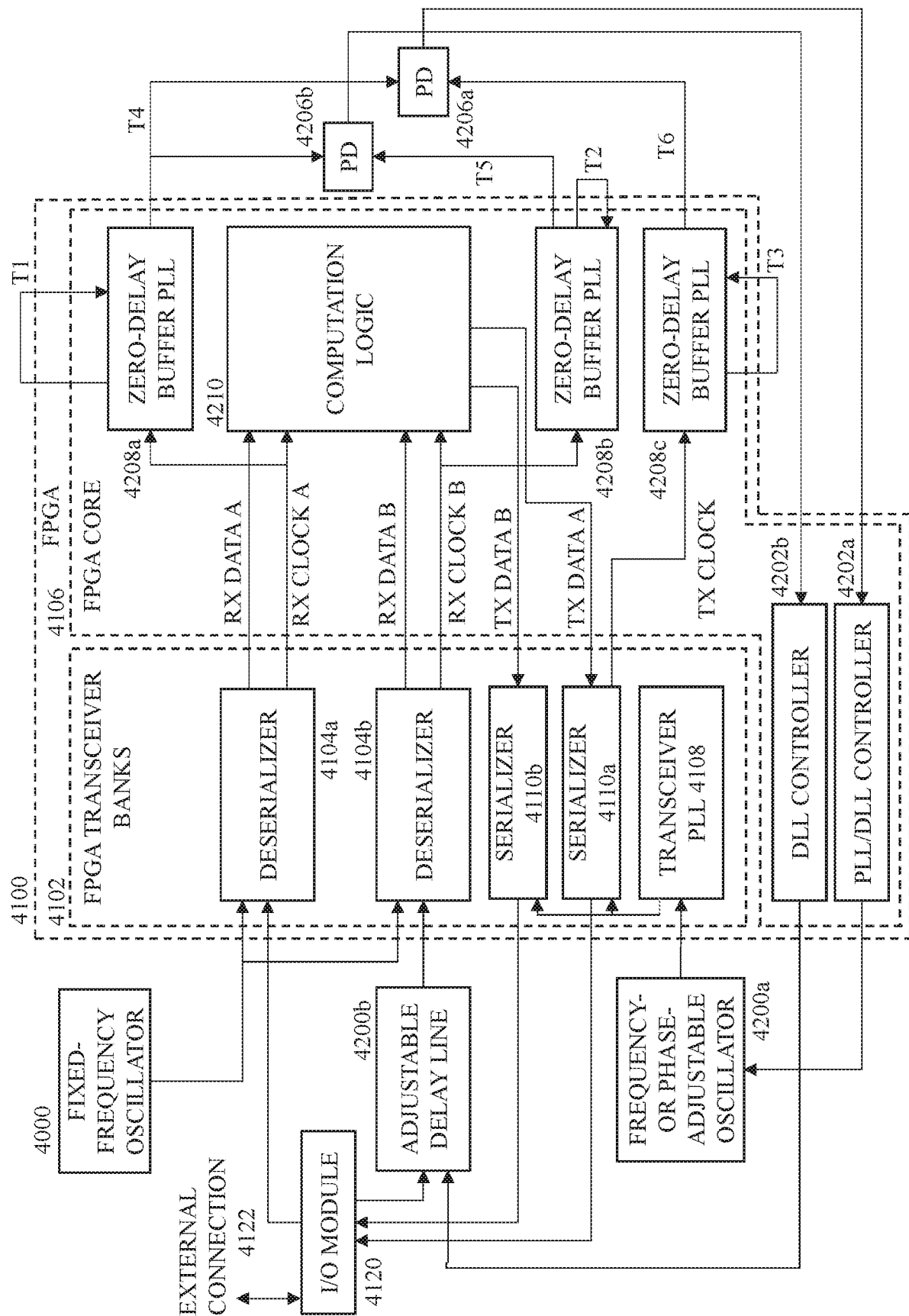


FIG. 4B

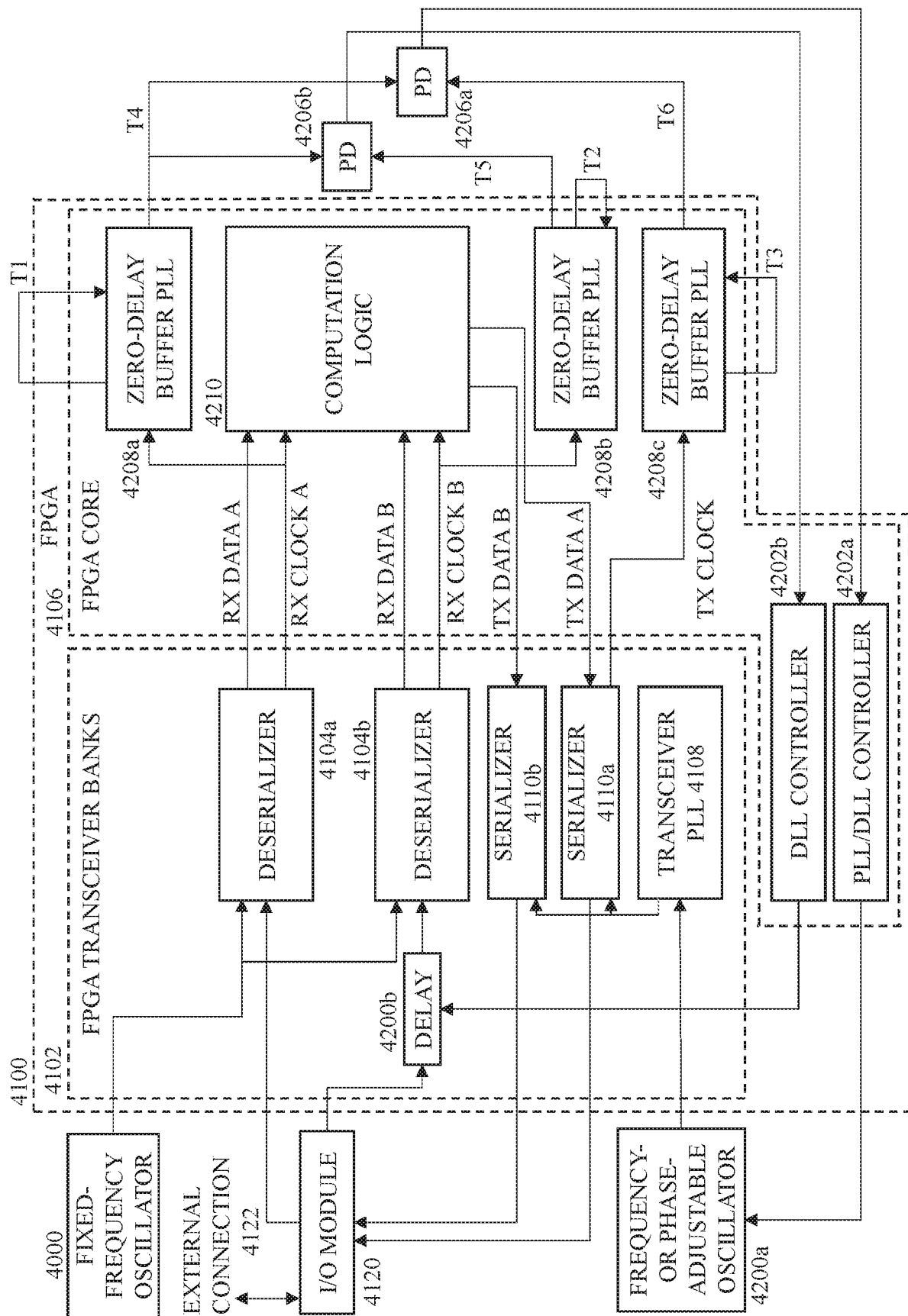


FIG. 4C

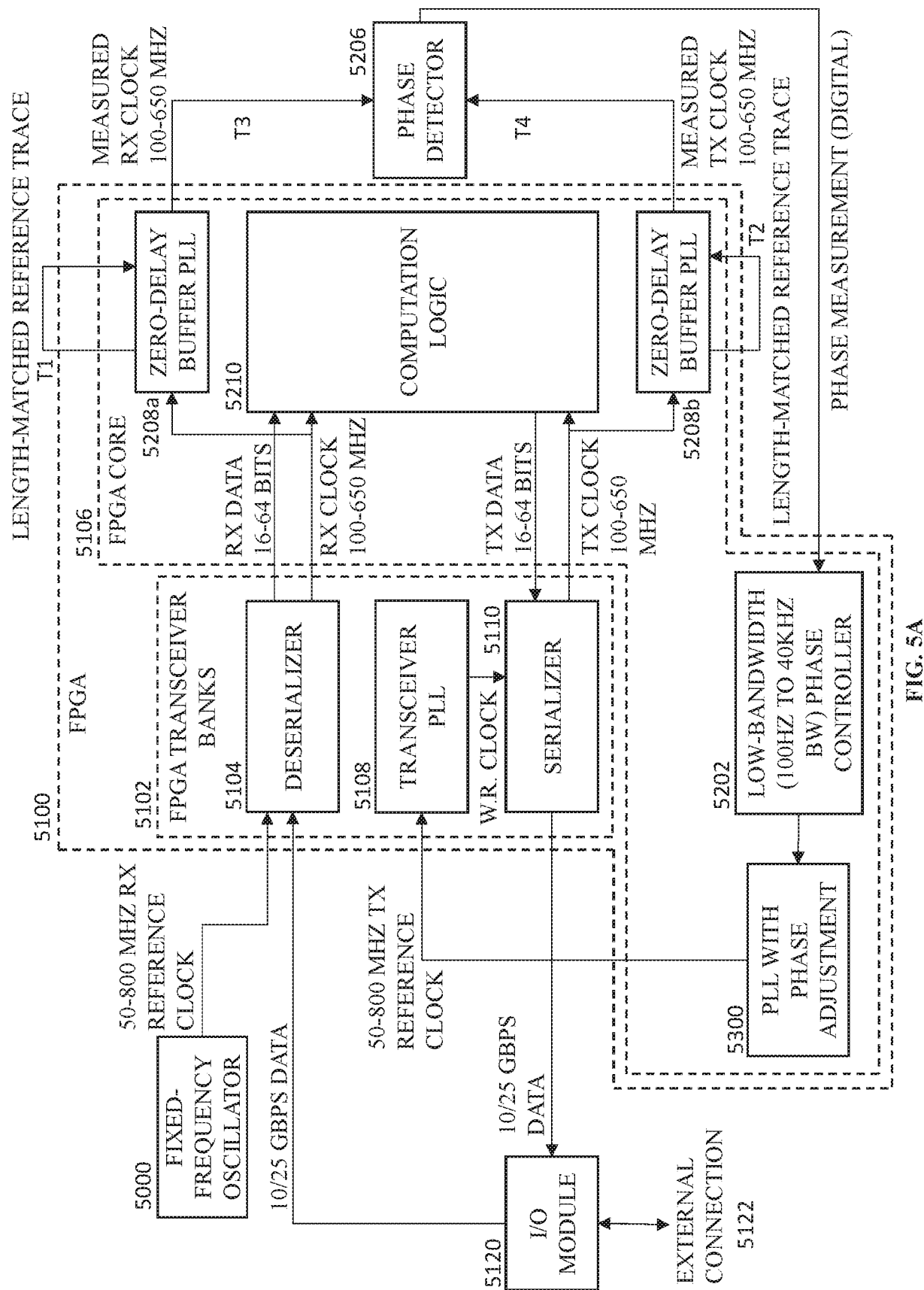


FIG. 5A

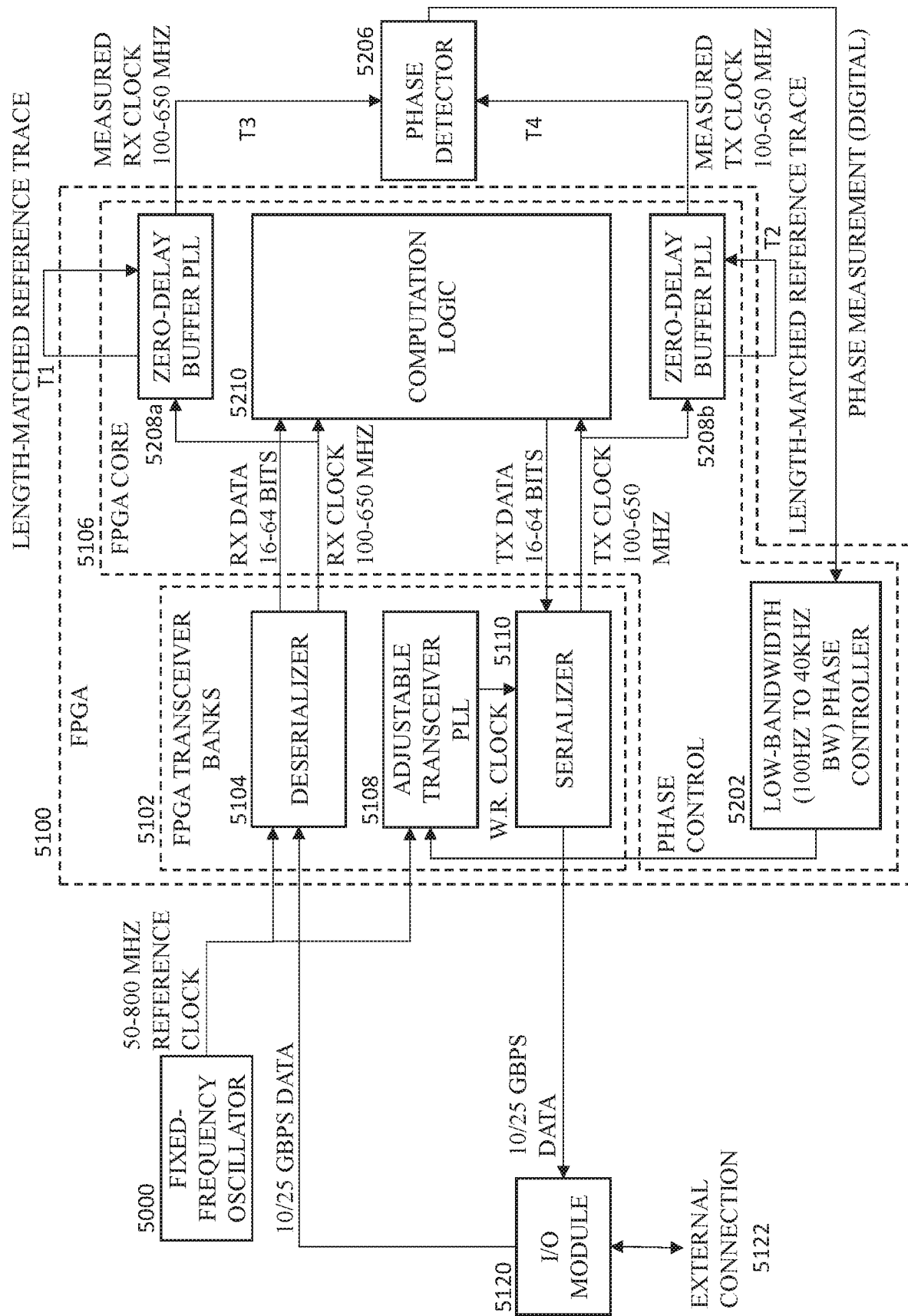


FIG. 5B

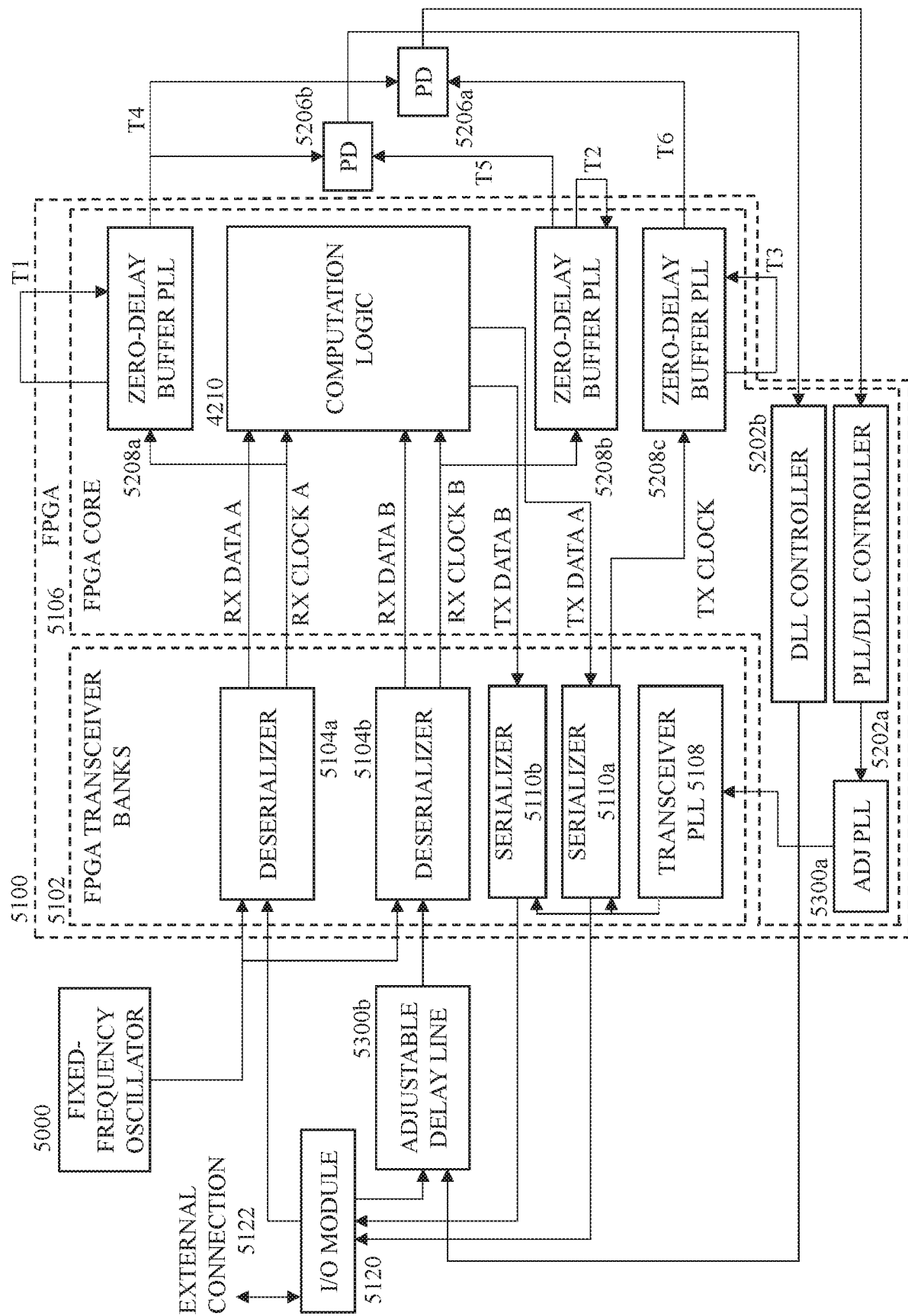


FIG. 5C

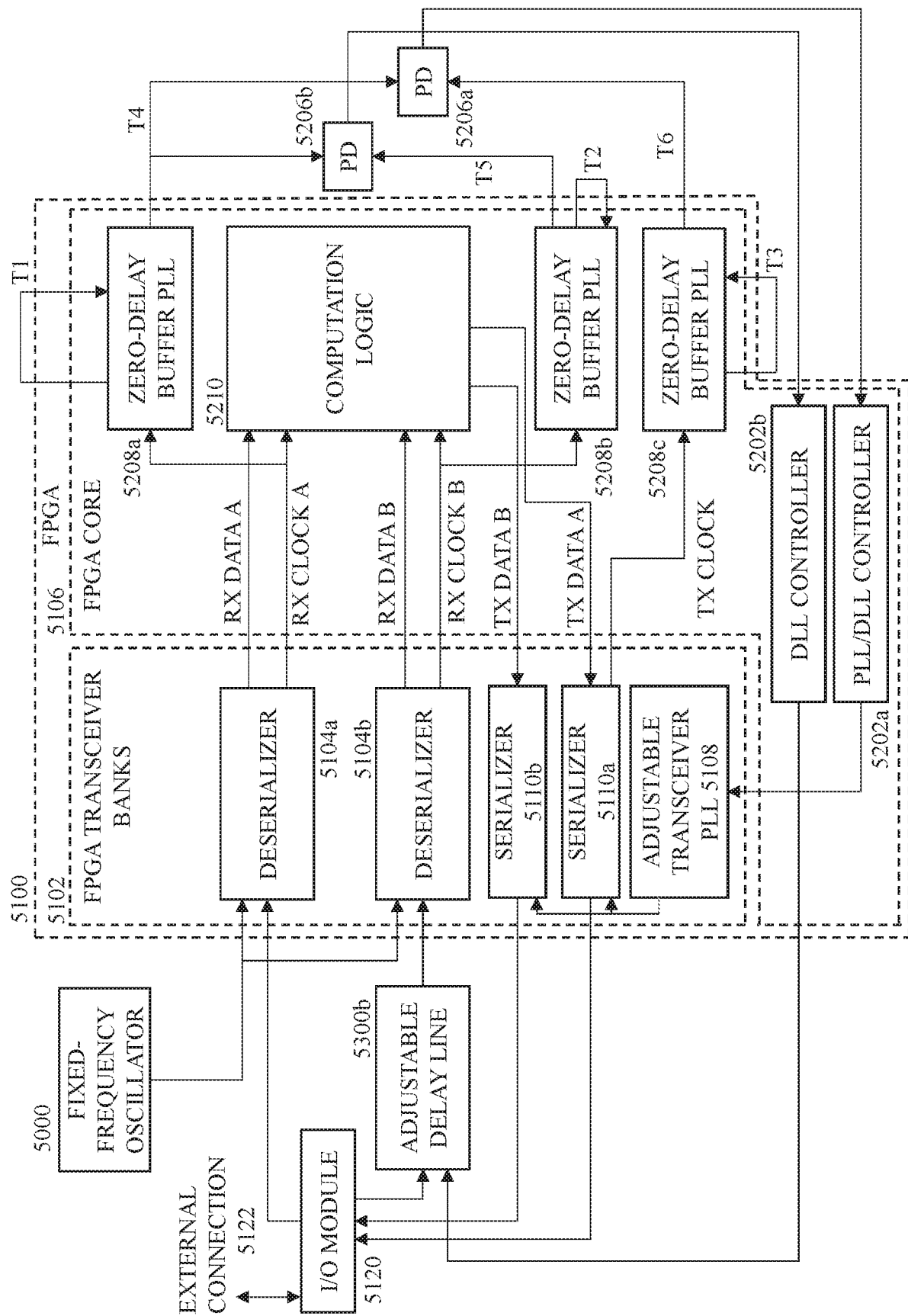


FIG. 5D

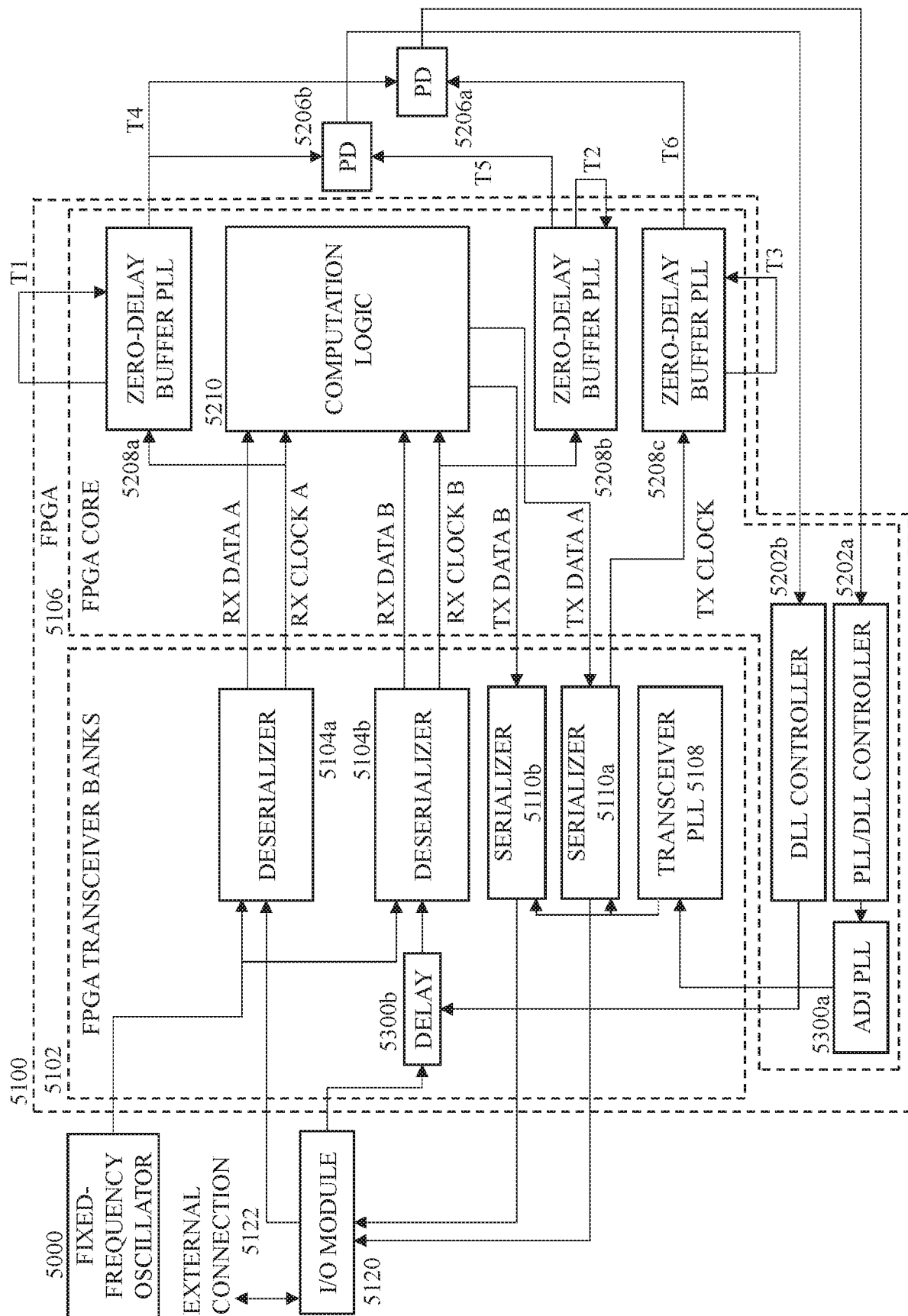


FIG. 5E

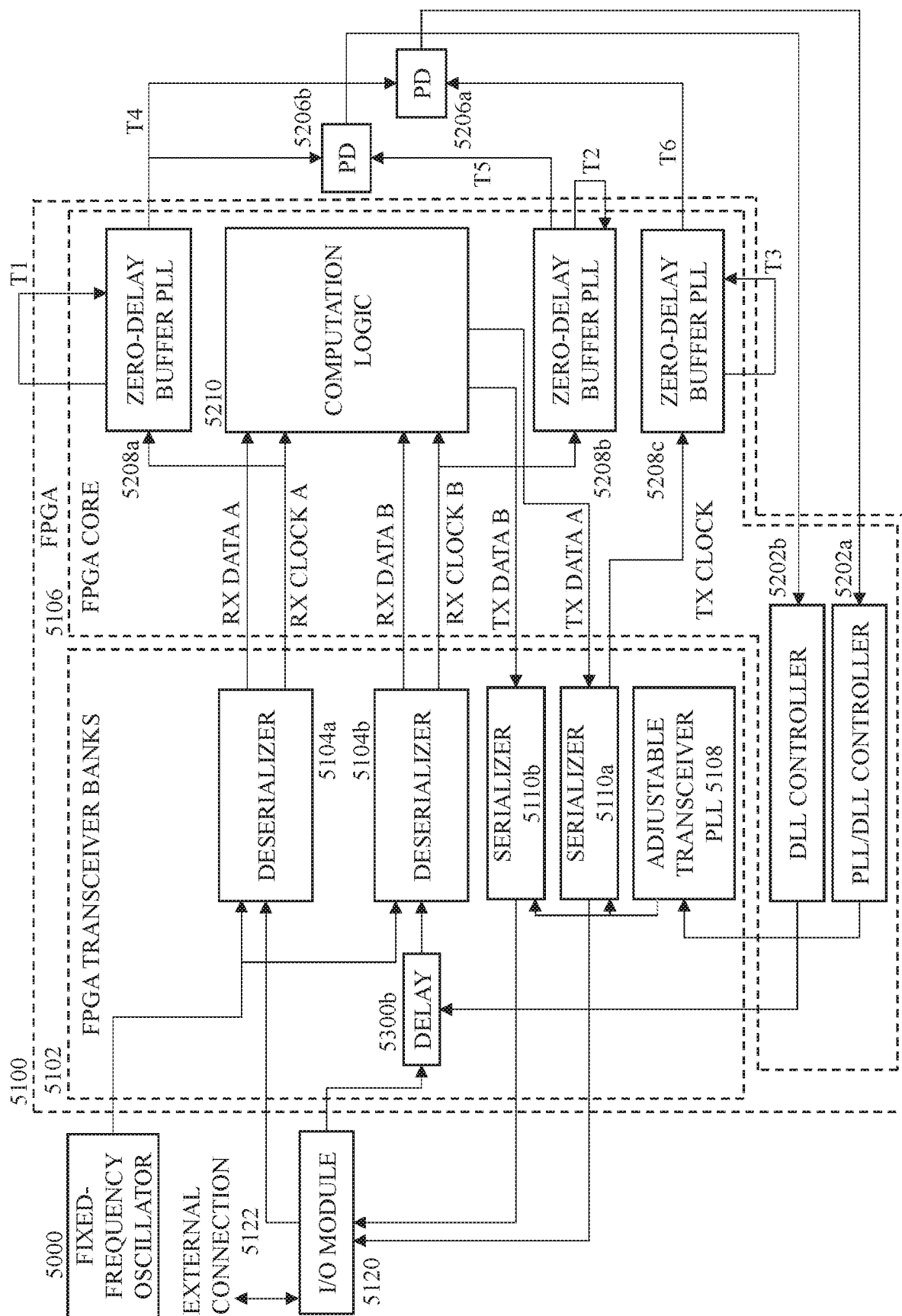


FIG. 5F

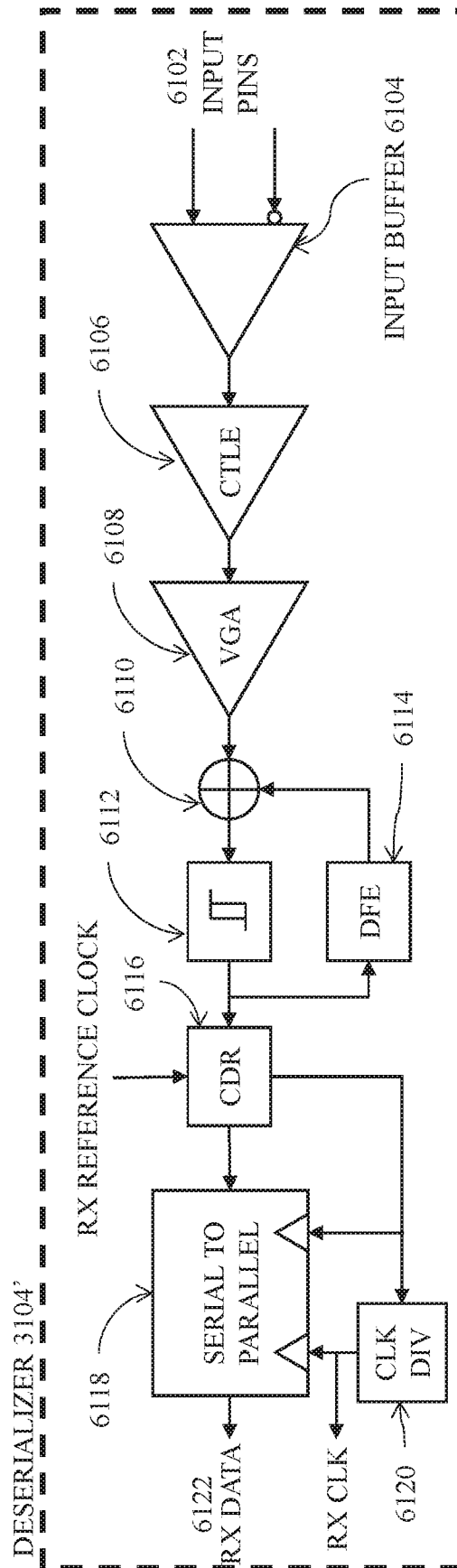


FIG. 6A

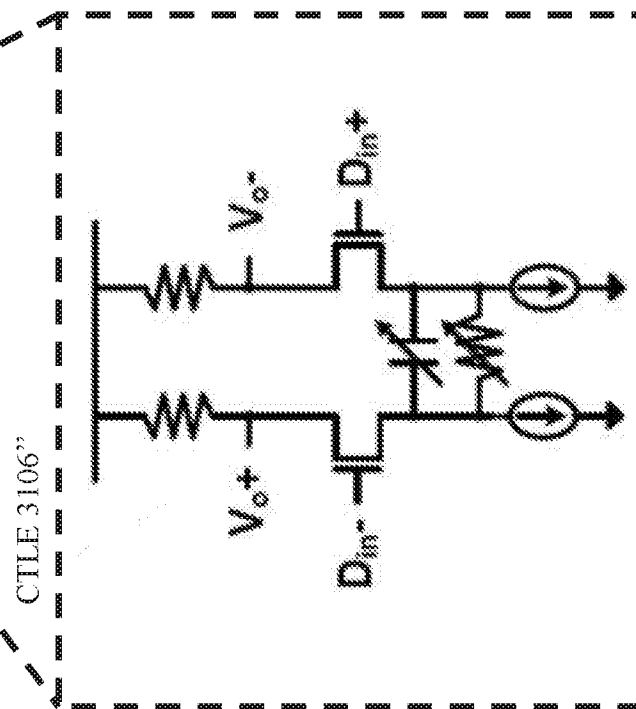
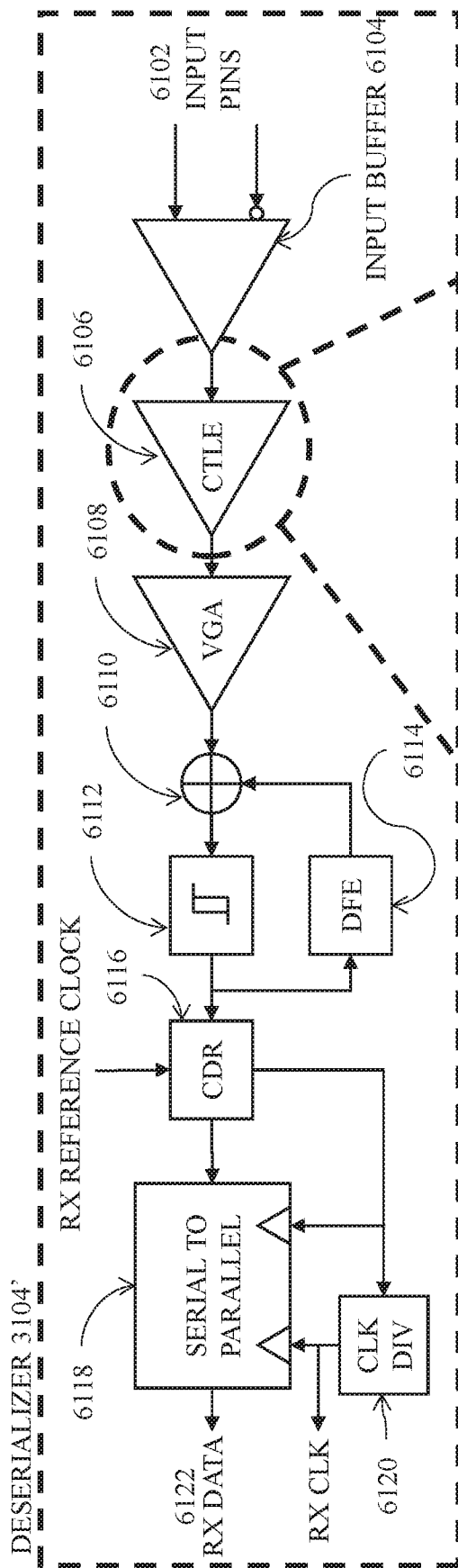


FIG. 6B

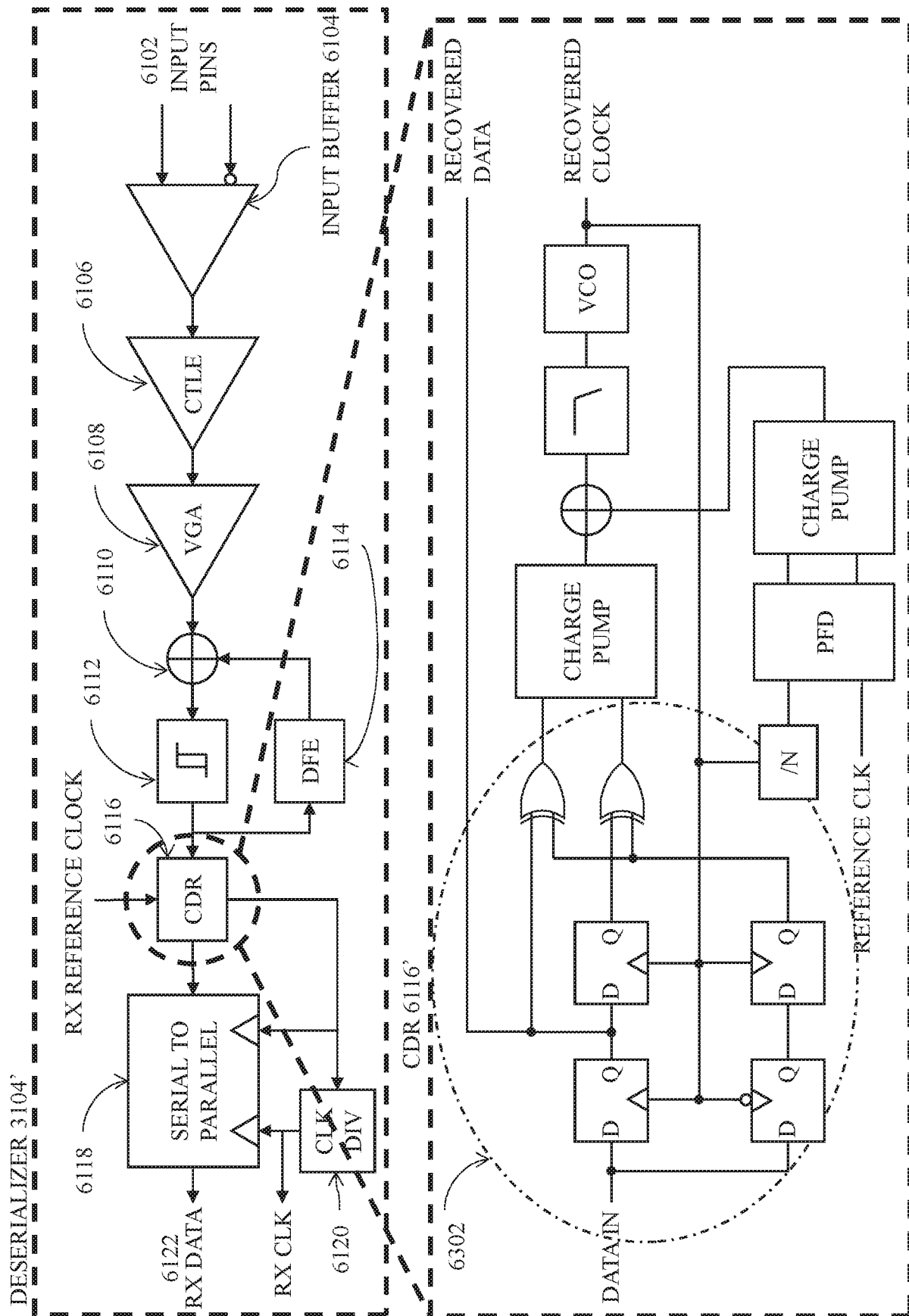


FIG. 6C

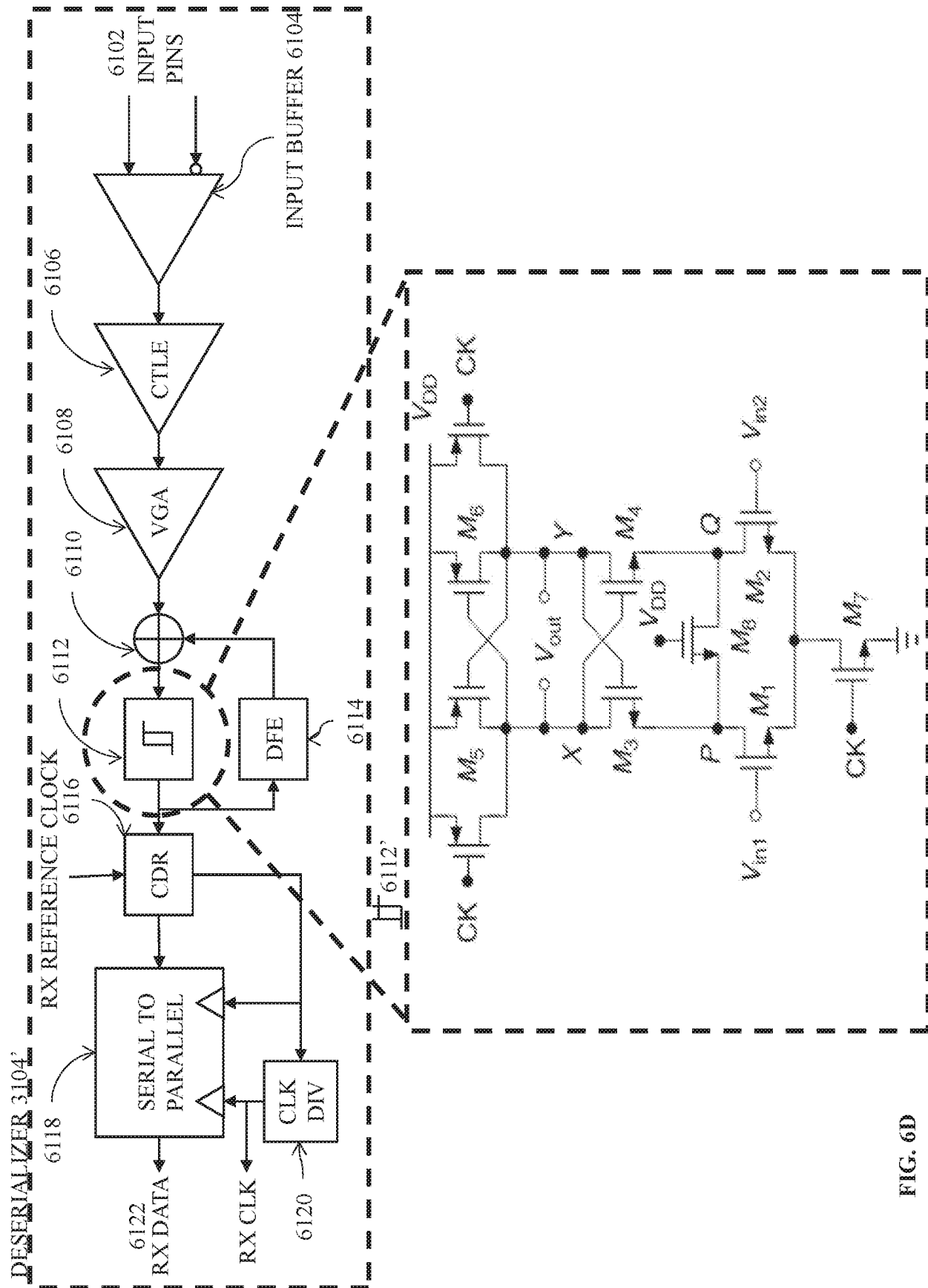


FIG. 6D

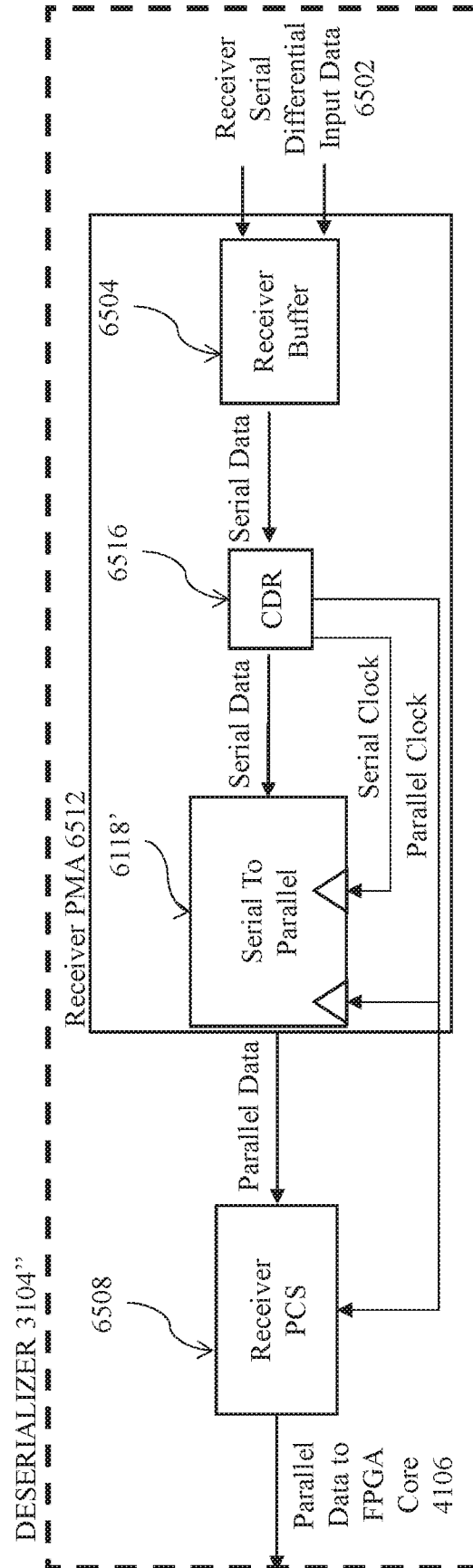
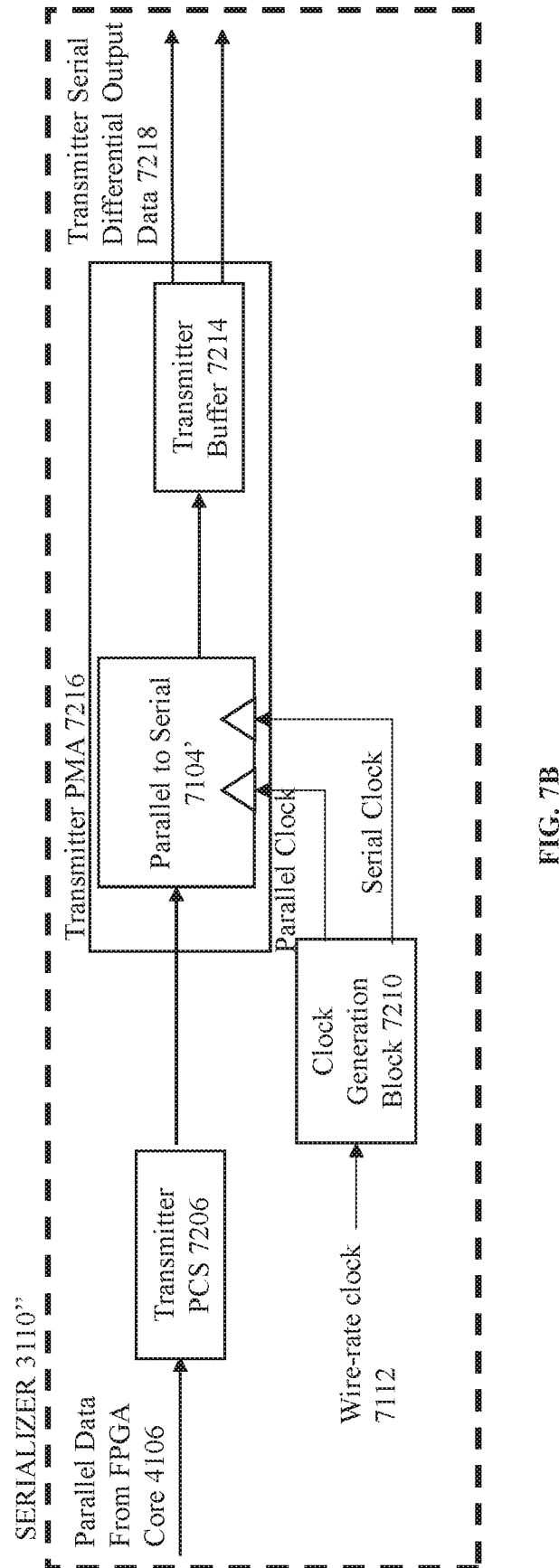
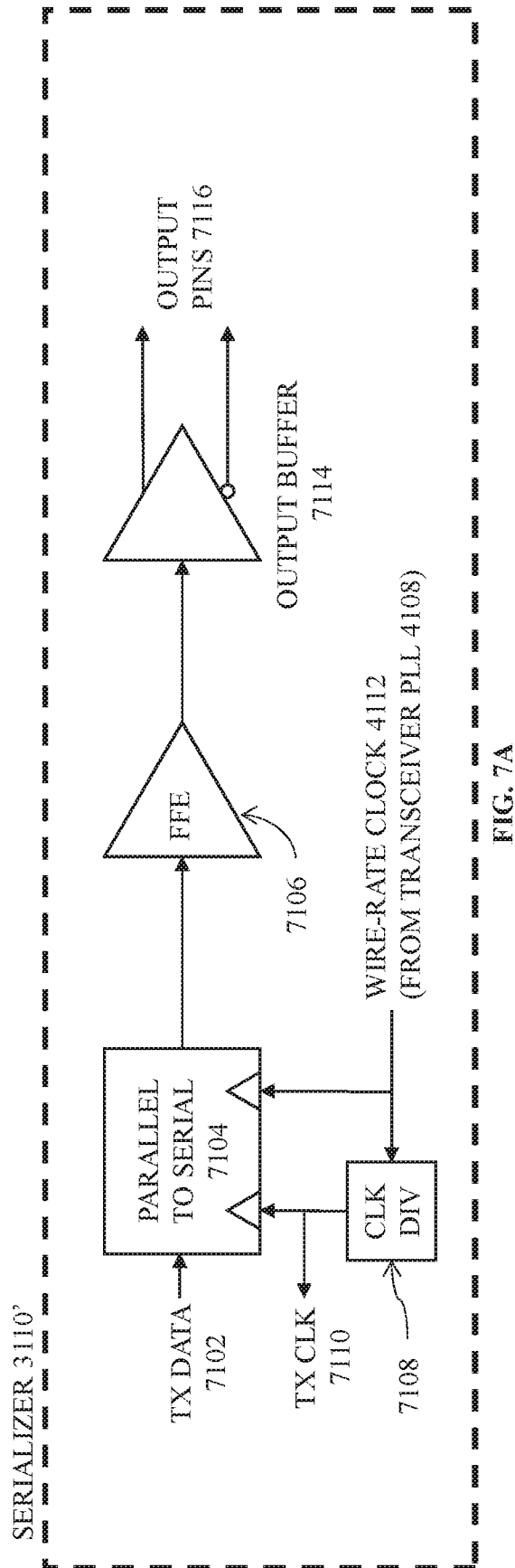


FIG. 6E



Phase Detector 3206''

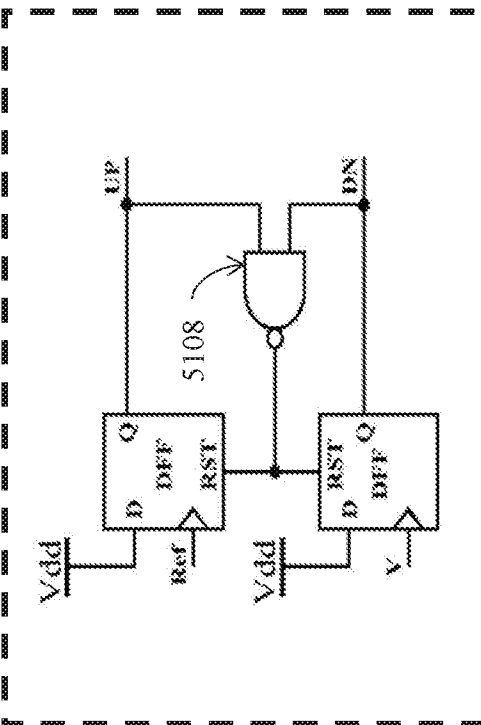


FIG. 8A

Phase Detector 3206''

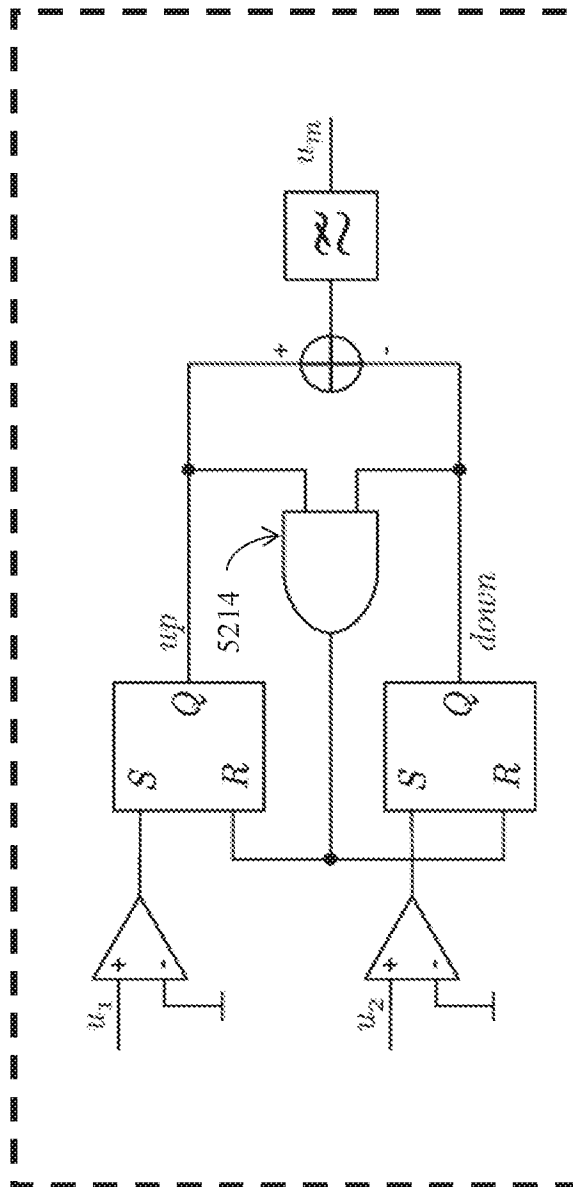
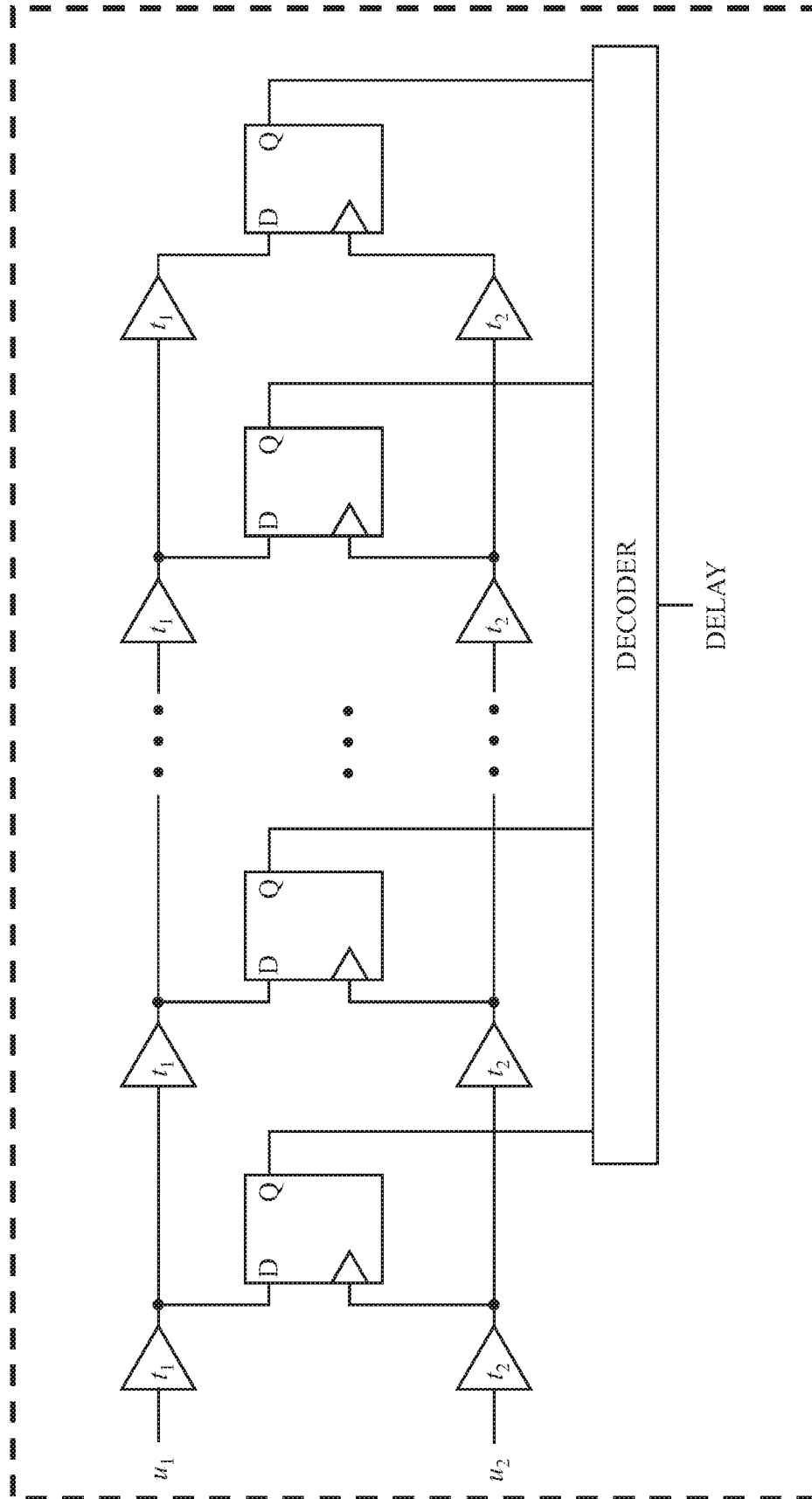


FIG. 8B

Phase Detector 3206³²²



PRIOR ART

FIG. 8C

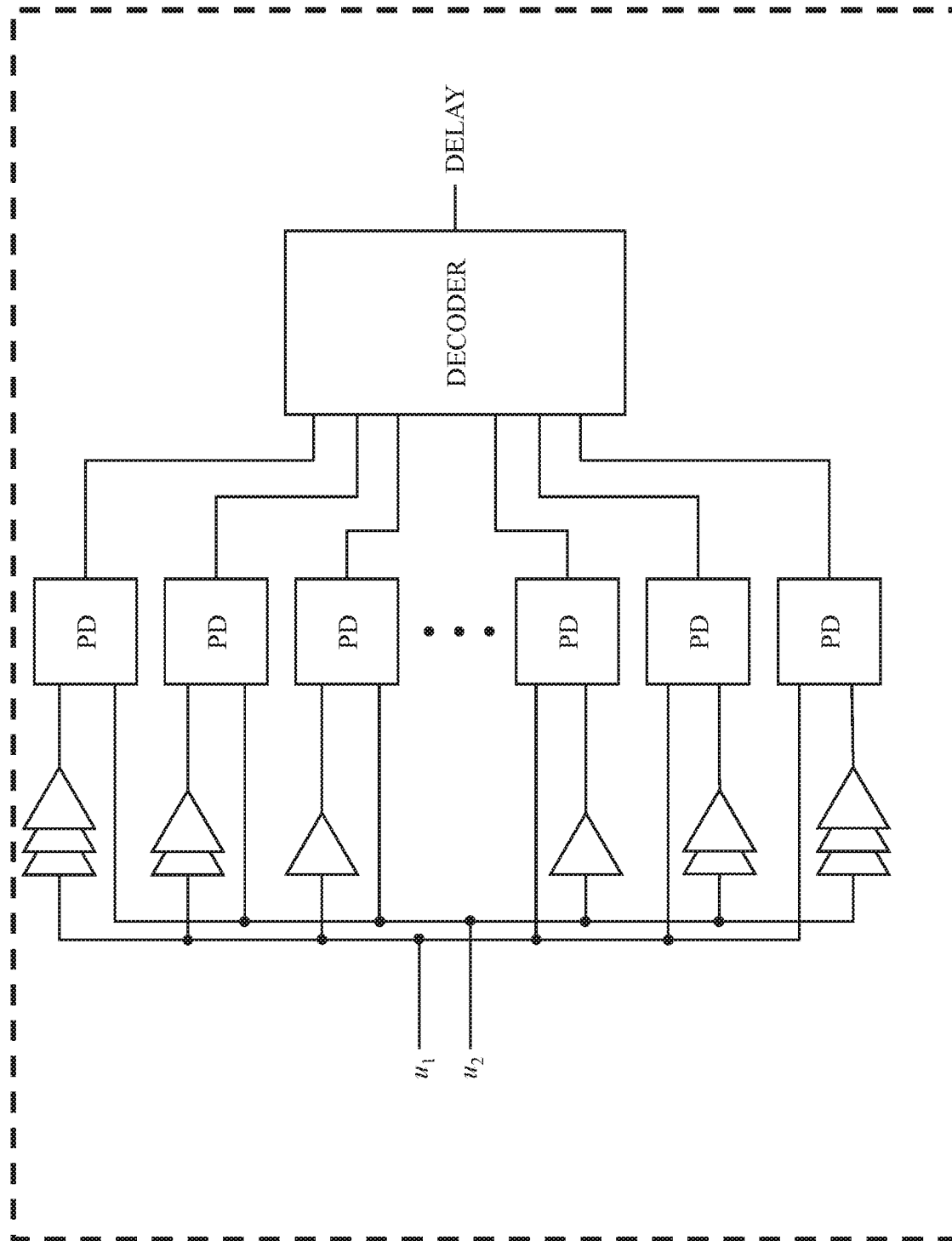


FIG. 8D

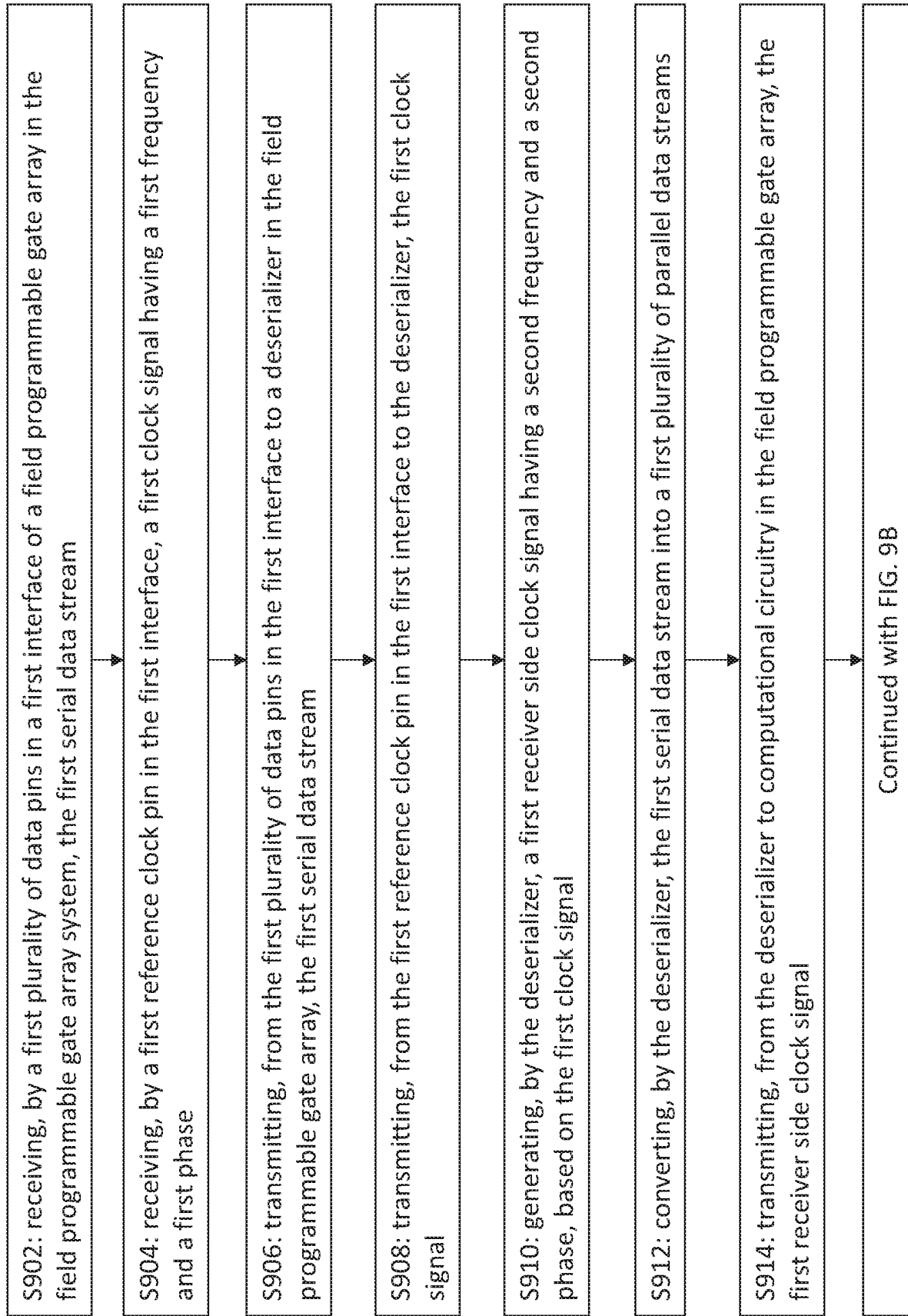


FIG. 9A

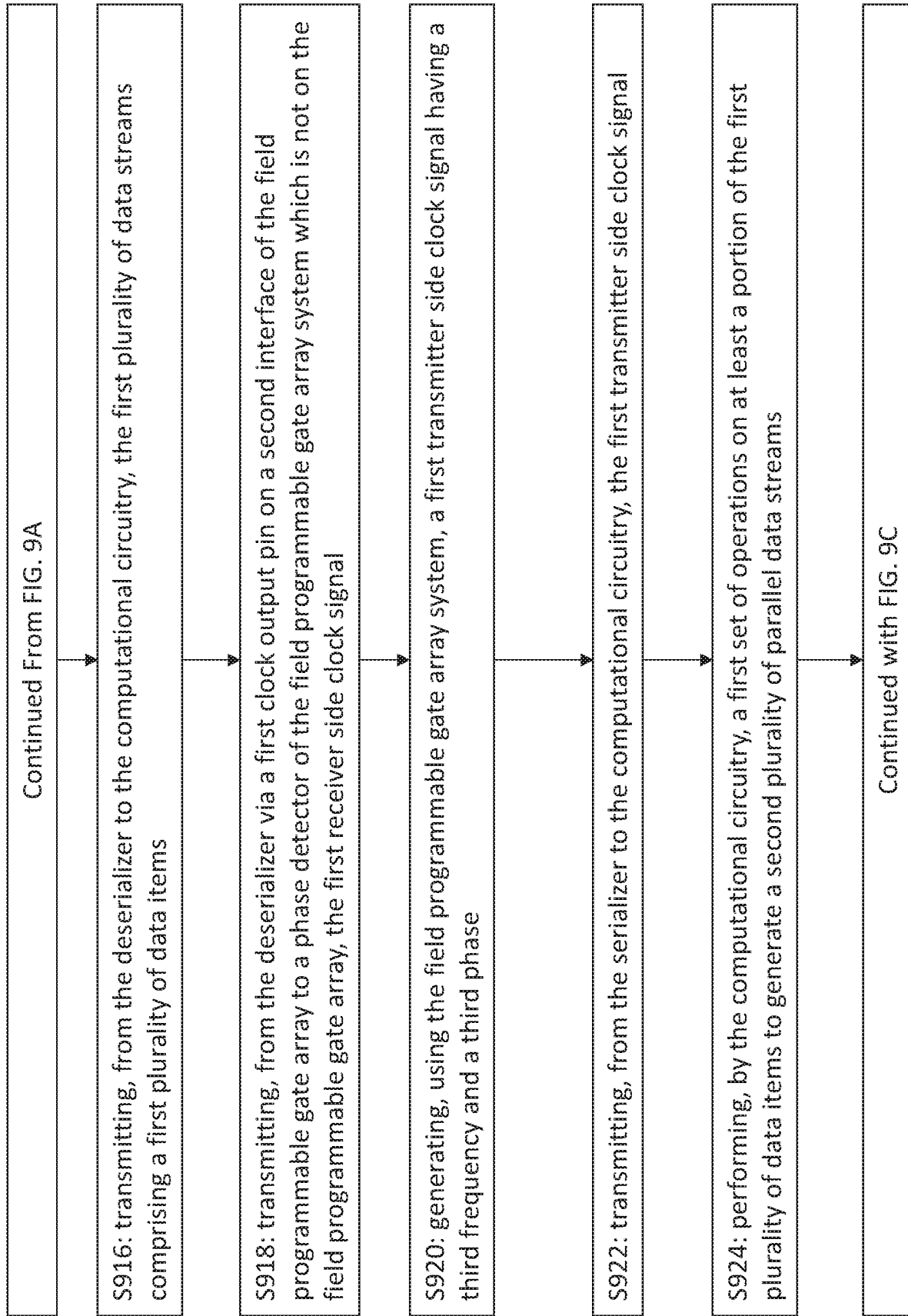


FIG. 9B

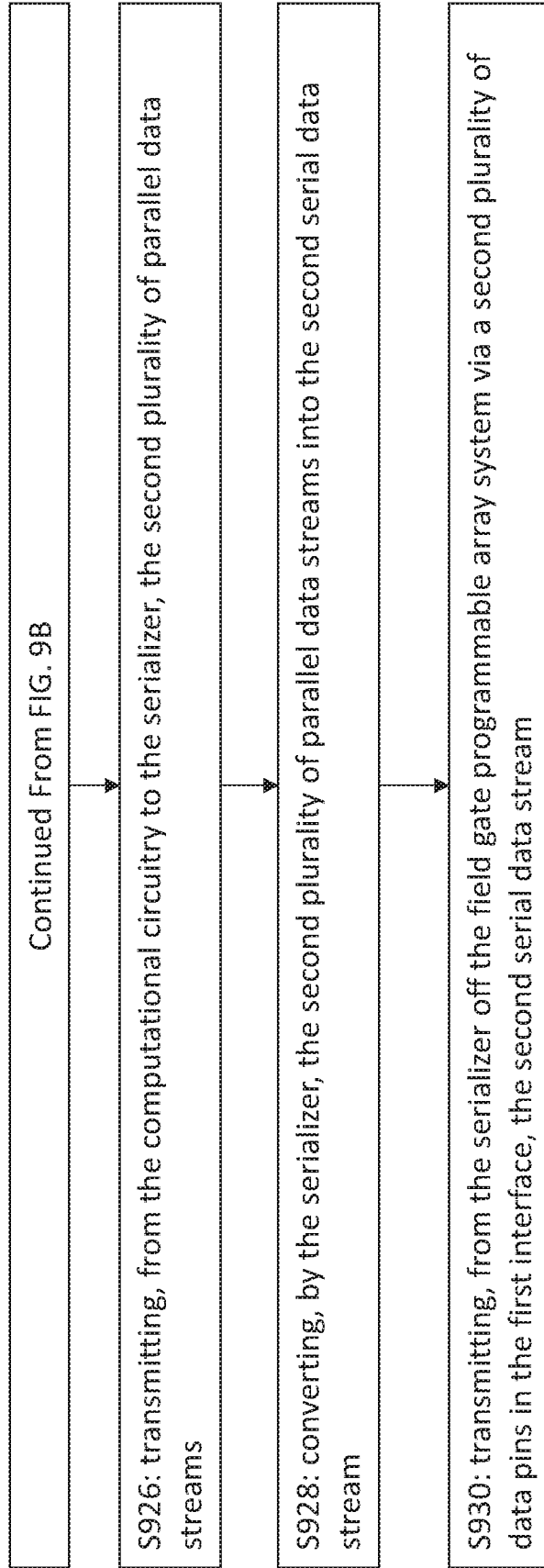


FIG. 9C

S920: generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level

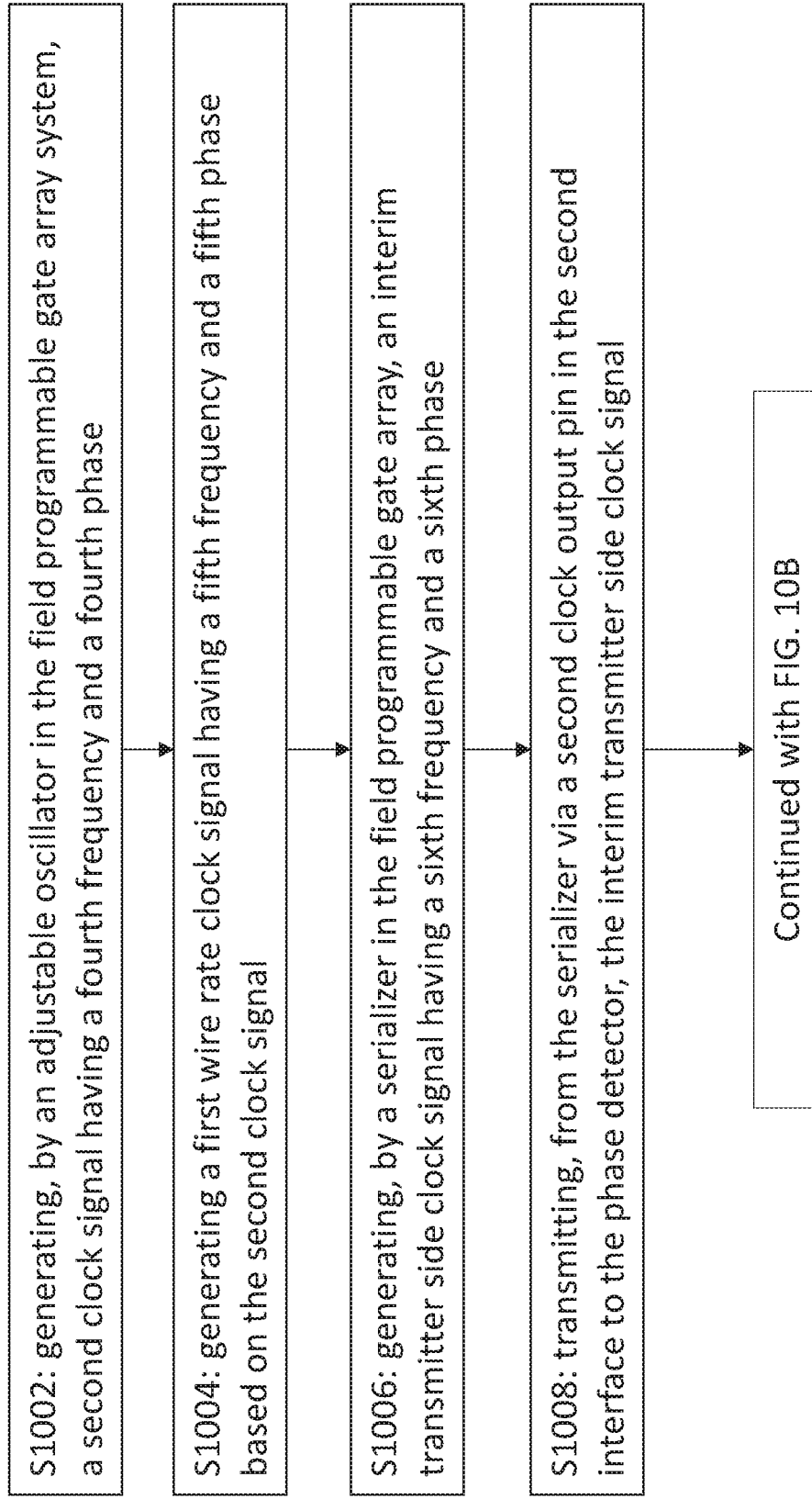


FIG. 10A

Continued From FIG. 10A

S1010: generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal

S1012: transmit, from the phase detector to a phase controller of the field programmable gate array system, which is placed within the field programmable gate array, the first output

S1014: determining, by the phase controller, interim adjustment information based on the first output

S1016: transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information, wherein the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps S1002 through S1016 are repeated until the first output of the phase detector is below the first threshold level

FIG. 10B

S1004: generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal

S1102: receiving, from the adjustable oscillator at a transceiver phase lock loop via a second reference clock pin in the first interface, the second clock signal

S1104: processing, by the transceiver phase lock loop, the received second clock signal

S1106: providing, by the transceiver phase lock loop, the first wire rate clock signal based on the processing of the received clock signal

S1108: transmitting, by the transceiver phase lock loop, the first wire rate clock signal to the serializer

FIG. 11

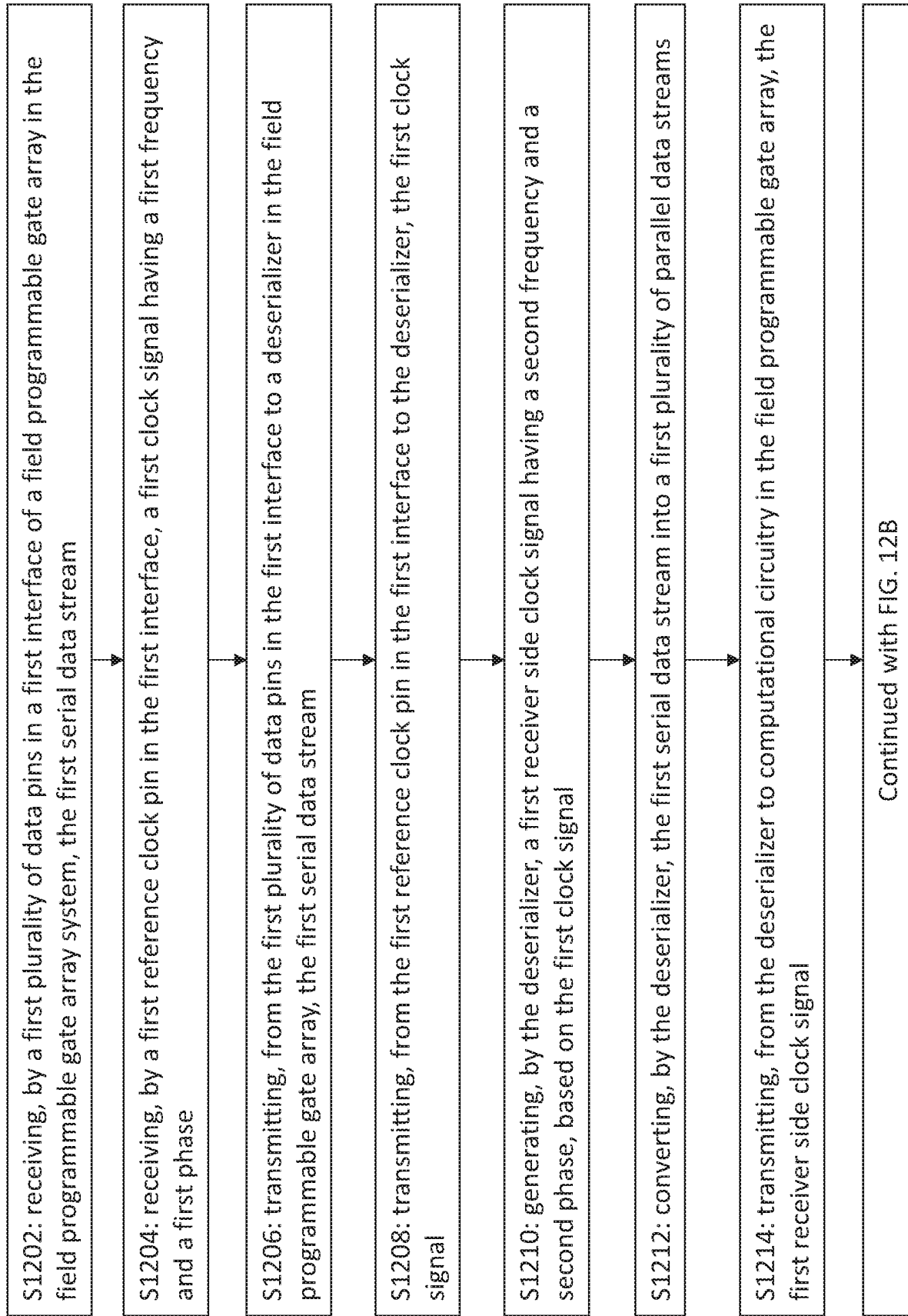


FIG. 12A

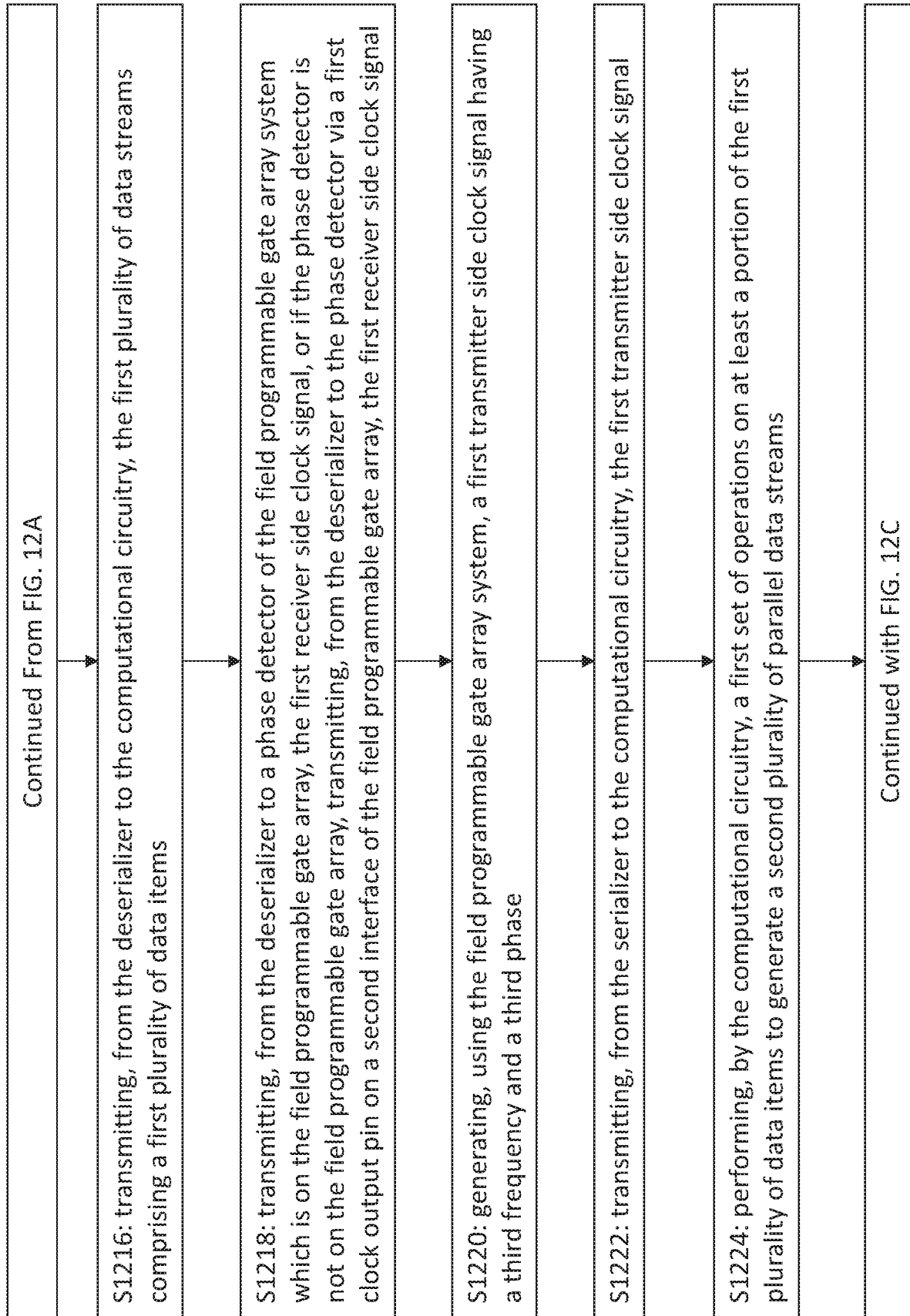


FIG. 12B

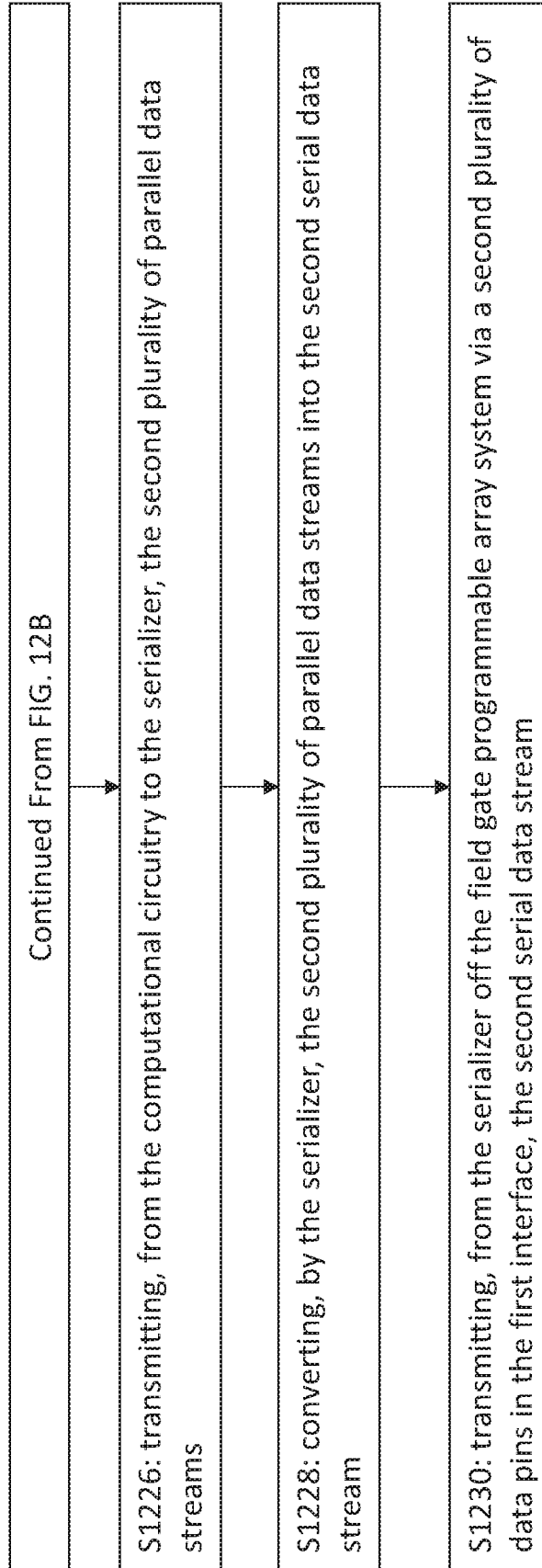


FIG. 12C

S1220: generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level

S1302: generating, by a phase lock loop with phase adjustment in the field programmable gate array system which is on the field programmable gate array, a second clock signal having a fourth frequency and a fourth phase

S1304: generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal

S1306: generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase

S1308: transmitting, from the serializer to the phase detector which is on the field programmable gate array, the interim transmitter side clock signal, or if the phase detector is not on the field programmable gate array, transmitting, from the serializer to the phase detector via a second clock output pin in the second interface, the interim transmitter side clock

Continued with FIG. 13B

FIG. 13A

Continued From FIG. 13A

S1310: generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal

S1312: transmit, from the phase detector to a phase controller of the field programmable gate array system, which is placed within the field programmable gate array, the first output

S1314: determining, by the phase controller, interim adjustment information based on the first output

S1316: transmitting, from the phase controller to the phase lock loop with phase adjustment, the interim adjustment information, wherein the phase lock loop with phase adjustment adjusts the second clock signal based on the interim adjustment information and steps S1302 through S1316 are repeated until the first output of the phase detector is below the first threshold level

FIG. 13B

S1204: generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal

S1402: receiving, from the phase lock loop with phase adjustment at a transceiver phase lock loop via a second reference clock pin in the first interface, the second clock signal

S1404: processing, by the transceiver phase lock loop, the received second clock signal

S1406: providing, by the transceiver phase lock loop, the first wire rate clock signal based on the processing of the received clock signal

S1408: transmitting, by the transceiver phase lock loop, the first wire rate clock signal to the serializer

FIG. 14

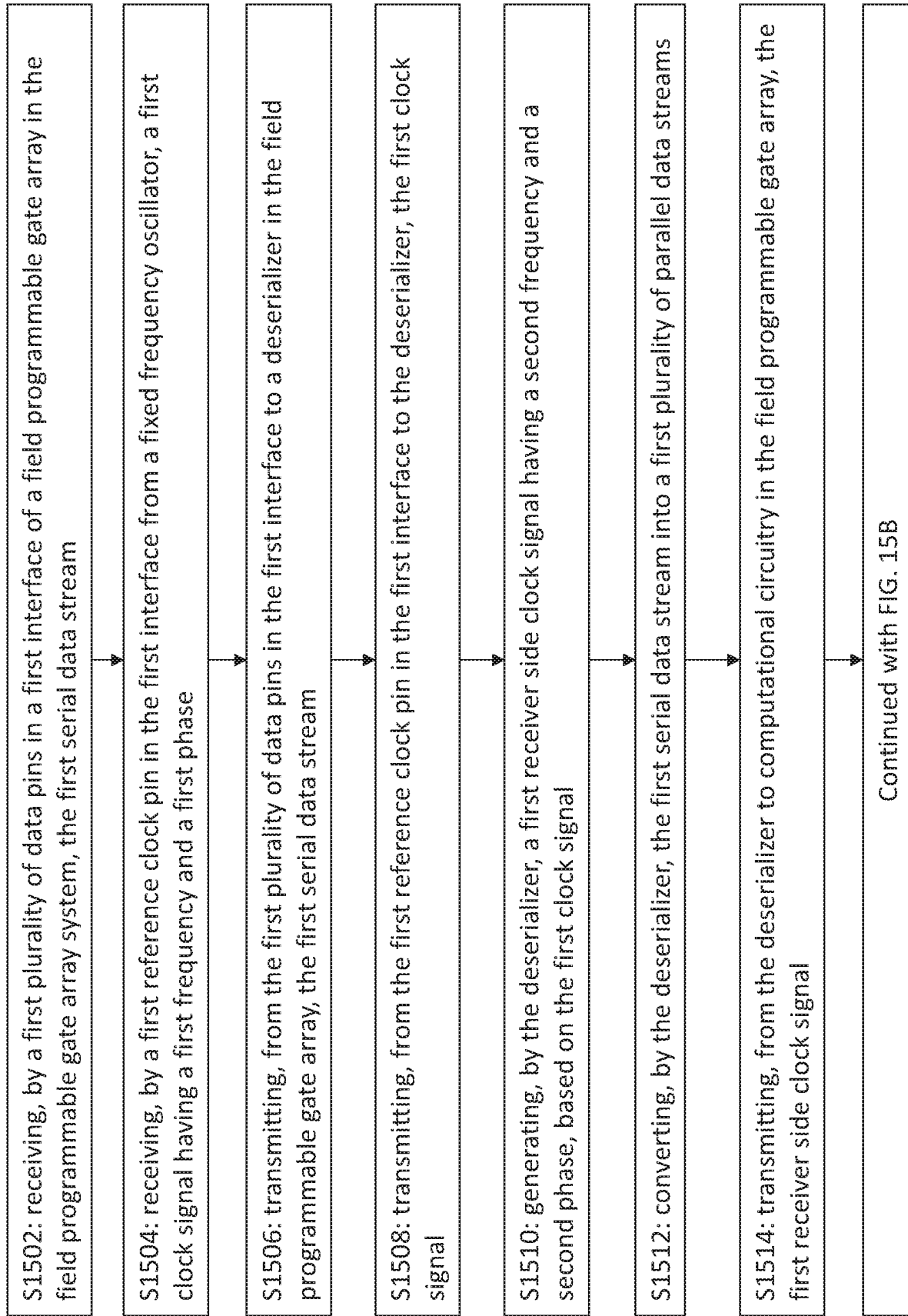


FIG. 15A

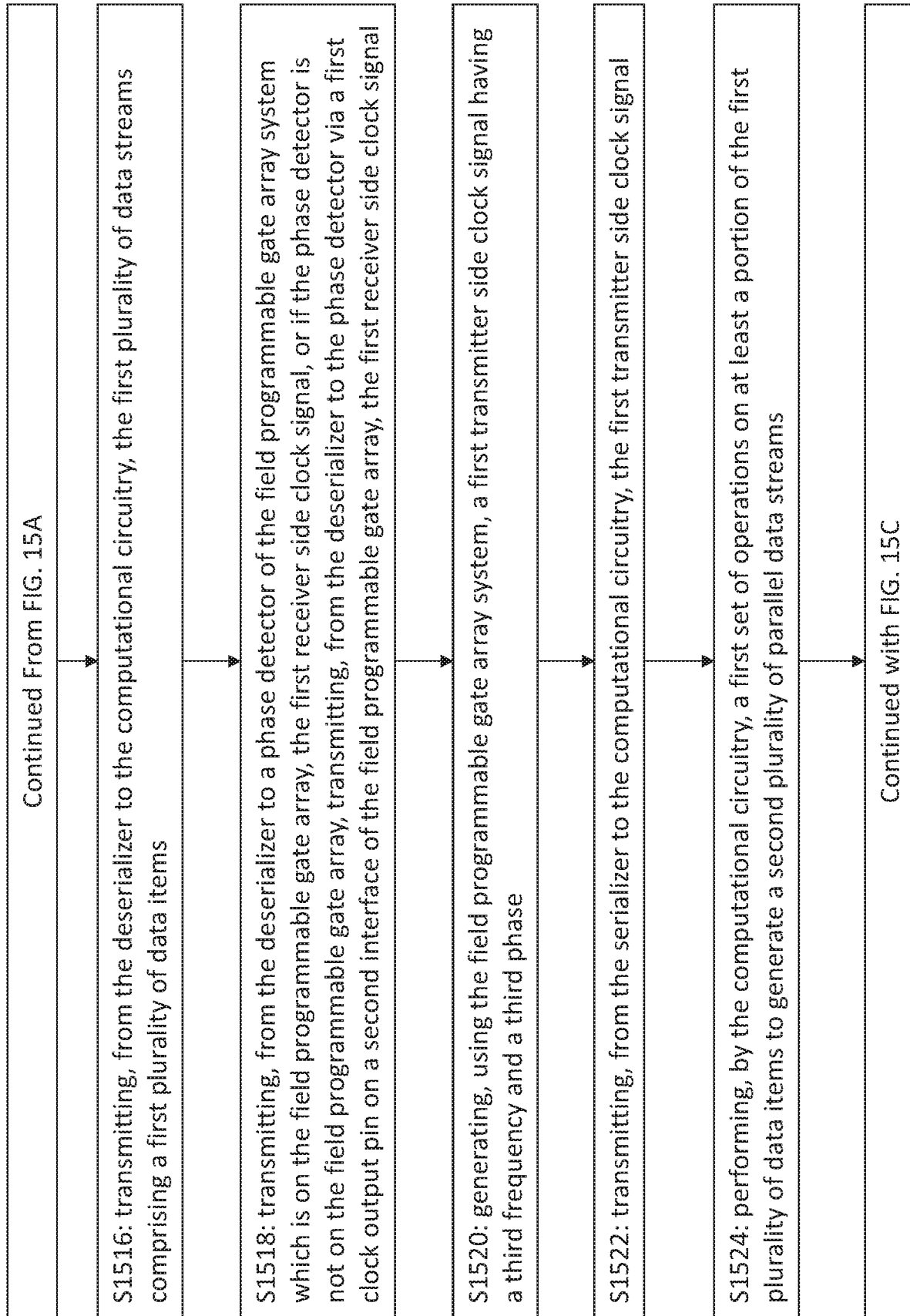


FIG. 15B

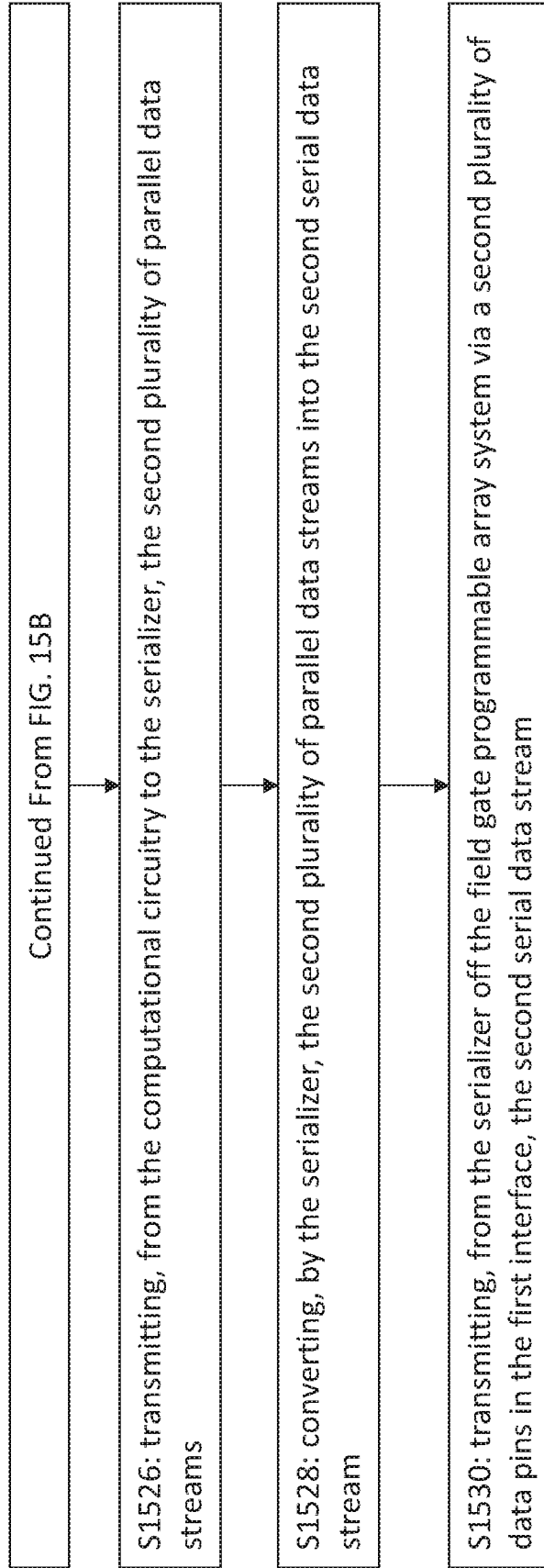


FIG. 15C

S1520: generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level

S1602: receiving, from the fixed frequency oscillator at an adjustable transceiver phase lock loop via a second reference clock pin in the first interface, the first clock signal to generate a second clock signal having a fourth frequency and a fourth phase

S1604: generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal and the interim adjustment information from the phase controller

S1606: generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase

S1608: transmitting, from the serializer to the phase detector which is on the field programmable gate array, the interim transmitter side clock signal, or if the phase detector is not on the field programmable gate array, transmitting, from the serializer to the phase detector via a second clock output pin in the second interface, the interim transmitter side clock signal

Continued with FIG. 16B

FIG. 16A

Continued From FIG. 16A

S1610: generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal

S1612: transmit, from the phase detector to a phase controller of the field programmable gate array system, which is placed within the field programmable gate array, the first output

S1614: determining, by the phase controller, interim adjustment information based on the first output

S1616: transmitting, from the phase controller to the adjustable transceiver phase lock loop, the interim adjustment information, wherein the adjustable transceiver phase lock loop adjusts the second clock signal based on the interim adjustment information and steps S1602 through S1616 are repeated until the first output of the phase detector is below the first threshold level

FIG. 16B

S1604: generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal and the interim adjustment information from the phase controller

S1702: generating, by the adjustable transceiver phase lock loop, the second clock signal based at least in part on the received first clock signal

S1704: processing, by the adjustable transceiver phase lock loop, the second clock signal based on the interim adjustment information received from the phase controller

S1706: providing, by the adjustable transceiver phase lock loop, the first wire rate clock signal based on the processing of the second clock signal

S1708: transmitting, by the adjustable transceiver phase lock loop, the first wire rate clock signal to the serializer

FIG. 17

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP		
First Named Inventor/Applicant Name:		Nima Badizadegan		
Filer:		Keith J. Barkaus/Victoria Gilmore		
Attorney Docket Number:		05301-0009		
Filed as Small Entity				
Filing Fees for Track I Prioritized Examination - Nonprovisional Application under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	75	75
UTILITY SEARCH FEE	2111	1	330	330
UTILITY EXAMINATION FEE	2311	1	380	380
REQUEST FOR PRIORITIZED EXAMINATION	2817	1	2000	2000
Pages:				
UTILITY APPL SIZE FEE PER 50 SHEETS >100	2081	1	200	200
Claims:				
CLAIMS IN EXCESS OF 20	2202	2	50	100

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous-Filing:				
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
PROCESSING FEE, EXCEPT PROV. APPLS.	2830	1	70	70
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				3155

Electronic Acknowledgement Receipt

EFS ID:	39581003
Application Number:	16888218
International Application Number:	
Confirmation Number:	2004
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP
First Named Inventor/Applicant Name:	Nima Badizadegan
Customer Number:	1912
Filer:	Keith J. Barkaus/Victoria Gilmore
Filer Authorized By:	Keith J. Barkaus
Attorney Docket Number:	05301-0009
Receipt Date:	29-MAY-2020
Filing Date:	
Time Stamp:	18:04:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$3155
RAM confirmation Number	E20205SI05005125
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	TrackOne Request	1-Track1Req.pdf	114447	no	2
			54f7d35974cf3d06a3f8729b7965fdfed19c9d3c		
Warnings:					
Information:					
2	Application Data Sheet	2-ADS.pdf	1255861	no	8
			f02248015e7b34c1bb04d77eecdad82c4c9519b6		
Warnings:					
Information:					
3	Power of Attorney	3-PowerofAtty.pdf	367244	no	2
			8ffc1e469481197305e07c2b6b187259bd81576		
Warnings:					
Information:					
4	Oath or Declaration filed	4-Declaration.pdf	157360	no	1
			75ed7b6f11b5ccf5fd555e0db8081e4992c41060		
Warnings:					
Information:					
5		5-Specification.pdf	471609	yes	107
			9b716c84fa730201f7b66629216073900bb6cc5d		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Abstract		107	107	
	Claims		102	106	
	Specification		1	101	

Warnings:					
Information:					
6	Drawings-only black and white line drawings	6-Drawings.pdf	1159540	no	47
			d276e458855e40689608f5c12049f9175c5b3d37		
Warnings:					
Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	43382	no	2
			aad19fa68de6d6d3514026b5166cf2fa5775484b		
Warnings:					
Information:					
Total Files Size (in bytes):			3569443		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

**CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION
UNDER 37 CFR 1.102(e) (Page 1 of 1)**

First Named Inventor:	Nima Badizadegan	Nonprovisional Application Number (if known):	
Title of Invention:	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i)(1) and the prioritized examination fee set forth in 37 CFR 1.17(c) have been filed with the request. The publication fee requirement is met because that fee, set forth in 37 CFR 1.18(d), is currently \$0. The basic filing fee, search fee, and examination fee are filed with the request or have been already been paid. I understand that any required excess claims fees or application size fee must be paid for the application.
2. I understand that the application may not contain, or be amended to contain, more than four independent claims, more than thirty total claims, or any multiple dependent claims, and that any request for an extension of time will cause an outstanding Track I request to be dismissed.
3. The applicable box is checked below:

I. ☒ Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)

- i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.
---OR---
(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.
- ii. An executed inventor's oath or declaration under 37 CFR 1.63 or 37 CFR 1.64 for each inventor, or the application data sheet meeting the conditions specified in 37 CFR 1.53(f)(3)(i) is filed with the application.

II. ☐ Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)

- i. A request for continued examination has been filed with, or prior to, this form.
- ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
- iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
- iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
- v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature /Keith J. Barkaus/	Date 2020-05-29
Name (Print/Typed) Keith J. Barkaus	Practitioner Registration Number 51,431

Note: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required.*

☒ *Total of 1 forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	05301-0009
		Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--------------------------	---

Inventor Information:

Inventor	1				Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Nima		Badizadegan			
Residence Information (Select One) • ☒ US Residency ☐ Non US Residency ☐ Active US Military Service						
City	New York	State/Province	NY	Country of Residence	US	
Mailing Address of Inventor:						
Address 1	455 W 37th Street, #716					
Address 2						
City	New York	State/Province	NY			
Postal Code	10018	Country	US			
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add						

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	01912		
Email Address	ptodocket@arelaw.com		Add Email Remove Email

Application Information:

Title of the Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP		
Attorney Docket Number	05301-0009	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	47	Suggested Figure for Publication (if any)	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	05301-0009
		Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP		

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☒ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	01912		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	16670702	2019-10-31

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	05301-0009
		Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP		
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16670702	Claims benefit of provisional	62808404	2019-02-21
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ⁱ (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	05301-0009
	Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	05301-0009
		Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.				
Applicant	1	Remove		
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.				
Clear				
Assignee	Legal Representative under 35 U.S.C. 117		Joint Inventor	
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest		
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:				
Name of the Deceased or Legally Incapacitated Inventor:				
If the Applicant is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Applicant:				
Address 1				
Address 2				
City		State/Province		
Country		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Applicant Data may be generated within this form by selecting the Add button. Add				

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	05301-0009
		Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP		

Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
Remove				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country ⁱ		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add				

Signature:					Remove
NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).					
This Application Data Sheet must be signed by a patent practitioner if one or more of the applicants is a juristic entity (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, all joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of all joint inventor-applicants.					
See 37 CFR 1.4(d) for the manner of making signatures and certifications.					
Signature	/Keith J. Barkaus/			Date (YYYY-MM-DD)	2020-05-29
First Name	Keith J.	Last Name	Barkaus	Registration Number	51,431
Additional Signature may be generated within this form by selecting the Add button. Add					

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	05301-0009
		Application Number	
Title of Invention	FIELD PROGRAMMABLE GATE ARRAY WITH INTERNAL PHASE-LOCKED LOOP		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

- 1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
- 2 A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
- 3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
- 4 A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
- 5 A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
- 6 A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
- 7 A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
- 8 A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
- 9 A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

SCORE Placeholder Sheet for IFW Content

Application Number: 16888218

Document Date: 05/29/2020

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

- Drawing

At the time of document entry (noted above):

- USPTO employees may access SCORE content via DAV or via the SCORE web page.
- External customers may access SCORE content via PAIR using the Supplemental Content tab.