UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

OPTIVER US LLC and OPTIVER TRADING US LLC,
Petitioners

v.

HFT SOLUTIONS, LLC,
Patent Owner.

Case No. IPR2026-00384
U.S. Patent No. 10,763,865

Corrected Petition for *Inter Partes* Review of U.S. Patent No. 10,763,865

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TABLE OF EXHIBITS

Exhibit No.	Document
1001	U.S. Patent No. 10,763,865 ("the '865 patent")
1002	File History for U.S. Patent No. 10,763,865
1003	Declaration of Benjamin Carrion Schaefer, Ph.D.
1004	Declaration of Carrie Gardner
1005	R. Giordano and A. Aloisio, *Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs*, 58-1 IEEE Transactions on Nuclear Science 194 (2011) [Giordano]
1006	*(intentionally omitted)*
1007	U.S. Pat. No. 10,447,463 [Raymond]
1008	*(intentionally omitted)*
1009	Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 [Virtex-UG]
1010	U.S. Pat. No. 7,453,301 [Kaviani]
1011	Declaration of Gordon MacPherson
1012	Curriculum Vitae of Benjamin Carrion Schaefer, Ph.D.
1013	Redline of Corrected Petition for *Inter Partes Review* of U.S. Patent No. 10,763,865
1014	Redline of Corrected Declaration of Benjamin Carrion Schaefer, Ph.D.

TABLE OF ABBREVIATIONS

Abbreviation	Term
’865 patent	U.S. Patent No. 10,763,865
AIA	America Invents Act
Challenged Claims	Claims 1–21 of U.S. Patent No. 10,763,865
Ex.	Exhibit
Fig.	Figure
IPR	*inter partes* review
Patent Owner	HFT Solutions, LLC
Petitioners	Optiver US LLC and Optiver Trading US LLC
Giordano	R. Giordano and A. Aloisio, *Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs*, 58-1 IEEE Transactions on Nuclear Science 194 (2011)
Kaviani	U.S. Pat. No. 7,453,301
Raymond	U.S. Pat. No. 10,447,463
Virtex-UG	Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009
CDC	Clock Domain Crossing
CDR	Clock and Data Recovery
DLL	Delay Locked Loop
PLL	Phase Locked Loop
FPGA	Field Programmable Gate Array
PMA	Physical Medium Attachment
PCS	Physical Coding Sublayer
MAC	Media Access Controller
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration

MANDATORY NOTICES

A. Real Parties-in-Interest: 37 C.F.R. §42.8(b)(1)

Optiver US LLC and Optiver Trading US LLC are the real parties-in-interest. Optiver Services US LLC is a corporate affiliate and services entity supporting Optiver US LLC and Optiver Trading US LLC. The ultimate parent company of all three entities is Optiver Holding BV.

B. Related Matters Under: 37 C.F.R. §42.8(b)(2)

1. Current Litigation

The ’865 patent is presently not subject to any litigation. Petitioners are not aware of any litigation involving the ’865 patent.

2. Administrative Proceedings

There are no other administrative proceedings at issue. Petitioners have filed or intend to file petitions for *inter partes* review regarding four additional patents—U.S. Pat. Nos. 12,107,587 (IPR2026-00383); 11,018,678 (IPR2026-00385); 10,771,069 (IPR2026-00386); and 11,329,655 (IPR2026-00387)—in the same patent family as the ’865 patent.

C. Lead and Back-Up Counsel: 37 C.F.R. §42.8(b)(3)

Petitioners provide the following designation of counsel:

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Petitioners respectfully request authorization to file motions for Brian Rosenthal to appear before the USPTO *pro hac vice*. Mr. Rosenthal is an experienced attorney and is currently serving as lead counsel for Petitioners in an action between Petitioners and Patent Owner.[1] He is familiar with the subject matter at issue in this proceeding. Petitioners intend to file a motion to appear *pro hac vice* under 37 C.F.R. §42.10. Pursuant to 37 C.F.R. §42.10(b), powers of attorney accompany this petition.

[1] Petitioners are currently defending Patent Owner's assertion of U.S. Pat. Nos. 10,931,286; 11,128,305; 11,575,381 in *HFT Solutions, LLC v. Optiver US LLC and Optiver Trading US LLC*, 7:25-cv-415 (W.D. Tex. filed Sept. 8, 2025). These three patents list the same sole inventor (Nima Badizadegan) as the '865 patent but belong to a separate patent family.

D. Service of Information: 37 C.F.R. §42.8(b)(4)

Service of any documents via hand delivery may be made at the mailing address of lead and backup counsel. Petitioners also consent to electronic service, and service via electronic mail may be made at the email addresses provided for the lead and backup counsel.

I. INTRODUCTION

Pursuant to 35 U.S.C. §311, Petitioners seek *inter partes* review of U.S. Pat. No. 10,763,865 (Ex. 1001) and cancellation of claims 1–21 as unpatentable under 35 U.S.C. §103.

The Challenged Claims are directed to an FPGA system that receives and transmits data using synchronized receiver and transmitter clock signals. Ex. 1001, 1:18–23. The alleged invention of the '865 patent is in using an "internal phase-locked loop" for "***phase matching*** receiver side and transmitter side clocks of a FPGA without introducing unnecessary delay in processing." *Id.*, 2:12–15.[2] The Challenged Claims purport to achieve this phase matching with a "phase detector" that is "not part of the [FPGA]," and a "phase controller" that is "placed within the [FPGA]." *Id.*, cl. 1.

Yet the prior art taught these concepts before the '865 patent. **Giordano**, the primary reference for all grounds in this petition, teaches aligning clock signals for serialization/deserialization ("SER/DES") processes with a deterministic, fixed phase difference. Ex. 1005, 197. Giordano plainly discloses performing everything in claims 1–18, 21 using Xilinx FPGA systems, but lacks certain details of off-FPGA components and how the phase alignment is achieved. **Kaviani**, a Xilinx patent, and

[2] Unless noted otherwise, emphasis added.

Virtex-UG, a Xilinx user guide, disclose these details. Kaviani discloses elements, implemented in separate circuitry, that disclose the "phase detector" off the FPGA and "phase controller" that is within the FPGA. Virtex-UG teaches specifics of the clock phase alignment features inherent to the Virtex-5 FPGAs used in Giordano. Given the programmable nature of FPGAs (which allows users to modify hardware as needed) and Giordano's guidance to seek further specifics of phase alignment, a POSITA would have found it obvious to incorporate the teachings of Kaviani and/or Virtex-UG into Giordano's FPGA system. Ex. 1005, 198; Ex. 1010, 1:36–43, Fig. 2.

Claims 19 and 20 of the '865 patent add only the application of these well-known FPGA systems to financial trading. **Raymond** expressly teaches using FPGA systems and phase matching (as in Giordano, Kaviani, and Virtex-UG) in high-frequency trading applications. Ex. 1007, 1:18–38. Applying the known FPGA phase matching teachings disclosed in Giordano, Kaviani, and Virtex-UG to financial-trading applications as suggested by Raymond would have been straightforward and obvious. *See also* Ex. 1001, 1:41–43 ("FPGAs are used in the financial industry").

Because this Petition demonstrates a reasonable likelihood that Petitioners will prevail on at least one challenged claim based on prior art not considered during prosecution, the Board should institute *inter partes* review ("IPR") and cancel claims 1–21 under 35 U.S.C. §103.

II. REQUIREMENTS OF IPR

A. Standing: 37 C.F.R. §42.104(a)

Petitioners certify that the ’865 patent is eligible for IPR and that Petitioners are not barred or estopped from requesting IPR of the Challenged Claims.

B. Identification of Challenge and Relief Requested: 37 C.F.R. §42.104(b)

Petitioners request IPR of claims 1–21 of the ’865 patent under AIA 35 U.S.C. §103.

The ’865 patent issued from an application filed May 29, 2020, and claims priority to a provisional application filed February 21, 2019. For purposes of this Petition only, Petitioners do not dispute that the Challenged Claims are entitled to an effective filing date of February 21, 2019.

Petitioners request cancellation of claims 1–21 based on:

Ground	Claims	Basis for Rejection[3]
1	1–18, 21	Obviousness over Giordano in view of Kaviani
2	1–21	Obviousness over Giordano in view of Kaviani further in view of Raymond
3	1–18, 21	Obviousness over Giordano in view of Kaviani further in view of Virtex-UG[4]

[3] All obviousness grounds include the knowledge of a POSITA.
[4] Giordano inherently discloses the features of Virtex-UG, and further incorporates Virtex-UG by reference. Ex. 1003, ¶¶77, 118. To the extent a POSITA would not have understood the features of Virtex-5 are necessarily present in Giordano, a

(Cont'd on next page)

Ground	Claims	Basis for Rejection[3]
4	1–21	Obviousness over Giordano in view of Kaviani, Virtex-UG, and Raymond

1. R. Giordano and A. Aloisio, *Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs*, 58-1 IEEE Transactions on Nuclear Science 194 (2011) ("Giordano") (Ex. 1005)

Giordano was published in IEEE Transactions on Nuclear Science on January 28, 2011. Ex. 1004, ¶¶21–26; *id*., ¶27, 33–34, 37 (citing Ex. 1011). Giordano qualifies as prior art under AIA 35 U.S.C. §102(a)(1). Giordano was neither cited nor considered during prosecution of the '865 patent.

2. Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 ("Virtex-UG") (Ex. 1009)

Virtex-UG was published on December 3, 2009. Ex. 1004, ¶¶41–47. Virtex-UG qualifies as prior art under AIA 35 U.S.C. §102(a)(1). Virtex-UG was neither cited nor considered during prosecution of the '865 patent.

3. U.S. Pat. No. 7,453,301 ("Kaviani") (Ex. 1010)

Kaviani, titled "Method of and Circuit for Phase Shifting a Clock Signal," was filed August 5, 2005, and granted November 18, 2008. Kaviani qualifies as prior art under AIA 35 U.S.C. §102(a)(1) and §102(a)(2). Kaviani was neither cited nor considered during prosecution of the '865 patent.

POSITA would have been motivated to combine Virtex-UG to all grounds based on Giordano.

4. U.S. Pat. No. 10,447,463 ("Raymond") (Ex. 1007)

Raymond, titled "Device and Method for Ultra-low Latency Communication," claims priority to a provisional application filed July 13, 2017, and an application filed July 13, 2018. Raymond qualifies as prior art under AIA 35 U.S.C. §102(a)(2). Raymond was neither cited nor considered during prosecution of the '865 patent.

C. Claim Construction: 37 C.F.R. §42.104(b)(3)

Petitioners submit that no construction of any claim term is necessary for the Board to resolve, and the Challenged Claims would have been obvious under any reasonable construction.

D. Challenge: 37 C.F.R. §42.104(b)(4)

Explanation of how the Challenged Claims are unpatentable under the grounds identified above, including where each claim element is found in the prior art, is provided below.

E. Supporting Evidence: 37 C.F.R. §42.104(b)(5)

The supporting exhibits, their relevance to the Challenged Claims, and the specific portions supporting the asserted grounds are identified below. The Petition's technical analysis and grounds are further supported by the Declaration of Dr. Benjamin Carrion Schaefer (Ex. 1003). The public availability of the cited prior art is further supported by the Declaration of Carrie Gardner (Ex. 1004), which further includes cites to Declaration of Gordon MacPherson (Ex. 1011).

A List of Exhibits is included pursuant to 37 C.F.R. §42.63(e).

F. Payment of Fees: 37 C.F.R. §§42.103, 42.15(a)

The required fee was submitted. The Office is authorized to charge any fee deficiency, or credit overpayment, to Deposit Account 50-1408, including additional fees related to this Petition.

III. PERSON OF ORDINARY SKILL IN THE ART ("POSITA")

A POSITA, on February 21, 2019, would have a Bachelor's degree in Computer Engineering, Electrical Engineering, or equivalent discipline, and at least three years of academic or industry experience relating to clocking techniques for FPGAs with high-speed transceivers. Educational requirements may be substituted by work experience, and vice versa.

IV. STATE OF THE ART

By February 21, 2019, FPGA-based communication systems were highly developed, and components such as SERDESes, PLLs, DLLs, CDRs, and phase-alignment mechanisms were standard FPGA features. Ex. 1001, 1:41–43; Ex. 1003, ¶86. Commercial user guides, such as Virtex-5 RocketIO GTP Transceiver User Guide ("Virtex-UG"), document many of these features. Ex. 1003, ¶86.

Commercial FPGA transceivers already implemented integrated serialization and deserialization using parallel-in/serial-out (PISO) and serial-in/parallel-out (SIPO) circuitry. Ex. 1009, 104; Ex. 1003, ¶89. The transceivers interfaced directly

with FPGA programmable logic through user-accessible clock and data interfaces, enabling custom processing of deserialized data. Ex. 1005, 194–95; Ex. 1003, ¶89. This includes built-in clock management and phase-alignment features. For example, Xilinx transceivers were capable of receiver clock phase alignment. Referring to Figure 7-22 of Virtex-UG, due to phase alignment, "SIPO parallel clock phase matches RXUSRCLK phase" and there is "[n]o phase difference between XCLK and RXUSRCLK." Ex. 1009, 179–180 ("Using RX Phase Alignment to Bypass the RX Elastic Buffer"); Ex. 1003, ¶95. With no phase difference, the RX Elastic Buffer (which is a clock domain crossing circuit enabling transition between XCLK and RXUSRCLK domains) is bypassed, removing latency caused by such buffers and FIFOs. *Id*.

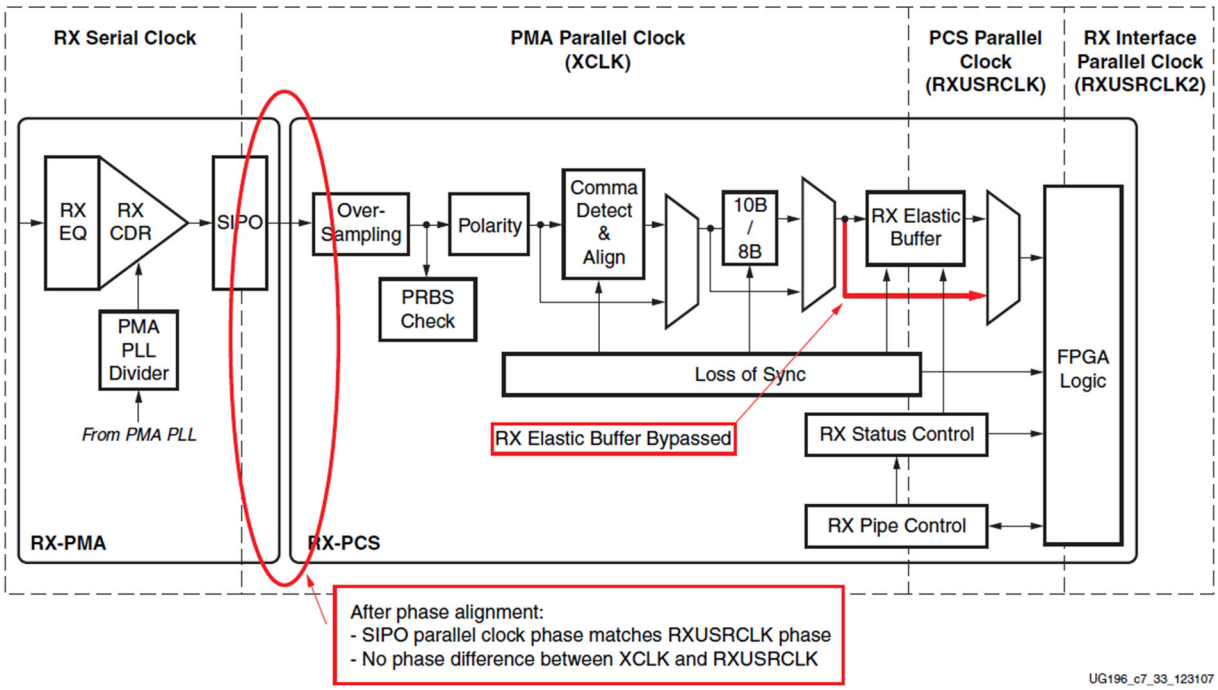


Figure 7-22: **Using Phase Alignment**

As discussed below, the prior art also recognized the need to synchronize recovered receiver clocks with transmitter clocks in high-speed serial links.

1. Giordano

Giordano, a 2011 IEEE paper, explains timing synchronization and clock-distribution applications "would benefit from high-speed fixed-latency SerDeses." Ex. 1005, 194.

Giordano presents "a link architecture" using "GTP transceiver" of the "Xilinx Virtex 5 FPGA family." Ex. 1005, 194. Giordano explains that transceivers are implemented as "configurable hard-macros (or 'tiles')," with each tile including a receiver and a transmitter. *Id*. Each receiver and transmitter has a Physical Medium Attachment (PMA) sublayer for serialization (in transmitter PMA) or deserialization (in receiver PMA), and a Physical Coding Sublayer (PCS) for processing data. *Id*.

Giordano also describes an FPGA Fabric with programmable hardware, which can implement user-programmed circuits such as "Comma Detect and Align" circuits and DLLs. *Id*., 197–199. Figure 1 below shows Giordano's architecture:

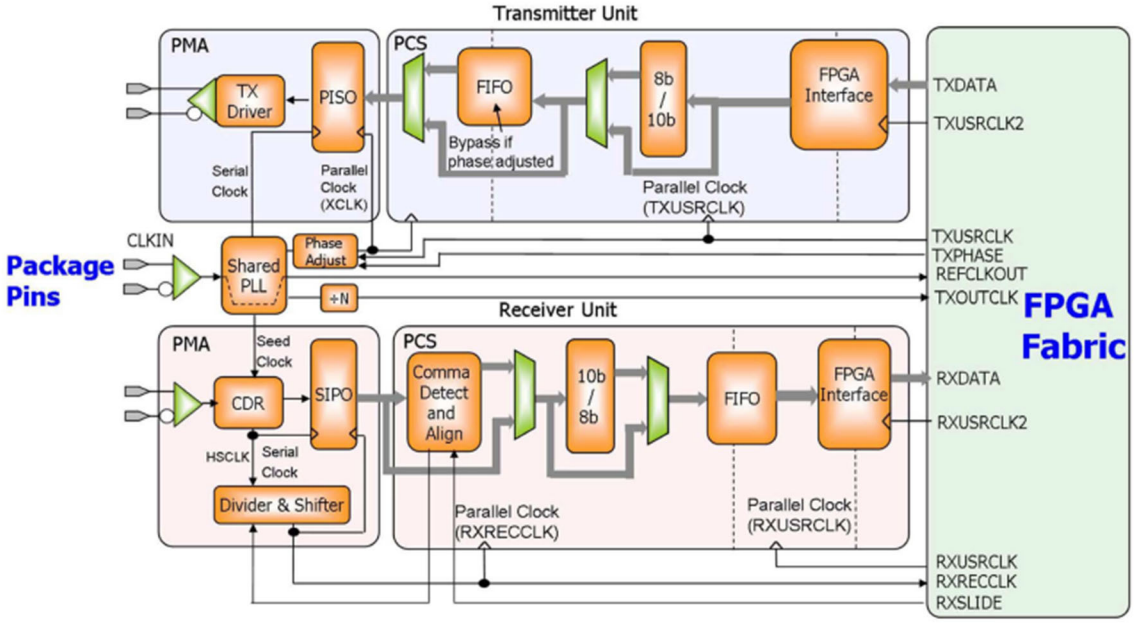


Fig. 1. Simplified block diagram of the GTP transceiver. Half a tile is shown.

Giordano repeatedly references the RocketIO GTP Transceiver, for example referencing the overall transceiver architecture (*id*., 195) and taking estimated latencies values from the RocketIO GTP Transceiver User Guide (*id*., 198). Giordano further provides that "the procedure we follow for activating the alignment circuit is the one suggested in the GTP user's guide." *Id*., 197. As such, Giordano inherently discloses the features of Virtex-UG (Ex. 1009), and further incorporates it by reference.

2. Virtex-UG

Virtex-UG is Xilinx's Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), dated December 3, 2009, hence it was publicly available before Giordano. Ex. 1009, 1; Ex. 1004, ¶¶41–47. Virtex-UG states that it "shows how to use the RocketIO™ GTP transceivers in Virtex®-5 FPGAs," and describes

the GTP transceiver as a power-efficient, highly configurable transceiver "tightly integrated with the programmable logic resources of the FPGA." Ex. 1009, 17, 23. The GTP transceiver supports line rates from 100 Mb/s to 3.75 Gb/s, optional PCS features such as 8b/10b encoding, comma alignment, channel bonding, and clock correction, and "fixed latency modes for minimized, deterministic datapath latency." *Id*., 23. The guide also explains that GTP transceivers are placed as dual-transceiver GTP_DUAL tiles in Virtex-5 LXT and SXT devices, allowing two transceivers to share a single PLL with the TX and RX functions of both, which is just how Giordano describes its use of the Virtex 5 FPGA. *Id*., 24; Ex. 1005, 194.

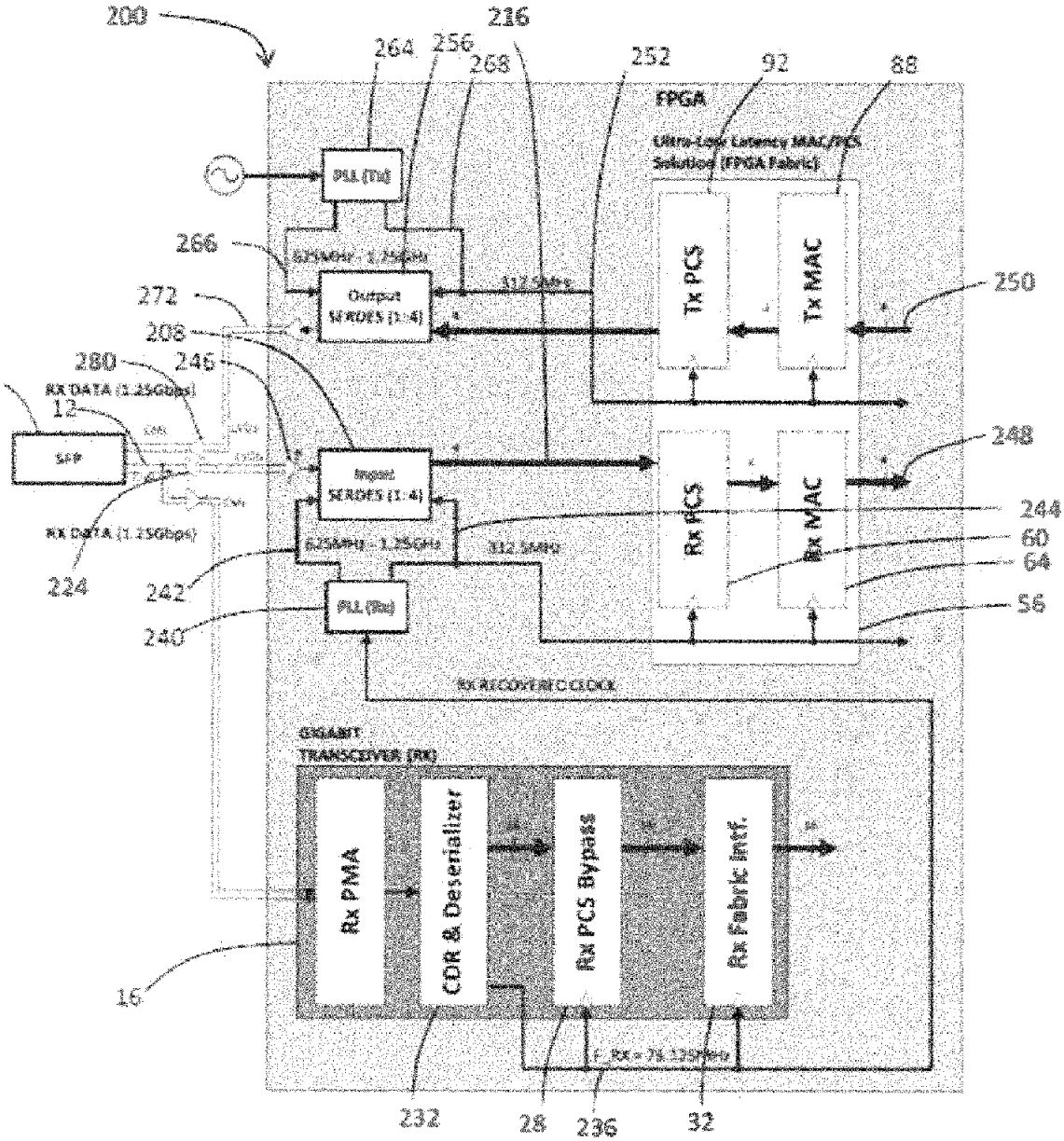
3. Kaviani

Kaviani (U.S. Pat. No. 7,453,301) explains that "DLLs in the Virtex or Spartan Field Programmable Gate Array (FPGA) product series from Xilinx" are clock-management systems used for "deskewing and phase shifting." Ex. 1010, 1:44–49. Kaviani explains that integrated circuits "such as a programmable logic device (PLD)" receive "external reference clock signals" to generate "internal clock signals," which "must be carefully controlled to ensure proper timing," and that it is "important" for generated clock signals to be "maintained accurately at the specified phase and frequency." *Id*., 1:13–17, 1:34–38. Kaviani further discloses a control circuit that "generate[s] delay select values," and provides "synchronization of the digital delay lines to avoid delay select set up and hold times." *Id*., 4:8–4:11.

4. Raymond

Raymond (U.S. Pat. No. 10,447,463) explains that "[u]ltra-low latency communication is critical" for applications such as electronic trading and that trading firms use FPGAs to improve throughput and latency. Ex. 1007, 1:18–24. Raymond discusses processing incoming financial trading data, exchanged with financial exchanges. *Id*., 4:52–59.

Raymond states that "prefabricated transceivers used to process incoming and outgoing physical layer signals" may be "replaced by low-latency serializer/de-serializer modules" programmed by the FPGA. *Id*., 4:43–47; 9:3–8 ("SerDes module" is "implemented using programmable logic"), 11:65–67. Raymond's proposed solution is depicted in Figure 2:



V. OVERVIEW OF THE ’865 PATENT

A. Summary of the File History of the ’865 patent

The application for the ’865 patent was filed May 29, 2020. During prosecution, the Examiner did not issue an Office Action rejecting the claims. Instead, during a July 7, 2020 examiner-initiated interview, the Examiner identified

potential provisional non-statutory double-patenting issues involving parent Application No. 16/670,702 and co-pending Application No. 16/672,076, and Applicant indicated that a terminal disclaimer would be filed. Ex. 1002, 15. After a terminal disclaimer, the Examiner then allowed the pending claims. Ex. 1002, 11–13.

VI. DETAILED CHALLENGE

A. Ground 1: Claims 1–18, 21 Are Rendered Obvious by Giordano in View of Kaviani

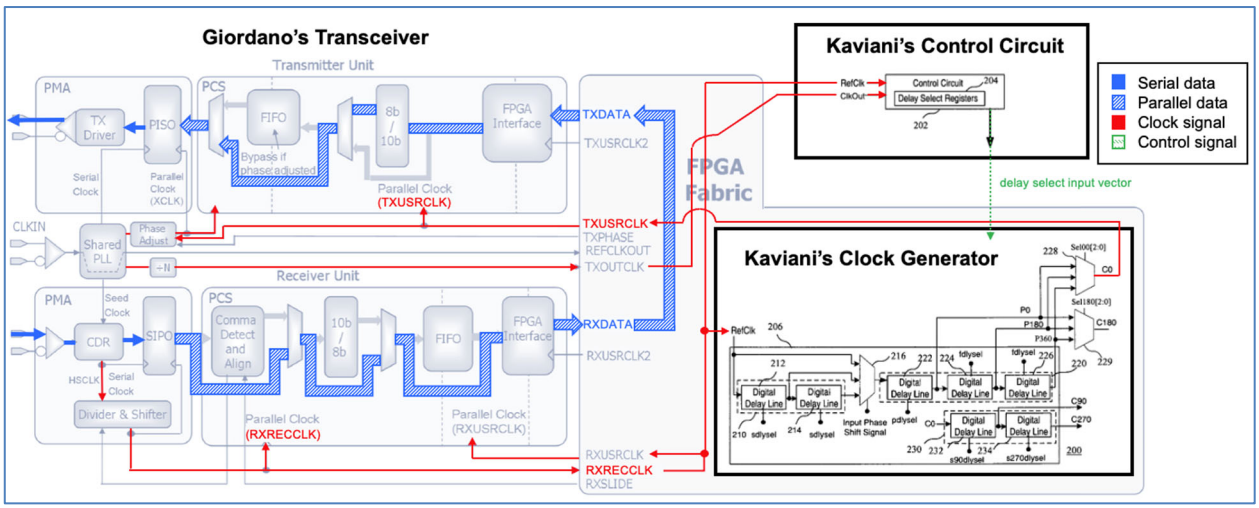
1. Prior Art Overview

Giordano's FPGA comprises two portions—a Xilinx Virtex-5 "RocketIO" GTP transceiver (with separate receiver and transmitter sides) and an FPGA Fabric. Ex. 1005, 195. The GTP transceiver comprises preprogrammed, fixed (but configurable with operating parameters and settings by user) hardware commonly referred to as hard-macro tiles. *Id*., 4; Ex. 1003, ¶104. In contrast, FPGA Fabric comprises user-modifiable, programmable hardware. *Id*. Giordano also discloses using FPGA circuit boards and configuring circuit boards for specific applications / experiments. Ex. 1005, Fig. 6; Ex. 1003, ¶104.

The proposed combination uses Giordano's Xilinx Virtex-5 GTP transceiver, FPGA Fabric, and FPGA circuit board, where the FPGA Fabric is programmed to implement Kaviani's Clock Generator and circuit board is modified to include Kaviani's control circuit. Kaviani, a Xilinx patent, expressly discusses Xilinx Virtex

FPGAs. Ex. 1010, 1:44–49. Given the shared Xilinx FPGA architecture, a POSITA would have understood how to implement Kaviani's clock-alignment circuitry in Giordano's FPGA Fabric and related circuit boards. Ex. 1003, ¶106.

The annotated image below, based on Figure 1 of Giordano and Figure 2 of Kaviani with modifications, depicts this proposed combination:



Giordano's GTP transceiver generates a receiver side-clock signal, RXRECCLK, from a clock extracted from incoming serial data. Ex. 1003, ¶108. RXRECCLK is provided to Kaviani's Clock Generator on the FPGA Fabric, which creates a transmitter-side clock signal TXUSRCLK. TXUSRCLK then goes to the transmitter PMA and related PLLs, resulting in TXOUTCLK. Kaviani's Control Circuit, implemented on the circuit board and off the FPGA, receives both RXRECCLK and TXOUTCLK to generate control signals and information to phase-match the two clock signals. *Id*. TXUSRCLK, which is phase-matched to RXRECCLK, is sent to the transmitter. *Id*.

a. Motivation to Combine Giordano and Kaviani

A POSITA would have been motivated to combine Giordano and Kaviani because they address synchronization and phase alignment of clock signals in FPGA transceivers. Ex. 1003, ¶110. Giordano seeks fixed-latency timing synchronization and clock distribution in Xilinx Virtex-5 GTP transceivers, while Kaviani is a Xilinx patent concerning "phase shifting of a generated clock signal." Ex. 1005, 194; Ex. 1010, Abstract.

Giordano identifies the need that Kaviani's phase alignment teachings fulfill. While Giordano's fixed latency architecture achieves deterministic (*i.e.*, fixed) phase relationships between the receiver clock and transmit clock, Giordano identifies gaps for directly using this receiver clock for the transmitter. Ex. 1005, 198; Ex. 1003, ¶111. Giordano states:

> *The clock recovered by the receiver cannot be directly used as a reference clock for the re-transmission. In fact, the internal PLL is shared among the transmitters and receivers in the same tile and at the receiver tile it is already locked to the seed clock. Moreover, the recovered clock might also require to be filtered in order to match the jitter specifications for the GTP reference clock*

Ex. 1005, 198. Giordano thus recognizes that jitter-filtering is beneficial to condition the recovered receiver clock to serve as a transmitter reference clock. Kaviani provides precisely such a solution through a phase shifting circuit that filters jitter and generates a transmit clock "phase aligned and frequency aligned with the reference clock signal." Ex. 1010, 1:36–43.

A POSITA reading Giordano would have naturally consulted Xilinx's own materials (such as Kaviani, a Xilinx patent), for a DLL-based phase alignment solution. Giordano uses a Xilinx Virtex FPGA, a chip that Kaviani mentions as well. Ex. 1005, 194, 197–199; Ex. 1010, 1:44–49.

Incorporating Kaviani's phase shifting teachings into Giordano would require routine programming of FPGA Fabric logic and conventional circuit element modifications. Ex. 1003, ¶114.

Giordano itself demonstrates programming custom hardware in the FPGA Fabric, and further using elements on the circuit board as needed. For example, Giordano implemented a custom Comma Detector and Aligner in the FPGA Fabric because the GTP's built-in comma detector (which is a fixed block inside the transceiver) did not support the particular operations the user needed. Ex. 1005, 198; Ex. 1003, ¶115. Giordano also discloses implementing DLL blocks "external to the GTP" transceiver, *i.e.*, on the FPGA Fabric. Ex. 1005, Fig. 5; Ex. 1003, ¶115. This DLL receives the REFCLKOUT from the receiver, and generates a phase-matched transmitter clock TXUSRCLK. Ex. 1005, 197; Ex. 1003, ¶115. Similarly, Giordano discusses configuring the circuit boards for experimental setups. Ex. 1005, 198; Ex. 1003, ¶115. Kaviani describes its Clock Generator (which includes multiple decoders) and Control Circuit as separate circuits, supporting that these are implementable in different physical regions. Ex. 1010, Fig. 2; Ex. 1003, ¶115.

Implementing Kaviani's Clock Generator in the FPGA Fabric and Control Circuit in the circuit board thus represents a straightforward extension of techniques already used in Giordano. Ex. 1003, ¶115.

Such FPGA hardware programming is how the '865 patent suggests implementing its claimed invention. In the '865 patent, phase detector, phase controller, delay locked loop (DLL) components, and phase locked loop (PLL) are implemented in a "FPGA Core." Ex. 1001, Figs. 3A–F, 4A–C, 5A–F. This FPGA Core includes logic elements, DSP blocks, clock distribution components, and memories, mirroring Giordano's FPGA Fabric. Ex. 1001, 26:35–53; Ex. 1003, ¶116. Thus, implementing Kaviani's teachings in Giordano's FPGA mirrors the '865 patent's own approach. Ex. 1003, ¶116.

A POSITA would have had a reasonable expectation of success. Giordano's FPGA implementation was physically tested on Xilinx evaluation boards and used circuit blocks similar to those disclosed in Kaviani, including PLLs, DLLs, serializers, and pattern generators. Ex. 1005, 197–200. Giordano acknowledges the elements used for phase matching (such as DLL) are implemented on the FPGA Fabric, circuitry that can be programmed for whatever function the user desires. Ex. 1005, 195, 197; Ex. 1003, ¶117. Because both references rely on the same Xilinx FPGA infrastructure, there would have been high expectation that, through routine FPGA programming, the combination functions as intended. Ex. 1003, ¶117.

b. Features of Virtex-UG are Inherent to Giordano, and Giordano Incorporates Virtex-UG by Reference

Giordano presents a system with the "RocketIO" GTP transceiver of the Xilinx Virtex 5 FPGA family. Ex. 1005, 194, 199. Giordano repeatedly references the RocketIO GTP Transceiver, for example referencing the overall transceiver architecture (*id*., 195) and taking estimated latency values from the RocketIO GTP Transceiver User Guide (*id*., 198). Giordano further describes phase alignment of clock signals, and that "the procedure we follow for activating the alignment circuit is the one suggested in the GTP user's guide." *Id*., 197. A POSITA would have known to reference Xilinx documents on the GTP transceiver to understand the relevant inherent features. Ex. 1003, ¶118. As such, Giordano inherently discloses the features of Virtex-UG. *Id*.

In such a case, the features of the Virtex-UG are necessarily present in Giordano, and it is proper to use extrinsic evidence (such as the Virtex-UG) to understand said features. *See Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1328 (Fed. Cir. 2001) ("[R]ecourse to extrinsic evidence is proper to determine whether a feature, while not explicitly discussed, is necessarily present in a reference. The evidence must make clear that the missing feature is necessarily present, and that it would be so recognized by persons of ordinary skill in the relevant art."); *Sage Prods., LLC v. Stewart*, 133 F.4th 1376, 1385 (Fed. Cir. 2025) ("There was likewise nothing improper in the Board relying on evidence outside of the PAR

to make findings as to what the skilled artisan would understand the PAR to be disclosing."); *Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1345 (Fed. Cir. 2018) ("It is well established that such reliance on extrinsic evidence is proper in an inherency analysis."); *see also In re Haines*, No. 2024-2338, 2025 WL 1403578, at *2 (Fed. Cir. May 15, 2025) (examiner properly used another publication "as evidence to explain why [the prior art's] disclosure of a mass spectrometer implicitly discloses 'obtaining mass spectral channel signals (m/z)'" (cleaned up)).

For the same reasons as above, Giordano incorporates Virtex-UG (Ex. 1009) by reference. Ex. 1005, 197 ("the procedure we follow for activating the alignment circuit is the one suggested in the GTP user's guide."). Virtex-UG, by incorporation, becomes part of the disclosures of Giordano. *Verizon Connect Inc. v. Omega Patents, LLC*, IPR2023-01162, 2024 WL 714951, at *3, 14-15 (P.T.A.B. Feb. 21, 2024) (the incorporated secondary reference's disclosures become part of the primary reference); *Paice LLC v. Ford Motor Co.*, 881 F.3d 894, 906-07 (Fed. Cir. 2018) ("[T]he standard of one reasonably skilled in the art should be used to determine whether the host document describes the material to be incorporated by reference with sufficient particularity.") (citing *Advanced Display Systems, Inc. v. Kent State University*, 212 F.3d 1272 (2000)).

2. Analysis

a. Independent Claim 1

[1.pre]: "A method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of:"

This preamble, at least with respect to "market data" and "entry data," is not limiting. Ex. 1003, ¶120.

A preamble is limiting "if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (citation omitted). "Conversely, a preamble is not limiting 'where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.'" *Id.*; *see also Shoes by Firebug LLC v. Stride Rite Children's Grp., LLC*, 962 F.3d 1362, 1367 (Fed. Cir. 2020).

Here, the terms "market data" and "entry data" are nothing more than recited purpose and use of the claimed invention. Indeed, they are not recited in other limitations in claim 1, supporting that "market data" and "entry data" are not "essential" to the steps of this claim.

Where the terms "market data" and "entry data" do appear again further supports that the preamble of claim 1 is not limiting. "By definition, an independent claim is ***broader*** than a claim that depends from it." *Littelfuse, Inc. v. Mersen USA*

EP Corp., 29 F.4th 1376, 1379–82 (Fed. Cir. 2022); *see also* 35 U.S.C. §112(d) ("[A] claim in dependent form shall contain a reference to a claim previously set forth and then specify ***a further limitation*** of the subject matter claimed.").

If the preamble is limiting, the limitations of claims 19 and 20 are rendered superfluous, and fail to narrow claim 1. Claims 19 and 20 recite:

> *19. The method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.*
>
> *20. The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.*

Claims 19 and 20 add to claim 1 that the limitation for the "first serial data stream" comprises market data, and claim 19 also adds that the "second serial data stream" comprises order entry data. These are the same terms recited in the preamble of claim 1, hence they are rendered superfluous should that preamble be limiting.

Otherwise, Giordano discloses Xilinx Virtex-5 FPGA that includes "serializer-deserializer (SerDes)." Ex. 1005, 194. Giordano discloses a receiver taking in serial data, and a transmitter sending out processed serial data. Ex. 1003, ¶122.

[1.a]: "(a) receiving, by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream;"

Giordano discloses this limitation. Ex. 1003, ¶123.

Giordano discloses the GTP transceiver, which includes separate "Receiver Unit" and "Transmitter Unit." Ex. 1005, 194. Within each receiver- and transmitter-unit are a Physical Medium Attachment ("PMA") and Physical Coding Sublayer ("PCS"). *Id*., 194–195. Giordano points to the PMA sublayer as the component "actually serializing and de-serializing the data," and the PCS layer as "processing" data. *Id*., 194.

Giordano discloses package pins that interface the Receiver Unit PMA with external components, which disclose the claimed "first plurality of data pins" and "first interface." Ex. 1005, Fig. 1; Ex. 1003, ¶125. This Receiver Unit PMA receives incoming serial data, which discloses the "first serial data stream." Ex. 1005, 195; Ex. 1003, ¶125.

This mirrors the '865 patent, which describes a deserializer with a receiver PMA. Ex. 1001, 53:16–19, Fig. 6E.

[1.b]: "(b) receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase;"

Giordano discloses this limitation. Ex. 1003, ¶127. As discussed in element [1.a], Giordano's Receiver Unit package pins disclose the claimed "first plurality of data pins" and "first interface."

Giordano's Receiver Unit PMA has a Clock and Data Recovery ("CDR") block, "which extracts a clock (HSCLK)" from the incoming serial data stream. Ex. 1005, 195. HSCLK discloses the "first clock signal," and also "first frequency and

first phase." Ex. 1003, ¶128. The package pin that receives this incoming serial data clock signal discloses "first reference clock pin."

This mirrors the '865 patent, which describes a receiver PMA further comprising a CDR block. Ex. 1001, 53:16–19, Fig. 6E. Like Giordano, the CDR block of the '865 patent receives serial data, and extracts a clock signal from the incoming serial data. Ex. 1001, 53:22–32.

[1.c]: "(c) transmitting, from the first plurality of data pins of the first interface to a deserializer in the field programmable gate array, the first serial data stream;"

Giordano discloses this limitation. Ex. 1003, ¶130.

Giordano's Receiver Unit PMA discloses the claimed "deserializer."

The Receiver Unit PMA includes a "Serial In to Parallel Output (SIPO)" block, which deserializes incoming serial data. Ex. 1005, 195–196; Ex. 1003, ¶132. The package pins transmit the incoming serial data to the Receiver Unit PMA. Ex. 1005, 195; Ex. 1003, ¶132.

This mirrors the '865 patent, which describes a receiver PMA that receives serial data. Ex. 1001, 53:15–32, Fig. 6E.

[1.d]: "(d) transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal;"

Giordano discloses this limitation. Ex. 1003, ¶134. As discussed in element [1.b], HSCLK discloses the claimed "first clock signal."

Giordano's Receiver Unit PMA has a Clock and Data Recovery ("CDR") block, "which extracts a clock (HSCLK)" from the incoming serial data stream. Ex. 1005, 195. As such, HSCLK is sent with the serial data from the package pins to this CDR. *Id*.; Ex. 1003, ¶135.

This mirrors the '865 patent, which describes a deserializer with a receiver PMA. Ex. 1001, 53:16–19, Fig. 6E. This receiver PMA further comprises a CDR block. *Id*. Like Giordano, the CDR block of the '865 patent receives serial data, and extracts a clock signal from the incoming serial data. Ex. 1001, 53:22–32.

[1.e]: "(e) generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal;"

Giordano discloses this limitation. Ex. 1003, ¶137. As discussed in element [1.c], Giordano's Receiver Unit PMA discloses the claimed "deserializer."

Giordano's parallel recovered clock (RXRECCLK) discloses the "receiver side clock signal." Ex. 1003, ¶138. RXRECCLK discloses the "second frequency" and "second phase." Ex. 1003, ¶138.

The CDR in Giordano's Receiver Unit PMA extracts a clock (HSCLK) signal from the incoming serial data. Ex. 1005, 195. HSCLK is then used to "generate a parallel recovered clock (RXRECCLK)" for the SIPO block and Receiver Unit PCS. *Id*.; Ex. 1003, ¶139. This RXRECCLK discloses the claimed "receiver side clock

signal," and the frequency and phase of RXRECCLK disclose the claimed second frequency and phase. Ex. 1003, ¶139.

This mirrors the '865 patent, which describes a CDR that receives serial data, and generates clock signals for blocks such as Serial to Parallel and receiver PCS. Ex. 1001, 53:22–32, Fig. 6E.

[1.f]: "(f) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;"

Giordano discloses this limitation. Ex. 1003, ¶141. As discussed in elements [1.a] and [1.c], Giordano's Receiver Unit PMA discloses the claimed "deserializer," and the serial data into the PMA discloses the "first serial data stream."

Giordano's SIPO block output discloses the "first plurality of parallel data streams." Ex. 1003, ¶142.

Giordano's Receiver Unit PMA has a SIPO block that converts incoming serial data to parallel data, which discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶143.

This mirrors the '865 patent, which describes a Serial to Parallel block within the Receiver PMA that "converts the serial data into parallel data, transmitting the parallel data to the receiver PCS." Ex. 1001, 53:28–32, Fig. 6E.

[1.g]: "(g) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal;"

Giordano discloses this limitation. Ex. 1003, ¶145. As discussed in elements [1.c] and [1.e], Giordano's Receiver Unit PMA discloses the claimed "deserializer," and its recovered clock signal RXRECCLK discloses "receiver side clock signal."

Giordano's Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS individually and collectively disclose the "computational circuitry in the [FPGA]." Ex. 1003, ¶146.

Giordano points to PCS (both receiver and transmitter sides) as "processing" data, disclosing computational circuitry. Ex. 1005, 194; Ex. 1003, ¶147. Giordano describes that FPGA Fabric includes "logic," which discloses the claimed "computational circuitry in the [FPGA]." Ex. 1005, 195–196; Ex. 1003, ¶147. Giordano discloses providing RXRECCLK (*i.e.*, "receiver side clock signal") to the Receiver Unit PCS and FPGA Fabric. Ex. 1005, 195; Ex. 1003, ¶147.

This mirrors the '865 patent, with figures depicting computational circuitry capable of performing logical operation as "Computation Logic." Ex. 1001, Figs. 4B–C, 5A–F, cl. 5.

[1.h]: "(h) transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams;"

Giordano discloses this limitation. Ex. 1003, ¶149. As discussed in elements [1.c], [1.f], and [1.g], Giordano's Receiver Unit PMA discloses the claimed

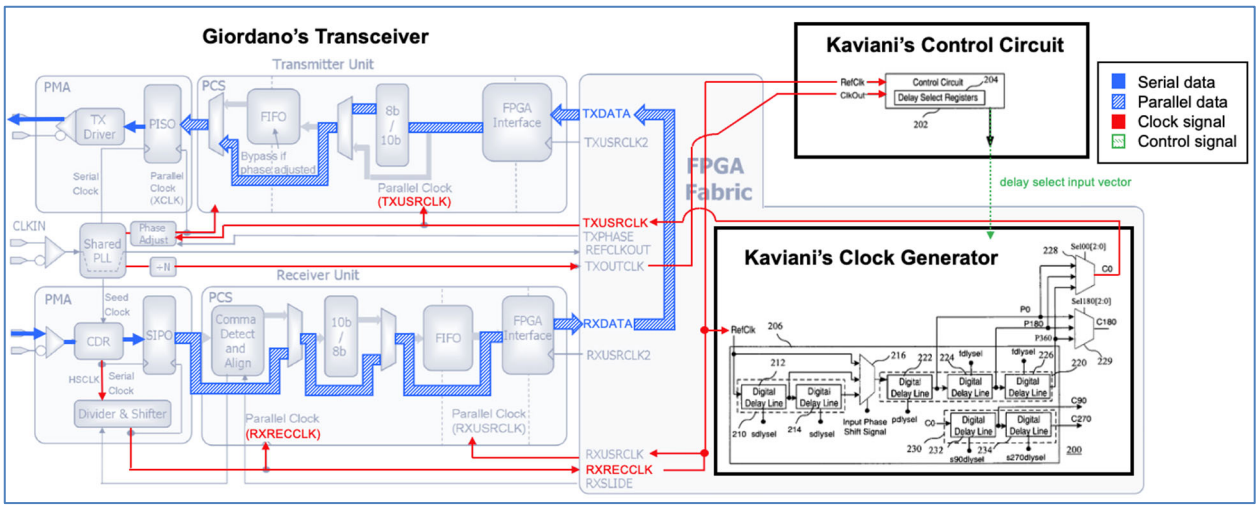
"deserializer," SIPO block output discloses the "first plurality of parallel data streams," and Giordano's Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS together disclose the "computational circuitry in the [FPGA]."

Giordano's SIPO block output, further processed by the Receiver Unit PCS, discloses the "first plurality of parallel data streams" (where the bit size of said parallel data discloses "first amount of data streams" and data transferred using this format discloses "first plurality of data items"). Ex. 1005, 195, Fig. 1; Ex. 1003, ¶150.

[1.i]: "(i) transmitting, from the deserializer via a first clock output pin on a second interface of the field programmable gate array to a phase detector that is part of the field programmable gate array system and not part of the field programmable gate array, the first receiver side clock signal;"

Giordano in view of Kaviani renders obvious this limitation. Ex. 1003, ¶151. As discussed in elements [1.c] and [1.e], Giordano's Receiver Unit PMA discloses the claimed "deserializer," and its recovered clock signal RXRECCLK discloses "receiver side clock signal."

Kaviani's Control Circuit discloses this limitation. The connection between the FPGA and said Control Circuit discloses the claimed "second interface," and the connection specific for Kaviani's RefClk input to the Control Circuit discloses the "first clock output pin." Ex. 1003, ¶152. Kaviani's Control Circuit 202, which is a separate circuit from the FPGA, discloses the claimed "phase detector." Ex. 1003, ¶152. The combination is depicted below:



Giordano discloses providing RXRECCLK (*i.e.*, "receiver side clock signal") to the off-FPGA Control Circuit. Ex. 1005, 195; Ex. 1010, Fig. 2; Ex. 1003, ¶153.

Kaviani discloses Control Circuit 202 and Clock Generator Circuit 206 as separate circuits, implementable in different physical regions. Ex. 1010, Fig. 2; Ex. 1003, ¶154. As such, in light of Giordano's teachings, a POSITA would have known to implement the Clock Generator on the FPGA Fabric, and the Control Circuit off the FPGA chip but still on the circuit board (*e.g.*, FPGA system). Section VI.A.1; Ex. 1003, ¶154.

[1.j]: "(j) generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level:"

Giordano in view of Kaviani renders obvious this limitation. Ex. 1003, ¶155. As discussed in element [1.i], Kaviani's Control Circuit discloses the claimed "phase detector."

The output of the combined clock generator results in a "first transmitter side clock signal" TXUSRCLK. Ex. 1003, ¶156. This TXUSRCLK discloses the "third frequency" and the "third phase." Ex. 1003, ¶156. Kaviani's Control Circuit output, that contains control signals for Kaviani's delay lines (sdlysel, pdlhysel, and fdlysel; or shift delay vectors) and MUXs (Input Phase Shift Signal and Sel00[2:0], or delay select input vectors), discloses the claimed "first output." Ex. 1010, Figs. 2, 5, 4:20–5:23, 9:46–10:3. Kaviani's phase in window concept discloses the claimed repetitive steps.

In the proposed combination, the FPGA Fabric creates a clock path from RXRECCLK (*i.e.*, "receiver side clock signal") to TXUSRCLK (*i.e.*, "transmitter side clock signal"), with Kaviani's Control Circuit 202 and Clock Generator Circuit 206 between the two clocks. Ex. 1010, 3:64–4:19; Ex. 1003, ¶157. The result is a transmitter-side clock phase matched to the receiver-side clock. Ex. 1005, 198; Ex. 1003, ¶157.

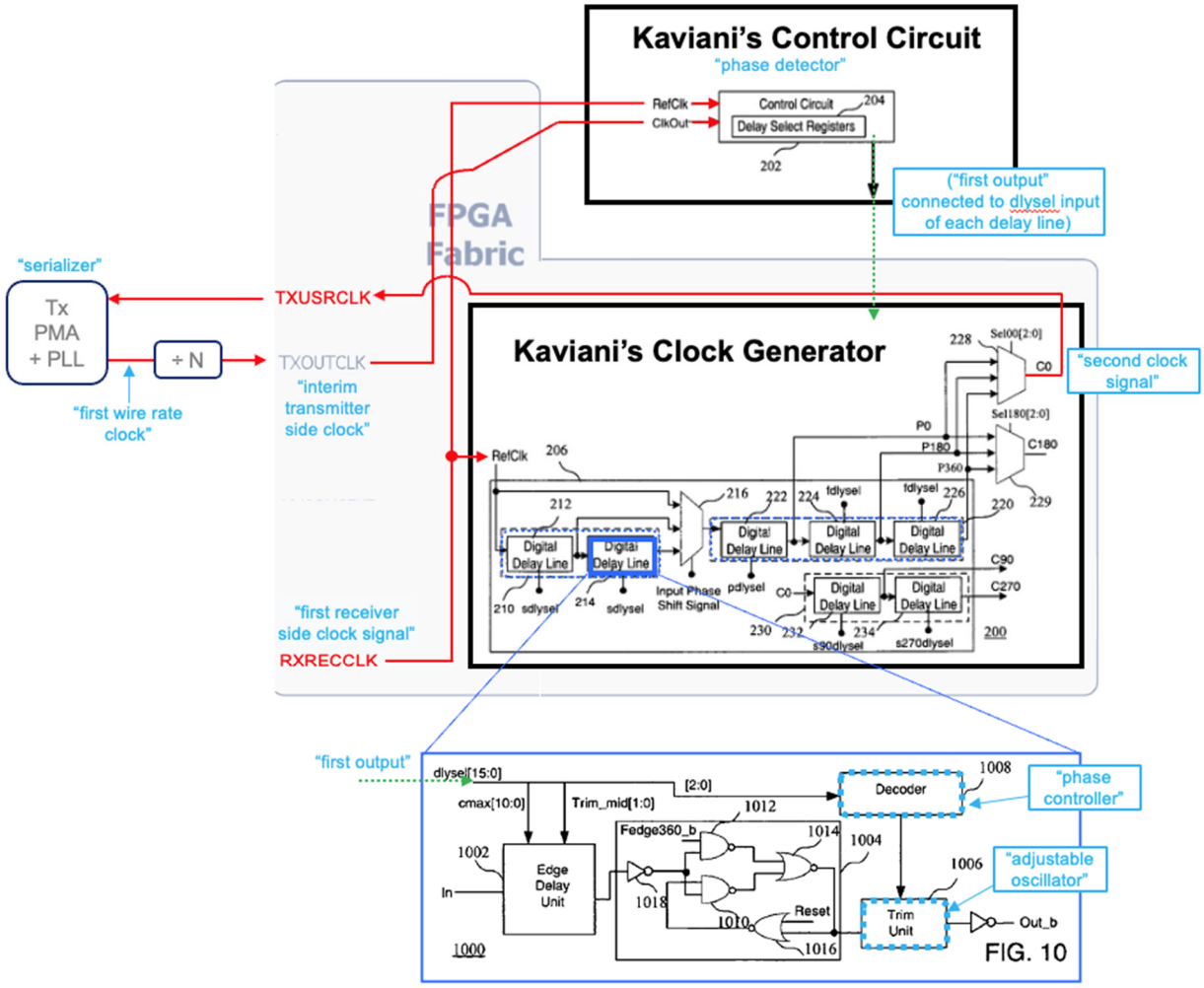
Kaviani discloses concepts of "frequency in window" and "phase in window." Ex. 1010, 6:22–54; Figs. 5–6. Phase in window is the time taken for the phase to match that of a target level, where such matching discloses "below a first threshold level." *Id.*; Ex. 1003, ¶158. Kaviani discloses a signal phase_inwindow that transitions to logic high once phase matching happens. Ex. 1010, Figs. 5–6; Ex. 1003, ¶158. Phase adjustments continue iteratively using the phase detected by the

Control Circuit 202, for example following the sequence disclosed in Kaviani Fig. 4. *Id*., 6:15–22 ("phase align signal P is increased until before a phase match is detected."); Ex. 1003, ¶158. This iterative process in Kaviani discloses the claimed repetitive steps of this limitation.

[1.k] steps (i) through (viii)

Giordano in view of Kaviani renders obvious the claimed steps. Ex. 1003, ¶159.

For ease of discussion, the claimed "steps" (i) through (viii) are discussed together, per the annotated image below based on Giordano Figure 1 and Kaviani's Figures 2 and 10:



"(i) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase;"

Kaviani's sets of delay lines (212, 214, 222, 224, 226) each have internal components that cause phase delays, for example, Trim Unit 1006, which disclose the claimed "adjustable oscillator." Ex. 1010, Figs. 2, 10; Ex. 1003, ¶161. The Clock Generator output (C0) discloses the "second clock signal" (including fourth frequency and phase). Ex. 1010, Fig. 2; Ex. 1003, ¶161.

Kaviani discloses using multiple digital delay lines to generate signals with different amounts of added phase delays, where each delay line is controlled by a shift delay vector (such as sdlysel). Ex. 1010, 4:25–40. Within each delay line are trim units that "provides a fine grain delay adjustment to the combined clock signal," which are controlled by decoders. *Id*., 9:46–10:28. These trim units disclose the claimed "adjustable oscillator." Ex. 1003, ¶162.

This mirrors the '865 patent, which acknowledges that "the adjustable oscillator [] may be implemented with a digital delay line." Ex. 1001, 38:62–64.

"(ii) generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal;"

Giordano's Shared PLL output, which goes through a divider (depicted with "÷ N") to become TXOUTCLK, discloses the "first wire rate clock signal" (including fifth frequency and phase). Ex. 1005, Fig. 1; Ex. 1003, ¶164.

Giordano's Shared PLL generates a signal, based on TXUSRCLK, that is provided to a divider. Ex. 1005, Fig. 1; Ex. 1003, ¶165. The output of this divider becomes TXOUTCLK. Ex. 1005, Fig. 1; Ex. 1003, ¶165.

This mirrors the '865 patent, which describes a divider for adjusting the frequency of a clock signal. Ex. 1001, 29:18–21, 51:63–52:8. Like Giordano, this divider outputs a "lower-frequency" signal, from dividing the input signal by a user-settable number. Ex. 1001, 52:31–41; Ex. 1003, ¶166.

"(iii) generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase;"

Giordano's Transmitter Unit PMA with the Shared PLL discloses the claimed "serializer," and TXOUTCLK discloses "interim transmitter side clock signal" (including sixth frequency and phase). Ex. 1003, ¶167.

Giordano discloses Shared PLL generating TXOUTCLK. Ex. 1005, 195 (Shared PLL "provides a parallel clock output (TXOUTCLK)").

"(iv) transmitting, from the serializer via a second clock output pin of the second interface to the phase detector, the interim transmitter side clock signal;"

As discussed in element [1.i], Kaviani's Control Circuit discloses the claimed "phase detector," and the connection between Giordano's FPGA and Kaviani's Control Circuit discloses the claimed "second interface."

Giordano discloses sending TXOUTCLK ("interim transmitter side clock signal") from Shared PLL to the FPGA Fabric. Ex. 1005, 195. In the proposed combination, FPGA Fabric sends TXOUTCLK to Kaviani's Control Circuit. Ex. 1010, Fig. 2; Ex. 1003, ¶170. This connection to Kaviani's Control Circuit discloses the "second clock output pin." Ex. 1003, ¶170.

"(v) generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal;"

As discussed in elements [1.e], [1.i], [1.j], and [1.k.iii], Giordano's RXRECCLK discloses the "receiver side clock signal," TXOUTCLK discloses the

"interim transmitter side clock signal," and Kaviani's Control Circuit discloses the claimed "phase detector" and its output "first output."

Kaviani's Control Circuit discloses this limitation. Ex. 1003, ¶172.

Kaviani discloses the Control Circuit 202 generating shift delay vectors (*e.g.*, sdlysel, pdlhysel, fdlysel) and delay select input vectors (*e.g.*, Input Phase Shift Signal, Sel00[2:0]). Ex. 1010, 3:64–4:28. The various functions of Control Circuit 202 are further described in Kaviani Figure 3:

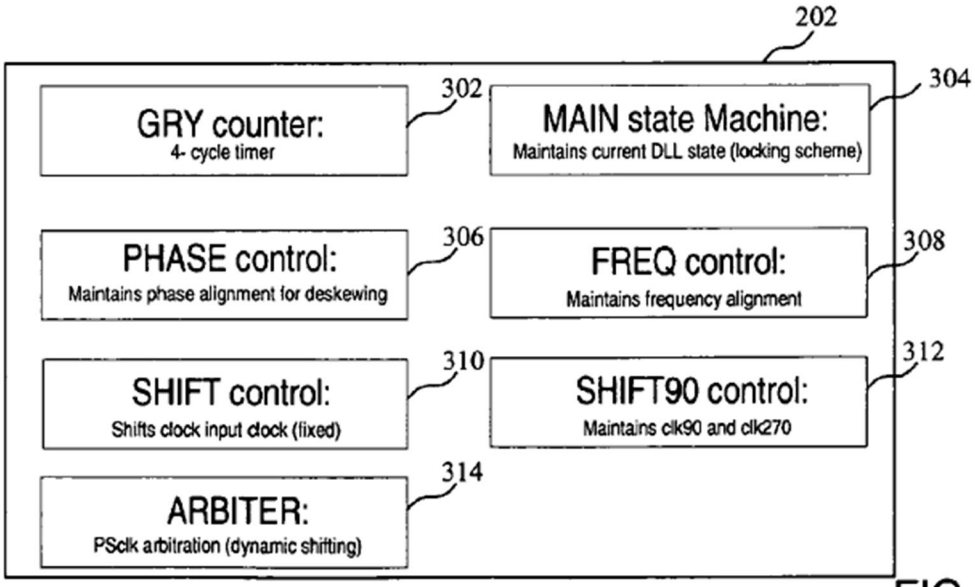


FIG. 3

Kaviani's PHASE control 306 generates signals "for maintaining phase alignment for deskewing," and FREQ control 308 "for maintaining frequency alignment." *Id.*, 5:37–51. Kaviani discloses generating such control signals based on comparison of the two incoming clock signals, which in the proposed combination are RXRECCLK

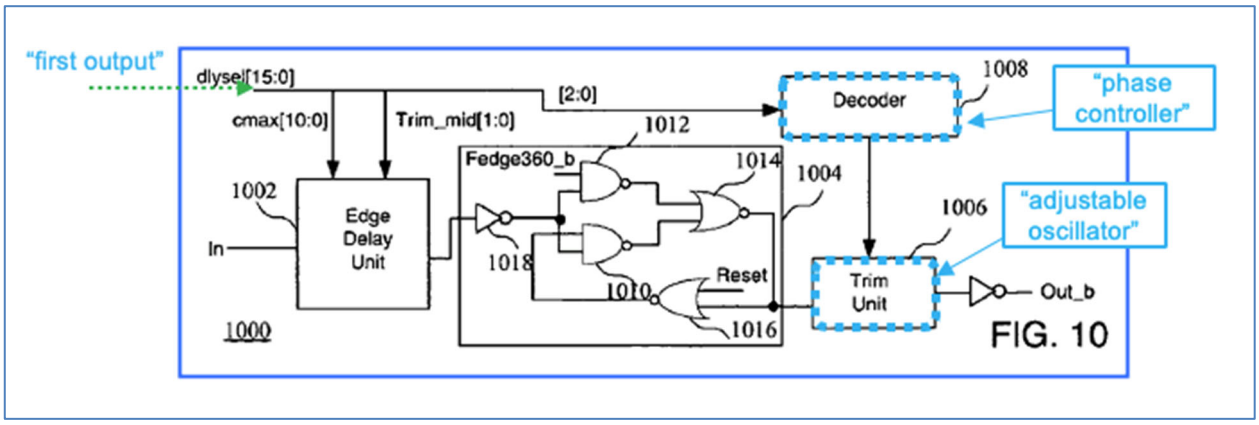
("receiver side clock signal") and TXOUTCLK ("interim transmitter side clock signal"). Ex. 1003, ¶174.

"(vi) transmitting, from the phase detector to a phase controller of the field programmable gate array system which is placed within the field programmable gate array, the first output;"

As discussed in elements [1.i] and [1.j], Kaviani's Control Circuit discloses the claimed "phase detector," and its output shift delay vectors disclose the "first output."

Kaviani discloses this limitation. Ex. 1003, ¶176.

The decoder in Kaviani's Digital Delay Line, which is implemented on Giordano's FPGA Fabric, discloses the claimed "phase controller." Annotated Kaviani Figure 10 illustrates this mapping:



Kaviani discloses Control Circuit 202 generating shift delay vectors (*e.g.*, sdlysel, pdlhysel, fdlysel), which are then provided to appropriate Digital Delay Lines. Ex. 1010, 3:64–4:28. Within the delay line, a decoder receives the incoming shift delay vector. Ex. 1003, ¶178.

"(vii) determining, by the phase controller, interim adjustment information based on the first output; and"

As discussed in element [1.k.vi], Kaviani's decoder discloses the claimed "phase controller."

This decoder receives incoming delay vectors and controls the trim unit for "fine grain delay adjustment." Ex. 1010, 9:46–10:3. The decoder's control signal to the trim unit discloses the claimed "interim adjustment information." Ex. 1003, ¶180.

"(viii) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information,

As discussed in elements [1.k.i] and [1.k.vi], Kaviani's trim discloses the claimed "adjustable oscillator" and the decoder discloses the "phase controller."

This decoder receives incoming delay vectors and controls the trim unit for "fine grain delay adjustment." Ex. 1010, 9:46–10:3. The decoder's control signal to the trim unit discloses the claimed "interim adjustment information." Ex. 1003, ¶182.

wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through (viii) are repeated until the first output of the phase detector is below the first threshold level;"

Giordano in view of Kaviani renders obvious this limitation. Ex. 1003, ¶183.

In the proposed combination, Kaviani's Control Circuit takes in RXRECCLK ("first receiver side clock signal") and TXOUTCLK ("interim transmitter side clock signal"). Based on the comparison of the two signals, Kaviani's Control Circuit

determines the "correct amount of shifting required by all the delay lines" so the Clock Generator output is phase-matched to the reference clock signal. Ex. 1010, 5:24–35. Kaviani refers to this determination as "locking process." *Id*. The Control Circuit also maintains the correct shifting after lock, maintaining the phase-matching between the two clock signals. *Id*., 5:35–37; Ex. 1003, ¶184.

Kaviani Figure 4 discloses this iterative process for "locking" the output clock to the reference clock:

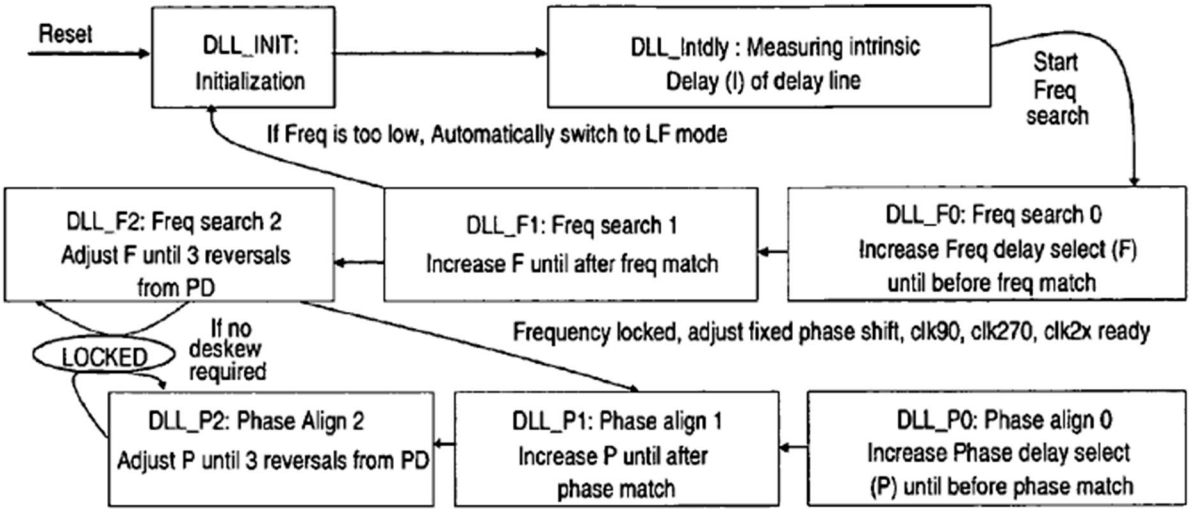


FIG. 4

[1.l]: "(k) transmitting, from the serializer to the computational circuitry, first transmitter side clock signal;"

Giordano discloses this limitation. Ex. 1003, ¶186. As discussed in elements [1.g], [1.j], and [1.k.iii], Giordano's Transmitter Unit PMA with the Shared PLL discloses the claimed "serializer," Receiver Unit PCS, FPGA Fabric, and

Transmitter Unit PCS together disclose the "computational circuitry," and TXUSRCLK discloses the "first transmitter side clock signal."

Giordano discloses the Shared PLL providing clock signals to the Transmitter Unit PCS, namely the XCLK signal. Ex. 1005, Fig. 1. Giordano discloses that "[i]n some configurations XCLK and TXUSRCLK have the same frequency and a constant phase offset," where for "sufficiently small" phase offset the two are treated the same, and clock domain crossing between XCLK and TXUSRCLK is bypassed. Ex. 1005, 195; Ex. 1003, ¶187. Giordano's providing of XCLK from the Shared PLL to the Transmitter Unit PCS, and disclosure of treating XCLK the same as TXUSRCLK, discloses this limitation. Ex. 1003, ¶187.

[1.m]: "(l) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams, wherein the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams;"[5]

Giordano discloses this limitation. Ex. 1003, ¶188. As discussed in elements [1.f] and [1.g], Giordano's SIPO block output discloses the "first plurality of parallel data streams" and PCSs / FPGA Fabric discloses the "computational circuitry."

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[5] The term "first set of parallel data streams" lacks antecedent basis. For the purpose of this IPR, Petitioner will correlate this term with the "first plurality of parallel data streams" discussed in element [1.f].

Giordano's processed parallel data exiting the Transmitter Unit PCS into the PMA discloses the "second plurality of parallel data streams" (where the bit size of said parallel data discloses "second amount of data streams"). Ex. 1005, Fig. 1; Ex. 1003, ¶189.

As to "first set of operations," Giordano describes an FPGA Fabric that includes "logic," which discloses this limitation. Ex. 1005, 195–196, 198; Ex. 1003, ¶190. Giordano describes programming a Comma Detector and Aligner in the FPGA Fabric, which performs "comma detection." Ex. 1005, 198; Ex. 1003, ¶190. Giordano's "comma detector looks for commas (*e.g.*, the one included in the K28.5 symbol) and when it finds one it determines how many bit shifts" are "required in order to align the parallel data." Ex. 1005, 198; Ex. 1003, ¶190. A POSITA would have understood this pattern matching operation (to locate comma characters) and computing number of bit shifts for alignment to disclose the claimed "first set of operations." Ex. 1003, ¶190.

In addition, Giordano points to the PCS layer (both receiver and transmitter sides) as "processing" data, rendering obvious computational circuitry. Ex. 1005, 194; Ex. 1003, ¶191. The PCS layer includes 8b/10b encoding / decoding functions, which require arithmetic calculations, hence rendering obvious "first set of operations." Ex. 1005, 197; Ex. 1003, ¶191.

<u>As to "not include clock domain crossing operations,"</u> Giordano discloses this limitation. Ex. 1003, ¶192.

Giordano discloses bypassing the First In First Out (FIFO) buffer, a circuit block allowing safe data transfer between different clock domains (*e.g.*, "data transfers between TXUSRCLK domain and the XCLK domain"). Ex. 1005, 195; Ex. 1003, ¶193. A POSITA would have understood FIFO as a clock domain crossing circuit, and Giordano's bypassing of the FIFO block discloses this limitation. Ex. 1003, ¶193.

Giordano discloses bypassing the FIFO buffer by having the two clock domains have "the same phase" and "therefore also the same latency for the data." Ex. 1005, 195; Ex. 1003, ¶194. In the transmitter, Giordano discusses two clocks (XCLK and TXUSRCLK) that are adjusted to have the same frequency and phase. Ex. 1005, 195. The transmitter has a FIFO block for crossing between XCLK and TXUSRCLK clock domains. *Id.*; Ex. 1003, ¶194. Giordano discloses bypassing this FIFO block by using a phase alignment option provided in Xilinx Virtex-5 FPGA systems. Ex. 1005, 195; Ex. 1003, ¶194. Through this built-in phase alignment, XCLK and TXUSRCLK are phase aligned, in which "the transmit FIFO is unnecessary and therefore we bypassed it." Ex. 1005, 197.

Virtex-UG further discloses[6] this limitation. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses this limitation. Ex. 1003, ¶195.

In the receiver, Virtex-UG confirms this FIFO bypass. When receiver clock phase alignment is used, "RXUSRCLK must be driven directly from RXRECCLK using a BUFR regional clock buffer." Ex. 1009, 179 ("Using RX Phase Alignment to Bypass the RX Elastic Buffer"). Due to phase alignment, "SIPO parallel clock phase matches RXUSRCLK phase" and there is "no phase difference between XCLK and RXUSRCLK." *Id*., 180. With no phase difference, the RX Elastic Buffer (which is the FIFO block described in Giordano) is bypassed. This bypass is described in the red arrow below in Figure 7-22 of Virtex-UG:

[6] The Virtex-UG's disclosures in this Petition are express and also inherent.

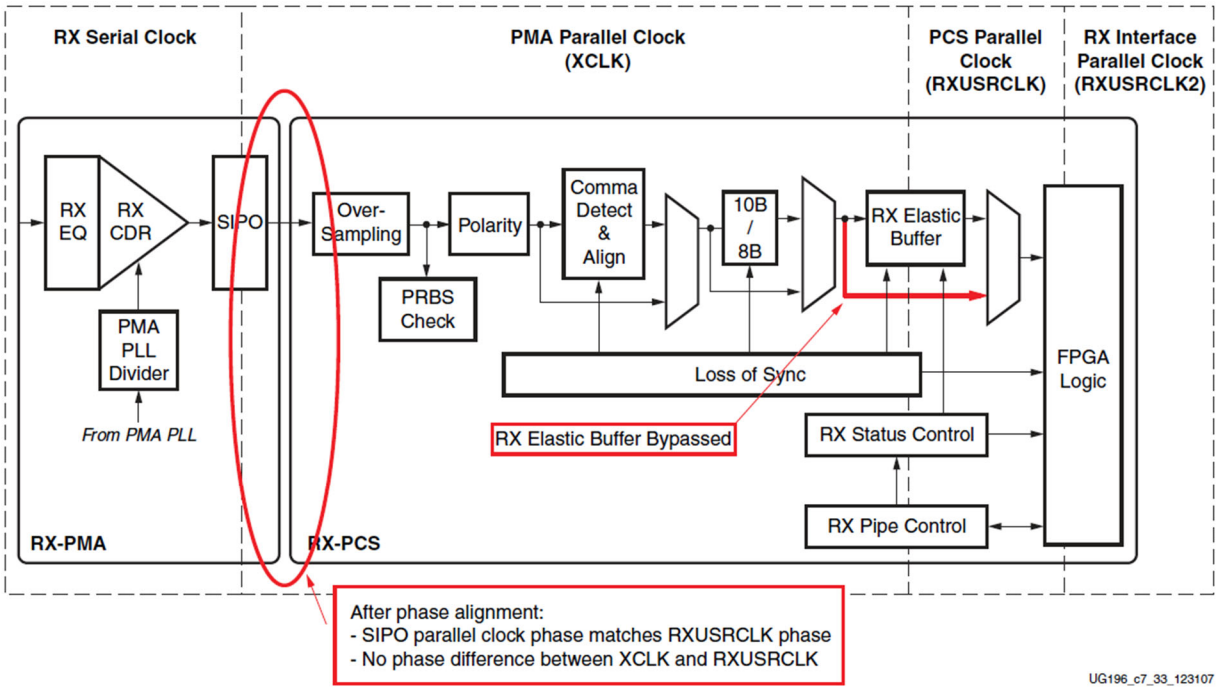


Figure 7-22: **Using Phase Alignment**

The bypass of all clock domain crossing circuits after phase alignment of clock signals, as in Giordano, discloses this limitation. Ex. 1003, ¶197.

[1.n]: "(m) transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams;"

Giordano discloses this limitation. Ex. 1003, ¶198.

As discussed in elements [1.g], [1.k.iii], and [1.m], Giordano's Transmitter Unit PMA with the Shared PLL discloses the claimed "serializer," Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS together disclose the "computational circuitry," and Giordano's processed parallel data exiting the Transmitter Unit PCS into the PMA discloses the "second plurality of parallel data streams."

Giordano discloses transmitting parallel data from the Transmitter Unit PCS into the PISO block of the Transmitter Unit PMA, disclosing this limitation. Ex. 1005, Fig. 1; Ex. 1003, ¶200.

[1.o]: "(n) converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and"

Giordano discloses this limitation. Ex. 1003, ¶201. As discussed in element [1.m], Giordano's PISO block input discloses the "second plurality of parallel data streams."

Giordano's Transmitter Unit PMA discloses the claimed "serializer." Ex. 1005, 195–196; Ex. 1003, ¶202. The Transmitter PMA includes a Parallel Input to Serial Output ("PISO") block that converts parallel data to serial data. Ex. 1005, 195; Ex. 1003, ¶202. The serial data output of PISO discloses the "second serial data stream." Ex. 1003, ¶202.

This mirrors the '865 patent, which describes a serializer with a transmitter PMA with a Parallel to Serial block. Ex. 1001, 53:60–54:13, Fig. 7B. Like Giordano, this Parallel to Serial block converts the incoming parallel data to serial data. *Id*.

[1.p]: "(o) transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface, the second serial data stream."

Giordano discloses this limitation. Ex. 1003, ¶204.

As discussed in elements [1.k.iii] and [1.o], Giordano's Transmitter Unit PMA with the Shared PLL discloses the claimed "serializer," where the output of the PISO block discloses the "second serial data stream."

The Transmitter Unit PMA in Giordano has a TX Driver that sends out serial data, which discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶206. Giordano discloses package pins that interface the Transmitter Unit PMA with external components, which disclose the claimed "second plurality of data pins" of the "first interface." Ex. 1005, Fig. 1; Ex. 1003, ¶206. This Transmitter Unit PMA transmits processed serial data, *i.e.*, "second serial data stream," off the FPGA. Ex. 1005, 195; Ex. 1003, ¶206.

This mirrors the '865 patent, which describes a Transmitter PMA with a Transmitter Buffer that sends out serial data. Ex. 1001, 53:60–54:13, Fig. 7B.

b. Claims 2–4

Claims 2–4 concern the relationship between "first clock signal" (with "first frequency" and "first phase") and "first transmitter side clock signal" (with "third frequency" and "third phase"). Giordano in view of Kaviani renders obvious these claims. Ex. 1003, ¶208.

As discussed in elements [1.b] and [1.j], HSCLK discloses the "first clock signal" and TXUSRCLK discloses the "first transmitter side clock signal." As

discussed in element [1.k], TXUSRCLK is phase-matched with RXRECCLK (which discloses the "first receiver side clock signal").

[2]: "The method of claim 1, wherein the third frequency corresponds to the first frequency."

[3]: "The method of claim 2, wherein the third phase is not aligned with the first phase."

[4]: "The method of claim 1, wherein the third frequency is different than the first frequency."

Giordano discloses claims 2–4. Ex. 1003, ¶210.

Giordano discloses that in the Receiver Unit PMA, "HSCLK is divided down by 5 and then fed in a 5-bit shift-register," which then becomes RXRECCLK. Ex. 1005, 196, Fig. 3. Using signal RXSLIDE from the FPGA Fabric, this 5-bit shift-register selects the phase shift of RXRECCLK with respect to HSCLK. *Id.*; Ex. 1003, ¶211. As such, RXRECCLK, in this implementation, has a frequency that is 20% (one-fifth) of that of HSCLK, and shifted in phase (by the 5-bit shift-register) to HSCLK. Ex. 1003, ¶211.

Since TXUSRCLK is phase-matched with RXRECCLK, TXUSRCLK also has a frequency that is one-fifth of that of HSCLK, and phase-shifted to HSCLK. Ex. 1003, ¶212. This discloses claims 3 and 4.

Since TXUSRCLK has a frequency that is one-fifth of that of HSCLK, the two clock frequencies "correspond" with each other. Ex. 1003, ¶213. This discloses claim 2.

Virtex-UG further discloses claim 2. If "correspond" requires the two frequencies to be identical, Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 2. Ex. 1003, ¶214. As discussed in elements [1.b] and [1.j], HSCLK discloses the "first clock signal" and TXUSRCLK discloses the "first transmitter side clock signal." As discussed in element [1.k], TXUSRCLK is phase-matched with RXRECCLK (which discloses the "first receiver side clock signal").

Virtex-UG discloses configuration signals PLL_RXDIVSEL_OUT and PLL_DIVSEL_REF. Ex. 1009, 72. These are exemplary user configuration signals for the Xilinx Virtex-5 GTP Transceivers that control dividers that relate to RXRECCLK (and through control of RXRECCLK, impacts TXUSRCLK). Ex. 1003, ¶215. PLL_RXDIVSEL_OUT, which can be set to 1, 2, or 4, is used to divide the incoming clock signal to produce a receiver side clock. Ex. 1009, 73; Ex. 1003, ¶215. Virtex-UG discloses that setting PLL_RXDIVSEL_OUT to 1 results in a clock division of one, hence the same frequency. Ex. 1009, 77 (providing example where incoming clock at 1.5625 GHz with "the external divider (PLL_RXDIVSEL_OUT)" set to 1 results in same clock rate of 1.5625 GHz); Ex. 1003, ¶215. Likewise, PLL_DIVSEL_REF "[c]ontrols the reference clock divider," hence it impacts both RXRECCLK and TXUSRCLK at the same time, and can be set to 1 or 2. Ex. 1009, 73; Ex. 1003, ¶215.

Virtex-UG's disclosures of clock dividers that divide by one disclose this limitation. As discussed in Ground 1, claim 3, Giordano discloses that in the Receiver Unit PMA, "HSCLK is divided down by 5" by a clock divider (denoted as "÷ 5"), which then outputs RXRECCLK. Ex. 1005, 196, Fig. 3. As such, RXRECCLK, in this implementation, has a frequency that is 20% (one-fifth) of that of HSCLK.

It would have been obvious to a POSITA to modify the "÷ 5" block in Giordano to incorporate the clock dividers of Virtex-UG, namely those that can be set to 1. Ex. 1003, ¶217. With such clock divider, RXRECCLK (and thus TXUSRCLK) would have the same frequency as HSCLK, rendering obvious this limitation. Ex. 1003, ¶217.

c. Claim 5

[5]: "The method of claim 1, wherein the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation."

Giordano discloses this limitation. Ex. 1003, ¶218. As discussed in element [1.m], Giordano's disclosures on PCS layer processing and FPGA Fabric "logic" disclose the claimed "set of operations."

The operations on PCS layers and FPGA Fabric each disclose this limitation.

Giordano's Comma Detector and Aligner implemented in the FPGA Fabric performs pattern matching (detecting comma characters in the raw 10-bit data),

comparison (determining the number of bit shifts required), and conditional branching (the even/odd decision logic that either applies RXSLIDE assertions or resets the CDR). Ex. 1005, 198. These are examples of logical operations, which disclose this limitation. Ex. 1003, ¶220.

In addition, Giordano points to the PCS layer (both receiver and transmitter sides) as "processing" data, rendering obvious computational circuitry. Ex. 1005, 194; Ex. 1003, ¶221. The PCS layer includes 8b/10b encoding / decoding functions, which require arithmetic calculations, hence rendering obvious this claim. Ex. 1005, 197; Ex. 1003, ¶221.

d. Claim 6

[6]: "The method of claim 1, wherein the first amount of data streams is the same as the second amount of data streams."

Giordano's disclosure of 8b/10b encoding / decoding discloses this limitation. Ex. 1003, ¶222.

Giordano discloses using 8b/10b encoding, where the SIPO deserializes incoming stream 10-bit parallel words, then decoded into 8-bit parallel data words. Ex. 1005, 195. On the transmit side, the FPGA fabric supplies 8-bit parallel data words to the GTP, which encodes them using the internal 8b-to-10b encoder before the PISO serializes the resulting 10-bit words. Ex. 1005, 195, 197. A POSITA would have found it obvious to have what is identified as the first amount of data

streams to be identical to the second amount of data streams, either 8-bits or 10-bits. Ex. 1003, ¶223.

e. Claim 7

[7]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams."

Giordano discloses this limitation. Ex. 1003, ¶224. As discussed in claim 6, Giordano discloses internal parallel data width to be the same on both receiver and transmitter sides.

Giordano's use of 8-bit parallel words (eight data streams) and 10-bit parallel words (ten data streams) discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶225.

f. Claim 8

[8]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer."

Giordano discloses this limitation. Ex. 1003, ¶226.

Giordano discloses use of 8-bit parallel words (eight data streams), which is two to the power of three and discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶227.

g. Claim 9

[9]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer."

Giordano discloses this limitation. Ex. 1003, ¶228.

Giordano discloses use of 10-bit parallel words (ten data streams), which is ten times two to the power of zero and discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶229.

h. Claim 10

[10]: The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

Giordano discloses this claim. Ex. 1003, ¶230.

Virtex-UG further discloses claim 10. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 10. Ex. 1003, ¶231. As discussed in Ground 1, elements [1.h] and [1.m], Giordano's SIPO block output, further processed by the Receiver Unit PCS, disclose the "first amount of data streams," and processed parallel data going through the Transmitter Unit PCS and PMA disclose the "second amount of data streams."

Virtex-UG discloses that the Virtex-5 FPGA GTP Transceiver supports 64b/66b encoding, in addition to the 8b/10b encoding demonstrated by Giordano (using the same Virtex-5 FPGA GTP Transceiver). Ex. 1009, 283, 286, 290; Ex. 1005, 194 ("The architecture we present in this paper is based on the GTP transceiver

of the Xilinx Virtex 5 FPGA family"); Ex. 1003, ¶232. By using the 64b/66b encoding standard, it would have been obvious to modify the GTP transceiver of the proposed combination to support 66-bit data words. Ex. 1003, ¶232. This would have rendered obvious the first and second amounts of data streams at 66 bits. Ex. 1003, ¶232. Since 66 is 33 times two to the power of one, Virtex-UG discloses this limitation.

i. Claim 11

[11]: The method of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.

Giordano discloses this claim. Ex. 1003, ¶233. As discussed in element [1.k], Kaviani's Clock Generator output (C0) discloses the "second clock signal" (with the fourth frequency), and output from Giordano's Shared PLL discloses the "first wire rate clock" (with the fifth frequency). As discussed in claim 8, Giordano discloses 8-bit and 10-bit words, which disclose the "second amount of data streams."

Giordano's disclosure of 10-bit words as the claimed "second amount" means that the claimed "second amount of data streams" is equal to ten. Ex. 1003, ¶234. This, with Giordano's use of clock dividers, discloses this limitation.

Giordano discloses that the output of the Shared PLL ("first wire rate clock") is connected to a divider block denoted "÷N," which in turn outputs TXOUTCLK. A POSITA would have understood N to be an integer, including ten. Ex. 1003, ¶235. This results in Giordano's Shared PLL output ("first wire rate clock") having a

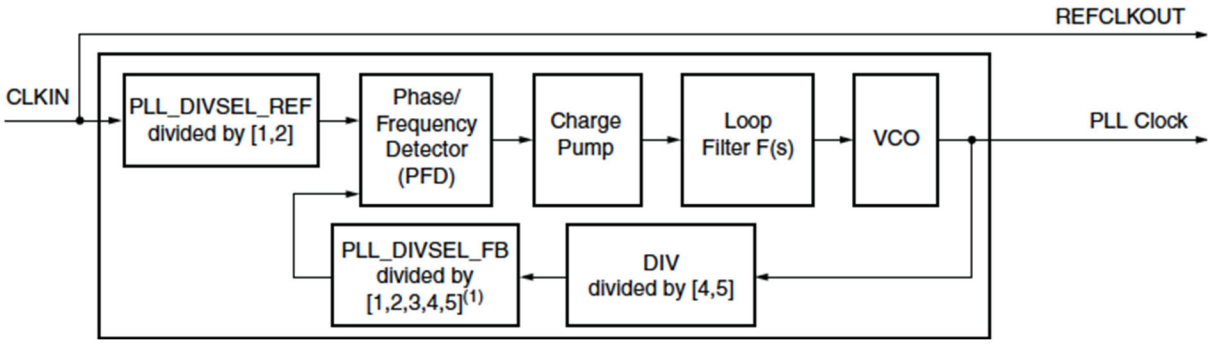
frequency ten times that of TXOUTCLK. Ex. 1003, ¶235. Since TXOUTCLK is synchronized with Clock Generator output ("second clock signal"), it would have been obvious to a POSITA for the two clocks to have the same frequency. Ex. 1003, ¶235. Hence the Shared PLL output ("first wire rate clock") would have a frequency ten times that of Clock Generator output ("second clock signal"), rendering obvious this limitation. Ex. 1003, ¶235.

Virtex-UG further discloses claim 11. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 11. Ex. 1003, ¶236. As discussed in element [1.k], Kaviani's Clock Generator output (C0) discloses the "second clock signal" (with the fourth frequency), and output from Giordano's Shared PLL discloses the "first wire rate clock" (with the fifth frequency). As discussed in claim 8, Giordano discloses 8-bit and 10-bit words, which disclose the "second amount of data streams."

Giordano's disclosure of 10-bit words as the claimed "second amount" means that the claimed "second amount of data streams" is equal to ten. Ex. 1003, ¶236. This, with Giordano's use of clock dividers, discloses this limitation.

Giordano discloses that the output of the Shared PLL ("first wire rate clock") is connected to a divider block denoted "÷N," which in turn outputs TXOUTCLK.

Virtex-UG discloses two divider blocks DIV and PLL_DIVSEL_FB, when put together, could divide signals by eight or ten. Per Figure 5-2 of Virtex-UG, an exemplary cascade of dividers is shown:



The clock path that includes the PLL_DIVSEL_FB block and the DIV block results in various combinations of frequency divisions. Ex. 1003, ¶240. For example, PLL_DIVSEL_FB dividing by 2 and DIV dividing by 5 results in overall division of ten. Ex. 1003, ¶240. PLL_DIVSEL_FB dividing by 2 and DIV dividing by 4 results in overall division of eight. Ex. 1003, ¶240.

Applying this to the proposed combination, a POSITA would have known to implement Virtex-UG's cascaded dividers into Giordano's divider block "÷N." Ex. 1003, ¶241. Using the cascade to have total division of ten results in Giordano's Shared PLL output ("first wire rate clock") having a frequency ten times that of TXOUTCLK. Ex. 1003, ¶241. Since TXOUTCLK is synchronized with Clock Generator output ("second clock signal"), it would have been obvious to a POSITA for the two clocks to have the same frequency. Ex. 1003, ¶241. Hence the Shared PLL output ("first wire rate clock") would have a frequency ten times that of Clock

Generator output ("second clock signal"), rendering obvious this limitation. Ex. 1003, ¶241.

j. Claim 12

[12]: "The method of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams."

Giordano in view of Kaviani renders obvious this claim. Ex. 1003, ¶242. As discussed in element [1.k], Kaviani's Clock Generator output (C0) discloses the "second clock signal" (with the fourth frequency), and output from Giordano's Shared PLL discloses the "first wire rate clock" (with the fifth frequency). As discussed in claim 8, Giordano discloses 8-bit and 10-bit words, which disclose the "second amount of data streams."

Giordano's disclosure of 10-bit words as the claimed "second amount" means that the claimed "half of the second amount of data streams" is equal to five. Ex. 1003, ¶243. This, with Giordano's use of clock dividers, discloses this limitation.

Giordano discloses using clock dividers of "÷ 5" for the receiver clock divider. Ex. 1005, Fig. 3. On the transmitter side, the output of the Shared PLL ("first wire rate clock") is connected to a divider block denoted "÷N," which in turn outputs TXOUTCLK. A POSITA would have known to use the "÷ 5" divider, explicitly used for the receiver side, for the "÷N" block on the transmitter side. Ex. 1003, ¶244. This results in Giordano's Shared PLL output ("first wire rate clock") having a frequency five times that of TXOUTCLK. Ex. 1003, ¶244. Since TXOUTCLK is

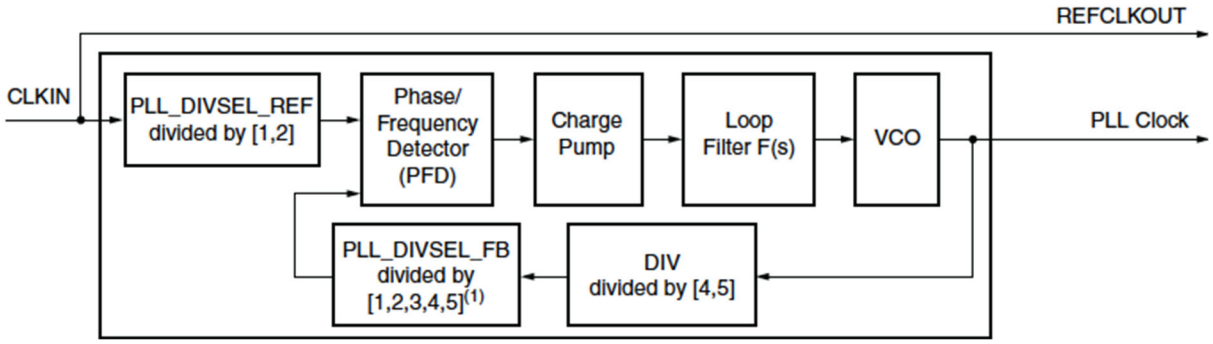
synchronized with Clock Generator output ("second clock signal"), it would have been obvious to a POSITA for the two clocks to have the same frequency. Ex. 1003, ¶244. Hence, the Shared PLL output ("first wire rate clock") would have a frequency five times that of Clock Generator output ("second clock signal"), rendering obvious this limitation. Ex. 1003, ¶244.

Virtex-UG further discloses claim 12. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 12. Ex. 1003, ¶245. As discussed in claim 11, Virtex-UG discloses cascading dividers that support a multitude of clock frequency division options.

Giordano's disclosure of 10-bit words as the claimed "second amount" means that the claimed "second amount of data streams" is equal to ten. Ex. 1003, ¶246. This, with Giordano's use of clock dividers, discloses this limitation.

Giordano discloses that the output of the Shared PLL ("first wire rate clock") is connected to a divider block denoted "÷N," which in turn outputs TXOUTCLK.

Virtex-UG discloses two divider blocks DIV and PLL_DIVSEL_FB, that when put together, could divide signals by four or five. Per Figure 5-2 of Virtex-UG, an exemplary cascade of dividers is shown:



The clock path that includes the PLL_DIVSEL_FB block and the DIV block results in various combinations of frequency divisions. Ex. 1003, ¶249. For example, PLL_DIVSEL_FB dividing by 1 and DIV dividing by 5 results in overall division of five. Ex. 1003, ¶249. PLL_DIVSEL_FB dividing by 1 and DIV dividing by 4 results in overall division of four. Ex. 1003, ¶249.

Applying this to the proposed combination, a POSITA would have known to implement Virtex-UG's cascaded dividers into Giordano's divider block "÷N." Ex. 1003, ¶250. Using the cascade to have total division of five results in Giordano's Shared PLL output ("first wire rate clock") having a frequency five times that of TXOUTCLK. *Id*. Since TXOUTCLK is synchronized with Clock Generator output ("second clock signal"), it would have been obvious to a POSITA for the two clocks to have the same frequency. *Id*. Hence, the Shared PLL output ("first wire rate clock") would have a frequency five times that of Clock Generator output ("second clock signal"), rendering obvious this limitation. *Id*.

k. Claim 13

[13]: "The method of claim 1, wherein the fourth frequency is a rational multiple of the second frequency."

Giordano in view of Kaviani renders obvious this claim. Ex. 1003, ¶251. As discussed in elements [1.e] and [1.k], Giordano's recovered clock (RXRECCLK) discloses the "second frequency," and Clock Generator output (C0) discloses the "fourth frequency."

In the proposed combination, C0 and RXRECCLK have the same frequency. Multiplication by one is a rational multiple, hence C0 and RXRECCLK disclose this limitation. Ex. 1003, ¶252.

Virtex-UG further discloses claim 13. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 13. Ex. 1003, ¶253. As discussed in elements [1.e] and [1.k], Giordano's recovered clock (RXRECCLK) discloses the "second frequency," and Clock Generator output (C0) discloses the "fourth frequency."

In the proposed combination, C0 is tied to TXUSRCLK, and hence have the same frequency. Ex. 1003, ¶254.

Virtex-UG discloses various potential relationships between TXUSRCLK and RXRECCLK. Depending on the value for PLL_TXDIVSEL_OUT and PLL_RXDIVSEL_OUT, which are control signals for dividers for TXUSRCLK and RXRECCLK respectively, the frequency relationship between the two clocks differ.

Ex. 1009, 72; Ex. 1003, ¶255. PLL_TXDIVSEL_OUT and PLL_RXDIVSEL_OUT can be assigned values of 1, 2, and 4. Ex. 1009, 73. For example, if both PLL_TXDIVSEL_OUT and PLL_RXDIVSEL_OUT are set to 1, 2, or 4, since both TXUSRCLK and RXRECCLK are subject to the same amount of division, with other conditions set the same, TXUSRCLK and RXRECCLK will have the same frequency. This will change if the ratio between PLL_TXDIVSEL_OUT and PLL_RXDIVSEL_OUT shifts. For example, if PLL_TXDIVSEL_OUT is set to 4 while PLL_RXDIVSEL_OUT is set to 1, since the transmitter clock is subject to division of 4 while receiver clock is only subject to division by 1, RXRECCLK's frequency will be four times that of TXUSRCLK. This allows for the frequency ratio between TXUSRCLK and RXRECCLK to range in 1/4, 1/2, 1, 2, and 4, which are all rational multiples, hence disclosing this limitation. Ex. 1003, ¶255.

l. Claim 14

[14]: "The method of claim 1, wherein the phase difference indicator signal is a pulse signal."[7]

Kaviani discloses this claim. Ex. 1003, ¶256.

As discussed in element [1.j], Kaviani discloses a phase in window function. Kaviani discloses a "phase_inwindow" signal used for this phase-matching function,

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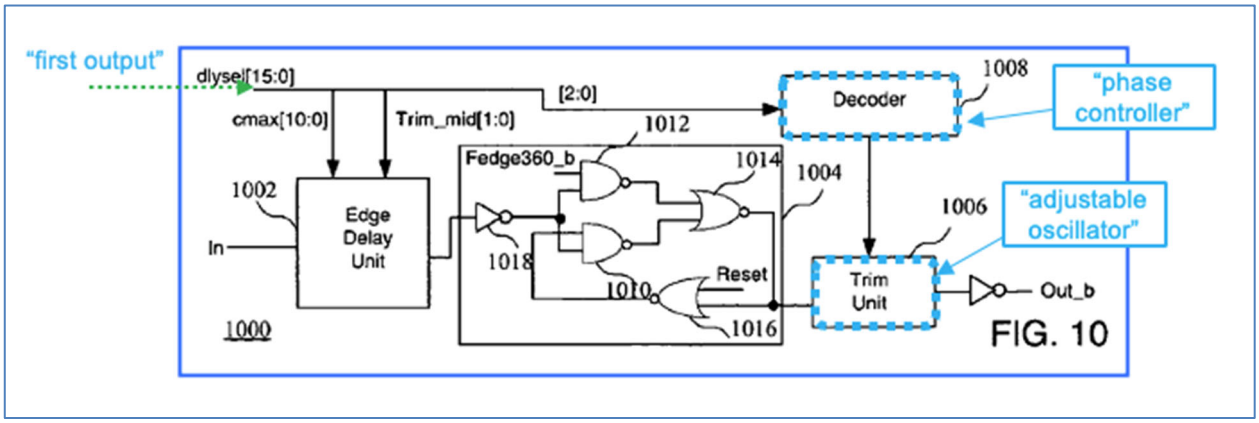
[7] The term "the phase difference indicator signal" lacks antecedent basis. For the purpose of this IPR, Petitioner understands this as a term introduced in claim 14, hence should be understood as "***a*** phase difference indicator signal." Ex. 1003, at 96 n.3.

which takes a form of a pulse signal. Ex. 1010, 6:15–54, Figs. 5–6. Phase_inwindow discloses this limitation. Ex. 1003, ¶257. Kaviani further discloses various pulse signals used for phase matching, which discloses this limitation. Ex. 1010, 11:33–58, Fig. 13; Ex. 1003, ¶257.

m. Claims 15–18

Claims 15–18 concern "adjustment information," which Petitioners understand to refer to the claimed "interim adjustment information." As discussed in element [1.k], the signal from Kaviani's decoder to trim unit (shown in the annotated image below) discloses the claimed "interim adjustment information."



[15]: "The method of claim 1, wherein adjustment information indicates at least one of the following: (A) a desired phase; (B) a desired frequency; (C) a change in phase; and (D) a change in frequency."

Kaviani discloses claim 15. Ex. 1003, ¶259. The control signals to trim unit 1006 include at least an indication of a desired phase and change in phase, disclosing this limitation. *Id.*, 9:46–10:28; Ex. 1003, ¶259.

[16]: "The method of claim 15, wherein adjustment information comprises a voltage."

Kaviani discloses claim 16. Ex. 1003, ¶260. The decoder 1008 takes in a vector signal dlysel[15:0] to control the trim unit, which per Figures 5, 6, and 13 is shown as voltage signals. A POSITA would have understood the output of the decoder to also be a voltage. Ex. 1003, ¶260. Indeed, all control signals (which are described in Figures 5, 6, and 13) take the form of a voltage signal. Ex. 1003, ¶260.

[17]: "The method of claim 16, wherein adjustment information comprises a digital transmission."

Kaviani discloses claim 17. Ex. 1003, ¶261. The control signal is a voltage signal, which is an output from a decoder that takes in vector signal dlysel[15:0]. A POSITA would have understood the output of the decoder to disclose digital transmission. Ex. 1003, ¶261.

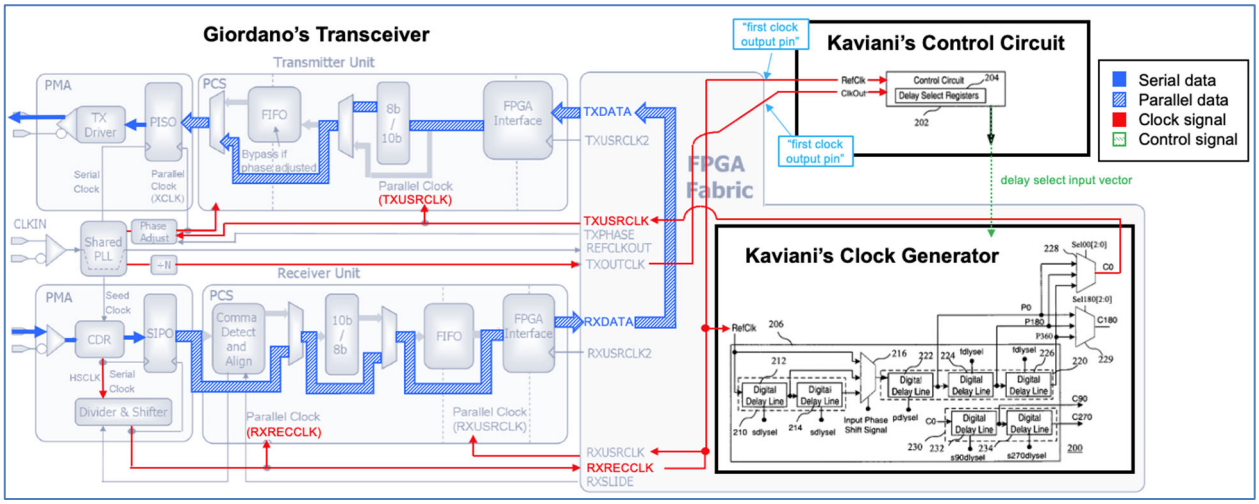
[18]: "The method of claim 1, wherein the adjustment information is used to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay."

Kaviani discloses this claim. Ex. 1003, ¶262. Kaviani discloses that this trim unit 1006 "provides a fine grain delay adjustment to the combined clock signal," which is controlled by decoders. *Id.*, 9:46–10:28. This discloses at least setting a delay, which discloses this limitation. Ex. 1003, ¶262.

n. Claim 21

[21.a]: "The method of claim 1, wherein the first clock output pin is operationally connected to the deserializer and the second clock output pin is operationally connected to the serializer; and"

Giordano in view of Kaviani renders obvious this limitation. Ex. 1003, ¶263. As discussed in elements [1.i] and [1.k], the connection from the FPGA Fabric to Kaviani's off-FPGA Control Circuit inputs disclose the clock output pins—the connection to RefClk input discloses "first clock output pin" and that to ClkOut input discloses "second clock output pin." As discussed in elements [1.c] and [1.k], Giordano's Receiver Unit PMA discloses the claimed "deserializer" and Transmitter Unit PMA with the Shared PLL discloses the claimed "serializer." Overall connections, with the two output pins marked in blue, are shown in the annotated image below:



In the proposed combination, RefClk input ("first clock output pin") of Kaviani's Control Circuit is connected to Receiver Unit PMA ("deserializer")

through RXRECCLK ("receiver side clock signal"). ClkOut input ("second clock output pin") of Kaviani's Control Circuit is connected to the Shared PLL through TXOUTCLK ("interim transmitter side clock signal"). Having signal connections between a circuit component and pin would have been understood as being operationally connected, hence the connections above render obvious this limitation. Ex. 1003, ¶264.

[21.b]: "wherein the phase detector is not on the field programmable gate array and is operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array."

Giordano in view of Kaviani renders obvious this limitation. Ex. 1003, ¶265. As discussed in element [1.i], Kaviani's Control Circuit discloses the off-FPGA-chip "phase detector."

In the proposed combination, RefClk input ("first clock output pin") of Kaviani's Control Circuit is connected to Receiver Unit PMA ("deserializer") through RXRECCLK ("receiver side clock signal"). ClkOut input ("second clock output pin") of Kaviani's Control Circuit is connected to the Shared PLL through TXOUTCLK ("interim transmitter side clock signal"). Having signal connections between a circuit component and pin would have been understood as being operationally connected, hence the connections above render obvious this limitation. Ex. 1003, ¶266.

B. Ground 2: Claims 1–21 Are Rendered Obvious by Giordano in View of Kaviani Further in View of Raymond

1. Prior Art Overview

The proposed combination is to use the Giordano and Kaviani combination of Ground 1 and further modify the FPGA for financial trading applications explicitly disclosed in Raymond.

a. Motivation to Combine Giordano, Kaviani, and Raymond

Motivations to combine Giordano and Kaviani are detailed in Ground 1. Section VI.A.1 (Ground 1 Prior Art Overview).

A POSITA would have been motivated to look to Raymond to combine with Giordano and Kaviani.

Raymond emphasizes the importance of minimizing latency in communication devices, particularly for applications such as financial exchange. Ex. 1007 at 1:18–38. Raymond recognizes that higher clock rates reduce latency but also notes that this requires adding a distinct (faster) clock, and additional clock conversions introduce unwanted latency. *Id*., 8:40–50.

A POSITA reading Raymond would therefore have recognized that Giordano in view of Kaviani offers a solution for synthesizing clock signals at the required frequencies while managing phase alignment and filtering jitter—precisely the clock distribution challenges Raymond identifies. Section VI.A.1.a (Motivation to Combine Giordano and Kaviani); Ex. 1003, ¶272.

A POSITA would have recognized Giordano in view of Kaviani as an attractive solution for the PLL functionality depicted in Raymond's system, and motivated to look to Giordano and Kaviani to combine with Raymond. Raymond repeatedly discusses implementing its invention with Xilinx UltraScale GTY transceivers. Ex. 1007 at 5:48–56, 6:3–8, 8:18–28, 8:51–55. A POSITA reading Raymond would have naturally consulted Xilinx's own materials (such as Kaviani, a Xilinx patent) and publications demonstrating Xilinx FPGA implementations (such as Giordano), for a PLL-based phase alignment solution. Ex. 1003, ¶273.

A POSITA would have had a reasonable expectation of success in combining Giordano, Kaviani, and Raymond. A POSITA would have recognized that the FPGA's programmable logic and on-chip clock management resources could be configured to implement the teachings of the three references as needed. Ex. 1003, ¶274. Because all references suggest implementations with Xilinx transceiver infrastructure, a POSITA would have had a high expectation that the combination would function as intended. Section VI.A.1.a (Motivation to Combine Giordano and Kaviani); Ex. 1003, ¶274.

2. Analysis

a. Independent Claim 1

[1.pre]: "A method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of:"

If the preamble is found limiting with respect to "market data" and "entry data," Raymond discloses [1.pre]. Ex. 1003, ¶275.

Raymond expressly identifies electronic trading as a primary application for its ultra-low latency communication device, and describes the incoming and outgoing data streams in terms that correspond directly to market data and order entry data. For example, Raymond discloses incoming and outgoing serial data streams in the context of "financial trading data," which are transmitted to and from "financial exchange." Ex. 1007, 4:52–65.

Indeed, Raymond discloses "market data feed handler" and "market data feed distribution systems" applications, disclosing receiving market data. Ex. 1007, 13:61–64; Ex. 1003, ¶277. Raymond further discloses that the outgoing data link layer signal 250 is "outputted after logical processing (*e.g.*, applying financial trading algorithms)," hence disclosing sending out financial order related data and operations associated with trading algorithms. *Id.* at 11:57–60; Ex. 1003, ¶277.

[1.a] through [1.p]:

Giordano in view of Kaviani renders obvious these limitations. Section VI.A.2.a (Ground 1, cl. 1).

b. Claims 2–4

Giordano in view of Kaviani renders obvious these claims. Section VI.A.2.b (Ground 1, cls. 2–4).

c. Claim 5

[5]: "The method of claim 1, wherein the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation."

Giordano in view of Kaviani renders obvious this claim. Section VI.A.2.c (Ground 1, cl. 5).

Raymond further discloses this limitation. Ex. 1003, ¶281.

Raymond discloses that data on the transmitting side includes "an outgoing data link layer signal 250 that has been outputted after logical processing (*e.g.*, applying financial trading algorithms)" and "[a] transmitting side PCS module 92 converts the data link layer signal to an outgoing electrical physical layer parallel output signal 252." Ex. 1007, 11:57–63. The applying of financial trading algorithms in Raymond discloses the claimed "first set of operations." Ex. 1003, ¶282. Raymond's application of financial trading algorithms involves arithmetic operations, hence discloses this limitation. Ex. 1007, 11:57–60; Ex. 1003, ¶282.

d. Claim 6

[6]: "The method of claim 1, wherein the first amount of data streams is the same as the second amount of data streams."

Giordano in view of Kaviani renders obvious this claim. Section VI.A.2.d (Ground 1, cl. 6).

Raymond further discloses this limitation. Ex. 1003, ¶284.

Raymond discloses that "the transmitting-side SerDes module 256 can have the same serialization ratio as the de-serialization ratio of the receiving side SerDes module 240." Ex. 1007, 12:23–25. The same ratio results in the same parallel data streams, hence rendering this limitation obvious. Ex. 1003, ¶285.

e. Claim 7

[7]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams."

Giordano in view of Kaviani renders obvious this claim. Section VI.A.2.e (Ground 1, cl. 7).

Raymond further discloses this limitation. Ex. 1003, ¶287.

Raymond discloses that "the UltraScale™ GTY from Xilinx™ has internal data buses of 16, 20, 32, 40 or 64 bits, with a minimum bit-width of 16 bits and a minimum de-serialization ratio of 1:16." Ex. 1007, 6:5–8. A POSITA would have

understood that the SerDes module 208 could be configured to apply any of these de-serialization ratios depending on the application requirements, and that the serialization ratio of SerDes module 256 would match. Ex. 1003, ¶288.

f. Claim 8

[8]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer."

Giordano in view of Kaviani renders obvious this claim. Section VI.A.2.f (Ground 1, cl. 8).

Raymond further discloses this limitation. Ex. 1003, ¶290.

Raymond discloses "internal data buses of 16, 20, 32, 40 or 64 bits." Ex. 1007, 6:5–8. 16 is two to the power of four, 32 is two to the power of five, and 64 is two to the power of six; hence, Raymond's 16, 32, and 64 bit buses disclose this limitation. Ex. 1003, ¶291.

g. Claim 9

[9]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer."

Giordano in view of Kaviani renders obvious this claim. Section VI.A.2.g (Ground 1, cl. 9).

Raymond further discloses this limitation. Ex. 1003, ¶293.

Raymond discloses "internal data buses of 16, 20, 32, 40 or 64 bits." Ex. 1007, 6:5–8. 20 is ten times two to the power of one, and 40 is ten times two to the

power of two; hence, Raymond's 20 and 40 bit buses disclose this limitation. Ex. 1003, ¶294.

h. Claims 10–18

Giordano in view of Kaviani renders obvious these claims. Sections VI.A.2.h–VI.A.2.m (Ground 1, cls. 10–18).

i. Claim 19

[19]: "The method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm."

Raymond further discloses this limitation. Ex. 1003, ¶296.

As discussed in [1.pre], Raymond discloses applying financial trading algorithms to market data to generate order entry data. Ex. 1003, ¶297.

j. Claim 20

[20]: "The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data."

Raymond further discloses this limitation. Ex. 1003, ¶298.

As discussed in [1.pre], Raymond discloses applying financial trading algorithms to market data to generate order entry data. Ex. 1003, ¶299.

k. Claim 21

Giordano in view of Kaviani renders obvious this claim. Section VI.A.2.n (Ground 1, cl. 21).

C. Ground 3: Claims 1–18, 21 Are Rendered Obvious by Giordano in View of Kaviani further in View of Virtex-UG

1. Prior Art Overview

The proposed combination is to use the Giordano and Kaviani combination of Ground 1 and further modify transceiver and FPGA configurations as necessary based on the teachings of Virtex-UG.

a. Motivation to Combine Giordano, Kaviani, and Virtex-UG

While Giordano already inherently discloses and incorporates Virtex-UG, if necessary, a POSITA would have been motivated to look to Virtex-UG to combine with Giordano and Kaviani. Virtex-UG is a user guide for Xilinx Virtex FPGA offerings, which is the FPGA chip used in Giordano and referenced in Kaviani. Ex. 1005, 194, 197–199; Ex. 1010, 1:44–49. Virtex-UG details how to use, configure, and modify the Virtex-5 FPGA "RocketIO" GTP transceiver. *See generally* Ex. 1009; Ex. 1003, ¶303.

A POSITA reading Virtex-UG would therefore have recognized that its teachings would be helpful in the use, configuration, and modification of the FPGA system based on Giordano in view of Kaviani, including for synthesizing clock signals at the required frequencies while managing phase alignment and filtering jitter. Section VI.A.1.a (Motivation to Combine Giordano and Kaviani); Ex. 1003, ¶304.

A POSITA would have had a reasonable expectation of success in combining Giordano, Kaviani, and Virtex-UG. A POSITA would have recognized that the FPGA's programmable logic and on-chip clock management resources could be configured to implement the teachings of the three references as needed. Ex. 1003, ¶305. Because all references suggest implementations with Xilinx transceiver infrastructure, a POSITA would have had a high expectation that the combination would function as intended. Section VI.A.1.a (Motivation to Combine Giordano and Kaviani); Ex. 1003, ¶305.

2. Analysis

a. Claims 1–18, 21

Giordano in view of Kaviani and Virtex-UG renders obvious these claims. Section VI.A.2 (Ground 1, Analysis).

D. Ground 4: Claims 1–21 Are Rendered Obvious by Giordano in View of Kaviani, Virtex-UG, and Raymond

1. Prior Art Overview

The proposed combination is to use the Giordano, Kaviani, and Virtex-UG combination of Ground 3 and further modify the FPGA for financial trading applications explicitly disclosed in Raymond.

a. Motivation to Combine Giordano, Kaviani, Virtex-UG, and Raymond

Motivations to combine Giordano, Kaviani, and Virtex-UG are detailed in Ground 3. Section VI.C.1 (Ground 3 Prior Art Overview).

A POSITA would have been motivated to look to Raymond to combine with Giordano, Kaviani, and Virtex-UG, for the same reasons to combine Raymond with Giordano and Kaviani. Section VI.B.1 (Ground 2 Prior Art Overview).

2. Analysis

a. Claims 1–21

Giordano in view of Kaviani and Virtex-UG renders obvious claims 1–18, 21. Section VI.C.2 (Ground 3, cls. 1–18, 21).

In addition, if the preamble of claim 1 is found limiting with respect to "market data" and "entry data," Raymond discloses [1.pre]. Section VI.B.2.a (Ground 2, cl. 1).

Raymond further discloses claims 5–9, 19–20. Sections VI.B.2.c–VI.B.2.k (Ground 2, cls. 5–9, 19–20).

VII. CONCLUSION

Petitioners have established a reasonable likelihood that the Challenged Claims are unpatentable. Petitioners therefore respectfully request that IPR be instituted.

DATED: August 3, 2026

Respectfully Submitted,

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CERTIFICATION UNDER 37 C.F.R. §42.24(d)

Under the provisions of 37 C.F.R. §42.24(d), the undersigned attorney hereby certifies that the word count for Sections I–VII of the foregoing Petition for *Inter Partes* Review is 13,888, according to the word count tool in Microsoft Word.

DATED: August 3, 2026

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CERTIFICATE OF SERVICE

The undersigned certifies service pursuant to 37 C.F.R. §§42.6(e) and 42.105(b) on the Patent Owner electronically on the Patent Owner at the following email addresses:

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APPENDIX: CHALLENGED CLAIM LISTING

No.	Limitation
[1.pre]	A method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of:
[1.a]	(a) receiving, by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream;
[1.b]	(b) receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase;
[1.c]	(c) transmitting, from the first plurality of data pins of the first interface to a deserializer in the field programmable gate array, the first serial data stream;
[1.d]	(d) transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal;
[1.e]	(e) generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal;
[1.f]	(f) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;
[1.g]	(g) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal;
[1.h]	(h) transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams;
[1.i]	(i) transmitting, from the deserializer via a first clock output pin on a second interface of the field programmable gate array to a phase detector that is part of the field programmable gate array system and not part of the field programmable gate array, the first receiver side clock signal;

No.	Limitation
[1.j]	(j) generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level:
[1.k]	(i) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase; (ii) generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal; (iii) generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase; (iv) transmitting, from the serializer via a second clock output pin of the second interface to the phase detector, the interim transmitter side clock signal; (v) generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal; (vi) transmitting, from the phase detector to a phase controller of the field programmable gate array system which is placed within the field programmable gate array, the first output; (vii) determining, by the phase controller, interim adjustment information based on the first output; and (viii) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information, wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through (viii) are repeated until the first output of the phase detector is below the first threshold level;
[1.l]	(k) transmitting, from the serializer to the computational circuitry, first transmitter side clock signal;

No.	Limitation
[1.m]	(l) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams, wherein the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams;
[1.n]	(m) transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams;
[1.o]	(n) converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and
[1.p]	(o) transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface, the second serial data stream.
[2]	The method of claim 1, wherein the third frequency corresponds to the first frequency.
[3]	The method of claim 2, wherein the third phase is not aligned with the first phase.
[4]	The method of claim 1, wherein the third frequency is different than the first frequency.
[5]	The method of claim 1, wherein the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.
[6]	The method of claim 1, wherein the first amount of data streams is the same as the second amount of data streams.
[7]	The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

No.	Limitation
[8]	The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.
[9]	The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.
[10]	The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.
[11]	The method of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.
[12]	The method of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.
[13]	The method of claim 1, wherein the fourth frequency is a rational multiple of the second frequency.
[14]	The method of claim 1, wherein the phase difference indicator signal is a pulse signal.
[15]	The method of claim 1, wherein adjustment information indicates at least one of the following: (A) a desired phase; (B) a desired frequency; (C) a change in phase; and (D) a change in frequency.
[16]	The method of claim 15, wherein adjustment information comprises a voltage.
[17]	The method of claim 16, wherein adjustment information comprises a digital transmission.
[18]	The method of claim 1, wherein the adjustment information is used to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay.
[19]	The method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.

No.	Limitation
[20]	The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.
[21.a]	The method of claim 1, wherein the first clock output pin is operationally connected to the deserializer and the second clock output pin is operationally connected to the serializer; and
[21.b]	wherein the phase detector is not on the field programmable gate array and is operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array.