UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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OPTIVER US LLC and OPTIVER TRADING US LLC,
Petitioners

v.

HFT SOLUTIONS, LLC,
Patent Owner.

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Case No. IPR2026-00384
U.S. Patent No. 10,763,865

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**Corrected Declaration of Dr. B. Carrion Schaefer**

## Table of Contents

TABLE OF EXHIBITS ..... 10
TABLE OF ABBREVIATIONS ..... 11
I. BACKGROUND AND QUALIFICATIONS ..... 13
II. SCOPE OF OPINIONS ..... 20
III. MATERIALS REVIEWED ..... 20
IV. Person of Ordinary Skill in the Art ..... 21
V. Statement of Legal Principles ..... 21
A. Legal Standard for Prior Art ..... 21
B. Anticipation and Prior Art ..... 22
C. Legal Standard for Obviousness ..... 23
D. Legal Standard for Claim Construction ..... 29
VI. Summary of the ’865 Patent ..... 32
A. Challenged Claims ..... 33
B. File History of the ’865 Patent ..... 33
VII. Application of the Prior Art to the CHALLENGED Claims ..... 33
C. Priority Date ..... 33
D. Claim Construction ..... 34
E. Overview of Prior Art ..... 34
1. R. Giordano and A. Aloisio, *Fixed- Latency, Multi-Gigabit Serial Links with Xilinx FPGAs*, 58-1 IEEE Transactions on Nuclear Science 194 (2011) (“Giordano”) (Ex. 1005) ..... 34
a) Ex. 1009, Virtex-UG (incorporated by Giordano) ..... 36
2. Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 (“Virtex-UG”) (Ex. 1009) ..... 37
3. U.S. Pat. No. 10,447,463 (“Raymond”) (Ex. 1007) ..... 38
4. U.S. Pat. No. 7,453,301 (“Kaviani”) (Ex. 1010) ..... 40
VIII. State of the Art ..... 40
A. Serialization and Deserialization (SERDES) in FPGAs ..... 41

B. Phase-Locked Loops (PLLs) and Delay-Locked Loops (DLLs) in FPGAs ..43

C. Clock Synchronization and Phase Alignment Between Receiver and Transmitter ....44

D. Application to Financial Trading Systems ....47

E. Summary of State of the Art ....48

IX. Detailed Analysis of Invalidity Grounds ....49

A. Ground 1: Claims 1-18 and 21 Are Rendered Obvious By Giordano in view of Kaviani ....50

1. Prior Art Overview ....50

a) Motivation to Combine Giordano and Kaviani ....52

b) Features of Virtex-UG are Inherent to Giordano, and Giordano Incorporates Virtex-UG by Reference ....56

2. Ground 1 - Analysis ....58

a) Independent Claim 1 ....58

[1.pre]: "A method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of:" ....58

[1.a]: "(a) receiving, by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream;" ....59

[1.b]: "(b) receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase;" ....60

[1.c]: "(c) transmitting, from the first plurality of data pins of the first interface to a deserializer in the field programmable gate array, the first serial data stream;" ....60

[1.d]: "(d) transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal;" ....61

[1.e]: "(e) generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal;" ....61

[1.f]: "(f) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;".....62

[1.g]: "(g) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal;"....63

[1.h]: "(h) transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams;".....64

[1.i]: "(i) transmitting, from the deserializer via a first clock output pin on a second interface of the field programmable gate array to a phase detector that is part of the field programmable gate array system and not part of the field programmable gate array, the first receiver side clock signal;".....64

[1.j]: "(j) generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level:".....66

[1.k]: steps (i) through (viii).....67

"(i) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase;".....68

"(ii) generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal;".....69

"(iii) generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase;".....70

"(iv) transmitting, from the serializer via a second clock output pin of the second interface to the phase detector, the interim transmitter side clock signal;".....70

"(v) generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal;".....71

"(vi) transmitting, from the phase detector to a phase controller of the field programmable gate array system which is placed within the field programmable gate array, the first output;".....72

"(vii) determining, by the phase controller, interim adjustment information based on the first output; and" ..... 73

"(viii) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information, ..... 73

wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through (viii) are repeated until the first output of the phase detector is below the first threshold level;" ..... 74

[1.l]: "(k) transmitting, from the serializer to the computational circuitry, first transmitter side clock signal;" ..... 75

[1.m]: "(l) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams, wherein the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams;" ..... 76

[1.n]: "(m) transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams;" ..... 79

[1.o]: "(n) converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and" ..... 80

[1.p]: "(o) transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface, the second serial data stream." ..... 80

b) Claims 2–4 ..... 81

[2] The method of claim 1, wherein the third frequency corresponds to the first frequency ..... 82

[3]: "The method of claim 2, wherein the third phase is not aligned with the first phase." ..... 82

[4]: "The method of claim 1, wherein the third frequency is different than the first frequency." ..... 82

c) Claim 5 ..... 84

[5]: "The method of claim 1, wherein the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical

operation; (iii) a pipeline operation; and (iv) a memory access operation." .....84

d) Claim 6 .....85

[6]: "The method of claim 1, wherein the first amount of data streams is the same as the second amount of data streams." .....85

e) Claim 7 .....86

[7]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams." .....86

f) Claim 8 .....86

[8]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer." .....86

g) Claim 9 .....86

[9]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer." .....86

h) Claim 10 .....87

[10]: The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer. .....87

i) Claim 11 .....88

[11]: The method of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams...88

j) Claim 12 .....91

[12]: "The method of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams." .....91

k) Claim 13 .....93

[13]: "The method of claim 1, wherein the fourth frequency is a rational multiple of the second frequency." ..... 93

l) Claim 14 ..... 95

[14]: "The method of claim 1, wherein the phase difference indicator signal is a pulse signal." ..... 95

m) Claims 15-18 ..... 95

[15]: "The method of claim 1, wherein adjustment information indicates at least one of the following: (A) a desired phase; (B) a desired frequency; (C) a change in phase; and (D) a change in frequency." ..... 96

[16]: "The method of claim 15, wherein adjustment information comprises a voltage." ..... 96

[17]: "The method of claim 16, wherein adjustment information comprises a digital transmission." ..... 97

[18]: "The method of claim 1, wherein the adjustment information is used to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay." ..... 97

n) Claim 21 ..... 97

[21.a]: "The method of claim 1, wherein the first clock output pin is operationally connected to the deserializer and the second clock output pin is operationally connected to the serializer; and" ..... 97

[21.b]: "wherein the phase detector is not on the field programmable gate array and is operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array." ..... 99

B. Ground 2: Claims 1–21 Are Rendered Obvious By Giordano in view of Kaviani further in view of Raymond ..... 99

1. Prior Art Overview ..... 99

a) Motivation to Combine Giordano, Kaviani, and Raymond ..... 100

2. Ground 2 – Analysis ..... 101

a) Independent Claim 1 ..... 101

[1.pre]: "A method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a

second serial data stream comprising order entry data, wherein the method comprises the steps of:” ..... 101

[1.a] through [1.p]: ..... 102

b) Claims 2-4 ..... 102

c) Claim 5 ..... 103

[5]: “The method of claim 1, wherein the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.” ..... 103

d) Claim 6 ..... 103

[6]: “The method of claim 1, wherein the first amount of data streams is the same as the second amount of data streams.” ..... 103

e) Claim 7 ..... 104

[7]: “The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.” ..... 104

f) Claim 8 ..... 105

[8]: “The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.” ..... 105

g) Claim 9 ..... 105

[9]: “The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.” ..... 105

h) Claims 10–18 ..... 106

i) Claim 19 ..... 106

[19]: “The method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.” ..... 106

j) Claim 20 ..... 106

[20]: "The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data" ..... 106

k) Claim 21 ..... 106

C. Ground 3: Claims 1–18, 21 Are Rendered Obvious By Giordano in view of Kaviani further in view of Virtex-UG ..... 107

1. Prior Art Overview ..... 107

a) Motivation to Combine Giordano, Kaviani, and Virtex-UG ..... 107

2. Ground 3 – Analysis ..... 108

a) Claims 1-18 and 21 ..... 108

D. Ground 4: Claims 1–21 Are Rendered Obvious By Giordano in view of Kaviani , Virtex-UG, and Raymond ..... 108

1. Prior Art Overview ..... 109

a) Motivation to Combine Giordana, Kaviani, and Virtex-UG ..... 109

2. Ground 4 – Analysis ..... 109

a) Claims 1–21 ..... 109

X. Secondary Considerations of Non-Obviousness ..... 110

XI. Conclusion ..... 111

## TABLE OF EXHIBITS

| Exhibit No. | Document |
|---|---|
| 1001 | U.S. Patent No. 10,763,865 ("the '865 patent") |
| 1002 | File History for U.S. Patent No. 10,763,865 |
| 1003 | Declaration of Benjamin Carrion Schaefer, Ph.D. |
| 1004 | Declaration of Carrie Gardner |
| 1005 | R. Giordano and A. Aloisio, *Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs*, 58-1 IEEE Transactions on Nuclear Science 194 (2011) [Giordano] |
| 1006 | *(intentionally omitted)* |
| 1007 | U.S. Pat. No. 10,447,463 [Raymond] |
| 1008 | *(intentionally omitted)* |
| 1009 | Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 [Virtex-UG] |
| 1010 | U.S. Pat. No. 7,453,301 [Kaviani] |
| 1011 | Declaration of Gordon MacPherson |
| 1012 | Curriculum Vitae of Benjamin Carrion Schaefer, Ph.D. |
| 1013 | Redline of Corrected Petition for *Inter Partes Review* of U.S. Patent No. 10,763,865 |
| 1014 | Redline of Corrected Declaration of Benjamin Carrion Schaefer, Ph.D. |

## TABLE OF ABBREVIATIONS

| Abbreviation | Term |
|---|---|
| ’865 patent | U.S. Patent No. 10,763,865 |
| AIA | America Invents Act |
| Challenged Claims | Claims 1–21 of U.S. Patent No. 10,763,865 |
| Ex. | Exhibit |
| Fig. | Figure |
| IPR | *inter partes* review |
| Patent Owner | HFT Solutions, LLC |
| Petitioners | Optiver US LLC and Optiver Trading US LLC |
| Giordano | R. Giordano and A. Aloisio, *Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs*, 58-1 IEEE Transactions on Nuclear Science 194 (2011) |
| Kaviani | U.S. Pat. No. 7,453,301 |
| Raymond | U.S. Pat. No. 10,447,463 |
| Virtex-UG | Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 |
| CDC | Clock Domain Crossing |
| CDR | Clock and Data Recovery |
| DLL | Delay Locked Loop |
| PLL | Phase Locked Loop |
| FPGA | Field Programmable Gate Array |
| PMA | Physical Medium Attachment |
| PCS | Physical Coding Sublayer |
| MAC | Media Access Controller |
| VCO | Voltage Controlled Oscillator |
| VLSI | Very Large Scale Integration |

1. I, Dr. Benjamin Carrion Schaefer, declare as follows:

2. I have been retained by counsel for Petitioners Optiver US LLC and Optiver Trading US LLC to submit a Declaration in support of the Petition for *Inter Partes* Review of U.S. Patent No. 10,763,865 ("the Petition").

3. I have been asked to provide my independent analysis and opinion on whether the '865 patent is invalid over the prior art. My opinions are based on my experience, knowledge, and skill in computer architecture and VLSI design, as well as my experience with field programmable gate arrays and clocking architectures. In preparation for this declaration, I have reviewed the '865 patent, its file history, and all exhibits cited in this Declaration and in the Petition.

4. I may rely upon these materials, my experience and knowledge, and/or additional materials to rebut arguments raised by the Patent Owner. Further, I may also consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me.

5. My analysis of the materials produced in this investigation is ongoing and I will continue to review any new material as it is provided. This Declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

6. I am being paid at my normal hourly rate for my time spent working on this matter. I have no personal or financial stake or interest in the outcome of the Petition.

## I. BACKGROUND AND QUALIFICATIONS

7. My qualifications are stated more fully in my curriculum vitae, which is attached as **Appendix A**. Below is a summary of my education, work experience, and other qualifications.

8. I am an Associate Professor in the Department of Electrical and Computer Engineering at The University of Texas at Dallas ("UTD"), where I also serve as Assistant Dean for Graduate Student Success in the School of Engineering.

9. I hold a Ph.D. in Reconfigurable Computing from The University of Birmingham, United Kingdom (2003); a Master of Science degree in Microelectronics from Birmingham City University, United Kingdom (1999), awarded with distinction; a Bachelor of Engineering degree in Electronic Engineering from Universidad Politecnica, Madrid, Spain (1997); and a Master of Business Administration from McGill University, Canada (2010). My doctoral research focused specifically on reconfigurable computing architectures, which include Field-Programmable Gate Arrays ("FPGAs").

10. I have over twenty years of professional experience in the fields of reconfigurable computing, FPGAs, Electronic Design Automation, High-Level

Synthesis, hardware security, low-power design, and approximate computing. Prior to my current position at UTD, I served as an Assistant Professor in the Department of Electronic and Information Engineering at The Hong Kong Polytechnic University (2012–2016).

11. Before entering academia, I was a Researcher at NEC Corporation's Central Research and Development Laboratories in Japan (2007–2012), where I conducted research on high-level synthesis and FPGA-related design automation. I also held postdoctoral research positions at Seoul National University, Korea (2005–2007) and the University of California, Los Angeles (2003–2004).

12. At UTD, I have held the position of Assistant Professor (2016–2022) and Associate Professor (2022–present). My primary research interests include Reconfigurable Computing, FPGAs, Electronic Design Automation, High-Level Synthesis, Hardware Security, Low-power design, and Approximate Computing. I regularly teach graduate and undergraduate courses directly relevant to the subject matter of the '865 patent, including "Reconfigurable Systems" (a graduate-level course focused on FPGA architectures, design, and implementation), "Computer Architecture," and "Embedded Systems." I also teach an FPGA design course, and one of the projects for that course involves implementing a financial trading algorithm on an FPGA.

13. I have authored or co-authored over 154 publications, including three books, three book chapters, 41 journal articles, and over 106 conference papers. My publications have been cited over 2,400 times, and my h-index is 26 (as of January 2025). My three books focus on High-Level Synthesis, including "High-Level Synthesis Made Easy" (2023, with a Second Edition in 2026) and "High-Level Synthesis: Applications" (2025). My work has been published in leading journals including IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, ACM Transactions on Design Automation of Electronic Systems, and ACM Computing Surveys.

14. A substantial portion of my research career has been devoted specifically to FPGA design, implementation, and optimization. My Ph.D. dissertation at the University of Birmingham focused on reconfigurable computing using FPGAs. Beginning with my earliest publications in 2001 and 2002, I have published extensively on FPGA implementations, including "Scalable Implementation of the Discrete Element Method on a Reconfigurable Computing Platform" (Field-Programmable Logic and Applications, Springer, 2002), "Analysis and implementation of the discrete element method using a dedicated highly parallel architecture in reconfigurable computing" (IEEE Symposium on Field-Programmable Custom Computing Machines, 2002), "Description of a Dedicated

Hardware Architecture for the Discrete Element Method (DEM) implemented on a Field Programmable Gate Array (FPGA)" (ACME, 2002), and "Acceleration of the Discrete Element Method (DEM) on a reconfigurable co-processor" (Computers and Structures, 2004). These early works demonstrate my deep familiarity with FPGA architectures, hardware description, and implementation.

15. Throughout my career, I have continued to publish prolifically on FPGA-related topics. Representative publications include "Enabling High-Level Synthesis Resource Sharing Design Space Exploration in FPGAs Through Automatic Internal Bitwidth Adjustments" (IEEE Transactions on Computer-Aided Design, 2017); "Learning from the Past: Efficient High-Level Synthesis Design Space Exploration for FPGAs" (ACM TODAES, 2022); "Hardware-assisted Simulation of Voltage-behind-reactance Models of Electric Machines on FPGA" (IEEE Transactions on Energy Conversion, 2020); "Accelerating FPGA Prototyping through Predictive Model-Based HLS Design Space Exploration" (DAC, 2019); "Efficient and reliable High-Level Synthesis Design Space Explorer for FPGAs" (FPL, 2016); "Low Power Design of Runtime Reconfigurable FPGAs through Contexts Approximations" (ICCD, 2019); and "FREEDOM: FPGA-based Hardware Redaction Emulator" (FCCM, 2025). I have also served on the Technical Program Committees of the premier FPGA conferences, including the IEEE Conference on Field Programmable Gate Arrays (FPL), IEEE International Symposium on Field-

Programmable Custom Computing Machines (FCCM), and the IEEE Conference on Field Programmable Technology (FPT).

16. My research also encompasses clocking architectures and frequency control mechanisms used in connection with FPGAs, which are directly relevant to the subject matter of the ’865 patent. I have published research addressing clock domain management and dynamic frequency scaling in reconfigurable architectures, including: “Tunable Multiprocess Mapping on Coarse-Grain Reconfigurable Architectures With Dynamic Frequency Control” (IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016), which addresses dynamic frequency control techniques in reconfigurable FPGA-based architectures; “Micro-architecture Tuning for Dynamic Frequency Scaling in Coarse-Grain Runtime Reconfigurable Arrays with Adaptive Clock Domain Support” (IEEE ISVLSI, 2021), which specifically addresses adaptive clock domain support in runtime reconfigurable arrays; and “Low Power Design through Frequency-Optimized Runtime Micro-architectural Adaptation” (ICCD, 2019), which addresses frequency optimization in reconfigurable computing systems. These publications demonstrate my expertise in the design and implementation of clocking mechanisms, clock domain crossings, and frequency management in FPGA and reconfigurable computing systems.

17. My research further encompasses high-speed data communication and interconnect technologies relevant to serialization and deserialization (“SerDes”) in

FPGA systems. I co-authored "Recent trends and considerations for high speed data in chips and system interconnects" (SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference (IMOC), 2015), which addresses high-speed data communication considerations in chip and system interconnects — a topic encompassing serialization and deserialization techniques used to transfer data at high speeds between components. Additionally, my extensive work on High-Level Synthesis for FPGAs inherently involves the design of data communication interfaces, including serialized data paths, between hardware modules and between on-chip and off-chip components. My work on pin multiplexing — "Investigation and Optimization of Pin Multiplexing in High-Level Synthesis" (GLSVLSI, 2018) — directly relates to serialization techniques where multiple data signals are multiplexed over shared physical connections, a fundamental concept underlying serializer/deserializer architectures.

18. I am a Senior Member of IEEE (since 2010). I currently serve as an Associate Editor for IEEE Transactions on Computer-Aided Design (TCAD) and IEEE Transactions on Sustainable Computing. I have served as General Chair of the IEEE International Conference on Computer Design (ICCD) in 2025, TPC Chair of ICCD in 2024, and Track Chair for the ACM/IEEE Design Automation Conference (DAC), IEEE Design Automation and Test Europe (DATE), and ACM/IEEE Asia

and South Pacific Design Automation Conference (ASP-DAC). I have also served as an NSF reviewer on multiple occasions.

19. I hold two patents: U.S. Patent 8,977,996 B2, "Method and Apparatus for Incremental Design Space Exploration," and a corresponding Japanese Patent (JP 2012-522281).

20. My research has been supported by over $4 million in external funding from sources including the National Science Foundation (NSF), the Office of Naval Research (ONR), the Air Force Research Laboratory (AFRL/AFWERX), NATO, Boeing, Huawei, and Texas Instruments.

21. I have supervised 15 Ph.D. students and 20 Master's students to completion, many of whom have gone on to positions at leading semiconductor and technology companies including NVIDIA, Qualcomm, Apple, Cadence, Intel, AMD, and MathWorks.

22. Based on my education, research, publications, teaching, and professional experience spanning over two decades in the fields of reconfigurable computing, FPGA design and implementation, electronic design automation, clock architectures, frequency control, and high-speed data interconnects, I am qualified to offer expert opinions regarding the subject matter of the '865 patent, including its claims relating to serialization and deserialization, Field-Programmable Gate Arrays,

and clocks used in connection with FPGAs. My opinions in this declaration are based on my knowledge, training, education, and experience in these fields.

## II. SCOPE OF OPINIONS

23. I was asked to provide my opinions regarding whether the Challenged Claims of the ’865 patent would have been obvious to one of ordinary skill in the art at the time of the claimed invention for claims 1–18 and 21 by Giordano in view of Kaviani (Ground 1), claims 1–21 by Giordano in view of Kaviani in further view of Raymond (Ground 2), claims 1–18 and 21 by Giordano in view of Kaviani in further view of Virtex-UG (Ground 3), and claims 1–21 by Giordano in view of Kaviani, Virtex-UG, and Raymond (Ground 4).

24. This Declaration, including the exhibits cited herein, sets forth my opinions on these topics. It is my opinion that the Challenged Claims of the ’865 patent would have been obvious based on the Grounds listed above. I do not take a position on whether any of the claims are invalid under other aspects of patent law, such as indefiniteness or written description, and my analysis of the claims and opinions on validity are not intended to convey an opinion that the claims are not otherwise invalid.

## III. MATERIALS REVIEWED

25. The materials I considered and relied upon in preparing my Declaration and forming my opinions include all exhibits cited in this Declaration and the

Petition, including the ’865 patent, the file history of the ’865 patent, and the cited prior art.

26. I also relied on my professional experience, knowledge, and skill in computer architecture and VLSI design, as well as my experience with FPGAs and clocking techniques in reaching the opinions expressed in this Declaration.

## IV. PERSON OF ORDINARY SKILL IN THE ART

27. A person of ordinary skill in the art (“POSITA”) on February 21, 2019, would have a Bachelor’s degree in Computer Engineering, Electrical Engineering, or an equivalent discipline, and at least three years of academic or industry experience relating to clocking techniques for FPGAs with high-speed transceivers. Educational requirements may be substituted by greater relevant work experience, and vice versa.

## V. STATEMENT OF LEGAL PRINCIPLES

28. I am not an attorney. I am informed by attorneys of the relevant legal principles and have applied them to arrive at the opinions set forth in this declaration.

### A. Legal Standard for Prior Art

29. I understand that the petitioner for *inter partes* review may request the cancellation of one or more claims of a patent based on grounds available under AIA 35 U.S.C. § 102 and 35 U.S.C. § 103 using prior art that consists of patents and printed publications.

## B. Anticipation and Prior Art

30. I understand that § 102 specifies when a challenged claim is invalid for lacking novelty over the prior art, and that this concept is also known as "anticipation." I understand that a prior art reference anticipates a challenged claim, and thus renders it invalid by anticipation, if all elements of the challenged claim are disclosed in the prior art reference. I understand the disclosure in the prior art reference can be either explicit or inherent, meaning it is necessarily present or implied. I understand that the prior art reference does not have to use the same words as the challenged claim, but all of the requirements of the claim must be disclosed so that a person of ordinary skill in the art could make and use the claimed subject matter.

31. I also understand that § 102 defines what is available for use as a prior art reference to a challenged claim.

32. Under § 102(a)(1), a challenged claim is anticipated if it was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.

33. Under § 102(a)(2), a challenged claim is anticipated if it was described in an issued patent or published patent application, in which the patent or application names another inventor and was effectively filed before the effective filing date of the claimed invention.

34. I understand that the effective filing date of a patent or patent application is the earlier of the actual filing date of the patent or the application for patent or, if the patent or application for patent is entitled to claim earlier priority or the benefit of an earlier filing, the filing date of the earliest application that describes the claimed subject matter.

35. I understand that when a challenged claim covers several structures, either generically or as alternatives, the claim is deemed anticipated if any of the structures within the scope of the claim is found in the prior art reference.

36. I understand that when a challenged claim requires selection of an element from a list of alternatives, the prior art teaches the element if one of the alternatives is taught by the prior art.

### C. Legal Standard for Obviousness

37. I understand that even if a challenged claim is not anticipated, it is still invalid if the differences between the claimed subject matter and the prior art are such that the claimed subject matter would have been obvious to a person of ordinary skill in the pertinent art at the time of the claimed invention.

38. I understand that for a prior art reference to be proper for use in an obviousness analysis, the reference must be analogous art. I understand that a prior art reference is analogous art if: (1) the reference is from the same field of endeavor as the challenged patent (even if it addresses a different problem); or (2) the reference

is reasonably pertinent to the problem faced by the inventor of the challenged patent (even if it is not in the same field of endeavor). I understand that the field of endeavor is determined by reference to explanations of the challenged claims' subject matter in the challenged patent, including the embodiments, functions, and structures of the challenged claims. A prior art reference is "reasonably pertinent" to a problem if it would have logically commended itself to an inventor's attention in considering the problem.

39. I understand that obviousness must be determined with respect to the challenged claim as a whole.

40. I understand that one cannot rely on hindsight in deciding whether a claim is obvious.

41. I also understand an obviousness analysis includes the consideration of factors such as (1) the scope and content of the prior art, (2) the differences between the prior art and the challenged claim, (3) the level of ordinary skill in the pertinent art, and (4) "secondary" or "objective" evidence of non-obviousness.[1]

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[1] Secondary or objective evidence of non-obviousness includes evidence of: (1) a long felt but unmet need in the prior art that was satisfied by the claimed invention; (2) commercial success or the lack of commercial success of the claimed invention; (3) unexpected results achieved by the claimed invention; (4) praise of the claimed invention by others skilled in the art; (5) taking of licenses under the patent by others; (6) deliberate copying of the claimed invention; and (7) contemporaneous and independent invention by others. However, I understand that there must be a relationship between any secondary evidence of non-obviousness and the claimed invention.

42. I understand a challenged claim can be invalid for obviousness over a combination of prior art references if a reason existed (at the time of the claimed invention) that would have prompted a person of ordinary skill in the art to combine elements of the prior art in the manner required by the challenged claim. I understand that this requirement is also referred to as a "motivation to combine," "suggestion to combine," or "reason to combine," and that there are several rationales that meet this requirement.

43. I understand the prior art references themselves may provide a motivation to combine, but other times simple common sense can link two or more prior art references. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may come from market forces.

44. I understand obviousness to include, for instance, scenarios where known techniques are simply applied to other devices, systems, or processes to improve them in an expected or known way. I also understand that practical and common-sense considerations should be applied in a proper obviousness analysis. For instance, familiar items may have obvious uses beyond their primary purposes.

45. I understand combining familiar elements according to known methods is obvious when it yields predictable results. For instance, obviousness bars patentability of a predictable variation of a technique even if the technique originated

in another field of endeavor. This is because design incentives and other market forces can prompt variations of it, and predictable variations are not the product of innovation, but rather ordinary skill and common sense.

46. I understand a particular combination may be obvious if it was obvious to try the combination. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. This would result in something obvious because the result is the product not of innovation but of ordinary skill and common sense. However, I understand that it may not be obvious to try a combination when it involves unpredictable technologies.

47. I also understand a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

48. It is my understanding that the Manual of Patent Examining Procedure §2143 sets forth the following as exemplary rationales that support a conclusion of obviousness:

(A) Combining prior art elements according to known methods to yield predictable results;

(B) Simple substitution of one known element for another to obtain predictable results;

(C) Use of known technique to improve similar devices (methods, or products) in the same way;

(D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) "Obvious to try" – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;

(G) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

49. A person of ordinary skill in the art looking to overcome a problem will often use the teachings of multiple publications together. I understand that obviousness analysis considers inferences, creative steps, common sense, and

practical logic and applications that a person of ordinary skill in the art would employ under the circumstances.

50. I understand a claim can be obvious in light of a single reference, if the elements of the challenged claim that are not explicitly or inherently disclosed in the reference can be supplied by the common sense of one of skill in the art.

51. I understand obviousness also bars the patentability of applying known or obvious design choices to the prior art. One cannot patent merely substituting one prior art element for another if the substitution can be made with predictable results. Likewise, combining prior art techniques that are interoperable with respect to one another is generally obvious and not patentable.

52. For a claim to be found invalid based upon a modification or combination of the prior art, there must be reasonable expectation that a person of ordinary skill would have successfully modified or combined the prior art to arrive at the claimed arrangement. This does not mean that it must be certain that a person of ordinary skill would have been successful—the law only requires that the person of ordinary skill in the art would have perceived a reasonable expectation of success in modifying or combining the prior art to arrive at the claimed invention.

53. In sum, my understanding is obviousness invalidates claims merely reciting combinations or obvious variations of prior art teachings using understanding and knowledge of one of skill in the art at the time and motivated by

the general problem facing the inventor at the time. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of or attempting obvious variations on prior art references in the claimed manner.

### D. Legal Standard for Claim Construction

54. I understand that before any invalidity analysis can be properly performed, the scope and meaning of the challenged claims must be determined by claim construction.

55. I understand that a patent may include two types of claims, independent claims and dependent claims. I understand that an independent claim stands alone and includes only the limitations it recites. I understand that a dependent claim depends from an independent claim or another dependent claim. I understand that a dependent claim includes all the limitations that it recites in addition to the limitations recited in the claim (or claims) from which it depends.

56. In comparing the challenged claims to the prior art, I carefully considered the patent and its file history in light of the understanding of a person of skill at the time of the earliest filing of the applicant's claimed invention.

57. I understand that to determine how a person of ordinary skill would have understood a claim term, one should look to sources available at the time of the claimed invention that show what a person of skill in the art would have understood

disputed claim language to mean. It is my understanding that this may include what is called "intrinsic" evidence as well as "extrinsic" evidence.

58. I understand that, in construing a claim term, one should primarily rely on intrinsic patent evidence, which includes the words of the claims themselves, the remainder of the patent specification, and the file history. I understand that extrinsic evidence, which is evidence external to the patent and the file history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient. I understand that extrinsic evidence may include principles, concepts, terms, and other resources available to those of skill in the art at the time of the invention.

59. I understand words or terms should be given their ordinary and accepted meaning unless it appears that the inventor was using them to mean something else or something more specific.

60. I understand that to determine whether a term has special meaning, the claims, the patent specification, and the file history are particularly important, and may show that the inventor gave a term a particular definition or intentionally disclaimed, disavowed, or surrendered claim scope.

61. I understand the claims of a patent define the scope of the rights conferred by the patent. I understand that because the claims point out and distinctly claim the subject matter which the inventor regards as the invention, claim construction analysis must begin with and is focused on the claim language itself. I

understand that the context of the term within the claim as well as other claims of the patent can inform the meaning of a claim term. For example, because claim terms are normally used consistently throughout the patent, how a term is used in one claim can often inform the meaning of the same term in other claims. Differences among claims or claim terms can also be a useful guide in understanding the meaning of particular claim terms. I understand a claim term should be construed not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the entire specification. I understand that because the specification is a primary basis for construing the claims, a correct construction should align with the specification.

62. I understand the file history of the patent as well as art incorporated by reference or otherwise cited during the file history is also highly relevant in construing claim terms. For instance, art cited or incorporated by reference may indicate how the inventor and others of skill in the art at the time of the invention understood certain terms and concepts. Additionally, the file history may show that the inventor disclaimed or disavowed claim scope, or further explained the meaning of a claim term.

63. With regard to extrinsic evidence, I understand that all evidence external to the patent and file history, including expert and inventor testimony, dictionaries, and learned treatises, can also be considered. For example, technical

dictionaries may indicate how one of skill in the art used or understood the claim terms. However, I understand that extrinsic evidence is considered to be less reliable than intrinsic evidence, and for that reason is generally given less weight than intrinsic evidence.

64. I understand that in general, a term or phrase found in the introductory words or preamble of the claim, should be construed as a limitation if it recites essential structure or steps, or is necessary to give meaning to the claim.

## VI. SUMMARY OF THE '865 PATENT

65. The '865 patent concerns a "field programmable gate array" with an "external or internal phase controller providing phase matching between a receiver clock and a transmitter clock used in the field programmable gate array." Ex. 1001, 1:17–23. It acknowledges that FPGAs were already used for fast processing, including high-frequency trading, because they allow computations to occur on a single chip with "massive fine-grained parallelism." *Id.*, 1:27–32. The patent identifies the problem as synchronizing receiving-side and transmitting-side clock signals within the FPGA, and alleges that prior-art clock-domain-crossing circuits introduced undesirable processing delay. *Id.*, 1:33–42. To reduce that alleged latency, the patent states that an object of the invention is "phase matching receiver side and transmitter side clocks of a FPGA without introducing unnecessary delay in processing." *Id.*, 2:12–15.

### A. Challenged Claims

66. All of the claims of the ’865 patent are Challenged Claims (claims 1–21).

### B. File History of the ’865 Patent

67. The application for the ’865 patent was filed May 29, 2020. During prosecution, the Examiner did not issue an Office Action rejecting the claims. Instead, during a July 7, 2020 examiner-initiated interview, the Examiner identified potential provisional non-statutory double-patenting issues involving parent Application No. 16/670,702 and co-pending Application No. 16/672,076, and Applicant indicated that a terminal disclaimer would be filed. Ex. 1002, pdf p. 15 (7/16/2020 Examiner-Initiated Interview Summary, p. 1). After a terminal disclaimer, the Examiner then allowed the pending claims. Ex. 1002, pdf pp. 11–13 (7/16/2020 Notice of Allowance (Allowability), pp. 1–3).

68. The Examiner did not apply Giordano, Kaviani, Virtex-UG, or Raymond as the basis for any rejection, nor does the ’865 patent cite to these references. Ex. 1001, 1–2.

## VII. APPLICATION OF THE PRIOR ART TO THE CHALLENGED CLAIMS

### A. Priority Date

69. I have been instructed to assume the ’865 patent and the Challenged Claims have a priority date of February 21, 2019, through continuation application

No. 16/670,702, dating back to U.S. Provisional Application No. 62/808,404, which was filed on February 21, 2019. Ex. 1001, p. 1 at "Related U.S. Application Data." If the actual priority date should be different than February 21, 2019, I reserve the right to supplement my opinions based on that change in priority date, if necessary.

## B. Claim Construction

70. As I explained above, unless I specify otherwise, I applied the ordinary and customary meaning of the terms of the Challenged Claims as understood by a POSITA throughout my analysis in this Declaration.

## C. Overview of Prior Art

71. The below challenges are made in view of the following prior art references, none of which were cited or considered during prosecution of the '865 patent.

### 1. R. Giordano and A. Aloisio, *Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs*, 58-1 IEEE Transactions on Nuclear Science 194 (2011) ("Giordano") (Ex. 1005)

72. Giordano was published in IEEE Transactions on Nuclear Science on January 28, 2011. I reviewed the declarations of Carrie Gardner and Gordon MacPherson concerning the public availability of Giordano and understand that Giordano was publicly available before February 21, 2019. In my opinion, a POSITA working in FPGA-based high-speed serial communications, clock synchronization, and SerDes systems before February 21, 2019, would have looked

to publications, including those of IEEE, as a standard source of technical information. Giordano therefore qualified as prior art under AIA 35 U.S.C. §102(a)(1). Giordano was neither cited nor considered during prosecution of the '865 patent.

73. Giordano is a 2011 IEEE paper that explains timing synchronization and clock-distribution applications "would benefit from high-speed fixed-latency SerDeses." Ex. 1005, 194.

74. Giordano presents "a link architecture based on high-speed transceivers embedded in latest generation [FPGAs]" based on "the GTP transceiver" of the "Xilinx Virtex 5 FPGA family." Ex. 1005, 194. Giordano further explains that GTPs are available inside the FPGA as "configurable hard-macros (or 'tiles')," with each tile including a pair of transceivers (i.e., a receiver and a transmitter) that share components including a phase-locked loop. *Id*. Within each transceiver is the Physical Medium Attachment (PMA) sublayer for serializing (in transmitter PMA) and deserializing (in receiver PMA) data, and the Physical Coding Sublayer (PCS) for additional data processing before serialization (in transmitter PCS) and after deserialization (in receiver PCS). *Id.*

75. Giordano also describes an FPGA Fabric for programming circuit blocks as needed. In Giordano, circuit blocks such as "Comma Detect and Align" and DLLs are programmed in the FPGA Fabric. *Id.*, 197–199.

76. A block diagram of the GTP transceiver is shown in Figure 1 of Giordano:

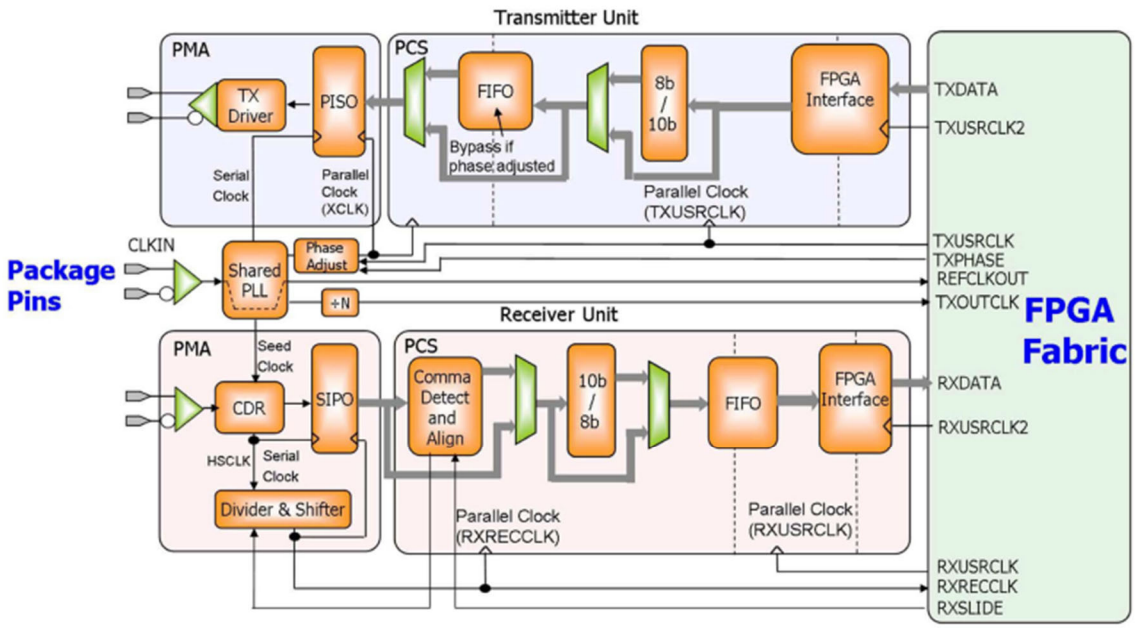



Fig. 1. Simplified block diagram of the GTP transceiver. Half a tile is shown.

### a) Ex. 1009, Virtex-UG (incorporated by Giordano)

77. Giordano presents a system with the "RocketIO" GTP transceiver of the Xilinx Virtex 5 FPGA family. Ex. 1005, 194, 199. Giordano repeatedly references the RocketIO GTP Transceiver, for example referencing the overall transceiver architecture (*id*., 195) and taking estimated latency values from the RocketIO GTP Transceiver User Guide (*id*., 198). Giordano further states that "the procedure we follow for activating the alignment circuit is the one suggested in the GTP user's guide." *Id*., 197. As such, Giordano inherently discloses the features of Virtex-UG (Ex. 1009), and further incorporates it by reference.

78. Virtex-UG is Xilinx's Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), dated December 3, 2009, and hence publicly available before Giordano. Ex. 1009, 1.

### 2. Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 ("Virtex-UG") (Ex. 1009)

79. Virtex-UG was published on December 3, 2009. Virtex-UG therefore qualified as prior art under AIA 35 U.S.C. §102(a)(1). Virtex-UG was neither cited nor considered during prosecution of the '865 patent.

80. Virtex-UG is Xilinx's Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), dated December 3, 2009, hence publicly available before Giordano. Ex. 1009, 1; Ex. 1004, ¶¶41–47. I reviewed the declaration of Carrie Gardner concerning the public availability of Virtex-UG and understand that Virtex-UG was publicly available before February 21, 2019. In my opinion, a POSITA working in FPGA-based high-speed serial communications, clock synchronization, and SerDes systems before February 21, 2019, would have looked to publications, including those of IEEE and Virtex-UG, as a standard source of technical information. Virtex-UG states that it "shows how to use the RocketIO™ GTP transceivers in Virtex®-5 FPGAs," and describes the GTP transceiver as a power-efficient, highly configurable transceiver "tightly integrated with the programmable logic resources of the FPGA." Ex. 1009, 17, 23. The GTP transceiver supports line rates from 100 Mb/s to 3.75 Gb/s, optional PCS features

such as 8B/10B encoding, comma alignment, channel bonding, and clock correction, and "fixed latency modes for minimized, deterministic datapath latency." *Id*., 23. The guide also explains that GTP transceivers are placed as dual-transceiver GTP_DUAL tiles in Virtex-5 LXT and SXT devices, allowing two transceivers to share a single PLL with the TX and RX functions of both, just how Giordano describes its use of the Virtex-5 FPGA. *Id*., 24; Ex. 1005, 194.

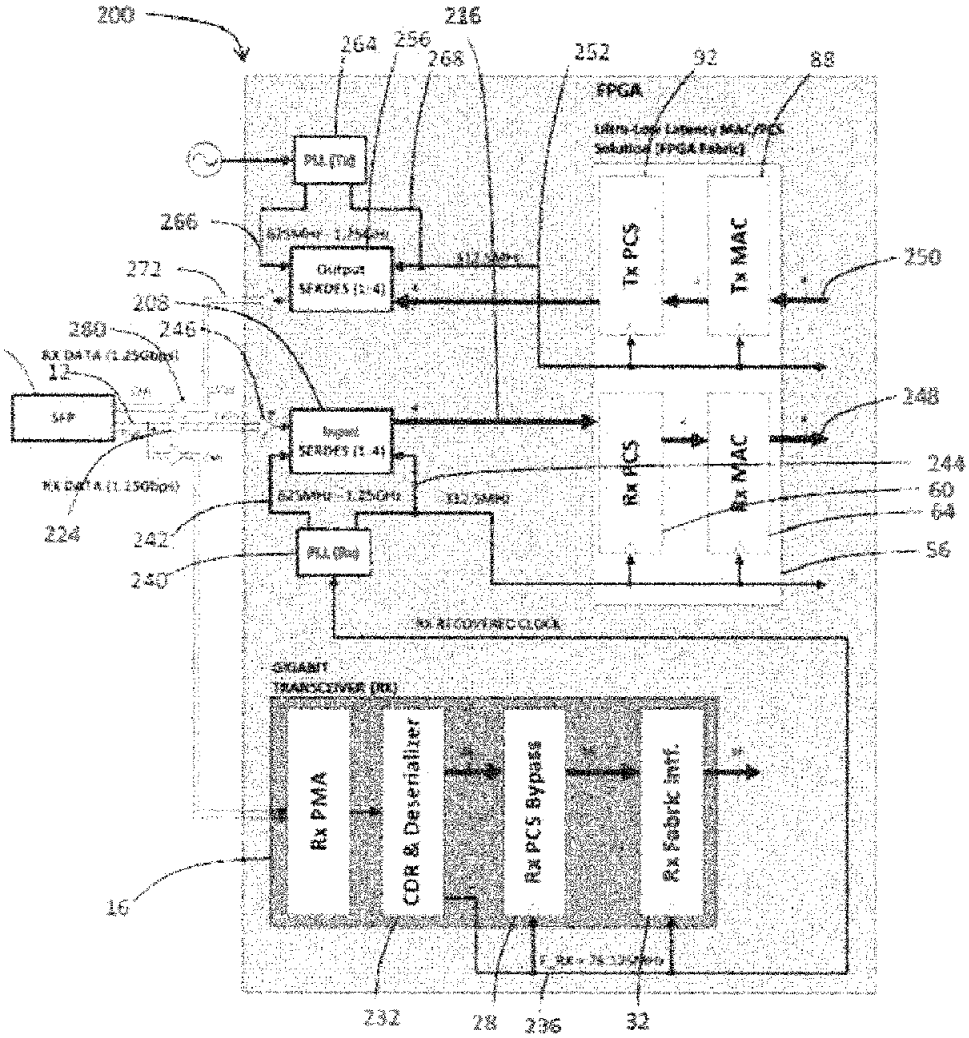
### 3. U.S. Pat. No. 10,447,463 ("Raymond") (Ex. 1007)

81. Raymond is titled "Device and Method for Ultra-low Latency Communication," claims priority to provisional application No. 62/531,965 filed on July 13, 2017. Raymond was filed on July 13, 2018, the application published on January 17, 2019, and granted on October 15, 2019. Raymond therefore qualifies as prior art under AIA 35 U.S.C. §102(a)(2). Raymond was neither cited nor considered during prosecution of the '865 patent.

82. Raymond (U.S. Patent No. 10,447,463) explains that "[u]ltra-low latency communication is critical" for applications depending on round-trip time, including "electronic trading," and that "some trading firms are now using FPGAs to improve throughput and latency performances of their trading equipment." Ex. 1007, 1:18–24. Raymond discusses "incoming signals" in "context of financial trading data," and exchanging such data with "financial exchange." *Id*., 4:52–59.Raymond discloses an "ultra-low latency communication device" that includes

"a clock recovery module, a de-serializer module, an FPGA fabric and a serializer module." *Id*., 1:42–44.

83. Raymond states that "prefabricated transceivers used to process incoming and outgoing physical layer signals" may be "replaced by low-latency serializer/de-serializer modules" that are programmed by the FPGA. *Id*., 4:43–47; *see also* 9:3–8 ("SerDes module" is "implemented using programmable logic"), 11:65–67. Raymond's proposed solution is depicted in Figure 2:



### 4. U.S. Pat. No. 7,453,301 ("Kaviani") (Ex. 1010)

84. Kaviani, titled "Method of and Circuit for Phase Shifting a Clock Signal," was filed August 5, 2005, and granted November 18, 2008. Kaviani therefore qualifies as prior art under AIA 35 U.S.C. §102(a)(1) and §102(a)(2). Kaviani was neither cited nor considered during prosecution of the '865 patent.

85. Kaviani (U.S. Pat. No. 7,453,301) explains that "DLLs in the Virtex or Spartan Field Programmable Gate Array (FPGA) product series from Xilinx" are clock-management systems used for "deskewing and phase shifting." Ex. 1010, 1:44–49. Kaviani explains that integrated circuits "such as a programmable logic device (PLD)" receive "external reference clock signals" to generate "internal clock signals," which "must be carefully controlled to ensure proper timing," and that it is "important" for generated clock signals to be "maintained accurately at the specified phase and frequency." *Id.*, 1:13–17, 1:34–38. Kaviani further discloses a control circuit that "generate[s] delay select values," provides "synchronization of the digital delay lines to avoid delay select set up and hold times." *Id.*, 4:8–4:11.

## VIII. STATE OF THE ART

86. As of the priority date of February 21, 2019, the state of the art in FPGA-based serial communication systems was highly developed. FPGAs had been commercially available for decades and were widely deployed in applications requiring high-speed data processing, including financial trading systems. Ex. 1001,

1:41-43 (FPGAs are used in the financial industry in high frequency trading where the rapid processing of the FPGA is desired). The fundamental building blocks at issue in this proceeding—serializers/deserializers (SERDES), phase-locked loops (PLLs), delay-locked loops (DLLs), clock and data recovery (CDR) circuits, and phase alignment mechanisms—were all well-understood, standardized components that had been available in commercial FPGA devices for many years prior to the priority date.

87. I am familiar with the body of technical literature and patent disclosures concerning FPGA clock synchronization, serialization/deserialization, and phase-locked loop architectures as they existed before the priority date. In my opinion, the techniques claimed in the '865 patent represent straightforward applications of well-known principles to standard FPGA hardware resources. Below, I describe the state of the art in each relevant technical area as of February 21, 2019.

### A. <u>Serialization and Deserialization (SERDES) in FPGAs</u>

88. By February 2019, high-speed serial transceivers with integrated SERDES functionality were a standard feature of commercial FPGAs. These transceivers converted serial data streams into parallel data for processing in the FPGA fabric, and parallel data from the FPGA fabric back into serial data streams for transmission. Xilinx's Virtex-5 FPGA, for example, included RocketIO GTP transceivers that implemented deserialization through a serial-in/parallel-out (SIPO)

block, and serialization through a parallel-in/serial-out (PISO) block and supporting data widths of 8, 10, 16, or 20 bits. Ex. 1009, 104. These transceivers operated at multi-gigabit rates, with Giordano demonstrating operation at 2.5 Gbps. Ex. 1005, 197.

89. The architecture of these transceivers was organized into well-defined sublayers. As Giordano explains, the Physical Medium Attachment (PMA) sublayer contained the Serial In to Parallel Output (SIPO) and Parallel input to Serial Output (PISO) blocks responsible for serialization and deserialization, while the Physical Coding Sublayer (PCS) handled data processing functions such as 8b/10b encoding and decoding. Ex. 1005, 194-95. The transceiver connected to the FPGA fabric through user-accessible clock and data interfaces, allowing the FPGA designer to process deserialized parallel data using custom logic. *Id.* Raymond similarly describes an ultra-low latency communication device architecture comprising "a clock recovery module, a de-serializer module, an FPGA fabric, and a serializer module." Ex. 1007, 1:42–44.

90. It was further known that SERDES modules could be implemented either as hardened (pre-fabricated) transceiver blocks within the FPGA or as soft logic within the programmable fabric itself. Raymond expressly teaches replacing "prefabricated transceivers with low-latency serializer/de-serializer modules," implemented "using programmable logic." Ex. 1007, 4:43–47, 9:3–8. Raymond

discloses that Xilinx UltraScale GTY transceivers support "internal data buses of 16, 20, 32, 40 or 64 bits" for interfacing between the serial link and the parallel processing domain. Ex. 1007, 6:5–8. These various port widths were standard options that a person of ordinary skill in the art would have routinely selected based on the desired line rate and processing requirements.

### B. Phase-Locked Loops (PLLs) and Delay-Locked Loops (DLLs) in FPGAs

91. Phase-locked loops and delay-locked loops were fundamental clock management resources available in FPGAs well before the priority date. PLLs and DLLs were used for frequency, synthesis, phase alignment, and deskewing of clock signals. Kaviani explains that integrated circuits "such as a programmable logic device (PLD)" receive "external reference clock signals" to generate "internal clock signals," which "must be carefully controlled to ensure proper timing," and that it is "important" for generated clock signals to be "maintained accurately at the specified phase and frequency." Ex. 1010, 1:13–17, 1:34–38. Kaviani discloses that "DLLs in the Virtex or Spartan Field Programmable Gate Array (FPGA) product series from Xilinx" are clock-management systems used for "deskewing and phase shifting." Ex. 1010, 1:44–49. Kaviani's circuit comprises a Clock Generator circuit 206, which includes a plurality of digital delay lines for generating phase-shifted clock signals, and a separate Control Circuit 202 that receives a reference clock signal (RefClk)

and an output clock signal (C0) and generates delay select values for the delay lines. Ex. 1010, 3:64–4:19, Fig. 2.

92. These clock management resources were integral components of the FPGA silicon. Kaviani's Control Circuit provides multiple functions for clock management, including a phase control function "for maintaining phase alignment for deskewing" and a frequency control function "for maintaining frequency alignment." Ex. 1010, 5:37–51. The Control Circuit runs at a single frequency independent of the clock generator circuit, and "provides synchronization of the digital delay lines to avoid delay select set up and hold times." Ex. 1010, 4:8–11. Kaviani further discloses an iterative locking process in which phase and frequency delay select values are adjusted until the output clock is aligned with the reference clock, including concepts of "frequency in window" and "phase in window." Ex. 1010, 5:24–35, 6:22–54. These were not novel mechanisms—they were standard, commercially available building blocks that a person of ordinary skill in the art would routinely employ.

### C. Clock Synchronization and Phase Alignment Between Receiver and Transmitter

93. A central challenge in high-speed FPGA transceiver design—one that was well-recognized and addressed in the prior art long before 2019—is synchronizing the clock domains of the receiver and transmitter paths to minimize latency. When data arrives at an FPGA's receiver, a clock and data recovery (CDR)

circuit extracts a recovered clock (often called RXRECCLK) from the incoming data stream. This recovered clock is phase-aligned to the incoming data but is independent of the transmitter's clock. If the receiver and transmitter clocks are not synchronized, a clock domain crossing (CDC) mechanism—typically implemented as an elastic buffer or FIFO—is required to safely transfer data between domains. Such CDC mechanisms introduce additional latency.

94. The prior art recognized this latency problem and provided solutions to eliminate or reduce clock domain crossing delays. Giordano describes the GTP transceiver architecture in which a PLL is shared between both the receiver and transmitter within the same tile. Ex. 1005, 194-95. Giordano implements phase alignment to bypass the TX FIFO buffer, eliminating clock domain crossing. Ex. 1005, 195, 197. By aligning the phase of the transmitter user clock (TXUSRCLK) with the internal parallel clock, Giordano eliminates the need for a TX elastic buffer that would otherwise introduce variable latency due to clock domain crossing. *Id.*

95. The Virtex-5 RocketIO GTP Transceiver User Guide documents these phase alignment procedures in detail. For the receive path, the RX phase alignment allows bypassing the RX elastic buffer, resulting in "SIPO parallel clock phase matching RXUSRCLK phase" and "[n]o phase difference between XCLK and RXUSRCLK." Ex. 1009, 180. Such receiver phase alignment and bypass of clock

domain crossing circuitry is depicted in Figure 7-22 of the GTP Transceiver User Guide as seen below:

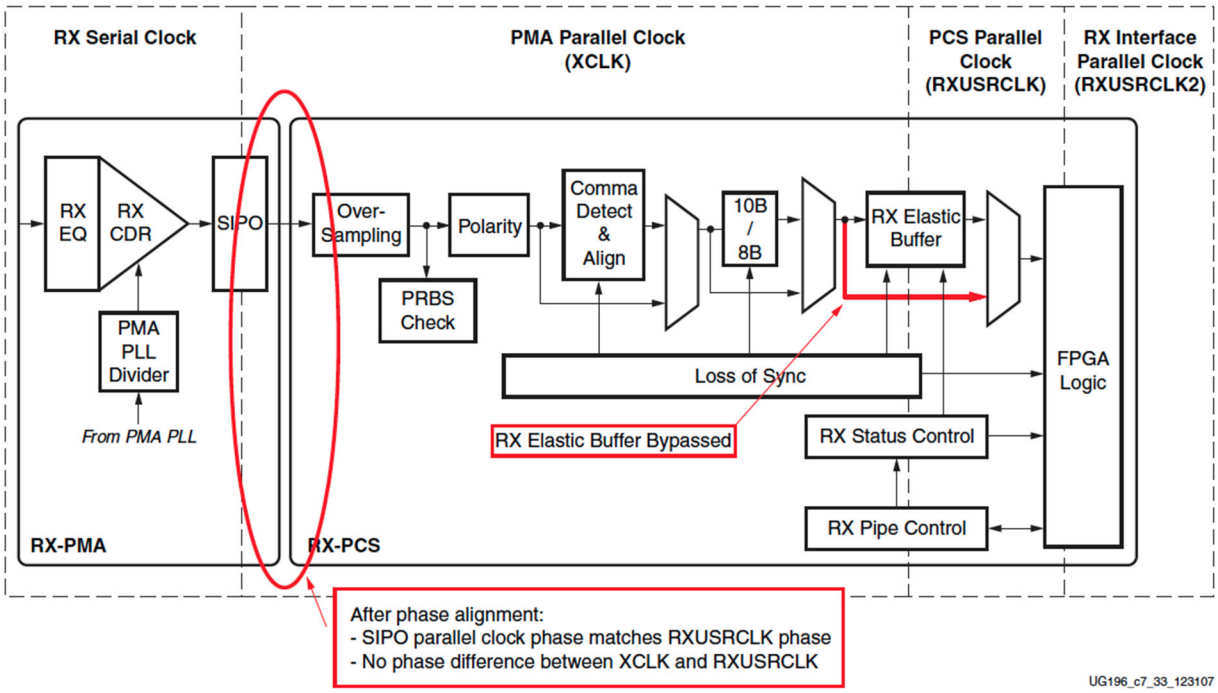



*Figure 7-22:* **Using Phase Alignment**

96. For the transmit path, TX phase alignment similarly allows bypassing the TX buffer. Ex. 1009, 121. These mechanisms were documented standard features of the hardware, available to any designer using these FPGAs.

97. Giordano further explains the relationship between the recovered receiver clock and the transmitter reference clock: "The clock recovered by the receiver cannot be directly used as a reference clock for the re-transmission. In fact, the internal PLL is shared among the transmitters and receivers in the same tile and at the receiver tile it is already locked to the seed clock. Moreover, the recovered clock might also require to be filtered in order to match the jitter specifications for

the GTP reference clock." Ex. 1005, 198. To address this, Giordano uses a DLL "external to the GTP" to multiply the reference clock frequency by 4, "thus providing TXUSRCLK." Ex. 1005, 197–198. This is precisely the type of clock conditioning that Kaviani's Clock Generator and Control Circuit are designed to perform.

98. Raymond addresses the same clock synchronization challenge in the context of ultra-low latency financial trading applications. Raymond discloses a receiving-side PLL that "up-converts the recovered clock signal" to provide transmitting driving clock signals. Ex. 1007, 9:52–66. Critically, Raymond teaches that the "receiving-side driving signals and transmitting-side driving signals have the same clock frequencies." Ex. 1007, 2:29–31. This frequency relationship between receiver and transmitter clocks is what enables data to pass between the receiver and transmitter paths without requiring an asynchronous FIFO or elastic buffer for clock domain crossing.

### D. <u>Application to Financial Trading Systems</u>

99. The application of FPGA-based low-latency serial communication to financial trading was well-established before the priority date. Raymond expressly teaches an "ultra-low latency communication" device for "electronic trading" applications. Ex. 1007, 1:18–24. Raymond describes processing "financial trading data" from the market exchange, and uses for "market data feed handler" and

"market data feed distribution systems." Ex. 1007, 4:52–59, 13:61–64. Raymond further describes that outgoing data is generated after "logical processing (e.g. applying financial trading algorithms)." Ex. 1007, 11:57–60.

100. As such, the motivation to minimize latency in financial trading systems was universally understood in the art. Every nanosecond of processing delay represents a competitive disadvantage in algorithmic trading. Accordingly, a person of ordinary skill in the art working on financial trading FPGA systems would have been strongly motivated to eliminate unnecessary sources of latency, including clock domain crossing delays introduced by elastic buffers and FIFOs. The prior art demonstrates that the technical means to accomplish this—phase alignment, PLL-based clock synthesis, and FIFO bypass—were all well-known and documented.

### E. Summary of State of the Art

101. In sum, the '865 patent disclosed and claims components and methods well known in the art at the time of its claimed invention. The '865 patent itself admits that FPGAs were already used "in the financial industry" for high-speed processing with "massive fine-grained parallelism," and acknowledges that prior-art synchronous Ethernet systems already employed internal PLLs to compare transmit and receive clocks. Ex. 1001, 1:27–32, 1:52–56. The technique of phase-matching FPGA receiver and transmitter clocks to avoid clock domain crossing delays was well-known and documented in the prior art. Ex. 1005, 195, 197; Ex. 1009, 121,

180; Ex. 1010, 3:64–4:19, 5:24–35. These were standard operating procedures and techniques for engineers working with these FPGAs. All of the components at issue—DLLs, PLLs, SERDES blocks, phase detectors, CDR circuits, digital delay lines, and elastic buffers—were standard building blocks available in commercial FPGA devices. Their implementation in FPGA fabric requires only programming existing silicon resources and configuring circuit board components according to well-documented procedures. Indeed, the challenged claims amount to nothing more than applying known clock management techniques—such as applying PLL-based clock synthesis, phase alignment, and FIFO bypass—to known hardware like Xilinx FPGAs with integrated transceivers to achieve the predictable result of low-latency data processing without clock domain crossing delays. A person of ordinary skill in the art would have combined these concepts using ordinary creativity with a reasonable expectation of success because the art was well aware of the same technical problems and used the same hardware platform contemplated by the ’865 patent.

## IX. DETAILED ANALYSIS OF INVALIDITY GROUNDS

102. I have analyzed all Challenged Claims of the ’865 patent, and it is my opinion that claims 1–18 and 21 are rendered obvious by Giordano in view of Kaviani (Ground 1), claims 1–21 are rendered obvious by Giordano in view of Kaviani in further view of Raymond (Ground 2), claims 1–18 and 21 are rendered

obvious by Giordano in view of Kaviani in further view of Virtex-UG (Ground 3), and claims 1–21 are rendered obvious by Giordano in view of Kaviani, Virtex-UG, and Raymond (Ground 4).

## A. Ground 1: Claims 1–18 and 21 Are Rendered Obvious By Giordano in view of Kaviani

### 1. Prior Art Overview

103. As discussed above in Sections VII.C and VIII, the prior art references Giordano and Kaviani and the state of the art at the time of the claimed invention help form my detailed analysis of Ground 1. I also provide the following descriptions below that further forms the basis of my analysis.

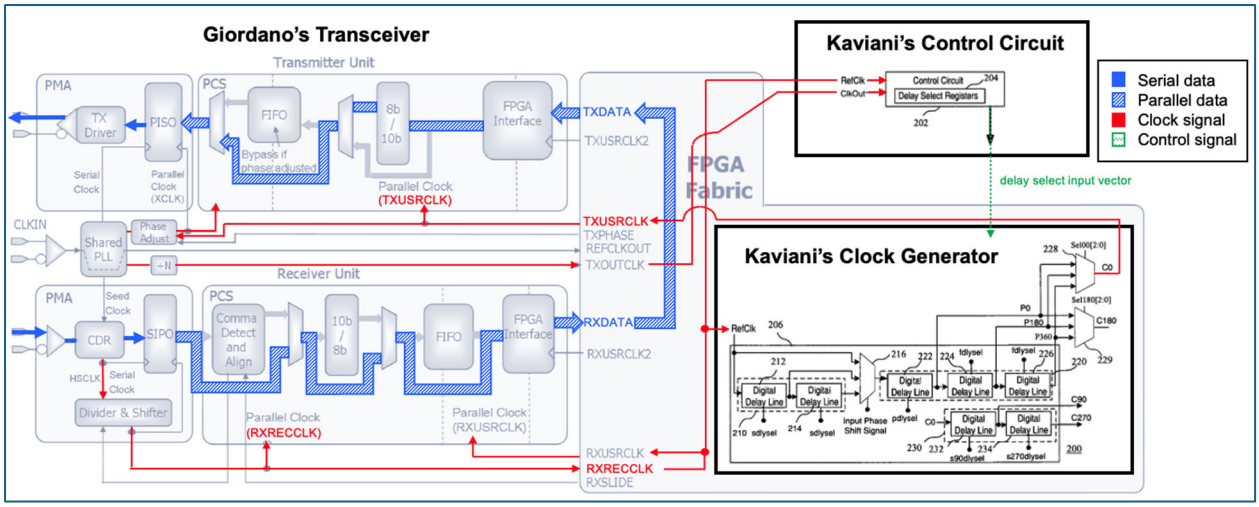
104. Giordano's FPGA system is comprised of two portions—Xilinx Virtex 5 FPGA "RocketIO" GTP transceiver (which has a receiver side and transmitter side) and the FPGA Fabric. Ex. 1005, 195. The GTP transceiver includes preprogrammed, fixed hardware components (such as dedicated pins and built-in analog circuits). *Id.*, 194; Ex. 1009, 50 (discussing the "analog nature of some blocks" within the GTP transceiver). These fixed components, commonly referred to as hard-macro tiles, cannot be modified or changed like FPGA programmable logic, but the user may still configure operating parameters and settings. *Id.*, 101 (noting that the FPGA logic may provide configuration data to the GTP transceiver). In contrast, the FPGA Fabric comprises programmable hardware that can be modified by the user. For example, Giordano discloses user-programmed hardware blocks such as "Comma

Detector and Aligner" off the GTP transceiver and on the FPGA Fabric. Ex. 1005, 198.

105. The mix of fixed and programmable hardware is common and well-understood in FPGAs. For example, Giordano designed and implemented a custom Comma Detector and Aligner in the programmable fabric because the GTP's built-in comma detector (which is a fixed block inside the GTP transceiver) only operates in certain modes, and not the mode in which Giordano was interested. Ex. 1005, 198. In addition, Giordano discloses implementing DLL blocks "external to the GTP" transceiver, i.e., on the FPGA Fabric. Ex. 1005, Fig. 5. The flexibility of the FPGA Fabric allows for customizing hardware as needed.

106. The proposed combination uses Giordano's Xilinx Virtex-5 GTP transceiver, FPGA Fabric, and FPGA circuit board, where the FPGA Fabric is programmed to implement Kaviani's Clock Generator and the circuit board is modified to include Kaviani's control circuit. Kaviani, a Xilinx patent, expressly discusses Xilinx Virtex FPGAs. Ex. 1010, 1:44–49. Given the shared Xilinx FPGA architecture, it is my opinion that a POSITA would have understood how to implement Kaviani's clock-alignment circuitry in Giordano's FPGA Fabric and related circuit boards.

107. The image below, based on Figure 1 of Giordano and Figure 2 of Kaviani with modifications, depicts this proposed combination:




108. Giordano's GTP transceiver generates a receiver side clock signal, RXRECCLK, from a clock extracted from incoming serial data. RXRECCLK is provided to Kaviani's Clock Generator on the FPGA Fabric, which creates a transmitter side clock signal TXUSRCLK. TXUSRCLK then goes to the transmitter PMA and related PLLs, resulting in TXOUTCLK. Kaviani's Control Circuit, implemented on the circuit board and off the FPGA, receives both RXRECCLK and TXOUTCLK to generate control signals and information to phase-match the two clock signals. TXUSRCLK, which is phase-matched to RXRECCLK, is sent to the transmitter.

### a) Motivation to Combine Giordano and Kaviani

109. The '865 patent sought to address the synchronization of receiving side and transmitting side clock signals within the FPGA. Ex. 1001, 1:32–35. Giordano and Kaviani demonstrate how a POSITA would have been motivated to combine the two references to address that problem.

110. It is my opinion that a POSITA would have been motivated to combine Giordano and Kaviani because they address synchronization and phase alignment of clock signals in FPGA transceivers. Giordano seeks fixed-latency timing synchronization and clock distribution in Xilinx Virtex-5 GTP transceivers, while Kaviani is a Xilinx patent concerning "phase shifting of a generated clock signal." Ex. 1005, 194; Ex. 1010, Abstract.

111. Giordano identifies the need that Kaviani's phase alignment teachings fulfill. While Giordano's fixed latency architecture achieves deterministic (i.e., fixed) phase relationships between the receiver clock and transmit clock, Giordano identifies gaps for directly using this receiver clock for the transmitter. Ex. 1005, 198. Giordano states:

> *The clock recovered by the receiver cannot be directly used as a reference clock for the re-transmission. In fact, the internal PLL is shared among the transmitters and receivers in the same tile and at the receiver tile it is already locked to the seed clock. Moreover, the recovered clock might also require to be filtered in order to match the jitter specifications for the GTP reference clock*

Ex. 1005, 198.

112. Giordano thus recognizes that jitter-filtering is beneficial to condition the recovered receiver clock to serve as a transmitter reference clock. Kaviani provides precisely such a solution through a phase shifting circuit that filters jitter and generates a transmit clock "phase aligned and frequency aligned with the reference clock signal." Ex. 1010, 1:36–43.

113. A POSITA reading Giordano would have naturally consulted Xilinx's own materials (such as Kaviani, a Xilinx patent), for a DLL-based phase alignment solution. Giordano uses a Xilinx Virtex FPGA, a chip that Kaviani mentions as well. Ex. 1005, 194, 197–199; Ex. 1010, 1:44–49.

114. It is my opinion that incorporating Kaviani's phase shifting teachings into Giordano would require routine programming of FPGA Fabric logic and conventional circuit element modifications.

115. Giordano itself demonstrates programming custom hardware in the FPGA Fabric, and further using elements on the circuit board as needed. For example, Giordano implemented a custom Comma Detector and Aligner in the FPGA Fabric because the GTP's built-in comma detector (which is a fixed block inside the transceiver) did not support the particular operations the user needed. Ex. 1005, 198. Giordano also discloses implementing DLL blocks "external to the GTP" transceiver, i.e., on the FPGA Fabric. Ex. 1005, Fig. 5. This DLL receives the REFCLKOUT from the receiver, and generates a phase-matched transmitter clock TXUSRCLK. Ex. 1005. Similarly, Giordano discusses configuring the circuit boards for experimental setups. Ex. 1005, 198. Implementing Kaviani's Clock Generator in the FPGA Fabric and Control Circuit in the circuit board thus represents a straightforward extension of techniques already used in Giordano.

116. In my opinion, such FPGA hardware programming is how the ’865 patent suggests implementing the claimed invention. In the ’865 patent, phase detector, phase controller, delay locked loop (DLL) components, and phase locked loop (PLL) are implemented in a “FPGA Core.” Ex. 1001, Figs. 3A–F, 4A–C, 5A–F. This FPGA Core includes logic elements, DSP blocks, clock distribution components, and memories, mirroring Giordano’s FPGA Fabric. Ex. 1001, 26:35–53. Thus, implementing Kaviani’s teachings in Giordano’s FPGA mirrors the ’865 patent’s own implementation approach.

117. In my opinion, a POSITA would have had a reasonable expectation of success. Giordano’s FPGA implementation was physically tested on Xilinx evaluation boards and used circuit blocks similar to those disclosed in Kaviani, including PLLs, DLLs, serializers, and pattern generators. Ex. 1005, 197–200. Giordano acknowledges the elements used for phase matching (such as DLL) are implemented on the FPGA Fabric, circuitry that can be programmed for whatever function the user desires. Ex. 1005, 195, 197. Because both references rely on the same Xilinx FPGA infrastructure, there would have been high expectation that, through routine FPGA programming, the combination functions as intended.

**b) Features of Virtex-UG are Inherent to Giordano, and Giordano Incorporates Virtex-UG by Reference**

118. Giordano presents a system with the "RocketIO" GTP transceiver of the Xilinx Virtex 5 FPGA family. Ex. 1005, 194, 199. Giordano repeatedly references the RocketIO GTP Transceiver, for example referencing the overall transceiver architecture (*id.*, 195) and taking estimated latency values from the RocketIO GTP Transceiver User Guide (*id.*, 198). Giordano further describes phase alignment of clock signals, and that "the procedure we follow for activating the alignment circuit is the one suggested in the GTP user's guide." *Id.*, 197. A POSITA would have known to reference Xilinx documents on the GTP transceiver to understand the relevant inherent features. As such, Giordano inherently discloses the features of Virtex-UG, and further incorporates Virtex-UG by reference. *Id*. In such a case, the features of the Virtex-UG are necessarily present in Giordano, and I have been informed by counsel that it is proper to use extrinsic evidence (such as the Virtex-UG) to understand said features. *See Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1328 (Fed. Cir. 2001) ("[R]ecourse to extrinsic evidence is proper to determine whether a feature, while not explicitly discussed, is necessarily present in a reference. The evidence must make clear that the missing feature is necessarily present, and that it would be so recognized by persons of ordinary skill in the relevant art."); *Sage Prods., LLC v. Stewart*, 133 F.4th 1376, 1385 (Fed. Cir.

2025) ("There was likewise nothing improper in the Board relying on evidence outside of the PAR to make findings as to what the skilled artisan would understand the PAR to be disclosing."); *Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1345 (Fed. Cir. 2018) ("It is well established that such reliance on extrinsic evidence is proper in an inherency analysis."); *see also In re Haines*, No. 2024-2338, 2025 WL 1403578, at *2 (Fed. Cir. May 15, 2025) (examiner properly used another publication "as evidence to explain why [the prior art's] disclosure of a mass spectrometer implicitly discloses 'obtaining mass spectral channel signals (m/z)'" (cleaned up)).

119. For the same reasons as above, Giordano incorporates Virtex-UG (Ex. 1009) by reference. Ex. 1005, 197 ("the procedure we follow for activating the alignment circuit is the one suggested in the GTP user's guide."). Virtex-UG, by incorporation, becomes part of the disclosures of Giordano. *Verizon Connect Inc. v. Omega Patents, LLC*, IPR2023-01162, 2024 WL 714951, at *3, 14-15 (P.T.A.B. Feb. 21, 2024) (the incorporated secondary reference's disclosures become part of the primary reference); *Paice LLC v. Ford Motor Co.*, 881 F.3d 894, 906-07 (Fed. Cir. 2018) ("[T]he standard of one reasonably skilled in the art should be used to determine whether the host document describes the material to be incorporated by reference with sufficient particularity.") (citing *Advanced Display Systems, Inc. v. Kent State University*, 212 F.3d 1272 (2000)).

## 2. Ground 1 - Analysis

### a) Independent Claim 1

**[1.pre]: "A method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of:"**

120. To the extent the preamble of claim [1] is limiting, Giordano discloses [1.pre]. It is my opinion that the terms "market data" and "entry data" are nothing more than recited purpose and use of the claimed invention. Indeed, they are not recited in other limitations in claim 1, supporting "market data" and "entry data." Thus, a POSITA would have understood that "market data" and "entry data" are not "essential" to the steps of this claim.

121. Further, the terms "market data" and "entry data" appear again only in later dependent claims [19] and [20]. If the preamble is limiting, the limitations of claims [19] and [20] are rendered superfluous, and fail to narrow claim [1]. A POSITA reading these claims would have understood that inclusion of "market data" and "entry data" in dependent claims, but not the body of the independent claim, further underscores that these terms in the preamble are non-essential statements of purpose, and are not limiting.

122. Giordano discloses an FPGA system, such as Xilinx Virtex 5, that includes a "serializer-deserializer (SerDes)." Ex. 1005, 194. And as such, Giordano

discloses a receiver that takes in serial data, and a transmitter that sends out post-processed serial data.

**[1.a]: "(a) receiving, by a first plurality of data pins of a first interface of a field programmable gate array in the field programmable gate array system, the first serial data stream;"**

123. It is my opinion that Giordano discloses this limitation.

124. Giordano discloses the GTP transceiver, which includes separate "Receiver Unit" and "Transmitter Unit." Ex. 1005, 194. Within each receiver- and transmitter-unit are a Physical Medium Attachment ("PMA") and Physical Coding Sublayer ("PCS"). *Id.*, 194–195. Giordano points to the PMA sublayer as the component "actually serializing and de-serializing the data," and the PCS layer as "processing" data. *Id.*, 194.

125. Giordano discloses package pins that interface the Receiver Unit PMA with external components, which disclose the claimed "first plurality of data pins" and "first interface." Ex. 1005, Fig. 1. This Receiver Unit PMA receives incoming serial data, which discloses the "first serial data stream." Ex. 1005, 195.

126. This mirrors the '865 patent, which describes a deserializer with a receiver PMA. Ex. 1001, 53:16–19, Fig. 6E.

**[1.b]: "(b) receiving, by a first reference clock pin in the first interface, a first clock signal having a first frequency and a first phase;"**

127. It is my opinion that Giordano discloses this limitation. As discussed in element [1.a], Giordano's Receiver Unit package pins disclose the claimed "first plurality of data pins" and "first interface."

128. Giordano's Receiver Unit PMA has a Clock and Data Recovery ("CDR") block, "which extracts a clock (HSCLK)" from the incoming serial data stream. Ex. 1005, 195. HSCLK discloses the "first clock signal," and also "first frequency and first phase." The package pin that receives this incoming serial data clock signal discloses "first reference clock pin."

129. This mirrors the '865 patent, which describes a receiver PMA further comprising a CDR block. Ex. 1001, 53:16–19, Fig. 6E. Like Giordano, the CDR block of the '865 patent receives serial data, and extracts a clock signal from the incoming serial data. Ex. 1001, 53:22–32.

**[1.c]: "(c) transmitting, from the first plurality of data pins of the first interface to a deserializer in the field programmable gate array, the first serial data stream;"**

130. It is my opinion that Giordano discloses this limitation.

131. Giordano's Receiver Unit PMA discloses the claimed "deserializer."

132. The Receiver Unit PMA includes a "Serial In to Parallel Output (SIPO)" block, which deserializes incoming serial data. Ex. 1005, 195–196. The package pins transmit the incoming serial data to the Receiver Unit PMA. Ex. 1005, 195.

133. This mirrors the ’865 patent, which describes a receiver PMA that receives serial data. Ex. 1001, 53:15–32, Fig. 6E.

**[1.d]: “(d) transmitting, from the first reference clock pin in the first interface to the deserializer, the first clock signal;”**

134. It is my opinion that Giordano discloses this limitation. As discussed in element [1.b], HSCLK discloses the claimed “first clock signal.”

135. Giordano’s Receiver Unit PMA has a Clock and Data Recovery (“CDR”) block, “which extracts a clock (HSCLK)” from the incoming serial data stream. Ex. 1005, 195. As such, HSCLK is sent with the serial data from the package pins to this CDR. *Id.*

136. This mirrors the ’865 patent, which describes a deserializer with a receiver PMA. Ex. 1001, 53:16–19, Fig. 6E. This receiver PMA further comprises a CDR block. *Id.* Like Giordano, the CDR block of the ’865 patent receives serial data, and extracts a clock signal from the incoming serial data. Ex. 1001, 53:22–32.

**[1.e]: “(e) generating, by the deserializer, a first receiver side clock signal having a second frequency and a second phase, based on the first clock signal;”**

137. It is my opinion that Giordano discloses this limitation. As discussed in element [1.c], Giordano’s Receiver Unit PMA discloses the claimed “deserializer.”

138. Giordano’s parallel recovered clock (RXRECCLK) discloses the “receiver side clock signal.” RXRECCLK discloses the “second frequency” and “second phase.”

139. The CDR in Giordano's Receiver Unit PMA extracts a clock (HSCLK) signal from the incoming serial data. Ex. 1005, 195. HSCLK is then used to "generate a parallel recovered clock (RXRECCLK)" for the SIPO block and Receiver Unit PCS. *Id.* This RXRECCLK discloses the claimed "receiver side clock signal," and the frequency and phase of RXRECCLK discloses the claimed second frequency and phase.

140. This mirrors the '865 patent, which describes a CDR that receives serial data, and generates clock signals for blocks such as Serial to Parallel and receiver PCS. Ex. 1001, 53:22–32, Fig. 6E.

**[1.f]: "(f) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;"**

141. It is my opinion that Giordano discloses this limitation. As discussed in elements [1.a] and [1.c], Giordano's Receiver Unit PMA discloses the claimed "deserializer," and the serial data into the PMA discloses the "first serial data stream."

142. Giordano's SIPO block output discloses the "first plurality of parallel data streams."

143. Giordano's Receiver Unit PMA has a SIPO block that converts incoming serial data to parallel data, which discloses this limitation. Ex. 1005, 195.

144. This mirrors the '865 patent, which describes a Serial to Parallel block within the Receiver PMA that "converts the serial data into parallel data, transmitting the parallel data to the receiver PCS." Ex. 1001, 53:28–32, Fig. 6E.

**[1.g]: "(g) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal;"**

145. It is my opinion that Giordano discloses this limitation. As discussed in elements [1.c] and [1.e], Giordano's Receiver Unit PMA discloses the claimed "deserializer," and its recovered clock signal RXRECCLK discloses "receiver side clock signal."

146. Giordano's Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS individually and collectively disclose the "computational circuitry in the [FPGA]."

147. Giordano points to PCS (both receiver and transmitter sides) as "processing" data, disclosing computational circuitry. Ex. 1005, 194. Giordano describes FPGA Fabric includes "logic," which discloses the claimed "computational circuitry in the [FPGA]." Ex. 1005, 195–196, 5. Giordano discloses providing RXRECCLK (i.e., "receiver side clock signal") to the Receiver Unit PCS and FPGA Fabric. Ex. 1005, 195.

148. This mirrors the '865 patent, with figures depicting computational circuitry capable of performing logical operation as "Computation Logic." Ex. 1001, Figs. 4B–C, 5A–F, cl. 5.

**[1.h]: "(h) transmitting, from the deserializer to the computational circuitry, the first plurality of data streams comprising a first plurality of data items and a first amount of data streams;"**

149. It is my opinion that Giordano discloses this limitation. As discussed in elements [1.c], [1.f], and [1.g], Giordano's Receiver Unit PMA discloses the claimed "deserializer," SIPO block output discloses the "first plurality of parallel data streams," and Giordano's Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS together disclose the "computational circuitry in the [FPGA]."

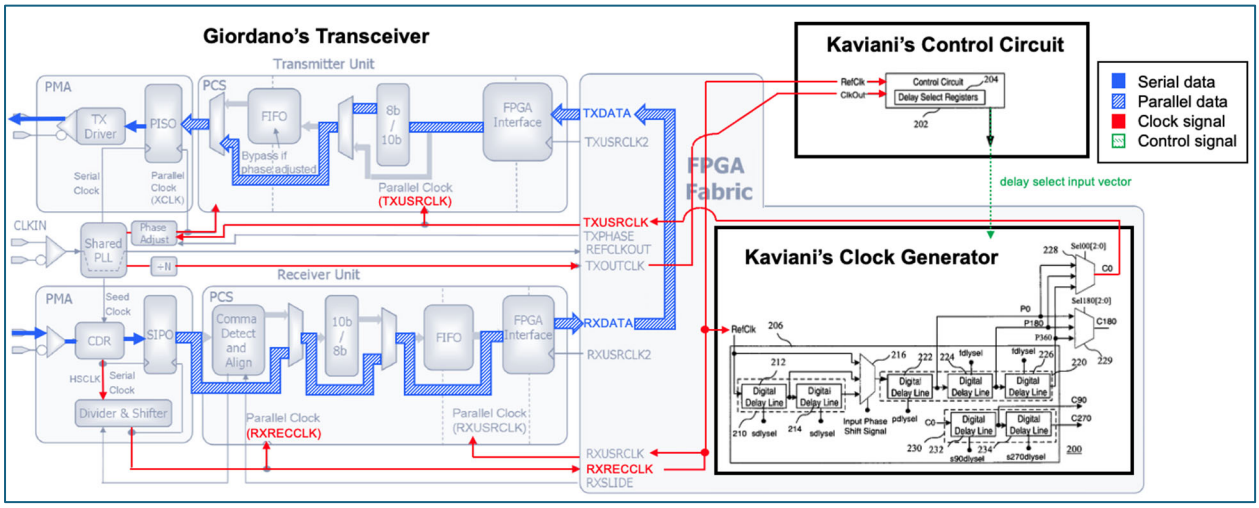
150. Giordano's SIPO block output, further processed by the Receiver Unit PCS, discloses the "first plurality of parallel data streams" (where the bit size of said parallel data discloses "first amount of data streams" and data transferred using this format discloses "first plurality of data items"). Ex. 1005, 195, Fig. 1.

**[1.i]: "(i) transmitting, from the deserializer via a first clock output pin on a second interface of the field programmable gate array to a phase detector that is part of the field programmable gate array system and not part of the field programmable gate array, the first receiver side clock signal;"**

151. It is my opinion that Giordano in view of Kaviani renders obvious this limitation. As discussed in elements [1.c] and [1.e], Giordano's Receiver Unit PMA discloses the claimed "deserializer," and its recovered clock signal RXRECCLK discloses "receiver side clock signal."

152. Kaviani's Control Circuit discloses this limitation. The connection between the FPGA and said Control Circuit discloses the claimed "second interface," and the connection specific for Kaviani's RefClk input to the Control Circuit

discloses the "first clock output pin." Kaviani's Control Circuit 202, which is a separate circuit from the FPGA, discloses the claimed "phase detector." The combination is depicted below:




153. Giordano discloses providing RXRECCLK (i.e., "receiver side clock signal") to the off-FPGA Control Circuit. Ex. 1005, 195; Ex. 1010, Fig. 2.

154. Kaviani discloses Control Circuit 202 and Clock Generator Circuit 206 as separate circuits, implementable in different physical regions. Ex. 1010, Fig. 2. As such, in light of Giordano's teachings, it is my opinion that a POSITA would have known to implement the Clock Generator on the FPGA Fabric, and the Control Circuit off the FPGA chip but still on the circuit board (e.g., FPGA system). Section IX.A.1.

**[1.j]: "(j) generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing the following steps until a first output of the phase detector is below a first threshold level:"**

155. It is my opinion that Giordano in view of Kaviani renders obvious this limitation. As discussed in element [1.i], Kaviani's Control Circuit discloses the claimed "phase detector."

156. The output of the combined clock generator results in a "first transmitter side clock signal" TXUSRCLK. This TXUSRCLK discloses the "third frequency" and the "third phase." Kaviani's Control Circuit output, that contains control signals for Kaviani's delay lines (sdlysel, pdlhysel, and fdlysel; or shift delay vectors) and MUXs (Input Phase Shift Signal and Sel00[2:0], or delay select input vectors), discloses the claimed "first output." Kaviani's phase in window concept discloses the claimed repetitive steps.

157. In the proposed combination, the FPGA Fabric creates a clock path from RXRECCLK (i.e., "receiver side clock signal") to TXUSRCLK (i.e., "transmitter side clock signal"), with Kaviani's Control Circuit 202 and Clock Generator Circuit 206 between the two clocks. Ex. 1010, 3:64–4:19. The result is a transmitter-side clock phase matched to the receiver-side clock. Ex. 1005, 198.

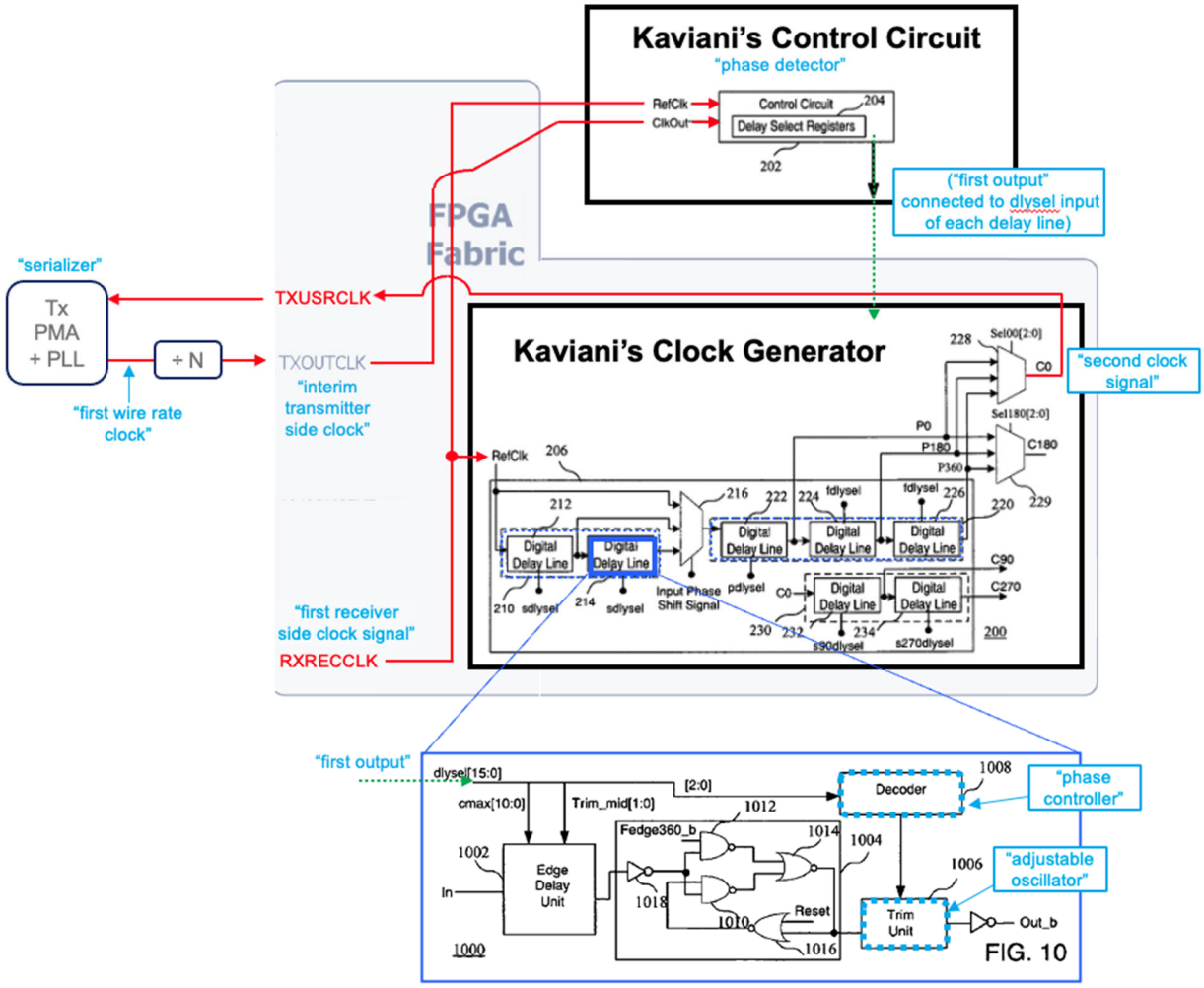
158. Kaviani discloses concepts of "frequency in window" and "phase in window." Ex. 1010, 6:22–54; Fig. 5–6. Phase in window is the time taken for the phase to match that of a target level, where such matching discloses "below a first

threshold level." *Id.* Kaviani discloses a signal phase_inwindow that transitions to logic high once phase matching happens. Ex. 1010, Fig. 5–6. Phase adjustments continue iteratively using the phase detected by the Control Circuit 202, for example following the sequence disclosed in Kaviani Fig. 4. *Id.*, 6:15–22 ("phase align signal P is increased until before a phase match is detected."). This iterative process in Kaviani discloses the claimed repetitive steps of this limitation.

**[1.k]: steps (i) through (viii)**

159. It is my opinion that Giordano in view of Kaviani renders obvious the claimed steps.

160. For ease of discussion, the claimed "steps" (i) through (viii) are discussed together, per the image below based on Giordano Figure 1 and Kaviani's Figures 2 and 10:




**<u>"(i) generating, by an adjustable oscillator in the field programmable gate array system, a second clock signal having a fourth frequency and a fourth phase;"</u>**

161. Kaviani's sets of delay lines (212, 214, 222, 224, 226) each have internal components that cause phase delays, for example, Trim Unit 1006, which renders obvious the claimed "adjustable oscillator." Ex. 1010, Figs. 2, 10. The Clock Generator output (C0) discloses the "second clock signal" (including fourth frequency and phase). Ex. 1010, Fig. 2.

162. Kaviani discloses using multiple digital delay lines to generate signals with different amount of added phase delays, where each delay line is controlled by a shift delay vector (such as sdlysel). Ex. 1010, 4:25–40. Within each delay line are trim units that "provides a fine grain delay adjustment to the combined clock signal," which are controlled by decoders. *Id.*, 9:46–10:28. These trim units render obvious the claimed "adjustable oscillator."

163. This mirrors the '865 patent, which notes that "the adjustable oscillator [] may be implemented with a digital delay line." Ex. 1001, 38:62–64.

**"(ii) generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal;"**

164. Giordano's Shared PLL output, which goes through a divider (depicted with "÷ N") to become TXOUTCLK, discloses the "first wire rate clock signal" (including fifth frequency and phase). Ex. 1005, Fig. 1.

165. Giordano's Shared PLL generates a signal, based on TXUSRCLK, that is provided to a divider. Ex. 1005, Fig. 1. The output of this divider becomes TXOUTCLK. Ex. 1005, Fig. 1.

166. This mirrors the '865 patent, which describes a divider for adjusting the frequency of a clock signal. Ex. 1001, 29:18–21, 51:63–52:8. Like Giordano, this divider outputs a "lower-frequency" signal, from dividing the input signal by a user-settable number. Ex. 1001, 52:31–41.

**"(iii) generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase;"**

167. Giordano's Transmitter Unit PMA with the Shared PLL discloses the claimed "serializer," and TXOUTCLK discloses "interim transmitter side clock signal" (including sixth frequency and phase).

168. Giordano discloses Shared PLL generating TXOUTCLK. Ex. 1005, 195 (Shared PLL "provides a parallel clock output (TXOUTCLK)").

**"(iv) transmitting, from the serializer via a second clock output pin of the second interface to the phase detector, the interim transmitter side clock signal;"**

169. As discussed in element [1.i], Kaviani's Control Circuit discloses the claimed "phase detector," and the connection between Giordano's FPGA and Kaviani's Control Circuit discloses the claimed "second interface."

170. Giordano discloses sending TXOUTCLK ("interim transmitter side clock signal") from Shared PLL to the FPGA Fabric. Ex. 1005, 195. In the proposed combination, FPGA Fabric sends TXOUTCLK to Kaviani's Control Circuit. Ex. 1010, Fig. 2. This connection to Kaviani's Control Circuit discloses the "second clock output pin."

**<u>"(v) generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal;"</u>**

171. As discussed in elements [1.e], [1.i], [1.j], and [1.k.iii], Giordano's RXRECCLK discloses the "receiver side clock signal," TXOUTCLK discloses the "interim transmitter side clock signal," and Kaviani's Control Circuit discloses the claimed "phase detector" and its output "first output."

172. Kaviani's Control Circuit discloses this limitation.

173. Kaviani discloses the Control Circuit 202 generating shift delay vectors (e.g., sdlysel, pdlhysel, fdlysel) and delay select input vectors (e.g., Input Phase Shift Signal, Sel00[2:0]). Ex. 1010, 3:64–4:28. The various functions of Control Circuit 202 is further described in Kaviani Figure 3:

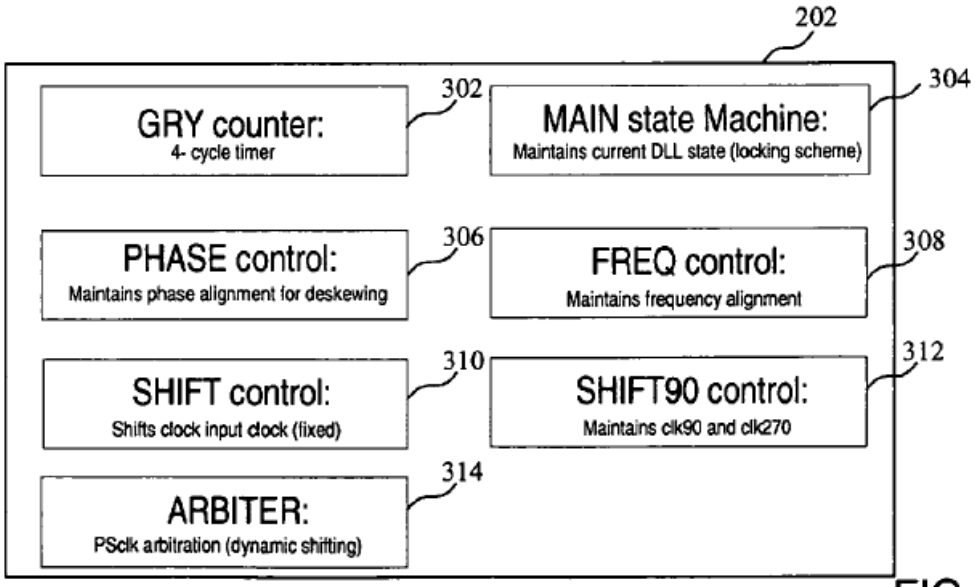



FIG. 3

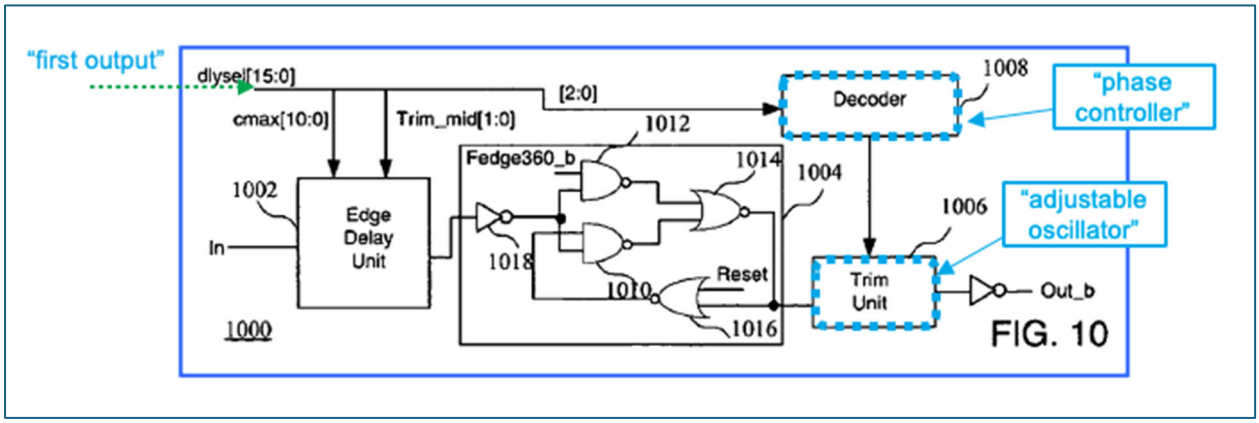
174. Kaviani's PHASE control 306 generates signals "for maintaining phase alignment for deskewing," and FREQ control 308 "for maintaining frequency alignment." *Id.*, 5:37–51. Kaviani discloses generating such control signals based on comparison of the two incoming clock signals, which in the proposed combination are RXRECCLK ("receiver side clock signal") and TXOUTCLK ("interim transmitter side clock signal").

**"(vi) transmitting, from the phase detector to a phase controller of the field programmable gate array system which is placed within the field programmable gate array, the first output;"**

175. As discussed in elements [1.i] and [1.j], Kaviani's Control Circuit discloses the claimed "phase detector," and its output shift delay vectors render obvious the "first output."

176. Kaviani renders obvious this limitation.

177. The decoder in Kaviani's Digital Delay Line, which is implemented on Giordano's FPGA Fabric, renders obvious the claimed "phase controller." Annotated Kaviani Figure 10 illustrates this mapping:



178. Kaviani discloses Control Circuit 202 generating shift delay vectors (e.g., sdlysel, pdlhysel, fdlysel), which are then provided to appropriate Digital Delay Lines. Ex. 1010, 3:64–4:28. Within the delay line, a decoder receives the incoming shift delay vector.

**"(vii) determining, by the phase controller, interim adjustment information based on the first output; and"**

179. As discussed in element [1.k.vi], Kaviani's decoder renders obvious the claimed "phase controller."

180. This decoder receives incoming delay vectors and controls the trim unit for "fine grain delay adjustment." Ex. 1010, 9:46–10:3. The decoder's control signal to the trim unit discloses the claimed "interim adjustment information."

**"(viii) transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information,**

181. As discussed in elements [1.k.i] and [1.k.vi], Kaviani's trim unit renders obvious the claimed "adjustable oscillator" and decoder renders obvious "phase controller."

182. This decoder receives incoming delay vectors and controls the trim unit for "fine grain delay adjustment." Ex. 1010, 9:46–10:3. The decoder's control signal to the trim unit discloses the claimed "interim adjustment information."

**wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information and steps (i) through (viii) are repeated until the first output of the phase detector is below the first threshold level;"**

183. Giordano in view of Kaviani renders obvious this limitation.

184. In the proposed combination, Kaviani's Control Circuit takes in RXRECCLK ("first receiver side clock signal") and TXOUTCLK ("interim transmitter side clock signal"). Based on the comparison of the two signals, Kaviani's Control Circuit determines the "correct amount of shifting required by all the delay lines" so the Clock Generator output is phase-matched to the reference clock signal. Ex. 1010, 5:24–35. Kaviani refers to this determination as "locking process." *Id.* The Control Circuit also maintains the correct shifting after lock, maintaining the phase-matching between the two clock signals. *Id.*, 5:35–37.

185. Kaviani Figure 4 discloses this iterative process for "locking" the output clock to the reference clock:

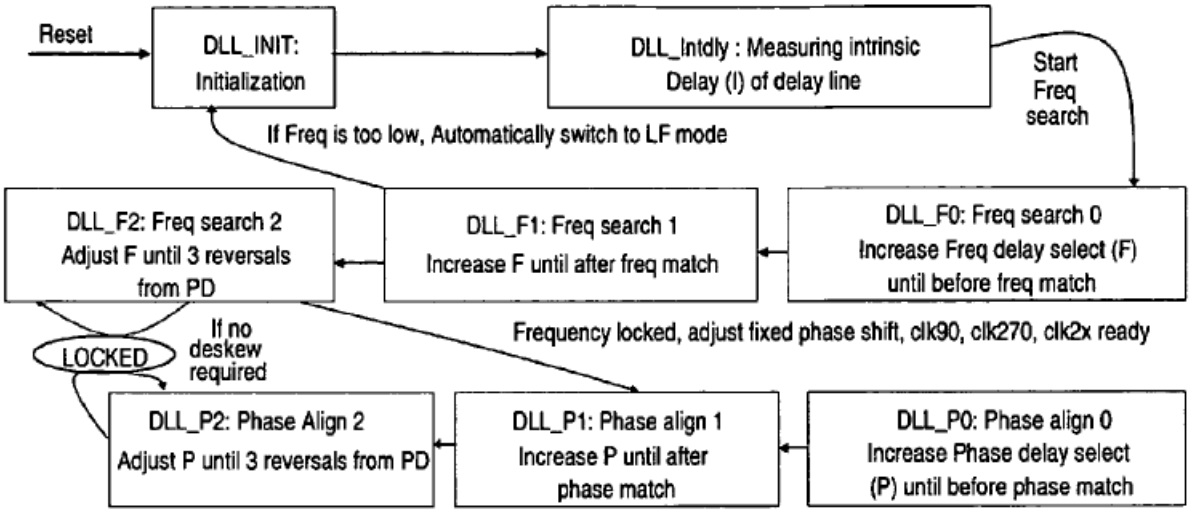



FIG. 4

**[1.l]: "(k) transmitting, from the serializer to the computational circuitry, first transmitter side clock signal;"**

186. It is my opinion that Giordano discloses this limitation. As discussed in elements [1.g], [1.j], and [1.k.iii], Giordano's Transmitter Unit PMA with the Shared PLL discloses the claimed "serializer," Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS together disclose the "computational circuitry," and TXUSRCLK discloses the "first transmitter side clock signal."

187. Giordano discloses the Shared PLL providing clock signals to the Transmitter Unit PCS, namely the XCLK signal. Ex. 1005, Fig. 1. Giordano discloses that "[i]n some configurations XCLK and TXUSRCLK have the same frequency and a constant phase offset," where for "sufficiently small" phase offset the two are treated the same, and clock domain crossing between XCLK and TXUSRCLK is bypassed. Ex. 1005, 195. Giordano's provision of XCLK from the Shared PLL to the Transmitter Unit PCS, and disclosure of treating XCLK the same as TXUSRCLK, renders obvious this limitation.

**[1.m]: "(l) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams, wherein the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams;"[2]**

188. It is my opinion that Giordano discloses this limitation. As discussed in elements [1.f] and [1.g], Giordano's SIPO block output discloses the "first plurality of parallel data streams" and PCSs / FPGA Fabric discloses the "computational circuitry." The term "the first ***set*** of parallel data streams" lacks antecedent basis in claim [1], and so I am reading this to refer to the "first ***plurality*** of parallel data streams" discussed in [1.f].

189. Giordano's processed parallel data exiting the Transmitter Unit PCS into the PMA discloses the "second plurality of parallel data streams" (where the bit size of said parallel data discloses "second amount of data streams"). Ex. 1005, Fig. 1.

190. Regarding "first set of operations," Giordano describes an FPGA Fabric that includes "logic," which discloses this limitation. Ex. 1005, 195–196, 198. Giordano describes programming a Comma Detector and Aligner in the FPGA Fabric, which performs "comma detection." Ex. 1005, 198. Giordano's "comma

[2] The term "the first set of parallel data streams" lacks antecedent basis. For the purpose of this IPR, I have been instructed to presume this as a term introduced in claim [1.f] and hence should be understood as "the first ***plurality*** of parallel data streams."

detector looks for commas (e.g., the one included in the K28.5 symbol) and when it finds one it determines how many bit shifts" are "required in order to align the parallel data." Ex. 1005, 198. A POSITA would have understood this pattern matching operation (to locate comma characters) and computing number of bit shifts for alignment to disclose the claimed "first set of operations."

191. In addition, Giordano points to the PCS layer (both receiver and transmitter sides) as "processing" data, rendering obvious computational circuitry. Ex. 1005, 194. The PCS layer includes 8b/10b encoding / decoding functions, which requires arithmetic calculations hence rendering obvious "first set of operations." Ex. 1005, 197.

192. As to "not include clock domain crossing operations," Giordano renders obvious this requirement.

193. Giordano discloses bypassing First In First Out (FIFO) buffer, a circuit block allowing safe data transfer between different clock domains (e.g., "data transfers between TXUSRCLK domain and the XCLK domain"). Ex. 1005, 195. A POSITA would have understood FIFO as a clock domain crossing circuit, and Giordano's bypassing of the FIFO block renders obvious this limitation.

194. Giordano discloses bypassing FIFO buffer by having the two clock domains have "the same phase" and "therefore also the same latency for the data." Ex. 1005, 195. In the transmitter, Giordano discusses two clocks (XCLK and

TXUSRCLK) that are adjusted to have the same frequency and phase. Ex. 1005, 195. The transmitter has a FIFO block for crossing between XCLK and TXUSRCLK clock domains. *Id.* Giordano discloses bypassing this FIFO block by using a phase alignment option provided in Xilinx Virtex-5 FPGA systems. Ex. 1005, 195. Through this built-in phase alignment, XCLK and TXUSRCLK are phase aligned, in which "the transmit FIFO is unnecessary and therefore we bypassed it." Ex. 1005, 197.

195. **Virtex-UG further discloses this limitation**. It is also my opinion that Virtex-UG, which Giordano incorporates by reference, discloses this limitation. The Virtex-UG's disclosures are express and also inherent.

196. In the receiver, Virtex-UG, which Giordano discloses and incorporates by reference, confirms this FIFO bypass. When receiver clock phase alignment is used, "RXUSRCLK must be driven directly from RXRECCLK using a BUFR regional clock buffer." Ex. 1009, 179 ("Using RX Phase Alignment to Bypass the RX Elastic Buffer"). Due to phase alignment, "SIPO parallel clock phase matches RXUSRCLK phase" and there is "no phase difference between XCLK and RXUSRCLK." *Id.*, 180. With no phase difference, the RX Elastic Buffer (which is the FIFO block described in Giordano) is bypassed. This bypass is described in the red arrow below in Figure 7-22 of Virtex-UG:

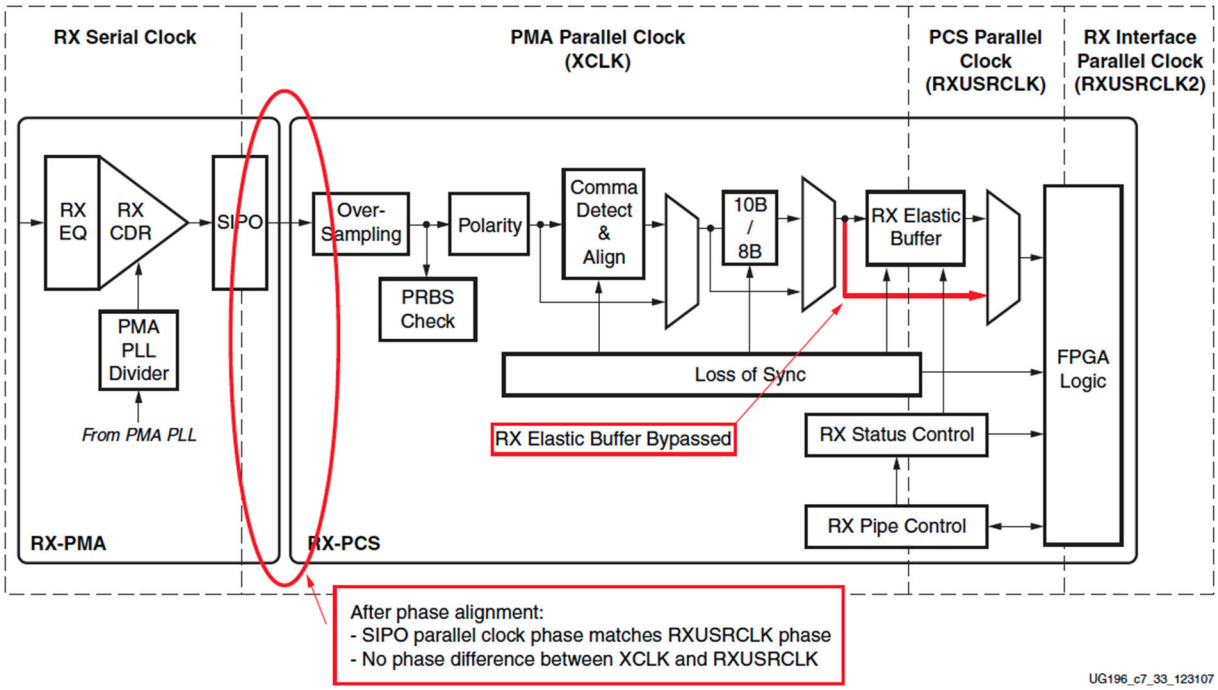



*Figure 7-22:* **Using Phase Alignment**

197. The bypass of all clock domain crossing circuits after phase alignment of clock signals, as disclosed in Giordano, renders obvious this limitation.

**<u>[1.n]: "(m) transmitting, from the computational circuitry to the serializer, the second plurality of parallel data streams;"</u>**

198. It is my opinion that Giordano discloses this limitation.

199. As discussed in elements [1.g], [1.k.iii], and [1.m], Giordano's Transmitter Unit PMA with the Shared PLL discloses the claimed "serializer," Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS together disclose the "computational circuitry," and Giordano's processed parallel data exiting the Transmitter Unit PCS into the PMA discloses the "second plurality of parallel data streams."

200. Giordano discloses transmitting parallel data from the Transmitter Unit PCS into the PISO block of the Transmitter Unit PMA, disclosing this limitation. Ex. 1005, Fig. 1.

**[1.o]: "(n) converting, by the serializer, the second plurality of parallel data streams into the second serial data stream; and"**

201. It is my opinion that Giordano discloses this limitation. As discussed in element [1.m], Giordano's PISO block input discloses the "second plurality of parallel data streams."

202. Giordano's Transmitter Unit PMA discloses the claimed "serializer." Ex. 1005, 195–196. The Transmitter PMA includes a Parallel Input to Serial Output ("PISO") block that converts parallel data to serial data. Ex. 1005, 195. The serial data output of PISO discloses the "second serial data stream."

203. This mirrors the '865 patent, which describes a serializer with a transmitter PMA with a Parallel to Serial block. Ex. 1001, 53:60–54:13, Fig. 7B. Like Giordano, this Parallel to Serial block converts the incoming parallel data to serial data. *Id.*

**[1.p]: "(o) transmitting, from the serializer off the field gate programmable array system via a second plurality of data pins of the first interface, the second serial data stream."**

204. It is my opinion that Giordano discloses this limitation.

205. As discussed in elements [1.k.iii] and [1.o], Giordano's Transmitter Unit PMA with the Shared PLL discloses the claimed "serializer," where the output of the PISO block discloses the "second serial data stream."

206. The Transmitter Unit PMA in Giordano has a TX Driver that sends out serial data, which discloses this limitation. Ex. 1005, 195. Giordano discloses package pins that interface the Transmitter Unit PMA with external components, which disclose the claimed "second plurality of data pins." Ex. 1005, Fig. 1. This Transmitter Unit PMA transmits processed serial data, i.e., "second serial data stream." Ex. 1005, 195.

207. This mirrors the '865 patent, which describe a Transmitter PMA with a Transmitter Buffer that sends out serial data. Ex. 1001, 53:60–54:13, Fig. 7B.

**b) Claims 2–4**

208. Claims 2–4 concern the relationship between "first clock signal" (with "first frequency" and "first phase") and "first transmitter side clock signal" (with "third frequency" and "third phase"). It is my opinion that Giordano in view of Kaviani renders obvious these claims.

209. As discussed in elements [1.b] and [1.j], HSCLK discloses the "first clock signal" and TXUSRCLK discloses the "first transmitter side clock signal." As discussed in element [1.k], TXUSRCLK is phase-matched with RXRECCLK (which discloses the "first receiver side clock signal").

**[2] "The method of claim 1, wherein the third frequency corresponds to the first frequency."**

**[3]: "The method of claim 2, wherein the third phase is not aligned with the first phase."**

**[4]: "The method of claim 1, wherein the third frequency is different than the first frequency."**

210. It is my opinion that Giordano discloses claims 2–4.

211. Giordano discloses that in the Receiver Unit PMA, "HSCLK is divided down by 5 and then fed in a 5-bit shift-register," which then becomes RXRECCLK. Ex. 1005, 196, Fig. 3. Using signal RXSLIDE from the FPGA Fabric, this 5-bit shift-register selects the phase shift of RXRECCLK with respect to HSCLK. *Id.* As such, RXRECCLK, in this implementation, has a frequency that is 20% (one-fifth) of that of HSCLK, and shifted in phase (by the 5-bit shift-register) to HSCLK.

212. Since TXUSRCLK is phase-matched with RXRECCLK, TXUSRCLK also has a frequency that is one-fifth of that of HSCLK, and phase-shifted to HSCLK. This renders obvious claims 3 and 4.

213. Since TXUSRCLK has a frequency that is one-fifth of that of HSCLK, the two clock frequencies "correspond" with each other. This renders obvious claim 2.

214. **Virtex-UG further discloses claim 2.** If "correspond" requires the two frequencies to be identical, it is my opinion that Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 2. As discussed

in elements [1.b] and [1.j], HSCLK discloses the "first clock signal" and TXUSRCLK discloses the "first transmitter side clock signal." As discussed in element [1.k], TXUSRCLK is phase-matched with RXRECCLK (which discloses the "first receiver side clock signal").

215. Virtex-UG discloses configuration signals PLL_RXDIVSEL_OUT and PLL_DIVSEL_REF. Ex. 1009, 72. These are exemplary user configuration signals for the Xilinx Virtex-5 GTP Transceivers that control dividers that relate to RXRECCLK (and through control of RXRECCLK, impacts TXUSRCLK). PLL_RXDIVSEL_OUT, which can be set to 1, 2, or 4, is used to divide the incoming clock signal to produce a receiver side clock. Ex. 1009, 73. Virtex-UG discloses that setting PLL_RXDIVSEL_OUT to 1 results in a clock division of one, hence the same frequency. Ex. 1009, 77 (providing example where incoming clock at 1.5625 GHz with "the external divider (PLL_RXDIVSEL_OUT)" set to 1 results in same clock rate of 1.5625 GHz). Likewise, PLL_DIVSEL_REF "[c]ontrols the reference clock divider" hence impacts both RXRECCLK and TXUSRCLK at the same time, and can be set to 1 or 2. Ex. 1009, 73.

216. Virtex-UG's disclosures of clock dividers that divide by one render obvious this limitation. As discussed in Ground 1, claim 3, Giordano discloses that in the Receiver Unit PMA, "HSCLK is divided down by 5" by a clock divider (denoted as "÷ 5"), which then outputs RXRECCLK. Ex. 1005, 196, Fig. 3. As

such, RXRECCLK, in this implementation, has a frequency that is 20% (one-fifth) of that of HSCLK.

217. It would have been obvious to a POSITA to modify the "÷ 5" block in Giordano to incorporate the clock dividers of Virtex-UG, namely those that can be set to 1. With such clock divider, RXRECCLK (and thus TXUSRCLK) would have the same frequency as HSCLK, rendering obvious this limitation.

### c) Claim 5

**[5]: "The method of claim 1, wherein the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation."**

218. It is my opinion that Giordano renders obvious this claim. As discussed in element [1.m], Giordano's disclosures on PCS layer processing and FPGA Fabric "logic" discloses the claimed "set of operations."

219. The operations on PCS layers and FPGA Fabric each discloses this limitation.

220. Giordano's Comma Detector and Aligner implemented in the FPGA Fabric performs pattern matching (detecting comma characters in the raw 10-bit data), comparison (determining the number of bit shifts required), and conditional branching (the even/odd decision logic that either applies RXSLIDE assertions or resets the CDR). Ex. 1005, 198. These are examples of logical operations, which disclose this limitation.

221. In addition, Giordano points to the PCS layer (both receiver and transmitter sides) as "processing" data, rendering obvious computational circuitry. Ex. 1005, 194. The PCS layer includes 8b/10b encoding / decoding functions, which requires arithmetic calculations hence rendering obvious this claim. Ex. 1005, 197.

**d) Claim 6**

**[6]: "The method of claim 1, wherein the first amount of data streams is the same as the second amount of data streams."**

222. It is my opinion that Giordano's disclosure of 8b/10b encoding / decoding renders obvious this claim.

223. Giordano discloses using 8b/10b encoding, where the SIPO deserializes incoming stream 10-bit parallel words, then decoded into 8-bit parallel data words. Ex. 1005, 195. On the transmit side, the FPGA fabric supplies 8-bit parallel data words to the GTP, which encodes them using the internal 8b-to-10b encoder before the PISO serializes the resulting 10-bit words. Ex. 1005, 195, 197. A POSITA would have found it obvious to have what is identified as first amount of data streams to be identical to second amount of data streams, either 8-bits or 10-bits.

### e) Claim 7

**[7]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams."**

224. It is my opinion that Giordano discloses this claim. As discussed in claim 6, Giordano renders obvious internal parallel data width to be the same on both receiver and transmitter sides.

225. Giordano's use of 8-bit parallel words (eight data streams) and 10-bit parallel words (ten data streams) discloses this limitation. Ex. 1005, 195.

### f) Claim 8

**[8]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer."**

226. It is my opinion that Giordano discloses this claim.

227. Giordano discloses use of 8-bit parallel words (eight data streams), which is two to the power of three and discloses this limitation. Ex. 1005, 195.

### g) Claim 9

**[9]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer."**

228. It is my opinion that Giordano discloses this claim.

229. Giordano discloses use of 10-bit parallel words (ten data streams), which is ten times two to the power of zero and discloses this limitation. Ex. 1005, 195.

### h) Claim 10

**[10]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer."**

230. It is my opinion that Giordano renders obvious this claim.

231. **Virtex-UG further discloses claim 10**. It is my opinion that Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 10. As discussed in Ground 1, elements [1.h] and [1.m], Giordano's SIPO block output, further processed by the Receiver Unit PCS, disclose the "first amount of data streams," and processed parallel data going through the Transmitter Unit PCS and PMA disclose the "second amount of data streams."

232. Virtex-UG discloses that the Virtex-5 FPGA GTP Transceiver supports 64b/66b encoding, in addition to the 8b/10b encoding demonstrated by Giordano (using the same Virtex-5 FPGA GTP Transceiver). Ex. 1009, 283, 286, 290; Ex. 1005, 194 ("The architecture we present in this paper is based on the GTP transceiver of the Xilinx Virtex 5 FPGA family"). By using the 64b/66b encoding standard, it would have been obvious to modify the GTP transceiver of the proposed combination to support 66-bit data words. This would have rendered obvious first

and second amount of data streams at 66 bits. Since 66 is thirty-three times two to the power of one, Virtex-UG renders obvious this limitation.

### i) Claim 11

**[11]: "The method of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams."**

233. It is my opinion that Giordano renders obvious this claim. As discussed in element [1.k], Kaviani's Clock Generator output (C0) discloses the "second clock signal" (with the fourth frequency), and output from Giordano's Shared PLL discloses the "first wire rate clock" (with the fifth frequency). As discussed in claim 8, Giordano discloses 8-bit and 10-bit words, which disclose the "second amount of data streams."

234. Giordano's disclosure of 10-bit words as the claimed "second amount" means that the claimed "second amount of data streams" is equal to ten. This, with Giordano's use of clock dividers, renders obvious this limitation.

235. Giordano discloses that the output of the Shared PLL ("first wire rate clock") is connected to a divider block denoted "÷N," which in turn outputs TXOUTCLK. A POSITA would have understood N to be an integer, including ten. This results in Giordano's Shared PLL output ("first wire rate clock") to have a frequency ten times that of TXOUTCLK. Since TXOUTCLK is synchronized with Clock Generator output ("second clock signal"), it would have been obvious to a POSITA for the two clocks to have the same frequency. Hence the Shared PLL

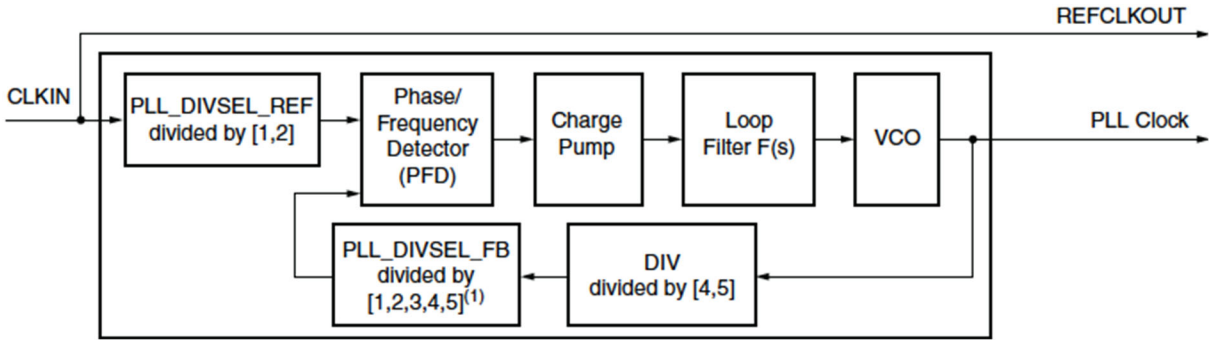
output ("first wire rate clock") would have a frequency ten times that of Clock Generator output ("second clock signal"), rendering obvious this limitation.

236. **Virtex-UG further discloses claim 11.** Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 11. As discussed in element [1.k], Kaviani's Clock Generator output (C0) discloses the "second clock signal" (with the fourth frequency), and output from Giordano's Shared PLL discloses the "first wire rate clock" (with the fifth frequency). As discussed in claim 8, Giordano discloses 8-bit and 10-bit words, which disclose the "second amount of data streams."

237. Giordano's disclosure of 10-bit words as the claimed "second amount" means that the claimed "second amount of data streams" is equal to ten. This, with Giordano's use of clock dividers, renders obvious this limitation.

238. Giordano discloses that the output of the Shared PLL ("first wire rate clock") is connected to a divider block denoted "÷N," which in turn outputs TXOUTCLK.

239. Virtex-UG discloses two divider blocks DIV and PLL_DIVSEL_FB, when put together, could divide signals by eight or ten. Per Figure 5-2 of Virtex-UG, an exemplary cascade of dividers are shown:




240. The clock path that includes the PLL_DIVSEL_FB block and the DIV block results in various combinations of frequency divisions. For example, PLL_DIVSEL_FB dividing by 2 and DIV dividing by 5 results in overall division of ten. PLL_DIVSEL_FB dividing by 2 and DIV dividing by 4 results in overall division of eight.

241. Applying this to the proposed combination, a POSITA would have known to implement Virtex-UG's cascaded dividers into Giordano's divider block "÷N." Using the cascade to have total division of ten results in Giordano's Shared PLL output ("first wire rate clock") to have a frequency ten times that of TXOUTCLK. Since TXOUTCLK is synchronized with Clock Generator output ("second clock signal"), it would have been obvious to a POSITA for the two clocks to have the same frequency. Hence the Shared PLL output ("first wire rate clock") would have a frequency ten times that of Clock Generator output ("second clock signal"), rendering obvious this limitation.

### j) Claim 12

**[12]: "The method of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams."**

242. It is my opinion that Giordano in view of Kaviani renders obvious this claim. As discussed in element [1.k], Kaviani's Clock Generator output (C0) discloses the "second clock signal" (with the fourth frequency), and output from Giordano's Shared PLL discloses the "first wire rate clock" (with the fifth frequency). As discussed in claim 8, Giordano discloses 8-bit and 10-bit words, which disclose the "second amount of data streams."

243. Giordano's disclosure of 10-bit words as the claimed "second amount" means that the claimed "half of the second amount of data streams" is equal to five. This, with Giordano's use of clock dividers, renders obvious this limitation.

244. Giordano discloses using clock dividers of "÷ 5" for the receiver clock divider. Ex. 1005, Fig. 3. On the transmitter side, the output of the Shared PLL ("first wire rate clock") is connected to a divider block denoted "÷N," which in turn outputs TXOUTCLK. A POSITA would have known to use the "÷ 5" divider, explicitly used for the receiver side, for the "÷N" block on the transmitter side. This results in Giordano's Shared PLL output ("first wire rate clock") to have a frequency five times that of TXOUTCLK. Since TXOUTCLK is synchronized with Clock Generator output ("second clock signal"), it would have been obvious to a POSITA for the two clocks to have the same frequency. Hence the Shared PLL output ("first

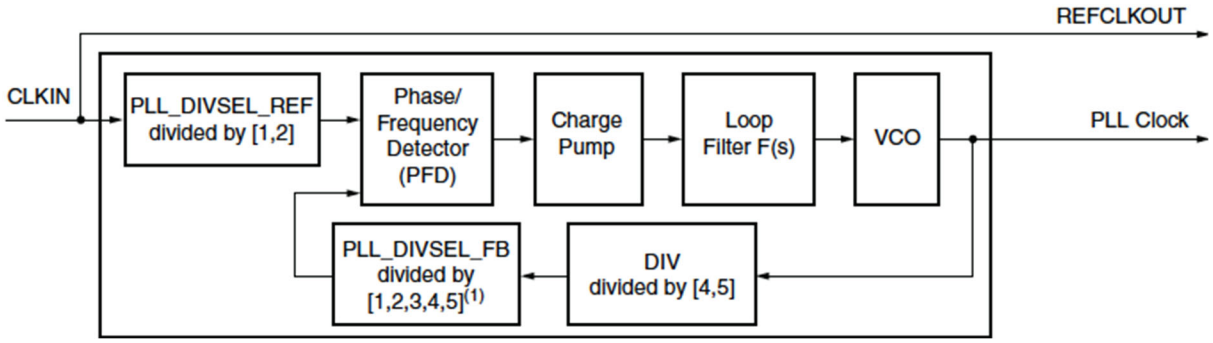
wire rate clock") would have a frequency five times that of Clock Generator output ("second clock signal"), rendering obvious this limitation.

245. **Virtex-UG further discloses claim 12**. It is my opinion that Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 12. As discussed in claim 11, Virtex-UG discloses cascading dividers that support multitude of clock frequency division options.

246. Giordano's disclosure of 10-bit words as the claimed "second amount" means that the claimed "second amount of data streams" is equal to ten. This, with Giordano's use of clock dividers, renders obvious this limitation.

247. Giordano discloses that the output of the Shared PLL ("first wire rate clock") is connected to a divider block denoted "÷N," which in turn outputs TXOUTCLK.

248. Virtex-UG discloses two divider blocks DIV and PLL_DIVSEL_FB, when put together, could divide signals by four or five. Per Figure 5-2 of Virtex-UG, an exemplary cascade of dividers are shown:



249. The clock path that includes the PLL_DIVSEL_FB block and the DIV block results in various combinations of frequency divisions. For example, PLL_DIVSEL_FB dividing by 1 and DIV dividing by 5 results in overall division of five. PLL_DIVSEL_FB dividing by 1 and DIV dividing by 4 results in overall division of four.

250. Applying this to the proposed combination, a POSITA would have known to implement Virtex-UG's cascaded dividers into Giordano's divider block "÷N." Using the cascade to have total division of five results in Giordano's Shared PLL output ("first wire rate clock") to have a frequency five times that of TXOUTCLK. Since TXOUTCLK is synchronized with Clock Generator output ("second clock signal"), it would have been obvious to a POSITA for the two clocks to have the same frequency. Hence the Shared PLL output ("first wire rate clock") would have a frequency five times that of Clock Generator output ("second clock signal"), rendering obvious this limitation.

### k) Claim 13

**[13]: "The method of claim 1, wherein the fourth frequency is a rational multiple of the second frequency."**

251. Giordano in view of Kaviani renders obvious this claim. As discussed in elements [1.e] and [1.k], Giordano's recovered clock (RXRECCLK) discloses the "second frequency," and Clock Generator output (C0) discloses the "fourth frequency."

252. In the proposed combination, C0 and RXRECCLK have the same frequency. Multiplication by one is a rational multiple, hence C0 and RXRECCLK disclose this limitation.

253. **Virtex-UG further discloses claim 13.** Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 13. As discussed in elements [1.e] and [1.k], Giordano's recovered clock (RXRECCLK) discloses the "second frequency," and Clock Generator output (C0) discloses the "fourth frequency."

254. In the proposed combination, C0 is tied to TXUSRCLK, and hence have the same frequency.

255. Virtex-UG discloses various potential relationships between TXUSRCLK and RXRECCLK. Depending on the value for PLL_TXDIVSEL_OUT and PLL_RXDIVSEL_OUT, which are control signals for dividers for TXUSRCLK and RXRECCLK respectively, the frequency relationship between the two clocks differs. Ex. 1009, 72. PLL_TXDIVSEL_OUT and PLL_RXDIVSEL_OUT can be assigned values of 1, 2, and 4. Ex. 1009, 73. For example, if both PLL_TXDIVSEL_OUT and PLL_RXDIVSEL_OUT are set to 1, 2, or 4, since both TXUSRCLK and RXRECCLK are subject to the same amount of division, with other conditions set the same, TXUSRCLK and RXRECCLK will have the same frequency. This will change if the ratio between

PLL_TXDIVSEL_OUT and PLL_RXDIVSEL_OUT shifts. For example, if PLL_TXDIVSEL_OUT is set to 4 while PLL_RXDIVSEL_OUT is set to 1, since the transmitter clock is subject to division of 4 while receiver clock is only subject to division by 1, RXRECCLK's frequency will be four times of TXUSRCLK. This allows for the frequency ratio between TXUSRCLK and RXRECCLK to range in 1/4, 1/2, 1, 2, and 4, which are all rational multiples, hence disclosing this limitation.

### l) Claim 14

**[14]: "The method of claim 1, wherein the phase difference indicator signal is a pulse signal."** [3]

256. It is my opinion that Kaviani discloses this claim.

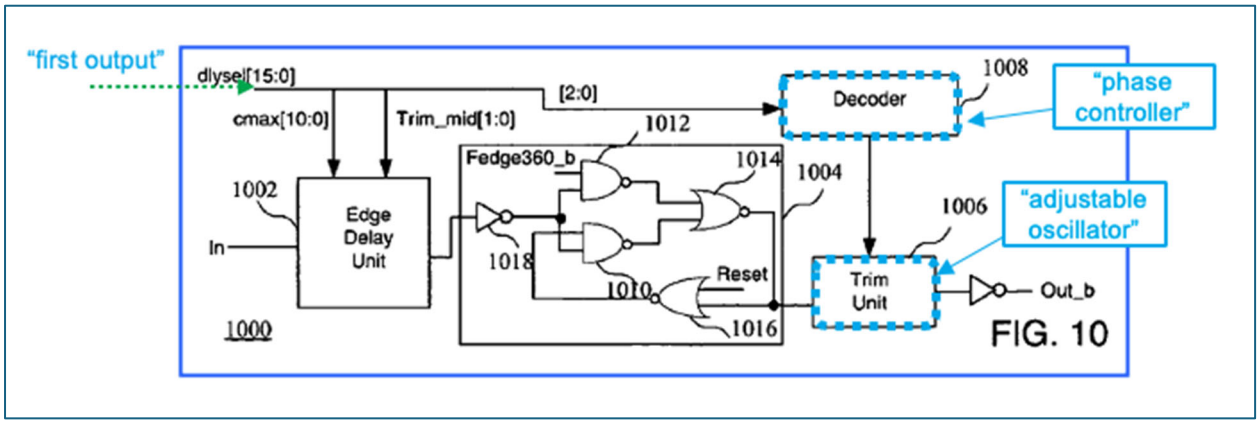
257. As discussed in element [1.j], Kaviani discloses a phase in window function. Kaviani discloses a "phase_inwindow" signal used for this phase-matching function, which takes a form of a pulse signal. Ex. 1010, 6:15–54, Figs. 5–6. Phase_inwindow discloses this limitation. Kaviani further discloses various pulse signals used for phase matching, which render obvious this limitation. Ex. 1010, 11:33–58, Fig. 13.

### m) Claims 15-18

258. Claims 15–18 concern "adjustment information," which Petitioners understand to refer to the claimed "interim adjustment information." As discussed

[3] The term "the phase difference indicator signal" lacks antecedent basis. For the purpose of this IPR, I have been instructed to presume this as a term introduced in claim 14 and hence should be understood as "***a*** phase difference indicator signal."

in element [1.k], the signal from Kaviani's decoder to trim unit (shown in image below) discloses the claimed "interim adjustment information."




**[15]: "The method of claim 1, wherein adjustment information indicates at least one of the following: (A) a desired phase; (B) a desired frequency; (C) a change in phase; and (D) a change in frequency."**

259. It is my opinion that Kaviani discloses this claim. The control signals to trim unit 1006 include at least an indication of a desired phase and change in phase, disclosing this limitation. *Id.*, 9:46–10:28.

**[16]: "The method of claim 15, wherein adjustment information comprises a voltage."**

260. It is my opinion that Kaviani discloses this claim. The decoder 1008 takes in a vector signal dlysel[15:0] to control the trim unit, which per Figures 5, 6, and 13 are shown as voltage signals. A POSITA would have understood the output of the decoder to also be a voltage. Indeed, all control signals (which are described in Figures 5, 6, and 13) take form of a voltage signal.

**[17]: "The method of claim 16, wherein adjustment information comprises a digital transmission."**

261. It is my opinion that Kaviani discloses this claim. The control signal is a voltage signal, which is an output from a decoder that takes in vector signal dlysel[15:0]. A POSITA would have understood the output of the decoder to disclose digital transmission.

**[18]: "The method of claim 1, wherein the adjustment information is used to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay."**

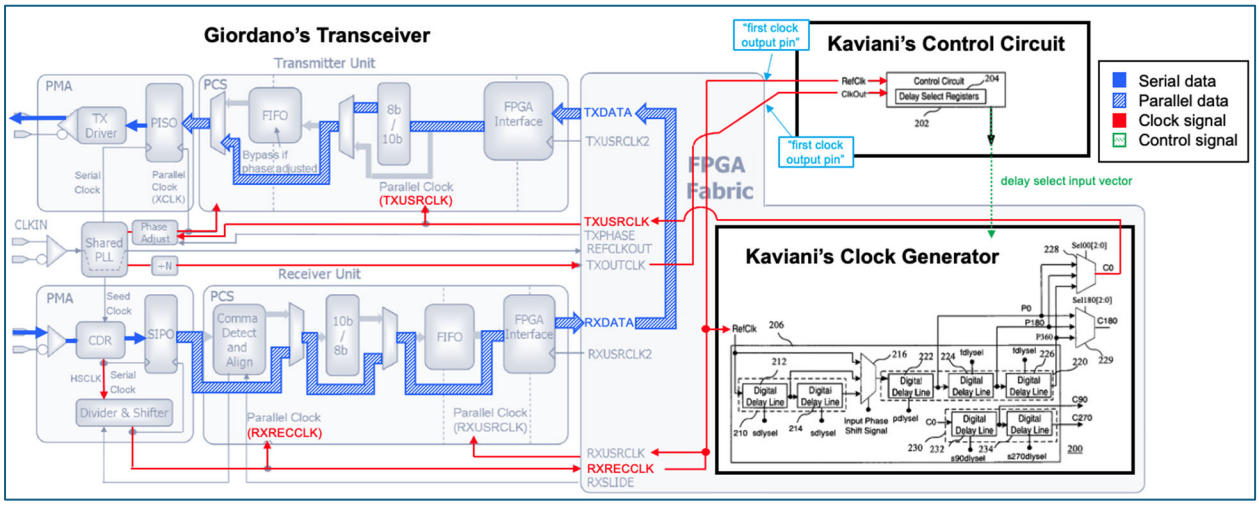
262. It is my opinion that Kaviani discloses this claim. Kaviani discloses that this trim unit 1006 "provides a fine grain delay adjustment to the combined clock signal," which are controlled by decoders. *Id.*, 9:46–10:28. This discloses at least setting a delay, which discloses this limitation.

### n) Claim 21

**[21.a]: "The method of claim 1, wherein the first clock output pin is operationally connected to the deserializer and the second clock output pin is operationally connected to the serializer; and"**

263. It is my opinion that Giordano in view of Kaviani renders obvious this limitation. As discussed in elements [1.i] and [1.k], the connection from the FPGA Fabric to Kaviani's off-FPGA Control Circuit inputs disclose the clock output pins—the connection to RefClk input discloses "first clock output pin" and that to ClkOut input discloses "second clock output pin." As discussed in elements [1.c] and [1.k], Giordano's Receiver Unit PMA discloses the claimed "deserializer" and Transmitter

Unit PMA with the Shared PLL discloses the claimed "serializer." Overall connections, with the two output pins marked in blue, are shown in the image below:




264. In the proposed combination, RefClk input ("first clock output pin") of Kaviani's Control Circuit is connected to Receiver Unit PMA ("deserializer") through RXRECCLK ("receiver side clock signal"). ClkOut input ("second clock output pin") of Kaviani's Control Circuit is connected to the Shared PLL through TXOUTCLK ("interim transmitter side clock signal"). Having signal connections between a circuit component and pin would have been understood as being operationally connected, hence the connections above render obvious this limitation.

**[21.b]: "wherein the phase detector is not on the field programmable gate array and is operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array."**

265. It is my opinion that Giordano in view of Kaviani renders obvious this limitation. As discussed in element [1.i], Kaviani's Control Circuit discloses the off-FPGA-chip "phase detector."

266. In the proposed combination, RefClk input ("first clock output pin") of Kaviani's Control Circuit is connected to Receiver Unit PMA ("deserializer") through RXRECCLK ("receiver side clock signal"). ClkOut input ("second clock output pin") of Kaviani's Control Circuit is connected to the Shared PLL through TXOUTCLK ("interim transmitter side clock signal"). Having signal connections between a circuit component and pin would have been understood as being operationally connected, hence the connections above render obvious this limitation.

## B. Ground 2: Claims 1–21 Are Rendered Obvious By Giordano in view of Kaviani further in view of Raymond

267. It is my opinion that Giordano in view of Kaviani further in view of Raymond renders obvious each and every element of claims 1–21.

### 1. Prior Art Overview

268. As discussed above in Sections VII.C, VIII, and IX.A.1, the prior art references Giordano, Kaviani, and Raymond, and the state of the art at the time of the claimed invention help form my detailed analysis of Ground 2.

#### a) Motivation to Combine Giordano, Kaviani, and Raymond

269. As discussed above in Section IX.A.1 (Ground 1 Prior Art Overview), it would have been obvious to a POSITA to combine Giordano and Kaviani.

270. It is my opinion that a POSITA would have been motivated to look to Raymond to combine with Giordano and Kaviani.

271. Raymond emphasized the importance of minimizing latency in communication devices, particularly for applications such as financial exchange. Ex. 1007 at 1:18–38. Raymond recognizes that higher clock rates reduce latency but also notes that this requires adding a distinct (faster) clock, and additional clock conversions introduce unwanted latency. *Id.*, 8:40–50.

272. A POSITA reading Raymond would therefore have recognized that Giordano in view of Kaviani offers a solution for synthesizing clock signals at the required frequencies while managing phase alignment and filtering jitter—precisely the clock distribution challenges Raymond identifies. Section IX.A.1.a (Motivation to Combine Giordano and Kaviani).

273. A POSITA would have recognized Giordano in view of Kaviani as an attractive solution for the PLL functionality depicted in Raymond's system, and would have been motivated to look to Giordano and Kaviani to combine with Raymond. Raymond repeatedly discusses implementing its invention with Xilinx UltraScale GTY transceivers. Ex. 1007 at 5:48–56, 6:3–8, 8:18–28, 8:51–55. A

POSITA reading Raymond would have naturally consulted Xilinx's own materials (such as Kaviani, a Xilinx patent) and publications demonstrating Xilinx FPGA implementations (such as Giordano), for a PLL-based phase alignment solution.

274. A POSITA would have had a reasonable expectation of success in combining Giordano, Kaviani, and Raymond. A POSITA would have recognized that the FPGA's programmable logic and on-chip clock management resources could be configured to implement the teachings of the three references as needed. Because all references suggest implementations with Xilinx transceiver infrastructure, a POSITA would have had a high expectation that the combination would function as intended. Section IX.A.1.a (Motivation to Combine Giordano and Kaviani).

### 2. Ground 2 – Analysis

#### a) Independent Claim 1

**[1.pre]: "A method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data, wherein the method comprises the steps of:"**

275. If the preamble is found limiting with respect to "market data" and "entry data," Raymond discloses [1.pre].

276. Raymond expressly identifies electronic trading as a primary application for its ultra-low latency communication device, and describes the incoming and outgoing data streams in terms that correspond directly to market data and order entry data. For example, Raymond discloses incoming and outgoing serial

data streams in context of "financial trading data," which are transmitted to and from "financial exchange." Ex. 1007, 4:52–65.

277. Indeed, Raymond discloses "market data feed handler" and "market data feed distribution systems" applications, disclosing receiving market data. Ex. 1007, 13:61–64. Raymond further discloses that the outgoing data link layer signal 250 is "outputted after logical processing (e.g., applying financial trading algorithms)," hence disclosing sending out financial order related data and operations associated with trading algorithms. *Id.* at 11:57–60.

**[1.a] through [1.p]:**

278. As discussed in Section IX.A.2.a (Ground 1, cl. 1), it is my opinion that Giordano in view of Kaviani renders obvious these limitations. Because Giordano in view of Kaviani renders claim 1 obvious, the combination of Giordano, Kaviani, and Raymond also renders claim 1 obvious.

**b) Claims 2-4**

279. As discussed in Section IX.A.2.b (Ground 1, cls. 2–4), it is my opinion that Giordano in view of Kaviani renders obvious these claims. Because Giordano in view of Kaviani renders claims 2–4 obvious, the combination of Giordano, Kaviani, and Raymond also renders claims 2–4 obvious.

### c) Claim 5

**[5]: "The method of claim 1, wherein the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation."**

280. As discussed in Section IX.A.2.c (Ground 1, cl. 5), it is my opinion that Giordano in view of Kaviani renders obvious this claim.

281. It is my opinion that Raymond further discloses this claim.

282. Raymond discloses that data on the transmitting side includes "an outgoing data link layer signal 250 that has been outputted after logical processing (e.g., applying financial trading algorithms)" and "[a] transmitting side PCS module 92 converts the data link layer signal to an outgoing electrical physical layer parallel output signal 252." Ex. 1007, 11:57–63. The applying of financial trading algorithms in Raymond discloses the claimed "first set of operations." Raymond's application of financial trading algorithms involves arithmetic operations, hence discloses this limitation. Ex. 1007, 11:57–60.

### d) Claim 6

**[6]: "The method of claim 1, wherein the first amount of data streams is the same as the second amount of data streams."**

283. As discussed in Section IX.A.2.d (Ground 1, cl. 6), it is my opinion that Giordano in view of Kaviani renders obvious this claim.

284. It is my opinion that Raymond further discloses this claim.

285. Raymond discloses that "the transmitting-side SerDes module 256 can have the same serialization ratio as the de-serialization ratio of the receiving side SerDes module 240." Ex. 1007, 12:23–25. The same ratio results in the same parallel data streams, hence rendering this limitation obvious.

**e) Claim 7**

**[7]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams."**

286. As discussed in Section IX.A.2.e (Ground 1, cl. 7), it is my opinion that Giordano in view of Kaviani renders obvious this claim.

287. It is my opinion that Raymond further discloses this claim.

288. Raymond discloses that "the UltraScale™ GTY from Xilinx™ has internal data buses of 16, 20, 32, 40 or 64 bits, with a minimum bit-width of 16 bits and a minimum de-serialization ratio of 1:16." Ex. 1007, 6:5–8. A POSITA would have understood that the SerDes module 208 could be configured to apply any of these de-serialization ratios depending on the application requirements, and that the serialization ratio of SerDes module 256 would match.

### f) Claim 8

**[8]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer."**

289. As discussed in Section IX.A.2.f (Ground 1, cl. 8), it is my opinion that Giordano in view of Kaviani renders obvious this claim.

290. It is my opinion that Raymond further discloses this claim.

291. Raymond discloses that "internal data buses of 16, 20, 32, 40 or 64 bits." Ex. 1007, 6:5–8. 16 is two to the power of four, 32 is two to the power of five, and 64 is two to the power of six, hence Raymond's 16, 32, and 64 bit buses disclose this limitation.

### g) Claim 9

**[9]: "The method of claim 6, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer."**

292. As discussed in Section IX.A.2.g (Ground 1, cl. 9), it is my opinion that Giordano in view of Kaviani renders obvious this claim.

293. It is my opinion that Raymond further discloses this claim.

294. Raymond discloses that "internal data buses of 16, 20, 32, 40 or 64 bits." Ex. 1007, 6:5–8. 20 is ten times two to the power of one, and 40 is ten times two to the power of two, hence Raymond's 20 and 40 bit buses disclose this limitation.

### h) Claims 10–18

295. As discussed in Section IX.A.2.h–m (Ground 1, cls. 10–18), it is my opinion that Giordano in view of Kaviani renders obvious these claims. Because Giordano in view of Kaviani renders claims 10–18 obvious, the combination of Giordano, Kaviani, and Raymond also renders claims 10–18 obvious.

### i) Claim 19

**[19]: "The method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm."**

296. It is my opinion that Raymond discloses this claim.

297. As discussed in [1.pre], Raymond discloses applying financial trading algorithms to market data to generate order entry data.

### j) Claim 20

**[20]: "The method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data."**

298. It is my opinion that Raymond discloses this claim.

299. As discussed in [1.pre], Raymond discloses applying financial trading algorithms to market data to generate order entry data.

### k) Claim 21

300. As discussed in Section IX.A.2.n (Ground 1, cl. 21), it is my opinion that Giordano in view of Kaviani renders obvious these claims. Because Giordano

in view of Kaviani renders claim 21 obvious, the combination of Giordano, Kaviani, and Raymond also renders claim 21 obvious.

### C. Ground 3: Claims 1–18, 21 Are Rendered Obvious By Giordano in view of Kaviani further in view of Virtex-UG

301. It is my opinion that Giordano in view of Kaviani further in view of Virtex UG renders obvious each and every element of claims 1–18, and 21.

#### 1. Prior Art Overview

302. As discussed above in Sections VII.C, VIII, and IX.A.1, the prior art references Giordano, Kaviani, and Virtex-UG and the state of the art at the time of the claimed invention help form my detailed analysis of Ground 3.

##### a) Motivation to Combine Giordano, Kaviani, and Virtex-UG

303. While Giordano already inherently discloses and incorporates Virtex-UG, if necessary, it is my opinion that a POSITA would have been motivated to look to Virtex-UG to combine with Giordano and Kaviani. Virtex-UG is a user guide for Xilinx Virtex FPGA offerings, which is the FPGA chip used in Giordano and referenced in Kaviani. Ex. 1005, 194, 197–199; Ex. 1010, 1:44–49. Virtex-UG details how to use, configure, and modify the Virtex-5 FPGA "RocketIO" GTP transceiver. *See generally*, Ex. 1009.

304. A POSITA reading Virtex-UG would therefore have recognized that its teachings would be helpful in the use, configuration, and modification of the FPGA

system based on Giordano in view of Kaviani, including for synthesizing clock signals at the required frequencies while managing phase alignment and filtering jitter. Section IX.A.1.a (Motivation to Combine Giordano and Kaviani).

305. A POSITA would have had a reasonable expectation of success in combining Giordano, Kaviani, and Virtex-UG. A POSITA would have recognized that the FPGA's programmable logic and on-chip clock management resources could be configured to implement the teachings of the three references as needed. Because all references suggest implementations with Xilinx transceiver infrastructure, a POSITA would have had a high expectation that the combination would function as intended. Section IX.A.1.a (Motivation to Combine Giordano and Kaviani).

#### 2. Ground 3 – Analysis

##### a) Claims 1-18 and 21

306. For the same reasons as discussed in Section IX.A.2, it is my opinion that Giordano in view of Kaviani and Virtex-UG renders obvious each and every element of claims 1–18 and 21.

### D. Ground 4: Claims 1–21 Are Rendered Obvious By Giordano in view of Kaviani, Virtex-UG, and Raymond

307. It is my opinion that Giordano in view of Kaviani, Virtex-UG, and Raymond renders obvious each and every element of claims 1–21.

### 1. Prior Art Overview

308. As discussed above in Sections VII.C, VIII, IX.A.1, and IX.C.1, the prior art references Giordano, Kaviani, Virtex-UG, and Raymond, and the state of the art at the time of the claimed invention, help form my detailed analysis of Ground 4.

#### a) Motivation to Combine Giordano, Kaviani, and Virtex-UG

309. As discussed in Section IX.C.1, it is my opinion that a POSITA would have been motivated to combine Giordano, Kaviani, and Virtex-UG, and would have had a reasonable likelihood of success in making such a combination.

310. It is my opinion that a POSITA would have been motivated to look to Raymond to combine with Giordano, Kaviani, and Virtex-UG, for the same reasons to combine Raymond with Giordano and Kaviani, as presented in Section IX.B.1.

### 2. Ground 4 – Analysis

#### a) Claims 1–21

311. As discussed in Section IX.C.2.a (Ground 3, cls. 1–18, 21), it is my opinion that Giordano in view of Kaviani and Virtex-UG renders obvious these claims. Because Giordano in view of Kaviani and Virtex-UG renders claims 1–18 and 21 obvious, the combination of Giordano, Kaviani, Virtex-UG, and Raymond also renders claims 1–18 and 21 obvious.

312. In addition, if the preamble of claim 1 is found limiting with respect to "market data" and "entry data," it is my opinion that Raymond discloses [1.pre]. Section IX.B.2.a (Ground 2, cl. 1).

313. It is my opinion that Raymond further discloses claims 5–9, 19–21. Section IX.B.2.c–g, i–k.

## X. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS

314. In my opinion, the prior art references that I rely on for the grounds of invalidity are enabled.

315. As I explained above in Section V, I understand an obviousness analysis includes consideration of "secondary" or "objective" evidence of non-obviousness, including things such as: (1) a long-felt but unmet need in the prior art that was satisfied by the claimed invention; (2) commercial success or the lack of commercial success of the claimed invention; (3) unexpected results achieved by the claimed invention; (4) praise of the claimed invention by others skilled in the art; (5) taking of licenses under the patent by others; (6) deliberate copying of the claimed invention; and (7) contemporaneous and independent invention by others.

316. I am not aware of any secondary considerations of non-obviousness raised by Patent Owner with respect to the Challenged Claims of the '865 patent.

317. As an example, I am not aware of any showing of a long-felt but unmet need satisfied by the '865 patent. As I explained in my state of the art and

obviousness analyses above, any alleged "need" that would have been satisfied by the '865 patent had already been satisfied in light of the prior art cited herein. As another example, I am not aware of any commercial success of any data processing system that is due to its practicing of the Challenged Claims of the '865 patent. I likewise am not aware of any evidence relating to the other "secondary" or "objective" considerations listed above.

318. Accordingly, the consideration of "secondary" or "objective" evidence of non-obviousness does not change my opinion that claims 1–21 of the '865 patent would have been obvious to one of skill in the art.

## XI. CONCLUSION

319. Based on my review and above analysis of the prior art, it is my opinion that claims 1–21 of the '865 patent would have been obvious to one of skill in the art.

I, Benjamin Carrion Schaefer, hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like are so made punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the Petition for *inter partes* review.

Executed on June __9____, 2026

By

Benjamin Carrion Schaefer

# Appendix A

# Benjamin Carrion Schaefer

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## EDUCATION

| | |
|---|---|
| **MBA**, McGill University, Canada | 2008 - 2010 |
| **Ph.D.**, Reconfigurable Computing, The University of Birmingham, UK | 1999 - 2003 |
| **M.Sc.**, Microelectronics, Birmingham City University, UK | 1998 - 1999 |
| **B.Eng.**, Electronic Engineering, Universidad Politecnica, Madrid, Spain | 1993 - 1997 |

## EMPLOYMENT HISTORY

| | |
|---|---|
| **Assistant Dean Graduate Student Success**, School of Engineering, UTD | 2023 - present |
| **Associate Professor**, ECE dept., The University of Texas at Dallas | 2022 - present |
| **Assistant Professor**, ECE dept., The University of Texas at Dallas | 2016 - 2022 |
| **Assistant Professor**, EIE dept., The Hong Kong Polytechnic University | 2012 - 2016 |
| **Researcher**, NEC Corp. Central R&D Laboratories, Japan | 2007 - 2012 |
| **Postdoc**, Seoul National University, Korea | 2005 - 2007 |
| **Postdoc**, University of California Los Angeles, USA | 2003 - 2004 |

## RESEARCH INTERESTS

Reconfigurable Computing, FPGAs, Electronic Design Automation (EDA), High-Level Synthesis (HLS), Hardware Security, Low-power design, Approximate Computing.

## PROFESSIONAL RECOGNITIONS AND HONORS

GOMACTech 2025 Best Poster Award, 2025
$35^{th}$ Great Lakes Symposium on VLSI (GLSVLSI) best poster award, 2025
Winner of faculty 3 minute talk (f3mt) UT Dallas Jonsson School of Engineering, 2024
MVP Career Service Faculty Award UT Dallas Jonsson School of Engineering, 2023
UT Dallas Erik Jonsson School of Engineering dean's fellow, 2022-2023
$32^{nd}$ Great Lakes Symposium on VLSI (GLSVLSI) best paper award, 2022
UT Dallas Erik Jonsson School of Engineering & Computer Science best teacher award, 2022
$34^{th}$ Int'l Conference on VLSI Design (VLSID) Naresh Malipeddy honorable mention award, 2021
Best program committee member in GLSVLSI symposium, 2018
Hack at DAC competition, third place, 2017
Brain Korean 21 (BK21) scholarship, Seoul, Korea, 2005
Interdisciplinary Research Fund scholarship, University of Birmingham, UK, 1999
M.Sc. Birmingham City University, UK, awarded with distinction, 1999
GFTN Gesellschaft zur Förderung technischen Nachwuchses, Darmstadt, Germany, 1998

## SCHOLARLY AND PROFESSIONAL SERVICE ACTIVITIES

**Service within the University**

| | |
|---|---|
| Member, CE Graduate Committee | 2025 - 2026 |
| Member, Search Committee | 2024 - 2025 |
| Member, Search Committee | 2023 - 2024 |
| Member, University Committee on Student Technology Requirements | 2022 - 2023 |
| Member, Search Committee | 2022 - 2023 |
| Member, CE Graduate Committee | 2020 - 2021 |

| | |
|---|---|
| Member, University Library Committee | 2020 - 2021 |
| Member, CE Graduate Committee | 2019 - 2020 |
| Member, University Library Committee | 2019 - 2020 |
| Member, Undergraduate Teaching Committee | 2018 - 2019 |
| Member, Search Committee | 2018 - 2019 |
| Member, Search Committee | 2017 - 2018 |
| Member, Undergraduate Teaching Committee | 2016 - 2017 |

**Journal Editorial Activities**

| | |
|---|---|
| Associate Editor, IEEE Transaction on Computer-Aided Design (TCAD) | 2025-present |
| Associate Editor, IEEE Transaction on Sustainable Computing | 2022-present |
| Associate Editor, Integration, The VLSI Journal (Elsevier) | 2014 - 2022 |

**Conference Organization, Executive Committee, Track chair**

| | |
|---|---|
| Track Chair, IEEE Design Automation and Test Europe (DATE) | 2027 |
| Track Chair, IEEE Design Automation and Test Europe (DATE) | 2026 |
| Track Chair, Innovative Applications of Artificial Intelligence (IAAI) | 2026 |
| **General Chair**, IEEE International Conference on Computer Design (ICCD) | 2025 |
| TPC Chair, IEEE International Conference on Computer Design (ICCD) | 2024 |
| Track Chair, IEEE Design Automation and Test Europe (DATE) | 2025 |
| **General Chair**, IEEE Dallas Circuits and Systems Conference (DCAS) | 2024 |
| Track Chair, ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) | 2024 |
| Track Chair (EDA), IEEE International Conference on Computer Design (ICCD) | 2023 |
| Technical Program co-Chair, IEEE Dallas Circuits and Systems Conference (DCAS) | 2023 |
| Track Chair (EDA), IEEE International Conference on Computer Design (ICCD) | 2022 |
| Workshop co-chair, 7th Workshop on Approximate Computing (AxC22) | 2022 |
| Special Sessions Chair, IEEE Dallas Circuits and Systems Conference (DCAS) | 2022 |
| Track co-Chair, ACM/IEEE International Conference on CAD (ICCAD) | 2021 |
| Track Chair, ACM/IEEE Design Automation Conference (DAC) | 2021 |
| Track Chair, ACM Great Lakes Symposium on VLSI (GLSVLSI) | 2021 |
| Track Chair, ACM/IEEE Design Automation Conference (DAC) | 2020 |
| Track Chair, ACM Great Lakes Symposium on VLSI (GLSVLSI) | 2020 |
| Track Chair, ACM/IEEE Design Automation Conference (DAC) | 2019 |
| Track Chair, ACM Great Lakes Symposium on VLSI (GLSVLSI) | 2019 |
| Local Arrangement Chair, IEEE Midwest Symposium on Circuits and Systems (MWSCAS) | 2019 |
| **General Chair**, ESLsyn conference, co-located with DAC | 2014 |

**Member of the Technical Program Committee**

| | |
|---|---|
| IEEE Conference on Field Programmable Technology (FPT) | 2026 |
| IEEE Conference on Field Programmable Gate Arrays (FPL) | 2026 |
| IEEE Reconfigurable Architectures Workshop (RAW) | 2026 |
| IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM) | 2026 |
| IEEE Design Automation Conference (DAC) | 2026 |
| ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) | 2026 |
| ACM/IEEE International Conference on Computer Aided Design (ICCAD) | 2025 |
| IEEE Conference on Field Programmable Gate Arrays (FPL) | 2025 |
| IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM) | 2025 |
| IEEE Design Automation Conference (DAC) | 2025 |
| IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM) | 2024 |
| IEEE Design Automation and Test Europe (DATE) | 2024 |
| ACM Great Lakes Symposium on VLSI (GLSVLSI) | 2023 |
| ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) | 2023 |
| ACM/IEEE International Conference on Computer Aided Design (ICCAD)(student competition) | 2022 |

| | |
|---|---|
| IEEE Conference on Field Programmable Gate Arrays (FPL) | 2022 |
| IEEE Application-Specific Systems, Architectures and Processors (ASAP) | 2022 |
| ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) | 2022 |
| IEEE International Conference on Computer Design (ICCD) | 2021 |
| IEEE Transaction on Computers. TPC for special issue on Compiler Optimizations for FPGAs | 2021 |
| ACM/IEEE International Conference on Computer Aided Design (ICCAD) | 2021 |
| IEEE Application-Specific Systems, Architectures and Processors (ASAP) | 2021 |
| ACM/IEEE Design Automation Conference (DAC) | 2021 |
| IEEE Design Automation and Test Europe (DATE) | 2021 |
| IEEE Conference on Field Programmable Gate Arrays (FPL) | 2021 |
| ACM Great Lakes Symposium on VLSI (GLSVLSI) | 2021 |
| ACM/IEEE International Conference on Computer Aided Design (ICCAD) | 2020 |
| IEEE Application-Specific Systems, Architectures and Processors (ASAP) | 2020 |
| ACM/IEEE Design Automation Conference (DAC) | 2020 |
| IEEE Design Automation and Test Europe (DATE) | 2020 |
| IEEE Conference on Field Programmable Gate Arrays (FPL) | 2020 |
| ACM Great Lakes Symposium on VLSI (GLSVLSI) | 2020 |
| ACM/IEEE International Conference on Computer Aided Design (ICCAD) | 2019 |
| IEEE Application-Specific Systems, Architectures and Processors (ASAP) | 2019 |
| ACM/IEEE Design Automation Conference (DAC) | 2019 |
| ACM/IEEE Design Automation and Test Europe (DATE) | 2019 |
| IEEE Conference on Field Programmable Gate Arrays (FPL) | 2019 |
| ACM Great Lakes Symposium on VLSI (GLSVLSI) | 2019 |
| IEEE Conference on Field Programmable Gate Arrays (FPL) | 2018 |
| ACM Great Lakes Symposium on VLSI (GLSVLSI) | 2018 |
| ACM/IEEE Design Automation Conference (DAC) | 2018 |
| IEEE Conference on Field Programmable Gate Arrays (FPL) | 2018 |
| ACM Great Lakes Symposium on VLSI (GLSVLSI) | 2018 |
| ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) | 2017 |
| IEEE Conference on Field Programmable Gate Arrays (FPL) | 2017 |
| ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) | 2016 |
| Electronic System Level Synthesis Conference (ESLSyn) | 2015 |
| ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) | 2015 |
| Electronic System Level Synthesis Conference (ESLSyn) | 2014 |
| Electronic System Level Synthesis Conference (ESLSyn) | 2013 |

**NSF Reviewer**

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|---|---|
| NSF Reviewer | 2026 |
| NSF Reviewer | 2025 |
| NSF Reviewer | 2024 |
| NSF Reviewer | 2022 |
| NSF Reviewer | 2021 |
| NSF Reviewer | 2021 |
| NSF Reviewer | 2019 |

**External PhD Reviewer**

| | |
|---|---|
| City University, HKSAR | 2024 |
| Columbia University, USA | 2022 |
| Universidad Politecnica de Madrid, Spain | 2021 |
| Universidad Politecnica de Madrid, Spain | 2020 |
| Visvesvaraya Technological University (VTU), India | 2018 |

## ACHIEVEMENTS IN ORIGINAL INVESTIGATION

**Total: 154 Publications (3 Books, 3 Book chapters, 41 Journals, and 106 Conferences)**
**First author: 40 Publications (3 Books, 1 Book chapter, 19 Journals, and 17 Conferences)**

## Books

[B4] **B. Carrion Schaefer**. *High-Level Synthesis Made Easy (Second Edition)*. 2nd. highX Technologies, 2026, pp. 1–183. URL: http://www.hlsbook.com.

[B4] **B. Carrion Schaefer**. *High-Level Synthesis : Applications*. 1st. highX Technologies, 2025, pp. 1–98. URL: http://www.hlsbook.com.

[B4] **B. Carrion Schaefer**. *High-Level Synthesis Made Easy*. 1st. highX Technologies, 2023, pp. 1–135. URL: http://www.hlsbook.com.

## Book Chapters

[BC4] Srinivas Katkoori and Sheikh Ariful Islam. *Source Code Obfuscation of Behavioral IPs: Challenges and Solutions, chapter 3*. 2020.

[BC4] Wim Vanderbauwhede and Khaled Benkrid. *High-Level Synthesis: From Algorithm to Digital Circuit, chapter 7*. 2013.

[BC4] Philippe Coussy and Adam Morawiec. *High-Level Synthesis: From Algorithm to Digital Circuit*. 2008.

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[J43] Md. Imtiaz Rashid and **B. Carrion Schafer**. "Robust and Efficient RTL to C Compiler Optimized for High-Level Synthesis". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 42.11 (Nov. 2024), pp. 1–9.

[J43] T. Kaur, A. Gamez, J.L. Olvera, **B. Carrion Schaefer**, and A. Corona-Chavez. "I-TAINTED: Identification of Turmeric Adulteration using the Cavity Perturbation Technique and Technology optimized Machine Learning". In: *IEEE Access* (2023), pp. 1–11.

[J43] Md. Imtiaz Rashid and **B. Carrion Schafer**. "Fast and Inexpensive High-Level Synthesis Design Space Exploration : Machine Learning to the Rescue". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 42.11 (Nov. 2023), pp. 3939–3950.

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## Conference Papers

[C107] Baharealsadat Parchamdar and **B. Carrion Schafer**. "Breaking Behavioral IPs Design Space Lock". In: *Great Lakes Symposium on VLSI* ***(Best Poster Award)***. GLSVLSI'25. Association for Computing Machinery, 2025, pp. 1–6.

[C107] Sabrina Ahmed, Khaza Anuarul Hoque and **B. Carrion Schafer**. "Robust and Fault-Aware Design for Resilient Edge Computing AI Accelerators". In: *Great Lakes Symposium on VLSI*. GLSVLSI'25. Association for Computing Machinery, 2025, pp. 1–6.

[C107] Victoria Gammenthaler and **B. Carrion Schafer**. "Improving the Quality of the High-Level Synthesis Estimation Results through Multi-Level Predictive Models". In: *Great Lakes Symposium on VLSI*. GLSVLSI'25. Association for Computing Machinery, 2025, pp. 1–6.

[C107] C.G. Sathe,Y. Makris, **B. Carrion Schafer**. "FREEDOM: FPGA-based Hardware Redaction Emulator". In: *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM 2025)*. 2025, pp. 1–5.

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[C107] C.G. Sathe, A. Fowler, C. Sechen, **B. Carrion Schafer**, Y. Makris, M. Zaman and R. Narumi. "What to Redact? Guideliens for Cost-Effecive Hardware Intellectual Propoerty Protection **(Best Poster Award)**". In: *GOMACTech*. 2025, pp. 1–4.

[C107] B. Parchamdar and **B. Carrion Schafer**. "ADVISOR: Approximate Computing-frienDly High-LeVel Synthesis DesIgn Space ExplORer". In: *ACM/IEEE Design Automation Conference (DAC)*. June 2025, pp. 1–6.

[C107] M. Imtiaz Rashid and **B. Carrion Schafer**. "Making Legacy Hardware Robust against Side Channel Attacks via High-Level Synthesis". In: *Asia and South Pacific Design Automation (ASP-DAC)*. Jan. 2025, pp. 1–6.

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[C107] Q. Si and **B. Carrion Schafer**. "HAMMER: Hardware-aware Runtime Program Execution Acceleration through runtime reconfigurable CGRAs". In: *Asia and South Pacific Design Automation (ASP-DAC)*. Jan. 2025, pp. 1–6.

[C107] M. Imtiaz Rashid and **B. Carrion Schafer**. "VeriPy: A Python-Powered Framework for Parsing Verilog HDL and High-Level Behavioral Analysis of Hardware". In: *IEEE Dallas Circuits and Systems (DCAS)*. Apr. 2024, pp. 1–6.

[C107] B. Parchamdar and **B. Carrion Schafer**. "Investigating the Effect of Hyper-Parameter Settings on Simulated Annealing-based High-Level Synthesis Design Space Exploration". In: *IEEE Dallas Circuits and Systems (DCAS)*. Apr. 2024, pp. 1–5.

[C107] B. Parchamdar and **B. Carrion Schafer**. "Finding Bugs in RTL Descriptions: High-Level Synthesis to the Rescue". In: *ACM/IEEE Design Automation Conference (DAC)*. June 2024, pp. 1–6.

[C107] S. Shetty and **B. Carrion Schafer**. "Facilitating the Design of complete System-on-Chip through High-Level Synthesis". In: *GOMACTech*. 2024, pp. 1–4.

[C107] S. Yu and **B. Carrion Schafer**. "Temperature Control through dynamic Approximation". In: *GOMACTech*. 2024, pp. 1–4.

[C107] **B. Carrion Schafer** and C.G. Sathe. "Circumventing Restrictions in commercial High-Level Synthesis Tools". In: *Design, Automation, and Test in Europe (DATE)*. Mar. 2024, pp. 1–2.

[C107] Qilin Si and **B. Carrion Schafer**. "PEPA: Performance Enhancement of Embedded Processors through HW Accelerator Resource Sharing". In: *Great Lakes Symposium on VLSI*. GLSVLSI'23. Association for Computing Machinery, 2023, pp. 1–6.

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[C107] Md Imtiaz Rashid, A.H. Torabi and **B. Carrion Schafer**. "CERTIFY: Automatic Measuring the Quality of High-Level Synthesis". In: *IEEE International Symposium on Circuits and Systems (ISCAS)*. May 2023, pp. 1–5.

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[C107] C.G. Sathe, Y. Makris, and **B. Carrion Schafer**. "MANTIS: Machine Learning-Based Approximate ModeliNg of RedacTed Integrated CircuitS". In: *Design, Automation, and Test in Europe (DATE)*. Mar. 2023, pp. 1–6.

[C107] A. Hossein Md I. Rashid and **B. Carrion Schafer**. "Automatic Modernization of Hardware Assets". In: *GOMACTech*. 2023, pp. 1–5.

[C107] C. Sathe Md I. Rashid and **B. Carrion Schafer**. "ROPE: Re-usability Lock of Behavioral Intellectual Property". In: *GOMACTech*. 2023, pp. 1–5.

[C107] Prattay Chowdhury, Jorge Castro Godinez, and **B. Carrion Schafer**. "Approximating HWAccelerators through Partial Extractions onto shared Artificial Neural Networks". In: *Asia and South Pacific Design Automation (ASP-DAC)*. Jan. 2023, pp. 1–6.

[C107] P. Chowdhury, C.G. Sathe, **B. Carrion Schafer**. "Predictive Model Attack for Embedded FPGA Logic Locking". In: *International Symposium on Low Power Electronics and Design (ISLPED)*. ISLPED '22. ACM/IEEE, 2022, pp. 1–6.

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[C107] S. Shetty and **B. Carrion Schafer**. "Enabling the Design of Behavioral Systems-on-Chip". In: *ACM/IEEE Design Automation Conference (DAC)*. July 2021, pp. 1–6.

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[C107] R. Sreekumar, P. Chowdhury, and **B. Carrion Schafer**. "Bespoke Approximate Behavioral Processors". In: *IEEE 38th International Conference on Computer Design (ICCD)*. Nov. 2020, pp. 1–4.

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[C107] J. Chen and **B. Carrion Schafer**. "Exploiting the Benefits of High-level Synthesis for Thermal-aware VLSI Design". In: *IEEE 37th International Conference on Computer Design (ICCD)*. Nov. 2019.

[C107] S. Xu and **B. Carrion Schafer**. "Low Power Design of Runtime Reconfigurable FPGAs through Contexts Approximations". In: *IEEE 37th International Conference on Computer Design (ICCD)*. Nov. 2019.

[C107] S. Xu and **B. Carrion Schafer**. "Approximating Behavioral HW Accelerators through Selective Partial Extractions onto Synthesizable Predictive Models". In: *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*. Nov. 2019, pp. 1–8.

[C107] M. R. Babu, F. N. Taher, A. Balachandran, and **B. Carrion Schafer**. "Efficient Hardware Acceleration for Design Diversity Calculation to Mitigate Common Mode Failures". In: *IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*. Apr. 2019, pp. 267–270.

[C107] Jianqi Chen and **B. Carrion Schafer**. "Thermal Fingerprinting of FPGA Designs through High-Level Synthesis". In: *Great Lakes Symposium on VLSI*. GLSVLSI '19. Tysons Corner, VA, USA: Association for Computing Machinery, 2019, pp. 331–334.

[C107] Zhiqi Zhu, Farah Naz Taher, and **B. Carrion Schafer**. "Exploring Design Trade-Offs in Fault-Tolerant Behavioral Hardware Accelerators". In: *Great Lakes Symposium on VLSI*. GLSVLSI '19. Tysons Corner, VA, USA: Association for Computing Machinery, 2019, pp. 291–294.

[C107] Bo Hu, Jingxiang Tian, Mustafa Shihab, Gaurav Rajavendra Reddy, William Swartz, Yiorgos Makris, **B. Carrion Schafer**, and Carl Sechen. "Functional Obfuscation of Hardware Accelerators through Selective Partial Design Extraction onto an Embedded FPGA". In: *Great Lakes Symposium on VLSI*. GLSVLSI '19. Tysons Corner, VA, USA: Association for Computing Machinery, 2019, pp. 171–176.

[C107] S. Liu, F. C. Lau, and **B. Carrion Schafer**. "Accelerating FPGA Prototyping through Predictive Model-Based HLS Design Space Exploration". In: *56th ACM/IEEE Design Automation Conference (DAC)*. June 2019, pp. 1–6.

[C107] A. Mahapatra and **B. Carrion Schafer**. "Optimizing RTL to C Abstraction Methodologies to Improve HLS Design Space Exploration". In: *IEEE International Symposium on Circuits and Systems (ISCAS)*. May 2019, pp. 1–5.

[C107] Z. Wang and **B. Carrion Schafer**. "Partial Encryption of Behavioral IPs to Selectively Control the Design Space in High-Level Synthesis". In: *Design, Automation Test in Europe Conference Exhibition (DATE)*. Mar. 2019, pp. 642–645.

[C107] M. M. Shihab, J. Tian, G. R. Reddy, B. Hu, W. Swartz, **B. Carrion Schafer**, C. Sechen, and Y. Makris. "Design Obfuscation through Selective Post-Fabrication Transistor-Level Programming". In: *Design, Automation Test in Europe Conference Exhibition (DATE)*. Mar. 2019, pp. 528–533.

[C107] F. N. Taher, M. Joslin, A. Balachandran, Z. Zhu, and **B. Carrion Schafer**. "Common-Mode Failure Mitigation: Increasing Diversity through High-Level Synthesis". In: *Design, Automation Test in Europe Conference Exhibition (DATE)*. Mar. 2019, pp. 1563–1566.

[C107] Z. Zhu, J. Callenes-Sloan, and **B. Carrion Schafer**. "Control Flow Checking Optimization Based on Regular Patterns Analysis". In: *IEEE 23rd Pacific Rim International Symposium on Dependable Computing (PRDC)*. Dec. 2018, pp. 203–212.

[C107] S. Xu and **B. Carrion Schafer**. "DEEP: Dedicated Energy-Efficient Approximation for Dynamically Reconfigurable Architectures". In: *IEEE 36th International Conference on Computer Design (ICCD)*. Oct. 2018, pp. 587–594.

[C107] S. Xu and **B. Carrion Schafer**. "Autonomous Temperature Management through Selective Control of Exact-Approximate Tiles". In: *IEEE 36th International Conference on Computer Design (ICCD)*. Oct. 2018, pp. 346–349.

[C107] F. N. Taher, M. Kishani, and **B. Carrion Schafer**. "Design and Optimization of Reliable Hardware Accelerators: Leveraging the Advantages of High-Level Synthesis". In: *IEEE 24th International Symposium on On-Line Testing And Robust System Design (IOLTS)*. July 2018, pp. 232–235.

[C107] Shuangnan Liu, Francis Lau, and **B. Carrion Schafer**. "Investigation and Optimization of Pin Multiplexing in High-Level Synthesis". In: *Great Lakes Symposium on VLSI*. GLSVLSI '18. Chicago, IL, USA: Association for Computing Machinery, 2018, pp. 427–430.

[C107] Farah Naz Taher, Joseph Callenes-Sloan, and **B. Carrion Schafer**. "A Machine Learning Based Hard Fault Recuperation Model for Approximate Hardware Accelerators". In: *55th Annual Design Automation Conference*. DAC '18. San Francisco, California: Association for Computing Machinery, 2018.

[C107] S. Xu, J. Chen, and **B. Carrion Schafer**. "HW/SW co-design experimental framework using configurable SoCs". In: *International Conference on ReConFigurable Computing and FPGAs (ReConFig)*. Dec. 2017, pp. 1–6.

[C107] S. Xu, **B. Carrion Schafer**, and Y. Liu. "Configurable SoC In-Situ Hardware/Software Co-Design Design Space Exploration". In: *IEEE International Conference on Computer Design (ICCD)*. Nov. 2017, pp. 509–512.

[C107] S. Xu and **B. Carrion Schafer**. "Approximate Reconfigurable Hardware Accelerators: Adapting the Micro-architecture to Dynamic Workloads". In: *IEEE International Conference on Computer Design (ICCD)*. Nov. 2017, pp. 1–7.

[C107] S. Liu and **B. Carrion Schafer**. "Learning-based interconnect-aware dataflow accelerator optimization". In: *27th International Conference on Field Programmable Logic and Applications (FPL)*. Sept. 2017, pp. 1–7.

[C107] **B. Carrion Schafer**, David Aledo, and Félix Moreno. "Application Specific Behavioral Synthesis Design Space Exploration: Artificial Neural Networks. A Case Study". In: *Euromicro Conference on Digital System Design, DSD*. 2017, pp. 129–136.

[C107] Y. Liu, M. Villaverde, F. Moreno, and **B. Carrion Schafer**. "Characterization and optimization of behavioral hardware accelerators in heterogeneous MPSoCs". In: *12th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*. July 2017, pp. 1–8.

[C107] Muhammad Yasin, Abhrajit Sengupta, **B. Carrion Schafer** Schafer, Yiorgos Makris, Ozgur Sinanoglu, and Jeyavijayan (JV) Rajendran. "What to Lock? Functional and Parametric Locking". In: *Great Lakes Symposium on VLSI 2017*. GLSVLSI '17. Banff, Alberta, Canada: Association for Computing Machinery, 2017, pp. 351–356.

[C107] N. Veeranna and **B. Carrion Schafer**. "Efficient behavioral intellectual properties source code obfuscation for high-level synthesis". In: *2017 18th IEEE Latin American Test Symposium (LATS)*. Mar. 2017, pp. 1–6.

[C107] N. Veeranna and **B. Carrion Schafer**. "Hardware Trojan avoidance and detection for dynamically re-configurable FPGAs". In: *International Conference on Field-Programmable Technology (FPT)*. Dec. 2016, pp. 193–196.

[C107] Dong Liu and **B. Carrion Schafer**. "Efficient and reliable High-Level Synthesis Design Space Explorer for FPGAs". In: *26th International Conference on Field Programmable Logic and Applications (FPL)*. Aug. 2016, pp. 1–8.

[C107] A. Balachandran, N. Veeranna, and **B. Carrion Schafer**. "On Time Redundancy of Fault Tolerant C-Based MPSoCs". In: *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. July 2016, pp. 631–636.

[C107] Y. Liu and **B. Carrion Schafer**. "Optimization of behavioral IPs in multi-processor system-on-chips". In: *21st Asia and South Pacific Design Automation Conference (ASP-DAC)*. Jan. 2016, pp. 336–341.

[C107] I. Llamas-Garro, J. Bas, J. M. Fàbrega, M. S. Moreolo, **B. Carrion Schafer**, R. Torres-Torres, M. R. T. de Oliveira, M. T. de Melo, Jung-Mu Kim, and D. Vukobratovic. "Recent trends and considerations for high speed data in chips and system interconnects". In: *SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference (IMOC)*. Nov. 2015, pp. 1–6.

[C107] Xiaotong Li and **B. Carrion Schafer**. "Temperature-triggered behavioral IPs HW Trojan detection method with FPGAs". In: *25th International Conference on Field Programmable Logic and Applications (FPL)*. Sept. 2015, pp. 1–4.

[C107] Yidi Liu and **B. Carrion Schafer**. "Adaptive combined macro and micro-exploration of concurrent applications mapped on shared bus Reconfigurable SoC". In: *Electronic System Level Synthesis Conference (ESLsyn)*. June 2015, pp. 11–16.

[C107] **B. Carrion Schafer**. "Process selection for maximum resource sharing in High-Level Synthesis". In: *Electronic System Level Synthesis Conference (ESLsyn)*. June 2015, pp. 35–40.

[C107] Y. Liu and **B. Carrion Schafer**. "HW acceleration of multiple applications on a single FPGA". In: *International Conference on Field-Programmable Technology (FPT)*. Dec. 2014, pp. 284–285.

[C107] **B. Carrion Schafer**. "Time sharing of Runtime Coarse-Grain Reconfigurable Architectures processing elements in multi-process systems". In: *International Conference on Field-Programmable Technology (FPT)*. Dec. 2014, pp. 76–82.

[C107] A. Mahapatra and **B. Carrion Schafer**. "Machine-learning based simulated annealer method for high level synthesis design space exploration". In: *Proceedings of the 2014 Electronic System Level Synthesis Conference (ESLsyn)*. May 2014, pp. 1–6.

[C107] **B. Carrion Schafer**. "Allocation of FPGA DSP-macros in multi-process high-level synthesis systems". In: *19th Asia and South Pacific Design Automation Conference (ASP-DAC)*. Jan. 2014, pp. 616–621.

[C107] **B. Carrion Schafer**. "Automatic partitioning of behavioral descriptions for high-level synthesis with multiple internal throughputs". In: *Electronic System Level Synthesis Conference (ESLsyn)*. May 2013, pp. 1–6.

[C107] Shahin Golshan, Eli Bozorgzadeh, **B. Carrion Schafer**, Kazutoshi Wakabayashi, Houman Homayoun, and Alex Veidenbaum. "Exploiting Power Budgeting in Thermal-Aware Dynamic Placement for Reconfigurable Systems". In: *Proceedings of the 16th ACM/IEEE International Symposium on Low Power Electronics and Design*. ISLPED 2010. Austin, Texas, USA: ACM, 2010, pp. 49–54.

[C107] **B. Carrion Schafer**, Takashi Takenaka, and Kazutoshi Wakabayashi. "Adaptive Simulated Annealer for high level synthesis design space exploration". In: *2009 International Symposium on VLSI Design, Automation and Test*. Apr. 2009, pp. 106–109.

[C107] **B. Carrion Schafer**, Y. Lee, and T. Kim. "Temperature-Aware Compilation for VLIWProcessors". In: *13th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2007)*. Aug. 2007, pp. 426–431.

[C107] **B. Carrion Schafer** and T. Kim. "Thermal-Aware Instruction Assignment for VLIW Processors". In: *11th Workship on Interaction between Compilers and Computer Architectures (INTERACT-11))*. Feb. 2007.

[C107] **B. Carrion Schafer**, S. F. Quigley, and A. H. C. Chan. "Scalable Implementation of the Discrete Element Method on a Reconfigurable Computing Platform". In: *Field-Programmable Logic and Applications: Reconfigurable Computing Is Going Mainstream*. Berlin, Heidelberg: Springer Berlin Heidelberg, 2002, pp. 925–934.

[C107] **B. Carrion Schafer**, S. F. Quigley, and A. H. C. Chan. "Implementation of the Discrete Element Method using reconfigurable computing (FPGAs)," in: *15th Engineering Mechanics Conference (EM2002)*. 2002.

[C107] **B. Carrion Schafer**, S. F. Quigley, and A. H. C. Chan. "Analysis and implementation of the discrete element method using a dedicated highly parallel architecture in reconfigurable computing". In: *10th Annual IEEE Symposium on Field-Programmable Custom Computing Machines*. 2002, pp. 173–181.

[C107] **B. Carrion Schafer**, S. F. Quigley, and A. H. C. Chan. "Description of a Dedicated Hardware Architecture for the Discrete Element Method (DEM) implemented on a Field Programmable Gate Array (FPGA)," in: *10th Annual conference of the Association for Computational Mechanics in Engineering (ACME)*. 2002, pp. 51–54.

[C107] **B. Carrion Schafer**, Steven F. Quigley, and Andrew H. C. Chan. "Evaluation of an FPGA Implementation of the Discrete Element Method". In: *Field-Programmable Logic and Applications*. Berlin, Heidelberg: Springer Berlin Heidelberg, 2001, pp. 306–314.

[C107] **B. Carrion Schafer**, S. F. Quigley, and A. H. C. Chan. "Numeric Modeling of the Mechanical interaction between non-biological particles using reconfigurable computing". In: *9th Annual conference of the Association for Computational Mechanics in Engineering (ACME)*. 2001, pp. 53–56.

## Patents

[P2] **B. Carrion Schafer**. *Method and Apparatus for Incremental Design Space Exploration*. U.S. Patent 8,977,996 B2.

[P2] **B. Carrion Schafer**. *Method and Apparatus for Design Space Exploration*. JP Patent 2012-522281.

### RESEARCH IMPACT AND CITATIONS

h-index (Google Scholar January 2025): 26
i10-index (Google Scholar January 2025): 45
Citations (Google Scholar January 2025): 2402

## SOFTWARE ARTIFACTS RELEASED

**FREEDOM: FPGA-based Hardware Redaction Emulator**
Hardware redaction emulation framework that allows to quickly prototype ASIC+eFPGA designs onto a single low-cost FPGA. The emulator is available at *https://github.com/chaitalisathe/FREEDOM*. The framework only requires a Terasic DE1-SoC standard board.

**DSE2Frame: DSE Explorer Framework**
DSEFrame is a QT-based open source development framework to create and visualize High-Level Synthesis (HLS) design space exploration results. The development framework is freely available online at *https://github.com/DARCLabHao/DSEframe*.

**S2CBench: Synthesizable SystemC Benchmark Suite**
S2CBench is collection of over 20 SystemC benchmarks from different domain that comply with the latest Accelera's SystemC synthesizable subset. The benchmark suite is freely available online at *https://sourceforge.net/projects/s2cbench/* from where it has been downloaded over 1,000 times.

**S3CBench: Security Synthesizable SystemC Benchmark Suite**
S3CBench is the extension of the S2CBench benchmarks instrumented with malicious alterations a.k.a. Hardware Trojan that when triggered lead to deviation of the benchmark from its original intended behavior . The benchmark suite is freely available online at *https://sourceforge.net/projects/s3cbench/* from where it has been downloaded over 300 times.

## UNIVERSITY COURSES TAUGHT

**At the University of Texas at Dallas**

| Year | Semester | Code | Type | Title, Credits, Students |
|---|---|---|---|---|
| 2025 | Fall | EEDG/CE6370 | Grad/elec | Reconfigurable Systems, 3, 48 |
| 2024 | Fall | EEDG/CE6370 | Grad/elec | Reconfigurable Systems, 3, 43 |
| 2024 | Summer | EE/CE4304 | Under/core | Computer Architecture, 3, 14 |
| 2023 | Fall | EEDG/CE6304 | Grad/core | Computer Architecture, 3, 60 |
| 2023 | Fall | EEDG/CE6370 | Grad/elec | Reconfigurable Systems, 3, 48 |
| 2023 | Summer | EE/CE4304 | Under/core | Computer Architecture, 3, 16 |
| 2022 | Fall | EE/CE4307 | Under/core | Embedded Systems, 3, 37 |
| 2022 | Fall | EEDG/CE6304 | Grad/core | Computer Architecture, 3, 55 |
| 2022 | Summer | EE/CE4304 | Under/core | Computer Architecture, 3, 10 |
| 2022 | Spring | EE/CE4307 | Under/core | Embedded Systems, 3, 60 |
| 2021 | Fall | EEDG/CE6331 | Grad/elec | High-Level Synthesis, 3, 8 |
| 2021 | Fall | EEDG/CE6304 | Grad/core | Computer Architecture, 3, 60 |
| 2021 | Spring | EE/CE4307 | Under/core | Embedded Systems, 3, 55 |
| 2020 | Spring | EEDG7V81 | Grad/elec | High-Level Synthesis, 3, 7 |
| 2020 | Fall | EEDG/CE6304 | Grad/core | Computer Architecture, 3, 43 |
| 2020 | Spring | EE/CE4307 | Under/core | Embedded Systems 3, 60 |
| 2019 | Fall | EEDG7V81 | Grad/elec | High-Level Synthesis, 3, 7 |
| 2019 | Fall | EEDG/CE6304 | Grad/core | Computer Architecture, 3, 43 |
| 2019 | Spring | EE/CE4307 | Under/core | Embedded Systems, 3, 49 |
| 2018 | Fall | EEDG7V81 | Grad/elec | High-Level Synthesis, 3, 15 |
| 2018 | Fall | EEDG6304 | Grad/core | Computer Architecture, 3, 13 |
| 2018 | Spring | EEDG6304 | Grad/core | Computer Architecture, 3, 13 |
| 2018 | Spring | EE/CE4370 | Under/core | Embedded Systems, 3, 43 |
| 2017 | Fall | EEDG/CE6304 | Grad/core | Computer Architecture, 3, 16 |
| 2017 | Spring | EEDG/CE6304 | Grad/core | Computer Architecture, 3, 16 |

**At the Hong Kong Polytechnic University**

| Year | Semester | Code | Type | Title, Credits, Students |
|---|---|---|---|---|
| 2016 | Spring | EIE4110 | Under/elect | VLSI&CAD, 3, 31 |
| 2015 | Fall | EIE511 | Grad/elect | VLSI System design,3, 15 |
| 2014 | Spring | EIE4110 | Under/elect | VLSI&CAD, 3, 63 |
| 2014 | Spring | EIE3361 | Under/core | Computer Fund, 3, 62 |
| 2014 | Fall | EIE511 | Grad/elect | VLSI System design, 3, 26 |
| 2014 | Fall | EIE2105 | Under/core | Digital Design, 3, 28 |
| 2014 | Spring | EIE4110 | Under/elect | VLSI&CAD, 3, 29 |
| 2014 | Spring | EIE3361 | Under/core | Computer Fund, 3, 74 |
| 2013 | Fall | EIE2105 | Under/elect | Digital Design, 3, 35 |
| 2013 | Spring | EIE305 | Under/elect | Digital Circuits, 3, 18 |
| 2013 | Spring | EIE361 | Under/core | Computer Fund, 3, 56 |
| 2013 | Spring | EIE410 | Under/elect | VLSI&CAD, 3, 22 |

## STUDENT SUPERVISION SUMMARY

| | |
|---|---|
| **Ph.D. students currently supervised:** | 6 |
| **M.S. students currently supervised:** | 3 |
| **Ph.D. students graduated:** | 15 |
| **M.S. students graduated:** | 20 |
| **Undergraduate researchers supervised:** | 9 |
| **High School Students supervised:** | 3 |

## GRADUATE STUDENTS CURRENTLY SUPERVISED

**Doctoral Students**

| Ph.D. Candidate | Research Area | Years |
|---|---|---|
| Sabrina Ahmed | Sustainable HW Design | 2023–present |
| Victoria Gammenthaler | Hardware Security | 2024–present |
| Daksith Chandrasekera | LLM-based EDA | 2025–present |
| Salam Kadhim Al-Khammasi | LLM-based VLSI System Generation | 2026–present |
| Adam Kayyal | LLM-based Design Optimization | 2026–present |
| Emmanuel Llanes | TBD (starting in fall) | 2026–present |

**Master Students**

| MS | Research Area | Years |
|---|---|---|
| Mark Ivey | Efficient LLM implementations on FPGAs | 2025–present |
| Sathwik Sudhindranath | Complex DSP applications on FPGAs | 2026–present |
| Samarth Nandeesh | Custom FPGA fabrics for HLS generated Designs | 2026–present |

## GRADUATE STUDENTS PREVIOUSLY SUPERVISED

**Doctoral Advisement/Direction**

| Name | Year | Dissertation (compact) | Job |
|---|---|---|---|
| Baharealsadat Parchamdar | 2026 | HLS optimization/applications | – |
| Chaitali Sathe | 2025 | HW IP security attacks/defense | – |
| Md Imtiaz Rashid | 2024 | HLS circuit modernization | Univ. of Florida (Postdoc) |
| Qilin Si | 2023 | Behavioral processors | NVIDIA |
| Prattay Chowdhury | 2022 | Approximate computing systems | Qualcomm |
| Zi Wang | 2021 | HLS design space search | Cadence |
| Bo Hu | 2021 | Thermal/security HLS design | Apple |
| Jianqi Chen | 2020 | HLS security/low-power design | Cirrus Logic |
| Anjana Balachandran | 2020 | Fault-tolerant circuits | Huawei |
| Zhiqi Zhu | 2020 | Fault-tolerant accelerators | Nubis Comm. |
| Farah Naz Taher | 2019 | HW fault detection/mitigation | Raytheon |
| Siyuan Xu | 2019 | Robust approximate computing | MathWorks |
| Shuangnan Liu | 2019 | Behavioral dataflow design | Cadence |
| Ansuhree Mahapatra | 2018 | RTL abstraction for HLS | ASTRI |
| Nandeesh Veeranna | 2017 | BIP protection | NTU (Postdoc) |

**Masters Advisement/Direction**

| Name | Year | Dissertation (short) | Job After Graduation |
|---|---|---|---|
| Adam Kayyal | 2026 | Synthesis-aware HLS DSE | UT Dallas (PhD), USA |
| Valliyappan Senthilkumar | 2023 | ANN optimization HW/SW | Marvell Tech., USA |
| Amir H. Torabi | 2023 | HLS quality estimation | UT Dallas (PhD), USA |
| Santosh Shetty | 2020 | Behavioral SoC generation | AMD, India |
| Akshay R. Krisnani | 2020 | CNN in-situ training | Intel, USA |
| Yiheng Gao | 2020 | HLS design space search | Nokia, USA |
| Rohit Sreekumar | 2020 | Bespoke processors | Amazon, USA |
| Himanshu Patra | 2019 | HLS language conversion | Intel, USA |
| Maheswaran R. Babu | 2019 | FPGA diversity accel. | Intel, USA |
| Mihir Shah | 2018 | Partial reconfig. architecture | Varex Imaging, USA |
| Monica Gowda | 2018 | HLS exploration | MicroChip, USA |
| Vinay Dasandi | 2018 | Bitwidth optimization | Delphi, USA |
| Songseok Choi | 2018 | FPGA acceleration automation | SK Hynix, Korea |
| Susmitha Gogineni | 2017 | OpenCL accel. | Texas Instruments, USA |
| Siyuan Xu | 2015 | SoC design exploration | PhD, UT Dallas |
| Zhendong Gao | 2015 | FPGA voice viz. | PCCW, Hong Kong |
| Jieshi Chen | 2015 | (not specified) | DJI, China |
| Yidi Liu | 2015 | Parallel HW acceleration | Huawei |
| Yu Li | 2014 | FPGA gaming console | ZTE, China |
| Xiaotong Li | 2014 | HW Trojan detection | TCL, China |

## VISITING GRADUATE STUDENTS SUPERVISED

| | |
|---|---|
| Takafumi Miyazaki (Visiting from Ritsumeikan University, Japan) | 09/2018-10/2018 |
| Shuangnan Liu (Visiting from Hong Kong Polytechnic University, HKSAR) | 09/2017-12/2018 |
| Nandeesh Veeranna (Visiting from Hong Kong Polytechnic University, HKSAR) | 04/2017-07/2017 |
| Monica Villaverde (Visiting from Universidad Politecnica de Madrid, Spain) | 01/2017-04/2017 |

## UNDERGRADUATE AND HIGH SCHOOL STUDENTS SUPERVISED

**Undergraduate Students**

| | |
|---|---|
| Juan Diego Rosero Rodriguez | Spring 2026 |
| Omar Abiola Abioye | Spring 2025 |
| Shruthigna Chandupatla | Spring 2024 |
| Axel Gamez **(Qualcomm Research Award Recipient)** | Fall 2022 |
| Preston T. Glenn | Summer and Fall 2021 |
| Kimberly Klein **(Qualcomm Research Award Recipient)** | Spring 2021 |
| Michael Nelson | Fall and Spring 2017/2018 |
| Rodolfo Martinez | Summer 2018 |
| Ryota Watanabe | Summer 2018 |
| Kristen Nguyen | Summer 2018 |
| Sean Kennedy | Summer 2018 |

**High School Students**

| | |
|---|---|
| Ishaan Javali | Summer 2019 |
| Alondra Ramos | Summer 2018 |
| Natasha Trayers | Summer 2018 |

## KEYNOTES, INVITED TALKS AND SHORT COURSES TAUGHT

**B. Carrion Schaefer**, "Fast and Efficient Domain Specific Hardware Design", The University of Houston, USA, August, 2024.

**B. Carrion Schaefer**, "C-based VLSI Design: Making Hardware Design Easier", Hiroshima City University, Japan, July, 2024.

**B. Carrion Schaefer**, "Career Development: Hiring and Promotion", DAC Early Career Workshop, San Francisco, USA, June, 2024.

**B. Carrion Schaefer** and Jeff Roane, "HLS Adoption and Key Technologies: Rethinking the use of High-Level Synthesis: From FPGA Prototyping to ASIC Design", Cadence Lunch and Learn, Dallas, USA, August, 2023.

**B. Carrion Schaefer**, "Techniques for Finding Security Vulnerabilities in SoCs", ACM/IEEE Design Automation Conference (DAC), San Francisco, USA, June, 2018.

**B. Carrion Schafer**, "Behavioral IPs Micro-architectural Diversity and its Applications", ESLSyn, San Francisco, Co-located with DAC, June 2015,

**B. Carrion Schaefer** and J.H. Anderson, "FPGA high-level synthesis: from software to programmable hardware", tutorial delivered at the ACM/IEEE Asia-South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan, January 2015.

A. Mahapatra and **B. Carrion Schaefer**, "S2CBench:Synthesizable SystemC Benchmark Suite for HighLevel Synthesis", 20th meeting of the North American SystemC Users Group,San Francisco, June, 2014.

**B. Carrion Schaefer**,"The ESL Hotspot - Where Software and Hardware Meet", Design Automation Conference (DAC), 10th annual ESL Symposium, San Francisco, (invited panelist), 2012.

**B. Carrion Schaefer**,"High-Level Synthesis Production Deployment: Are We Ready?", Design Automation Conference (DAC), San Francisco, (invited speaker), 2012.

**B. Carrion Schaefer**,"Challenges and Opportunities of Behavioral Level SoC Design", ESLSyn, Co-located with DAC, San Francisco, (Keynote speaker), 2012.

## GRANTS, CONTRACTS, GIFTS AND DONATIONS

| Sponsor Type | Total Funding ($) | My Share ($) |
|---|---|---|
| U.S. Federal (NSF, ONR, AFRL/AFWERX) | 3,347,139 | 1,211,799 |
| Industry (Boeing, Huawei, Texas Instruments) | 224,000 | 107,000 |
| International Government (NATO, HK UGC, NSFC China) | 443,000 | 134,333 |
| University / Internal (JSRI) | 20,000 | 10,000 |
| Equipment / Software Grants | 25,000 | 25,000 |
| **Total** | **4,059,139** | **1,488,132** |

**Office of Naval Research (ONR), Self-aware Computing Through AI (Sole PI).** 2025-2027
Total amount : $169,729

**NSF, Advancing Innovation in Master of Science and Engineering Scholars Career Development (co-PI w. PI Pearson, UTD).** 2025-2030
Total amount : $2,000,000

**NSF CHEST I/UCRC, Investigating the Weaknesses of IP Protection through eFPGA-based Hardware Redaction (PI w. co-PI Makris). Continuation grant.** 2024-2025
Total amount : $75,000

**NSF, Collaborative Research: DESC: Type I: SEEDED: Sustainability-aware Reliable and Reusable AI Hardware Design (co-PI w. PI Hoque, University of Missouri).** 2023-2026
Total amount : $600,000
Amount UTD: $260,00

**NSF CHEST I/UCRC, Investigating the Weaknesses of IP Protection through eFPGA-based Hardware Redaction (PI w. co-PI Makris).** 2023-2024
Total amount : $65,000

**Jonsson School Research Initiative (JSRI), UTD, Methods for Practical Design for Trust of Complex System-on-Chip (PI w. Co-PI Wong)** 2023-2024
Total amount : $20,000

**NSF CHEST I/UCRC,CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming(co-PI w. PI-Makris and Sechen). Continuation grant** 2022-2023
Total amount : $125,000

**NSF CHEST I/UCRC,CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming(co-PI w. PI-Makris and Sechen). Continuation grant** 2021-2022
Total amount : $125,000

**AFWERX, Microelectronics Challenge Phase III (lead-PI w. Makris and Sechen)** 2020
Total amount : $200,000

**NSF CHEST I/UCRC,CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming(co-PI w. PI-Makris and Sechen)** 2020-2021
Total amount : $100,000

**Boeing/AFRL (co-PI w. PI-Makris and Sechen)** 2020
Total amount : $150,000

**AFWERX, Microelectronics Challenge Phase II (lead-PI w. Makris and Sechen)** 2019
Total amount : $88,410

**NATO, Nerve Agent Detection, (co-PI w. PI-Llamas and Mung)** 2019-2022
Total amount : $236,000

**Huawei USA, Based Band SoC Approximate Computing (Sole PI)** 2018
Total amount : $60,000

**Texas Instruments (Sole PI)** 2018
Total amount : $14,000

**NEC Corporation, Software Grant (CyberWorkBench Software license donation)** 2017
Value: $10,000

**Altera Equipment Grant (Arria SoC and DE1 FPGA Boards)** 2017
Value: $7,000

**Xilinx Equipment Grant (Virtex-5 and Zynq FPGA Boards)** 2017
Total amount : $8,000

**Early Career Scheme, University Grant Council, Hong Kong (Sole PI)** 2014
Total amount : HKD $677,000 ($87,000)

**National Natural Science Foundation of China (co-PI w. PI-Lau and Ho)** 2014
Total amount : RMB $750,000 ($120,000)

## PROFESSIONAL MEMBERSHIPS AND LICENSES

IEEE Senior Member since 2010

Last updated May 4, 2026.