

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

OPTIVER US LLC and OPTIVER TRADING US LLC,
Petitioners

v.

HFT SOLUTIONS, LLC,
Patent Owner.

Case No. IPR2026-00385
U.S. Patent No. 11,018,678

Petition for *Inter Partes* Review of U.S. Patent No. 11,018,678

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TABLE OF EXHIBITS

Exhibit No.	Document
1001	U.S. Patent No. 11,018,678 (“the ’678 patent”)
1002	File History for U.S. Patent No. 11,018,678
1003	Declaration of Ben Carrion Schaefer, Ph.D.
1004	Declaration of Carrie Gardner
1005	R. Giordano and A. Aloisio, <i>Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs</i> , 58-1 IEEE Transactions on Nuclear Science 194 (2011) [Giordano]
1006	<i>(intentionally omitted)</i>
1007	U.S. Pat. No. 10,447,463 [Raymond]
1008	U.S. Pat. No. 8,788,553 [Lee]
1009	Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 [Virtex-UG]
1010	<i>(intentionally omitted)</i>
1011	Declaration of Gordon MacPherson

TABLE OF ABBREVIATIONS

Abbreviation	Term
'678 patent	U.S. Patent No. 11,018,678
AIA	America Invents Act
CDC	Clock Domain Crossing
CDR	Clock and Data Recovery
Challenged Claims	Claims 1–22 of U.S. Patent No. 11,018,678
DLL	Delay Locked Loop
Ex.	Exhibit
Fig.	Figure
FPGA	Field Programmable Gate Array
Giordano	R. Giordano and A. Aloisio, <i>Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs</i> , 58-1 IEEE Transactions on Nuclear Science 194 (2011)
IPR	<i>inter partes</i> review
Lee	U.S. Pat. No. 8,788,553
MAC	Media Access Controller
Patent Owner	HFT Solutions, LLC
PCS	Physical Coding Sublayer
Petitioners	Optiver US LLC and Optiver Trading US LLC
PLL	Phase Locked Loop
PMA	Physical Medium Attachment
Raymond	U.S. Pat. No. 10,447,463
VCO	Voltage Controlled Oscillator
Virtex-UG	Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009
VLSI	Very Large Scale Integration

MANDATORY NOTICES

A. Real Parties-in-Interest: 37 C.F.R. §42.8(b)(1)

Optiver US LLC and Optiver Trading US LLC are the real parties-in-interest. Optiver Services US LLC is a corporate affiliate and services entity supporting Optiver US LLC and Optiver Trading US LLC. The ultimate parent company of all three entities is Optiver Holding BV.

B. Related Matters Under: 37 C.F.R. §42.8(b)(2)

1. Current Litigation

The '678 patent is presently not subject to any litigation. Petitioners are not aware of any litigation involving the '678 patent.

2. Administrative Proceedings

There are no other administrative proceedings at issue. Petitioners have filed or intend to file petitions for *inter partes* review regarding four additional patents—U.S. Pat. Nos. 12,107,587 (IPR2026-00383); 10,763,865 (IPR2026-00384); 10,771,069 (IPR2026-00386); and 11,329,655 (IPR2026-00387)—in the same patent family as the '678 patent.

C. Lead and Back-Up Counsel: 37 C.F.R. §42.8(b)(3)

Petitioners provide the following designation of counsel:

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Petitioners respectfully request authorization to file motions for Brian Rosenthal to appear before the USPTO *pro hac vice*. Mr. Rosenthal is an experienced attorney and is currently serving as lead counsel for Petitioners in an action between Petitioners and Patent Owner.¹ He is familiar with the subject matter at issue in this proceeding. Petitioners intend to file a motion to appear *pro hac vice* under 37 C.F.R. §42.10. Pursuant to 37 C.F.R. §42.10(b), powers of attorney accompany this petition.

¹ Petitioners are currently defending Patent Owner's assertion of U.S. Pat. Nos. 10,931,286; 11,128,305; 11,575,381 in *HFT Solutions, LLC v. Optiver US LLC and Optiver Trading US LLC*, 7:25-cv-415 (W.D. Tex. filed Sept. 8, 2025). These three patents list the same sole inventor (Nima Badizadegan) as the '678 patent but belong to a separate patent family.

D. Service of Information: 37 C.F.R. §42.8(b)(4)

Service of any documents via hand delivery may be made at the mailing address of lead and backup counsel. Petitioners also consent to electronic service, and service via electronic mail may be made at the email addresses provided for the lead and backup counsel.

I. INTRODUCTION

Pursuant to 35 U.S.C. §311, Petitioners seek *inter partes* review of U.S. Pat. No. 11,018,678 (Ex. 1001) and cancellation of claims 1–22 as unpatentable under 35 U.S.C. §103.

The Challenged Claims are directed to an FPGA system that receives and transmits data using synchronized receiver and transmitter clock signals. Ex. 1001, 1:23–28. The alleged invention of the ’678 patent is in using an “internal phase-locked loop” for “*phase matching* receiver side and transmitter side clocks of a FPGA without introducing unnecessary delay in processing.” *Id.*, 2:17–20.² The Challenged Claims purport to achieve this phase matching with a “phase control circuit” that is “at least partially on the [FPGA].” *Id.*, cl. 1.

Yet the prior art taught these concepts before the ’678 patent. **Giordano**, the primary reference for all grounds in this petition, teaches aligning clock signals for serialization/deserialization (“SER/DES”) processes with a deterministic, fixed phase difference. Ex. 1005, 197. Giordano plainly discloses performing everything in claims 1–20 using Xilinx FPGA systems, but lacks certain details in how the phase alignment is achieved. **Lee**, a Xilinx patent, and **Virtex-UG**, a Xilinx user guide, disclose these details. Lee discloses phase matching circuitry that discloses details

² Unless noted otherwise, emphasis added.

of the “phase control circuit.” Virtex-UG teaches specifics of the clock phase alignment features inherent to the Virtex-5 FPGAs used in Giordano. Given the programmable nature of FPGAs (which allows users to modify hardware as needed) and Giordano’s guidance to seek further specifics of phase alignment, a POSITA would have found it obvious to incorporate the teachings of Lee and/or Virtex-UG into Giordano’s FPGA system. Ex. 1005, 198; Ex. 1008, 2:35–3:24, Fig. 2.

Claims 21 and 22 of the ’678 patent add only the application of these well-known FPGA systems to financial trading. **Raymond** expressly teaches using FPGA systems and phase matching (as in Giordano, Lee, and Virtex-UG) in high-frequency trading applications. Ex. 1007, 1:18–38. Applying the known FPGA phase matching teachings disclosed in Giordano, Lee, and Virtex-UG to financial-trading applications as suggested by Raymond would have been straightforward and obvious. *See also* Ex. 1001, 1:41–43 (“FPGAs are used in the financial industry”).

Because this Petition demonstrates a reasonable likelihood that Petitioners will prevail on at least one challenged claim based on prior art not considered during prosecution, the Board should institute *inter partes* review (“IPR”) and cancel claims 1–22 under 35 U.S.C. §103.

II. REQUIREMENTS OF IPR

A. Standing: 37 C.F.R. §42.104(a)

Petitioners certify that the '678 patent is eligible for IPR and that Petitioners are not barred or estopped from requesting IPR of the challenged claims.

B. Identification of Challenge and Relief Requested: 37 C.F.R. §42.104(b)

Petitioners request IPR of claims 1–22 of the '678 patent under AIA 35 U.S.C. §103.

The '678 patent issued from an application filed July 23, 2020, and claims priority to a provisional application filed February 21, 2019. For purposes of this Petition only, Petitioners do not dispute that the Challenged Claims are entitled to an effective filing date of February 21, 2019.

Petitioners request cancellation of claims 1–22 based on:

Ground	Claims	Basis for Rejection³
1	1–20	Obviousness over Giordano in view of Lee
2	1–22	Obviousness over Giordano in view of Lee further in view of Raymond
3	1–20	Obviousness over Giordano in view of Lee further in view of Virtex-UG ⁴

³ All obviousness grounds include the knowledge of a POSITA.

⁴ Giordano inherently discloses the features of Virtex-UG, and further incorporates Virtex-UG by reference. Ex. 1003, ¶¶77, 113. To the extent a POSITA would have not understood the features of Virtex-5 are necessarily present in Giordano, a POSITA would have been motivated to combine Virtex-UG with all grounds based on Giordano.

Ground	Claims	Basis for Rejection ³
4	1–22	Obviousness over Giordano in view of Lee, Virtex-UG, and Raymond

1. R. Giordano and A. Aloisio, *Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs*, 58-1 IEEE Transactions on Nuclear Science 194 (2011) (“Giordano”) (Ex. 1005)

Giordano was published in IEEE Transactions on Nuclear Science on January 28, 2011. Ex. 1004, ¶¶21–26; *id.*, ¶27, 33–34, 37 (citing Ex. 1011). Giordano therefore qualified as prior art under AIA 35 U.S.C. §102(a)(1). Giordano was neither cited nor considered during prosecution of the ’678 patent.

2. Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 (“Virtex-UG”) (Ex. 1009)

Virtex-UG was published on December 3, 2009. Ex. 1004, ¶¶41–47. Virtex-UG therefore qualified as prior art under AIA 35 U.S.C. §102(a)(1). Virtex-UG was neither cited nor considered during prosecution of the ’678 patent.

3. U.S. Pat. No. 8,788,553 (“Lee”) (Ex. 1008)

Lee, titled “Method and Circuit for Providing Digital Frequency Synthesis,” was filed January 28, 2009, and granted July 22, 2014. Lee therefore qualifies as prior art under AIA 35 U.S.C. §102(a)(1) and §102(a)(2). Lee was neither cited nor considered during prosecution of the ’678 patent.

4. U.S. Pat. No. 10,447,463 (“Raymond”) (Ex. 1007)

Raymond, titled “Device and Method for Ultra-low Latency Communication,” claims priority to a provisional application filed July 13, 2017, and an application filed July 13, 2018. Raymond therefore qualifies as prior art under AIA 35 U.S.C. §102(a)(2). Raymond was neither cited nor considered during prosecution of the ’678 patent.

C. Claim Construction: 37 C.F.R. §42.104(b)(3)

Petitioners submit that no construction of any claim term is necessary for the Board to resolve, and the Challenged Claims would have been obvious under any reasonable construction.

D. Challenge: 37 C.F.R. §42.104(b)(4)

Explanation of how the Challenged Claims are unpatentable under the grounds identified above, including where each claim element is found in the prior art, is provided below.

E. Supporting Evidence: 37 C.F.R. §42.104(b)(5)

The supporting exhibits, their relevance to the challenged claims, and the specific portions supporting the asserted grounds are identified below. The Petition’s technical analysis and grounds are further supported by the Declaration of Dr. Ben Carrion Schaefer (Ex. 1003). The public availability of the cited prior art is further supported by the Declarations of Carrie Gardner (Ex. 1004), which further includes cites to the Declaration of Gordon MacPherson (Ex. 1011).

A List of Exhibits is included pursuant to 37 C.F.R. §42.63(e).

F. Payment of Fees: 37 C.F.R. §§42.103, 42.15(a)

The required fee was submitted. The Office is authorized to charge any fee deficiency, or credit overpayment, to Deposit Account 50-1408, including additional fees related to this Petition.

III. PERSON OF ORDINARY SKILL IN THE ART (“POSITA”)

A POSITA, on February 21, 2019, would have a Bachelor’s degree in Computer Engineering, Electrical Engineering, or equivalent discipline, and at least three years of academic or industry experience on clocking techniques for FPGAs with high-speed transceivers. Educational requirements may be substituted by work experience, and vice versa.

IV. STATE OF THE ART

By February 21, 2019, FPGA-based communication systems were highly developed, and components such as SERDESEs, PLLs, DLLs, CDRs, and phase-alignment mechanisms were standard FPGA features. Ex. 1001, 1:41–43; Ex. 1003, ¶88. Commercial user guides, such as Virtex-5 RocketIO GTP Transceiver User Guide (“Virtex-UG”), document many of these features. *Id.*

Commercial FPGA transceivers already implemented integrated serialization and deserialization using parallel-in/serial-out (PISO) and serial-in/parallel-out (SIPO) circuitry. Ex. 1009, 104; Ex. 1003, ¶88. The transceivers interfaced directly

with FPGA programmable logic through user-accessible clock and data interfaces, enabling custom processing of deserialized data. Ex. 1005, 194–95; Ex. 1003, ¶89.

1. Giordano

Giordano presents “a link architecture” using “GTP transceiver” of the “Xilinx Virtex 5 FPGA family.” Ex. 1005, 194. Giordano explains that transceivers are implemented as “configurable hard-macros (or ‘tiles’),” with each tile including a receiver and a transmitter. *Id.* Each receiver and transmitter has a Physical Medium Attachment (PMA) sublayer for serialization (in transmitter PMA) or deserialization (in receiver PMA), and a Physical Coding Sublayer (PCS) for processing data. *Id.*

Giordano also describes an FPGA Fabric with programmable hardware, which can implement user-programmed circuits such as “Comma Detect and Align” circuits and DLLs. *Id.*, 197–199. Figure 1 below shows Giordano’s architecture:

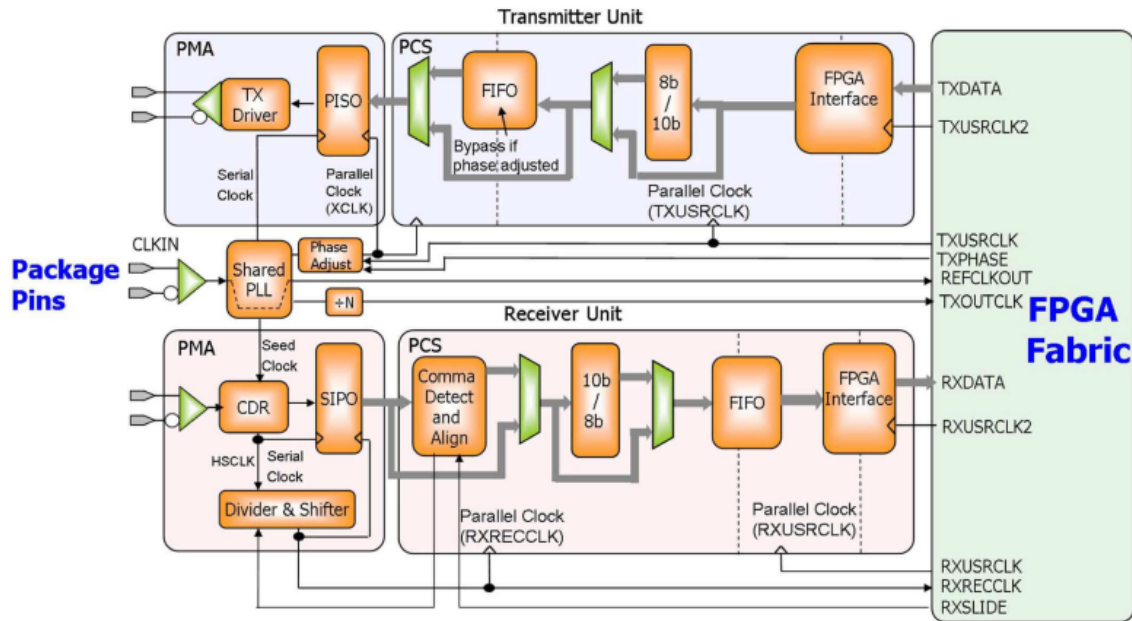


Fig. 1. Simplified block diagram of the GTP transceiver. Half a tile is shown.

2. Virtex-UG

Virtex-UG is Xilinx’s Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), dated December 3, 2009, hence publicly available before Giordano. Ex. 1009, 1; Ex. 1004, ¶¶41–47. Virtex-UG states that it “shows how to use the RocketIO™ GTP transceivers in Virtex®-5 FPGAs,” and describes the GTP transceiver as a power-efficient, highly configurable transceiver “tightly integrated with the programmable logic resources of the FPGA.” Ex. 1009, 17, 23. The GTP transceiver supports line rates from 100 Mb/s to 3.75 Gb/s, optional PCS features such as 8B/10B encoding, comma alignment, channel bonding, and clock correction, and “fixed latency modes for minimized, deterministic datapath latency.” *Id.*, 23. The guide also explains that GTP transceivers are placed as dual-transceiver GTP_DUAL tiles in Virtex-5 LXT and SXT devices, allowing two transceivers to

share a single PLL with the TX and RX functions of both, just how Giordano describes its use of the Virtex 5 FPGA. *Id.*, 24; Ex. 1005, 194.

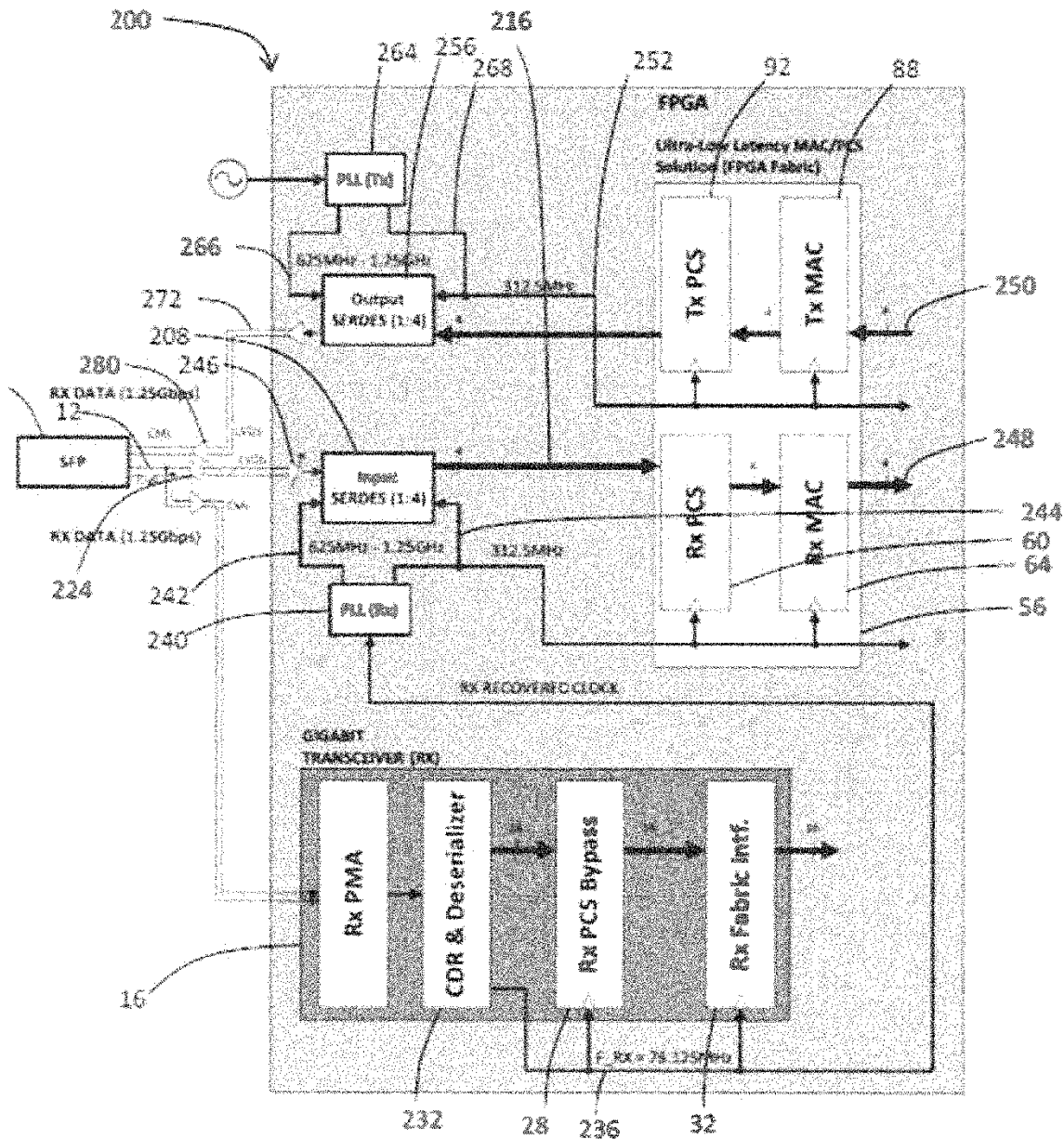
3. Lee

Lee (U.S. Pat. No. 8,788,553) discloses adjustable PLLs to accommodate different clocks for receivers and transmitters, with capabilities for frequency synthesis and phase shifting. Ex. 1008, 1:12–23. Lee addresses taking advantage of frequency aligned mode and phase aligned mode, separately and together for finer clock management. *Id.*, 2:35–55.

4. Raymond

Raymond (U.S. Pat. No. 10,447,463) explains that “[u]ltra-low latency communication is critical” for electronic trading and that trading firms use FPGAs to improve throughput and latency. Ex. 1007, 1:18–24. Raymond discusses processing incoming financial trading data, exchanged with financial exchanges. *Id.*, 4:52–59.

Raymond states that “prefabricated transceivers used to process incoming and outgoing physical layer signals” may be “replaced by low-latency serializer/deserializer modules” programmed by the FPGA. *Id.*, 4:43–47; 9:3–8 (“SerDes module” is “implemented using programmable logic”), 11:65–67. Raymond’s proposed solution is depicted in Figure 2:



V. OVERVIEW OF THE '678 PATENT

A. Summary of the Prosecution History of the '678 patent

The application for the '678 patent was filed July 23, 2020. During prosecution, the Examiner did not issue an Office Action rejecting the claims. Instead, during a January 21, 2021 examiner-initiated interview, the Examiner

identified possible double-patenting issues involving U.S. Pat. Nos. 10,771,069, 10,763,865, and 10,826,502, and U.S. Application No. 16/937,314, and Applicant indicated that electronic terminal disclaimers would be filed. Ex. 1002, 40. The Examiner then allowed claims 1–22. Ex. 1002, 38–39. The Notice of Allowability stated that the “communication was responsive to terminal disclaimers received 1/22/2021,” and that the “[t]erminal disclaimers have been filed and approved to obviate possible double patenting rejections involving the cited references” identified by the Examiner. *Id.* The Examiner further stated that “[n]one of the other cited references disclose each of the limitations recited in the claims.” *Id.*

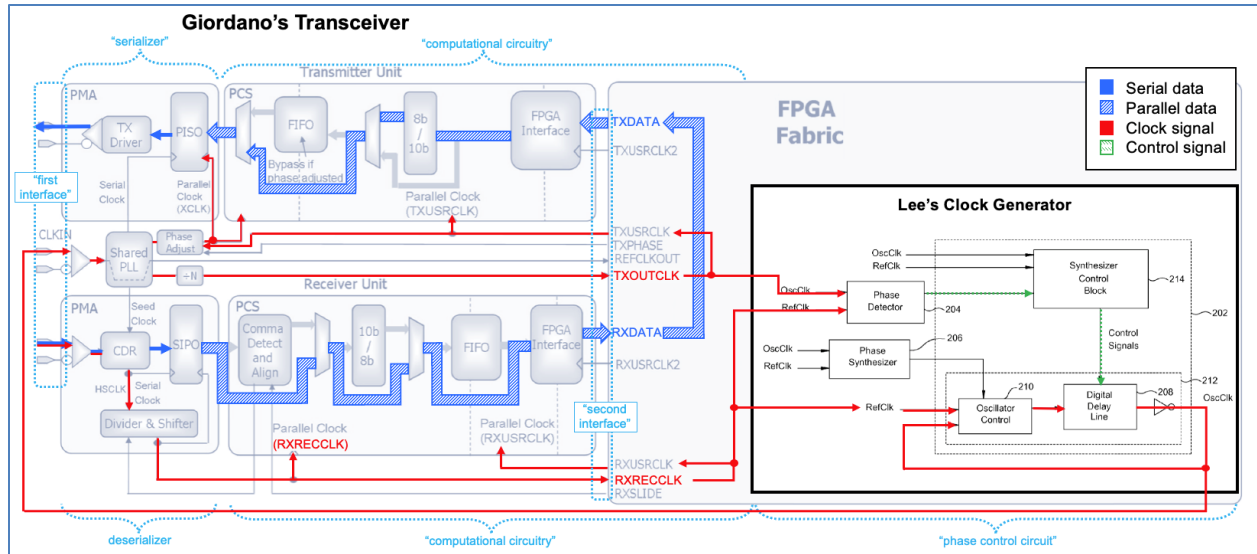
VI. GROUNDS FOR UNPATENTABILITY

A. Ground 1: Claims 1–20 Are Rendered Obvious by Giordano in View of Lee

1. Overview

Giordano’s FPGA comprises two portions—Xilinx Virtex-5 “RocketIO” GTP transceiver (with separate receiver and transmitter sides) and FPGA Fabric. Ex. 1005, 195. The GTP transceiver comprises preprogrammed, fixed (but configurable with operating parameters and settings by a user) hardware commonly referred to as hard-macro tiles. *Id.*, 194; Ex. 1003, ¶103. In contrast, FPGA Fabric comprises user-modifiable, programmable hardware. *Id.*

The annotated image below, based on Figure 1 of Giordano and Figure 2 of Lee with modifications, depicts this proposed combination:



Giordano's GTP transceiver generates a receiver side clock signal, **RXRECCLK**, from clock extracted from incoming serial data, and provides **RXRECCLK** to Lee's Clock Generator implemented in the FPGA Fabric. Ex. 1003, ¶106. The serializer, which includes Shared PLL of Giordano, generates a transmitter side clock signal **TXOUTCLK** and sends this to the Clock Generator. *Id.* The Clock Generator compares the phase of **RXRECCLK** and **TXOUTCLK**, and uses that information to generate a clock signal that is provided back to the **CLKIN** port of the GTP transceiver. *Id.* This results in **RXRECCLK** and **TXOUTCLK** being phase matched. *Id.*

a. Motivation to Combine Giordano and Lee

A POSITA would have been motivated to combine Giordano and Lee because they address synchronization and phase alignment of clock signals in FPGA transceivers. Ex. 1003, ¶107. Giordano seeks fixed-latency timing synchronization

and clock distribution in Xilinx GTP transceivers, while Lee discusses solutions for achieving “low output jitter of the frequency aligned mode along with the low phase error of the phase aligned mode.” Ex. 1005, 194; Ex. 1008, 2:35–55.

Giordano identifies the need that Lee’s teachings fulfill. While Giordano’s fixed-latency architecture achieves deterministic (*i.e.*, fixed) phase relationships between the receiver clock and transmit clock, Giordano identifies gaps for directly using this receiver clock for the transmitter. Ex. 1005, 198; Ex. 1003, ¶108.

Giordano states:

The clock recovered by the receiver cannot be directly used as a reference clock for the re-transmission. In fact, the internal PLL is shared among the transmitters and receivers in the same tile and at the receiver tile it is already locked to the seed clock. Moreover, the recovered clock might also require to be filtered in order to match the jitter specifications for the GTP reference clock.

Ex. 1005, 198. Lee provides precisely such a solution through a clock generator that filters jitter and phase matches the output to the input reference clock. Ex. 1008, 2:35–51, Fig. 2.

A POSITA reading Giordano would have naturally consulted Xilinx’s own materials (such as Lee, a Xilinx patent), for a phase alignment solution. Giordano repeatedly references the Xilinx RocketIO GTP Transceiver User Guide and Lee is a Xilinx patent, hence both are within the Xilinx FPGA infrastructure. Ex. 1005, 194, 197–199; Ex. 1008, Cover.

Incorporating Lee's Clock Generator teachings into Giordano would require only programming existing FPGA Fabric logic. Ex. 1003, ¶110.

Giordano itself demonstrates programming custom hardware in the FPGA Fabric. For example, Giordano implemented a custom Comma Detector and Aligner in the FPGA Fabric because the GTP's built-in comma detector (which is a fixed block inside the transceiver) operated only in unsupported modes. Ex. 1005, 198; Ex. 1003, ¶110. Giordano also discloses implementing DLL blocks "external to the GTP" transceiver, *i.e.*, on the FPGA Fabric. Ex. 1005, Fig. 5; Ex. 1003, ¶110. Implementing Lee's Clock Generator in the FPGA Fabric thus represents a straightforward extension of techniques already used in Giordano. Ex. 1003, ¶110.

Similarly, Lee also discusses implementing its clock generating teachings "using components that are all digital." Ex. 1008, 2:35–37, 4:31–35. A POSITA would have understood this to support implementing Lee's teachings on programmable logic such as on Giordano's FPGA Fabric. Ex. 1003, ¶110.

Such FPGA hardware programming is how the '678 patent suggests implementing its claimed invention, which programs components such as phase detector, phase controller, DLL, and PLL in a "FPGA Core," mirroring Giordano's FPGA Fabric. Ex. 1001, Figs. 3A–F, 4A–C, 5A–F, 26:38–56; Ex. 1003, ¶111.

A POSITA would have had a reasonable expectation of success. Giordano's FPGA implementation was physically tested on Xilinx evaluation boards and used

circuit blocks similar to those disclosed in Lee, including PLLs, DLLs, serializers, and pattern generators which were implemented on the programmable FPGA Fabric as the user intended. Ex. 1005, 195, 197–200; Ex. 1008, 2:56–3:15; Ex. 1003, ¶112. Because both references rely on the same Xilinx FPGA infrastructure, there would have been high expectations that, through routine FPGA programming, the combination functions as intended. *Id.*

b. Features of Virtex-UG are Inherent to Giordano, and Giordano Incorporates Virtex-UG by Reference

Giordano presents a system with the “RocketIO” GTP transceiver of the Xilinx Virtex 5 FPGA family. Ex. 1005, 194, 199. Giordano repeatedly references the RocketIO GTP Transceiver, for example referencing the overall transceiver architecture (*id.*, 195) and taking estimated latency values from the RocketIO GTP Transceiver User Guide (*id.*, 198). Giordano further describes phase alignment of clock signals, and that “the procedure we follow for activating the alignment circuit is the one suggested in the GTP user’s guide.” *Id.*, 197. A POSITA would have known to reference Xilinx documents on the GTP transceiver to understand the relevant inherent features. Ex. 1003, ¶113. As such, Giordano inherently discloses the features of Virtex-UG. *Id.*

In such case, the features of the Virtex-UG are necessarily present in Giordano, and it is proper to use extrinsic evidence (such as the Virtex-UG) to understand said features. *See Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247

F.3d 1316, 1328 (Fed. Cir. 2001) (“[R]ecourse to extrinsic evidence is proper to determine whether a feature, while not explicitly discussed, is necessarily present in a reference. The evidence must make clear that the missing feature is necessarily present, and that it would be so recognized by persons of ordinary skill in the relevant art.”); *Sage Prods., LLC v. Stewart*, 133 F.4th 1376, 1385 (Fed. Cir. 2025) (“There was likewise nothing improper in the Board relying on evidence outside of the PAR to make findings as to what the skilled artisan would understand the PAR to be disclosing.”); *Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1345 (Fed. Cir. 2018) (“It is well established that such reliance on extrinsic evidence is proper in an inherency analysis.”); *see also In re Haines*, No. 2024-2338, 2025 WL 1403578, at *2 (Fed. Cir. May 15, 2025) (examiner properly used another publication “as evidence to explain why [the prior art’s] disclosure of a mass spectrometer implicitly discloses ‘obtaining mass spectral channel signals (m/z)’” (cleaned up)).

For the same reasons as above, Giordano incorporates Virtex-UG (Ex. 1009) by reference. Ex. 1005, 197 (“the procedure we follow for activating the alignment circuit is the one suggested in the GTP user’s guide.”). Virtex-UG, by incorporation, becomes part of the disclosures of Giordano. *Verizon Connect Inc. v. Omega Patents, LLC*, IPR2023-01162, 2024 WL 714951, at *3, 14-15 (P.T.A.B. Feb. 21, 2024) (the incorporated secondary reference’s disclosures become part of the

primary reference); *Paice LLC v. Ford Motor Co.*, 881 F.3d 894, 906-07 (Fed. Cir. 2018) (“[T]he standard of one reasonably skilled in the art should be used to determine whether the host document describes the material to be incorporated by reference with sufficient particularity.”) (citing *Advanced Display Systems, Inc. v. Kent State University*, 212 F.3d 1272 (2000)).

2. Analysis

a. Independent Claim 1

[1.pre]: 1. A field programmable gate array system, comprising:

To the extent limiting, Giordano discloses [1.pre]. Ex. 1003, ¶114.

Giordano discloses Xilinx Virtex-5 FPGA on FPGA boards for experimentally testing its proposed architecture. Ex. 1005, 198. FPGA board, where the FPGA is physically installed in, discloses the claimed “[FPGA] system.” Ex. 1003, ¶114.

[1.a]: (a) a field programmable gate array comprising

Giordano discloses Xilinx Virtex-5 FPGA, which discloses the claimed “field programmable gate array.” Ex. 1005, 194; Ex. 1003, ¶115.

[1.b]: (1) a first interface comprising

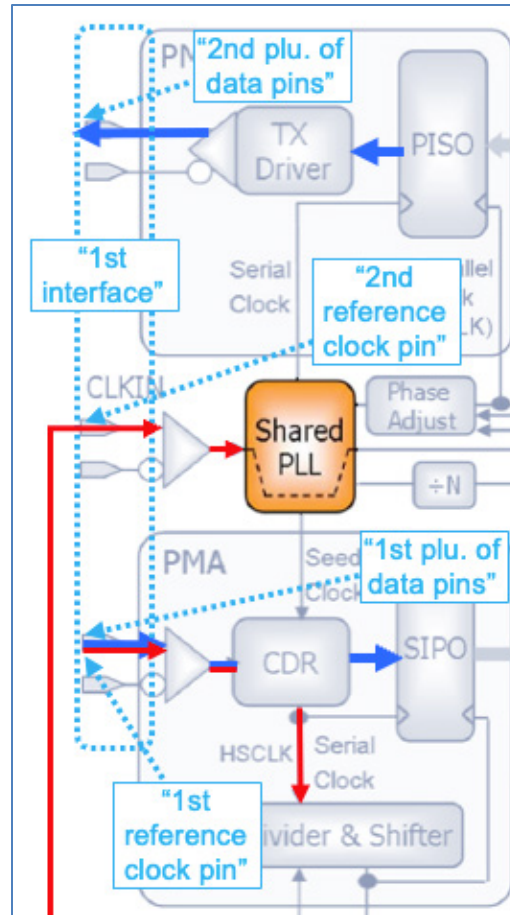
(A) a first reference clock pin, wherein said first reference clock pin is configured to receive a first clock signal having a first frequency and a first phase;

(B) a second reference clock pin, wherein said second reference clock pin is configured to receive a second clock signal having a second frequency and a second phase;

(C) a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream;

(D) a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream;

Giordano discloses [1.b]. Ex. 1003, ¶116. The image below, based on Giordano Figure 1 with additional annotations, shows the portions of the Giordano-Lee combination relevant to the claimed “first interface”:



For “first interface,” Giordano’s FPGA package pins, which interface external signals with the FPGA, disclose the “first interface.” Ex. 1005, 195; Ex. 1003, ¶117.

Giordano discloses the GTP transceiver, which includes separate “Receiver Unit” and “Transmitter Unit.” Ex. 1005, 194. Within each receiver- and transmitter-unit are a Physical Medium Attachment (“PMA”) and Physical Coding Sublayer (“PCS”). *Id.*, 194–195. Giordano points to the PMA sublayer as the component “actually serializing and de-serializing the data,” and the PCS layer as “processing” data. *Id.*, 194.

Giordano discloses package pins that interface both Receiver Unit PMA and Transmitter Unit PMA with external components, which disclose the claimed “first interface.” Ex. 1005, Fig. 1; Ex. 1003, ¶119.

For “first reference clock pin,” Giordano’s FPGA pin into the Receiver Unit PMA, specifically that for the signal from which HSCLK is recovered, discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶120.

Giordano’s Receiver Unit PMA has a Clock and Data Recovery (“CDR”) block, “which extracts a clock (HSCLK)” from the incoming serial data stream. Ex. 1005, 195. HSCLK discloses the “first clock signal,” and also “first frequency” and “first phase.” Ex. 1003, ¶121. The package pin that receives this incoming signal discloses “first reference clock pin.”

This mirrors the ’678 patent, which describes a receiver PMA further comprising a CDR block. Ex. 1001, 53:21–24, Fig. 6E. Like Giordano, the CDR block of the ’678 patent receives serial data, and extracts a clock signal from the incoming serial data. Ex. 1001, 53:27–37.

For “second reference clock pin,” Giordano’s FPGA pin for CLKIN into the Shared PLL discloses this limitation. Ex. 1005, 197; Ex. 1003, ¶122. In the proposed combination, this CLKIN pin is connected to the output of Lee’s Clock Generator. *Id.* This CLKIN signal discloses the “second clock signal,” and also “second frequency” and “second phase.” Ex. 1005, Fig. 1; Ex. 1003, ¶122.

For “first plurality of data pins,” Giordano discloses package pins that interface the Receiver Unit PMA with external components, which disclose the claimed “first plurality of data pins.” Ex. 1005, Fig. 1; Ex. 1003, ¶123. This Receiver Unit PMA receives incoming serial data, which discloses the “first serial data stream.” Ex. 1005, 195; Ex. 1003, ¶123.

This mirrors the ’678 patent, which describes a deserializer with a receiver PMA. Ex. 1001, 53:21–24, Fig. 6E.

For “second plurality of data pins,” Giordano’s FPGA pins out from the Transmitter Unit PMA discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶124.

Giordano’s Transmitter Unit PMA discloses a Parallel Input to Serial Output (“PISO”) block that converts parallel data to serial data. Ex. 1005, 195; Ex. 1003, ¶125. The serial data output of PISO discloses the “second serial data stream.” *Id.* This output is sent to the transmitter driver, which is then sent outside the FPGA through package pins. Ex. 1005, Fig. 1; Ex. 1003, ¶125.

This mirrors the ’678 patent, which describes a serializer with a transmitter PMA with a Parallel to Serial block. Ex. 1001, 53:65–54:18, Fig. 7B. Like Giordano, this Parallel to Serial block converts the incoming parallel data to serial data. *Id.*

[1.c]: (2) a deserializer operationally connected to

(A) the first reference clock pin to receive as a first input the first clock signal and

(B) the first plurality of data pins to receive as a second input the first serial data stream, and

Giordano's Receiver Unit PMA discloses the claimed "deserializer." Ex. 1003, ¶126.

For "as a first input", Giordano's Receiver Unit PMA has a Clock and Data Recovery ("CDR") block, "which extracts a clock (HSCLK)" from the incoming serial data stream. Ex. 1005, 195. As such, HSCLK is sent with the serial data from the package pins to this CDR, which discloses receiving "as a first input" HSCLK (*i.e.*, "first clock signal"). *Id.*; Ex. 1003, ¶127.

This mirrors the '678 patent, which describes a deserializer with a receiver PMA. Ex. 1001, 53:21–24, Fig. 6E. This receiver PMA further comprises a CDR block. *Id.* Like Giordano, the CDR block of the '678 patent receives serial data, and extracts a clock signal from the incoming serial data. Ex. 1001, 53:27–37.

For "as a second input", Giordano's Receiver Unit PMA includes a "Serial In to Parallel Output (SIPO)" block, which deserializes incoming serial data. Ex. 1005, 195–196; Ex. 1003, ¶129. The package pins transmit the incoming serial data to the Receiver Unit PMA, which discloses receiving "as a second input" incoming serial data (*i.e.*, "first serial data stream"). Ex. 1005, 195, Ex. 1003, ¶129.

This mirrors the '678 patent, which describes a receiver PMA that receives serial data. Ex. 1001, 53:20–37, Fig. 6E.

[1.d]: wherein the deserializer is configured to

(i) convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams;

(ii) generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase; and

(iii) transmit the first plurality of parallel data streams and the first receiver side clock signal within the field programmable gate array;

As discussed in [1.c], Giordano's Receiver Unit PMA discloses the claimed "deserializer."

For sub-element (i), as discussed in [1.b], the serial data into Giordano's Receiver Unit PMA discloses the "first serial data stream."

Giordano's SIPO block output discloses the "first plurality of parallel data streams," and the output's data size discloses the "first amount of data streams." Ex. 1003, ¶131.

Giordano's Receiver Unit PMA has a SIPO block that converts incoming serial data to parallel data, which discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶132. Giordano's SIPO block output, further processed by the Receiver Unit PCS, discloses the "first plurality of parallel data streams" (where the bit size of said parallel data discloses "first amount of data streams"). Ex. 1005, 195; Ex. 1003, ¶132.

This mirrors the '678 patent, which describes a Serial to Parallel block within the Receiver PMA that “converts the serial data into parallel data, transmitting the parallel data to the receiver PCS.” Ex. 1001, 53:33–37, Fig. 6E.

For sub-element (ii), as discussed in [1.b], HSCLK discloses the “first clock signal.”

Giordano’s parallel recovered clock (RXRECCLK) discloses the “first receiver side clock signal.” Ex. 1003, ¶133. RXRECCLK discloses the “third frequency” and “third phase.” *Id.*

The CDR in Giordano’s Receiver Unit PMA extracts a clock (HSCLK) signal from the incoming serial data. Ex. 1005, 195. HSCLK is then used to “generate a parallel recovered clock (RXRECCLK)” for the SIPO block and Receiver Unit PCS. *Id.*; Ex. 1003, ¶134. This RXRECCLK discloses the claimed “receiver side clock signal,” and the frequency and phase of RXRECCLK discloses the claimed third frequency and phase. *Id.*

This mirrors the '678 patent, which describes a CDR that receives serial data, and generates clock signals for blocks such as Serial to Parallel and receiver PCS. Ex. 1001, 53:27–37, Fig. 6E.

For sub-element (iii), Giordano discloses this limitation. Ex. 1003, ¶135.

Giordano discloses providing RXRECCLK (*i.e.*, “receiver side clock signal”) to the Receiver Unit PCS and FPGA Fabric. Ex. 1005, 195; Ex. 1003, ¶135.

Giordano discloses providing the SIPO block output to be further processed by PCS (both receiver and transmitter sides) and logic implemented on FPGA Fabric. Ex. 1005, 195, Fig. 1; Ex. 1003, ¶135.

[1.e]: (3) computational circuitry operationally connected to the deserializer to receive the first plurality of parallel data streams and the first receiver side clock signal, wherein the computational circuitry is configured to perform a first set of operations on the first plurality of parallel data streams to generate a second plurality of parallel processed data streams having a second amount of data streams and the computational circuitry performs the first set of operations to generate the second plurality of parallel processed data without use of a clock domain crossing circuit;

Giordano discloses [1.e]. Ex. 1003, ¶137.

As discussed in [1.c] and [1.d], Giordano's Receiver Unit PMA discloses the claimed "deserializer," SIPO block output discloses the "first plurality of parallel data streams," and parallel recovered clock (RXRECCLK) discloses the "first receiver side clock signal."

Giordano's Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS individually and collectively disclose the "computational circuitry" and this limitation. Ex. 1003, ¶139. These blocks, as seen in the proposed combination image, receive deserialized parallel data from the SIPO block (which is within the Receiver Unit PMA, *i.e.*, "deserializer") and are along the data path between the receiver side SIPO and transmitter side PISO, hence are "operationally connected" to the "deserializer." *Id.*

Giordano's processed parallel data exiting the Transmitter Unit PCS into the Transmitter Unit PMA discloses the "second plurality of parallel processed data streams" (where the bit size of said parallel data discloses "second amount of data streams"). Ex. 1005, Fig. 1; Ex. 1003, ¶140.

For "first set of operations," Giordano discloses logic operations in the FPGA Fabric and the PCS layers (both receiver and transmitter). Giordano's Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS individually and collectively disclose the "computational circuitry." Ex. 1003, ¶141.

Giordano points to the PCS layer (both receiver and transmitter sides) as "processing" data, disclosing computational circuitry. Ex. 1005, 194; Ex. 1003, ¶142. The PCS layer includes optional 8b/10b encoding / decoding functions, which require arithmetic calculations hence disclosing "first set of operations." Ex. 1005, 197; Ex. 1003, ¶142.

Giordano also describes FPGA Fabric as including "logic," which discloses this limitation. Ex. 1005, 195–196, 198; Ex. 1003, ¶143. Giordano describes programming a Comma Detector and Aligner in the FPGA Fabric, which performs "comma detection." Ex. 1005, 198; Ex. 1003, ¶143. Giordano's "comma detector looks for commas (*e.g.*, the one included in the K28.5 symbol) and when it finds one it determines how many bit shifts" are "required in order to align the parallel data." Ex. 1005, 198; Ex. 1003, ¶143. A POSITA would have understood this pattern

matching operation (to locate comma characters) and computing number of bit shifts for alignment to disclose the claimed “first set of operations.” *Id.*

This mirrors the ’678 patent, with figures depicting computational circuitry capable of performing a logical operation as “Computation Logic.” Ex. 1001, Figs. 4B–C, 5A–F.

For “second plurality of parallel processed data streams,” Giordano’s Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS process parallel data, which is then transmitted from the Transmitter Unit PCS into the Transmitter Unit PMA. This processed parallel data discloses this limitation. Ex. 1005, Fig. 1; Ex. 1003, ¶144.

For “without use of a clock domain crossing circuit,” Giordano discloses this requirement. Ex. 1003, ¶145.

Giordano discloses bypassing First In First Out (FIFO) buffer, a circuit block allowing safe data transfer between different clock domains (*e.g.*, “data transfers between TXUSRCLK domain and the XCLK domain”). Ex. 1005, 195; Ex. 1003, ¶146. A POSITA would have understood FIFO as a clock domain crossing circuit, and Giordano’s bypassing of the FIFO block discloses this limitation. *Id.*

Giordano discloses bypassing FIFO buffer by having the two clock domains have “the same phase” and “therefore also the same latency for the data.” Ex. 1005, 195; Ex. 1003, ¶146. In the transmitter, Giordano discusses two clocks (XCLK and

TXUSRCLK) that are adjusted to have the same frequency and phase. Ex. 1005, 195. The transmitter has a FIFO block for crossing between XCLK and TXUSRCLK clock domains. *Id.*; Ex. 1003, ¶146. Giordano discloses bypassing this FIFO block by using a phase alignment option provided in Xilinx Virtex-5 FPGA systems. Ex. 1005, 195; Ex. 1003, ¶146. Through this built-in phase alignment, XCLK and TXUSRCLK are phase aligned, in which “the transmit FIFO is unnecessary and therefore we bypassed it.” Ex. 1005, 197.

Virtex-UG further discloses⁵ this limitation. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses this limitation. Ex. 1003, ¶147.

In the receiver, Virtex-UG confirms this FIFO bypass. When receiver clock phase alignment is used, “RXUSRCLK must be driven directly from RXRECCLK using a BUFR regional clock buffer.” Ex. 1009, 179 (“Using RX Phase Alignment to Bypass the RX Elastic Buffer”). Due to phase alignment, “SIPO parallel clock phase matches RXUSRCLK phase” and there is “no phase difference between XCLK and RXUSRCLK.” *Id.*, 180. With no phase difference, the RX Elastic Buffer (which is the FIFO block described in Giordano) is bypassed. This bypass is described in the red arrow below in Figure 7-22 of Virtex-UG:

⁵ The Virtex-UG’s disclosures discussed in this Petition are express. In addition, Giordano inherently discloses Virtex-UG’s express disclosures.

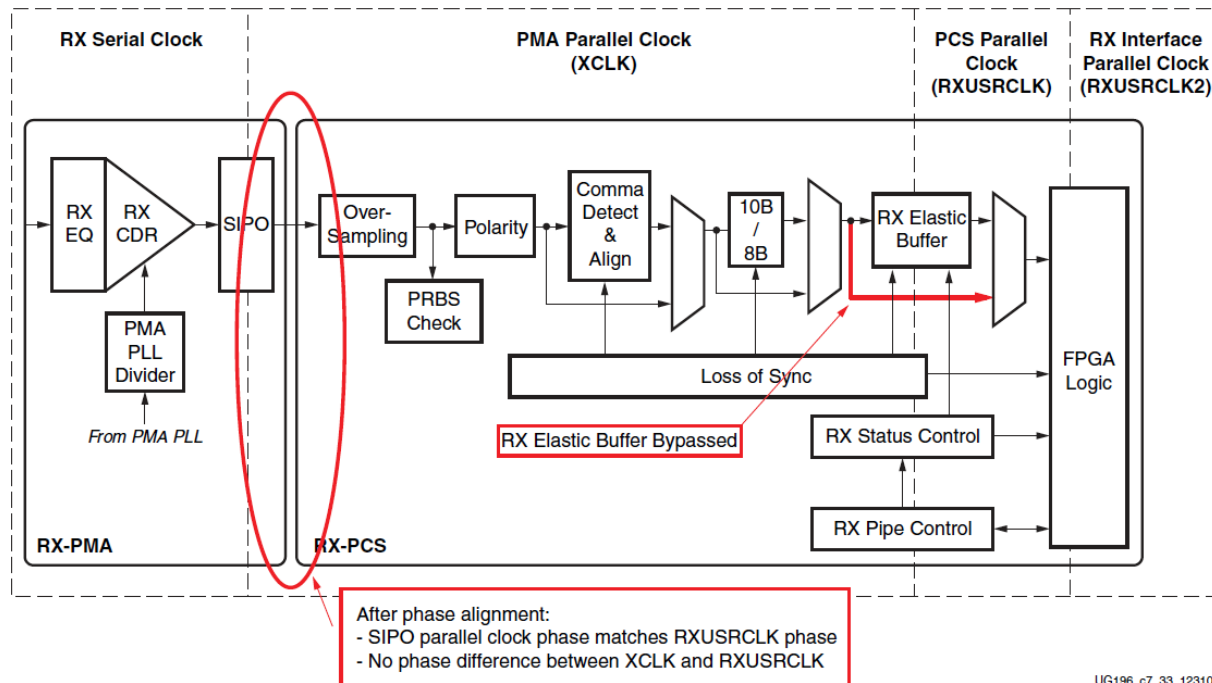


Figure 7-22: Using Phase Alignment

The bypass of all clock domain crossing circuits after phase alignment of clock signals, as disclosed in Giordano, discloses this limitation. Ex. 1003, ¶148.

[1.f]: (4) a serializer operationally connected to

(i) a transceiver phase lock loop to receive as a third input a first wire rate clock signal based on the second clock signal, wherein the first wire rate clock signal has a fourth frequency and a fourth phase;⁶

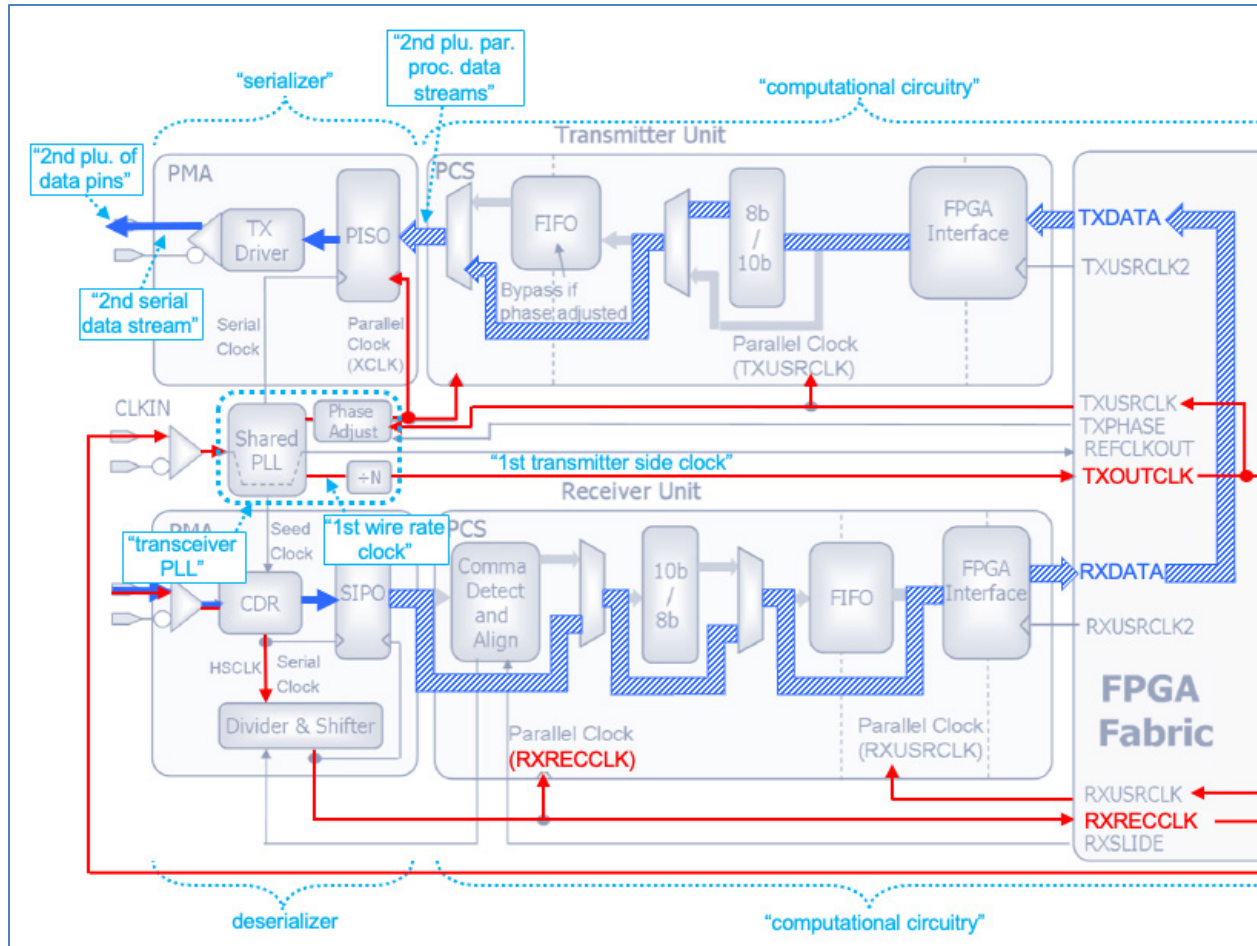
(ii) the second plurality of data pins to transmit as a first output the second serial data stream; and

(iii) the computational circuitry, wherein the serializer receives the second plurality of parallel processed data streams from the computational circuitry and the serializer transmits to the computational circuitry a first transmitter side clock signal including a fifth frequency and a fifth phase, and

Giordano's Transmitter Unit PMA with the Shared PLL discloses the claimed "serializer." Ex. 1003, ¶149.

The annotated image below, based on Giordano Figure 1, shows relevant portions of the Giordano-Lee combination, with a table summarizing relevant mappings:

⁶ Regarding "first wire rate clock signal," claim 12, which depends from claim 1, requires the "transceiver phase lock loop" be configured to *generate* said "first wire rate clock signal." Ex. 1001, cl. 12. Here, this limitation requires that "transceiver phase lock loop" *receive* the "first wire rate clock signal." Since the scope of claim 1 encompasses that of claim 12, Petitioners understand that a "transceiver phase lock loop" which both receives and generates (using different sub-components) the "first wire rate clock signal" discloses this limitation.



Claim Limitation	Disclosures
"serializer"	Giordano's Transmitter Unit PMA and Shared PLL collectively
"transceiver PLL"	Giordano's Shared PLL, Phase Adjustment Circuit, and Divider ("÷N") collectively
"first clock signal" (with first frequency and phase)	Giordano's HSCLK
"second clock signal" (with second frequency and phase)	Giordano's CLKIN (connected to the output of Lee's Clock Generator using GREFCLK mode). <i>Infra</i> , [1.m].
"first receiver side clock signal" (with third frequency and phase)	Giordano's RXRECCLK

“first wire rate clock signal” (with fourth frequency and phase)	Giordano’s Shared PLL output to Divider (“÷N”)
“first transmitter side clock signal” (with fifth frequency and phase)	Giordano’s TXOUTCLK

As discussed in [1.b] and [1.e], Giordano’s FPGA pins out from the Transmitter Unit PMA discloses “second plurality of data pins,” with the exiting data disclosing “second serial data stream,” Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS individually and collectively disclose “computational circuitry,” and processed parallel data exiting the Transmitter Unit PCS into the Transmitter Unit PMA discloses “second plurality of parallel processed data streams.”

For sub-element (i), Giordano’s Shared PLL, phase adjustment circuit, and divider together disclose the “transceiver [PLL],” and an output of the Shared PLL discloses “first wire rate clock signal” (and also “fourth frequency” and “fourth phase”). Ex. 1003, ¶152.

Giordano’s Shared PLL generates clock signals based on incoming signals, including one that is provided through the CLKIN port. Ex. 1005, Fig. 1; Ex. 1003, ¶153. One of these output clock signals is provided to a divider (depicted with “÷N”), where this divider generates TXOUTCLK. Ex. 1005, Fig. 1; Ex. 1003, ¶153. The clock signal going into this divider discloses “first wire rate clock signal.” Ex. 1003, ¶153.

This mirrors the '678 patent, which describes a divider for adjusting the frequency of a clock signal. Ex. 1001, 29:20–26, 52:1–13. Like Giordano, this divider outputs a “lower-frequency” signal, from dividing the input signal by a user-settable number. Ex. 1001, 52:36–46; Ex. 1003, ¶153.

For sub-element (ii), Transmitter Unit PMA in Giordano has a TX Driver that sends out serial data, which discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶154. Giordano’s package pins interfacing Transmitter Unit PMA with external components disclose the claimed “second plurality of data pins.” Ex. 1005, Fig. 1; Ex. 1003, ¶154. This Transmitter Unit PMA transmits processed serial data, *i.e.*, “second serial data stream.” Ex. 1005, 195; Ex. 1003, ¶154.

This mirrors the '678 patent, which describes a Transmitter PMA with a Transmitter Buffer that sends out serial data. Ex. 1001, 53:65–54:18, Fig. 7B.

For sub-element (iii), Giordano’s TXOUTCLK discloses “first transmitter side clock signal,” and also the “fifth frequency” and “fifth phase.” Ex. 1003, ¶155.

Giordano discloses PISO block in the Transmitter Unit PMA (of the “serializer”) receiving parallel data (“second plurality of parallel processed data streams”) from the Transmitter Unit PCS (of the “computational circuitry”). Ex. 1005, Fig. 1.

In the proposed combination, the Shared PLL (of the “serializer”) transmits to the FPGA Fabric (of the “computational circuitry”) the TXOUTCLK signal (“first transmitter side clock signal”) through a divider block “÷N.” Ex. 1005, Fig. 1.

[1.g] wherein the serializer is configured to:

- a. convert the second plurality of parallel processed data streams into the second serial data stream;**
- b. generate the first transmitter side clock signal based on the first wire rate signal, wherein the first transmitter side clock signal has the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency; and**
- c. transmit the second serial data stream to the second plurality of data pins for transmission off the field programmable gate array;**

As discussed in [1.f], Giordano’s Transmitter Unit PMA with the Shared PLL discloses the claimed “serializer.”

For sub-element a., as discussed in [1.b] and [1.e], serial data output of PISO discloses the “second serial data stream,” and the parallel data from the Transmitter Unit PCS into the Transmitter Unit PMA discloses “second plurality of parallel processed data streams.”

Giordano’s PISO block converts parallel data (“second plurality of parallel processed data streams”) to serial data (“second serial data stream”). Ex. 1005, 195; Ex. 1003, ¶156.

This mirrors the ’678 patent, which describes a serializer with a transmitter PMA with a Parallel to Serial block. Ex. 1001, 53:65–54:18, Fig. 7B. Like

Giordano, this Parallel to Serial block converts the incoming parallel data to serial data. *Id.*

For sub-element b., as discussed in [1.f], Giordano's TXOUTCLK discloses "first transmitter side clock signal," and the output of the Shared PLL going into the divider discloses "first wire rate clock signal."

Giordano discloses a divider (depicted with " $\div N$ ") that generates TXOUTCLK ("first transmitter side clock signal") based on a signal from the Shared PLL ("first wire rate clock signal"). Ex. 1005, Fig. 1; Ex. 1003, ¶158.

This mirrors the '678 patent, which describes a divider for adjusting the frequency of a clock signal. Ex. 1001, 29:20–26, 52:1–13. Like Giordano, this divider outputs a "lower-frequency" signal, from dividing the input signal by a user-settable number. Ex. 1001, 52:36–46; Ex. 1003, ¶158.

Giordano discloses using clock dividers of " $\div 5$ " for the receiver clock divider. Ex. 1005, Fig. 3. A POSITA would have known to use the " $\div 5$ " divider, explicitly used for the receiver side, for the " $\div N$ " block on the transmitter side. Ex. 1003, ¶159. This results in Giordano's Shared PLL output ("first wire rate clock") to have a frequency five times that of TXOUTCLK. Ex. 1003, ¶159. Hence the Shared PLL output ("first wire rate clock") would have a frequency five times that of Clock Generator output ("second clock signal"), disclosing this limitation. *Id.*

For sub-element c., Transmitter Unit PMA in Giordano has a TX Driver that sends out serial data, which discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶160. Giordano's package pins interfacing Transmitter Unit PMA with external components disclose the claimed "second plurality of data pins." Ex. 1005, Fig. 1; Ex. 1003, ¶160. This Transmitter Unit PMA transmits processed serial data, *i.e.*, "second serial data stream." Ex. 1005, 195; Ex. 1003, ¶160.

This mirrors the '678 patent, which describes a Transmitter PMA with a Transmitter Buffer that sends out serial data. Ex. 1001, 53:65–54:18, Fig. 7B.

[1.h]: (5) a second interface comprising

(i) a first clock output pin configured to transmit the first receiver side clock signal, wherein the first clock output pin is operationally connected to the deserializer; and

(ii) a second clock output pin configured to transmit the first transmitter side clock signal, wherein the second clock output pin is operationally connected to the serializer; and

Giordano discloses this limitation. Ex. 1003, ¶165. As discussed in [1.c], Giordano's Receiver Unit PMA discloses the claimed "deserializer," and in [1.f], Giordano's Transmitter Unit PMA with the Shared PLL discloses the claimed "serializer." As discussed in [1.d] and [1.g], Giordano's parallel recovered clock (RXRECCLK) discloses the "first receiver side clock signal" and TXOUTCLK discloses "first transmitter side clock signal."

The interface between Giordano's PCS (both receiver and transmitter sides) and FPGA Fabric discloses the "second interface." Ex. 1005, Fig. 1; Ex. 1003, ¶165.

For sub-element (i), the connection between Giordano's Receiver Unit PCS and the FPGA Fabric discloses the claimed "first clock output pin." Ex. 1005, Fig. 1; Ex. 1003, ¶162. This connection includes that for RXRECCLK ("first receiver side clock signal"), which is transmitted from the Receiver Unit PMA ("deserializer") into the FPGA Fabric. Ex. 1005, Fig. 1; Ex. 1003, ¶162. The clock path for RXRECCLK connects the Receiver Unit PMA ("deserializer") and FPGA Fabric, hence discloses the "operationally connected" limitation. Ex. 1005, Fig. 1; Ex. 1003, ¶162.

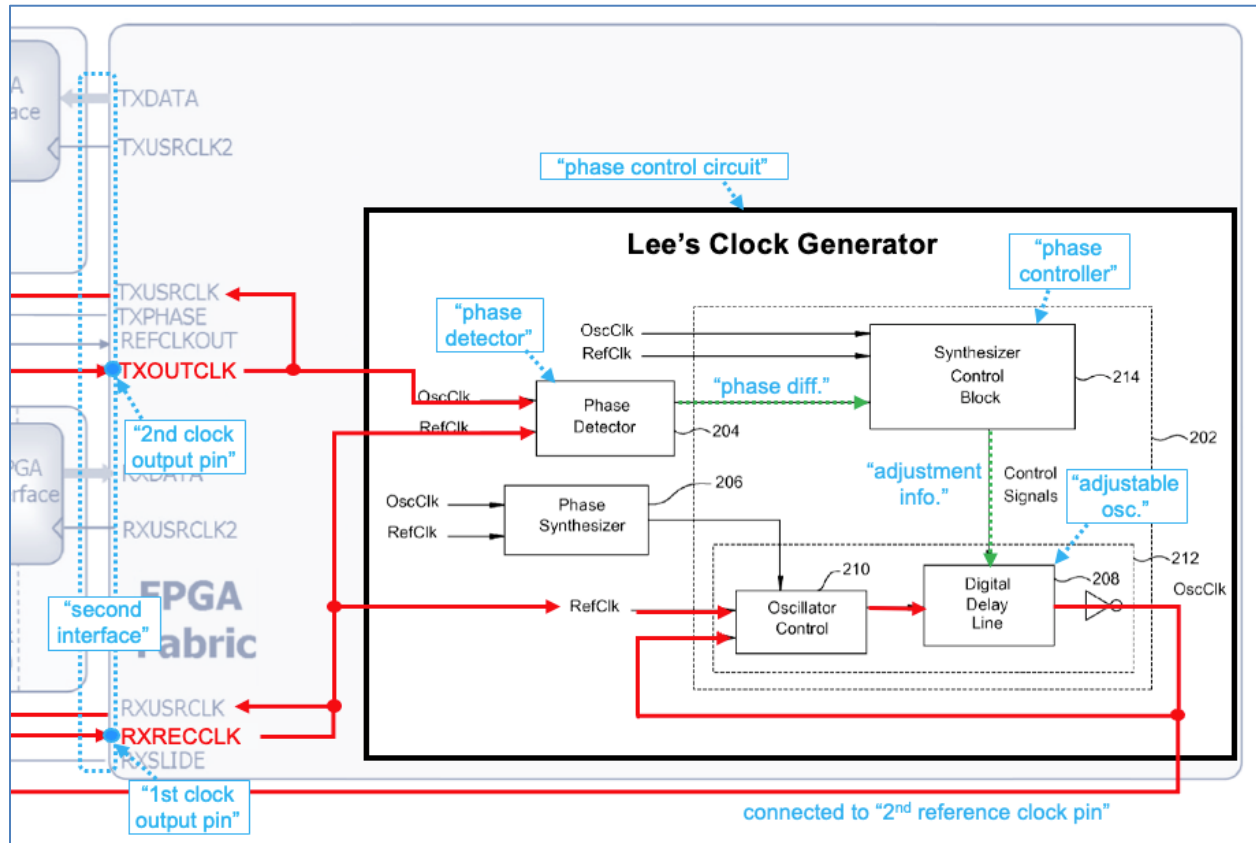
For sub-element (ii), the connection between Giordano's Shared PLL / divider and the FPGA Fabric discloses the claimed "second clock output pin." Ex. 1005, Fig. 1; Ex. 1003, ¶163. This connection includes that for TXOUTCLK ("first transmitter side clock signal"), which is transmitted from the Shared PLL ("serializer") into the divider " $\div N$ " block, then into the FPGA Fabric. Ex. 1005, Fig. 1; Ex. 1003, ¶163. The clock path for TXOUTCLK connects the Shared PLL ("serializer") and FPGA Fabric, hence discloses the "operationally connected" limitation. Ex. 1005, Fig. 1; Ex. 1003, ¶163.

[1.i] (b) a phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises:

Lee discloses this limitation. Ex. 1003, ¶163.

Lee's Clock Generator implemented in the FPGA Fabric, hence on the FPGA, discloses "phase control circuit." Ex. 1008, Fig. 2; Ex. 1003, ¶163.

The image below shows the portions of the Giordano-Lee combination relevant to the claimed “phase control circuit,” with additional annotations:



[1.j]: (1) a phase detector operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array, and

wherein the phase detector is configured to compare the third phase of the first receiver side clock signal to the fifth phase of the transmitter side clock signal and to generate a phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the fifth phase of the transmitter side clock signal;

Lee discloses this limitation. Ex. 1003, ¶165. As discussed in [1.h], the FPGA Fabric clock paths for RXRECCLK discloses the “first clock output pin” and that for TXOUTCLK discloses the “second clock output pin.”

Lee's Phase Detector 204 discloses the claimed "phase detector," which takes in RXRECCLK and TXOUTCLK as input and hence "operationally connected" to the two output pins of the "second interface." Ex. 1008, Fig. 2; Ex. 1003, ¶166.

Lee discloses Phase Detector 204 sending a control signal based on the measured phase difference between RXRECCLK (with "third phase") and TXOUTCLK (with "fifth phase") to Synthesizer Control Block 214 for adjusting the generated clock. Ex. 1008, 3:16–31; Ex. 1003, ¶166. Lee further discloses an iterative process until the two input clocks are phase aligned (Ex. 1008, 1:30–35, 3:16–24), through the feedback loop depicted in the annotated image above in [1.i] (based on Lee Figure 2). This signal to the Synthesizer Control Block 214 discloses the claimed "phase difference indicator signal." Ex. 1003, ¶166. The relationships between the aforementioned signals disclose this limitation. *Id.*

[1.k]: (2) a phase controller operationally connected to the phase detector and configured to receive the phase difference indicator signal, wherein the phase controller is configured to determine adjustment information based on the phase difference indicator signal; and

Lee discloses this limitation. Ex. 1003, ¶167. As discussed in [1.j], Lee's Phase Detector 204 discloses the claimed "phase detector" and its output discloses "phase difference indicator signal."

Lee's Synthesizer Control Block 214 discloses the claimed "phase controller," which takes in the output from the Phase Detector 204 ("phase detector"), hence "operationally connected" to the phase detector.

Lee discloses Synthesizer Control Block 214 providing Control Signals to Digital Delay Line 208 for modifying the output clock signal, where said Control Signals disclose “adjustment information.” Ex. 1008, 3:16–31; Ex. 1003, ¶168. Lee discloses multiple variations of Synthesizer Control Blocks, each disclosing how that block may generate the Control Signals. *E.g.*, Ex. 1008, Figs. 3–5; Ex. 1003, ¶168.

[1.l]: (3) an adjustable oscillator operationally connected to the phase controller and the second reference clock pin of the first interface of the field programmable gate array,

Lee discloses this limitation. Ex. 1003, ¶169. As discussed in [1.k], Lee’s Synthesizer Control Block 214 discloses the claimed “phase controller,” and as discussed in [1.b], Giordano’s FPGA pin for CLKIN into the Shared PLL discloses the “second reference clock pin of the first interface.”

Lee’s Digital Delay Line 208 discloses the claimed “adjustable oscillator.” Ex. 1003, ¶170. Lee’s Digital Delay Line 208 output OscClk discloses the claimed “second clock signal.” Ex. 1003, ¶170.

Lee discloses Digital Delay Line 208, “controlled by a synthesizer control block 214,” can modify the frequency and phase of the output signal OscClk. Ex. 1008, 2:56–3:24; Ex. 1003, ¶170. In the proposed combination, as seen in the image above in [1.i], the output OscClk is connected to the CLKIN pin of the FPGA. The

Digital Delay Line 208's connection with Synthesizer Control Block 214 and CLKIN discloses this limitation. Ex. 1003, ¶170.

This mirrors the '678 patent, which acknowledges that “the adjustable oscillator [] may be implemented with a digital delay line.” Ex. 1001, 39:4–6.

[1.m] wherein the adjustable oscillator is configured to:

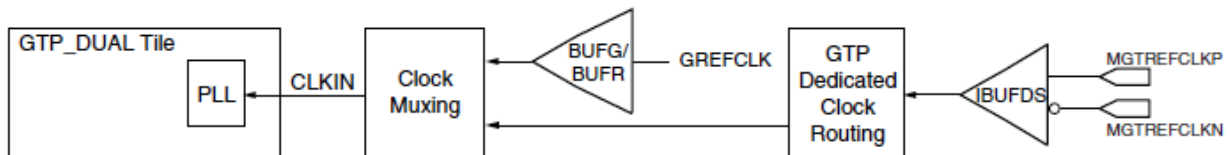
- (i) receive the adjustment information;**
- (ii) generate the second clock signal including the second frequency and the second phase based on the adjustment information; and**
- (iii) transmit the second clock signal to the second reference clock pin of the first interface of the field programmable gate array, and**

Giordano and Lee render obvious this limitation. Ex. 1003, ¶170. As discussed in [1.k], Control Signals from the Synthesizer Control Block 214 disclose the “adjustment information,” and as discussed in [1.b], Giordano's FPGA pin for CLKIN into the Shared PLL discloses the “second reference clock pin” and CLKIN signal discloses the “second clock signal.”

Lee discloses Digital Delay Line 208, controlled by Control Signals (“adjustment information”) from Synthesizer Control Block 214, generating the OscClk output and modifying its frequency and phase. Ex. 1008, 2:56–3:24; Ex. 1003, ¶171. In the proposed combination, as seen in the image above in [1.i], the output OscClk is connected to the CLKIN pin of the FPGA.

Virtex-UG further discloses this limitation. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses this limitation. Ex. 1003, ¶172.

Virtex-UG discloses three different options for CLKIN, depicted in Figure 5-3 of Virtex-UG below (where CLKIN for the GTP transceiver is noted on the left side, with the Shared PLL denoted as “PLL”):



The three options are using an external oscillator (referring to “MGTREFCLK”), using another neighboring GTP transceiver (referring to the “GTP Dedicated Clock Routing” block), and using a clock from inside the FPGA (referring to “GREFCLK”). Ex. 1009, 80. The last option, GREFCLK, uses a clock generated from inside the FPGA Fabric to drive the CLKIN port into the FPGA. *Id.*, 80, 84; Ex. 1003, ¶173.

This GREFCLK mode, where Lee’s Clock Generator output OscClk is used to operate as GREFCLK, discloses this limitation. Ex. 1003, ¶173.

[1.n] wherein the transmitter side clock signal and the first receiver side clock signal are phase aligned such that there is a fixed phase difference between the third phase and the fifth phase.

Giordano and Lee render obvious this limitation. Ex. 1003, ¶174. As discussed in [1.d] and [1.g], Giordano’s parallel recovered clock (RXRECCLK)

discloses the “first receiver side clock signal” (with “third phase”) and TXOUTCLK discloses “first transmitter side clock signal” (with “fifth phase”).

Giordano discloses that, based on measurements and test results, “the transmission latency and the phase of the recovered clock *remained always the same*,” where the signal latencies (hence phase) were measured “with respect to the reference clock at the transmitter.” Ex. 1005, 199. In Giordano’s architecture, the recovered clock (“RXRECCLK”) and the transmit-side reference clock (from which TXOUTCLK is derived) have a fixed phase difference of approximately 400 picoseconds, hence disclosing the two clocks having a fixed phase difference. *Id.*; Ex. 1003, ¶174.

In the proposed combination, Lee discloses Phase Detector 204 sending a control signal based on the measured phase difference between RXRECCLK (with “third phase”) and TXOUTCLK (with “fifth phase”) to Synthesizer Control Block 214 for adjusting the generated clock. Ex. 1008, 3:16–31; Ex. 1003, ¶175. Lee further discloses an iterative process until the two input clocks are phase aligned (Ex. 1008, 1:30–35, 3:16–24), through the feedback loop depicted in the annotated image above in [1.i] (based on Lee Figure 2). This signal to the Synthesizer Control Block 214 discloses the claimed “phase difference indicator signal.” Ex. 1003, ¶175. The relationships between the aforementioned signals disclose this limitation. *Id.*

b. Claims 2–4

Claims 2–4 concern the relationship between “first clock signal” (with “first frequency” and “first phase”) and “first receiver side clock signal” (with “third frequency” and “third phase”). Giordano in view of Lee renders obvious these claims. Ex. 1003, ¶176.

As discussed in [1.b] and [1.d], HSCLK discloses the “first clock signal” and RXRECCLK discloses the “first receiver side clock signal.”

[2]: The field programmable gate array system of claim 1, wherein the third frequency corresponds to the first frequency.

[3]: The field programmable gate array system of claim 1, wherein the third phase is not aligned with the first phase.

[4]: The field programmable gate array system of claim 1, wherein the third frequency is different than the first frequency.

Giordano discloses claims 2–4. Ex. 1003, ¶179.

Giordano discloses that in the Receiver Unit PMA, “HSCLK is divided down by 5 and then fed in a 5-bit shift-register,” which then becomes RXRECCLK. Ex. 1005, 196, Fig. 3. Using signal RXSLIDE from the FPGA Fabric, this 5-bit shift-register selects the phase shift of RXRECCLK with respect to HSCLK. *Id.*; Ex. 1003, ¶179. As such, RXRECCLK, in this implementation, has a frequency that is 20% (one-fifth) of that of HSCLK, and shifted in phase (by the 5-bit shift-register) to HSCLK. *Id.* This discloses claims 3 and 4.

Since RXRECCLK has a frequency that is one-fifth of that of HSCLK, the two clock frequencies “correspond” with each other, disclosing claim 2. Ex. 1003, ¶179.

Virtex-UG further discloses claim 2. If “correspond” requires the two frequencies to be identical, Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 2. Ex. 1003, ¶180. As discussed in [1.b] and [1.d], HSCLK discloses the “first clock signal” and RXRECCLK discloses the “first receiver side clock signal.”

Virtex-UG discloses configuration signals PLL_RXDIVSEL_OUT and PLL_DIVSEL_REF. Ex. 1009, 72. These are exemplary user configuration signals for the Xilinx Virtex-5 GTP Transceivers that control dividers that relate to RXRECCLK. Ex. 1003, ¶181. PLL_RXDIVSEL_OUT, which can be set to 1, 2, or 4, is used to divide the incoming clock signal to produce a receiver side clock. Ex. 1009, 73; Ex. 1003, ¶181. Virtex-UG discloses that setting PLL_RXDIVSEL_OUT to 1 results in a clock division of one, hence the same frequency. Ex. 1009, 77 (providing example where incoming clock at 1.5625 GHz with “the external divider (PLL_RXDIVSEL_OUT)” set to 1 results in same clock rate of 1.5625 GHz); Ex. 1003, ¶181. Likewise, PLL_DIVSEL_REF “[c]ontrols the reference clock divider” (hence impacts RXRECCLK) and can be set to 1 or 2. Ex. 1009, 73; Ex. 1003, ¶181.

Virtex-UG's disclosures of clock dividers that divide by one discloses this limitation. As discussed in claim 3, Giordano discloses that in the Receiver Unit PMA, "HSCLK is divided down by 5" by a clock divider (denoted as " $\div 5$ "), which then outputs RXRECCLK. Ex. 1005, 196, Fig. 3. As such, RXRECCLK, in this implementation, has a frequency that is 20% (one-fifth) of that of HSCLK.

It would have been obvious to a POSITA to modify the " $\div 5$ " block in Giordano to incorporate the clock dividers of Virtex-UG, namely those that can be set to 1. Ex. 1003, ¶183. With such clock divider, RXRECCLK would have the same frequency as HSCLK, disclosing this limitation. *Id.*

c. Claim 5

[5]: The field programmable gate array system of claim 1, wherein the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

Giordano discloses this claim. Ex. 1003, ¶184.

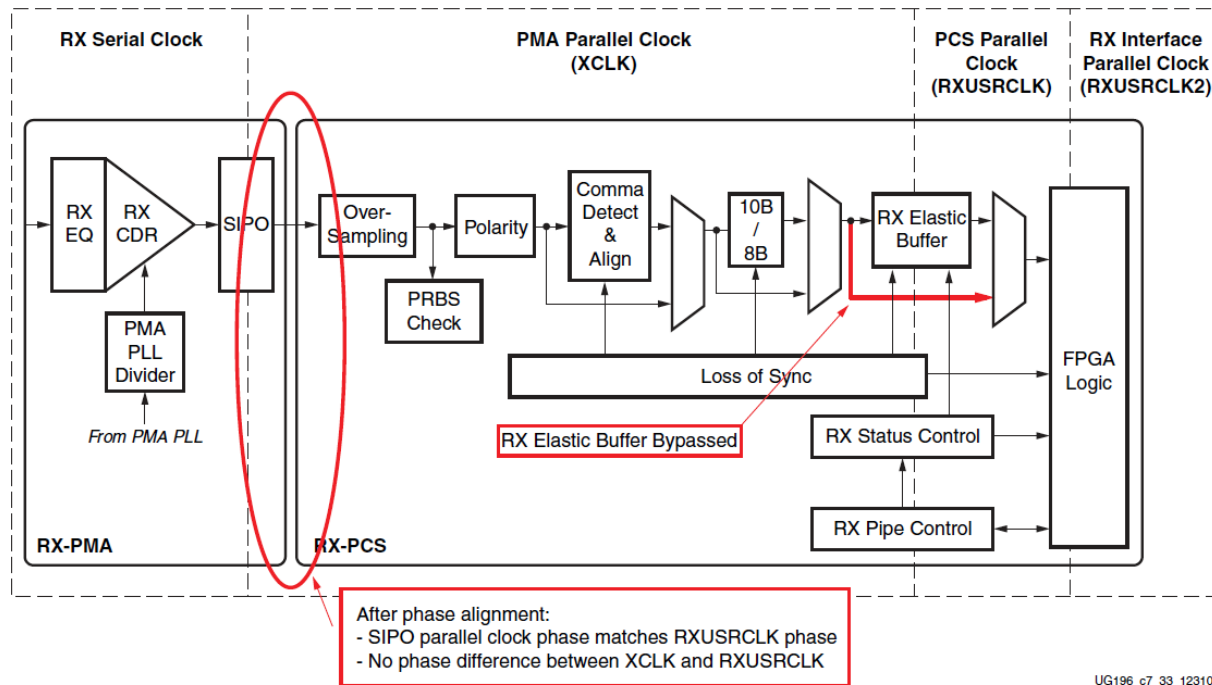
Giordano discloses bypassing First In First Out (FIFO) buffer, a circuit block allowing safe data transfer between different clock domains (*e.g.*, "data transfers between TXUSRCLK domain and the XCLK domain"). Ex. 1005, 195; Ex. 1003, ¶185. A POSITA would have understood FIFO as executing clock domain crossing operations, and Giordano's bypassing of FIFO block discloses this limitation. *Id.*

Giordano discloses bypassing FIFO buffer by having the two clock domains have "the same phase" and "therefore also the same latency for the data." Ex. 1005,

195; Ex. 1003, ¶186. In the transmitter, Giordano discusses two clocks (XCLK and TXUSRCLK) that are adjusted to have the same frequency and phase. Ex. 1005, 195. The transmitter has a FIFO block for crossing between XCLK and TXUSRCLK clock domains. *Id.*; Ex. 1003, ¶186. Giordano discloses bypassing this FIFO block by using a phase alignment option provided in Xilinx Virtex-5 FPGA systems. Ex. 1005, 195; Ex. 1003, ¶186. Through this built-in phase alignment, XCLK and TXUSRCLK are phase aligned, in which “the transmit FIFO is unnecessary and therefore we bypassed it.” Ex. 1005, 197.

Virtex-UG further discloses this limitation. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses this limitation. Ex. 1003, ¶187.

In the receiver, Virtex-UG confirms this FIFO bypass. When receiver clock phase alignment is used, “RXUSRCLK must be driven directly from RXRECCLK using a BUFR regional clock buffer.” Ex. 1009, 179 (“Using RX Phase Alignment to Bypass the RX Elastic Buffer”). Due to phase alignment, “SIPO parallel clock phase matches RXUSRCLK phase” and there is “no phase difference between XCLK and RXUSRCLK.” *Id.*, 180. With no phase difference, the RX Elastic Buffer (which is the FIFO block described in Giordano) is bypassed. This bypass is described in the red arrow below in Figure 7-22 of Virtex-UG:



Giordano's bypass of all clock domain crossing circuits after phase alignment of clock signals discloses this limitation. Ex. 1003, ¶188.

d. Claim 6

[6]: The field programmable gate array system of claim 1, wherein the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

Giordano discloses this limitation. Ex. 1003, ¶189. As discussed in [1.e], Giordano's disclosures on the PCS layer processing and the FPGA Fabric "logic" disclose the claimed "first set of operations."

The operations on PCS layers and FPGA Fabric each discloses this limitation.

Giordano's Comma Detector and Aligner implemented in the FPGA Fabric performs pattern matching (detecting comma characters in the raw 10-bit data),

comparison (determining the number of bit shifts required), and conditional branching (the even/odd decision logic that either applies RXSLIDE assertions or resets the CDR). Ex. 1005, 198. These are examples of logical operations, which disclose this limitation. Ex. 1003, ¶190.

In addition, Giordano points to the PCS layer (both receiver and transmitter sides) as “processing” data, disclosing computational circuitry. Ex. 1005, 194; Ex. 1003, ¶191. The PCS layer includes optional 8b/10b encoding / decoding functions, which require arithmetic calculations, hence disclosing this claim. Ex. 1005, 197; Ex. 1003, ¶191.

e. Claim 7

[7]: The field programmable gate array system of claim 1, wherein the first amount of data streams is the same as the second amount of data streams.

Giordano’s use of the optional 8b/10b encoding / decoding feature discloses this limitation. Ex. 1003, ¶192.

Giordano discloses the SIPO deserializing incoming serial data stream into 10-bit parallel words, which may then be decoded into 8-bit parallel words using 8b/10b decoding (and if not, kept at 10-bit). Ex. 1005, 195. On the transmit side, the FPGA fabric provides either 8-bit words for re-encoding into 10-bit words or, if 8b/10b encoding is not used, 10-bit words directly to the PISO block. Ex. 1005, 195, 197. A POSITA would have found it obvious to have what is identified as first

amount of data streams to be identical to second amount of data streams, either 8-bits or 10-bits. Ex. 1003, ¶192.

f. Claim 8

[8]: The field programmable gate array system of claim 1, wherein the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

Giordano discloses this limitation. Ex. 1003, ¶193. As discussed in claim 7, Giordano discloses internal parallel data width to be same on both receiver and transmitter sides.

Giordano's use of 8-bit parallel words (eight data streams) and 10-bit parallel words (ten data streams) disclose this limitation. Ex. 1005, 195; Ex. 1003, ¶193.

g. Claim 9

[9]: The field programmable gate array system of claim 1, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

Giordano discloses use of 8-bit parallel words (eight data streams), which is two to the power of three, discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶194.

h. Claim 10

[10]: The field programmable gate array system of claim 1, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

Giordano discloses use of 10-bit parallel words (ten data streams), which is ten times two to the power of zero, discloses this limitation. Ex. 1005, 195; Ex. 1003, ¶195.

i. Claim 11

[11]: The field programmable gate array system of claim 1, wherein the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

Giordano discloses this claim. Ex. 1003, ¶196.

Virtex-UG further discloses claim 11. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 11. Ex. 1003, ¶196. As discussed in elements [1.d] and [1.e], Giordano's SIPO block output, further processed by the Receiver Unit PCS, disclose the "first amount of data streams," and processed parallel data going through the Transmitter Unit PCS and PMA disclose the "second amount of data streams."

Virtex-UG discloses that the Virtex-5 FPGA GTP Transceiver supports 64b/66b encoding, in addition to the optional 8b/10b encoding demonstrated by Giordano (using the same Virtex-5 FPGA GTP Transceiver). Ex. 1009, 283, 286, 290; Ex. 1005, 194 ("The architecture we present in this paper is based on the GTP transceiver of the Xilinx Virtex 5 FPGA family"); Ex. 1003, ¶197. By using the

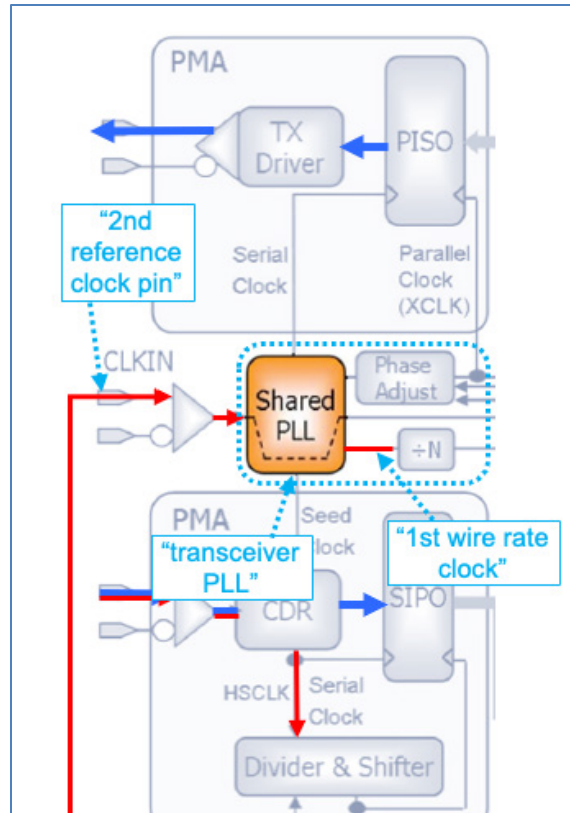
64b/66b encoding standard, it would have been obvious to modify the GTP transceiver of the proposed combination to support 66-bit data words. Ex. 1003, ¶197. This would have rendered obvious first and second amount of data streams at 66 bits. *Id.* Since 66 is thirty-three times two to the power of one, Virtex-UG discloses this limitation.

j. Claim 12

[12a]: The field programmable gate array system of claim 1, wherein the transceiver phase lock loop is operationally connected to the second reference clock pin, and

Giordano discloses this claim. Ex. 1003, ¶198. As discussed in [1.f], Giordano's Shared PLL, phase adjustment circuit, and divider together disclose the "transceiver [PLL]," and as discussed in [1.b], Giordano's FPGA pin for CLKIN into the Shared PLL discloses the "second reference clock pin."

The image below, based on Giordano Figure 1 with additional annotations, shows the portions of the Giordano-Lee combination relevant to this limitation:



As seen above, CLKIN is provided to the Shared PLL, disclosing this limitation. Ex. 1003, ¶200.

[12b] wherein the transceiver phase lock loop is configured to:

- (i) receive the second clock signal, as a fourth input, to generate the first wire rate clock signal; and**
- (ii) transmit the first wire rate clock signal as the third input, to the serializer.**

Claim 1 (from which claim 12 depends) requires that the transceiver phase lock loop “*receive[s]* a first wire rate clock signal based on the second clock signal,” whereas claim 12 requires that the transceiver phase lock loop “*generate[s]* the first wire rate clock signal.” As explained in [1.f], Giordano discloses that the Shared

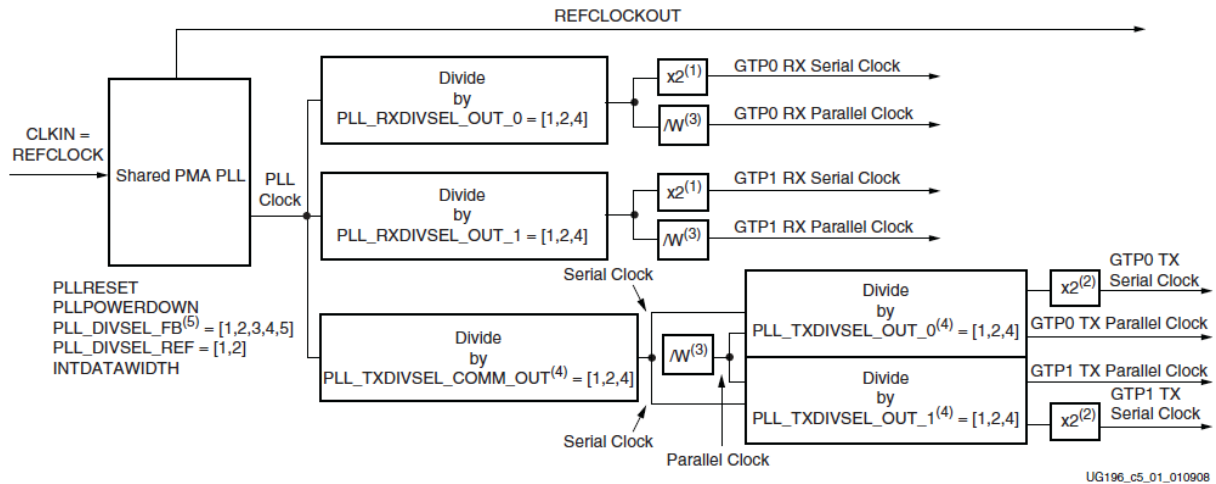
PLL receives CLKIN (“the second clock signal”), generates an output (“the first wire rate clock signal”), and transmits output to the clock divider (denoted as “÷ 5”).

Each of the Shared PLL, phase adjust, and divider is a part of the transceiver phase lock loop. Section VI.A.1.f. Thus, Giordano discloses that the transceiver phase lock loop both receives (claim 12) and generates (claim 1) the first wire rate clock signal, hence disclosing limitation 12(b)(i).

Giordano further discloses that the transceiver phase lock loop transmits its output to the PISO, which is a part of the PMA (the “serializer,” *see* [1.f]). Thus, Giordano discloses limitation 12(b)(ii).

Virtex-UG further discloses this limitation. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses this limitation. Ex. 1003, ¶202.

Virtex-UG discloses that the Shared PLL generates “a high-speed serial clock from a high-quality reference clock (CLKIN).” Ex. 1009, 72; Ex. 1003, ¶202. Virtex-UG discloses components (including dividers and multipliers) involved with converting the reference clock (CLKIN, *i.e.*, “second clock signal”) to multiple clock signals, as seen in Virtex-UG Figure 5-1:



Ex. 1003, ¶202. The Shared PLL’s generation of multiple clock signals, derived from CLKIN, discloses this limitation. *Id.*

k. Claim 13

[13]: The field programmable gate array system of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.

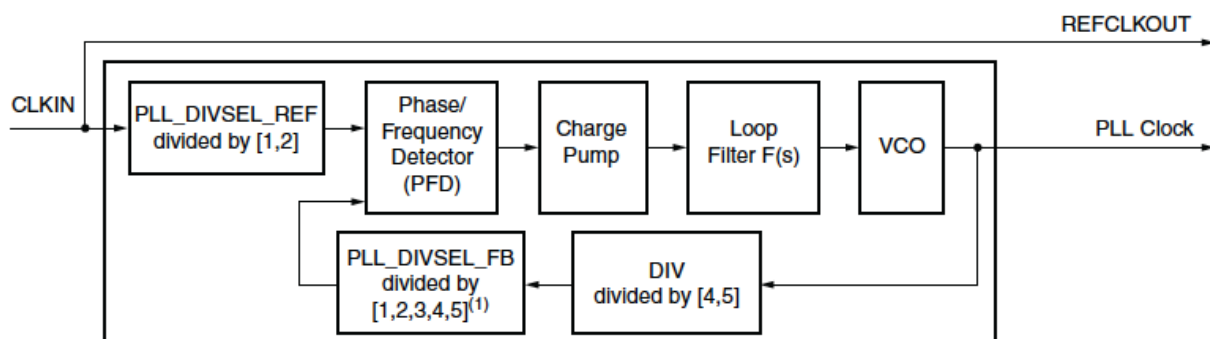
Giordano discloses this limitation. Ex. 1003, ¶203. As discussed in [1.f], Giordano’s Shared PLL output into divider “÷ N” discloses “first wire rate clock signal” (and the “fourth frequency”), and TXOUTCLK discloses “first transmitter side clock signal” (and the “fifth frequency”). As discussed in claim 7, Giordano discloses 8-bit and 10-bit words, which disclose the “second amount of data streams.”

Giordano’s disclosure of 10-bit words as the claimed “second amount” means that the claimed “second amount of data streams” is equal to ten. Ex. 1003, ¶204. This, with Giordano’s use of clock dividers, discloses this limitation.

Giordano discloses that the output of the Shared PLL (“first wire rate clock”) is connected to a divider block denoted “÷N,” which in turn outputs TXOUTCLK. A POSITA would have understood N to be an integer, including ten. Ex. 1003, ¶205. This results in Giordano’s Shared PLL output (“first wire rate clock”) having a frequency ten times that of TXOUTCLK. *Id.* Since TXOUTCLK is synchronized with Clock Generator output (“second clock signal”), it would have been obvious to a POSITA for the two clocks to have the same frequency. *Id.* Hence the Shared PLL output (“first wire rate clock”) would have a frequency ten times that of Clock Generator output (“second clock signal”), rendering obvious this limitation. *Id.*

Virtex-UG further discloses claim 13. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 13. Ex. 1003, ¶206.

Virtex-UG discloses two divider blocks DIV and PLL_DIVSEL_FB, when put together, could divide signals by eight or ten. Per Figure 5-2 of Virtex-UG, an exemplary cascade of dividers is shown:



The clock path that includes the PLL_DIVSEL_FB block and the DIV block results in various combinations of frequency divisions. Ex. 1003, ¶206. For example, PLL_DIVSEL_FB dividing by 2 and DIV dividing by 5 results in overall division of ten. *Id.* PLL_DIVSEL_FB dividing by 2 and DIV dividing by 4 results in overall division of eight. *Id.*

Applying this to the proposed combination, a POSITA would have known to implement Virtex-UG's cascaded dividers into Giordano's divider block " $\div N$." Ex. 1003, ¶207. Using the cascade to have total division of ten results in Giordano's Shared PLL output ("first wire rate clock") having a frequency ten times that of TXOUTCLK. *Id.* Since TXOUTCLK is synchronized with Clock Generator output ("second clock signal"), it would have been obvious to a POSITA for the two clocks to have the same frequency. *Id.* Hence the Shared PLL output ("first wire rate clock") would have a frequency ten times that of Clock Generator output ("second clock signal"), rendering obvious this limitation. *Id.*

I. Claim 14

[14]: The field programmable gate array system of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.

Giordano discloses this limitation. Ex. 1003, ¶208. As discussed in [1.f], Giordano's Shared PLL output into divider " $\div N$ " discloses "first wire rate clock signal" (and the "fourth frequency"), and TXOUTCLK discloses "first transmitter

side clock signal” (and the “fifth frequency”). As discussed in claim 7, Giordano discloses 8-bit and 10-bit words, which disclose the “second amount of data streams.”

Giordano’s disclosure of 10-bit words as the claimed “second amount” means that the claimed “half of the second amount of data streams” is equal to five. Ex. 1003, ¶208. This, with Giordano’s use of clock dividers, discloses this limitation.

Giordano discloses using clock dividers of “ $\div 5$ ” for the receiver clock divider. Ex. 1005, Fig. 3. On the transmitter side, the output of the Shared PLL (“first wire rate clock”) is connected to a divider block denoted “ $\div N$,” which in turn outputs TXOUTCLK. A POSITA would have known to use the “ $\div 5$ ” divider, explicitly used for the receiver side, for the “ $\div N$ ” block on the transmitter side. Ex. 1003, ¶209. This results in Giordano’s Shared PLL output (“first wire rate clock”) having a frequency five times that of TXOUTCLK. *Id.* Since TXOUTCLK is synchronized with Clock Generator output (“second clock signal”), it would have been obvious to a POSITA for the two clocks to have the same frequency. *Id.* Hence, the Shared PLL output (“first wire rate clock”) would have a frequency five times that of Clock Generator output (“second clock signal”), rendering obvious this limitation. *Id.*

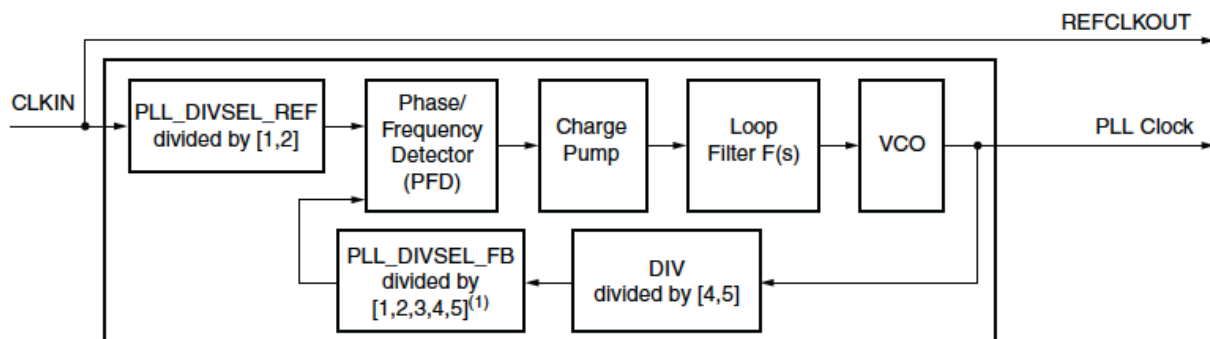
Virtex-UG further discloses claim 14. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 14. Ex. 1003,

¶210. As discussed in claim 13, Virtex-UG discloses cascading dividers that support a multitude of clock frequency division options.

Giordano’s disclosure of 10-bit words as the claimed “second amount” means that the claimed “second amount of data streams” is equal to ten. Ex. 1003, ¶211. This, with Giordano’s use of clock dividers, discloses this limitation.

Giordano discloses that the output of the Shared PLL (“first wire rate clock”) is connected to a divider block denoted “÷N,” which in turn outputs TXOUTCLK.

Virtex-UG discloses two divider blocks DIV and PLL_DIVSEL_FB, that when put together, could divide signals by four or five. Per Figure 5-2 of Virtex-UG, an exemplary cascade of dividers is shown:



The clock path that includes the PLL_DIVSEL_FB block and the DIV block results in various combinations of frequency divisions. Ex. 1003, ¶214. For example, PLL_DIVSEL_FB dividing by 1 and DIV dividing by 5 results in overall division of five. *Id.* PLL_DIVSEL_FB dividing by 1 and DIV dividing by 4 results in overall division of four. *Id.*

Applying this to the proposed combination, a POSITA would have known to implement Virtex-UG's cascaded dividers into Giordano's divider block " $\div N$." Ex. 1003, ¶214. Using the cascade to have total division of five results in Giordano's Shared PLL output ("first wire rate clock") having a frequency five times that of TXOUTCLK. *Id.* Since TXOUTCLK is synchronized with Clock Generator output ("second clock signal"), it would have been obvious to a POSITA for the two clocks to have the same frequency. *Id.* Hence, the Shared PLL output ("first wire rate clock") would have a frequency five times that of Clock Generator output ("second clock signal"), rendering obvious this limitation. *Id.*

m. Claim 15

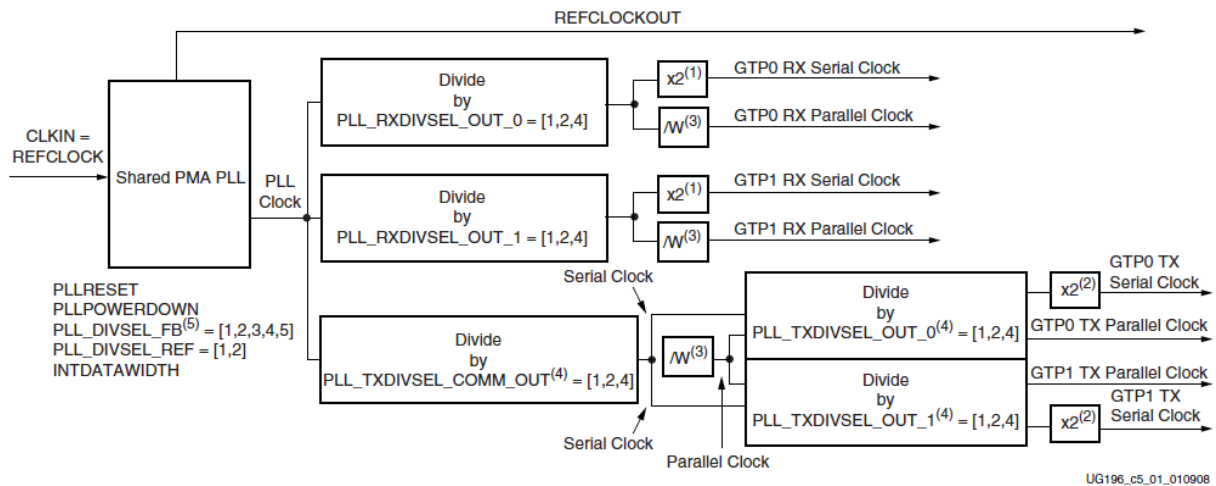
[15]: The field programmable gate array system of claim 1, wherein the fourth frequency is a rational multiple of the second frequency.

Giordano discloses this limitation. Ex. 1003, ¶215. As explained in [1.b] and [1.f], CLKIN signal discloses the "second clock signal" (and the "second frequency"), and Giordano's Shared PLL output into divider " $\div N$ " discloses "first wire rate clock signal" (and the "fourth frequency").

Giordano discloses that the "shared PLL locks to a reference clock (CLKIN)" (the "second frequency") and generates the Shared PLL output ("fourth frequency"). A POSITA would have known that this discloses a fourth frequency that is a rational multiple of a second frequency. Ex. 1003, ¶215.

Virtex-UG further discloses claim 15. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 15. Ex. 1003, ¶216.

Virtex-UG discloses that the Shared PLL generates “a high-speed serial clock from a high-quality reference clock (CLKIN).” Ex. 1009, 72; Ex. 1003, ¶216. Virtex-UG discloses components (including dividers and multipliers) involved with converting the reference clock (CLKIN, *i.e.*, “second clock signal”) to multiple clock signals, as seen in Virtex-UG Figure 5-1:



Ex. 1003, ¶216. Virtex-UG discloses multiple dividers in cascade and parallel routes, each with different configurable divider values (such as dividing by 1, 2, or 4). Ex. 1009, Fig. 5-1; Ex. 1003, ¶216. These various options of divisions each disclose this limitation. *Id.*

n. Claim 16

[16]: The field programmable gate array system of claim 1, wherein the phase difference indicator signal is a pulse signal.

Giordano and Lee render obvious this limitation. Ex. 1003, ¶217. As discussed in [1.j], Lee discloses a Phase Detector which transmits a signal (“phase difference indicator signal”) to a Synthesizer Control block.

In exemplary Figures 3 and 4, Lee discloses that the signal is a “binary error signal,” disclosing the limitation. Ex. 1008, 3:25–31, 4:13–18; Ex. 1003, ¶217.

In the proposed combination, Lee’s teachings are implemented on Giordano’s FPGA Fabric via programmable logic. Section VI.A.1. Giordano discloses that the signals on the FPGA Fabric, such as RXSLIDE, are in the form of pulse signals. Ex. 1005, Figs. 4, 7.

Thus, the combination of Giordano and Lee renders this claim obvious.

Virtex-UG further discloses claim 16. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 16. Ex. 1003, ¶219.

Virtex-UG discloses that RXSLIDE is a signal where each assertion (*i.e.*, pulse) “of RXSLIDE causes just one adjustment.” Ex. 1009, 164; Ex. 1003, ¶219. This describes pulse behavior, where each pulse results in one discrete bit-slide. *Id.* This disclosure of signals in pulse form in the FPGA Fabric, with the teachings of Lee, renders obvious this limitation. *Id.*

o. Claim 17

[17]: The field programmable gate array system of claim 1, wherein adjustment information indicates at least one of the following: (i) a desired phase; (ii) a desired frequency; (iii) a change in phase; and (iv) a change in frequency.

Lee discloses this limitation. Ex. 1003, ¶220.

As explained in [1.k], Lee discloses Synthesizer Control Block 214 providing Control Signals (“adjustment information”). Lee further discloses that the Control signal may “adjust the frequency of the generated clock signal toward the desired frequency,” disclosing this claim. Ex. 1008, 3:16–31; *see also id.*, Figs. 3–5; Ex. 1003, ¶220.

p. Claim 18

[18]: The field programmable gate array system of claim 1, wherein adjustment information comprises a voltage.

Lee discloses this limitation. Ex. 1003, ¶221. As explained in [1.k], Lee discloses Synthesizer Control Block 214 providing Control Signals (“adjustment information”).

Lee further discloses that an oscillator may be “voltage controlled,” and depicts a “Frequency Control Signal” provided to such an oscillator. Ex. 1008, 1:24–51, Fig. 1.

q. Claim 19

[19]: The field programmable gate array system of claim 1, wherein adjustment information comprises a digital transmission.

Lee discloses this limitation. Ex. 1003, ¶222. As explained in [1.k], Lee discloses Control Signals (“adjustment information”) and provides examples in Figures 3–5.

Lee further discloses with respect to each of Figures 3–5 that the control block “can be implemented as a portion of a digital frequency register,” disclosing this claim. Ex. 1008, 3:32–33, 4:20–21, 5:5–6; Ex. 1003, ¶222.

r. Claim 20

[20]: The field programmable gate array system of claim 1, wherein the adjustment information is configured to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay.

Lee discloses this limitation. Ex. 1003, ¶223. As explained in [1.k], Lee discloses Control Signals (“adjustment information”).

Lee further discloses, with respect to each of Figures 3–5, that the control block may comprise a “delay select signal” provided to the oscillator. Ex. 1008, 4:9–12, 4:59–64, 6:13–18. Lee further discloses that a divider may be added to the Control Signal of Fig. 4, as depicted in Fig. 7. Ex. 1008, 6:19–27.

B. Ground 2: Claims 1–22 Are Rendered Obvious by Giordano in View of Lee further in View of Raymond

1. Overview

This proposes using the Giordano and Lee combination of Ground 1 and further implementing components for financial trading context explicitly disclosed in Raymond.

a. Motivation to Combine Giordano, Lee, and Raymond

Raymond emphasized the importance of minimizing latency in communication devices, particularly for applications such as financial exchange. Ex. 1007 at 1:18–38. Raymond recognizes that higher clock rates reduce latency but also notes that this requires adding a distinct (faster) clock, and additional clock conversions introduce unwanted latency. *Id.*, 8:40–50.

A POSITA reading Raymond would therefore have recognized that Giordano in view of Lee offers a solution for synthesizing clock signals at the required frequencies while managing phase alignment and filtering jitter—precisely the clock distribution challenges Raymond identifies. Section VI.A.1.a (Motivation to Combine Giordano and Lee); Ex. 1003, ¶227.

A POSITA would have recognized Giordano in view of Lee as an attractive solution for the PLL functionality depicted in Raymond’s system, and motivated to look to Giordano and Lee to combine with Raymond. Raymond repeatedly discusses implementing its invention with Xilinx UltraScale GTY transceivers. Ex.

1007 at 5:48–56, 6:3–8, 8:18–28, 8:51–55. A POSITA reading Raymond would have naturally consulted Xilinx’s own materials (such as Lee, a Xilinx patent) and publications demonstrating Xilinx FPGA implementations (such as Giordano), for a PLL-based phase alignment solution. Ex. 1003, ¶228.

A POSITA would have had a reasonable expectation of success in combining Giordano, Lee, and Raymond. A POSITA would have recognized that the FPGA’s programmable logic and on-chip clock management resources could be configured to implement the teachings of the three references as needed. Ex. 1003, ¶229. Because all references suggest implementations with Xilinx transceiver infrastructure, a POSITA would have had a high expectation that the combination would function as intended. Section VI.A.1.a (Motivation to Combine Giordano and Lee); Ex. 1003, ¶229.

2. Analysis

a. Claims 1–5

Giordano in view of Lee renders obvious these claims. Section VI.A.2.a–VI.A.2.c (Ground 1, cls. 1–5).

b. Claim 6

[6]: The field programmable gate array system of claim 1, wherein the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

Giordano in view of Lee renders obvious this claim. Section VI.A.2.d (Ground 1, cl. 6).

Raymond further discloses this limitation. Ex. 1003, ¶232.

Raymond discloses that data on the transmitting side includes “an outgoing data link layer signal 250 that has been outputted after logical processing (*e.g.*, applying financial trading algorithms)” and “[a] transmitting side PCS module 92 converts the data link layer signal to an outgoing electrical physical layer parallel output signal 252.” Ex. 1007, 11:57–63. The applying of financial trading algorithms in Raymond discloses the claimed “first set of operations.” Ex. 1003, ¶232. Raymond’s application of financial trading algorithms involves arithmetic operations, hence discloses this limitation. Ex. 1007, 11:57–60; Ex. 1003, ¶232.

c. Claim 7

[7]: The field programmable gate array system of claim 1, wherein the first amount of data streams is the same as the second amount of data streams.

Giordano in view of Lee renders obvious this claim. Section VI.A.2.e (Ground 1, cl. 7).

Raymond further discloses this limitation. Ex. 1003, ¶234.

Raymond discloses that “the transmitting-side SerDes module 256 can have the same serialization ratio as the de-serialization ratio of the receiving side SerDes module 240.” Ex. 1007, 12:23–25. The same ratio results in the same parallel data streams, hence disclosing this limitation. Ex. 1003, ¶234.

d. Claim 8

[8]: The field programmable gate array system of claim 1, wherein the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

Giordano in view of Lee renders obvious this claim. Section VI.A.2.f (Ground 1, cl. 8).

Raymond further discloses this limitation. Ex. 1003, ¶236.

Raymond discloses that “the UltraScale™ GTY from Xilinx™ has internal data buses of 16, 20, 32, 40 or 64 bits, with a minimum bit-width of 16 bits and a minimum de-serialization ratio of 1:16.” Ex. 1007, 6:5–8. A POSITA would have understood that the SerDes module 208 could be configured to apply any of these de-serialization ratios depending on the application requirements, and that the serialization ratio of SerDes module 256 would match. Ex. 1003, ¶236.

e. Claim 9

[9]: The field programmable gate array system of claim 1, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

Giordano in view of Lee renders obvious this claim. Section VI.A.2.g (Ground 1, cl. 9).

Raymond further discloses this limitation. Ex. 1003, ¶238.

Raymond discloses that “internal data buses of 16, 20, 32, 40 or 64 bits.” Ex. 1007, 6:5–8. 16 is two to the power of four, 32 is two to the power of five, and 64 is two to the power of six, hence Raymond’s 16, 32, and 64 bit buses disclose this limitation. Ex. 1003, ¶238.

f. Claim 10

[10]: The field programmable gate array system of claim 1, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

Giordano in view of Lee renders obvious this claim. Section VI.A.2.h (Ground 1, cl. 10).

Raymond further discloses this limitation. Ex. 1003, ¶240.

Raymond discloses that “internal data buses of 16, 20, 32, 40 or 64 bits.” Ex. 1007, 6:5–8. 20 is ten times two to the power of one, and 40 is ten times two to the power of two, hence Raymond’s 20 and 40 bit buses disclose this limitation. Ex. 1003, ¶240.

g. Claims 11–20

Giordano in view of Lee renders obvious these claims. Section VI.A.2.i–A.2.r (Ground 1, cls. 11–20).

h. Claim 21

[21]: The field programmable gate array system of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.

Raymond discloses this limitation. Ex. 1003, ¶242.

Raymond expressly identifies electronic trading as a primary application for its ultra-low latency communication device, and describes the incoming and outgoing data streams in terms that correspond directly to market data and order entry data. For example, Raymond discloses incoming and outgoing serial data streams in context of “financial trading data,” which are transmitted to and from “financial exchange.” Ex. 1007, 4:52–65.

Indeed, Raymond discloses “market data feed handler” and “market data feed distribution systems” applications, disclosing receiving market data. Ex. 1007, 13:61–64; Ex. 1003, ¶243. Raymond further discloses that the outgoing data link layer signal 250 is “outputted after logical processing (*e.g.*, applying financial trading algorithms),” hence disclosing sending out financial order related data and operations associated with trading algorithms. *Id.* at 11:57–60; Ex. 1003, ¶243.

i. Claim 22

[22]: The field programmable gate array system of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.

Raymond discloses this limitation. Ex. 1003, ¶244. As discussed in claim 21, Raymond discloses receiving market data and transmitting the results of applying financial trading algorithms, hence disclosing this limitation. *Id.*

C. Ground 3: Claims 1–20 Are Rendered Obvious by Giordano in View of Lee further in View of Virtex-UG

1. Overview

This proposes using the Giordano and Lee combination of Ground 1 and further modifying transceiver and FPGA configurations as necessary based on teachings of Virtex-UG.

a. Motivation to Combine Giordano, Lee, and Virtex-UG:

While Giordano already inherently discloses and incorporates Virtex-UG, if necessary, a POSITA would have been motivated to look to Virtex-UG to combine with Giordano and Lee. Virtex-UG is a user guide for Xilinx Virtex FPGA offerings, which is the FPGA chip used in Giordano. Ex. 1005, 194, 197–199. Virtex-UG details how to use, configure, and modify the Virtex-5 FPGA “RocketIO” GTP transceiver. *See generally*, Ex. 1009; Ex. 1003, ¶247.

A POSITA reading Virtex-UG would therefore have recognized that its teachings would be helpful in the use, configuration, and modification of the FPGA

system based on Giordano in view of Lee, including for synthesizing clock signals at the required frequencies while managing phase alignment and filtering jitter. Section VI.A.1.a (Motivation to Combine Giordano and Lee); Ex. 1003, ¶248.

A POSITA would have had a reasonable expectation of success in combining Giordano, Lee, and Virtex-UG, recognizing that the FPGA's programmable logic and on-chip clock management resources could be configured to implement the teachings of the three references as needed. Ex. 1003, ¶249. Because all references suggest implementations with Xilinx transceiver infrastructure, a POSITA would have had a high expectation that the combination would function as intended. Section VI.A.1.a (Motivation to Combine Giordano and Lee); Ex. 1003, ¶249.

2. Analysis

a. Claims 1–20

Giordano in view of Lee and Virtex-UG renders obvious these claims. Section VI.A.2 (Ground 1, Analysis).

D. Ground 4: Claims 1–22 Are Rendered Obvious By Giordano in view of Lee, Virtex-UG, and Raymond

1. Overview

This proposes using the Giordano, Lee, and Virtex-UG combination of Ground 3 and further modifying the FPGA for financial trading applications explicitly disclosed in Raymond.

**a. Motivation to Combine Giordano, Lee, Virtex-UG,
and Raymond**

Motivations to combine Giordano, Lee, and Virtex-UG is detailed in Ground
3. Section VI.C.1 (Ground 3 Prior Art Overview).

A POSITA would have been motivated to look to Raymond to combine with
Giordano, Lee, and Virtex-UG, for the same reasons to combine Raymond with
Giordano and Lee. Section VI.B.1 (Ground 2 Prior Art Overview).

2. Analysis

a. Claims 1–22

Giordano in view of Lee and Virtex-UG renders obvious claims 1–20. Section
VI.C.2 (Ground 3, Analysis).

Raymond further discloses claims 6–10, 21–22. Section VI.B.2 (Ground 2,
Analysis).

VII. CONCLUSION

Petitioners have established a reasonable likelihood that the Challenged
Claims are unpatentable. Petitioners therefore respectfully request that IPR be
instituted.

DATED: June 4, 2026

Respectfully Submitted,

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CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned attorney hereby certifies that the word count for Sections I–VII of the foregoing Petition for *Inter Partes* Review is 13,954, according to the word count tool in Microsoft Word.

DATED: June 4, 2026

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CERTIFICATE OF SERVICE

The undersigned certifies service pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(a), (b) on the Patent Owner via FedEx overnight mail of a copy of this Petition for *Inter Partes* Review and supporting materials at the correspondence address of record for the '678 patent shown in USPTO Patent Center:

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APPENDIX: CHALLENGED CLAIM LISTING

No.	Limitation
[1.pre]	1. A field programmable gate array system, comprising:
[1.a]	(a) a field programmable gate array comprising
[1.b]	(1) a first interface comprising (A) a first reference clock pin, wherein said first reference clock pin is configured to receive a first clock signal having a first frequency and a first phase; (B) a second reference clock pin, wherein said second reference clock pin is configured to receive a second clock signal having a second frequency and a second phase; (C) a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream; (D) a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream;
[1.c]	(2) a deserializer operationally connected to (A) the first reference clock pin to receive as a first input the first clock signal and (B) the first plurality of data pins to receive as a second input the first serial data stream, and
[1.d]	wherein the deserializer is configured to (i) convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams; (ii) generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase; and (iii) transmit the first plurality of parallel data streams and the first receiver side clock signal within the field programmable gate array;

No.	Limitation
[1.e]	(3) computational circuitry operationally connected to the deserializer to receive the first plurality of parallel data streams and the first receiver side clock signal, wherein the computational circuitry is configured to perform a first set of operations on the first plurality of parallel data streams to generate a second plurality of parallel processed data streams having a second amount of data streams and the computational circuitry performs the first set of operations to generate the second plurality of parallel processed data without use of a clock domain crossing circuit;
[1.f]	(4) a serializer operationally connected to (i) a transceiver phase lock loop to receive as a third input a first wire rate clock signal based on the second clock signal, wherein the first wire rate clock signal has a fourth frequency and a fourth phase; (ii) the second plurality of data pins to transmit as a first output the second serial data stream; and (iii) the computational circuitry, wherein the serializer receives the second plurality of parallel processed data streams from the computational circuitry and the serializer transmits to the computational circuitry a first transmitter side clock signal including a fifth frequency and a fifth phase, and
[1.g]	wherein the serializer is configured to: a. convert the second plurality of parallel processed data streams into the second serial data stream; b. generate the first transmitter side clock signal based on the first wire rate signal, wherein the first transmitter side clock signal has the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency; and c. transmit the second serial data stream to the second plurality of data pins for transmission off the field programmable gate array;

No.	Limitation
[1.h]	(5) a second interface comprising (i) a first clock output pin configured to transmit the first receiver side clock signal, wherein the first clock output pin is operationally connected to the deserializer; and (ii) a second clock output pin configured to transmit the first transmitter side clock signal, wherein the second clock output pin is operationally connected to the serializer; and
[1.i]	(b) a phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises:
[1.j]	(1) a phase detector operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array, and wherein the phase detector is configured to compare the third phase of the first receiver side clock signal to the fifth phase of the transmitter side clock signal and to generate a phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the fifth phase of the transmitter side clock signal;
[1.k]	(2) a phase controller operationally connected to the phase detector and configured to receive the phase difference indicator signal, wherein the phase controller is configured to determine adjustment information based on the phase difference indicator signal; and
[1.l]	(3) an adjustable oscillator operationally connected to the phase controller and the second reference clock pin of the first interface of the field programmable gate array,
[1.m]	wherein the adjustable oscillator is configured to: (i) receive the adjustment information; (ii) generate the second clock signal including the second frequency and the second phase based on the adjustment information; and (iii) transmit the second clock signal to the second reference clock pin of the first interface of the field programmable gate array, and

No.	Limitation
[1.n]	wherein the transmitter side clock signal and the first receiver side clock signal are phase aligned such that there is a fixed phase difference between the third phase and the fifth phase.
[2]	The field programmable gate array system of claim 1, wherein the third frequency corresponds to the first frequency.
[3]	The field programmable gate array system of claim 1, wherein the third phase is not aligned with the first phase.
[4]	The field programmable gate array system of claim 1, wherein the third frequency is different than the first frequency.
[5]	The field programmable gate array system of claim 1, wherein the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.
[6]	The field programmable gate array system of claim 1, wherein the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.
[7]	The field programmable gate array system of claim 1, wherein the first amount of data streams is the same as the second amount of data streams.
[8]	The field programmable gate array system of claim 1, wherein the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.
[9]	The field programmable gate array system of claim 1, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

No.	Limitation
[10]	The field programmable gate array system of claim 1, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.
[11]	The field programmable gate array system of claim 1, wherein the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.
[12a]	The field programmable gate array system of claim 1, wherein the transceiver phase lock loop is operationally connected to the second reference clock pin, and
[12b]	wherein the transceiver phase lock loop is configured to: (i) receive the second clock signal, as a fourth input, to generate the first wire rate clock signal; and (ii) transmit the first wire rate clock signal as the third input, to the serializer.
[13]	The field programmable gate array system of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.
[14]	The field programmable gate array system of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.
[15]	The field programmable gate array system of claim 1, wherein the fourth frequency is a rational multiple of the second frequency.
[16]	The field programmable gate array system of claim 1, wherein the phase difference indicator signal is a pulse signal.
[17]	The field programmable gate array system of claim 1, wherein adjustment information indicates at least one of the following: (i) a desired phase; (ii) a desired frequency; (iii) a change in phase; and (iv) a change in frequency.
[18]	The field programmable gate array system of claim 1, wherein adjustment information comprises a voltage.
[19]	The field programmable gate array system of claim 1, wherein adjustment information comprises a digital transmission.

No.	Limitation
[20]	The field programmable gate array system of claim 1, wherein the adjustment information is configured to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay.
[21]	The field programmable gate array system of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.
[22]	The field programmable gate array system of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.