

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

OPTIVER US LLC and OPTIVER TRADING US LLC,
Petitioners

v.

HFT SOLUTIONS, LLC,
Patent Owner.

Case No. IPR2026-00386
U.S. Patent No. 10,771,069

Petition for *Inter Partes* Review of U.S. Patent No. 10,771,069

Mail Stop **PATENT BOARD**
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

TABLE OF CONTENTS.....	i
TABLE OF EXHIBITS	iii
TABLE OF ABBREVIATIONS	iv
MANDATORY NOTICES.....	a
A. Real Parties-in-Interest: 37 C.F.R. §42.8(b)(1).....	a
B. Related Matters Under: 37 C.F.R. §42.8(b)(2)	a
1. Current Litigation.....	a
2. Administrative Proceedings	a
C. Lead and Back-Up Counsel: 37 C.F.R. §42.8(b)(3)	a
D. Service of Information: 37 C.F.R. §42.8(b)(4)	c
I. INTRODUCTION	1
II. REQUIREMENTS OF IPR.....	3
A. Standing: 37 C.F.R. §42.104(a).....	3
B. Identification of Challenge and Relief Requested: 37 C.F.R. §42.104(b)	3
1. R. Giordano and A. Aloisio, <i>Fixed-Latency, Multi- Gigabit Serial Links with Xilinx FPGAs</i> , 58-1 IEEE Transactions on Nuclear Science 194 (2011) (“Giordano”) (Ex. 1005)	4
2. Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 (“Virtex-UG”) (Ex. 1009).....	4
3. U.S. Pat. No. 7,453,301 (“Kaviani”) (Ex. 1010)	4
4. U.S. Pat. No. 10,447,463 (“Raymond”) (Ex. 1007)	4
C. Claim Construction: 37 C.F.R. §42.104(b)(3)	5
D. Challenge: 37 C.F.R. §42.104(b)(4).....	5
E. Supporting Evidence: 37 C.F.R. §42.104(b)(5)	5
F. Payment of Fees: 37 C.F.R. §§42.103, 42.15(a).....	6
III. PERSON OF ORDINARY SKILL IN THE ART (“POSITA”).....	6

IV.	STATE OF THE ART	6
1.	Giordano.....	7
2.	Virtex-UG	8
3.	Kaviani	9
4.	Raymond	9
V.	OVERVIEW OF THE '069 PATENT	11
A.	Summary of the Prosecution History of the '069 patent.....	11
VI.	DETAILED CHALLENGE	11
A.	Ground 1: Claims 1–19, 22 Are Rendered Obvious By Giordano in view of Kaviani.....	11
1.	Overview	11
2.	Analysis.....	18
B.	Ground 2: Claims 1–22 Are Rendered Obvious By Giordano in view of Kaviani and Raymond.....	66
1.	Overview	66
2.	Analysis.....	67
C.	Ground 3: Claims 1–19, 22 Are Rendered Obvious By Giordano in view of Kaviani further in view of Virtex-UG	72
1.	Overview	72
2.	Analysis.....	73
D.	Ground 4: Claims 1–22 Are Rendered Obvious By Giordano in view of Kaviani, Virtex-UG, and Raymond	73
1.	Overview	73
2.	Analysis.....	74
VII.	CONCLUSION.....	74
	APPENDIX: CHALLENGED CLAIM LISTING	77

TABLE OF EXHIBITS

Exhibit No.	Document
1001	U.S. Patent No. 10,771,069 (“the ’069 patent”)
1002	File History for U.S. Patent No. 10,771,069
1003	Declaration of Ben Carrion Schaefer, Ph.D.
1004	Declaration of Carrie Gardner
1005	R. Giordano and A. Aloisio, <i>Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs</i> , 58-1 IEEE Transactions on Nuclear Science 194 (2011) [Giordano]
1006	<i>(intentionally omitted)</i>
1007	U.S. Pat. No. 10,447,463 [Raymond]
1008	<i>(intentionally omitted)</i>
1009	Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 [Virtex-UG]
1010	U.S. Pat. No. 7,453,301 [Kaviani]
1011	Declaration of Gordon MacPherson

TABLE OF ABBREVIATIONS

Abbreviation	Term
'069 patent	U.S. Patent No. 10,771,069
AIA	America Invents Act
CDC	Clock Domain Crossing
CDR	Clock and Data Recovery
Challenged Claims	Claims 1–22 of U.S. Patent No. 10,771,069
DLL	Delay Locked Loop
Ex.	Exhibit
Fig.	Figure
FPGA	Field Programmable Gate Array
Giordano	R. Giordano and A. Aloisio, <i>Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs</i> , 58-1 IEEE Transactions on Nuclear Science 194 (2011)
IPR	<i>inter partes</i> review
Kaviani	U.S. Pat. No. 7,453,301
MAC	Media Access Controller
Patent Owner	HFT Solutions, LLC
PCS	Physical Coding Sublayer
Petitioners	Optiver US LLC and Optiver Trading US LLC
PLL	Phase Locked Loop
PMA	Physical Medium Attachment
Raymond	U.S. Pat. No. 10,447,463
VCO	Voltage Controlled Oscillator
Virtex-UG	Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009
VLSI	Very Large Scale Integration

MANDATORY NOTICES

A. Real Parties-in-Interest: 37 C.F.R. §42.8(b)(1)

Optiver US LLC and Optiver Trading US LLC are the real parties-in-interest. Optiver Services US LLC is a corporate affiliate and services entity supporting Optiver US LLC and Optiver Trading US LLC. The ultimate parent company of all three entities is Optiver Holding BV.

B. Related Matters Under: 37 C.F.R. §42.8(b)(2)

1. Current Litigation

The '069 patent is presently not subject to any litigation. Petitioners are not aware of any litigation involving the '069 patent.

2. Administrative Proceedings

There are no other administrative proceedings at issue. Petitioners have filed or intend to file petitions for *inter partes* review regarding four additional patents—U.S. Pat. Nos. 12,107,587 (IPR2026-00383); 10,763,865 (IPR2026-00384); 11,018,678 (IPR2026-00385); and 11,329,655 (IPR2026-00387)—in the same patent family as the '069 patent.

C. Lead and Back-Up Counsel: 37 C.F.R. §42.8(b)(3)

Petitioners provide the following designation of counsel:

Lead Counsel	Backup Counsel
Brian M. Buroker (Reg. No. 39,125) Gibson, Dunn & Crutcher LLP 1700 M St. NW Washington, D.C. 20036-4504 Tel: (202) 955-8500 bburoker@gibsondunn.com	Benjamin Hershkowitz (Reg. No. 41,833) Gibson, Dunn & Crutcher LLP 200 Park Avenue New York, NY 10166-0193 Tel: (212) 351-2339 bhershkowitz@gibsondunn.com
	Brian A. Rosenthal (<i>pro hac vice</i> motion requested) Gibson, Dunn & Crutcher LLP 200 Park Avenue New York, NY 10166-0193 Tel: (212) 351-2339 brosenthal@gibsondunn.com

Petitioners respectfully request authorization to file motions for Brian Rosenthal to appear before the USPTO *pro hac vice*. Mr. Rosenthal is an experienced attorney and is currently serving as lead counsel for Petitioners in an action between Petitioners and Patent Owner.¹ He is familiar with the subject matter at issue in this proceeding. Petitioners intend to file a motion to appear *pro hac vice* under 37 C.F.R. §42.10. Pursuant to 37 C.F.R. §42.10(b), powers of attorney accompany this petition.

¹ Petitioners are currently defending Patent Owner's assertion of U.S. Pat. Nos. 10,931,286; 11,128,305; 11,575,381 in *HFT Solutions, LLC v. Optiver US LLC and Optiver Trading US LLC*, 7:25-cv-415 (W.D. Tex. filed Sept. 8, 2025). These three patents list the same sole inventor (Nima Badizadegan) as the '069 patent but belong to a separate patent family.

D. Service of Information: 37 C.F.R. §42.8(b)(4)

Service of any documents via hand delivery may be made at the mailing address of lead and backup counsel. Petitioners also consent to electronic service, and service via electronic mail may be made at the email addresses provided for the lead and backup counsel.

I. INTRODUCTION

Pursuant to 35 U.S.C. §311, Petitioners seek *inter partes* review of U.S. Pat. No. 10,771,069 (Ex. 1001) and cancellation of claims 1–22 as unpatentable under 35 U.S.C. §103.

The Challenged Claims are directed to an FPGA system that receives and transmits data using synchronized receiver and transmitter clock signals. Ex. 1001, 1:49–53. The alleged invention of the '069 patent is in using an “internal phase-locked loop” for “*phase matching* receiver side and transmitter side clocks of a FPGA without introducing unnecessary delay in processing.” *Id.*, 2:9–12.² The Challenged Claims purport to achieve this phase matching with a “phase control circuit” that is “at least partially on the [FPGA].” *Id.*, cl. 1. This includes phase matching using a “phase detector” that is “not on the [FPGA].” *Id.*, cl. 22.

Yet the prior art taught these concepts before the '069 patent. **Giordano**, the primary reference for all grounds in this petition, teaches aligning clock signals for serialization/deserialization (“SER/DES”) processes with a deterministic, fixed phase difference. Ex. 1005, 197. Giordano plainly discloses performing everything in claims 1–19, 22 using Xilinx FPGA systems, but lacks certain details of off-FPGA components and how the phase alignment is achieved. **Kaviani**, a Xilinx patent, and

² Unless noted otherwise, emphasis added.

Virtex-UG, a Xilinx user guide, disclose these details. Kaviani discloses elements, implemented in separate circuitry, that disclose the “phase detector” off the FPGA. Virtex-UG teaches specifics of the clock phase alignment features inherent to the Virtex-5 FPGAs used in Giordano. Given the programmable nature of FPGAs (which allows users to modify hardware as needed) and Giordano’s guidance to seek further specifics of phase alignment, a POSITA would have found it obvious to incorporate the teachings of Kaviani and/or Virtex-UG into Giordano’s FPGA system. Ex. 1005, 198; Ex. 1010, 1:36–43, Fig. 2.

Claims 20 and 21 of the ’069 patent add only the application of these well-known FPGA systems to financial trading. **Raymond** expressly teaches using FPGA systems and phase matching (as in Giordano, Kaviani, and Virtex-UG) in high-frequency trading applications. Ex. 1007, 1:18–38. Applying the known FPGA phase matching teachings disclosed in Giordano, Kaviani, and Virtex-UG to financial-trading applications as suggested by Raymond would have been straightforward and obvious. *See also* Ex. 1001, 1:27–29 (“FPGAs are used in the financial industry”).

Because this Petition demonstrates a reasonable likelihood that Petitioners will prevail on at least one challenged claim based on prior art not considered during prosecution, the Board should institute *inter partes* review (“IPR”) and cancel claims 1–22 under 35 U.S.C. §103.

II. REQUIREMENTS OF IPR

A. Standing: 37 C.F.R. §42.104(a)

Petitioners certify that the '069 patent is eligible for IPR and that Petitioners are not barred or estopped from requesting IPR of the challenged claims.

B. Identification of Challenge and Relief Requested: 37 C.F.R. §42.104(b)

Petitioners request IPR of claims 1–22 of the '069 patent under AIA 35 U.S.C. §103.

The '069 patent issued from an application filed October 31, 2019, and claims priority to a provisional application filed February 21, 2019. For purposes of this Petition only, Petitioners do not dispute that the Challenged Claims are entitled to an effective filing date of February 21, 2019.

Petitioners request cancellation of claims 1–22 based on:

Ground	Claims	Basis for Rejection³
1	1–19, 22	Obviousness over Giordano in view of Kaviani
2	1–22	Obviousness over Giordano in view of Kaviani further in view of Raymond
3	1–19, 22	Obviousness over Giordano in view of Kaviani further in view of Virtex-UG ⁴

³ All obviousness grounds include the knowledge of POSITA.

⁴ Giordano inherently discloses the features of Virtex-UG, and further incorporates Virtex-UG by reference. Ex. 1003, ¶¶77, 118. If necessary, a POSITA would have been motivated to combine Virtex-UG to all grounds based on Giordano.

Ground	Claims	Basis for Rejection ³
4	1–22	Obviousness over Giordano in view of Kaviani, Virtex-UG, and Raymond

1. R. Giordano and A. Aloisio, *Fixed-Latency, Multi-Gigabit Serial Links with Xilinx FPGAs*, 58-1 IEEE Transactions on Nuclear Science 194 (2011) (“Giordano”) (Ex. 1005)

Giordano was published in IEEE Transactions on Nuclear Science on January 28, 2011. Ex. 1004, ¶¶21–26; *id.*, ¶27, 33–34, 37 (citing Ex. 1011). Giordano qualifies as prior art under AIA 35 U.S.C. §102(a)(1). Giordano was neither cited nor considered during prosecution of the ’069 patent.

2. Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), December 3, 2009 (“Virtex-UG”) (Ex. 1009)

Virtex-UG was published on December 3, 2009. Ex. 1004, ¶¶41–47. Virtex-UG therefore qualifies as prior art under AIA 35 U.S.C. §102(a)(1). Virtex-UG was neither cited nor considered during prosecution of the ’069 patent.

3. U.S. Pat. No. 7,453,301 (“Kaviani”) (Ex. 1010)

Kaviani, titled “Method of and Circuit for Phase Shifting a Clock Signal,” was filed August 5, 2005, and granted November 18, 2008. Kaviani therefore qualifies as prior art under AIA 35 U.S.C. §102(a)(1) and §102(a)(2). Kaviani was neither cited nor considered during prosecution of the ’069 patent.

4. U.S. Pat. No. 10,447,463 (“Raymond”) (Ex. 1007)

Raymond, titled “Device and Method for Ultra-low Latency Communication,” claims priority to a provisional application filed July 13, 2017,

and an application filed July 13, 2018. Raymond therefore qualifies as prior art under AIA 35 U.S.C. §102(a)(2). Raymond was neither cited nor considered during prosecution of the '069 patent.

C. Claim Construction: 37 C.F.R. §42.104(b)(3)

Petitioners submit that no construction of any claim term is necessary for the Board to resolve, and the Challenged Claims would have been obvious under any reasonable construction.

D. Challenge: 37 C.F.R. §42.104(b)(4)

Explanation of how the Challenged Claims are unpatentable under the grounds identified above, including where each claim element is found in the prior art, is provided below.

E. Supporting Evidence: 37 C.F.R. §42.104(b)(5)

The supporting exhibits, their relevance to the challenged claims, and the specific portions supporting the asserted grounds are identified below. The Petition's technical analysis and grounds are further supported by the Declaration of Dr. Ben Carrion Schaefer (Ex. 1003). The public availability of the cited prior art is further supported by the Declaration of Carrie Gardner (Ex. 1004), which further includes cites to the Declaration of Gordon MacPherson (Ex. 1011).

A List of Exhibits is included pursuant to 37 C.F.R. §42.63(e).

F. Payment of Fees: 37 C.F.R. §§42.103, 42.15(a)

The required fee was submitted. The Office is authorized to charge any fee deficiency, or credit overpayment, to Deposit Account 50-1408, including additional fees related to this Petition.

III. PERSON OF ORDINARY SKILL IN THE ART (“POSITA”)

A POSITA, on February 21, 2019, would have a Bachelor’s degree in Computer Engineering, Electrical Engineering, or equivalent discipline, and at least three years of academic or industry experience on clocking techniques for FPGAs with high-speed transceivers. Educational requirements may be substituted by work experience, and vice versa.

IV. STATE OF THE ART

By February 21, 2019, FPGA-based communication systems were highly developed, and components such as SERDESEs, PLLs, DLLs, CDRs, and phase-alignment mechanisms were standard FPGA features. Ex. 1001, 1:41–43; Ex. 1003, ¶¶86–87. Commercial user guides, such as Virtex-5 RocketIO GTP Transceiver User Guide (“Virtex-UG”), document many of these features. Ex. 1003, ¶88.

Commercial FPGA transceivers already implemented integrated serialization and deserialization using parallel-in/serial-out (PISO) and serial-in/parallel-out (SIPO) circuitry. Ex. 1009, 104; Ex. 1003, ¶¶88–89. The transceivers interfaced directly with FPGA programmable logic through user-accessible clock and data

interfaces, enabling custom processing of deserialized data. Ex. 1005, 194–95; Ex. 1003, ¶¶88–90.

1. Giordano

Giordano presents “a link architecture” using “GTP transceiver” of the “Xilinx Virtex 5 FPGA family.” Ex. 1005, 194. Giordano explains that transceivers are implemented as “configurable hard-macros (or ‘tiles’),” with each tile including a receiver and a transmitter. *Id.* Each receiver and transmitter has a Physical Medium Attachment (PMA) sublayer for serialization (in transmitter PMA) or deserialization (in receiver PMA), and a Physical Coding Sublayer (PCS) for processing data. *Id.*

Giordano also describes an FPGA Fabric with programmable hardware, which can implement user-programmed circuits such as “Comma Detect and Align” circuits and DLLs. *Id.*, 197–199. Figure 1 below shows Giordano’s architecture:

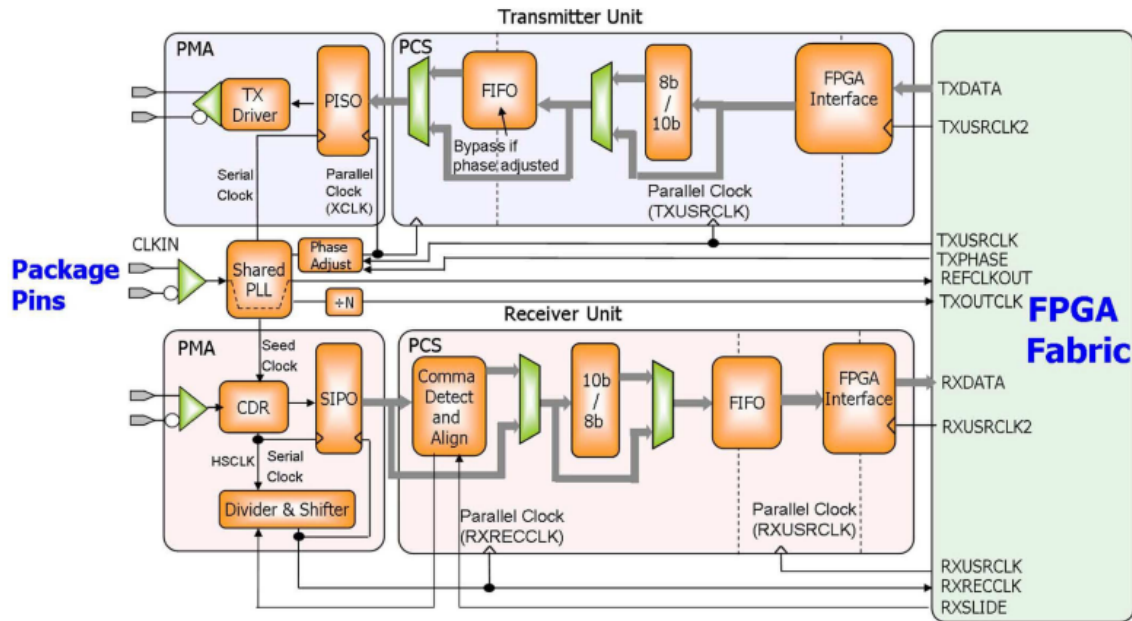


Fig. 1. Simplified block diagram of the GTP transceiver. Half a tile is shown.

2. Virtex-UG

Virtex-UG is Xilinx’s Virtex-5 FPGA RocketIO GTP Transceiver User Guide, UG196 (v2.1), dated December 3, 2009, hence it was publicly available before Giordano. Ex. 1009, 1; Ex. 1004, ¶¶41–47. Virtex-UG states that it “shows how to use the RocketIO™ GTP transceivers in Virtex®-5 FPGAs,” and describes the GTP transceiver as a power-efficient, highly configurable transceiver “tightly integrated with the programmable logic resources of the FPGA.” Ex. 1009, 17, 23. The GTP transceiver supports line rates from 100 Mb/s to 3.75 Gb/s, optional PCS features such as 8b/10b encoding, comma alignment, channel bonding, and clock correction, and “fixed latency modes for minimized, deterministic datapath latency.” *Id.*, 23. The guide also explains that GTP transceivers are placed as dual-transceiver GTP_DUAL tiles in Virtex-5 LXT and SXT devices, allowing two transceivers to

share a single PLL with the TX and RX functions of both, which is just how Giordano describes its use of the Virtex 5 FPGA. *Id.*, 24; Ex. 1005, 194.

3. Kaviani

Kaviani (U.S. Pat. No. 7,453,301) explains that “DLLs in the Virtex or Spartan Field Programmable Gate Array (FPGA) product series from Xilinx” are clock-management systems used for “deskewing and phase shifting.” Ex. 1010, 1:44–49. Kaviani explains that integrated circuits “such as a programmable logic device (PLD)” receive “external reference clock signals” to generate “internal clock signals,” which “must be carefully controlled to ensure proper timing,” and that it is “important” for generated clock signals to be “maintained accurately at the specified phase and frequency.” *Id.*, 1:13–17, 1:34–38. Kaviani further discloses a control circuit that “generate[s] delay select values,” provides “synchronization of the digital delay lines to avoid delay select set up and hold times.” *Id.*, 4:8–4:11.

4. Raymond

Raymond (U.S. Pat. No. 10,447,463) explains that “[u]ltra-low latency communication is critical” for electronic trading and that trading firms use FPGAs to improve throughput and latency. Ex. 1007, 1:18–24. Raymond discusses processing incoming financial trading data, exchanged with financial exchanges. *Id.*, 4:52–59.

V. OVERVIEW OF THE '069 PATENT

A. Summary of the Prosecution History of the '069 patent

The application for the '069 patent was filed on October 31, 2019. Initially the Examiner rejected claims 1–22 as obvious over Figure 1 of the application (as admitted prior art) in view of Law (U.S. Pat. No. 7,668,524). Ex. 1002, 86–98.

In response, Applicant amended claim 1 to require that “the computational circuitry performs the first set of operations to generate the second plurality of parallel processed data without use of a clock domain crossing circuit.” Ex. 1002, 39. Applicant argued that Law did not disclose a phase-control circuit provided on an FPGA and distinguished the prior-art FPGA architecture depicted in the application as relying on a clock domain crossing circuit. *Id.*, 44–45.

The Examiner allowed claims 1–22, specifically citing the newly added limitation requiring operation “without use of a clock domain crossing circuit.” Ex. 1002, 18–19.

VI. DETAILED CHALLENGE

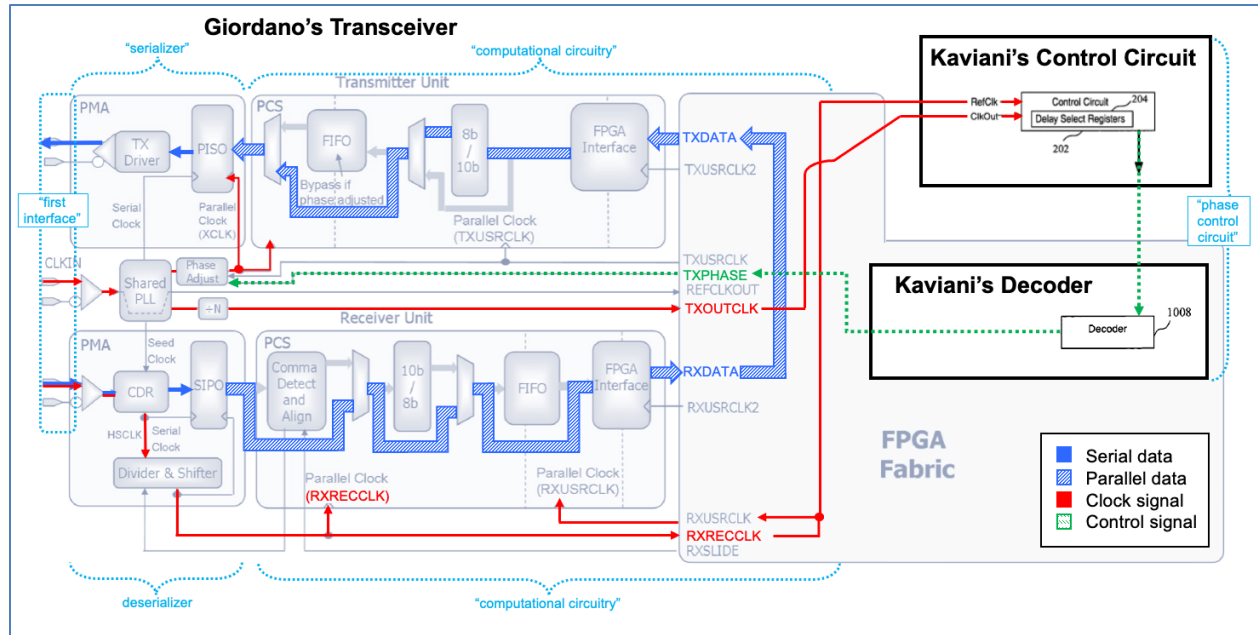
A. Ground 1: Claims 1–19, 22 Are Rendered Obvious By Giordano in view of Kaviani

1. Overview

Giordano’s FPGA comprises two portions—Xilinx Virtex-5 “RocketIO” GTP transceiver (with separate receiver and transmitter sides) and FPGA Fabric. Ex. 1005, 195. The GTP transceiver comprises preprogrammed, fixed (but configurable

with operating parameters and settings by user) hardware commonly referred to as hard-macro tiles. *Id.*, 194; Ex. 1003, ¶104. In contrast, FPGA Fabric comprises user-modifiable, programmable hardware. *Id.* Giordano also discloses using FPGA circuit boards and configuring circuit boards for specific applications / experiments. Ex. 1005, Fig. 6; Ex. 1003, ¶¶105-108, 115.

The annotated image below, based on Figure 1 of Giordano and Figures 2 and 10 of Kaviani with modifications, depicts this proposed combination:



Giordano's GTP transceiver generates a receiver side clock signal, RXRECCLK, from the clock extracted from the incoming serial data. Ex. 1003, ¶¶107-08. Giordano's Shared PLL (and related clock components such as Phase Adjustment Circuit and divider) generates a transmitter side clock signal TXUSRCLK. TXUSRCLK then goes to the transmitter PMA and related PLLs,

resulting in TXOUTCLK. Kaviani's Control Circuit, implemented on the circuit board and off the FPGA, receives both RXRECCLK and TXOUTCLK to generate control signals and information to phase-match clock signals. Ex. 1003, ¶108. This results in RXRECCLK and TXOUTCLK being phase matched. *Id.*

a. Motivation to Combine Giordano and Kaviani

A POSITA would have been motivated to combine Giordano and Kaviani because they address synchronization and phase alignment of clock signals in FPGA transceivers. Ex. 1003, ¶¶109-10. Giordano seeks fixed-latency timing synchronization and clock distribution in Xilinx Virtex-5 GTP transceivers, while Kaviani is a Xilinx patent concerning "phase shifting of a generated clock signal." Ex. 1005, 194; Ex. 1010, Abstract.

Giordano identifies the need that Kaviani's phase alignment teachings fulfill. While Giordano's fixed latency architecture achieves deterministic (*i.e.*, fixed) phase relationships between the receiver clock and transmit clock, Giordano identifies gaps for directly using this receiver clock for the transmitter. Ex. 1005, 198; Ex. 1003, ¶¶110-11. Giordano states:

The clock recovered by the receiver cannot be directly used as a reference clock for the re-transmission. In fact, the internal PLL is shared among the transmitters and receivers in the same tile and at the receiver tile it is already locked to the seed clock. Moreover, the recovered clock might also require to be filtered in order to match the jitter specifications for the GTP reference clock

Ex. 1005, 198. Kaviani provides precisely such a solution through a phase shifting circuit that filters jitter and generates a transmit clock “phase aligned and frequency aligned with the reference clock signal.” Ex. 1010, 1:36–43

A POSITA reading Giordano would have naturally consulted Xilinx’s own materials (such as Kaviani, a Xilinx patent), for a DLL-based phase alignment solution. Giordano uses a Xilinx Virtex FPGA, a chip that Kaviani mentions as well. Ex. 1005, 194, 197–199; Ex. 1010, 1:44–49; Ex. 1003, ¶113.

Incorporating Kaviani’s phase shifting teachings into Giordano would require routine programming of FPGA Fabric logic and conventional circuit element modifications. Ex. 1003, ¶114.

Giordano itself demonstrates programming custom hardware in the FPGA Fabric, and further using elements on the circuit board as needed. For example, Giordano implemented a custom Comma Detector and Aligner in the FPGA Fabric because the GTP’s built-in comma detector (which is a fixed block inside the transceiver) did not support the particular operations the user needed. Ex. 1005, 198; Ex. 1003, ¶115. Giordano also discloses implementing DLL blocks “external to the GTP” transceiver, *i.e.*, on the FPGA Fabric. Ex. 1005, Fig. 5; Ex. 1003, ¶115. Similarly, Giordano discusses configuring the circuit boards for experimental setups. Ex. 1005, 198; Ex. 1003, ¶115. Kaviani describes its Clock Generator (which includes multiple decoders) and Control Circuit as separate circuits, supporting these

are implementable in different physical regions. Ex. 1010, Fig. 2; Ex. 1003, ¶115. Implementing components of Kaviani's Clock Generator (such as decoders) in the FPGA Fabric and Control Circuit in the circuit board thus represents a straightforward extension of techniques already used in Giordano. *Id.*

Such FPGA hardware programming is how the '069 patent suggests implementing its claimed invention, which programs components such as phase detector, phase controller, DLL, and PLL in a "FPGA Core." Ex. 1001, Figs. 3A–F, 4A–C, 5A–F; Ex. 1003, ¶116. This FPGA Core includes logic elements, DSP blocks, clock distribution components, and memories, mirroring Giordano's FPGA Fabric. Ex. 1001, 26:26–44; Ex. 1003, ¶116.

A POSITA would have had a reasonable expectation of success. Giordano's FPGA implementation was physically tested on Xilinx evaluation boards and used circuit blocks similar to those disclosed in Kaviani, including PLLs, DLLs, serializers, and pattern generators which were implemented on the programmable FPGA Fabric as the user intended. Ex. 1005, 195, 197–200; Ex. 1003, ¶117. Because both references rely on the same Xilinx FPGA infrastructure, there would have been high expectation that, through routine FPGA programming, the combination functions as intended. Ex. 1003, ¶117.

b. Features of Virtex-UG are Inherent to Giordano, and Giordano Incorporates Virtex-5 GTP by Reference

Giordano presents a system with the “RocketIO” GTP transceiver of the Xilinx Virtex 5 FPGA family. Ex. 1005, 194, 199. Giordano repeatedly references the RocketIO GTP Transceiver, for example referencing the overall transceiver architecture (*id.*, 195) and taking estimated latencies values from the RocketIO GTP Transceiver User Guide (*id.*, 198). Giordano further describes phase alignment of clock signals, and that “the procedure we follow for activating the alignment circuit is the one suggested in the GTP user’s guide.” *Id.*, 197. A POSITA would have known to reference Xilinx documents on the GTP transceiver to understand the relevant inherent features. Ex. 1003, ¶118. As such, Giordano inherently discloses the features of Virtex-UG. *Id.*

In such case, the features of the Virtex-UG are necessarily present in Giordano, and it is proper to use extrinsic evidence (such as the Virtex-UG) to understand said features. *See Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1328 (Fed. Cir. 2001) (“[R]ecourse to extrinsic evidence is proper to determine whether a feature, while not explicitly discussed, is necessarily present in a reference. The evidence must make clear that the missing feature is necessarily present, and that it would be so recognized by persons of ordinary skill in the relevant art.”); *Sage Prods., LLC v. Stewart*, 133 F.4th 1376, 1385 (Fed. Cir. 2025) (“There was likewise nothing improper in the Board relying on evidence outside of the PAR

to make findings as to what the skilled artisan would understand the PAR to be disclosing.”); *Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1345 (Fed. Cir. 2018) (“It is well established that such reliance on extrinsic evidence is proper in an inherency analysis.”); *see also In re Haines*, No. 2024-2338, 2025 WL 1403578, at *2 (Fed. Cir. May 15, 2025) (examiner properly used another publication “as evidence to explain why [the prior art’s] disclosure of a mass spectrometer implicitly discloses ‘obtaining mass spectral channel signals (m/z)’” (cleaned up)).

For the same reasons as above, Giordano incorporates Virtex-UG (Ex. 1009) by reference. Ex. 1005, 197 (“the procedure we follow for activating the alignment circuit is the one suggested in the GTP user’s guide.”). Virtex-UG, by incorporation, becomes part of the disclosures of Giordano. *Verizon Connect Inc. v. Omega Patents, LLC*, IPR2023-01162, 2024 WL 714951, at *3, 14-15 (P.T.A.B. Feb. 21, 2024) (the incorporated secondary reference’s disclosures become part of the primary reference); *Paice LLC v. Ford Motor Co.*, 881 F.3d 894, 906-07 (Fed. Cir. 2018) (“[T]he standard of one reasonably skilled in the art should be used to determine whether the host document describes the material to be incorporated by reference with sufficient particularity.”) (citing *Advanced Display Systems, Inc. v. Kent State University*, 212 F.3d 1272 (2000)); Ex. 1003, ¶118.

2. Analysis

a. Independent Claim 1

[1.pre]: A field programmable gate array system comprising:

To the extent limiting, Giordano discloses [1.pre]. Ex. 1003, ¶¶119-20.

Giordano discloses Xilinx Virtex-5 FPGA on FPGA boards for experimentally testing its proposed architecture. Ex. 1005, 198. FPGA board, where the FPGA is physically installed in, discloses the claimed “[FPGA] system.” Ex. 1003, ¶120.

[1.a]: (a) a field programmable gate array comprising:

Giordano discloses Xilinx Virtex-5 FPGA, which discloses the claimed “field programmable gate array.” Ex. 1005, 194; Ex. 1003, ¶¶ 121-22.

[1.b]: (1) a first interface comprising:

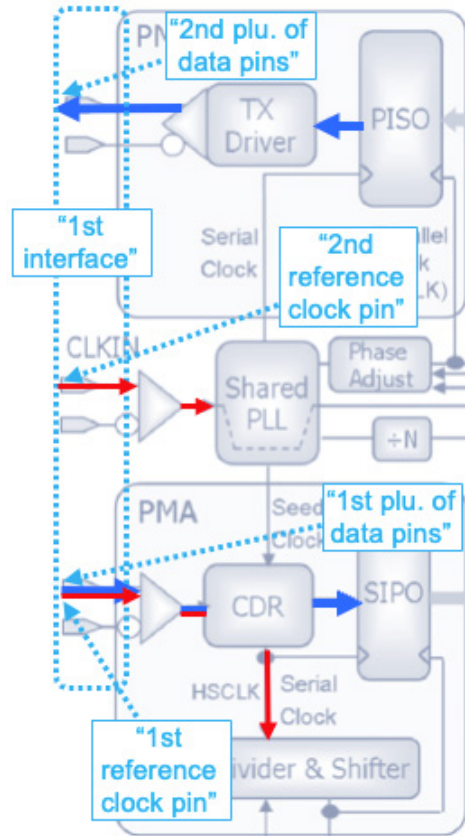
(A) a first reference clock pin, wherein said first reference clock pin is configured to receive a first clock signal having a first frequency and a first phase;

(B) a second reference clock pin, wherein said second reference clock pin is configured to receive the first clock signal.

(C) a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream;

(D) a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream;

Giordano discloses [1.b]. Ex. 1003, ¶123. The image below, based on Giordano Figure 1 with additional annotations, shows the portions of the Giordano-Kaviani combination relevant to the claimed “first interface”:



For “first interface,” Giordano’s FPGA package pins, which interface external signals with the FPGA, disclose the “first interface.” Ex. 1005, 195; Ex. 1003, ¶¶124-25.

Giordano discloses the GTP transceiver, which includes separate “Receiver Unit” and “Transmitter Unit.” Ex. 1005, 194. Within each receiver- and transmitter-unit are a Physical Medium Attachment (“PMA”) and Physical Coding Sublayer (“PCS”). *Id.*, 194–195. Giordano points to the PMA sublayer as the component “actually serializing and de-serializing the data,” and the PCS layer as “processing” data. *Id.*, 194.

Giordano discloses package pins that interface both Receiver Unit PMA and Transmitter Unit PMA with external components, which disclose the claimed “first interface.” Ex. 1005, Fig. 1; Ex. 1003, ¶¶125-26.

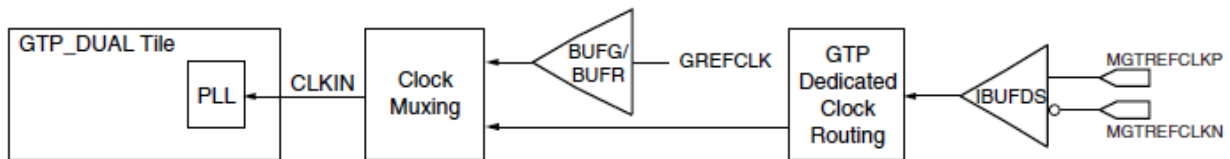
For “first reference clock pin,” Giordano’s FPGA pins into the Receiver Unit PMA, specifically that for the signal from which HSCLK is recovered, discloses the “first reference clock pin.” Ex. 1005, 195; Ex. 1003, ¶127.

Giordano’s Receiver Unit PMA has a Clock and Data Recovery (“CDR”) block, “which extracts a clock (HSCLK)” from the incoming serial data stream. Ex. 1005, 195. HSCLK discloses the “first clock signal,” and also “first frequency” and “first phase.” *Id.* The package pin that receives this incoming signal discloses “first reference clock pin.”

This mirrors the ’069 patent, which describes a receiver PMA further comprising a CDR block. Ex. 1001, 53:11–14, Fig. 6E. Like Giordano, the CDR block of the ’069 patent receives serial data, and extracts a clock signal from the incoming serial data. Ex. 1001, 53:17–27; Ex. 1003, ¶128.

For “second reference clock pin,” Giordano’s FPGA pin for CLKIN discloses the “second reference clock pin.” Ex. 1005, 197; Ex. 1003, ¶129. In the proposed combination, this CLKIN pin is connected to another GTP transceiver to extract the same HSCLK signal (“first clock signal”) as provided to the “first reference clock pin.” *Id.*

Virtex-UG further discloses⁵ the “second reference clock pin” and “first clock signal.” Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses this limitation. Ex. 1003, ¶¶130. Virtex-UG discloses three different options for CLKIN, depicted in Figure 5-3 of Virtex-UG below (where CLKIN for the GTP transceiver is noted on the left side, with the Shared PLL denoted as “PLL”):



The three options are using an external oscillator (referring to “MGTREFCLK”), using another neighboring GTP transceiver (referring to the “GTP Dedicated Clock Routing” block), and using a clock from inside the FPGA (referring to “GREFCLK”). Ex. 1009, 80; Ex. 1003, ¶131.

The second GTP Dedicated Clock Routing mode, where a neighboring GTP transceiver extracts the HSCLK clock from incoming data, and then providing to CLKIN port of the proposed combination, discloses the limitations regarding the “second reference clock pin” receiving the “first clock signal.” Ex. 1003, ¶132.

⁵ The Virtex-UG’s disclosures discussed in this Petition are express. In addition, Giordano inherently discloses Virtex-UG’s express disclosures.

For “first plurality of data pins,” Giordano discloses package pins that interface the Receiver Unit PMA with external components, which disclose the claimed “first plurality of data pins.” Ex. 1005, Fig. 1; Ex. 1003, ¶133. This Receiver Unit PMA receives incoming serial data, which discloses the “first serial data stream.” Ex. 1005, 195; Ex. 1003, ¶133.

This mirrors the '069 patent, which describes a deserializer with a receiver PMA. Ex. 1001, 53:11–14, Fig. 6E; Ex. 1003, ¶134.

For “second plurality of data pins,” Giordano’s FPGA pins out from the Transmitter Unit PMA discloses the “second plurality of data pins.” Ex. 1005, 195; Ex. 1003, ¶135.

Giordano’s Transmitter Unit PMA discloses a Parallel Input to Serial Output (“PISO”) block that converts parallel data to serial data. Ex. 1005, 195; Ex. 1003, ¶136. The serial data output of PISO discloses the “second serial data stream.” Ex. 1003, ¶136. This output is sent to the transmitter driver, which is then sent outside the FPGA through package pins. Ex. 1005, Fig. 1; Ex. 1003, ¶136.

This mirrors the '069 patent, which describes a serializer with a transmitter PMA with a Parallel to Serial block. Ex. 1001, 53:55–54:8, Fig. 7B. Like Giordano, this Parallel to Serial block converts the incoming parallel data to serial data. *Id.*; Ex. 1003, ¶137.

[1.c]: (2) a deserializer operationally connected to:

(A) the first reference clock pin to receive as a first input the first clock signal and

(B) the first plurality of data pins to receive as a second input the first serial data stream,

Giordano's Receiver Unit PMA discloses the claimed "deserializer." Ex. 1003, ¶¶138-40. As discussed in [1.b], Giordano's FPGA pins into the Receiver Unit PMA discloses the "first reference clock pin" and the "first plurality of data pins."

For "as a first input", Giordano's Receiver Unit PMA has a Clock and Data Recovery ("CDR") block, "which extracts a clock (HSCLK)" from the serial data stream coming through the FPGA package pins ("first reference clock pin"). Ex. 1005, 195. As such, HSCLK is sent with the serial data from the package pins to this CDR, which discloses receiving "as a first input" HSCLK (*i.e.*, "first clock signal"). *Id.*; Ex. 1003, ¶141.

This mirrors the '069 patent, which describes a deserializer with a receiver PMA. Ex. 1001, 53:11-14, Fig. 6E. This receiver PMA further comprises a CDR block. *Id.* Like Giordano, the CDR block of the '069 patent receives serial data, and extracts a clock signal from the incoming serial data. Ex. 1001, 53:17-27; Ex. 1003, ¶142.

For "as a second input", Giordano's Receiver Unit PMA includes a "Serial In to Parallel Output (SIPO)" block, which deserializes serial data incoming via the

FPGA package pins (“first plurality of data pins”). Ex. 1005, 195–196; Ex. 1003, ¶ 143. The package pins transmit the incoming serial data to the Receiver Unit PMA, which discloses receiving “as a second input” incoming serial data (*i.e.*, “first serial data stream”). Ex. 1005, 195, Ex. 1003, ¶ 143.

This mirrors the ’069 patent, which describes a receiver PMA that receives serial data. Ex. 1001, 53:10–27, Fig. 6E; Ex. 1003, ¶ 144.

[1.d]: and wherein the deserializer is configured to:

(A) convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams, and

(B) generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase; and

(C) transmit the first plurality of parallel data streams and the first receiver side clock signal within the field programmable gate array;

As discussed in [1.c], Giordano’s Receiver Unit PMA discloses the claimed “deserializer.”

For sub-element (A), as discussed in [1.b], the serial data into Giordano’s Receiver Unit PMA discloses the “first serial data stream.”

Giordano’s SIPO block output discloses the “first plurality of parallel data streams,” and the output’s data size discloses the “first amount of data streams.” Ex. 1003, ¶146.

Giordano’s Receiver Unit PMA has a SIPO block that converts incoming serial data to parallel data, which discloses this sub-element. Ex. 1005, 195; Ex.

1003, ¶146. Giordano's SIPO block output, further processed by the Receiver Unit PCS, discloses the "first plurality of parallel data streams" (where the bit size of said parallel data discloses "first amount of data streams"). Ex. 1005, 195; Ex. 1003, ¶146.

This mirrors the '069 patent, which describes a Serial to Parallel block within the Receiver PMA that "converts the serial data into parallel data, transmitting the parallel data to the receiver PCS." Ex. 1001, 53:23–27, Fig. 6E; Ex. 1003, ¶147.

For sub-element (B), as discussed in [1.b], HSCLK (which is the same as CLKIN) discloses the "first clock signal."

Giordano's parallel recovered clock (RXRECCLK) discloses the "first receiver side clock signal." Ex. 1003, ¶148. RXRECCLK discloses the "third frequency" and "third phase." *Id.*

The CDR in Giordano's Receiver Unit PMA extracts a clock (HSCLK) signal from the incoming serial data. Ex. 1005, 195. HSCLK is then used to "generate a parallel recovered clock (RXRECCLK)" for the SIPO block and Receiver Unit PCS. *Id.*; Ex. 1003, ¶149. This RXRECCLK discloses the claimed "first receiver side clock signal," and the frequency and phase of RXRECCLK disclose the claimed third frequency and phase. *Id.*

This mirrors the '069 patent, which describes a CDR that receives serial data, and generates clock signals for blocks such as Serial to Parallel and receiver PCS. Ex. 1001, 53:17–27, Fig. 6E; Ex. 1003, ¶150.

For sub-element (C), Giordano discloses this sub-element. Ex. 1003, ¶151.

Giordano discloses providing RXRECCLK (*i.e.*, “receiver side clock signal”) to the Receiver Unit PCS and FPGA Fabric. Ex. 1005, 195; Ex. 1003, ¶151. Giordano discloses providing the SIPO block output to be further processed by PCS (both receiver and transmitter sides) and logic implemented on FPGA Fabric. Ex. 1005, 195, Fig. 1; Ex. 1003, ¶151.

[1.e]: (3) computational circuitry operationally connected to the deserializer to receive the first plurality of parallel data streams and the first receiver side clock signal, wherein the computational circuitry is configured to perform a first set of operations on the first plurality of parallel data streams to generate a second plurality of parallel processed data streams having a second amount of data streams and the computational circuitry performs the first set of operations to generate the second plurality of parallel processed data without use of a clock domain crossing circuit;

Giordano discloses [1.e]. Ex. 1003, ¶152.

As discussed in [1.c] and [1.d], Giordano’s Receiver Unit PMA discloses the claimed “deserializer,” SIPO block output discloses the “first plurality of parallel data streams,” and parallel recovered clock (RXRECCLK) discloses the “first receiver side clock signal.” Ex. 1003, ¶152.

Giordano’s Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS individually and collectively disclose the “computational circuitry.” Ex. 1003, ¶153.

These blocks, as seen in the proposed combination image, receive deserialized parallel data from the SIPO block (which is within the Receiver Unit PMA, *i.e.*, “deserializer”) and are along the data path between the receiver side SIPO and transmitter side PISO, hence are “operationally connected” to the “deserializer.” Ex. 1003, ¶154.

Giordano’s processed parallel data exiting the Transmitter Unit PCS into the Transmitter Unit PMA discloses the “second plurality of parallel processed data streams” (where the bit size of said parallel data discloses “second amount of data streams”). Ex. 1005, Fig. 1; Ex. 1003, ¶154.

For “first set of operations,” Giordano discloses logic operations in the FPGA Fabric and the PCS layers (both receiver and transmitter). Giordano’s Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS individually and collectively disclose the “computational circuitry.” Ex. 1003, ¶155.

Giordano points to the PCS layer (both receiver and transmitter sides) as “processing” data, disclosing computational circuitry. Ex. 1005, 194; Ex. 1003, ¶156. The PCS layer includes 8b/10b encoding / decoding functions, which requires arithmetic calculations hence disclosing the “first set of operations.” Ex. 1005, 197; Ex. 1003, ¶156.

Giordano also describes FPGA Fabric as including “logic” which discloses the claimed “first set of operations.” Ex. 1005, 195–196, 198; Ex. 1003, ¶155.

Giordano describes programming a Comma Detector and Aligner in the FPGA Fabric, which performs “comma detection.” Ex. 1005, 198; Ex. 1003, ¶155. Giordano’s “comma detector looks for commas (*e.g.*, the one included in the K28.5 symbol) and when it finds one it determines how many bit shifts” are “required in order to align the parallel data.” Ex. 1005, 198; Ex. 1003, ¶155. A POSITA would have understood this pattern matching operation (to locate comma characters) and computing number of bit shifts for alignment to disclose the claimed “first set of operations.” *Id.*

This mirrors the ’069 patent, with figures depicting computational circuitry capable of performing logical operation as “Computation Logic.” Ex. 1001, Figs. 4B–C, 5A–F.

For “second plurality of parallel processed data streams,” Giordano’s Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS process parallel data, which is then transmitted from the Transmitter Unit PCS into the Transmitter Unit PMA. This processed parallel data discloses this limitation. Ex. 1005, Fig. 1; Ex. 1003, ¶158.

For “without use of a clock domain crossing circuit,” Giordano discloses this requirement. Ex. 1003, ¶159.

Giordano discloses bypassing First In First Out (FIFO) buffer, a circuit block allowing safe data transfer between different clock domains (*e.g.*, “data transfers

between TXUSRCLK domain and the XCLK domain”). Ex. 1005, 195; Ex. 1003, ¶160. A POSITA would have understood FIFO as a clock domain crossing circuit, and Giordano’s bypassing of the FIFO block discloses this limitation. *Id.*

Giordano discloses bypassing FIFO buffer by having the two clock domains have “the same phase” and “therefore also the same latency for the data.” Ex. 1005, 195; Ex. 1003, ¶161. In the transmitter, Giordano discusses two clocks (XCLK and TXUSRCLK) that are adjusted to have the same frequency and phase. Ex. 1005, 195. The transmitter has a FIFO block for crossing between XCLK and TXUSRCLK clock domains. *Id.*; Ex. 1003, ¶161. Giordano discloses bypassing this FIFO block by using a phase alignment option provided in Xilinx Virtex-5 FPGA systems. Ex. 1005, 195; Ex. 1003, ¶161. Through this built-in phase alignment, XCLK and TXUSRCLK are phase aligned, in which “the transmit FIFO is unnecessary and therefore we bypassed it.” Ex. 1005, 197.

Virtex-UG further discloses “without use of a clock domain crossing circuit.” Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses this limitation. Ex. 1003, ¶162.

In the receiver, Virtex-UG confirms this FIFO bypass. When receiver clock phase alignment is used, “RXUSRCLK must be driven directly from RXRECCLK using a BUFR regional clock buffer.” Ex. 1009, 179 (“Using RX Phase Alignment to Bypass the RX Elastic Buffer”). Due to phase alignment, “SIPO parallel clock

phase matches RXUSRCLK phase” and there is “no phase difference between XCLK and RXUSRCLK.” *Id.*, 180. With no phase difference, the RX Elastic Buffer (which is the FIFO block described in Giordano) is bypassed. This bypass is described in the red arrow below in Figure 7-22 of Virtex-UG:

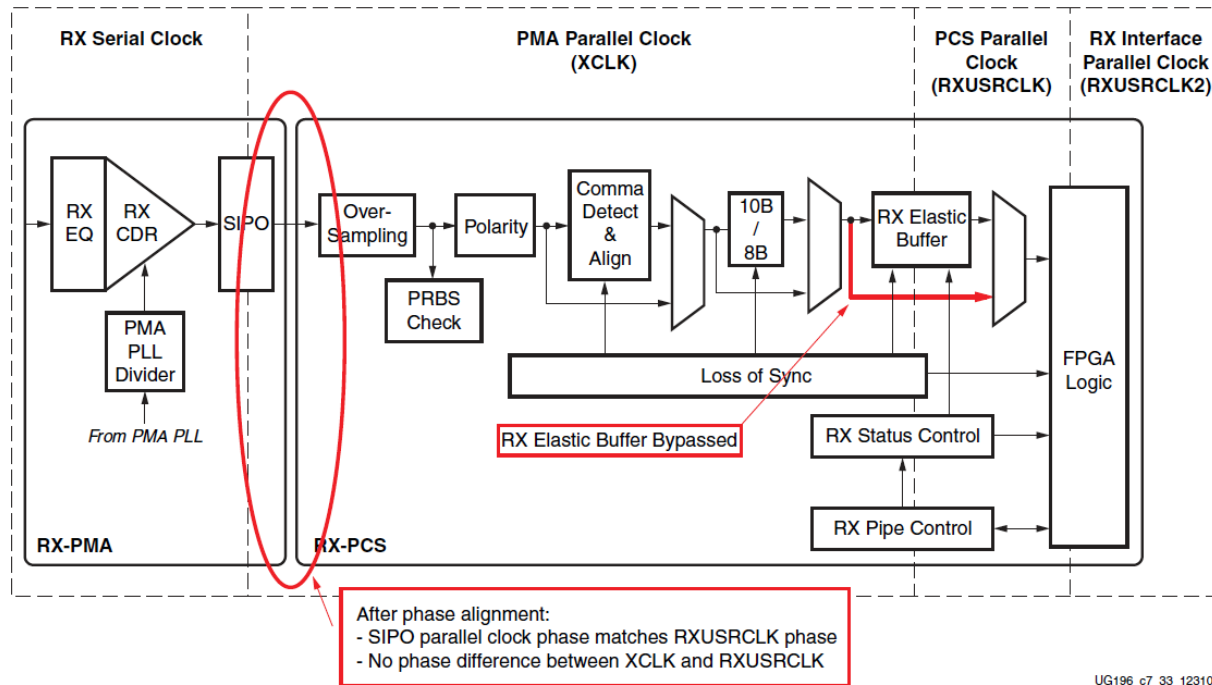


Figure 7-22: Using Phase Alignment

[1.f]: (4) a serializer operationally connected to:

(A) an adjustable transceiver phase lock loop to receive as a third input a first wire rate clock signal, wherein the first wire rate clock signal has a fourth frequency and a fourth phase;⁶

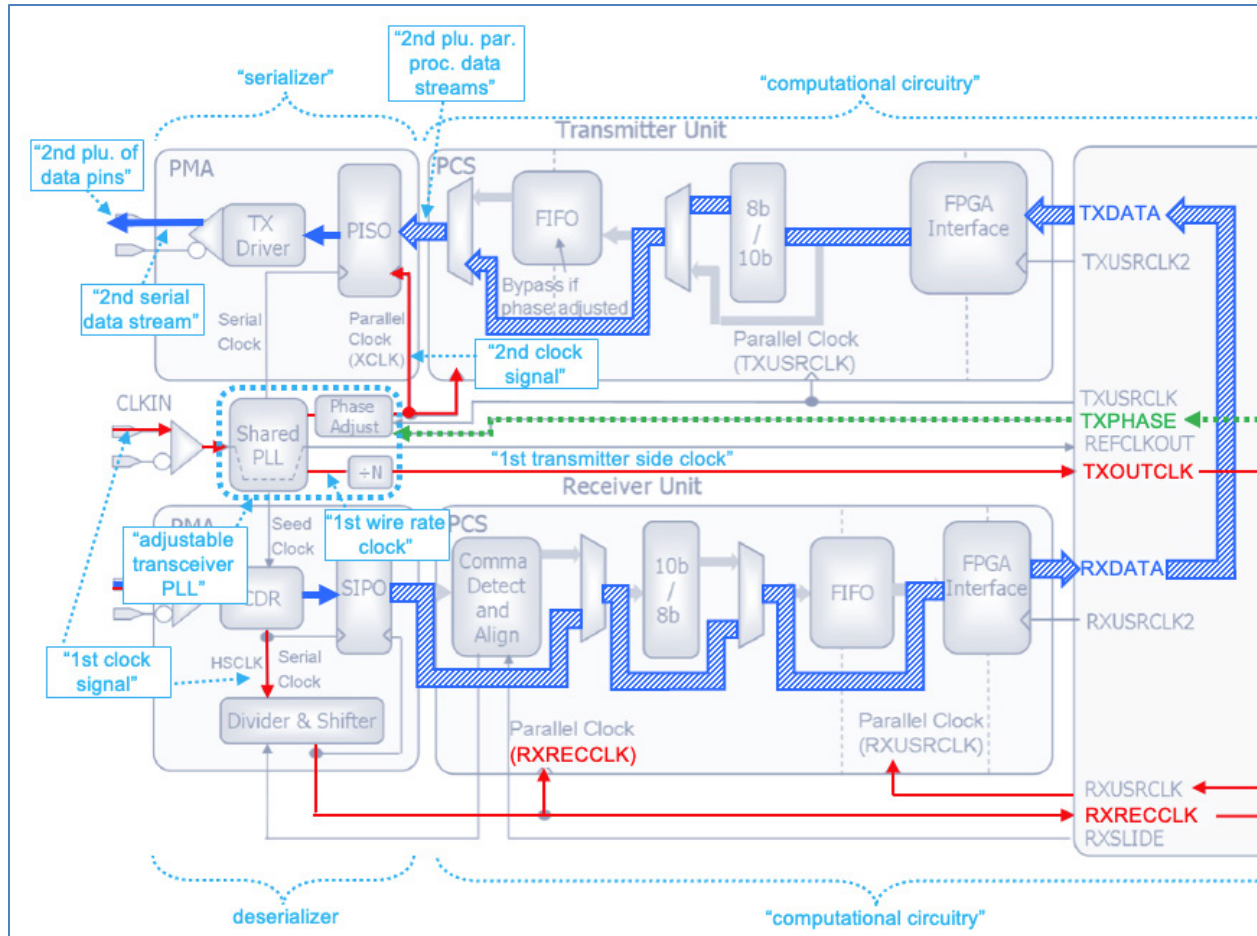
(B) the second plurality of data pins to transmit as a first output the second serial data stream;

(C) the computational circuitry, wherein the serializer receives the second plurality of parallel processed data streams from the computational circuitry and the serializer transmits to the computational circuitry a first transmitter side clock signal including a fifth frequency and a fifth phase; and

Giordano's Transmitter Unit PMA with the Shared PLL (and other related clock components such as phase adjustment circuit and divider) discloses the claimed "serializer." Ex. 1003, ¶166.

The annotated image below, based on Giordano Figure 1, shows relevant portions of the Giordano-Kaviani combination, with a table summarizing relevant mappings:

⁶ Regarding "first wire rate clock signal," element [1.1] requires the "transceiver phase lock loop" be configured to **generate** said "first wire rate clock signal." Ex. 1001, cl. 1. Here, this limitation requires that "transceiver phase lock loop" **receive** the "first wire rate clock signal." Petitioners understand that claim 1 of the '069 requires a "transceiver phase lock loop" which both receives and generates (using different sub-components) the "first wire rate clock signal." Ex. 1003, ¶164, fn. 2.



Claim Limitation	Disclosures
"serializer"	Giordano's Transmitter Unit PMA, Shared PLL, and Divider ("÷N") collectively
"adjustable transceiver PLL"	Giordano's Shared PLL, Phase Adjustment Circuit, and Divider ("÷N") collectively
"first clock signal" (with first frequency and phase)	Giordano's HCLK (both as clock internally generated by Receiver Unit PMA CDR, and provided by neighboring GTP transceiver to CLKIN pin using GTP Dedicated Clock Routing mode)

“second clock signal” (with second frequency and phase)	Giordano’s XCLK
“first receiver side clock signal” (with third frequency and phase)	Giordano’s RXRECCLK
“first wire rate clock signal” (with fourth frequency and phase)	Giordano’s Shared PLL output to Divider (“÷N”)
“first transmitter side clock signal” (with fifth frequency and phase)	Giordano’s TXOUTCLK

As discussed in [1.b] and [1.e], Giordano’s FPGA pins out from the Transmitter Unit PMA discloses the “second plurality of data pins,” with the exiting data disclosing the “second serial data stream,” Receiver Unit PCS, FPGA Fabric, and Transmitter Unit PCS individually and collectively disclose “computational circuitry,” and processed parallel data exiting the Transmitter Unit PCS into the Transmitter Unit PMA discloses the “second plurality of parallel processed data streams.”

For sub-element (A), Giordano’s Shared PLL, phase adjustment circuit, and divider collectively disclose the “adjustable transceiver [PLL],” and an output of the Shared PLL discloses “first wire rate clock signal” (and also “fourth frequency” and “fourth phase”). Ex. 1003, ¶168.

Giordano’s Shared PLL generates clock signals based on incoming signals, including signals provided through the CLKIN port. Ex. 1005, Fig. 1; Ex. 1003, ¶169. One of these output clock signals is provided to a divider (depicted with “÷

N”), where this divider generates TXOUTCLK. Ex. 1005, Fig. 1; Ex. 1003, ¶169. The clock signal going into this divider discloses “first wire rate clock signal.” *Id.*

This mirrors the ’069 patent, which describes a divider for adjusting the frequency of a clock signal. Ex. 1001, 29:8–14, 51:58–52:3. Like Giordano, this divider outputs a “lower-frequency” signal, from dividing the input signal by a user-settable number. Ex. 1001, 52:26–36; Ex. 1003, ¶170.

For sub-element (B). Transmitter Unit PMA in Giordano has a TX Driver that sends out serial data, which discloses sub-element (B). Ex. 1005, 195; Ex. 1003, ¶171. Giordano’s package pins interfacing Transmitter Unit PMA with external components disclose the claimed “second plurality of data pins.” Ex. 1005, Fig. 1; Ex. 1003, ¶171. This Transmitter Unit PMA transmits processed serial data, *i.e.*, “second serial data stream.” Ex. 1005, 195; Ex. 1003, ¶171.

This mirrors the ’069 patent, which describes a Transmitter PMA with a Transmitter Buffer that sends out serial data. Ex. 1001, 53:55–54:8, Fig. 7B.

For sub-element (C). Giordano’s TXOUTCLK discloses “first transmitter side clock signal,” and also the “fifth frequency” and “fifth phase.” Ex. 1003, ¶173.

Giordano discloses PISO block in the Transmitter Unit PMA (of the “serializer”) receiving parallel data (“second plurality of parallel processed data streams”) from the Transmitter Unit PCS (of the “computational circuitry”). Ex. 1005, Fig. 1.

In the proposed combination, the Shared PLL (of the “serializer”) transmits to the FPGA Fabric (of the “computational circuitry”) the TXOUTCLK signal (“first transmitter side clock signal”) through a divider block denoted “÷N.” Ex. 1005, Fig. 1.

[1.g]: wherein the serializer is configured to:

(A) convert the second plurality of parallel processed data streams into the second serial data stream;

(B) generate the first transmitter side clock signal based on the first wire rate signal, wherein the first transmitter side clock signal has the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency; and

(C) transmit the second serial data stream to the second plurality of data pins for transmission off the field programmable gate array; and

As discussed in [1.f], Giordano’s Transmitter Unit PMA with the Shared PLL discloses the claimed “serializer.”

For sub-element (A), as discussed in [1.b] and [1.e], serial data output of PISO discloses the “second serial data stream,” and the parallel data from the Transmitter Unit PCS into the Transmitter Unit PMA discloses “second plurality of parallel processed data streams.”

Giordano’s PISO block converts parallel data (“second plurality of parallel processed data streams”) to serial data (“second serial data stream”). Ex. 1005, 195; Ex. 1003, ¶175.

This mirrors the '069 patent, which describes a serializer with a transmitter PMA with a Parallel to Serial block. Ex. 1001, 53:55–54:8, Fig. 7B. Like Giordano, this Parallel to Serial block converts the incoming parallel data to serial data. *Id.*

For sub-element (B), as discussed in [1.f], Giordano's TXOUTCLK discloses "first transmitter side clock signal," and the output of the Shared PLL going into the divider discloses "first wire rate clock signal."

Giordano discloses a divider (depicted with " $\div N$ ") that generates TXOUTCLK ("first transmitter side clock signal") based on a signal from the Shared PLL ("first wire rate clock signal"). Ex. 1005, Fig. 1; Ex. 1003, ¶177.

This mirrors the '069 patent, which describes a divider for adjusting the frequency of a clock signal. Ex. 1001, 29:8–14, 51:58–52:3. Like Giordano, this divider outputs a "lower-frequency" signal, from dividing the input signal by a user-settable number. Ex. 1001, 52:26–36; Ex. 1003, ¶178.

Giordano discloses using clock dividers of " $\div 5$ " for the receiver clock divider. Ex. 1005, Fig. 3. A POSITA would have known to use the " $\div 5$ " divider, explicitly used for the receiver side, for the " $\div N$ " block on the transmitter side. Ex. 1003, ¶179. This results in Giordano's Shared PLL output ("first wire rate clock" with "fourth frequency") to have a frequency five times that of TXOUTCLK ("first transmitter side clock signal" with "fifth frequency"), disclosing this sub-element (B). *Id.*

For sub-element (C), Transmitter Unit PMA in Giordano has a TX Driver that sends out serial data, which discloses this sub-element. Ex. 1005, 195; Ex. 1003, ¶180. Giordano's package pins interfacing Transmitter Unit PMA with external components disclose the claimed "second plurality of data pins." Ex. 1005, Fig. 1; Ex. 1003, ¶180. This Transmitter Unit PMA transmits processed serial data, *i.e.*, "second serial data stream." Ex. 1005, 195; Ex. 1003, ¶180.

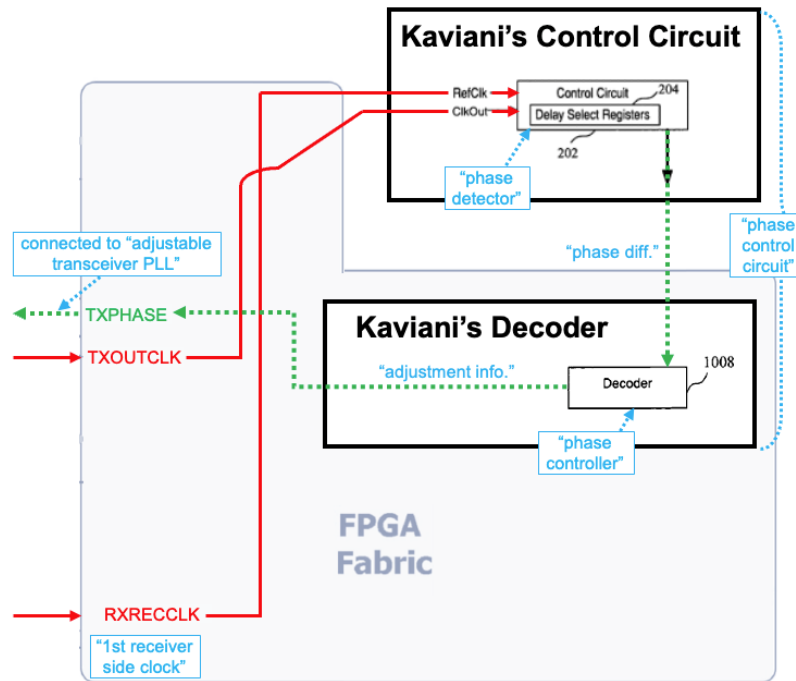
This mirrors the '069 patent, which describes a Transmitter PMA with a Transmitter Buffer that sends out serial data. Ex. 1001, 53:55–54:8, Fig. 7B.

[1.h]: (b) a phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises:

Kaviani discloses this limitation. Ex. 1003, ¶181.

Kaviani's Control Circuit and Decoder together disclose this limitation. Ex. 1010, Figs. 2, 10; Ex. 1003, ¶182.

The image below shows the portions of the Giordano-Kaviani combination relevant to the claimed "phase control circuit," with additional annotations:



Kaviani discloses Control Circuit 202, a component separate from other circuits (such as Kaviani's Decoder 1008 within Clock Generator Circuit 206), hence implementable in different physical regions. Ex. 1010, Fig. 2; Ex. 1003, ¶183. As such, in light of Giordano's teachings, a POSITA would have known to implement the Control Circuit off the FPGA chip but still on the circuit board (*e.g.*, FPGA system), while implementing other elements (such as Kaviani's Decoder 1008) on the FPGA Fabric. Section VI.A.1; Ex. 1003, ¶183.

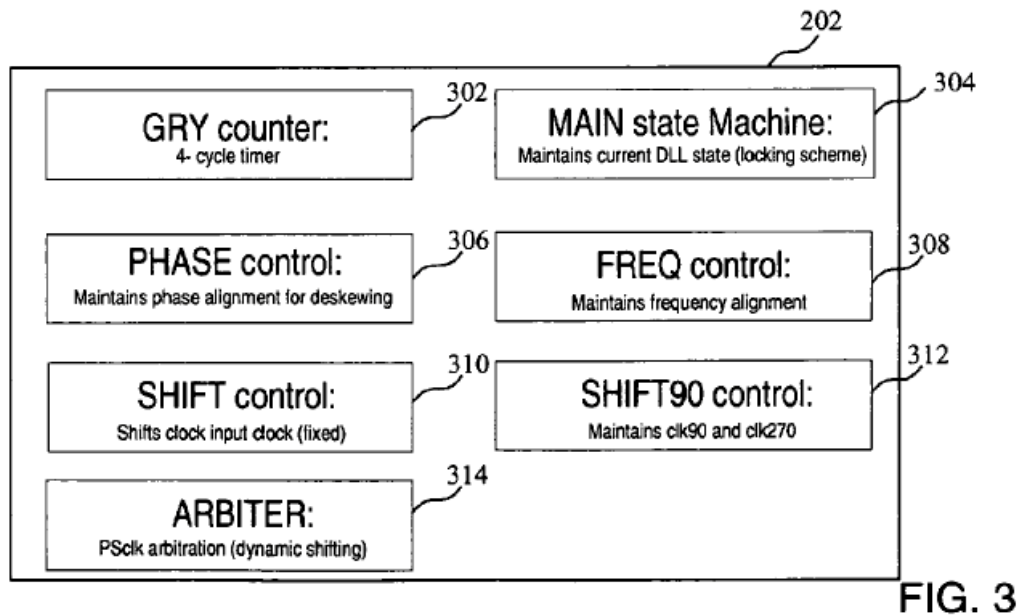
[1.i]: (1) a phase detector configured to compare the third phase of the first receiver side clock signal to the fifth phase of the transmitter side clock signal and to generate a phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the fifth phase of the transmitter side clock signal;

Kaviani discloses this limitation. Ex. 1003, ¶184. As discussed in [1.d], Giordano's parallel recovered clock RXRECCLK discloses the "first receiver side

clock signal” (with “third phase”) and TXOUTCLK discloses the “first transmitter side clock signal” (with “fifth phase”).⁷

Kaviani’s Control Circuit discloses the “phase detector.” Ex. 1003, ¶185.

Kaviani discloses the Control Circuit 202 generating shift delay vectors (*e.g.*, sdlysel, pdlhysel, fdlysel) and delay select input vectors (*e.g.*, Input Phase Shift Signal, Sel00[2:0]). Ex. 1010, 3:64–4:28. The various functions of Control Circuit 202 are further described in Kaviani Figure 3:



Kaviani’s PHASE control 306 generates signals “for maintaining phase alignment for deskewing,” and FREQ control 308 “for maintaining frequency

⁷ The term “transmitter side clock signal” lacks antecedent basis. For the purpose of this IPR, Petitioners will correlate this term with the “first transmitter side clock signal” discussed in element [1.f].

alignment.” *Id.*, 5:37–51. Kaviani discloses generating such control signals based on comparison of the two incoming clock signals, which in the proposed combination are RXRECCLK (“receiver side clock signal”) and TXOUTCLK (“transmitter side clock signal”). Ex. 1003, ¶188.

[1.j]: (2) a phase controller operationally connected to the phase detector and configured to receive the phase difference indicator signal, and wherein the phase controller is configured to determine adjustment information based on the phase difference indicator signal; and

Giordano in view of Kaviani renders obvious this limitation. Ex. 1003, ¶189. As discussed in [1.i], Kaviani’s Control Circuit 202 discloses the claimed “phase detector” and its output discloses “phase difference indicator signal.”

The Decoder 1008 in Kaviani’s Digital Delay Line, which is implemented on Giordano’s FPGA Fabric, discloses the claimed “phase controller,” which takes in the output from the Control Circuit 202 (“phase detector”) hence “operationally connected” to the phase detector. Ex. 1010, Figs. 2, 10; Ex. 1003, ¶190.

Kaviani discloses Control Circuit 202 generating shift delay vectors (*e.g.*, sdlysel, pdlysel, fdlysel), which are then used for controlling the phase of the target output clock. Ex. 1010, 3:64–4:28. Kaviani discloses that the Decoder 1008 receives these delay vectors. *Id.*, Fig. 10. The output of the Decoder, which becomes TXPHASE of Giordano, discloses “adjustment information.” Ex. 1005, Fig. 1; Ex. 1003, ¶191.

Indeed, Giordano also discloses using Phase Align Control circuitry to control the TXPHASE signal transmitted to the GTP transceiver. Ex. 1005, Fig. 5; Ex. 1003, ¶192. It would have been obvious to a POSITA to use the output of the decoder, with Giordano's Phase Align Control circuit, to control the TXPHASE signal. *Id.*

[1.k]: (3) the adjustable transceiver phase lock loop operationally connected to the phase controller and configured to receive the adjustment information as well as operationally connected to the second reference clock pin of the first interface of the field programmable gate array,

Giordano in view of Kaviani renders obvious this limitation. Ex. 1003, ¶193. As discussed in [1.b], [1.f], and [1.j], Kaviani's Decoder 1008 discloses the claimed "phase controller," Giordano's FPGA pin for CLKIN discloses the "second reference clock pin of the first interface," and Giordano's Shared PLL, phase adjustment circuit, and divider together disclose the "adjustable transceiver [PLL]."

In the proposed combination, as seen in the image above in [1.h], the Decoder 1008 ("phase controller") output becomes Giordano's TXPHASE ("adjustment information"), which is connected back to the phase adjustment circuit (which is part of the "adjustable transceiver [PLL]"). Giordano discloses that "a controller in the [FPGA Fabric] activates the phase align circuit by means of the TXPHASE signal." Ex. 1005, 197. Giordano's Shared PLL (also part of the "adjustable transceiver [PLL]") is connected to the CLKIN pin ("second reference clock pin").

[1.i] wherein the adjustable transceiver phase lock loop is configured to generate a second clock signal including the second frequency and the second phase based on the first clock signal received via the second reference clock pin and process the second clock signal based on the adjustment information received from the phase controller to generate the first wire rate clock signal,

Giordano discloses this limitation. Ex. 1003, ¶195. As discussed in [1.j], TXPHASE discloses the “adjustment information,” and as discussed in [1.b], Giordano’s FPGA pin for CLKIN discloses the “second reference clock pin” and CLKIN signal (which in the proposed combination is same as HSCLK) discloses the “first clock signal.”

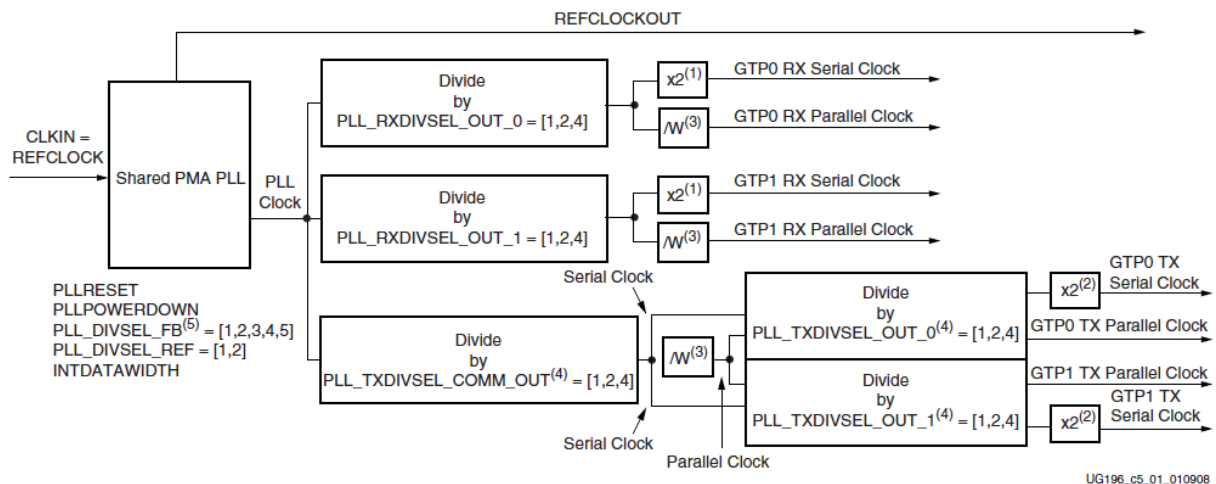
For “generate a second clock signal ... based on the first clock signal,”

Giordano’s Shared PLL and Phase Adjustment Circuit collectively generate an XCLK signal for the Transmitter Unit PMA, where XCLK discloses the claimed “second clock signal,” and the second frequency and phase. Ex. 1005, 195, 197; Ex. 1003, ¶196.

Giordano discloses that the Shared PLL generates a clock based on the CLKIN signal. Ex. 1005, 196; Ex. 1003, ¶197. The parallel clock for the PISO block, XCLK, is generated by multiplication and division (from within the Shared PLL) of the incoming CLKIN signal. Ex. 1005, 197; Ex. 1003, ¶197.

Virtex-UG further discloses this limitation. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses this limitation. Ex. 1003, ¶198.

Virtex-UG discloses that the Shared PLL generates “a high-speed serial clock from a high-quality reference clock (CLKIN).” Ex. 1009, 72; Ex. 1003, ¶199. Virtex-UG discloses components (including dividers and multipliers) involved with converting the reference clock (CLKIN, *i.e.*, “first clock signal”) to clocks (such as XCLK), as seen in Virtex-UG Figure 5-1:



Ex. 1003, ¶199.

For “process the second clock signal based on the adjustment information,” Giordano discloses processing XCLK (“second clock”) to align with other clocks by “a controller in the fabric” that “activates the phase align circuit by means of the TXPHASE signal.” Ex. 1005, 197; Ex. 1003, ¶200. As seen in Giordano Figure 1 (and the annotated version seen in element [1.f]), the TXPHASE signal (“adjustment information”) is sent from the FPGA Fabric to the Phase Adjustment circuit (part of “adjustable transceiver PLL”), to activate said Phase Adjustment circuit to phase align XCLK with TXUSRCLK.

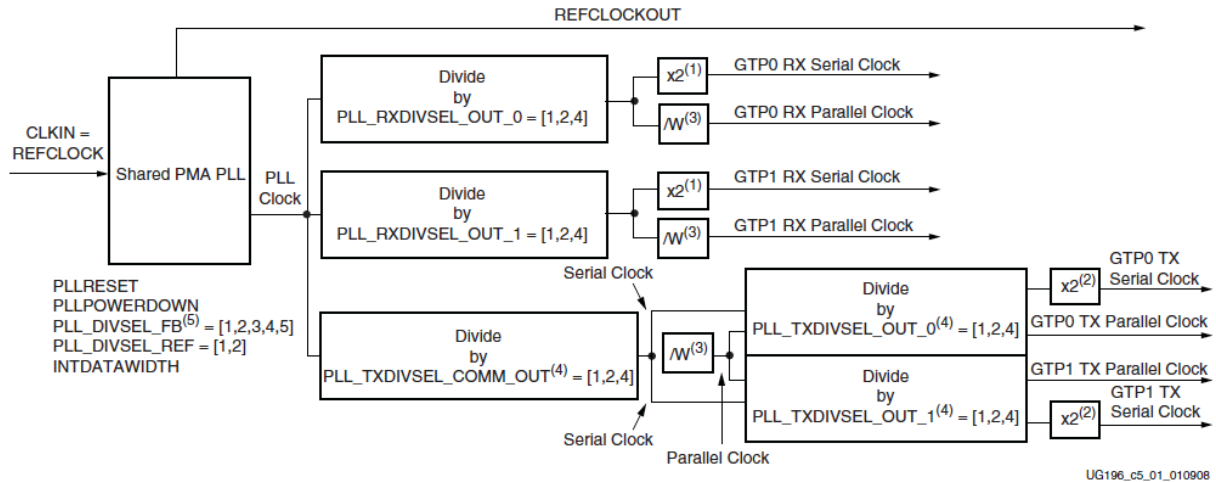
Virtex-UG further discloses this limitation. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses this limitation. Ex. 1003, ¶201.

Virtex-UG discloses that “[w]hen activated, TXPMASETPHASE aligns XCLK with TXUSRCLK.” Ex. 1009, 117; Ex. 1003, ¶202. A POSITA would have understood this TXPMASETPHASE is the same as TXPHASE in Giordano’s simplified figures and explanations. *Id.*

For “to generate the first wire rate clock signal,” Giordano discloses the Shared PLL generating the input (“first wire rate clock signal”) which is input into the divider block “÷N” (as shown in the annotated figure in [1.f]) which outputs TXOUTCLK. Ex. 1005, 195; Ex. 1003, ¶203.

Virtex-UG further discloses this limitation. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses this limitation. Ex. 1003, ¶204.

Virtex-UG discloses that the Shared PLL generates “a high-speed serial clock from a high-quality reference clock (CLKIN).” Ex. 1009, 72; Ex. 1003, ¶205. Virtex-UG discloses components (including dividers and multipliers) involved with converting the reference clock (CLKIN, *i.e.*, “first clock signal”) to various clocks to be supplied in the receiver and transmitter, as seen in Virtex-UG Figure 5-1:



Ex. 1003, ¶205.

[1.m]: wherein the transmitter side clock signal and the first receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the fifth phase.

Giordano in view of Kaviani renders obvious this limitation. Ex. 1003, ¶206.

As discussed in [1.d] and [1.f], Giordano’s parallel recovered clock (RXRECCLK) discloses the “first receiver side clock signal” (with “third phase”) and TXOUTCLK discloses “first transmitter side clock signal” (with “fifth phase”).

Giordano discloses that, based on measurements and test results, “the transmission latency and the phase of the recovered clock *remained always the same*,” where the signal latencies (hence phase) were measured “with respect to the reference clock at the transmitter.” Ex. 1005, 199. In Giordano’s architecture, the recovered clock (“RXRECCLK”) and the transmit-side reference clock (from which TXOUTCLK is derived) have a fixed phase difference of approximately 400

picoseconds, hence disclosing the two clocks having a fixed phase difference. *Id.*; Ex. 1003, ¶207.

In the proposed combination, Kaviani discloses Control Circuit 202 sending control signals based on the measured phase difference between RXRECCLK (with “third phase”) and TXOUTCLK (with “fifth phase”) to Decoder 1008, which then generates the TXPHASE signal. Ex. 1003, ¶208. As discussed in [1.1], this TXPHASE is used to phase match clock signals.

In addition, Kaviani discloses that based on the measured phase difference between RXRECCLK (with “third phase”) and TXOUTCLK (with “fifth phase”), Control Circuit determines the “correct amount of shifting required by all the delay lines” so the clock output is phase-matched to the reference clock signal. Ex. 1010, 5:24–35. Kaviani refers to this determination as “locking process.” *Id.* The Control Circuit also maintains the correct shifting after lock, maintaining the phase-matching between the two clock signals. *Id.*, 5:35–37; Ex. 1003, ¶209.

Kaviani Figure 4 discloses this iterative process for “locking” the output clock to the reference clock:

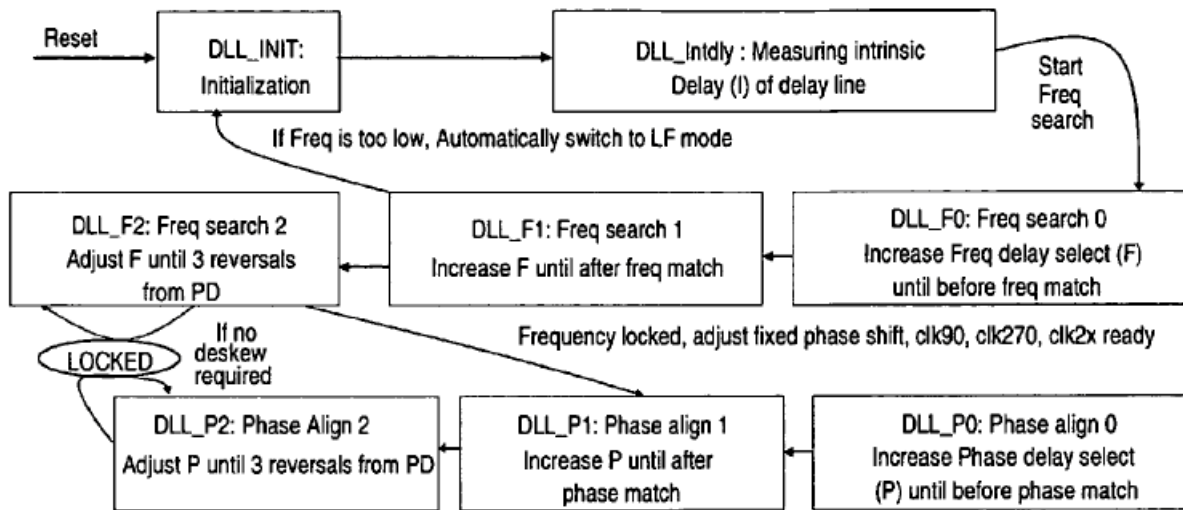


FIG. 4

b. Claims 2–4

Claims 2–4 concern the relationship between “first clock signal” (with “first frequency” and “first phase”) and “first receiver side clock signal” (with “third frequency” and “third phase”). Giordano in view of Kaviani renders obvious these claims. Ex. 1003, ¶211.

As discussed in [1.b] and [1.d], HSCLK discloses the “first clock signal” and RXRECCLK discloses the “first receiver side clock signal.”

[2]: The system of claim 1, wherein the third frequency corresponds to the first frequency.

[3]: The system of claim 2, wherein the third phase is not aligned with the first phase.

[4]: The system of claim 1, wherein the third frequency is different than the first frequency.

Giordano discloses claims 2–4. Ex. 1003, ¶213.

Giordano discloses that in the Receiver Unit PMA, “HSCLK is divided down by 5 and then fed in a 5-bit shift-register,” which then becomes RXRECCLK. Ex. 1005, 196, Fig. 3. Using signal RXSLIDE from the FPGA Fabric, this 5-bit shift-register selects the phase shift of RXRECCLK with respect to HSCLK. *Id.*; Ex. 1003, ¶214. As such, RXRECCLK, in this implementation, has a frequency that is 20% (one-fifth) of that of HSCLK, and shifted in phase (by the 5-bit shift-register) to HSCLK. *Id.* This discloses claims 3 and 4.

Since RXRECCLK has a frequency that is one-fifth of that of HSCLK, the two clock frequencies “correspond” with each other, disclosing claim 2. Ex. 1003, ¶215.

Virtex-UG further discloses claim 2. If “correspond” requires the two frequencies to be identical, Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 2. Ex. 1003, ¶216. As discussed in [1.b] and [1.d], HSCLK discloses the “first clock signal” and RXRECCLK discloses the “first receiver side clock signal.”

Virtex-UG discloses configuration signals PLL_RXDIVSEL_OUT and PLL_DIVSEL_REF. Ex. 1009, 72. These are exemplary user configuration signals for the Xilinx Virtex-5 GTP Transceivers that control dividers that relate to RXRECCLK. Ex. 1003, ¶217. PLL_RXDIVSEL_OUT, which can be set to 1, 2, or 4, is used to divide the incoming clock signal to produce a receiver side clock.

Ex. 1009, 73; Ex. 1003, ¶217. Virtex-UG discloses that setting PLL_RXDIVSEL_OUT to 1 results in a clock division of one, hence the same frequency. Ex. 1009, 77 (providing example where incoming clock at 1.5625 GHz with “the external divider (PLL_RXDIVSEL_OUT)” set to 1 results in same clock rate of 1.5625 GHz); Ex. 1003, ¶217. Likewise, PLL_DIVSEL_REF “[c]ontrols the reference clock divider” (hence impacts RXRECCLK) and can be set to 1 or 2. Ex. 1009, 73; Ex. 1003, ¶217.

Virtex-UG’s disclosures of clock dividers that divide by one discloses this claim. As discussed in claim 3, Giordano discloses that in the Receiver Unit PMA, “HSCLK is divided down by 5” by a clock divider (denoted as “÷ 5”), which then outputs RXRECCLK. Ex. 1005, 196, Fig. 3. As such, RXRECCLK, in this implementation, has a frequency that is 20% (one-fifth) of that of HSCLK.

It would have been obvious to a POSITA to modify the “÷ 5” block in Giordano to incorporate the clock dividers of Virtex-UG, namely those that can be set to 1. Ex. 1003, ¶219. With such clock divider, RXRECCLK would have the same frequency as HSCLK, disclosing claim 2. *Id.*

c. Claim 5

[5]: The system of claim 1, wherein the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

Giordano discloses this claim. Ex. 1003, ¶220.

Giordano discloses bypassing First In First Out (FIFO) buffer, a circuit block allowing safe data transfer between different clock domains (*e.g.*, “data transfers between TXUSRCLK domain and the XCLK domain”). Ex. 1005, 195; Ex. 1003, ¶221. A POSITA would have understood FIFO as executing clock domain crossing operations, and Giordano’s bypassing of the FIFO block discloses this claim. Ex. 1003, ¶221.

Giordano discloses bypassing FIFO buffer by having the two clock domains have “the same phase” and “therefore also the same latency for the data.” Ex. 1005, 195; Ex. 1003, ¶222. In the transmitter, Giordano discusses two clocks (XCLK and TXUSRCLK) that are adjusted to have the same frequency and phase. Ex. 1005, 195. The transmitter has a FIFO block for crossing between XCLK and TXUSRCLK clock domains. *Id.*; Ex. 1003, ¶222. Giordano discloses bypassing this FIFO block by using a phase alignment option provided in Xilinx Virtex-5 FPGA systems. Ex. 1005, 195; Ex. 1003, ¶222. Through this built-in phase alignment, XCLK and TXUSRCLK are phase aligned, in which “the transmit FIFO is unnecessary and therefore we bypassed it.” Ex. 1005, 197.

Virtex-UG further discloses this claim. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses this claim. Ex. 1003, ¶223.

In the receiver, Virtex-UG confirms this FIFO bypass. When receiver clock phase alignment is used, “RXUSRCLK must be driven directly from RXRECCLK using a BUFR regional clock buffer.” Ex. 1009, 179 (“Using RX Phase Alignment to Bypass the RX Elastic Buffer”). Due to phase alignment, “SIPO parallel clock phase matches RXUSRCLK phase” and there is “no phase difference between XCLK and RXUSRCLK.” *Id.*, 180. With no phase difference, the RX Elastic Buffer (which is the FIFO block described in Giordano) is bypassed. This bypass is described in the red arrow below in Figure 7-22 of Virtex-UG:

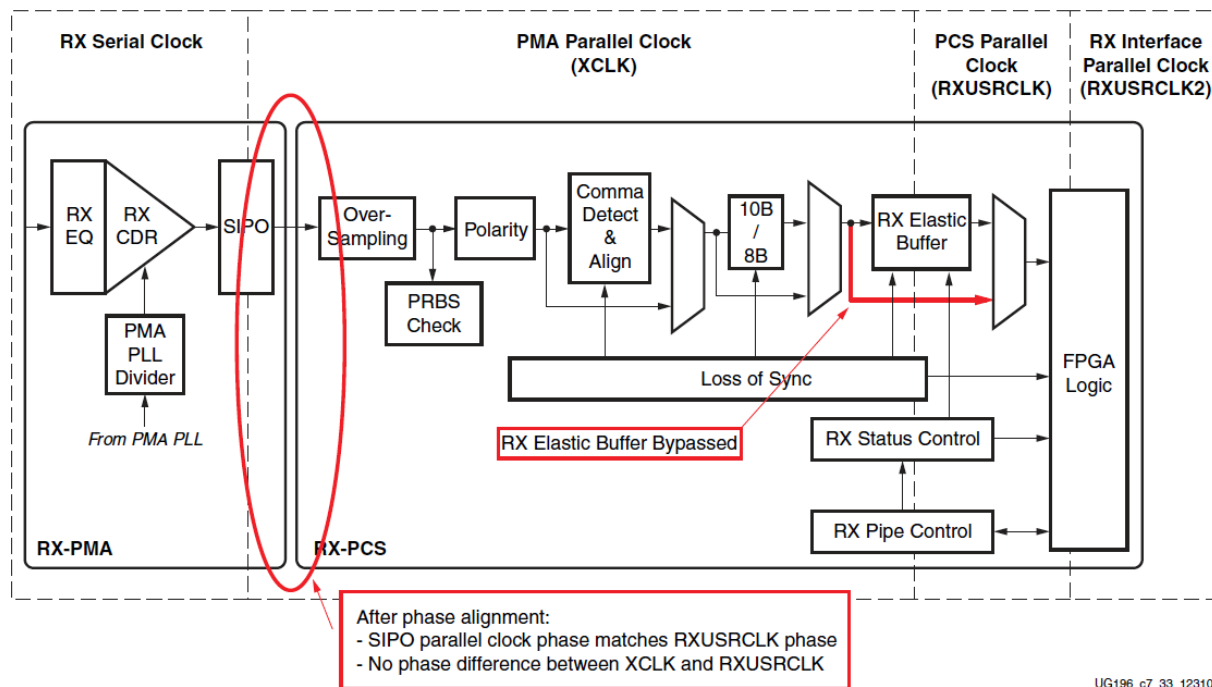


Figure 7-22: Using Phase Alignment

The bypass of all clock domain crossing circuits after phase alignment of clock signals, as disclosed in Giordano, discloses this claim. Ex. 1003, ¶225.

d. Claim 6

[6]: The system of claim 1, wherein the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

Giordano discloses this claim. Ex. 1003, ¶226. As discussed in element [1.e], Giordano’s disclosures on the PCS layer processing and the FPGA Fabric “logic” discloses the claimed “first set of operations.”

The operations on PCS layers and FPGA Fabric each discloses this claim.

Giordano’s Comma Detector and Aligner implemented in the FPGA Fabric performs pattern matching (detecting comma characters in the raw 10-bit data), comparison (determining the number of bit shifts required), and conditional branching (the even/odd decision logic that either applies RXSLIDE assertions or resets the CDR). Ex. 1005, 198. These are examples of logical operations, which disclose this claim. Ex. 1003, ¶228.

In addition, Giordano points to the PCS layer (both receiver and transmitter sides) as “processing” data, disclosing the “computational circuitry.” Ex. 1005, 194; Ex. 1003, ¶229. The PCS layer includes optional 8b/10b encoding / decoding functions, which requires arithmetic calculations hence disclosing this claim. Ex. 1005, 197; Ex. 1003, ¶229.

e. Claim 7

[7]: The system of claim 1, wherein the first amount of data streams is the same as the second amount of data streams.

Giordano's use of the optional 8b/10b encoding and decoding feature discloses this claim. Ex. 1003, ¶230.

Giordano discloses the SIPO deserializing incoming serial data stream into 10-bit parallel words, which may then be decoded into 8-bit parallel words using 8b/10b decoding (and if not, kept at 10-bit). Ex. 1005, 195. On the transmit side, the FPGA fabric provides either 8-bit words for re-encoding into 10-bit words or, if 8b/10b encoding is not used, 10-bit words directly to the PISO block. Ex. 1005, 195, 197. A POSITA would have found it obvious to have what is identified as first amount of data streams to be identical to second amount of data streams, either 8-bits or 10-bits. Ex. 1003, ¶231.

f. Claim 8

[8]: The system of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

Giordano discloses this claim. Ex. 1003, ¶232. As discussed in claim 7, Giordano discloses internal parallel data width to be same on both receiver and transmitter sides.

Giordano's use of 8-bit parallel words (eight data streams) and 10-bit parallel words (ten data streams) disclose this claim. Ex. 1005, 195; Ex. 1003, ¶233.

g. Claim 9

[9]: The system of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

Giordano discloses this claim. Ex. 1003, ¶234.

Giordano's disclosure of 8-bit parallel words (eight data streams), which is two to the power of three, discloses this claim. Ex. 1005, 195; Ex. 1003, ¶235.

h. Claim 10

[10]: The system of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

Giordano discloses this claim. Ex. 1003, ¶236.

Giordano's disclosure of 10-bit parallel words (ten data streams), which is ten times two to the power of zero, discloses this claim. Ex. 1005, 195; Ex. 1003, ¶236.

i. Claim 11

[11]: The system of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.

Giordano discloses this claim. Ex. 1003, ¶237.

Virtex-UG further discloses claim 11. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 11. Ex. 1003, ¶238. As discussed in elements [1.d] and [1.e], Giordano's SIPO block output,

further processed by the Receiver Unit PCS, discloses the “first amount of data streams,” and processed parallel data going through the Transmitter Unit PCS and PMA disclose the “second amount of data streams.”

Virtex-UG discloses that the Virtex-5 FPGA GTP Transceiver supports 64b/66b encoding, in addition to the optional 8b/10b encoding demonstrated by Giordano (using the same Virtex-5 FPGA GTP Transceiver). Ex. 1009, 283, 286, 290; Ex. 1005, 194 (“The architecture we present in this paper is based on the GTP transceiver of the Xilinx Virtex 5 FPGA family”); Ex. 1003, ¶239. By using the 64b/66b encoding standard, it would have been obvious to modify the GTP transceiver of the proposed combination to support 66-bit data words. *Id.* This discloses first and second amount of data streams at 66 bits. *Id.* Since 66 is thirty-three times two to the power of one, Virtex-UG discloses this claim.

j. Claim 12

[12]: The system of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.

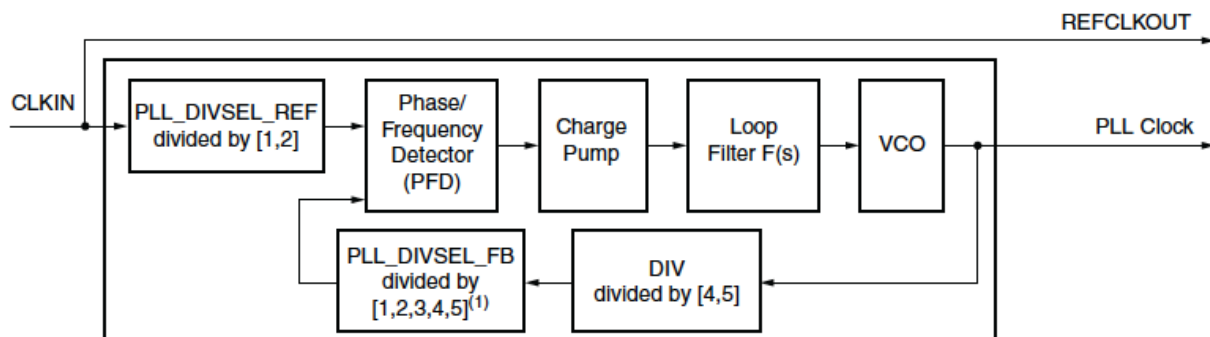
Giordano discloses this claim. Ex. 1003, ¶240. As discussed in [1.f], Giordano’s Shared PLL output into divider “÷ N” discloses “first wire rate clock signal” (and the “fourth frequency”), and TXOUTCLK discloses “first transmitter side clock signal” (and the “fifth frequency”). As discussed in claim 7, Giordano discloses 8-bit and 10-bit words, which disclose the “second amount of data streams.”

Giordano's disclosure of 10-bit words as the claimed "second amount" means that the claimed "second amount of data streams" is equal to ten. Ex. 1003, ¶241. This, with Giordano's use of clock dividers, discloses this claim.

Giordano discloses that the output of the Shared PLL ("first wire rate clock") is connected to a divider block denoted " $\div N$," which in turn outputs TXOUTCLK. A POSITA would have understood N to be an integer, including ten. Ex. 1003, ¶242. This results in Giordano's Shared PLL output ("first wire rate clock") having a frequency ten times that of TXOUTCLK ("first transmitter side clock signal"), disclosing this claim. *Id.*

Virtex-UG further discloses claim 12. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 12. Ex. 1003, ¶243.

Virtex-UG discloses two divider blocks DIV and PLL_DIVSEL_FB, when put together, could divide signals by eight or ten. Per Figure 5-2 of Virtex-UG, an exemplary cascade of dividers is shown:



The clock path that includes the PLL_DIVSEL_FB block and the DIV block results in various combinations of frequency divisions. Ex. 1003, ¶246. For example, PLL_DIVSEL_FB dividing by 2 and DIV dividing by 5 results in overall division of ten. *Id.* PLL_DIVSEL_FB dividing by 2 and DIV dividing by 4 results in overall division of eight. *Id.*

Applying this to the proposed combination, a POSITA would have known to implement Virtex-UG's cascaded dividers into Giordano's divider block " $\div N$." Ex. 1003, ¶247. Using the cascade to have total division of ten results in Giordano's Shared PLL output ("first wire rate clock") having a frequency ten times that of TXOUTCLK ("first transmitter side clock signal"), disclosing this claim. *Id.*

k. Claim 13

[13]: The system of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.

Giordano discloses this claim. Ex. 1003, ¶248. As discussed in [1.f], Giordano's Shared PLL output into divider " $\div N$ " discloses "first wire rate clock signal" (and the "fourth frequency"), and TXOUTCLK discloses "first transmitter side clock signal" (and the "fifth frequency"). As discussed in claim 7, Giordano discloses 8-bit and 10-bit words, which disclose the "second amount of data streams."

Giordano's disclosure of 10-bit words as the claimed "second amount" means that the claimed "half of the second amount of data streams" is equal to five. Ex. 1003, ¶249. This, with Giordano's use of clock dividers, discloses this claim.

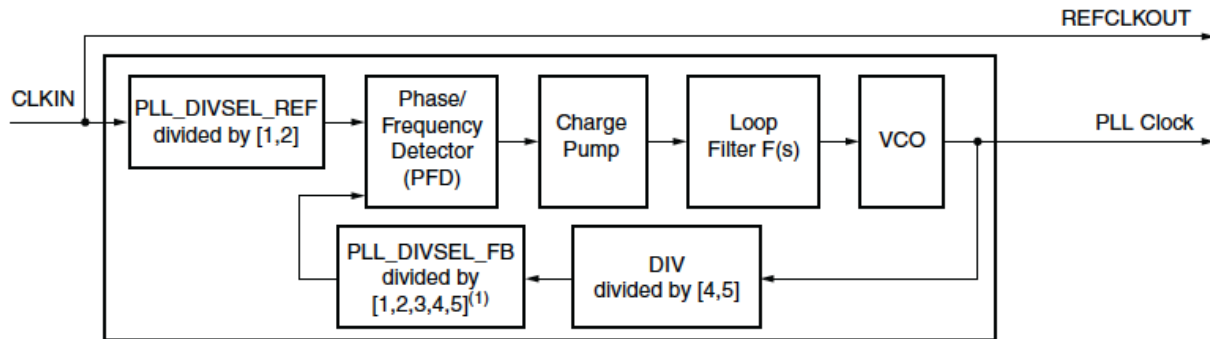
Giordano discloses using clock dividers of " $\div 5$ " for the receiver clock divider. Ex. 1005, Fig. 3. On the transmitter side, the output of the Shared PLL ("first wire rate clock") is connected to a divider block denoted " $\div N$," which in turn outputs TXOUTCLK. A POSITA would have known to use the " $\div 5$ " divider, explicitly used for the receiver side, for the " $\div N$ " block on the transmitter side. Ex. 1003, ¶250. This results in Giordano's Shared PLL output ("first wire rate clock") having a frequency five times that of TXOUTCLK ("first transmitter side clock signal"), disclosing this claim. *Id.*

Virtex-UG further discloses claim 13. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 13. Ex. 1003, ¶251. As discussed in claim 12, Virtex-UG discloses cascading dividers that support a multitude of clock frequency division options.

Giordano's disclosure of 10-bit words as the claimed "second amount" means that the claimed "second amount of data streams" is equal to ten. Ex. 1003, ¶252. This, with Giordano's use of clock dividers, discloses this claim.

Giordano discloses that the output of the Shared PLL ("first wire rate clock") is connected to a divider block denoted " $\div N$," which in turn outputs TXOUTCLK.

Virtex-UG discloses two divider blocks DIV and PLL_DIVSEL_FB, that when put together, could divide signals by four or five. Per Figure 5-2 of Virtex-UG, an exemplary cascade of dividers is shown:



The clock path that includes the PLL_DIVSEL_FB block and the DIV block results in various combinations of frequency divisions. Ex. 1003, ¶254. For example, PLL_DIVSEL_FB dividing by 1 and DIV dividing by 5 results in overall division of five. *Id.* PLL_DIVSEL_FB dividing by 1 and DIV dividing by 4 results in overall division of four. *Id.*

Applying this to the proposed combination, a POSITA would have known to implement Virtex-UG's cascaded dividers into Giordano's divider block "÷N." Ex. 1003, ¶255. Using the cascade to have total division of five results in Giordano's Shared PLL output ("first wire rate clock") having a frequency five times that of TXOUTCLK ("first transmitter side clock signal"), disclosing this claim. *Id.*

I. Claim 14

[14]: The system of claim 1, wherein the fourth frequency is a rational multiple of the second frequency.

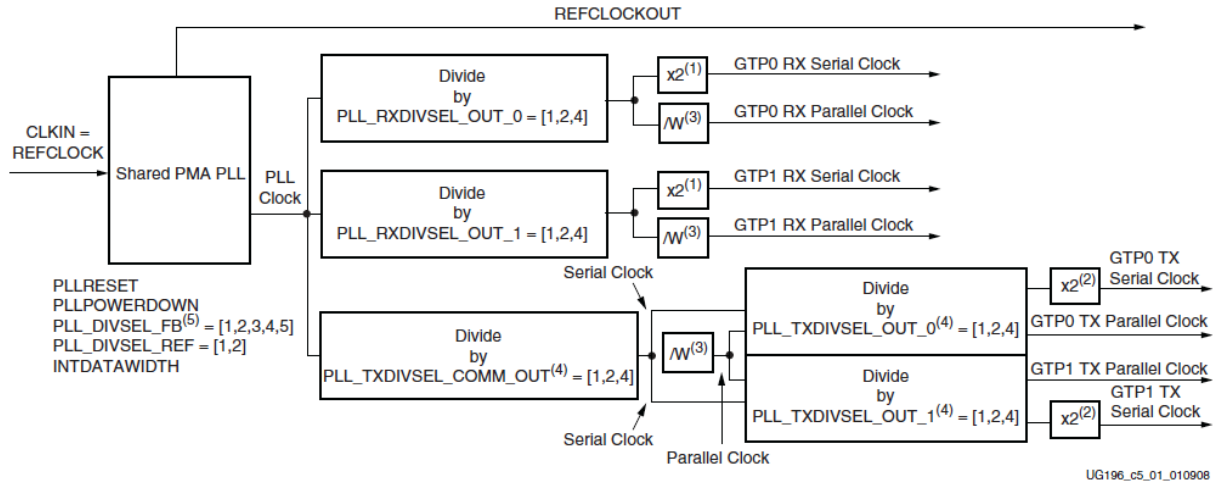
Giordano discloses this claim. Ex. 1003, ¶256. As explained in [1.f] and [1.l], Giordano's XCLK discloses the "second clock signal" (and the "second frequency"), and Giordano's Shared PLL output into divider " $\div N$ " discloses "first wire rate clock signal" (and the "fourth frequency").

Giordano discloses that the "shared PLL locks to a reference clock (CLKIN) and generates" the clock signal ("fourth frequency") and XCLK ("second frequency"). *Id.*, 194–195; Ex. 1003, ¶257. Giordano discloses both of these clocks are generated by the Shared PLL using a common reference signal (CLKIN) that is further modified by dividers and other clock elements. Ex. 1005, Fig. 1; Ex. 1003, ¶257. A POSITA would have known that this discloses a fourth frequency that is a rational multiple of a second frequency. *Id.*

Virtex-UG further discloses claim 14. Virtex-UG, which Giordano inherently discloses and incorporates by reference, discloses claim 14. Ex. 1003, ¶258.

Virtex-UG discloses that the Shared PLL generates "a high-speed serial clock from a high-quality reference clock (CLKIN)." Ex. 1009, 72; Ex. 1003, ¶259. Virtex-UG discloses components (including dividers and multipliers) involved with

converting the reference clock (CLKIN, *i.e.*, “first clock signal”) to multiple clock signals, as seen in Virtex-UG Figure 5-1:



Ex. 1003, ¶260. Virtex-UG discloses multiple dividers in cascade and parallel routes, each with different configurable divider values (such as dividing by 1, 2, or 4). Ex. 1009, Fig. 5-1; Ex. 1003, ¶260. These various options of divisions each disclose this claim. *Id.*

m. Claim 15

[15]: The system of claim 1, wherein the phase difference indicator signal is a pulse signal.

Kaviani discloses this claim. Ex. 1003, ¶261.

As explained in [1.i], Kaviani discloses the Control Circuit 202, which generates shift delay vectors (“phase difference indicator signal”). Kaviani further discloses that, in one embodiment, shift delay vectors may be pulse signals. Ex. 1010, 9:46–10:28.

Kaviani discloses a phase in window function. Kaviani discloses a “phase_inwindow” signal used for this phase-matching function, which takes a form of a pulse signal. Ex. 1010, 6:15–54, Figs. 5–6. Phase_inwindow discloses this claim. Ex. 1003, ¶262. Kaviani further discloses various pulse signals used for phase matching, which discloses this claim. Ex. 1010, 11:33–58, Fig. 13; Ex. 1003, ¶262.

n. Claim 16

[16]: The system of claim 1, wherein adjustment information indicates at least one of the following: (A) a desired phase; (B) a desired frequency; (C) a change in phase; and (D) a change in frequency.

Kaviani discloses claim 16. Ex. 1003, ¶263. Kaviani’s control signals such as vector signal dlysel[15:0] includes at least an indication of a desired phase and change in phase, disclosing this claim. *Id.*, 9:46–10:28; Ex. 1003, ¶263.

o. Claim 17

[17]: The system of claim 16, wherein adjustment information comprises a voltage.

Kaviani discloses claim 17. Ex. 1003, ¶264. The decoder 1008 takes in a vector signal dlysel[15:0] to control the output clock, which per Figures 5, 6, and 13 are shown as voltage signals. A POSITA would have understood the output of the decoder to also be in voltage. Ex. 1003, ¶264. Indeed, all control signals (which are described in Figures 5, 6, and 13) take form of voltage signals. Ex. 1003, ¶264.

p. Claim 18

[18]: The system of claim 17, wherein adjustment information comprises a digital transmission.

Kaviani discloses claim 18. Ex. 1003, ¶265. The control signal is a voltage signal, which is an output from a decoder that takes in vector signal dlysel[15:0]. A POSITA would have understood the output of the decoder to disclose digital transmission. Ex. 1003, ¶265.

q. Claim 19

[19]: The system of claim 1, wherein the adjustment information is used to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay.

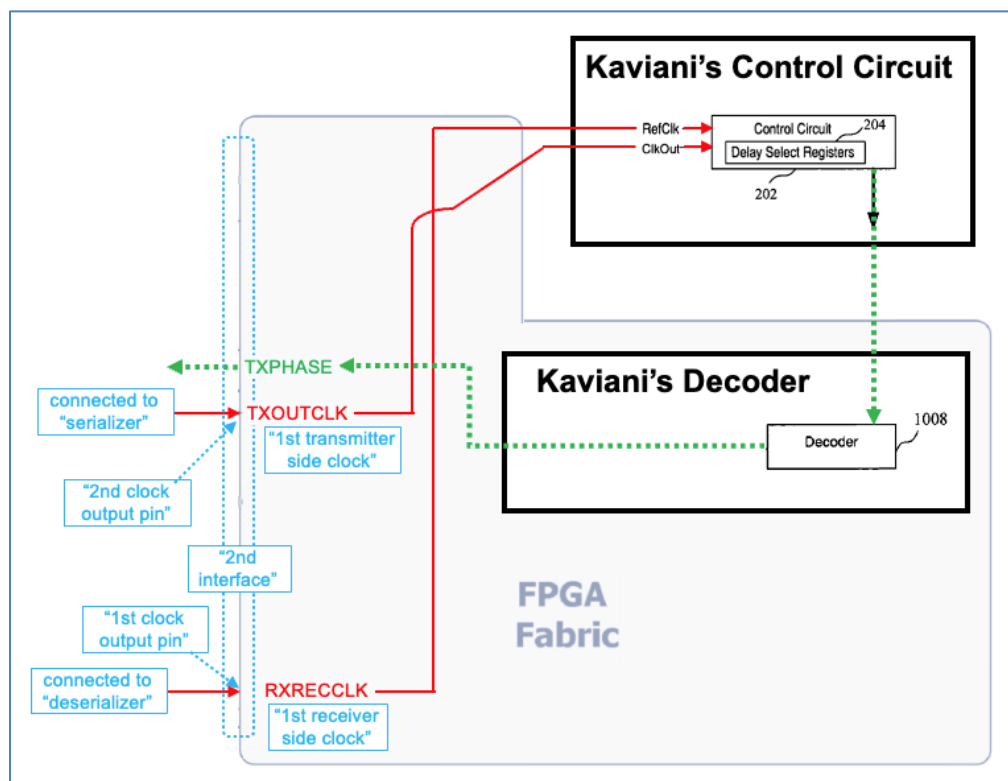
Kaviani discloses this claim. Ex. 1003, ¶266. Kaviani's control signals such as vector signal dlysel[15:0] includes at least an indication of a desired phase and change in phase, which results in "a fine grain delay adjustment to the combined clock signal" by controlled components. *Id.*, 9:46–10:28; Ex. 1003, ¶266. This discloses at least setting a delay, which discloses this claim. *Id.*

r. Claim 22

[22.a]: The system of claim 1, wherein the field programmable gate array further comprises: (5) a second interface comprising:

(A) a first clock output pin configured to transmit the first receiver side clock signal, wherein the first clock output pin is operationally connected to the deserializer; and

(B) a second clock output pin configured to transmit the first transmitter side clock signal, wherein the second clock output pin is operationally connected to the serializer; and



The combination of Giordano and Kaviani discloses this limitation. Ex. 1003, ¶268. As depicted above, in the combination of Giordano and Kaviani, RXRECCLK (“the first receiver side clock signal”) and TXOUTCLK (“the first transmitter side clock signal”) of Giordano are from the GTP transceiver to the FPGA Fabric. This

FPGA interface between the GTP transceiver and the FPGA Fabric discloses the “second interface.”

The clock signal pin for RXRECCLK (“first receiver side clock signal”) discloses the “first clock output pin,” which is connected to the Receiver Unit PMA (“deserializer”). Ex. 1003, ¶269.

The clock signal pin for TXOUTCLK (“first transmitter side clock signal”) discloses the “second clock output pin,” which is connected to the Shared PLL and Divider (“÷N”) (part of the “serializer”). Ex. 1003, ¶269.

[22.b]: wherein the phase detector is not on the field programmable gate array and is operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array.

The combination of Giordano and Kaviani discloses this limitation. Ex. 1003 ¶270. As explained in element [1.h], it would have been obvious to a POSITA combining Giordano and Kaviani to place the Control Circuit of Kaviani (the “phase detector”) not on the FPGA. As explained in [22.a], the Control Circuit receives RXRECCLK and TXOUTCLK, and so is in communication with the first and second pins of the second interface of the FPGA. Thus, the combination of Giordano and Kaviani discloses this limitation. Ex. 1003 ¶270.

B. Ground 2: Claims 1–22 Are Rendered Obvious By Giordano in view of Kaviani and Raymond

1. Overview

This proposes using the Giordano and Kaviani combination of Ground 1 and further implementing components for financial trading context explicitly disclosed in Raymond.

a. Motivation to Combine Giordano, Kaviani, and Raymond

Raymond emphasized the importance of minimizing latency in communication devices, particularly for applications such as financial exchange. Ex. 1007 at 1:18–38. Raymond recognizes that higher clock rates reduce latency but also notes that this requires adding a distinct (faster) clock, and additional clock conversions introduce unwanted latency. *Id.*, 8:40–50.

A POSITA reading Raymond would therefore have recognized that Giordano in view of Kaviani offers a solution for synthesizing clock signals at the required frequencies while managing phase alignment and filtering jitter—precisely the clock distribution challenges Raymond identifies. Section VI.A.1.a (Motivation to Combine Giordano and Kaviani); Ex. 1003, ¶276.

A POSITA would have recognized Giordano in view of Kaviani as an attractive solution for the PLL functionality depicted in Raymond’s system, and motivated to look to Giordano and Kaviani to combine with Raymond. Raymond repeatedly discusses implementing its invention with Xilinx UltraScale GTY

transceivers. Ex. 1007 at 5:48–56, 6:3–8, 8:18–28, 8:51–55. A POSITA reading Raymond would have naturally consulted Xilinx’s own materials (such as Kaviani, a Xilinx patent) and publications demonstrating Xilinx FPGA implementations (such as Giordano), for a PLL-based phase alignment solution. Ex. 1003, ¶277.

A POSITA would have had a reasonable expectation of success in combining Giordano, Kaviani, and Raymond. A POSITA would have recognized that the FPGA’s programmable logic and on-chip clock management resources could be configured to implement the teachings of the three references as needed. Ex. 1003, ¶278. Because all references suggest implementations with Xilinx transceiver infrastructure, a POSITA would have had a high expectation that the combination would function as intended. Section VI.A.1.a (Motivation to Combine Giordano and Kaviani); Ex. 1003, ¶278.

2. Analysis

a. Claims 1–5

Giordano in view of Kaviani renders obvious these claims. Section VI.A.2.a–VI.A.2.c (Ground 1, cls. 1–5).

b. Claim 6

[6]: The system of claim 1, wherein the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.

Giordano in view of Kaviani renders obvious this claim. Section VI.A.2.d (Ground 1, cl. 6).

Raymond further discloses this limitation. Ex. 1003, ¶282.

Raymond discloses that data on the transmitting side includes “an outgoing data link layer signal 250 that has been outputted after logical processing (*e.g.*, applying financial trading algorithms)” and “[a] transmitting side PCS module 92 converts the data link layer signal to an outgoing electrical physical layer parallel output signal 252.” Ex. 1007, 11:57–63. The applying of financial trading algorithms in Raymond discloses the claimed “first set of operations.” Ex. 1003, ¶283. Raymond’s application of financial trading algorithms involves arithmetic operations, hence discloses this limitation. Ex. 1007, 11:57–60; Ex. 1003, ¶283.

c. Claim 7

[7]: The system of claim 1, wherein the first amount of data streams is the same as the second amount of data streams.

Giordano in view of Kaviani renders obvious this claim. Section VI.A.2.e (Ground 1, cl. 7).

Raymond further discloses this limitation. Ex. 1003, ¶285.

Raymond discloses that “the transmitting-side SerDes module 256 can have the same serialization ratio as the de-serialization ratio of the receiving side SerDes module 240.” Ex. 1007, 12:23–25. The same ratio results in the same parallel data streams, hence disclosing this limitation. Ex. 1003, ¶286.

d. Claim 8

[8]: The system of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.

Giordano in view of Kaviani renders obvious this claim. Section VI.A.2.f (Ground 1, cl. 8).

Raymond further discloses this limitation. Ex. 1003, ¶288.

Raymond discloses that “the UltraScale™ GTY from Xilinx™ has internal data buses of 16, 20, 32, 40 or 64 bits, with a minimum bit-width of 16 bits and a minimum de-serialization ratio of 1:16.” Ex. 1007, 6:5–8. A POSITA would have understood that the SerDes module 208 could be configured to apply any of these de-serialization ratios depending on the application requirements, and that the serialization ratio of SerDes module 256 would match. Ex. 1003, ¶289.

e. Claim 9

[9]: The system of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.

Giordano in view of Kaviani renders obvious this claim. Section VI.A.2.g (Ground 1, cl. 9).

Raymond further discloses this limitation. Ex. 1003, ¶291.

Raymond discloses that “internal data buses of 16, 20, 32, 40 or 64 bits.” Ex. 1007, 6:5–8. 16 is two to the power of four, 32 is two to the power of five, and 64 is two to the power of six, hence Raymond’s 16, 32, and 64 bit buses disclose this limitation. Ex. 1003, ¶292.

f. Claim 10

[10]: The system of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.

Giordano in view of Kaviani renders obvious this claim. Section VI.A.2.h (Ground 1, cl. 10).

Raymond further discloses this limitation. Ex. 1003, ¶294.

Raymond discloses that “internal data buses of 16, 20, 32, 40 or 64 bits.” Ex. 1007, 6:5–8. 20 is ten times two to the power of one, and 40 is ten times two to the power of two, hence Raymond’s 20 and 40 bit buses disclose this limitation. Ex. 1003, ¶295.

g. Claims 11–19

Giordano in view of Kaviani renders obvious these claims. Section VI.A.2.i–VI.A.2.q (Ground 1, cls. 11–19).

h. Claim 20

[20]: The system of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.

Raymond discloses this limitation. Ex. 1003, ¶297.

Raymond expressly identifies electronic trading as a primary application for its ultra-low latency communication device, and describes the incoming and outgoing data streams in terms that correspond directly to market data and order entry data. For example, Raymond discloses incoming and outgoing serial data streams in context of “financial trading data,” which are transmitted to and from “financial exchange.” Ex. 1007, 4:52–65.

Indeed, Raymond discloses “market data feed handler” and “market data feed distribution systems” applications, disclosing receiving market data. Ex. 1007, 13:61–64; Ex. 1003, ¶299. Raymond further discloses that the outgoing data link layer signal 250 is “outputted after logical processing (*e.g.*, applying financial trading algorithms),” hence disclosing sending out financial order related data and operations associated with trading algorithms. *Id.* at 11:57–60; Ex. 1003, ¶299.

i. Claim 21

[21]: The system of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.

Raymond discloses this limitation. Ex. 1003, ¶300. As discussed in claim 20, Raymond discloses receiving market data and transmitting the results of applying financial trading algorithms, hence disclosing this limitation. Ex. 1003, ¶301.

j. Claim 22

Giordano in view of Kaviani renders obvious this claim. Section VI.A.2.r (Ground 1, cl. 22).

**C. Ground 3: Claims 1–19, 22 Are Rendered Obvious By Giordano
in view of Kaviani further in view of Virtex-UG**

1. Overview

This proposes using the Giordano and Kaviani combination of Ground 1 and further modifying transceiver and FPGA configurations as necessary based on teachings of Virtex-UG.

**a. Motivation to Combine Giordano, Kaviani, and
Virtex-UG:**

While Giordano already inherently discloses and incorporates Virtex-UG, if necessary, a POSITA would have been motivated to look to Virtex-UG to combine with Giordano and Kaviani. Virtex-UG is a user guide for Xilinx Virtex FPGA offerings, which is the FPGA chip used in Giordano. Ex. 1005, 194, 197–199. Virtex-UG details how to use, configure, and modify the Virtex-5 FPGA “RocketIO” GTP transceiver. *See generally*, Ex. 1009; Ex. 1003, ¶305.

A POSITA reading Virtex-UG would therefore have recognized that its teachings would be helpful in the use, configuration, and modification of the FPGA system based on Giordano in view of Kaviani, including for synthesizing clock signals at the required frequencies while managing phase alignment and filtering jitter. Section VI.A.1.a (Motivation to Combine Giordano and Kaviani); Ex. 1003, ¶306.

A POSITA would have had a reasonable expectation of success in combining Giordano, Kaviani, and Virtex-UG. A POSITA would have recognized that the

FPGA's programmable logic and on-chip clock management resources could be configured to implement the teachings of the three references as needed. Ex. 1003, ¶307. Because all references suggest implementations with Xilinx transceiver infrastructure, a POSITA would have had a high expectation that the combination would function as intended. Section VI.A.1.a (Motivation to Combine Giordano and Kaviani); Ex. 1003, ¶307.

2. Analysis

a. Claims 1–19, 22

Giordano in view of Kaviani and Virtex-UG renders obvious these claims. Section VI.A.2 (Ground 1, Analysis).

D. Ground 4: Claims 1–22 Are Rendered Obvious By Giordano in view of Kaviani, Virtex-UG, and Raymond

1. Overview

This proposes using the Giordano, Kaviani, and Virtex-UG combination of Ground 3 and further modifying the FPGA for financial trading applications explicitly disclosed in Raymond.

a. Motivation to Combine Giordano, Kaviani, Virtex-UG, and Raymond

Motivations to combine Giordano, Kaviani, and Virtex-UG are detailed in Ground 3. Section VI.C.1 (Ground 3, Overview).

A POSITA would have been motivated to look to Raymond to combine with Giordano, Kaviani, and Virtex-UG, for the same reasons to combine Raymond with Giordano and Kaviani. Section VI.B.1 (Ground 2, Overview).

2. Analysis

a. Claims 1–22

Giordano in view of Kaviani and Virtex-UG renders obvious claims 1–19, 22. Section VI.C.2 (Ground 3, Analysis).

Raymond further discloses claims 6–10, 20–21. Section VI.B.2 (Ground 2, Analysis).

VII. CONCLUSION

Petitioners have established a reasonable likelihood that the Challenged Claims are unpatentable. Petitioners therefore respectfully request that IPR be instituted.

DATED: June 4, 2026

Respectfully Submitted,

By: / Brian M. Buroker /

Brian M. Buroker
(Reg. No. 39,125)
Gibson, Dunn & Crutcher LLP
1700 M St. NW
Washington, D.C. 20036-4504
Tel: (202) 955-8500
bburoker@gibsondunn.com

*Attorney for Petitioners OPTIVER US LLC
and OPTIVER TRADING US LLC*

CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned attorney hereby certifies that the word count for Sections I–VII of the foregoing Petition for *Inter Partes* Review is 13,989 according to the word count tool in Microsoft Word.

DATED: June 4, 2026

Respectfully Submitted,

By: / Brian M. Buroker /

Brian M. Buroker
(Reg. No. 39,125)
Gibson, Dunn & Crutcher LLP
1700 M St. NW
Washington, D.C. 20036-4504
Tel: (202) 955-8500
bburoker@gibsondunn.com

*Attorney for Petitioners OPTIVER US LLC
and OPTIVER TRADING US LLC*

CERTIFICATE OF SERVICE

The undersigned certifies service pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(a), (b) on the Patent Owner via FedEx overnight mail of a copy of this Petition for *Inter Partes* Review and supporting materials at the correspondence address of record for the '069 patent shown in USPTO Patent Center:

AMSTER, ROTHSTEIN & EBENSTEIN LLP
405 LEXINGTON AVENUE
FLOOR 48
NEW YORK, NY 10174

DATED: June 4, 2026

Respectfully Submitted,

By: / Brian M. Buroker /

Brian M. Buroker
(Reg. No. 39,125)
Gibson, Dunn & Crutcher LLP
1700 M St. NW
Washington, D.C. 20036-4504
Tel: (202) 955-8500
bburoker@gibsondunn.com

*Attorney for Petitioners OPTIVER US LLC
and OPTIVER TRADING US LLC*

APPENDIX: CHALLENGED CLAIM LISTING

No.	Limitation
[1.pre]	A field programmable gate array system comprising:
[1.a]	a field programmable gate array comprising:
[1.b]	<p>(1) a first interface comprising:</p> <p>(A) a first reference clock pin, wherein said first reference clock pin is configured to receive a first clock signal having a first frequency and a first phase;</p> <p>(B) a second reference clock pin, wherein said second reference clock pin is configured to receive the first clock signal;</p> <p>(C) a first plurality of data pins, wherein said first plurality of data pins is configured to receive a first serial data stream;</p> <p>(D) a second plurality of data pins, wherein said second plurality of data pins is configured to transmit a second serial data stream;</p>
[1.c]	<p>(2) a deserializer operationally connected to:</p> <p>(A) the first reference clock pin to receive as a first input the first clock signal and</p> <p>(B) the first plurality of data pins to receive as a second input the first serial data stream,</p>
[1.d]	<p>And wherein the deserializer is configured to:</p> <p>(A) convert the first serial data stream into a first plurality of parallel data streams having a first amount of data streams, and</p> <p>(B) generate a first receiver side clock signal based on the first clock signal, wherein the first receiver side clock signal has a third frequency and a third phase; and</p> <p>(C) transmit the first plurality of parallel data streams and the first receiver side clock signal within the field programmable gate array;</p>

No.	Limitation
[1.e]	(3) computational circuitry operationally connected to the deserializer to receive the first plurality of parallel data streams and the first receiver side clock signal, wherein the computational circuitry is configured to perform a first set of operations on the first plurality of parallel data streams to generate a second plurality of parallel processed data streams having a second amount of data streams and the computational circuitry performs the first set of operations to generate the second plurality of parallel processed data without use of a clock domain crossing circuit;
[1.f]	(4) a serializer operationally connected to: (A) an adjustable transceiver phase lock loop to receive as a third input a first wire rate clock signal, wherein the first wire rate clock signal has a fourth frequency and a fourth phase; (B) the second plurality of data pins to transmit as a first output the second serial data stream; (C) the computational circuitry, wherein the serializer receives the second plurality of parallel processed data streams from the computational circuitry and the serializer transmits to the computational circuitry a first transmitter side clock signal including a fifth frequency and a fifth phase; and
[1.g]	wherein the serializer is configured to: (A) convert the second plurality of parallel processed data streams into the second serial data stream; (B) generate the first transmitter side clock signal based on the first wire rate signal, wherein the first transmitter side clock signal has the fifth frequency and the fifth phase, wherein the fifth frequency is different than and less than the fourth frequency; and (C) transmit the second serial data stream to the second plurality of data pins for transmission off the field programmable gate array; and
[1.h]	(b) a phase control circuit, provided at least partially on the field programmable gate array, wherein the phase control circuit comprises:

No.	Limitation
[1.i]	(1) a phase detector configured to compare the third phase of the first receiver side clock signal to the fifth phase of the transmitter side clock signal and to generate a phase difference indicator signal based on a difference between the third phase of the first receiver side clock signal and the fifth phase of the transmitter side clock signal;
[1.j]	(2) a phase controller operationally connected to the phase detector and configured to receive the phase difference indicator signal, and wherein the phase controller is configured to determine adjustment information based on the phase difference indicator signal; and
[1.k]	(3) the adjustable transceiver phase lock loop operationally connected to the phase controller and configured to receive the adjustment information as well as operationally connected to the second reference clock pin of the first interface of the field programmable gate array,
[1.l]	wherein the adjustable transceiver phase lock loop is configured to generate a second clock signal including the second frequency and the second phase based on the first clock signal received via the second reference clock pin and process the second clock signal based on the adjustment information received from the phase controller to generate the first wire rate clock signal,
[1.m]	wherein the transmitter side clock signal and the first receiver side clock signal are phase aligned so that there is a fixed phase difference between the third phase and the fifth phase.
[2]	The system of claim 1, wherein the third frequency corresponds to the first frequency.
[3]	The system of claim 2, wherein the third phase is not aligned with the first phase.
[4]	The system of claim 1, wherein the third frequency is different than the first frequency.
[5]	The system of claim 1, wherein the first set of operations does not include clock domain crossing operations that delays processing of the first set of parallel data streams.

No.	Limitation
[6]	The system of claim 1, wherein the first set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.
[7]	The system of claim 1, wherein the first amount of data streams is the same as the second amount of data streams.
[8]	The system of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.
[9]	The system of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to two (2) to the power of N, where N is an integer.
[10]	The system of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to ten (10) times two (2) to the power of N, where N is an integer.
[11]	The system of claim 7, wherein the first amount of data streams and the second amount of data streams are equal to thirty-three (33) times two (2) to the power of N, where N is an integer.
[12]	The system of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is the second amount of data streams.
[13]	The system of claim 1, wherein the fourth frequency is equal to x times the fifth frequency, where x is half of the second amount of data streams.
[14]	The system of claim 1, wherein the fourth frequency is a rational multiple of the second frequency.
[15]	The system of claim 1, wherein the phase difference indicator signal is a pulse signal.

No.	Limitation
[16]	The system of claim 1, wherein adjustment information indicates at least one of the following: (A) a desired phase; (B) a desired frequency; (C) a change in phase; and (D) a change in frequency.
[17]	The system of claim 16, wherein adjustment information comprises a voltage.
[18]	The system of claim 17, wherein adjustment information comprises a digital transmission.
[19]	The system of claim 1, wherein the adjustment information is used to do at least one of the following: (i) set a bias to an oscillator; (ii) set a divider ratio; and (iii) set a delay.
[20]	The system of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order entry data, and the first operation comprises a trading algorithm.
[21]	The system of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.
[22.a]	The system of claim 1, wherein the field programmable gate array further comprises: (5) a second interface comprising: (A) a first clock output pin configured to transmit the first receiver side clock signal, wherein the first clock output pin is operationally connected to the deserializer; and (B) a second clock output pin configured to transmit the first transmitter side clock signal, wherein the second clock output pin is operationally connected to the serializer; and
[22.b]	wherein the phase detector is not on the field programmable gate array and is operationally connected to the first clock output pin and the second clock output pin of the second interface of the field programmable gate array.