UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

OPTIVER US LLC and OPTIVER TRADING US LLC,

Petitioners

v.

HFT SOLUTIONS, LLC,

Patent Owner

Case No. IPR2026-00387
Patent No. 11,329,655

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

I. INTRODUCTION 1
II. BACKGROUND 1
A. Optiver's Petition 1
B. Overview of the '655 Patent 2
III. LEVEL OF ORDINARY SKILL IN THE ART 5
IV. THE PETITION DOES NOT DEMONSTRATE A LIKELIHOOD OF SUCCESS ON THE MERITS 5
A. Giordano Uses A Clock Domain Crossing Operation That Delays Processing Of the First Set of Parallel Data Streams 6
1. Giordano Teaches A Clock Domain Crossing 6
2. Virtex-UG Does Not Remove the Clock Domain Crossing 7
a. Bypassing the Receiver Side FIFO is Not Inherent To Giordano 8
b. Giordano Does Not Incorporate Ex. 1009 9
c. Ex. 1009 Is Not Prior Art 10
d. The Proposed Combination Violates the Teachings of Ex. 1009 13
B. Kaviani Does Not Teach A Phase Detector That Is Part Of The FPGA System And Not Part Of The Gate Array 14
V. CONCLUSION 17

TABLE OF AUTHORITIES

Cases

Apple Inc. v. Int'l Trade Comm'n,
725 F.3d 1356 (Fed. Cir. 2013).....10

Commonwealth Sci. & Indus. Rsch. Organisation v. Buffalo Tech. (USA), Inc.,
542 F.3d 1363 (Fed. Cir. 2008).....9

Finjan, Inc. v. Sophos, Inc.,
No. 14-CV-01197-WHO, 2016 WL 2988834 (N.D. Cal. May 24, 2016) 12

Hulu, LLC v. Sound View Innovations, LLC,
IPR2018-01039, Paper 29 (PTAB Dec. 20, 2019).....11

Kyocera Wireless Corp. v. Int'l Trade Comm'n
545 F.3d 1340 (Fed.Cir.2008).....11

Navico Inc. v. Garmin Int'l, Inc.,
No. 216CV00190JRGRSP, 2017 WL 3750252 (E.D. Tex. July 28, 2017).....12

ServiceNow, Inc. v. Hewlett-Packard Co.,
Case IPR2015- 00716, slip op. (Paper 13) (PTAB Aug. 26, 2015) 12

Telemac Cellular Corp. v. Topp Telecom, Inc.,
247 F.3d 1316 (Fed. Cir. 2001).....8

PATENT OWNER'S EXHIBIT LIST

No.	Description
Ex. 2001	*HFT Solutions, LLC, v. Optiver US LLC et al*, Case No. 7:25-cv-00415, Dkt. 1 (Sept. 8, 2025, W.D. Tex)
Ex. 2002	Optiver reports strong financial results for 2024, available at https://www.optiver.com/insights/news/optiver-reports-strong-financial-results-for-2024/

I. INTRODUCTION

The present Petition fails to establish a reasonable likelihood of success on the merits for numerous reasons. First, the Petition's primary reference for all grounds expressly includes a clock domain crossing circuit, contravening limitation 1.h. Second, the Petition cannot show support its showing of a phase control circuit partially on the FPGA because no reference shows that.

Because the Petition makes only a token effort to address these fatal issues, the Petition cannot succeed and justifies denial of institution. Together, they make it clear there is no likelihood of success on the merits. Because the Petition does not present any grounds that can be instituted, much less any that present a reasonable likelihood of success, institution should be denied.

II. BACKGROUND

A. Optiver's Petition

Petitioner Optiver US LLC and Optiver Trading US LLC ("Optiver" or "Petitioner") challenges claims 1–30 of U.S. Patent No. 11,329,655 (the "'655 Patent"). Petitioner structures its asserted grounds for unpatentability as follows:

- Ground 1: Giordano and Kaviani Render Obvious Claims 1-23, 26-30
- Ground 2: Giordano, Kaviani, and Raymond Render Obvious Claims 1-30
- Ground 3: Giordano, Kaviani, and Virtx-UG Render Obvious Claims 1-23, 26-30

- Ground 4: Giordano, Kaviani, Virtx-UG, and Raymond Render Obvious Claims 1-30

Because all challenged dependent claims across all grounds depend from claim 1, this Preliminary Response need only address the Petition's arguments concerning claim 1. If the Petition does not show a reasonable likelihood of prevailing on claim 1, then it cannot prevail on any other challenged claim.

B. Overview of the '655 Patent

At a high level, the '655 Patent is directed to addressing a need for phase control to minimize latency in high-speed FPGA systems. Ex. 1001 at 1:25-30, Abstract. Latency reduction is important "in the financial industry in high frequency trading where the rapid processing of the FPGA is desired." *Id*. at 1:37-39. Contrary to the prior art method of using a clock domain crossing circuit to synchronize clock signals, which adds delay, the invention teaches a technique that avoids clock domain crossings. *Id*. at 1:43-49.

In particular, the '655 Patent teaches utilizing a phase-locked loop to avoid the need for clock domain crossings. *Id*. 1:25-30. This solution is reflected, for example, in claim 1 of the '655 Patent, which recites:

> 1. A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:
> (a) receiving, by a deserializer via a first reference clock pin in a first interface of a field programmable array in the field programmable gate

array system, a first clock signal having a first frequency and a first phase;

(b) receiving, by the deserializer via a first plurality of data pins of the first interface of the field programmable gate array in the field programmable gate array system, the first serial data stream to generate a first receiver side clock signal having a second frequency and a second phase based on the first clock signal, and to convert the first serial data stream into a first plurality of parallel data streams comprising a first plurality of data items and a first amount of data streams;

(c) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first receiver side clock signal and the first plurality of data streams;

(d) transmitting, from the deserializer to a phase detector of the field programmable gate array system, the first receiver side clock signal;

(e) generating, using the field programmable gate array system, a first transmitter side clock signal having a third frequency and a third phase, by performing at least the following steps until a first output of the phase detector is below a first threshold level:

(i) receiving, by an adjustable transceiver phase lock loop the first clock signal to generate a second clock signal having a fourth frequency and a fourth phase based on the first clock signal;

(ii) generating a first wire rate clock signal having a fifth frequency and a fifth phase based on the second clock signal and the adjustment information;

(iii) generating, by a serializer in the field programmable gate array, an interim transmitter side clock signal having a sixth frequency and a sixth phase;

(iv) transmitting, from the serializer to the phase detector, the interim transmitter side clock signal;

(v) generating, by the phase detector, the first output based on a comparison of the first receiver side clock signal and the interim transmitter side clock signal;

(vi) transmitting, from the phase detector to a phase controller of the field programmable gate array system which is placed within the field programmable gate array, the first output;

(vii) determining, by the phase controller, interim adjustment information based on the first output; and

(viii) transmitting, from the phase controller to the adjustable transceiver phase lock loop, the interim adjustment information, wherein, the adjustable transceiver phase lock loop adjusts the second clock signal based on the interim adjustment information and steps (i) through (viii) are repeated until the first output of the phase detector is below the first threshold level;

(f) transmitting, from the serializer to the computational circuitry, the first transmitter side clock signal;

(g) performing, by the computational circuitry, a first set of operations on at least a portion of the first plurality of data items to generate a second plurality of parallel data streams comprising a second amount of data streams, wherein the first set of operations does not include clock domain crossing operations that delay processing of the first set of parallel data streams; and

(h) transmitting off the field programmable gate array system via a second plurality of data pins of the first interface using a serializer a second serial data stream based on the second plurality of parallel data streams.

Ex. 1001 at claim 1.

All other challenged claims (2–30) depend from claim 1.

III. LEVEL OF ORDINARY SKILL IN THE ART

The Petition proposes that a person of ordinary skill in the art in the field of the '655 Patent "would have a bachelor's degree in Computer Engineering, Electrical Engineering, or equivalent discipline, and at least three years of academic or industry experience relating to clocking techniques for FPGAs with high-speed transceivers." Paper 1 ("Petition" or "Pet.") at 6. For purposes of this preliminary response, Patent Owner does not challenge that definition.

IV. THE PETITION DOES NOT DEMONSTRATE A LIKELIHOOD OF SUCCESS ON THE MERITS

Each of the Petitions four grounds fail to show the same three limitations were obvious. While the Petition concedes FIFO buffers violate limitation 1.h, it is unable to navigate its express inclusion under any theory. Likewise, as to limitations 1.d and 1.f are shown only through hindsight bias not in the teaching of any prior art reference. Because the Petition presents no ground likely to invalidate any claim, institution should be denied.

A. Giordano Uses A Clock Domain Crossing Operation That Delays Processing Of the First Set of Parallel Data Streams

Giordano expressly teaches a clock domain crossing in a manner excluded by limitation 1.h. This crossing cannot be removed, indeed the user manual Optiver cites explains why. Limitation 1.h specifically prohibits the use of a clock domain crossing circuit that delays processing of the first set of parallel data streams. But Optiver focuses its analysis on removing only one of two clock domain crossings and when attempting to remove the other, Optiver references the wrong user manual which is not prior art and ultimately explains that the proposed combination is not feasible.

As all claims rely upon claim 1 and each of grounds 1-4 rely on Giordano in this same way for this limitation[1], they all fail.

1. Giordano Teaches A Clock Domain Crossing

Optiver's analysis of Giordano itself is insufficient to meet this limitation. Optiver focuses on bypassing a First In First Out (FIFO) buffer in the transmitter of Giordano. *See* Paper 1 at 37-39. But Giordano still teaches the same FIFO buffer on its receiver which processing the data flow.

[1] While Grounds 3-4 presents Virtex-UG as an obviousness reference, they do not present any new argument for why its inclusion would be obvious or at all motivated. *See* Paper 1 at 68-69 (providing no motivation to bypass a receiver side FIFO).

Indeed, the "first set of parallel data streams" does not bypass the receiver side FIFO buffer. This adds delay to the data flow being processed. Giordano's Figure 1 clearly shows data flowing from the SIPO (the "first set of parallel data streams") passes through a FIFO buffer before continuing to a FPGA Interface and the FPGA Fabric. Ex. 1005 at 195. Indeed, Section II of Giordano explains data is transmitted from the SIPO (serial in to parallel out) to the Comma Detect and Align block and the data "is then 10b to 8b decoded, if needed, and transferred to a FIFO (also called elastic buffer) in order to enter the RXUSRCLK domain." *Id*. This is in stark contrast to what Giordano provides regarding the transmitter side FIFO where it explains "[i]n some configurations XCLK and TXUSRCLK have the same frequency and a constant phase offset" so the FIFO may be bypassed. *Id*. Giordano offers no means to bypass the receiver side FIFO. Giordano's Table 1 confirms this distinction, describing the transmitter FIFO as "bypassed" and thus only having a 4 ns latency or delay, as compared with the receiver side FIFO with 20 ns of latency or delay. *Id*. at 198. As such, Giordano has a FIFO to cross clock domains that adds a 20ns delay to the "first plurality of data items" prior to it being processed. This does not meet limitation 1.e.

2. Virtex-UG Does Not Remove the Clock Domain Crossing

The Petition's reference to Virtex-UG does not rescue Optiver's failed analysis. Tellingly, while Optiver's analysis of Giordano ignores its receiver side

FIFO, the analysis of Virtex-UG recognizes the receiver side FIFO violates limitation 1.h. However, the analysis of Virtex-UG offers no basis to bypass Giordano's receiver side FIFO. Such a change to Giordano is not obvious, inherent, express, or even feasible. For these multiple reasons, Virtex-UG does not render this bypass obvious or inherent.

a. Bypassing the Receiver Side FIFO is Not Inherent To Giordano

First, Virtex-UG is not inherent to Giordano. While the Petition states the correct standard, "whether a feature, while not explicitly discussed, is necessarily present in a reference," Paper 1 at 16 citing *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1328 (Fed. Cir. 2001), the Petition cannot show bypassing Giordano's receiver side FIFO is necessarily present. Optiver argues "Giordano presents a system with the 'RocketIO' GTP transceiver of the Xilinx Virtex-5 FPGA family" and notes Giordano follows the procedures of Virtex-UG "for activating the alignment circuit." Paper 1 at 15-16. But this bears no relation to the cited feature of Virtex-UG, bypassing a receiver side FIFO. Virtex-UG itself provides bypassing this buffer "is an advanced feature" only operable "under certain system-level conditions and data rates." Ex. 1009 at 177. There is no reason an "advanced feature" would necessarily be present in Giordano's presentation of the RocketIO GTP transceiver. Especially when, as noted above, Giordano expressly does not bypass the receiver FIFO.

b. Giordano Does Not Incorporate Ex. 1009

Second, Virtex-UG's teachings are not express in Giordano. Giordano does not incorporate Ex. 1009 by reference. Ex. 1009 is cited by neither Giordano nor Kaviani and is not even prior art.

The only place a user manual[2] is referenced is in a footnote citation. But a footnote citation to a user manual, is not an incorporation by reference. *See Commonwealth Sci. & Indus. Rsch. Organisation v. Buffalo Tech. (USA), Inc.*, 542 F.3d 1363, 1372 (Fed. Cir. 2008) (explaining "[t]he footnote citation in [the host document] could provide justification for combining the reference for obviousness[3] purposes, but there is nothing about the reference [] that appears to constitute an incorporation of any or all of the information from the [] reference under the standard set forth in *Advanced Display Systems*."). Indeed, here Giordano makes only passing reference to two user manuals, a Virtex-5 user manual and an Evaluation Platform User Guide used for testing. Ex. 1005 at 199, 201. Those passing reference never address all of Ex. 1009 or bypassing a reference side buffer. Rather, they reference "[t]he architecture we present in this paper" and "the procedure we follow for activating the alignment circuit." *Id*. at 194, 197. But passing references that do not

[2] As explained below, the reference is not even to Ex. 1009.

[3] While the Petition mentions it would be obvious to implement Virtex-UG's teachings, "including for synthesizing clock signals at the required frequencies while managing phase alignment and filtering jitter," there is no motivation directed to bypassing a FIFO buffer in Giordano. *See* Paper 1 at 68; Ex. 1003 at ¶238.

even mention the portion relied upon by the presenting party do not incorporate the reference material. *See Apple Inc. v. Int'l Trade Comm'n,* 725 F.3d 1356, 1362-63 (Fed. Cir. 2013). Giordano only references user manuals for the portions it uses and does not bypass its receiver side FIFO, thus such a technique is not available under incorporation by reference.

Moreover, Ex. 1009 is not cited by Giordano or Kaviani. Giordano cites "Virtex-5 FPGA RocketIO GTP Transceiver USER Guide Xilinx, UG196, v. 1.7, 2008." Ex. 1005 at 201. Ex. 1009 is version 2.1 and has a date on its face of December 3, 2009. Ex. 1009. Ex. 1009 is an entire version and year later than what Giordano cites and the relevant portions regarding TX Buffering and RX Elastic Buffering cited by the Petition were extensively revised and revised in version 2.1. *See* Ex. 1009 at 6. Likewise, Kaviani has no citation to such user manuals at all. Because Optiver's entire basis for alleging Ex. 1009 is inherent or express to Giordano is Giordano's citation to a different user manual, Ex. 1009 is clearly neither express nor inherent. Similarly, it is not obvious to rely on an entirely user manual than cited in the reference.

c. Ex. 1009 Is Not Prior Art

Further still, Optiver fails to establish Ex. 1009 is even prior art. As Ex. 1009 is not a patent or patent application, the Petition must show that it was publicly available, i.e., that it was "disseminated or otherwise made available to the extent

that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it." *Kyocera Wireless Corp. v. Int'l Trade Comm'n,* 545 F.3d 1340, 1350 (Fed.Cir.2008). "[T]he burden is on the petitioner to identify with particularity evidence sufficient to establish a reasonable likelihood that the reference was publicly accessible before the critical date of the challenged patent, and therefore that there is a reasonable likelihood that it qualifies as a printed publication." *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 16 (PTAB Dec. 20, 2019) (precedential). Neither the Petition nor its expert declarations do this.

First, the Petition itself only suggest "Virtex-UG was published on December 3, 2009" and then concludes it qualifies as prior art. Paper 1 at 4. But a publishing date, particularly one supported only by assumption and hearsay, does not establish public availability. That requires dissemination and availability to the correct audience. The Petition never so much as states Ex. 1009 was ever available to public, much less showing such. Without even that much, Optiver cannot show Ex. 1009 is prior art.

Second, Dr. Gardner who is cited only for the notion that Ex. 1009 was published on December 3, 2009, similarly fails to show public availability. While Dr. Gardner declares Ex. 1009 authentic this has nothing to do with public availability. *See* Ex. 1004 at ¶¶41-46. Similarly, paragraph 47, the only portion of

her declaration relating to publication, fails to demonstrate public availability. Dr. Gardner merely reads a date from the user manual and assumes public accessibility based on "standard practice for technology companies." *Id*. at ¶47. But that date is hearsay and is routinely rejected as a basis for dating documents. *See e.g. ServiceNow, Inc. v. Hewlett-Packard Co.*, Case IPR2015- 00716, slip op. at 17 (Paper 13) (PTAB Aug. 26, 2015) (finding a copyright notice unreliable hearsay for purposes of establishing the date of a printed publication); *Navico Inc. v. Garmin Int'l, Inc.*, No. 216CV00190JRGRSP, 2017 WL 3750252, at *3 (E.D. Tex. July 28, 2017), *report and recommendation adopted*, No. 216CV00190JRGRSP, 2017 WL 3764213 (E.D. Tex. Aug. 29, 2017) (copyright and revision dates insufficient to show date of distribution); *Finjan, Inc. v. Sophos, Inc.*, No. 14-CV-01197-WHO, 2016 WL 2988834, at *26 (N.D. Cal. May 24, 2016) (copyright date and screen shot from decades later showing "Published/distributed" in 1995 insufficient to show date of distribution). Moreover, Dr. Gardner offers no basis for the alleged "standard practice for technology companies to add the release date to User Manuals." *See* Ex. 1004 at ¶47. Her declaration identifies no experience with "technology companies" or their practices regarding user manuals. At best, she notes she has assisted engineers in finding technical materials, but finding technical materials has little to do with establishing when or how they are made available or to whom as the legal standard requires. Because the declaration "authenticates" the wrong user manual

and offers no reliable basis for when or if it was publicly accessible, the Petition cannot show Ex. 1009 is prior art. Because every ground referencing Giordano relies on Ex. 1009 to suggest bypassing the receiver side FIFO, all such grounds fail.

d. The Proposed Combination Violates the Teachings of Ex. 1009

Last, the proposed revision of Giordano according to Ex. 1009 expressly violates Ex. 1009. Ex. 1009 expressly provides either FIFO buffer can only be bypassed "under certain system-level conditions and data rates." *See* Ex. 1009 at 177. As the Petition acknowledges "RXUSRCLK must be driven directly from RXECCLK using a BUFR regional clock buffer." *Id*. But the Petition's proposed arrangement does not include a BUFR regional clock buffer, instead the RXUSRCLK is RXECCLK, not driven from it. *See* Paper 1 at 11-13. Indeed, a similar requirement is in place for bypassing the transmit side that "[w]hen the buffer is bypassed, TXUSRCLK must be driven directly from REFCLKOUT using a BUFR regional clock buffer…" Ex. 1009 at 116. But the Petition proposes TXUSRCLK be driven by Giordano's Shared PLL, Paper 1 at 12, not the "clock synthesized in the fabric from the external reference clock" taught by Giordano, Ex. 1005 at 195. As a result, even if it was obvious to combine the Petition's references to bypass the receiver side FIFO, the proposed combination breaks Giordano's technique for bypassing the transmit side FIFO upon which the ground also depends.

Giordano's express teachings violate the Petition's showing of limitation 1.h by including a FIFO buffer on the receiver side. Giordano does not rely on Ex. 1009 or any version of that user guide to necessarily require bypassing the FIFO buffer it expressly includes. Moreover, there is no teaching or reason a POSITA would have been motivated to remove the FIFO buffer from Giordano based on Ex. 1009, not the least because it is not prior art. Because each of Grounds 1-4 rely on Giordano and Virtex-UG in the same way, *see* Paper 1 at 36-39, 63, 69-70, each ground fails.

B. Kaviani Does Not Teach A Phase Detector That Is Part Of The FPGA System And Not Part Of The Gate Array

The Petition relies on Kaviani to teach limitations 1.d and 1.f. In relevant part, these limitations require a phase detector "of the field programmable gate array system" and "a phase controller of the field programmable gate array system which is placed within the field programmable gate array." The Petition proposes this is met by placing Kaviani's control circuit off the FPGA but its Decoder on the FPGA. Paper 1 at 24. However, Kaviani does not teach that its components should be so arranged or indeed any particular arrangement within an FPGA. This, and in particular splitting Kaviani's figure 2 into a portion on the FPGA and a portion not on the FPGA, is an invention of Optiver and its expert. But neither the Petition nor Dr. Schaefer offer anything beyond hindsight to support this division of Kaviani's circuitry.

Kaviani discloses "a circuit 200 for deskewing and phase shifting a generated clock signal." Ex. 1010 at 3:64-65. Circuit 200 is composed of a control circuit 202 and a clock generation circuit 206. *Id*. at 3:67-4:4. While Kaviani does mention FPGAs on three occasions, *id*. at 1:45-46; 2:40-43; 5:27-29, none of these mentions suggests a particular arrangement of circuits 202 and 206. Rather, the first two references provide background on why Kaviani's phase shifting invention is important, suggesting FPGA could use the invention. *See id*. at 1:45-46; 2:40-43. The last provides that implementations of Figs 2 and 3 may be found in certain Xilinx FPGAs but with no clarity regarding the FPGA fabric. *See id*. at 5:27-29. As such, Kaviani does not teach a POSITA to place circuit 202 in an FPGA system but not in the FPGA while placing circuit 206 in the FPGA itself.

The Petition's counter argument here is that "Kaviani describes its Clock Generator (which includes multiple decoders) and Control Circuit as separate circuits, supporting these are implementable in different physical regions," citing Fig. 2 and Dr. Schaefer. Paper 1 at 11-12; *see also id*. at 24 (similar, pointing back to 11-12). But Dr. Schaefer offers no such support nor does Figure 2. Indeed, the cited portion of Dr. Schaefer's declaration, ¶112, discusses the teachings of Giordano and only cites Kaviani's figure 2 to repeat the petition. *See* Ex. 1003 at ¶112. Likewise, Figure 2 is described as a single circuit, Ex. 1010 at 3:64-65, and includes no suggestion that any portion could be "implementable in different

physical regions." The Petition offers nothing reliable to show a part on/part off FPGA arrangement of Kaviani's Figure 2 is disclosed in Kaviani.

Likewise, the Petition cannot demonstrate such an arrangement would have been obvious to a POSITA.

The Petition argues the Giordano-Kaviani combination as a whole would be obvious based on Giordano recognizing that "jitter filtering is beneficial to condition the recovered receiver clock." Paper 1 at 11-12. The Petition argues "Kaviani provides precisely such a solution through a phase shifting circuit that filters jitter…" *Id*. But the Petition cannot show any motivation to implement Kaviani's figure 2 in a manner that, as explained above, is not taught by Kaviani.

Rather, Dr. Schaefer suggests that because Giordano uses components both on and off the FPGA, "[i]mplementing Kaviani's Clock Generator in the FPGA Fabric and Control Circuit in the circuit board[] represents a straightforward extension of the techniques already used in Giordano." Ex. 1003 at ¶112. In the next paragraph, Dr. Schaefer explains "such FPGA hardware programming is how the '655 patent suggests implementing the claimed invention … [t]hus, implementing Kaviani's teachings in Giordano's FPGA mirrors the '069 patent's own implementation approach." *Id*. at ¶113. But this only suggests the prior art shows a POSITA ***could***[4] implement Kaviani in Giordano according to limitation 1.h but not

[4] Dr. Schaefer does not actually show a POSITA could implement Kaviani in this

why a POSITA ***would***. For why, at best, both Dr. Schaefer and the Petition cite to the patent, relying on hindsight bias.

Optiver fails to show the combination of Giordano and Kaviani render limitations 1.d and 1.f obvious. Neither reference teaches the part on/part off FPGA arrangement. Likewise, the Petition offers no reason for why the arrangement would be obvious. Because limitations 1.d and 1.f are not obvious, each of grounds 1-4 fail.

V. CONCLUSION

Because of the failures noted above, Patent Owner respectfully asks the Director to find the Petition has failed to establish any likelihood of success on the merits and deny institution.

Date: September 8, 2026

/ Dale Chang /

Dale Chang (Reg. No. 61,476)
Russ August & Kabat
12424 Wilshire Blvd., 12th Fl.
Los Angeles, CA 90025
Phone: (310) 826-7474
Fax: (310) 826-6991

Counsel for Patent Owner

way. The components pointed to in Giordano are entirely distinct from those in Kaviani. For example, Giordano implements a Comma Detector and Aligner in the fabric while the proposed Kaviani implementation would require an entire clock generation circuit. A comma detector and clock generation circuit are not shown to be at all comparable.

CERTIFICATE OF WORD COUNT

I certify that there are 4,023 words in this paper, excluding the portions exempted under 37 C.F.R. § 42.24(a)(1), according to the word count tool in Microsoft Word.

/ Dale Chang /
Dale Chang (Reg. No. 61,476)

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above document was served on September 8, 2026 by filing this document through the Patent Trial and Appeal Case Tracking System (PTACTS) as well as delivering a copy via electronic mail upon the following attorneys of record for Petitioner:

Brian M. Buroker
Gibson, Dunn & Crutcher LLP
1700 M St. NW
Washington, D.C. 20036-4504
Tel: (202) 955-8500
bburoker@gibsondunn.com

Benjamin Hershkowitz
Brian A. Rosenthal
(pro hac vice motion requested)
Gibson, Dunn & Crutcher LLP
200 Park Avenue
New York, NY 10166-0193
Tel: (212) 351-2339
bhershkowitz@gibsondunn.com

Date: September 8, 2026

/ Dale Chang /

Dale Chang (Reg. No. 61,476)
Russ August & Kabat
12424 Wilshire Blvd., 12th Fl.
Los Angeles, CA 90025
Phone: (310) 826-7474
Fax: (310) 826-6991

Counsel for Patent Owner