

Filed on behalf of Luxottica of America Inc. and Meta Platforms, Inc.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LUXOTTICA OF AMERICA INC. AND META PLATFORMS, INC.
Petitioners

v.

SOLOS TECHNOLOGY LIMITED,
Patent Owner.

Case No. IPR2026-00412
U.S. Patent No. 11,082,055

**DECLARATION OF THOMAS W. KENNY, PH.D.
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 11,082,055**

<p>Luxottica et al. v. Solos IPR2026-00412 Petitioners' Ex. 1003</p>

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I, Dr. Thomas W. Kenny, declare as follows:

I. INTRODUCTION

1. I have been retained as an expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 11,082,055 (“the ’055 patent”) (Ex.1001).¹ I have been asked to analyze the scope and content of the ’055 patent relative to the state of the art at the time of the earliest application to which the ’055 patent claims priority. My analysis relates to claims 1-10 (“the challenged claims”). I have also been retained to provide analysis regarding what a person of ordinary skill in the art (“POSA”) would have understood at the time of the earliest application underlying the ’055 patent.

2. This declaration summarizes the opinions I have formed to date. I reserve the right to modify or amend my opinions, if necessary, based on further review and analysis of information that I receive subsequent to the filing of this declaration, including in response to positions taken by Solos Technology Limited (“Solos”) or its experts that I have not yet seen, including any secondary considerations evidence that Solos or its expert may consider and present.

¹ In this declaration, I refer to exhibits that I understand are to be attached to the petition for *Inter Partes* Review of the ’055 patent.

3. I am being compensated for my time at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study and analysis, the substance of my opinions, or the outcome of any proceeding involving the challenged claims. I have no financial interest in the outcome of this matter or in any litigation involving the '055 patent.

II. BACKGROUND AND QUALIFICATIONS

4. My qualifications generally are set forth in my curriculum vitae ("CV"), which is attached as Ex.1004 and also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

5. My academic and professional background is in Physics, Mechanical Engineering, Sensing, and Robotics, with a research specialization focused on microfabricated physical sensors, and I have been working in those fields since the completion of my Ph.D. more than 35 years ago. The details of my background and education and a listing of all publications I have authored in the past 40 years are provided in my CV. Below I provide a short summary of my education and experience which I believe to be most pertinent to the opinions that I express here.

6. I received a B.S. in Physics from University of Minnesota, Minneapolis in 1983, and a Ph.D. in Physics from University of California at

Berkeley in 1989. I was educated as a Physicist specializing in sensors and measurement. My Physics Ph.D. thesis involved measurements of the heat capacity of monolayers of atoms on surfaces, and relied on precision measurements of temperature and power using time-varying electrical signals, and also on the design and construction of miniature sensor components and associated electrical circuits for conditioning and conversion to digital format.

7. After completion of my Ph.D. in Physics at U.C. Berkeley in 1989, I joined the Jet Propulsion Laboratory (JPL) in Pasadena, CA, as a staff scientist, and began working on miniature sensors and instruments for small spacecraft. This work involved the use of silicon microfabrication technologies for miniaturization of the sensors, and served as my introduction to the field of micro-electromechanical systems (MEMS), or the study of very small mechanical sensors powered by electricity and used for detection of physical and chemical signals.

8. While at JPL, we developed accelerometers, uncooled infrared sensors, magnetometers, seismometers, force and displacement sensors, soil chemistry sensors, miniature structures for trapping interstellar dust, and many other miniature devices. Some of these projects led to devices that were launched with spacecraft headed for Mars and for other interplanetary missions. Much of this work involved the use of physical sensors for detection of small forces and displacements using micromechanical sensors.

9. I am presently the Richard Weiland Professor at the Department of Mechanical Engineering at Stanford University, where I have taught for the past 32 years. I am also currently the Senior Associate Dean of Engineering for Student Affairs at Stanford.

10. For almost all of these 32 years, I have taught courses on Sensors and Mechatronics at Stanford University. The “Introduction to Sensors” course is a broad overview of all sensing technologies, from thermometers, to inertial sensors, ultrasound devices, flow sensors, optical and IR sensors, chemical sensors, microphones, pressure sensors, and many others, and has included sensors based on changes in capacitance, resistance, piezoelectricity. I first taught this course at Stanford in the Spring of 1994, and I offered this course at least annually until 2016, when my duties as Senior Associate Dean made this impractical, yet have continued to offer this course periodically since, including last year.

11. The “Introduction to Mechatronics” course is a review of the mechanical, electrical and computing technologies necessary to build systems with these contents, which include everything from cars and robots to cellphones and other consumer electronics devices. In this class, we routinely use IR, LEDs, ultrasound sensors, and photosensors as a way of detecting proximity to objects in the space around miniature robots. We also use inertial sensors to detect movement, and a number of sensors, such as encoders to measure changes in position and

trajectory. I was one of the instructors for the first offering of this course in 1995, and this course has been offered at least once each year ever since, except for the pandemic year of 2021. The 2026 offering was highly successful with 80 undergraduate and graduate students from many engineering and science disciplines.

12. I am co-author of a textbook titled “Introduction to Mechatronic Design,” which broadly covers the topic of integration of mechanical, electronic and computer systems design into “smart products.” This textbook includes chapters on Microprocessors, Programming Languages, Software Design, Electronics, Sensors, Signal Conditioning, and Motors, as well as topics such as Project Management, Troubleshooting, and Synthesis.

13. My research group at Stanford has focused on the area of microsensors and microfabrication—a domain in which we design and build micromechanical sensors using silicon microfabrication technologies. The various applications for these technologies are numerous.

14. I have advised 75 Ph.D. students that have completed Ph.D. degrees and many more M.S. and B.S. students in Engineering during my time at Stanford.

15. I have published over 250 technical papers in refereed journals and conferences in the field of sensors, MEMS, and measurements. I have further

presented numerous conference abstracts, posters, and talks in my field. I am a named inventor on 50 patents in my areas of work.

16. From 2020 to 2022 I served as CEO of Applaud Medical (now Avvio Medical), a startup that I co-founded in 2015. Avvio is developing improved methods for ultrasonic treatment of kidney stones, and during my time as CEO, we initiated a FDA-regulated pivotal clinical trial on our first product, concluded an Australian clinical study on our second product, and positioned the company for on-boarding of an experienced CEO with resources to guide the company through all remaining trials and to a successful outcome.

17. I received the Office of the Secretary of Defense Award for Exceptional Public Service in 2010, the IEEE Sensors Council Technical Achievement Award in 2011, and was named Fellow of the ASME in 2014. I was awarded the 2018 IEEE Daniel Noble Award for Emerging Technologies. In 2022, I was elected to the National Academy of Engineering.

18. I have previously served as an expert on a patent infringement case involving the mounting and use of pressure sensors on guidewire catheters for cardiovascular procedures that included a number of sensing aspects, such as recording static and dynamic pressure signals, and compensating for electrical and mechanical errors. I have also previously served as an expert on a patent infringement case involving the design and use of miniature inertial sensors. That

case involved the design and operations of micromechanical sensors, and particularly the use of inertial sensors for detection of states of movement and rest. I have also served as an expert in a patent infringement case involving the use of sensors on athletic shoes for determining athletic performance. More recently, I served as an expert in a patent infringement case involving optical proximity sensors in smartphones. I also served as an expert witness in an IPR proceeding describing the use of microphones and signal processing circuits for processing and cancellation of noise in wearable electronic devices. My CV includes a full listing of recent cases in which I have testified at deposition or trial in the preceding several years.

III. UNDERSTANDING OF GOVERNING LAW

19. I understand that statutory and judicially created standards must be considered to determine the validity of a patent claim. I am not an attorney and, consequently, will offer no opinion on the law itself. My understanding of the pertinent law is described in this section and is the result of explanations provided by counsel. I have applied this understanding in my analysis.

20. I understand that a patent claim is unpatentable if it is obvious in view of the prior art. I further understand that the frame of reference for determining whether a claim is obvious is from the perspective of a POSA at the time of the

invention. I have been asked to assume that the effective priority date is August 1, 2016. I have not been asked to determine whether this date is appropriate.

21. In analyzing obviousness in light of the prior art I understand that it is important to understand the scope of the claims, the level of skill in the relevant art, the scope and content of the prior art, the differences between the prior art and the claims, and any objective indicia of non-obviousness (also called secondary considerations).

22. I understand that a patent claim is unpatentable for obviousness if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a POSA to which said subject matter pertains. I understand that obviousness may be based on one reference or a combination of references. I understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.

23. In determining the scope and content of the prior art, it is my understanding that a reference is considered appropriate (e.g., analogous) prior art if it falls within the field of the inventor's endeavor. In addition, a reference is prior art if it is reasonably pertinent to the particular problem with which the inventor was involved. A reference is reasonably pertinent if it logically would have commended itself to an inventor's attention in considering his problem. If a

reference relates to the same problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

24. To assess the differences between prior art and the claimed subject matter, it is my understanding that the law requires the claimed invention to be considered as a whole. This “as a whole” assessment requires showing that one of ordinary skill in the art at the time of invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would have selected the elements from the prior art and combined them in the claimed manner.

25. It is my understanding that something is “inherent in,” and therefore taught by, the prior art, if it necessarily flows from the explicit disclosure of the prior art. I understand that the fact that a certain result or characteristic may be present in the prior art is not sufficient to establish inherency. However, if the result or characteristic is necessarily present based upon the explicit disclosure in the prior art, it is inherent in the prior art and is therefore disclosed.

26. I understand that when a patented invention is a combination of known elements, the Board must determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue by considering the teachings of prior art references, the effects of demands known to people working in the field or present in the marketplace, and the background knowledge possessed by a POSA.

27. I have been informed that the Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of the claimed subject matter. I understand that several of these rationales are: (1) combining prior art elements according to known methods to yield predictable results; (2) simple substitution of one known element for another to obtain predictable results; (3) use of a known technique to improve a similar device (method or product) in the same way; (4) applying a known technique to a known device (method or product) ready for improvement to yield predictable results; (5) choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and (6) some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

28. I understand that in order to prove that a claimed invention is not patentable for obviousness, a petitioner must (1) identify the differences between the claim and particular disclosures in the prior art references, singly or in combination, (2) specifically explain how the prior art references could have been combined in order to arrive at the subject matter of the claimed invention, and (3) specifically explain why a POSA would have had reasons to so combine the prior art references.

IV. MATERIALS REVIEWED

29. The opinions contained in this declaration are based on the documents I reviewed, as well as my professional judgment, education, experience, and knowledge regarding sensors, sensor arrays, digital signal processing, beamforming, oversampled analog-to-digital conversion, digital delay, filtering, and decimation.

30. In forming my opinions expressed in this declaration, I reviewed the following materials:

Exhibit No.	Description
1001	U.S. Patent No. 11,082,055 to Fan et al. (“’055 patent”)
1002	File History of U.S. Patent No. 11,082,055
1005	U.S. Patent App. Pub. No. 2014/0270247 (“Swanson”)
1006	European Patent App. Pub. No. 1,744,174 (“Moquin”)
1007	U.S. Patent App. Pub. No. 2007/0229336 (“Liu”)
1008	U.S. Patent No. 6,339,647 (“Andersen”)
1009	U.S. Patent No. 5,461,389 (“Dean”)
1010	U.S. Patent No. 5,203,335 (“Noujaim”)
1011	U.S. Patent No. 6,539,096 (“Sigwanz”)
1012	Tiete et al., <i>SoundCompass: A Distributed MEMS Microphone Array-Based Sensor for Sound Source Localization</i> , 14 Sensors 1918 (2014), available at https://www.mdpi.com/1424-8220/14/2/1918 .

Exhibit No.	Description
1013	Excerpts from Microsoft Computer Dictionary, Fifth Edition, 2002
1014	Rudolf F. Graf, Excerpts from Modern Dictionary of Electronics Seventh Edition, 1999
1015	M. Brandstein and D. Ward, Eds., <i>Microphone Arrays: Signal Processing Techniques and Applications</i> . Berlin, Germany: Springer-Verlag, 2001 (“Brandstein-Ward”)
1016	R. Kneipfer, Sonar Beamforming – An Overview of Its History and Status, NUWC-NL Technical Report, 10,003, 7 April 1992 (“Kneipfer”)
1017	Gannot, Sharon, and Israel Cohen. “Adaptive Beamforming and Postfiltering.” <i>Springer Handbook of Speech Processing</i> , edited by Jacob Benesty, M. Mohan Sondhi, and Yiteng Huang, Springer Berlin Heidelberg, 2008, pp. 945–978 (“Gannot-Cohen”)
1018	B. Van Veen, “Beamforming: A Versatile Approach to Spatial Filtering,” in <i>IEEE ASSP Magazine</i> , vol. 5, no. 2, pp. 4-24, April 1988 (“Van Veen”)
1019	S. R. Freeman et al., “Delta-sigma oversampled ultrasound beamformer with dynamic delays,” in <i>IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control</i> , vol. 46, no. 2, pp. 320-332, March 1999
1020	C.I.C Nilsen et al., “Distortion-Free Delta-Sigma Beamforming,” in <i>IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control</i> , vol. 55, no. 8, pp. 1719-1728, 2008
1021	L. Milic et al., Multirate Filters: An Overview, <i>APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems</i> , Singapore, 2006, pp. 912-915
1022	G. Moon et al., Design Approach for Decimation Filter for ADC Application, in <i>Int’l J. of Eng. Trends and Techn. (IJETT)</i> , vol. 10 no. 12 (2014)

Exhibit No.	Description
1023	J. Yu et al., A low-power multi-bit $\Sigma\Delta$ modulator in 90-nm digital CMOS without DEM, in <i>IEEE Journal of Solid-State Circuits</i> , vol. 40, no. 12, pp. 2428-2436, Dec. 2005
1024	M. Mano et al., Logic and Computer Design Fundamentals, Prentice-Hall, 1997 (selected excerpts)
1025	U.S. Patent App. Pub. No. 2015/0049578 (“Hector”)

31. I also considered any other documents and materials I refer to in this declaration.

32. My opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a POSA would have understood the state of the art, the prior art, and the claims and the specification of the '055 patent at the time of the alleged invention, which I discuss below.

33. I have been asked to assume that the time of the alleged invention of the '055 patent was no later than August 1, 2016, which I understand is the earliest claimed priority date asserted for the '055 patent.

34. Based on my experience and expertise, it is my opinion that certain references disclose or would have suggested to a POSA all the features recited in the challenged claims of the '055 patent, as I discuss in detail below.

V. PERSON OF ORDINARY SKILL IN THE ART

35. I understand that in determining the level of ordinary skill in the art, several factors are considered. Those factors may include: (i) the type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) the rapidity with which innovations are made; (iv) the sophistication of the technology; and (v) the educational level of active workers in the field. A POSA must have the capability of understanding the scientific and engineering principles applicable to the pertinent art.

36. I am familiar with the level of ordinary skill in the art regarding the '055 patent as of around August 1, 2016. Considering the '055 patent, the technology, the educational level and experience of workers in the field relating to the patent, and problems and solutions in that field, and drawing on my own experience, I believe a person of ordinary skill in the art at the time of the alleged invention (around August 1, 2016) (which I refer herein as "POSA") would have had at least a bachelor's degree in physics, electrical engineering, computer engineering, or a similar technical field, and at least two years of experience designing or implementing digital signal-processing systems for sensors or sensor arrays. Work experience could substitute for formal education and additional formal education could substitute for work experience.

37. My opinions in this declaration regarding the '055 patent and the prior art (including the state of the art) are from the perspective of one of ordinary skill in the art as I defined above, during the relevant timeframe including the '055 patent's earliest claimed priority date of August 1, 2016.

38. I can make this assessment because, before and around August 1, 2016, I was familiar with the design and implementation of sensor systems, sensor arrays, digital signal-processing systems, analog-to-digital conversion, filtering, and related signal-processing techniques. Through my teaching, research, and work with students and engineers, I was familiar with what engineers and researchers in this field would have known and been able to implement at that time.

39. As discussed below, it is my opinion that claims 1-10 of the '055 patent are rendered obvious in view of the prior art discussed below. It is also my opinion that the claims would have been obvious from the perspective of a POSA under any reasonable definition of a POSA.

VI. TECHNICAL BACKGROUND

40. Below, I present a brief overview of certain features relating to those discussed and claimed in the '055 patent that were known to a POSA prior to and at the time of the earliest claimed priority date of the '055 patent. The features, techniques, and concepts I describe below in this Technical Background section reflect the knowledge of state of the art that a POSA would have had prior to and at

the time of the earliest claimed priority date of the '055 patent. I rely on, and incorporate as applicable (even if not expressly mentioned below), the following disclosures and opinions to support my opinions in this declaration, including those opinions relating to how the prior art discloses or would have suggested the challenged claims of the '055 patent and how and why a person of ordinary skill in the art would have been motivated to consider and combine the disclosures and suggestions from one or more prior art references as I explain below in §§X-XX.

41. The prior-art references and technical background discussed in this section provide factual support for my opinions regarding the state of the art as of the earliest claimed priority date of the '055 patent. They also provide support for my opinions regarding why a POSA would have been motivated to use, modify, and combine the teachings of the prior-art references discussed below, and why a POSA would have had a reasonable expectation of success in doing so. The references identified in this section are exemplary in nature and are not intended to limit the scope of the state of the art.

42. Claim 1 of the '055 patent recites:

1. A non-transitory computer-readable storage medium storing program code for causing a data processing system to perform steps comprising:
outputting a first oversampled digital signal output from an analog-to-digital converter (ADC), wherein the first oversampled digital signal is responsive to an analog field and the first oversampled digital signal is created at a sampling clock frequency;

delaying the first oversampled digital signal by a time delay wherein the time delay is equal to an integer number of sampling clock cycles to produce a time delayed first oversampled digital signal; and

combining the time delayed first oversampled digital signal with a second oversampled digital signal to obtain the beamformed digital signal, wherein the second oversampled digital signal is responsive to the analog field.

43. A POSA would have recognized all of these very familiar elements of this claim, which include a “storage medium”, “code”, “data processing system”, “ADC”, “oversampled digital signal”, “signal is responsive to an analog field”, “sampling clock frequency”, “time delay”, “time delayed...signal”, “integer number of sampling clock cycles”, “combining”, and “beamformed digital signal”, and would have appreciated that each and every term recited here had existed in the prior art long before the earliest claimed priority date of the '055 patent. Further, a POSA would have recognized that the combination of these terms in this claim, in which a signal is oversampled, delayed, and combined with a second oversampled signal to beamform, had existed in the prior art long before the earliest claimed priority date of the '055 patent.

A. Beamforming Generally

44. Beamforming, which is an established signal processing technique often described as spatial filtering, generally involves processing and preparing signals from multiple sensors to be combined so as to emphasize signals from a

desired location or direction. *See, e.g.*, Ex.1015 (M. Brandstein and D. Ward, Eds., *Microphone Arrays: Signal Processing Techniques and Applications*. Berlin, Germany: Springer-Verlag, 2001) (hereafter, “Brandstein-Ward”), p. 102 (“Beamforming is a technique which extracts the desired signal contaminated by interference based on directivity, i.e. spatial signal selectivity. This extraction is performed by processing the signals obtained by multiple sensors such as microphones, antennas, and sonar transducers located at different positions in the space. **The principle of beamforming has been known for a long time.**”) (internal citations omitted) (emphasis added).

45. Beamforming has been around for nearly a century, long before the ’055 patent. For example, beamforming was used in sonar applications as far back as the 1940s when single beam beamforming systems were used in World War II (“WWII”) for detection of submarines. *See, e.g.*, Ex.1016 (R. Kneipfer, Sonar Beamforming – An Overview of Its History and Status, NUWC-NL Technical Report, 10,003, 7 April 1992) at p. 10-15. At that time, submarines were outfitted with sonar equipment utilizing rotatable horizontal line hydrophones (e.g., sensors). During WWII, German engineers developed a way to change the time delays applied to the hydrophone outputs. *See id.*, pp. 13-14 (discussing German development of “compensator system”), Fig.9. This time delay capability allowed sonar operators to manually scan a beam without moving the sensor array, and

accordingly to adjust the steer direction of the beamformer, thus allowing the operators to scan the beam in any direction. *Id.*, pp. 13-14. Here, all the way back to the 1940s, more than seven decades before the 2016 priority date, we see an example of a system capable of analog “delay and sum beamforming.”

46. Beamforming in other areas, such as radar, communications, imaging, geophysical and astrophysical exploration, and biomedical applications, became well known in the decades since, as well as long before the '055 patent. *See* Ex.1018 (B. Van Veen, Beamforming: A Versatile Approach to Spatial Filtering, in *IEEE ASSP Magazine*, vol. 5, no. 2, pp. 4-24, April 1988) (hereafter, “Van Veen”), p. 2, Table 1.1; *see also* Brandstein-Ward, p. 102.

47. Beamforming including microphone array processing was adopted by the speech community by the mid-1980s. *See, e.g.*, Ex.1017 (Gannot, Sharon, and Israel Cohen. “Adaptive Beamforming and Postfiltering.” *Springer Handbook of Speech Processing*, edited by Jacob Benesty, M. Mohan Sondhi, and Yiteng Huang, Springer Berlin Heidelberg, 2008, pp. 945–978) (hereafter, “Gannot-Cohen”), p. 2 (“Over the last four decades, array processing has become a well-established discipline, *see e.g.*, [47.1-14]. In the mid 1980s, array processing and beamforming methods were adopted by the speech community to deal with data received by microphone arrays.”); Van Veen, p. 2-3 (“Papers devoted to beamforming are often found in the IEEE Transactions on: *Antennas and Propagation, Acoustics, Speech,*

and Signal Processing, Aerospace and Electronic Systems, and in the *Journal of the Acoustical Society of America*. There is a vast body of literature on various aspects of beamforming and we can only reference a subset in support of our discussions.”).

B. Delay-and-Sum Beamforming

48. The delay-and-sum beamformer is often considered the simplest of the beamforming structures. *See, e.g.*, Gannot-Cohen, p. 2 (“The simplest structure is the delay-and-sum beamformer, which compensates for the relative delay between distinct microphone signals and then sums the steered signal to form a single output.”); Brandstein-Ward, p. 297 (“the most basic beamforming method, the delay-and-sum beamformer”); Ex.1006, [0002] (“The simplest filtering technique is the ubiquitous ‘delay and sum’ beamformer which sums the inputs together with an appropriate delay to obtain a desired beamshape and direction.”). The underlying principle of the delay-and-sum beamformer is to compensate for the propagation delay differences from a single source to each of the sensors in an array. Because a signal arriving from a specific angle or direction reaches different sensors at different times, the individual sensor outputs need to be relatively delayed in order to align them coherently before they are summed together.

49. Kneipfer and Van Veen both describe applications and examples of beamforming dating back many decades. The earlier implementations relied on analog signal conditioning, delay lines and other now-obsolete components to

provide beamforming, but the basic concept of “delay and sum” was very well established many years before the '055 patent. With the advent of the modern microprocessor and A/D converters, analog delay and sum beamforming became digital delay and sum beamforming.

50. For a digital implementation of a delay-and-sum beamformer, each sensor's analog output is first converted to a digital signal by an analog-to-digital converter (ADC). The digitized sensor signals may be delayed by an integer number of sample clock cycles and summed to produce the beamformed output. *See, e.g.,* Van Veen, pp. 3-4 (“Each sensor is assumed to have any necessary receiver electronics and an A/D converter if beamforming is performed digitally.”), Fig 2.2; Ex.1006, [0012] (“In digital systems, the delay can only take on values that are integer multiples of the sample time ($1/F_s$).”). The delay resolution and the steering precision of the beamformer is governed by the sampling rate. *See id.* A higher sampling rate yields finer delay resolution and more precise beam steering. Overall, the adoption of A/D converters and subsequent digital implementations of delays, filters and summers began decades ago, coincident with the emergence of microprocessors and the recognition that digital delays, digital filters, and digital combiners were available, efficient, inexpensive, adaptable, and powerful, and were a perfect upgrade to beamforming. This opportunity was recognized by Van Veen in 1988, almost 30 years prior to the earliest claimed priority date of the '055 patent,

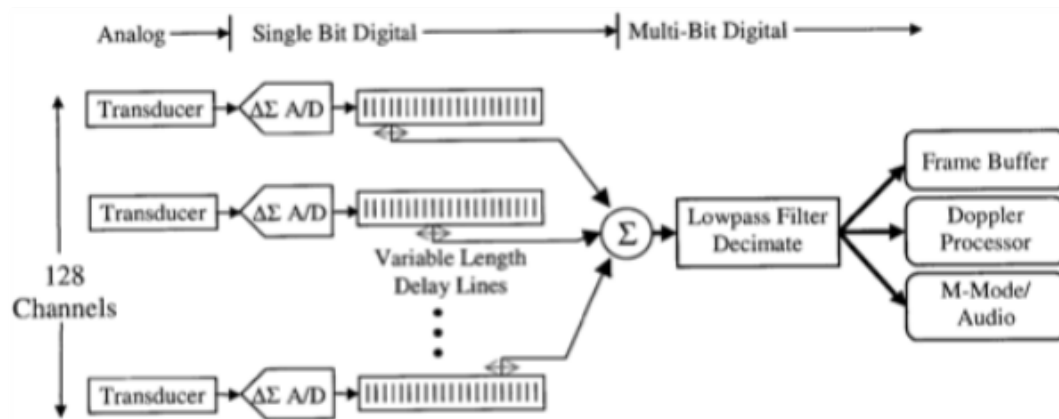
and work on modifications to digital delay and sum beamformers, including combinations and re-ordering of computational steps, has been underway throughout the time since Van Veen.

C. Beamforming Using Oversampled Digital Signals

51. Digital beamforming using oversampled analog-to-digital converters has also been around for decades, long before the '055 patent. *See, e.g.,* Ex.1019 (S. R. Freeman *et al.*, “Delta-sigma oversampled ultrasound beamformer with dynamic delays,” in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 46, no. 2, pp. 320-332, March 1999) (“Freeman”), Title, p. 1 (“digital beamforming is well established”), p. 1 (“In the late 1980s, advances in analog-to-digital conversion led many manufacturers to perform more beamformer processing digitally.”), p. 2; Exs.1006-1009.

52. One particularly efficient oversampling analog-to-digital converter (ADC) that was well-known for use in digital beamforming is the delta-sigma (also called sigma-delta) modulator. *See, e.g.,* Freeman, p. 2. A delta-sigma modulator uses one or more integration stages within a feedback loop such that a two-level, single-bit quantizer output tracks the average of the analog input, thus shaping quantization noise to higher frequencies outside the signal band where it can be rejected by a subsequent low-pass filter and decimation stage. *See id.*, pp. 2-3, Fig.1. A delta-sigma ADC may sample at a rate far exceeding the Nyquist rate of

the input signal, and is often called the oversampling rate. Its high-rate single-bit output stream enables accurate and fine-tuned beamforming delays to be implemented by manipulating individual samples using a variable-length shift register, without the need for complex interpolation or baseband circuitry. *See id.*, pp. 4-6, Fig. 3; Ex.1006, [0014]-[0016], Fig.4. As explained by Freeman, “...accurate delays can be achieved simply by manipulating individual samples at the high sampling rate. The complicated basebanding or interpolate/decimate circuits may be replaced by a variable length shift register determining the delay of the signal prior to summation...” Ex.1019, 5.



53. Freeman illustrates this process for digital oversampling and precision delay and sum in Figure 3, shown above. Here, the signal from the “Transducer” is converted to a single-bit digital data stream using a delta-sigma oversampling A/D converter. These signal streams pass through a variable length delay line, which transfers the signal through the line at the oversampled sample rate, and

selects data at taps corresponding to an integer number of sample intervals. These extracted signals are delayed by integer numbers of elements in the sample stream, which are sampled at the oversampling rate, and therefore the resulting delays represent integer multiples of the oversampling interval. The delayed single-bit outputs from each channel are summed across the array to form the beamformed signal, and a low-pass filter and decimator then converts the oversampled beamformed output to a conventional lower-rate digital signal. *See, e.g., Freeman, pp. 5-6, Fig.3; Ex.1006, [0014]-[0016].* The use of delta-sigma modulators in oversampled delay-and-sum beamforming was thus well-known in the art for decades before the '055 patent. *See, e.g., Freeman, Fig.3; Ex.1006, Abstract, [0002], [0014]-[0016], Fig.4; see also Exs. 1007-1009.*

54. So, by 1999, more than 16 years before the earliest claimed priority date of the '055 patent, there were already demonstrations of delay and sum beamforming of acoustic signals, including oversampling A/D converters, digital delays at integer multiples of the sampling interval, and combining to form a digitally beamformed signal.

55. Of course, there are many options for the sequencing of the processing of the oversampled digital signal. For example, Nilsen (Ex.1020, C.I.C Nilsen et al., "Distortion-Free Delta-Sigma Beamforming", in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 55, no. 8, pp. 1719-1728,

2008) describes beamforming implementations with oversampling followed by filtering, delaying, decimating and then combining. As explained by Nilsen, “Down-sampling to the Nyquist rate should not take place until after the delays have been applied, to achieve maximum resolution in time and a suitably low degree of delay quantization.” Ex.1020, 4. In this description of the Figure 3 embodiment shown below, digital delays are implemented on the oversampled signal by adding delays equal to an integer multiple of the oversampling interval. *Id.*

56. A key point in all of this is that there were more than 80 years of intense interest in beamforming of analog signals, first in sonar and radar, then in ultrasound imaging, and more recently for operation of audio signal processing in consumer electronic devices. Each of these application domains was deemed of critical importance at various times, and so there was substantial investment across academia, military, medical and consumer electronics sectors, and as a result, a lengthy historical record of innovation in which new ideas and concepts from all sectors were applied quickly and comprehensively. A POSA would have

appreciated that the challenged claims of the '055 patent simply present the well-known elements of these prior art systems, all performing well-known functions in a variety of arrangements that have all also been disclosed in the prior art. In particular, a POSA would recognize that the combination of these terms in claim 1, in which a signal is oversampled, delayed, and combined with a second oversampled signal to beamform, has existed in the prior art since long before the earliest claimed priority date of the '055 patent. A POSA would also recognize that claims 2-10 represent ordinary rearrangements of the elements described above, along with the addition of some other elements such as filters and decimators that were all also well-known and widely used in beamforming systems long before the earliest claimed priority date of the '055 patent. A POSA would appreciate that this subject matter was well-established and well-known long before the '055 patent. Simply put, the challenged claims of the '055 patent add no novelty to the known state of the art that existed many years before the earliest claimed priority date of the '055 patent.

57. By August 1, 2016, a POSA would also have understood that digital signal-processing operations, including delaying and combining digital samples as part of beamforming, could be implemented in hardware, software, firmware, or combinations of these approaches. *See e.g.*, Ex.1005, [0008]-[0024], [0054]-[0056], claims 1-20; Ex.1025, Abstract, [0016]-[0017], [0062], [0064], [0066]-

[0068], claims 1-30. A POSA would have understood that software or firmware implementations conventionally stored instructions or code in non-transitory memory for execution by a processor, microprocessor, digital signal processor, or other data-processing system. In my opinion, storing code for causing a processor or DSP to perform known digital signal-processing operations was a conventional implementation choice, and a POSA would not have regarded the mere use of a non-transitory computer-readable storage medium for such code as a technological advance separate from the underlying signal-processing operations.

VII. THE '055 PATENT

A. Description

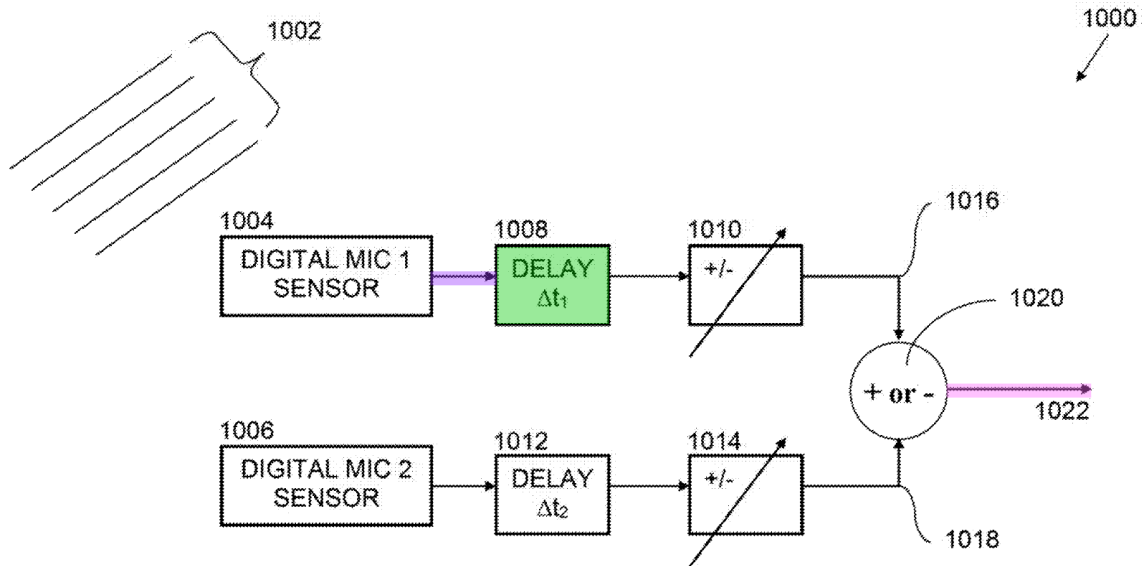
58. The '055 patent is titled “Beamforming Using Fractional Time Delay in Digitally Oversampled Sensor Systems, Apparatuses, and Methods.” Ex.1001, Title. It cites a number of related patent applications for priority, with the earliest claimed priority date being August 1, 2016.

59. The '055 patent states in its background: “Field quantities which exist in the natural world are generally analog signals which have continuously varying amplitude as a function of time. Examples of these field quantities are sound pressure, vibration, light, etc. Measurement of a field quantity is accomplished with an analog sensor or a digital sensor. Digital electronics work with digital signals. Interfacing analog signals with digital electronics presents a technical problem for

which a technical solution using technical means is needed.” Ex.1001, 1:30-39. This statement of the background overlooks that the “technical problem” of interfacing analog and digital electronics has existed since the advent of digital electronics more than 50 years ago, and further overlooks 40 years of the development of technical solutions using technical means.

60. The '055 patent's specification describes applying a time delay to an oversampled digital signal from a sensor, such as a digital microphone, before or within the signal-processing path that later performs low-pass filtering and decimation. *Id.*, 2:43-48, 3:1-31, 3:55-65. The patent explains that, when delay is applied in the oversampled domain, the delay is represented by an integer number of high-rate sampling-clock cycles. *Id.*, 3:28-31, 4:50-65, 13:42-58.

61. Figure 10 of the '055 patent illustrates two digital microphone sensors. *Id.*, Fig. 10. Each sensor receives an analog field, outputs an oversampled digital signal (purple), applies a time delay to those signals using a delay element (green), and then provides the resulting signal to an arithmetic block that provides the beamformed output (pink). *Id.*, 13:16-40. As discussed above and below, every single element of this exemplary system, and complete instances of this exemplary system as well as other exemplary systems presented and covered by the claims of the '055 patent, all existed in the art for many years prior to the earliest claimed priority date of the '055 patent.



Id., Fig.10.²

62. Independent claim 1 recites that same structure in computer-readable-medium form. It requires program code for causing a data-processing system to: output a first oversampled digital signal from an analog-to-digital converter; delay that signal by an integer number of sampling-clock cycles; and combine the delayed first oversampled digital signal with a second oversampled digital signal to obtain a beamformed digital signal. *Id.*, claim 1.

B. The Prosecution History

63. I reviewed the prosecution history of the '055 patent (Ex.1002). From that review, it is my understanding that during prosecution before the U.S. Patent and Trademark Office (Office), the Examiner allowed the challenged claims

² I have annotated figures in color throughout this declaration.

without rejecting them over prior art. Ex.1002, 211-216, 58, 53-55. The only rejections were non-prior art issues, namely, nonstatutory double patenting and lack of antecedent basis. *Id.*, 212-216.

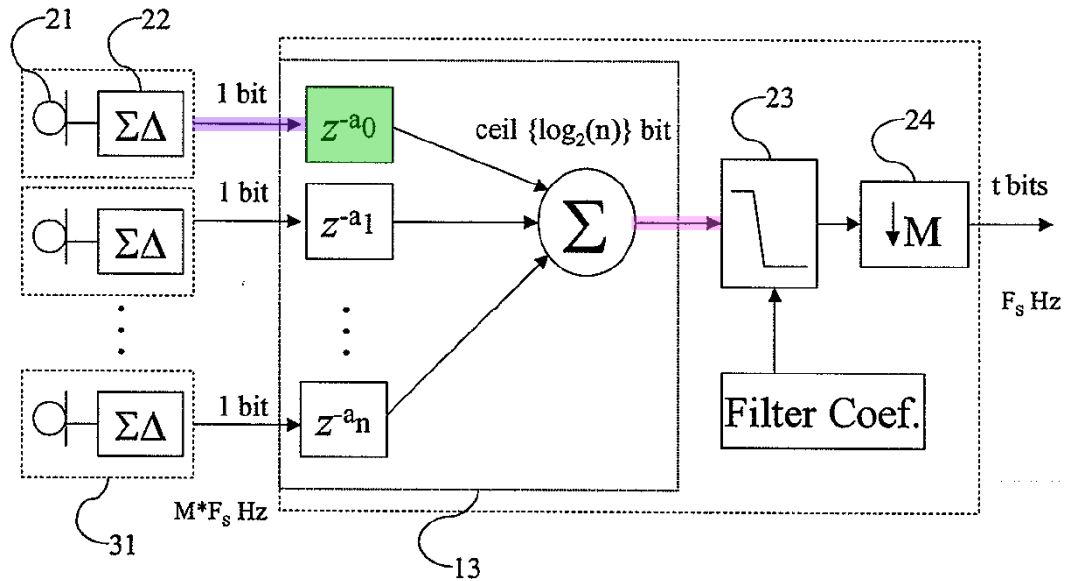
VIII. OVERVIEW OF THE PRIOR ART

A. Moquin (Ex.1006)

64. Moquin (European Patent Application Publication No. 1,744,174) published January 17, 2007, which is long before the earliest claimed priority date of the '055 patent (August 1, 2016). Moquin recognized that microphone arrays were well known in the art and were already widely used in conventional digital delay-and-sum beamformers. Ex.1006, [0002]. Moquin explained that such conventional beamformers had limited steering resolution because delay resolution was determined by the analog-to-digital sampling rate, which was generally limited to the Nyquist sampling rate. *Id.*, [0002]-[0006], [0012]. That said, Moquin recognized that oversampling delta-sigma type analog-to-digital converters existed. *Id.*, [0005] (“Most modern Analog-to-Digital converters (ADCs) are of the oversampling delta-sigma type.”).

65. Moquin’s solution was to use high-rate, one-bit outputs from delta-sigma digital microphones to produce a digital data stream that is an oversampled digital signal output. For example, as illustrated in Figure 4, Moquin discloses outputting an oversampled stream (purple) to a shift-register delay element (green),

selecting the appropriate tap to obtain the desired beamforming delay, and then summing the delayed output with other channels' delayed signals to form a beamformed signal (pink). *Id.*, [0014]. This system produces an oversampled and delayed digital signal output that has a time delay equal to an integer multiple of the sampling rate intervals. The oversampled and delayed signals are then combined to form an oversampled beamformed digital signal. The resulting sum is then filtered and decimated to a lower sample rate. *Id.*



Id., Fig.4.

66. Moquin also taught implementing the architecture in dedicated signal-processing hardware or a general-purpose signal processor. *Id.*, [0015]-[0016].

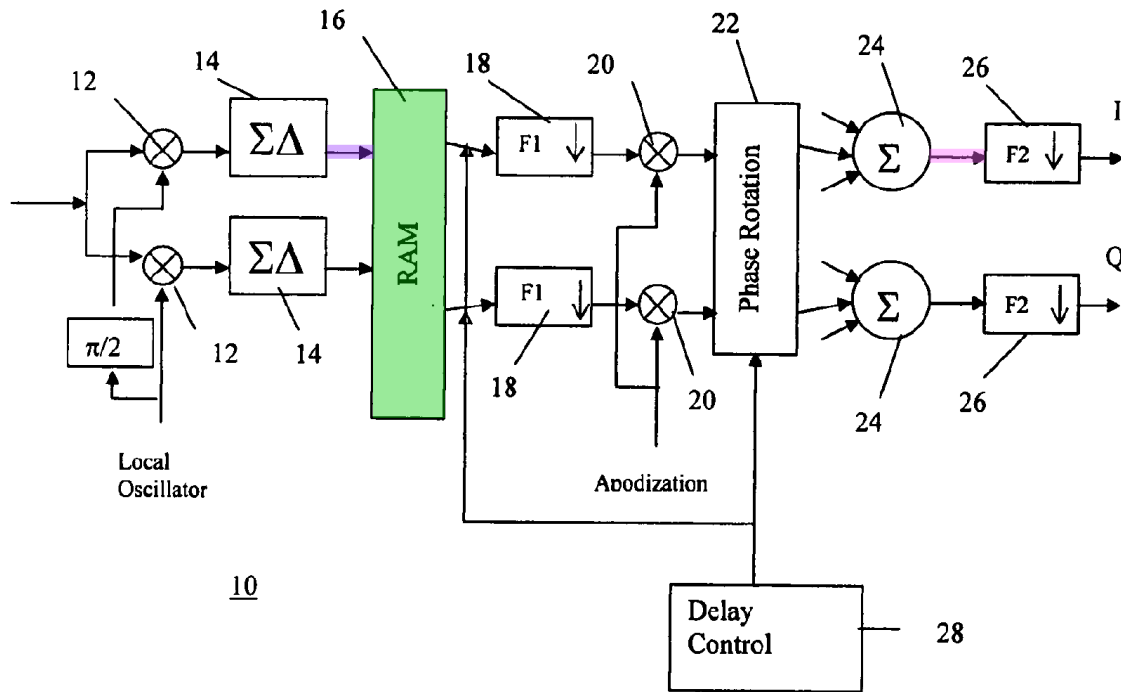
B. Liu (Ex.1007)

67. Liu (United States Patent Application Publication No. 2007/0229336) published October 4, 2007, which is well before the earliest claimed priority date

of the '055 patent (August 1, 2016). Liu likewise disclosed using oversampled receive-channel data for beamforming. *See, e.g.*, Ex.1007, [0002], [0006]. For example, in Liu's Figure 2 embodiment, each channel's received signal is digitized by an oversampling sigma-delta converter to output a one-bit stream (purple), stored in memory (green), and delayed by selecting data from the stored sample stream under control of a delay controller. This system produces an oversampled and delayed digital signal output that has a time delay equal to an integer multiple of the sampling rate intervals. *Id.*, [0006], [0025], [0029]-[0035], Fig.2 (annotated below). Liu then partially reconstructs the delayed channel data to an intermediate rate, sums the channel signals to form the beam (pink), and performs further reconstruction after summation. *Id.*, Abstract, [0006], [0035], [0038]-[0040], [0055]-[0057]. Therefore, Liu teaches a system in which downstream channel signals respectively derived from the delayed oversampled digital signal and a second oversampled digital signal are combined to form a beamformed digital signal.

68. Liu also taught a processor-based implementation of its teachings. For example, Liu discloses that its "system 10 for receive beamforming ultrasound information" and related methods may be implemented "using a processor." *Id.*, [0024] ("The system 10 is implemented on one or more integrated circuits.... Other

circuit implementations may be provided, such as ... using a processor,"); *see also, e.g., id.*, [0033]-[0034], [0036], [0038], [0048], [0059].

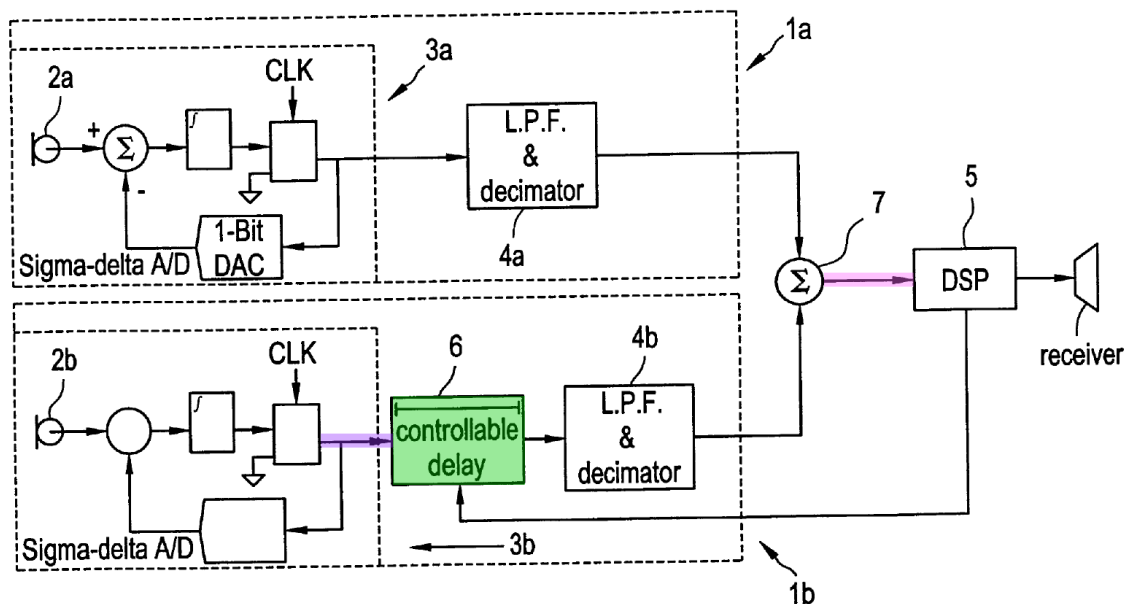


Id., Fig.2.

C. Andersen (Ex.1008)

69. Andersen (United States Patent No. 6,339,647) issued January 15, 2002, which is also well before the earliest claimed priority date of the '055 patent (August 1, 2016). Andersen disclosed a digital hearing aid with beamforming properties and at least two microphone channels. *See, e.g., Ex.1008*, 1:64-2:4. Each channel includes a sigma-delta analog-to-digital converter followed by a low-pass filter/decimator, which converts a high-clock-frequency one-bit stream (purple) into lower-rate digital words. *Id.*, Abstract, 2:5-14.

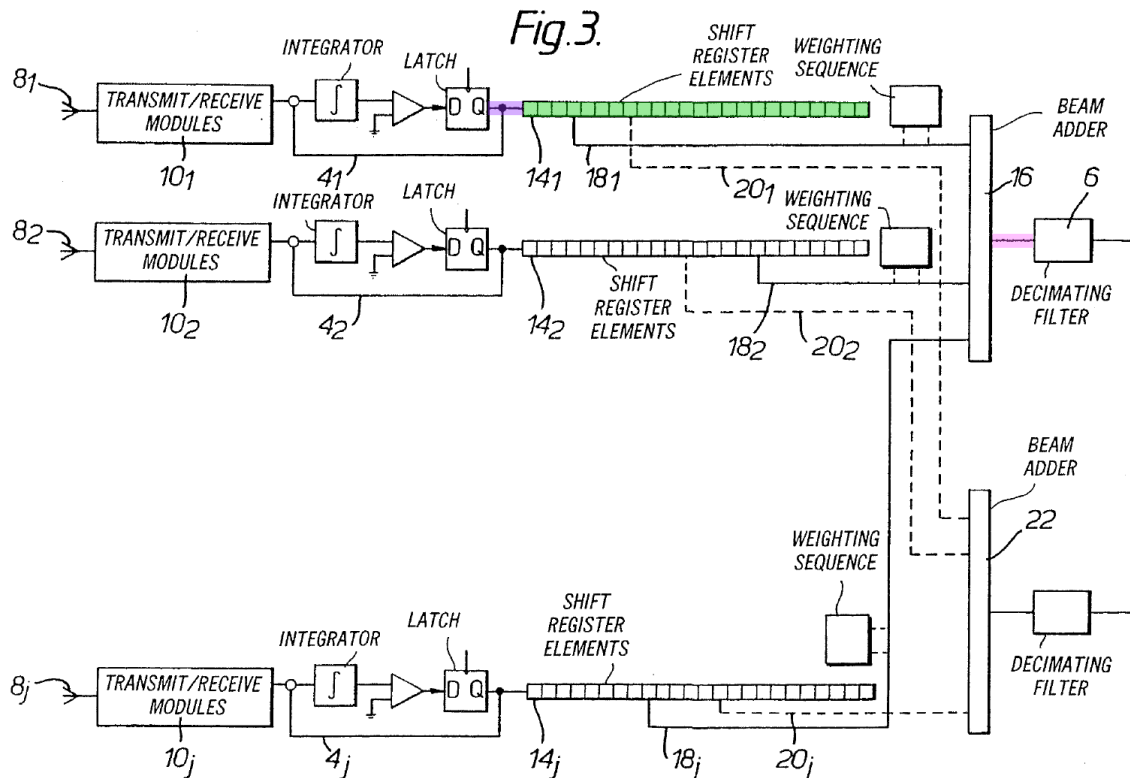
70. Andersen further disclosed a controllable delay (green) in the high-rate bitstream before the low-pass filter/decimator in order to obtain short beamforming delays without interpolation in the digital signal processor. *See, e.g., id.*, 1:21-57, 2:15-25. This system produces an oversampled and delayed digital signal that has a time delay equal to an integer multiple of the sampling rate intervals. As illustrated in Figure 3, the delayed and undelayed channel signals are filtered/decimated and then combined at a summing circuit 7 for downstream processing of the beamformed output (pink). *Id.*, 3:23-45. Therefore, Andersen teaches a system in which a delayed signal is then combined with an undelayed signal to form a beamformed digital signal.



Id., Fig.3.

D. Dean (Ex.1009)

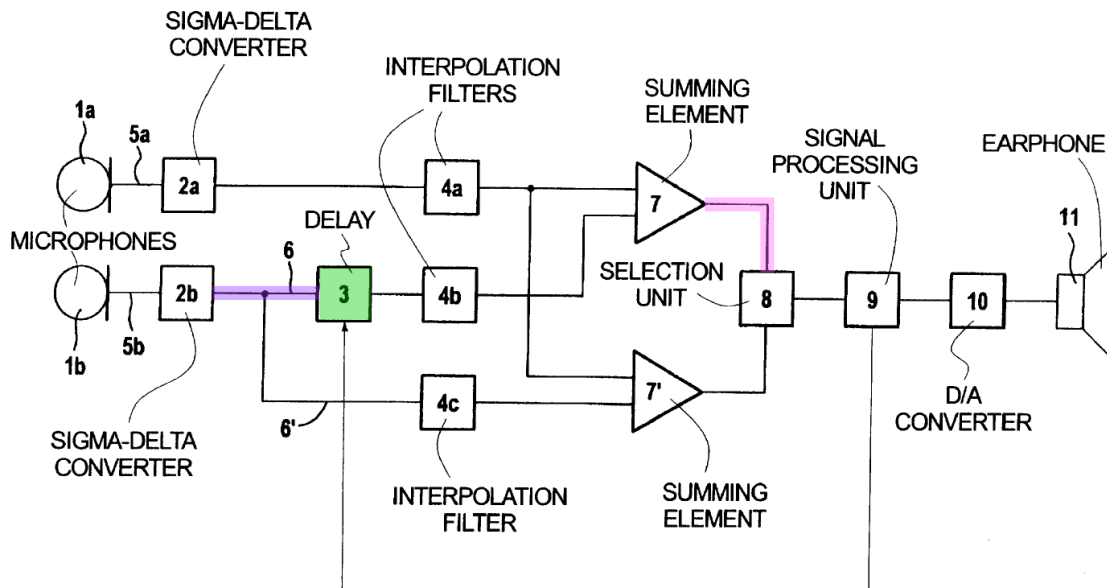
71. Dean (United States Patent No. 5,461,389) issued October 24, 1995, which is also well before the earliest claimed priority date of the '055 patent (August 1, 2016). Dean disclosed a digital beamforming array in which oversampled n-bit sensor signals are delayed using shift-register elements, combined by beam adders, and then decimated. Ex.1009, Abstract, 1:45-2:67.



Id., Fig.3. Dean's system produces an oversampled and delayed digital signal that has a time delay equal to an integer multiple of the sampling rate intervals. The oversampled and delayed signals are then combined to form a beamformed digital signal.

E. Sigwanz (Ex.1011)

72. Sigwanz (United States Patent No. 6,539,096) issued March 25, 2003, which is before the earliest claimed priority date of the '055 patent (August 1, 2016). Sigwanz disclosed microphone signals that are converted by sigma-delta analog-to-digital converters, a resulting one-bit signal is delayed, and delayed/undelayed signals are filtered and combined in summing elements. *See, e.g., Ex.1011, Abstract, 1:66-2:39, 2:65-3:29.*

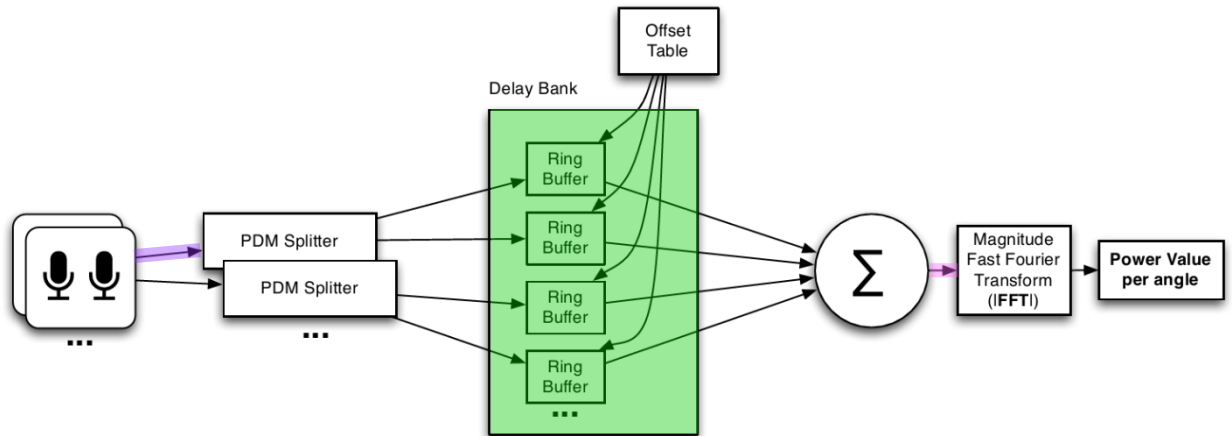


Id., Figure.

F. SoundCompass (Ex.1012)

73. Tiete et al., *SoundCompass: A Distributed MEMS Microphone Array-Based Sensor for Sound Source Localization*, 14 Sensors 1918 (2014), available at <https://www.mdpi.com/1424-8220/14/2/1918> (“SoundCompass”) was published in January 2014, which is before the earliest claimed priority date of the '055 patent

(August 1, 2016). SoundCompass disclosed a 52-microphone array, where one-bit microphone streams are delayed in a delay bank/ring buffer and then summed for beamforming. *See, e.g.*, Ex.1012, 6-8.



Id., Fig.4.

G. Noujaim (Ex.1010)

74. Noujaim (United States Patent No. 5,203,335) issued April 20, 1993, before the earliest claimed priority date of the '055 patent (August 1, 2016). Noujaim described ultrasonic beamforming in which sigma-delta modulators separately digitize transducer-element echo signals into oversampled one-bit digital representations. The oversampled one-bit representations are delayed as required for beam steering and focusing, summed together, and then provided to a decimator filter that reduces the sample rate of the digitized receive beam. Ex.1010, Abstract, 8:65-10:3, Fig.5.

H. Swanson (Ex.1005)

75. Swanson (United States Patent Application Publication No. 2014/0270247) published September 18, 2014, which is before the earliest claimed priority date of the '055 patent (August 1, 2016). Swanson disclosed a computer program product with code for receiving digital-microphone-array data, adjusting delay, combining the data, and beamforming. *See, e.g.*, Ex.1005, [0023]-[0024], claims 15, 18. Swanson also explained that, when the disclosed functions are implemented in firmware or software, the instructions/code may be stored on computer-readable media, including non-transitory computer-readable storage media, and executed by processors. *Id.*, [0054]-[0055].

I. Analogous Art

76. In my opinion, the asserted prior-art references discussed in this declaration are analogous art to the '055 patent. Swanson, Moquin, Liu, Andersen, Dean, and Noujaim are in the same field as the '055 patent because they concern digital signal processing for sampled sensor systems, including systems using oversampled ADC outputs, delay, combining, filtering, and decimation. They also are reasonably pertinent to problems addressed by the '055 patent, including implementing delay-based beamforming in digital sensor systems. I also consider Sigwanz and SoundCompass pertinent background art for the same reasons.

77. We see throughout these disclosures a variety of systems which produce an oversampled and delayed digital signal that has a time delay equal to an integer multiple of the sampling rate intervals. The oversampled and delayed signals are thus prepared for combination with other digital signals to form a beamformed digital signal. A POSA would appreciate that this subject matter was well-established and well-known long before the '055 patent.

IX. CLAIM CONSTRUCTION

78. It is my understanding that in determining whether a patent claim is obvious in view of the prior art, the Patent and Trademark Office construes the claim by giving the claim terms their plain and ordinary meaning, as they would have been understood by a POSA at the time of the invention in view of the intrinsic record (patent claims, patent specification, and file history). For the purposes of this review, and to the extent necessary, I have interpreted each claim term in accordance with its plain and ordinary meaning as it would have been understood by a person of ordinary skill in the art at the time of the alleged invention, in view of the intrinsic record.

79. I understand that a patent and its prosecution history are considered “intrinsic evidence” and are the most important sources for interpreting claim language in a patent. I also understand that in reading the claim, I must not import limitations from the specification into the claim terms; in other words, I must not

narrow the scope of the claim terms by implicitly adding disclosed limitations that have no express basis in the claims. The prosecution history of related patents and applications can also be relevant.

80. I understand that sources extrinsic to a patent and its prosecution history (such as dictionary definitions and technical publications) may also be used to help interpret the claim language, but that such extrinsic sources cannot be used to contradict the unambiguous meaning of the claim language that is evident from the intrinsic evidence.

81. Unless expressly stated herein, I have applied the plain and ordinary meaning of the claim terms, which I understand is the meaning that a POSA would have given to terms at the time of the claimed invention based on a review of the intrinsic evidence.

82. [RESERVED]

83. [RESERVED]

X. GROUND 1: CLAIMS 1-2, 4-5, AND 7-9 ARE OBVIOUS BASED ON MOQUIN AND SWANSON

84. In my opinion, a POSA would have found claims 1-2, 4-5, and 7-9 obvious based on Moquin in view of Swanson.

A. Motivation to Combine

85. In my opinion, a POSA implementing Moquin's digital signal processor (DSP)-based implementation of delay and sum beamforming would have

been motivated to further implement Swanson's teachings regarding storing code including instructions for controlling the operation of such DSP-based beamforming on a non-transitory computer-readable medium.

86. First, as described above in the Technical Background section, there were many well-known historical examples of digital systems for delay and sum beamforming of signals from microphone arrays, including use of microprocessors that include memory for storing code and are configured to execute such code, oversampled ADCs for converting analog signals to digital format, and digital signal processors for execution of filtering, delaying, decimating, and combining the signals from a microphone array. *See supra* §VI. A POSA at the time of the earliest claimed priority date of the '055 patent would have been well-aware of example uses of these elements, and the advantages of combining these elements in various ways. All elements of claims 1-10 were known long before the '055 patent.

87. A POSA would have been especially motivated to combine Moquin and Swanson because both references provide more modern and complete details concerning DSP-based beamforming, which would have reduced design effort and further confirmed a reasonable expectation of success. Moquin teaches an example of an implementation of an oversampled delay and sum beamforming system that operates within a general-purpose DSP. *See* Ex.1006, [0014]-[0016], claim 8. Swanson similarly teaches particular details of DSP-based beamforming systems—

more specifically, Swanson discloses a head-end chip, which “may be a processor, such as a digital signal processor (DSP)” (Ex.1005, [0005]), and that “may include a module 102C for data processing” such as for performing “beamform[ing].” *Id.*, [0035]-[0036], Fig.1. Further, Swanson provides details on the design and operation of the system for managing the digital data from the individual microphones to the DSP (*see id.*, [0047]-[0048]) and on construction of low-cost structures for housing and operating the elements of such a system. *Id.*, [0051]. All these implementation details would provide specific guidance to a POSA interested in constructing a system that uses oversampled digital data from a microphone array, provides filtering, delays, decimation and combining to produce a beamformed output.

88. Swanson further teaches a computer program product that comprises a non-transitory computer-readable medium with code for the aforementioned beamforming-related data processing on the DSP (head-end chip). Ex.1005, [0054]-[0055]; *see also id.*, [0023]-[0024], [0036], claim 15, claim 18. Even though a POSA would have already been motivated, in my opinion, to utilize a non-transitory computer-readable medium with code for a digital beamforming system without the disclosure of Swanson, a POSA would see the utility of these details from Swanson and would have been motivated to combine Swanson’s teachings regarding its computer program product including code (software) for causing

beamforming-related data processing by a DSP with Moquin's disclosed DSP-based beamforming-related implementation, including receiving digital microphone-array data and carrying out related array processing functions. The combination would have enabled a POSA to easily program and control Moquin's DSP-based beamforming-related implementation using code (software) stored on a non-transitory computer-readable medium. The software (code) implementation would have also provided the benefit of flexibility and facilitated the ability to amend or revise the beamforming-related processing more easily than if the implementation was hard wired into a fixed integrated circuit. This flexibility would have also resulted in reduced costs over time, as modifications to the beamforming-related processing could be implemented without manufacturing a new chip. That same flexibility would have motivated a POSA to use the stored-software implementation to program, update, or reuse Moquin's delay settings for different look directions, array geometries, or product configurations. Moquin explains that the selected delays determine the look direction, recognizes that phased arrays may employ different geometrical configurations, and states that its principles apply across different phased-array applications. *See* Ex.1006, [0009], [0012], [0014], [0017]; *see also* Ex.1005, [0010], [0023]-[0024], [0054]-[0055], claim 18. These benefits are in line with disclosure of the prior art. Ex.1006, [0016] (expressing that it may be "more expedient or economical" to "implement"

Moquin's "structure" in "a general-purpose DSP"). This same implementation would also have predictably fit Swanson's head-end/DSP architecture for processing digital-microphone-array data on a common platform, further motivating use of stored instructions for Moquin's disclosed DSP option in processor-based products. Ex.1005, [0005], [0009]-[0010], [0036], [0042], [0054]-[0055].

B. Reasonable Expectation of Success

89. In my opinion, a POSA would have had a reasonable expectation of success in combining Moquin and Swanson.

90. First, the combination of Moquin and Swanson applies the implementation of Moquin's known DSP-based beamformer with Swanson's known software/storage medium implementation without changing Moquin's underlying oversampled delay-and-sum beamforming operation.

91. Second, both Moquin and Swanson are specifically directed to digital signal processor (DSP)-based implementations of beamforming and provide details that are relevant to achieving modern implementations of the well-known delay and sum approaches used long before the time of the earliest claimed priority date of the '055 patent. More specifically, Moquin discloses that its beamformer arrangement may be implemented in a general-purpose digital signal processor (DSP) to process oversampled signals from audio microphones. *See, e.g.*, Ex.1006,

[0016], claim 8. Swanson similarly discloses that beamforming functions “implemented in firmware and/or software” and “stored as one or more instructions or code on a computer-readable medium,” including “non-transitory computer-readable storage media” are used to “cause one or more processors,” such as a DSP, to implement beamforming-related functions. Ex.1005, [0005], [0054]-[0055]; *see also id.*, [0023]-[0024].

92. The proposed modification presents nothing more than a predictable application of a known software storage implementation (as taught by Swanson) to a known digital signal processing based system (as taught by Moquin) according to their established functions.

C. Claim 1

93. In my opinion, claim 1 is directed to a non-transitory computer-readable medium storing program code for causing a data processing system to perform beamforming using oversampled digital sensor signals.

94. It is my opinion that Moquin is directed to beamforming using oversampled digital signals, including disclosing the claimed oversampled signal-generation, delay, and combining operations. As discussed above in the Technical Background and Overview of the Prior Art sections of this declaration, all elements of this claim have existed and been in use separately and together for many functions, including to form beamformed digital signals. *Supra* §§VI, VIII.

95. It is also my opinion that Swanson discloses a computer program product that comprises a non-transitory computer-readable medium with code for performing beamforming-related data processing. Thus, it is my opinion that considering Moquin in view of Swanson, a POSA would have been motivated to implement Moquin's oversampled beamforming technique in software and/or firmware, such as program code stored on a non-transitory computer-readable medium, thereby rendering claim 1 obvious.

1. 1[pre]: “A non-transitory computer-readable storage medium storing program code for causing a data processing system to perform steps comprising:”

96. I have been asked to assume that the preamble of claim 1 is limiting. Under that assumption, it is my opinion that examples of a “...non-transitory computer-readable storage medium storing program code for causing a data processing system to perform steps” existed in known prior art for many years prior to the earliest claimed priority date of the '055 patent's claims. *See e.g.*, Ex.1005, [0054]-[0056], claims 15-20; Ex.1025, [0016]-[0017], [0062], [0064], [0066]-[0068], claims 25-30. In particular, it is my opinion that Moquin in view of Swanson renders obvious the preamble of claim 1, 1[pre].

97. Before turning to the prior art disclosure, it is my opinion, having reviewed the '055 patent, that the '055 patent does not describe any unique or special technology for claim 1's storage-medium aspect. In fact, the '055 patent

does not mention any particular “computer readable storage medium” for implementing its alleged invention until the latter columns of the patent, where the patent recites the following, for example:

“An apparatus for performing the operations herein can implement the present invention. This apparatus may be specially constructed for the required purposes, or it may comprise a general-purpose computer, selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a computer readable storage medium, such as, but not limited to, any type of disk including floppy disks, hard disks, optical disks, compact disk read-only memories (CD-ROMs), and magnetic-optical disks, read-only memories (ROMs), random access memories (RAMs), electrically programmable read-only memories (EPROM)s, electrically erasable programmable read-only memories (EEPROMs), FLASH memories, magnetic or optical cards, etc., or any type of media suitable for storing electronic instructions either local to the computer or remote to the computer.”

Ex.1001, 17:62-18:10.

98. The '055 patent also recites the following:

“Non-transitory machine-readable media is understood to include any mechanism for storing information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium, synonymously referred to as a computer-readable medium, includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; except electrical, optical, acoustical or other forms of transmitting information via propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.”

Ex.1001, 19:4-14.

99. As demonstrated by the above excerpts, the '055 patent discusses software implementation and machine-readable media in generic, conventional terms, citing as possibilities many known combinations of well-known elements performing expected and well-known functions.

100. In my opinion, the '055 patent's disclosure confirms that the alleged improvement of claim 1 is not limited to or dependent on any particular storage-medium implementation. A POSA would appreciate that the underlying signal-processing operations, which Moquin discloses and which Swanson teaches, could be implemented in the broad range of combinations of firmware/software on non-transitory media, consistent with the generic list of components and combinations recited in the '055 patent.

101. Turning to the prior art's disclosure of claim 1, it is my opinion that Moquin discloses claim 1's recited signal-processing steps. Moquin describes a phased-array beamformer having multiple sensors arranged in an array, samplers generating oversampled digital signals, and a beamformer that delays and sums the oversampled digital signals to generate a beamformed output, with the beamforming performed at the oversampling frequency. *See* Ex.1006 at Title, Abstract, [0014]-[0016], Fig.4, claim 1. For example, Moquin teaches:

“Figure 4 shows an embodiment of the present invention. In contrast with the prior art arrangement of Figure 3, the delay and sum beamformer 13 is placed before the filter 23 and decimator 24. A

plurality of sensors 11 ($d_0, d_1 \dots d_n$) and delta-sigma modulators 22 receive and digitise input signals to the array. In the preferred embodiment, each of the sensors 31 is a "digital microphone" comprising an electret microphone element 11 and delta-sigma modulator 22, such as a Zarlink ZL70190 4th order $\Delta\Sigma$ modulator (see published [US patent application 2003/0235315](#)). The signal is sampled at a clock rate of 2,048 kHz ($M=256$ times 8 kHz) and the output is a single bit. The single-bit delta modulator outputs are fed to the aforementioned delay elements (preferably a shift register with taps at the appropriate length (a_x)) to obtain a desired delay. In the preferred embodiment, a shift register of length 180 permits steering from $\theta = 0^\circ$ to 90° . The outputs are then summed together and presented to the filter 23 and decimator 24. For an 8-element array ($N=8$) this sum can be adequately represent by a 3 bit word (ceiling $\{\log_2(N)\}$). The filter and decimator design is therefore solved as if the modulator was a 3-bit 4th order integrator to obtain 16 ($t=16$) bits of resolution at a sampling frequency (F_s) of 8kHz.

A significant advantage of the present invention relates to its hardware implementation, which permits configuration as an application specific integrated circuit (ASIC) (e.g. an FPGA, semi-custom chip, etc.) The complexity of the chip is increased by having to operate the summer and the delay lines at the higher sample rate ($M \cdot F_s$). However, this complexity is offset by the elimination of eight ($N=8$) 16 bit FIR filters (typically about 80 taps) running at F_s , or the undesirable alternative of an upsampling / downsampling delay and sum structure which would typically be even more complex.

It is also possible to implement the structure of the present invention in a general purpose DSP if it is more expedient or economical to do so. Often these devices have variable length FIFO buffers that can be used as delay elements, thereby speeding up the operation."

Ex.1006, [0014]-[0016]. *See also id.* Title, Abstract, Fig.4, claim 1. Moquin also describes implementing that phased array beamformer structure in ASIC hardware or in a general-purpose DSP. *Id.*, [0015]-[0017] ("it is also possible to implement

the structure of the present invention in a general purpose DSP”), claim 8 (“The phased array of claim 2, wherein said beamformer, filter and decimator are implemented within a general purpose Digital Signal Processor (DSP).”). It is my opinion, therefore, that Moquin already teaches a data-processing system that performs the claimed beamforming operations.

102. It is also my opinion that Swanson describes a non-transitory computer-readable-medium/program-code implementation. Specifically, Swanson explains that, when its microphone-array and related beamforming functions are “implemented in firmware and/or software,” those functions may be “stored as one or more instructions or code on a computer-readable medium,” including “non-transitory computer-readable storage media,” and that such instructions/data cause one or more processors to implement the disclosed functions:

“If implemented in firmware and/or software, the functions described above may be stored as one or more instructions or code on a computer-readable medium. Examples include non-transitory computer-readable media encoded with a data structure and computer-readable media encoded with a computer program. Computer-readable media includes physical computer storage media. A storage medium may be any available medium that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to store desired program code in the form of instructions or data structures and that can be accessed by a computer. Disk and disc includes compact discs (CD), laser discs, optical discs, digital versatile discs (DVD), floppy disks and blu-ray discs. Generally, disks reproduce data magnetically, and discs

reproduce data optically. Combinations of the above should also be included within the scope of computer-readable media.

In addition to storage on computer readable medium, instructions and/or data may be provided as signals on transmission media included in a communication apparatus. For example, a communication apparatus may include a transceiver having signals indicative of instructions and data. The instructions and data are configured to cause one or more processors to implement the functions outlined in the claims.”

Ex.1005, [0054]-[0055]; *see also id.*, [0023]-[0024]. Swanson identifies a head-end chip that performs microphone-array processing and explains that “the head-end chip may be a processor, such as a digital signal processor (DSP), located between the array of microphones and other circuitry in an electronic device.” *Id.*, [0005]. Swanson’s claim 15 likewise recites “a computer program product” comprising “a non-transitory computer readable medium comprising code for” receiving data from first and second digital microphone arrays, combining data, and beamforming; claim 18 further recites code for adjusting delay. *Id.*, claims 15, 18 (“The computer program product of claim 15, in which the medium further comprises code for performing the steps comprising at least one of adjusting a delay of a microphone of the first array of digital microphones....”).

103. It is my opinion that a POSA would have been motivated to implement Moquin’s DSP-based beamformer using software or firmware stored on a conventional non-transitory computer-readable medium for execution on a

processor, such as a DSP, as taught by Swanson. Moquin itself explains that it may be “more expedient or economical” to “implement” its “structure” in “a general-purpose DSP,” and further that such DSPs can use variable-length buffers as delay elements:

“It is also possible to implement the structure of the present invention in a general purpose DSP if it is more expedient or economical to do so. Often these devices have variable length FIFO buffers that can be used as delay elements, thereby speeding up the operation.”

Ex.1006, [0016]; *see also id.*, Abstract, [0014]-[0015], [0017], Fig.4, claims 1, 8.

It is my opinion that Swanson provided a straightforward implementation path for Moquin’s DSP-based beamformer. This is because Swanson teaches storing digital-microphone-array beamforming-related functions as software/firmware instructions on non-transitory computer-readable media for execution by processors and identifies a digital signal processor as an exemplary head-end chip. *See* Ex.1005, [0023]-[0024], [0054]-[0055], claims 15, 18. Not only would a POSA have understood that Swanson provided a straightforward path for Moquin’s DSP option, a POSA would have also had a reasonable expectation of success in such a modification of Moquin in view of Swanson because the proposed implementation applies Swanson’s known software/storage-medium implementation teachings to Moquin’s known DSP-based beamformer without changing Moquin’s underlying oversampled delay-and-sum beamforming operation. Thus, it is my opinion that

applying Swanson's known software-storage implementation to Moquin's known DSP-based beamformer would have been the predictable use of prior-art elements according to their established functions.

2. **1[a]: "outputting a first oversampled digital signal output from an analog-to-digital converter (ADC), wherein the first oversampled digital signal is responsive to an analog field and the first oversampled digital signal is created at a sampling clock frequency;"**

104. In my opinion, Moquin in view of Swanson renders this limitation obvious.

105. As an initial matter, as discussed in the Technical Background section above, beamforming systems that produce oversampled digital signals from received analog signals were widely known and widely used long before the '055 patent's earliest claimed priority date. *See, e.g., supra* §VI.

106. Referring specifically to the prior art cited in this section of my declaration, Moquin discloses a plurality of "sensors 31," each implemented as a "digital microphone" comprising microphone element 11 and delta-sigma modulator 22. Ex.1006, [0014] ("each of the sensors 31 is a 'digital microphone' comprising an electret microphone element 11 and delta-sigma modulator 22").³

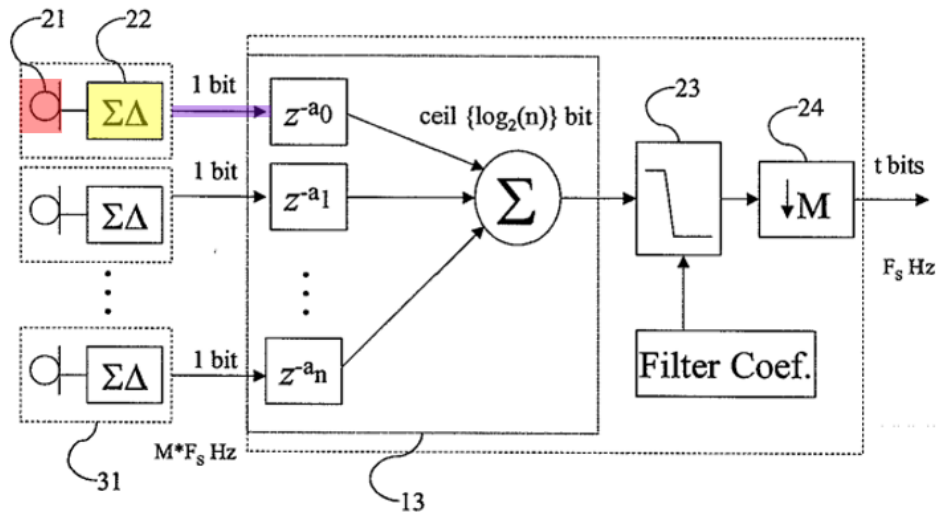
³ Moquin appears to use inconsistent reference numerals in certain places of its publication. For example, Moquin's paragraph [0014], in the course of explaining

Moquin explains that microphone-array signals are digitized by an “Analog-to-Digital Converter (ADC),” and further identifies the relevant oversampling ADC implementation as a delta-sigma modulator. *Id.*, [0002], [0005], [0014].

107. Moquin also states that its sensors “receive and digitise input signals to the array,” and that the signal may be sampled “at a clock rate of 2,048 kHz (M=256 times 8 kHz),” with a single-bit output. *Id.*, [0014]; *see also id.*, [0001], [0005]. This is illustrated in Figure 4 of Moquin, which depicts a microphone

Fig. 4, refers to a “microphone element 11,” while Figure 4 labels the corresponding microphone element as “21.” Ex.1006, [0014], Fig.4. Specifically, Moquin states “each of the sensors 31 is a ‘digital microphone’ comprising an electret microphone element 11 and delta-sigma modulator 22...” *Id.*, [0014]. Figure 4 illustrates sensor “31” and within it includes a) the symbol Moquin uses for a microphone element (*see, e.g., id.*, Fig. 3, [0013]) with the label “21” and b) the symbol Moquin consistently uses for a delta-sigma modulator (*see, e.g., id.*, Fig.3, [0013]) with the label “22.” In my opinion, the “21” in Figure 4 appears to be an apparent typo or reference-numeral inconsistency. In any event, it does not affect or otherwise diminish Moquin’s disclosure that each digital microphone sensor includes a microphone element and delta-sigma modulator.

element (red), delta-sigma modulator (yellow), and single-bit delta modulator output (purple):



Id., Fig.4. Thus, Moquin discloses sampling at a rate that is 256x the 8 kHz telephony sampling rate in the incoming analog data from the electret microphone, which would be understood to constitute oversampling. This oversampling is carried out by a delta-sigma ADC, resulting in an oversampled digital signal output which is sampled at a sampling clock frequency of 2,048 kHz. The fact that the oversampled digital signal is output from the analog-to-digital converter (element 22), which has the electret microphone as an input signal source, supports that the oversampled digital signal is responsive to an analog field. The microphone element senses the acoustic input and creates an analog signal that is converted into an oversampled digital signal by the analog-to-digital converter 22.

108. Thus, it is my opinion that Moquin discloses outputting a first oversampled digital signal output from an analog-to-digital converter (e.g., delta-sigma modulator 22), where the signal is responsive to an analog field (e.g., acoustic input received by microphone element 21) and is created at a sampling clock frequency.

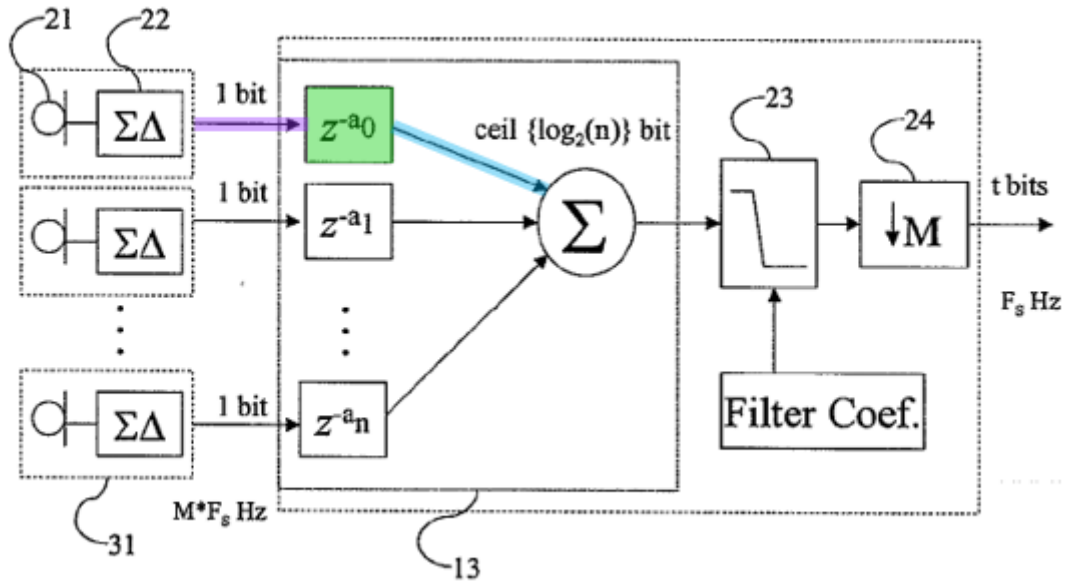
3. 1[b]: “delaying the first oversampled digital signal by a time delay wherein the time delay is equal to an integer number of sampling clock cycles to produce a time delayed first oversampled digital signal; and”

109. In my opinion, Moquin in view of Swanson renders this limitation obvious.

110. As an initial matter, as discussed in the Technical Background section in this declaration, the use of a time delay that is equal to an integer number of cycles of the sampling clock to produce a time-delayed oversampled signal was widely known and broadly used long before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §VI.

111. In its Figure 4 embodiment, Moquin explains that the “signal” from the electret microphone element “is sampled at a clock rate of 2,048 kHz (M=256 times 8kHz),” and that the resulting “single-bit delta modulator outputs are fed to the aforementioned delay elements (preferably a shift register with taps at the appropriate length (a_x)) to obtain a desired delay.” Ex.1006, [0014]. This arrangement is illustrated in Figure 4: specifically, a one-bit oversampled output

from a delta-sigma modulator is input to a corresponding delay element Z^{-a_0} (green), and the delayed output (blue) is then provided to the summing node.



Id., Fig.4. Thus, it is my opinion that Moquin discloses delaying a first oversampled digital signal by a time delay to produce a time-delayed first oversampled digital signal.

112. Moquin further discloses that the time delay is equal to an integer number of sampling clock cycles. Specifically, if the sampling frequency is F_s , then Moquin states that the delay can only take on integer multiples of $(1/F_s)$:

“Spatial aliasing in a discrete line array dictates the minimum inter-element spacing which is most critical at $\theta = 90^\circ$, where $d \leq \lambda/2$. In an analogue system τ is varied to accommodate the desired steering angle. **In digital systems τ can only take on values that are integer multiples of the sample time $(1/F_s)$.**”

Id., [0012] (emphasis added). Moquin also describes the delay elements as “preferably a shift register with taps at the appropriate length a_x) to obtain a desired delay.” *Id.*, [0014]. A POSA would have understood that Moquin is describing a digital delay that can be an integer multiple of the sampling interval, which is the reciprocal of the sampling rate of 2,048 kHz, therefore equal to just under 0.5 us. In other words, Moquin discloses introducing delays that are integer multiples of the $1/(2,048\text{kHz})$ sampling interval. In Moquin’s Figure 4 embodiment, the relevant sampled signal being delayed is the one-bit oversampled signal sampled at the oversampling clock rate (e.g., 2,048 kHz or $M*F_s$). *Id.*, [0014], Fig.4. With this sampling frequency ($M*F_s$), delay would take on integer multiples of $[1/(M*F_s)]$.

113. Moquin further discloses that its implementation of the desired time delay uses “a shift register with taps at the appropriate length (a_x),” and explains that “a shift register of length 180 permits steering from $\theta=0^\circ$ to 90° .” *Id.*, [0014]. It is my opinion that a POSA would have understood that Moquin’s tapped shift register provides integer sampling cycle delay for a couple of reasons. First, Moquin discloses that “[i]n digital systems” (which its system is), the delay “ τ can only take on values that are integer multiples of the sample time ($1/F_s$).” *Id.*, [0012]. Second, Moquin discloses that its implementation of delay is such that each clock pulse shifts the oversampled digital sample stream by one register stage. *Id.*, [0014].

Thus, selecting the output at the Nth tap delays the stream by N oversampling-clock cycles, i.e., an integer multiple of the oversampled sampling period. *See* Ex.1013, 3 (defining shift register as a “circuit in which all bits are shifted one position at each clock cycle”); Ex.1014, 5-6 (defining shift register as a “digital storage circuit in which information is shifted from one flip-flop of a chain to the adjacent flip-flop on application of each clock pulse”). Accordingly, Moquin’s shift-register delay of the one-bit oversampled signal sampled at 2,048 kHz delays the first oversampled digital signal by a time delay equal to an integer number of sampling clock cycles.

4. **1[c]: “combining the time delayed first oversampled digital signal with a second oversampled digital signal to obtain the beamformed digital signal, wherein the second oversampled digital signal is responsive to the analog field.”**

114. In my opinion, Moquin in view of Swanson renders this limitation obvious.

115. As a first matter, combining a delayed signal with another signal to form a beamformed signal was not new at the time of the earliest claimed priority date of the '055 patent. As discussed in the Technical Background section, combinations of signals with delays to produce beamformed signals was well established and widely-used long before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §VI. More recent combinations of oversampled digital signals responsive to analog fields emerged later, along with the emergence of

digital signal processing, but also well before the earliest claimed priority date of the '055 patent.

116. In relation to its Figure 4, Moquin discloses a plurality of sensors that “receive and digitise input signals to the array.” Ex.1006, [0014]. In that embodiment, each such sensor outputs a signal sampled “at a clock rate of 2,048 kHz ($M=256$ times 8kHz) and the output is a single bit.” *Id.* Given this disclosure, it is my opinion that Moquin discloses multiple oversampled digital signals, including a “second oversampled digital signal.” In my opinion, a POSA would have understood that a signal sampled at 256 times the base 8 kHz rate is an oversampled digital signal. *See also id.*, [0005] (“delta-sigma modulators typically oversample sample at $M=256$ times (i.e. $256 * 8 \text{ kHz} = 2,048 \text{ kHz}$)”). Because those signals, as disclosed by Moquin, are produced by sensors that “receive and digitise input signals to the array,” Moquin’s first and second oversampled digital signals are responsive to the analog field. *Id.*, [0014]. The microphone element senses the acoustic input and creates an analog signal that is then converted into an oversampled digital signal by the delta-sigma modulator 22, which is an analog-to-digital converter. *See, e.g., id.*, [0005] (“Most modem Analog-to-Digital converters (ADCs) are of the oversampling delta-sigma type. For telephony applications, delta-sigma modulators typically oversample sample at $M=256$ times (i.e. $256 * 8 \text{ kHz} = 2,048 \text{ kHz}$)...”).

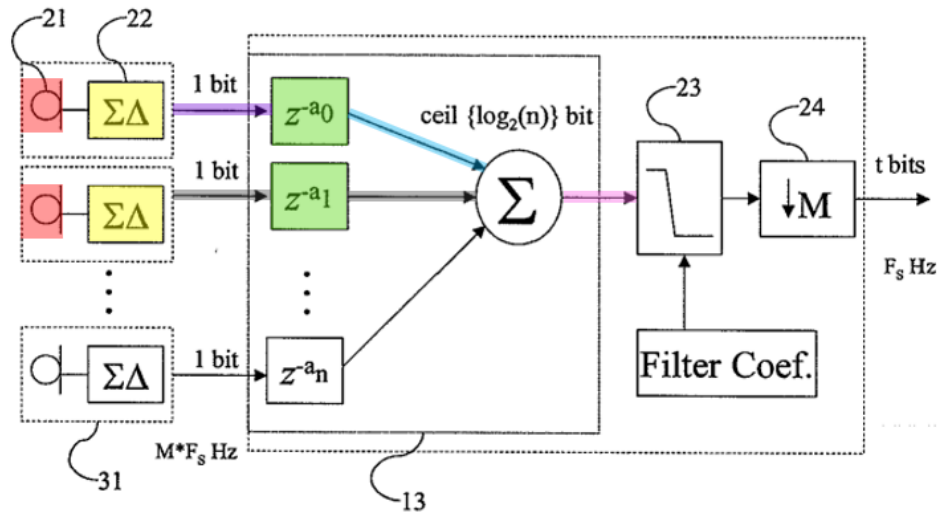
117. As Moquin further discloses, the “single-bit delta modulator outputs are fed to the aforementioned delay elements...to obtain a desired delay,” and the “outputs are then summed together and presented to the filter 23 and decimator 24.” *Id.*, [0014]. The oversampled signals are delay-and-summed to generate a beamformed output signal, as Moquin’s Abstract likewise explains:

“A phased array beamformer is provided, comprising a plurality of sensors arranged in an array, a plurality of samplers for generating respective oversampled signals, a digital filter for performing delay and sum filtering of the oversampled signals to generate a beamformed output signal, and a decimator for downsampling the beamformed output signal to generate a Nyquist sample rate signal at a predetermined look direction. The delay and sum beamforming operation is performed at the oversampling frequency, preferably within a $\Delta\Sigma$ modulator scheme.”

Id., Abstract. Moquin’s claim 6 similarly recites an adder “for summing delayed signals output from said taps to generate said beamformed output signal.” *Id.*, claim 6; *see also id.*, claim 1. A POSA would have understood that the “adder” disclosed by Moquin, like the addition and subtraction elements in many prior art “delay and sum” beamformers, combines the received oversampled signals. Thus, it is my opinion that the summed output of Moquin’s beamformer 13 corresponds to the claimed “beamformed digital signal.” That beamformed digital signal is subsequently processed by filter 23 and decimator 24.

118. Figure 4 of Moquin illustrates this—specifically, multiple one-bit oversampled outputs feed respective delay elements $Z^{-a_0}, Z^{-a_1}, \dots, Z^{-a_n}$, and the

delayed outputs are then summed at Σ in beamformer 13 before the beam sum (pink) is filtered and decimated:



Id., Fig.4.

119. Thus, it is my opinion that Moquin discloses combining the time-delayed first oversampled digital signal with a second oversampled digital signal to obtain the beamformed digital signal.

120. Accordingly, claim 1 would have been obvious to a POSA.

D. Claim 2

1. **“The non-transistory [sic] computer-readable storage medium of claim 1, wherein the combining is performed in an oversampled signal domain.”**

121. It is my opinion that a POSA would have found claim 2 obvious based on Moquin in view of Swanson.

122. As mentioned above, oversampled digital beamformers that combine oversampled signals were well-established long before the '055 patent's earliest

claimed priority date. *See, e.g., supra* §VI. Claim 2 represents a straightforward combination of well-known elements to achieve well-understood benefits.

123. As I explained above for claim 1, it is my opinion that a POSA would have found claim 1 obvious based on Moquin in view of Swanson. *Supra* §§X.A-C.

124. As I also explained for 1[c], Moquin discloses combining/summing the time-delayed oversampled digital signals to obtain the beamformed digital signal. *Supra* §X.C.4.

125. Moquin further discloses that this combining is performed in an oversampled signal domain because, as disclosed in Moquin's Figure 4 embodiment, the oversampled "single-bit delta modulator outputs are fed to the aforementioned delay elements" and "then summed together and presented to the filter 23 and decimator 24." Ex.1006, [0014]. In other words, "the delay and sum beamformer 13 is placed before the filter 23 and decimator 24." *Id.* The "summer and the delay lines" are also disclosed "to operate...at the higher sample rate ($M \cdot F_s$)."
Id., [0015]. The delay and summation thus occur before any down sampling is performed by the decimator 24. *Id.*; *see also id.*, Abstract ("a decimator for downsampling the beamformed output signal"), claim 1 ("a decimator for downsampling said beamformed output signal"). This arrangement, as described, is also illustrated in Figure 4.

126. Thus, it is my opinion that, in the Moquin-Swanson combination, the combining/summing is performed on oversampled signals before filtering and decimation, and therefore is performed in an oversampled signal domain. *See id.*, Abstract (“[t]he delay and sum beamforming operation is performed at the oversampling frequency”).

E. Claim 4

- 1. “The non-transitory computer-readable storage medium of claim 1, wherein the combining is performed in a baseband signal domain.”**

127. It is my opinion that a POSA would have found claim 4 obvious based on Moquin in view of Swanson.

128. Further, as mentioned above, oversampled digital beamformers were well-established long before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §VI. Claim 4 represents a straightforward combination of well-known elements to achieve well-understood benefits.

129. As I explained above for claim 1, it is my opinion that a POSA would have found claim 1 obvious based on Moquin in view of Swanson. *Supra* §§X.A-C.

130. As I further explained for claim 1, in Moquin’s Figure 4 arrangement, a sigma-delta analog-to-digital converter outputs oversampled one-bit digital

signals, and those signals are delayed at the oversampling rate using shift-register delay elements. *Supra* §X.C.

131. In terms of the limitations added by claim 4, a POSA would have been motivated to configure the claimed combining to be performed in the baseband signal domain by applying Moquin's oversampled-domain single-bit delays as in Figure 4's arrangement, and then applying Moquin's disclosed filter 23 and decimator 24 to the output of each delay channel signal before combining/summing.

132. Moquin discloses, with respect to Figure 4, that the delta-modulator output signals are oversampled "at a clock rate of 2,048 kHz ($M=256$ times 8kHz)," "a single bit," and fed to delay elements before being summed. Ex.1006, [0014], Fig.4. Moquin further confirms that "the summer and delay lines" in this Figure 4 arrangement operate "at the higher sample rate ($M \cdot F_s$)":

"A significant advantage of the present invention relates to its hardware implementation, which permits configuration as an application specific integrated circuit (ASIC) (e.g. an FPGA, semi-custom chip, etc.) The complexity of the chip is increased by having to operate the summer and the delay lines at the higher sample rate ($M \cdot F_s$). However, this complexity is offset by the elimination of eight ($N=8$) 16 bit FIR filters (typically about 80 taps) running at F_s , or the undesirable alternative of an upsampling / downsampling delay and sum structure which would typically be even more complex."

Id., [0015]. The output of Moquin's delay element remains a one-bit oversampled delta-modulator stream, which is the type of signal that Moquin's filter 23 and decimator 24 are designed to process. Moquin also discloses the corresponding

filter/decimator functionality: filter 23 and decimator 24 convert the single-bit oversampled delta-modulator output to a multi-bit signal at sampling frequency F_s , e.g., “16 (t=16) bits of resolution at a sampling frequency (F_s) of 8kHz.” *Id.*, [0014].

133. Moquin’s Figure 3 digital-microphone arrangement further shows that filtering/decimation before combining was a known ordering for the same digital-microphone beamformer architecture. In Figure 3, “[e]ach input is filtered at 23 and then decimated at 24 to achieve a desired resolution (t bits) and sampling frequency (F_s),” and the resulting outputs of microphones 31 are supplied to beamformer 13:

“... a typical application of oversampled delta-sigma modulators (such as described in [US Pat 5465270](#) and [US Pat. Application 2003/0235315](#)) is in a microphone array, as illustrated in Figure 3, wherein like references are used to denote like elements in Figure 2. In this case the microphone element 11 and the delta-sigma modulator 22 are packaged together and generally referred to as "digital microphone" 31. The output of microphone 31 is a high-speed digital signal that is immune to digital noise normally found in prior art arrangements such as shown in Figure 2. Each input is filtered at 23 and then decimated at 24 to achieve a desired resolution (t bits) and sampling frequency (F_s). The microphones 31 can be implemented within a single device or a plurality of devices. The outputs of microphones 31 are then supplied to the same type of beamformer 13 discussed above in connection with Figure 2. Integrating the digital circuitry of Figure 3 is reasonably easy and results in significant cost savings.”

Id., [0013], Fig.3. Thus, it is my opinion that to the extent that post-decimation signals are multi-bit signals, Moquin already discloses a beamformer/summer architecture for combining such multi-bit (e.g., t-bit) F_s signals (e.g., Fig.3's arrangement).

134. Whereas the pre-decimation digital signals are oversampled at a frequency $M \cdot F_s$, Moquin's post-decimation outputs are at the lower sampling frequency F_s , and are baseband digital signals. More specifically, Moquin explains that the filter/decimator reduces the oversampled $M \cdot F_s$ frequency signal to the desired lower sampling frequency F_s , and in its telephony example identifies F_s as 8 kHz for audio whose maximum frequency of interest is about 3.5 kHz. Ex.1006, [0003], [0013]-[0014]. This final post-decimation, in-band 8 kHz telephony output digital signal is a baseband digital signal. In my opinion, that understanding is consistent with the disclosure of the '055 patent, which describes a receiver module that low-pass filters and decimates an oversampled digital signal to output a baseband digital signal at a baseband sampling rate. Ex.1001, 3:55-3:67, 6:22-39.

Ex.1001 ('055 patent), 3:55-67:

"The output signal from the delay element 216 is a delayed oversampled digital signal 218 which is input into a receiver module 220. The receiver module 220 performs the functions of low pass filtering and decimation. Low pass filtering removes the high frequency noise resulting from the oversampling process and decimation reduces the sampling frequency to a baseband sampling rate. A baseband digital signal is output at 222 from the receiver

module 220. The baseband signal 222 is a digital signal having a bandwidth as prescribed by an application of interest and, depending on the digitization methodology, an increased dynamic range relative to the oversampled digital signal 214 output from the digital sensor 212.”

Ex.1001 ('055 patent), 6:22-39:

“Some baseband audio signal applications have established frequency ranges and these ranges together with a desired dynamic range for the audio signal place requirements on the sampling clock frequency used to with the digital microphone 272. For example, telephony, compact disk (CD) format, etc. all have requirements for the baseband audio signal that can be accommodated through embodiments of the invention as described herein. Some non-limiting examples are, for example, pulse code modulated (PCM) audio which can be provided at various dynamic ranges and sample rates, which could be provided at 16 bits per sample at 48 kHz in one or more embodiments. Another non-limiting example is 16 bit CD quality stereo PCM at 44.1 kHz. Telephony can be accommodated at different specifications. A non-limiting example is PCM audio at 12 bits per sample at 8 kHz. The foregoing examples of baseband audio formats are provided merely for example and do not limit embodiments of the invention.”

135. A POSA would have been motivated to place Moquin’s filter/decimator after each oversampled-domain delay element and before the summer to obtain the benefit of Moquin’s oversampled-domain delay resolution while performing the summation at a lower baseband rate. Before addressing the aforementioned motivation, I note that Moquin in fact discloses both filtering/decimating after delaying (in Figure 4’s arrangement) and filtering/decimating before combining (in Figure 3’s arrangement). Ex.1006, [0013]-[0015], Figs.3-4.

136. Turning to why a POSA would have been motivated to place Moquin's filter/decimator after each oversampled-domain delay element and before the summer. First, doing so would have maintained the benefit of Moquin's oversampled-delay resolution. As Moquin itself teaches, and a POSA would have understood, the delay resolution is inversely proportional to the sampling frequency. *Id.*, [0012] ("In digital systems τ can only take on values that are integer multiples of the sample time ($1/F_s$)."). By not filtering/decimating until after the delaying, Moquin's time delay can take on integer multiples of the oversampling time $1/(M \cdot F_s)$, which is finer resolution by a factor of M , than if the decimation occurs before the delay, in which case, the time delay can only take on integer multiples of $(1/F_s)$.

137. This would have provided motivation for a POSA to include such filtering/decimating after delaying, especially in light of Moquin's objective of "finer resolution in terms of time delay." *Id.*, [0006] ("The inventors of the present invention have recognised that access to the oversampled signal allows for construction of a low-cost delay and sum beamformer with much finer resolution in terms of time delay than is possible with the prior art."), [0004] ("It is an object of an aspect of the invention to provide a phased array with sub-millimetre resolution."), [0002] ("The simplest filtering technique is the ubiquitous 'delay and sum' beamformer which sums the inputs together with an appropriate delay to

obtain a desired beamshape and direction. A significant disadvantage of this technique is that the delay resolution is determined by the sampling frequency of the ADC, which, in general, is limited to the Nyquist sampling rate.”).

138. Second, placing the filter/decimator after the oversampled-domain delay element allows the same single-bit delay elements, as disclosed in Figure 4’s arrangement to be used, which would have understandably simplified the implementation. These single-bit delay elements would also allow for reduced complexity compared to multi-bit (e.g., 16-bit) delay elements. *See id.*, [0015].

139. Third, as a POSA would have also understood, and Moquin itself acknowledges, performing combination/summation at the higher oversampled-domain rate “increase[s] complexity.” *See id.*, [0015] (“The complexity of the chip is increased by having to operate the summer and the delay lines at the higher sample rate ($M \cdot F_s$).”). This follows from the fact that it is more complex in terms of the computational/processing resources needed to process the higher frequency data, than if the frequency was at a lower, baseband sampling frequency. Thus, a POSA would have understood that performing the combination/summation at the lower baseband frequency, F_s , instead of at the higher oversampled rate, $M \cdot F_s$, would have provided the benefit of a less complex combination/summation.

140. A POSA would have also understood that locating the filter/decimator before the combiner/summer and after the delay elements would reduce the

complexity of Moquin's combining/summing operations. *See, e.g., id.*, [0015] (“[t]he complexity of the chip is increased by having to operate the summer and the delay lines at the higher sample rate ($M \cdot F_s$).”). A POSA would also be motivated to pursue this proposed filter/decimator location because it would allow the delay lines to retain their single-bit operation as opposed to requiring multi-bit (e.g., 16-bit) functionality. *See id.* Although placing the filter/decimator before the combiner may involve implementation of filter/decimator circuitry in each channel, Moquin's Figure 3 expressly discloses that type of per-input filtering/decimation before beamformer 13, and a POSA would have understood the proposed ordering as a predictable design tradeoff that preserves Figure 4's fine oversampled-domain delay resolution while using Figure 3's known lower-rate, post-decimation beamformer/summer arrangement for baseband-domain combining. *Id.*, [0013]-[0015], Figs.3-4.

141. I do not understand Moquin as criticizing or excluding the use of per-channel filtering/decimation before summation. To the contrary, Moquin expressly identifies the Figure 3 architecture as a known digital-microphone arrangement in which each high-speed one-bit digital microphone output is filtered and decimated to F_s before being supplied to beamformer 13. *Id.*, [0013], Fig.3. Moquin's Figure 4 then teaches that placing the delay operation in the oversampled domain provides the fine delay resolution that was missing from conventional baseband-rate delay-

and-sum systems. *Id.*, [0012]-[0016], Fig.4. A POSA would have understood that those teachings could predictably be used together by applying the oversampled-domain delay first, while the signal is still a one-bit high-rate stream, and then applying the known per-channel filter/decimator before baseband-domain summation.

142. A POSA would have understood this as a design tradeoff rather than a change in operating principle. The arrangement preserves the principal advantage of Moquin's Figure 4—fine, sampling-clock-cycle delay resolution in the oversampled domain using simple one-bit delay elements—while moving the summer to the lower-rate F_s domain disclosed in Figure 3. That lower-rate summer would reduce the speed and switching requirements of the combining operation and would produce baseband-domain signals for downstream processing. Although the arrangement uses per-channel filtering/decimation as in Moquin's Figure 3, Moquin itself describes that per-channel filtering/decimation architecture as feasible and cost-saving in integrated digital circuitry. *Id.*, [0013]. A POSA therefore would have had a reasonable expectation of success implementing this ordering using Moquin's same known components for their known functions: sigma-delta digital microphones, high-rate single-bit delay elements/shift registers, low-pass filter/decimator stages, and a beamformer/summer.

143. Thus, implementing the claim-4-specific ordering would have predictably preserved the fine delay resolution provided by Moquin's Figure 4 shift-register delays and further allowed the signal combination/summation to be performed on lower-rate, post-decimation baseband signals, as in Moquin's Figure 3 arrangement.

144. A POSA would have also had a reasonable expectation of success with this implementation because this claim-4-specific ordering uses Moquin's disclosed components. More specifically, this implementation would have used the following expressly disclosed components for their known functions: oversampled-domain single-bit delay elements, as disclosed in Figure 4's arrangement; Moquin's filter 23 and decimator 24, which receive oversampled single-bit inputs and output multi-bit outputs at baseband (as taught by Figure 3); and Moquin's Figure 3 summer, which receives multi-bit baseband frequency sampled signals and outputs a beamformed digital signal at baseband frequency. *Id.*, [0013]-[0015]; Figs.3-4. Thus, it is my opinion that in the Moquin-Swanson combination as modified based on Moquin's Figure 3 arrangement teachings, the delayed channel signals are filtered/decimated after delaying and before summation, and the combining is therefore in the baseband signal domain.

F. Claim 5

1. **"The non-transitory computer-readable storage medium of claim 1, wherein the first oversampled digital signal and**

the second oversampled digital signal are obtained from different sensors.”

145. In my opinion, a POSA would have found claim 5 obvious based on Moquin in view of Swanson.

146. As I explained above, it is my opinion that a POSA would have found claim 1 obvious based on Moquin in view of Swanson. *Supra* §§X.A-C.

147. Further, as mentioned above, oversampled digital beamformers were well-established long before the '055 patent's earliest claimed priority date, and this included implementations with two or more distinct microphones. *See, e.g., supra* §VI. Claim 5 represents a straightforward combination of well-known elements to achieve well-understood benefits.

148. As I further discussed for 1[c], Moquin discloses multiple sensors that receive and digitize input signals to the array. *Supra* §X.C.4. With respect to Figure 4's arrangement, Moquin discloses a plurality of sensors (which are further disclosed to be digital microphones), each including a microphone element and a delta-sigma modulator, and each outputting a respective one-bit oversampled digital signal to beamformer 13. Ex.1006, [0014], Fig.4.

149. Thus, it is my opinion that, in the Moquin-Swanson combination, the claimed “first oversampled digital signal” and “second oversampled digital signal” would correspond to signals output from two different sensors, e.g., different digital microphones 31.

G. Claim 7

- 1. “The non-transitory computer-readable storage medium of claim 1, further comprising: applying a low pass filter with decimation to the time delayed first oversampled digital signal to output a baseband digital signal that is delayed by the time delay.”**

150. In my opinion, a POSA would have found claim 7 obvious based on Moquin in view of Swanson.

151. As I explained above for claim 1, it is my opinion that a POSA would have found claim 1 obvious based on Moquin in view of Swanson. *Supra* §§X.A-C.

152. As a first matter and as explained in the Technical Background section in this declaration, digital beamforming systems that used combinations of oversampling, delaying, filtering, decimation and combiners were well established long before the time of the '055 patent. *See, e.g., supra* §VI. Claim 7 represents a straightforward combination of well-known elements to achieve well-understood benefits.

153. As I further explained for 1[b], in Moquin's Figure 4 arrangement, the first oversampled digital signal is time delayed at the oversampling rate using delay elements $Z^{-a_0}, Z^{-a_1}, \dots, Z^{-a_n}$. *Supra* §X.C.3. And as I explained for claim 4, Moquin also teaches an alternative Figure 3 ordering in which filtering/decimation occurs before the beamformer, while Figure 4 teaches introducing delay in the

oversampled domain before summing. *Supra* §X.E. In my opinion, a POSA would have been motivated, in light of Figure 3's ordering, to apply Moquin's filter 23 and decimator 24 to each delayed channel signal after Moquin's oversampled-domain delay element and before summing, including for the reasons discussed above for claim 4. *See supra* §X.E. In such implementation, the filtering/decimating of Moquin's filter 23 and decimator 24 is applied to the time-delayed first oversampled digital signal output following the delay element. *Id.*

154. In my opinion, Moquin describes low pass filter with decimation functionality. Specifically, with respect to its Figure 4's arrangement, Moquin discloses that the one-bit signal sampled "at a clock rate of 2,048 kHz (M=256 times 8kHz)," is fed to delay elements, and then on to filter 23 and decimator 24, which produce, e.g., "16 (t=16) bits of resolution at a sampling frequency (Fs) of 8kHz." Ex.1006, [0014], Fig.4. A POSA would have understood that this transformation of the signal from 1-bit sampling at 2,048 kHz to 16-bit signal at 8 kHz could be achieved using a filter with decimation, and that digital filters with decimation were well-established long before the earliest claimed priority date of the '055 patent.

155. In my opinion, Moquin's filter 23 and decimator 24 disclose, or at least render obvious, the claimed low pass filter with decimation. Moquin discloses that its filter and decimator design downsamples the received delta-sigma data by a factor of 256 to produce a lower rate 16-bit signal. More specifically, Moquin's

signal path begins with oversampled delta-sigma data sampled at 2,048 kHz and uses its “filter and decimator design” to produce a 16-bit signal at $F_s=8$ kHz, a telephony sampling rate for audio content up to about 3.5 kHz. Ex.1006, [0003], [0005], [0014], Fig.4. Filter 23 provides the low-pass/anti-aliasing filtering by passing the desired in-band audio content and attenuating higher-frequency components, including out-of-band quantization noise, before downsampling. Decimator 24 then performs the decimation by reducing the sample rate to F_s . Ex.1006, [0014]; Ex.1014, 3-4; Ex.1021, 1; Ex.1022, 1.

156. As a POSA would have understood, filter 23 preceding decimator 24 is a low-pass filter. First, the filter passes the desired relatively low frequency in-band signal and attenuates higher-frequency components in the signal, including out-of-band quantization noise, before reducing the sample rate to F_s . *See, e.g.*, Ex.1022 (G. Moon et al., Design Approach for Decimation Filter for ADC Application, Int’l J. of Eng. Trends and Techn. (IJETT), vol. 10 no. 12 (2014)) at p. 1 (“Decimation is the process of reducing the sampling rate. In practice, this usually implies low-pass filtering a signal, then throwing away some of its samples.”), *id.* (“The main task of a decimation filter is to remove the quantization noise away from the band of interest and avoid aliasing of high frequency components down to low frequency region or within the signal bandwidth.”); Ex.1021 (L. Milic, Multirate Filters: An Overview, *APCCAS 2006 - 2006 IEEE*

Asia Pacific Conference on Circuits and Systems, Singapore, 2006, pp. 912-915), at p. 1 (“The use of an appropriate filter enables one to convert a digital signal of a specified sampling rate into another signal with the desired sampling rate without significantly destroying the signal components of interest.”); *id.* (“Decimating the sampling rate by an integer factor of M means that among the input samples, ... only every M th sample are used as in the output sequence. For avoiding aliasing, there is a need to use a low-pass anti-aliasing filter before down-sampler...”).

157. Second, a POSA would have understood that in the context of “decimation” generally, and especially in instances as present in Moquin where a decimation or downsampling factor of 256 is implemented, filtering is needed to suppress aliasing. Aliasing occurs in the process of downsampling where non-attenuated high frequency signals can fold back into the low-frequency passband and contribute to the amplitudes of lower frequency components. *See, e.g.*, Ex.1014, 3-4 (Rudolf F. Graf, Excerpts from Modern Dictionary of Electronics Seventh Edition, 1999, at pp. 16-17) (“aliasing –...A phenomenon arising as a result of the sampling process in which high-frequency components of the original analog signal (whether information or noise) appear as lower frequencies in the sampled signal. Aliasing occurs when the sampling rate is less than twice the highest frequency existing in the original analog signal.”).

158. As a POSA would have understood, a low-pass filter would prevent aliasing in Moquin's system. *See, e.g.,* Ex.1021 (L. Milic, Multirate Filters: An Overview, *APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, 2006, pp. 912-915), at p. 1 ("Filtering is required to suppress aliasing when reducing the sampling rate, called as decimation."); *id.* ("For avoiding aliasing, there is a need to use a low-pass...filter before down-sampler.").

159. Thus, in my opinion, applying Moquin's filter 23 and decimator 24 to the delayed oversampled stream applies a low-pass filter with decimation.

160. Even if Moquin's filter 23 were not a low-pass filter, a POSA would have found the claimed low pass filter with decimation obvious based on Moquin's filter 23 and decimator 24.

161. As a POSA would have understood, by the time of the '055 patent's earliest claimed priority date, decimation was generally preceded by a low-pass filter for all the reasons discussed above, including preventing aliasing. *Supra* ¶¶155-158. To the extent a different type of filter could have been used, a POSA would have understood that, of the limited and finite number of effective filter types, low-pass filters were predominant, relatively simple to implement, and widely applied.

162. Given the limited and finite number of ways to perform pre-decimation filtering, a POSA would have been motivated to use a low-pass filter. A POSA

would have selected a low-pass filter in particular because it would preserve the desired in-band/baseband signal content while attenuating out-of-band quantization noise and other components that otherwise could alias into the lower-rate output during decimation. The results of such an approach would have been predictable, given the predominant use of low-pass decimation filters in the field. Accordingly, even if Moquin did not disclose a low-pass filter, a POSA would have been motivated to implement Moquin's filter 23 as a low-pass filter.

163. Moquin's filter/decimator outputs a baseband digital signal. Moquin explains that for telephony applications, its delta-sigma converters oversample at $M=256$ times the 8 kHz and then downsample to $F_s=8\text{kHz}$. Ex.1006, [0005], [0014]. The filter/decimator in Moquin's Figure 4 arrangement outputs a 16-bit output at sampling frequency $F_s=8\text{ kHz}$. *Id.*, [0014]. The output from Moquin's filter and decimator design is the downsampled digital signal having a sampling frequency $F_s=8\text{kHz}$, which corresponds to the final lower-rate telephony audio representation of the oversampled microphone signal—i.e., a baseband digital signal. That understanding is consistent with the '055 patent, which describes receiver module 220 low-pass filtering and decimating an oversampled digital signal to output baseband digital signal 222 at a baseband sampling rate, with bandwidth prescribed by the application of interest. Ex.1001, 3:55-3:67, 6:22-39.

164. In the resulting Moquin arrangement, the output of the delay element remains a delayed one-bit oversampled delta-modulator stream, which is the same type of signal processed by Moquin's Figure 3 per-channel filter 23 and decimator 24. *See* Ex.1006, [0013]-[0014], Figs.3-4. Applying Moquin's filter 23 and decimator 24 downstream of the delay element would therefore convert the delayed oversampled stream into a lower-rate, higher-resolution baseband signal while preserving the time shift already imparted by the delay element; the filtering/decimation would not undo the selected delay. *Id.* Thus, it is my opinion that the output is a baseband digital signal delayed by the same time delay. *Id.*

165. Figure 3 also shows that the resulting t-bit F_s channel signals are supplied to beamformer 13 for summing. *Id.*, [0013]-[0014], Fig.3.

166. A POSA would have been motivated to use this Figure-3-informed Moquin arrangement for the reasons I explained for claim 4, including to preserve Moquin's fine oversampled-domain delay resolution (as in its Fig.4 arrangement) while producing a lower-rate baseband signal usable for subsequent processing. *Supra* §X.E. This arrangement uses Moquin's disclosed components (oversampled-domain delay elements (as in its Figure 4 arrangement), filter 23 and decimator 24 (as in both its Figures 3 and 4 arrangements), and, where subsequent summing is performed, Moquin's Figure 3 multi-bit beamformer/summer arrangement) for their known functions. *See* Ex.1006, [0013]-[0015], Figs.3-4.

167. For the same reasons explained for claim 4, the proposed ordering applies Moquin's filter 23 and decimator 24 to each delayed oversampled stream after the oversampled-domain delay and before baseband-domain summation. *Supra* §X.E. This is the same filter/decimator function Moquin already uses to convert high-speed one-bit delta-sigma streams to lower-rate t-bit Fs data, and the delay is preserved because filtering/decimation occurs downstream of the delay.

H. Claim 8

1. **“The non-transitory computer-readable storage medium of claim 7, wherein the time delay is equal to a fraction of a baseband sampling period.”**

168. In my opinion, a POSA would have found claim 8 obvious based on Moquin in view of Swanson.

169. As an initial matter, as discussed in the Technical Background section in this declaration, digital beamforming systems which relied on oversampled input signals, followed by delays and filters and decimation were well-known and in wide use well before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §VI. Claim 8 represents a straightforward combination of well-known elements to achieve well-understood benefits.

170. As I explained above for claim 7, it is my opinion that a POSA would have found claim 7 obvious based on Moquin in view of Swanson. *Supra* §§X.A-B, G.

171. As I further explained for claim 7, Moquin renders obvious outputting a baseband digital signal at the post-decimation sampling frequency F_s . *Supra* §X.G. In its Figure 4 embodiment, Moquin discloses that a signal is “sampled at a clock rate of 2,048 kHz ($M=256$ times 8 kHz),” and that the desired delay is implemented using “a shift register with taps at the appropriate length (a_x),” with a shift register length of 180 permitting steering from $\theta=0^\circ$ to 90° .” Ex.1006, [0014].

172. Because Moquin’s 2,048 kHz oversampling clock frequency is 256 times the 8 kHz baseband sampling frequency, each oversampling-clock period is $1/256$ of the baseband sampling period. This follows from the fact that the oversampling clock period = $[1/(256*8\text{kHz})]$, and the baseband clock period = $[1/(8\text{kHz})]$. *See, e.g., id.*, [0012] (explaining that “[i]n digital systems τ can only take on values that are integer multiples of the sample time”). Thus, the oversampling clock period = baseband sampling period/256.

173. Moquin’s tapped shift register supplies delays in those oversampling-clock period increments. More specifically, each clock period advances the sample stream by one register stage, and selecting the output at the N th tap produces an N -cycle delay. *Id.*, [0014]. Thus, given that the oversampling clock period is equal to the baseband sampling period divided by 256, any selected shift register tap with $N < 256$ provides a delay equal to a fraction of the baseband sampling period. *Id.* For example, a tap selected at the 180th stage of Moquin’s shift-register example

corresponds to 180 oversampling-clock periods (or cycles), or 180/256 of one baseband sampling period. *Id.*

174. A POSA would have been motivated to use such a fractional-baseband sampling period delay because Moquin discloses applying delays in the oversampled domain to obtain finer steering resolution than would be available using only baseband sampling period delay increments. *Id.*, [0004], [0006], [0012], [0014]. A POSA would have also understood that the desired delay may be less than one baseband period depending on array geometry, sensor spacing, propagation speed, steering angle, and focusing requirements.

I. Claim 9

1. “The non-transitory computer-readable storage medium of claim 7, wherein the time delay is greater than a baseband sampling period.”

175. In my opinion, a POSA would have found claim 9 obvious based on Moquin in view of Swanson.

176. As an initial matter, as discussed in the Technical Background section in this declaration, digital beamforming systems which relied on oversampled input signals, followed by delays and filters and decimation were well-known and in wide use well before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §VI. Claim 9 represents a straightforward combination of well-known elements to achieve well-understood benefits.

177. As I explained above for claim 7, it is my opinion that a POSA would have found claim 7 obvious based on Moquin in view of Swanson. *Supra* §§X.A-B, G.

178. As I further explained for claim 8, Moquin discloses oversampling at a frequency of 2,048 kHz, i.e., $M=256$ times the 8 kHz baseband sampling frequency. *Supra* §X.H; Ex.1006, [0005], [0014]. Thus, one baseband sampling period corresponds to 256 oversampling-clock periods (or cycles).

179. Moquin discloses implementing delay using “a shift register with taps at the appropriate length (a_x),” and also explains that, in a DSP implementation, variable-length buffers may be used as delay elements. Ex.1006, [0014], [0016]. Moquin’s 180-stage shift-register example is not a limit on the size of the delay element; it is an example for the disclosed microphone-array embodiment. *Id.*, [0014]. Because one baseband sampling period corresponds to 256 oversampling-clock cycles, a shift register tap position or buffer depth greater than 256 oversampling-clock periods (or cycles) would produce a delay greater than one baseband sampling period.

180. A POSA would have been motivated to allow selection of a delay length exceeding 256 in Moquin where such a desired beamforming delay exceeded one baseband period. Doing so would allow for a delay greater than one baseband period while preserving Moquin’s fine oversampled-domain delay resolution.

Moquin discloses using relative delays to steer a beam, explains that oversampled-domain delay provides finer resolution than baseband-rate delay, and states that its principles apply not only to the disclosed microphone-array embodiment but also to other phased arrays using oversampling ADCs, such as ultrasound, radar, and sonar arrays. Ex.1006, [0002]-[0006], [0012], [0014], [0017]. Moquin's disclosed 50-mm inter-element spacing and 350-m/s propagation speed, applied to its steering relationship at 90° end-fire, yield an inter-element delay of approximately 143 usec—about 293 cycles at 2.048 MHz and greater than the 125-usec period of the 8-kHz baseband output. Ex.1006, [0003], [0005], [0011]-[0014].

$$\text{Calculation 1: } \tau = \frac{d \sin \theta}{c} = \frac{0.050 \text{ m} \times \sin(90^\circ)}{350 \text{ m/s}} \approx 0.0001428 \text{ s} \approx 142.9 \text{ usec}$$

$$\text{Calculation 2: } 142.9 \text{ usec} \times 2.048 \text{ MHz} \approx 293 \text{ cycles}$$

$$\text{Calculation 3: } T_{BB} = \frac{1}{8 \text{ kHz}} = 125 \text{ usec}$$

181. A POSA would have had a reasonable expectation of success to select a shift register length or buffer depth exceeding 256 because increasing shift-register length or buffer depth simply extends the same delay mechanism Moquin already uses: each additional stage or buffer location stores another oversampled sample, and selecting a later tap or read position increases delay without changing the delay operation, summing operation, or downstream filtering/decimation.

XI. GROUND 2: CLAIM 3 IS OBVIOUS BASED ON MOQUIN, SWANSON, AND LIU

182. In my opinion, a POSA would have found claim 3 obvious based on Moquin in view of Swanson and Liu.

A. Motivation to Combine

183. In my opinion, a POSA implementing the Moquin-Swanson combination would have been motivated to apply Liu's staged-reconstruction teaching because Liu's approach performs summation below the ADC oversampling rate, and Moquin recognizes that operating the summer at the higher oversampling rate increases complexity. Ex.1007, Abstract, [0006], [0035], [0055]-[0057]; Ex.1006, [0015].

184. Similar to Moquin and Swanson, Liu discloses a system for beamforming that includes oversampling analog-to-digital converters 14, a memory/delay controller 28 for delaying digital samples, reconstruction/decimation filters 18 and 26, and a summer 24 for combining digital samples. Ex.1007, Abstract, [0025], [0029]-[0030], [0032]-[0035], [0038]-[0040], Fig.2.

185. Liu explains that its staged architecture avoids two undesirable extremes: summing at the sigma-delta rate, which may cause dynamic-receive artifacts, and completely demodulating each channel before summation, which requires long per-channel filters and may be complicated and expensive. *Id.*,

[0019]-[0020]. Liu instead performs partial reconstruction before summation and further reconstruction after summation. *Id.*, Abstract, [0006].

186. With that staged approach, Liu teaches signal combination/summation being performed “at a data rate less than output by the initial oversampling and greater than the Nyquist rate or other rate above the Nyquist rate,” with later reconstruction/decimation post-combination/summation reducing the sampling rate further. *Id.*, [0055]-[0057]. In other words, Liu’s first reconstruction/decimation filter 18 “outputs signals oversampled less than output by the oversampling converters 14 and more than output by the second filter 26,” and Liu’s summer 24 sums those signals. *Id.*, [0035], [0038]. Thus, Liu discloses combining at an intermediate sampling rate.

187. Moquin discloses performing signal combination/summation at the same oversampling rate as output by its analog-to-digital converter (ADC). Ex.1006, [0014], Fig.4. Nevertheless, Moquin acknowledges that “operat[ing] the summer and the delay lines” at that oversampling frequency (e.g., 2,048 kHz) increases complexity. *Id.*, [0015].

188. Liu recognizes that performing signal combination/summation at the ADC oversampling rate may “lead[] to dynamic receive artifacts,” while reducing each channel all the way to the final/Nyquist rate before summing can require long per-channel filters. Ex.1007, [0020] (“In one extreme, there is no channel

demodulation and the beam sum is computed at the sigma delta rate. This first extreme often leads to dynamic receive artifacts.”); *see also id.*, [0019]. To mitigate such artifacts, Liu teaches an approach whereby channel signals are downsampled by a first-stage filter to an intermediate sampling rate, which is higher than the final application/Nyquist rate but lower than the oversampled analog-to-digital converter rate, after time delaying, but before combination/summation. Ex.1007, Abstract, [0006]. Liu expresses that this downsampling to an intermediate frequency, between the ADC oversampled rate and the Nyquist rate, may be advantageous compared to downsampling to the Nyquist rate entirely in one stage. *See* Ex.1007, [0020], [0029]-[0030].

189. A POSA would have been motivated to incorporate Liu’s teachings regarding multi-staged downsampling into the Moquin-Swanson architecture. In the resulting combination, a first-stage reconstruction/decimation filter would be applied to Moquin’s delayed channel signals to downsample to an intermediate sampling frequency between the ADC oversampled rate (e.g., 2,048kHz) and the telephony application rate (e.g., 8kHz). Then, the resulting intermediate-rate signals would be combined/summed before being input to a second-stage reconstruction/decimation filter. This arrangement would have preserved Moquin’s fine delay resolution, substantially decreased the clock rate and computation overhead required by Moquin’s summing circuits while avoiding full per-channel

reconstruction before summation, and reduced the likelihood of dynamic receive artifacts.

B. Reasonable Expectation of Success

190. In my opinion, a POSA would have had a reasonable expectation of success in integrating Liu's teachings regarding intermediate-rate summation into the Moquin-Swanson system.

191. First, the combination addresses the implementation of decimation filtering, which has been well-known in the field of beamforming and signal processing long before the earliest claimed priority date. *See, e.g.*, Ex.1021 (L. Milic, Multirate Filters: An Overview, *APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, 2006, pp. 912-915), at p. 1 (Abstract) ("Multirate filtering techniques are widely used in ... sampling rate conversion systems..."); *id.* ("A multirate filter is a digital filter that changes the input sampling rate of the input signal into another desired one. These filters are of an essential importance in communications, image processing, digital audio, and multimedia.").

192. Both Moquin and Liu, in addition to teaching decimation filtering, teach beamforming summation, including summation of multi-bit signals at sampling rates decimated (or downsampled) from the ADC oversampled rate. *See*,

e.g., Ex.1006 (Moquin), Fig.3, [0013]; Ex.1007 (Liu), [0032]-[0035], [0038]-[0040], Fig.2.

193. Both Moquin and Liu likewise recognize the benefit of performing delay at the ADC oversampled rate, which provides fine delay resolution, and then providing decimating filters to downsample the signals. *See, e.g.*, Ex.1006 (Moquin), Fig.4, [0014]; Ex.1007 (Liu), [0032]-[0035], [0038]-[0040], Fig.2. The combination thus involved the implementation of known components having known functions (*e.g.*, Moquin's oversampled-domain delay elements and beamforming architecture; Liu's reconstruction/decimation filters and intermediate rate multi-bit summer).

C. Claim 3

- 1. “The non-transitory computer-readable storage medium of claim 1, wherein the combining is performed at an intermediate sampling rate.”**

194. In my opinion, a POSA would have found claim 3 obvious based on Moquin in view of Swanson and Liu.

195. As an initial matter, as discussed in the Technical Background section in this declaration, digital beamforming systems which relied on oversampled input signals, followed by various combinations of delays and filters and decimation were well-known and in wide use before the earliest claimed priority date of the '055 patent. *Supra* §VI. Thus, by that time, it was known that there were benefits to

various combinations of these elements depending on the capabilities of each element, the characteristics of the incoming signals, and the requirements for the resulting combined signals. Thus, claim 3 represents a straightforward combination of well-known elements to achieve well-understood benefits. Moreover, cost and power constraints would have motivated a POSA to select and combine these known signal-processing elements—such as oversampled ADCs, digital delays, filters/decimators, and combiners—in such a configuration that provided the desired beamforming performance while avoiding unnecessary processing, memory, and circuit overhead.

196. As I explained above for claim 1, it is my opinion that a POSA would have found claim 1 obvious based on Moquin in view of Swanson. *Supra* §§X.A-C.

197. As I further explained for claim 1 in Ground 1, Moquin and Swanson render obvious delaying oversampled digital sensor signals in the oversampled domain and combining the delayed signals to obtain a beamformed digital signal. *Supra* §X.C. Claim 3 further requires that the combining be performed at an intermediate sampling rate. Liu discloses such an implementation. For example, Liu discloses a beamforming system including oversampling analog-to-digital converters 14, a memory/delay controller 28 for delaying digital samples, reconstruction/decimation filters 18 and 26, and a summer 24 for combining digital

samples. Ex.1007, Abstract, [0025], [0029]-[0030], [0032]-[0035], [0038]-[0040], Fig.2.

198. Liu discloses performing reconstruction/decimation in stages. More specifically, Liu explains that “[p]artial reconstruction to a rate less than the oversampling rate, but greater than the Nyquist rate, occurs prior to summation across channels,” and that “[a]fter summation, the samples are reconstructed at a Nyquist or other rate.” *Id.*, Abstract, [0006]. In line with that staged approach, Liu’s first reconstruction/decimation filter 18 “outputs signals oversampled less than output by the oversampling converters 14 and more than output by the second filter 26,” and Liu’s summer 24 then sums those signals:

“The filter 18 partially reconstructs the samples. The filter 18 reduces the incoming samples in rate, such as by decimation. Any decimation scale may be used, such as reducing the rate to a half, a quarter, an eighth or more. The filter 18 may increase the samples in bit width, such as by combination in filtering. Any increase in bit width may be used, such as changing from one bit to three, four, five, six, or more bit samples. For example, the filter 18 outputs signals oversampled less than output by the oversampling converters 14 and more than output by the second filter 26. The filter 18 outputs signals with a bit width greater than output by the oversampling converters 14 and less than output by the second filter 26. The beam sum is computed at a high rate but using only a few bits as compared to Nyquist sampling. To improve digitization accuracy or for other purposes such as channel-wise decoding of coded-excitation, the filters 18 are cascaded with additional filters for each channel.”

“The summer 24 is a node, digital summer, processor, digital circuit, or other device for combining digital samples. The summer 24 sums the relatively apodized and focused signals from a plurality of channels. Multiple input arrows are shown for each summer 24 to reflect inputs from the multiple

channels. The summer 24 is a single multiple input summer or a cascade of summers each having two or more inputs. The summer 24 is a multiple bit sample summer, such as summing four or six bit samples.”

Id., [0035], [0038]. Liu confirms that summation is performed “at a data rate less than output by the initial oversampling and greater than the Nyquist rate or other rate above the Nyquist rate,” while later reconstruction (e.g., filtering and decimation) reduces the sampling rate below the beam-sum data rate. *Id.*, [0055]-[0057].

199. Thus, it is my opinion that Liu discloses combining at an intermediate sampling rate, with that intermediate rate being a rate below the initial oversampling analog-to-digital converter rate and above the later final/Nyquist output rate.

200. A POSA would have found it obvious to implement Moquin’s filtering/decimation functionality in light of Liu’s staged manner teachings by applying a first-stage reconstruction/decimation filter to Moquin’s delayed channel signals before summing, combining/summing the resulting intermediate-rate signals, and then applying a second-stage reconstruction/decimation filter after summing. This arrangement preserves Moquin’s oversampled-domain delay, which provides fine delay resolution (compared to delay at lower sampling rates) before the first-stage reconstruction/decimation while causing the combining to occur at Liu’s intermediate rate. *Id.*

201. In the combination, a POSA would have understood that the intermediate sampling rate summer would receive multi-bit inputs. Liu expressly discloses that filter 18 may increase bit width before summing and that summer 24 is “a multiple bit sample summer.” Ex.1007, [0035], [0038]. Moquin’s Figure 3 arrangement likewise discloses beamformer 13 receiving t-bit post-filter/decimator signals. Ex.1006, [0013], Fig.3.

202. A POSA would have been motivated to use Liu’s teachings regarding a staged reconstruction/decimation filter approach whereby the signal at the ADC oversampled rate is time delayed, and then downsampled to an intermediate sampling rate in the Moquin-Swanson combination.

203. Moquin acknowledges that “operat[ing] the summer and the delay lines” at that oversampling frequency (e.g., 2,048 kHz) increases complexity. *Id.*, [0015]. Liu recognizes that performing signal combination/summation at the ADC oversampling rate may lead to dynamic receive artifacts. Ex.1007, [0020] (“In one extreme, there is no channel demodulation and the beam sum is computed at the sigma delta rate. This first extreme often leads to dynamic receive artifacts.”).

204. To mitigate such artifacts, Liu teaches an approach whereby channel signals are downsampled by a first-stage filter to an intermediate sampling rate, which is higher than the final application/Nyquist rate but lower than the oversampled analog-to-digital converter rate, after time delaying, but before

combination/summation. *Id.*, Abstract, [0006]. Liu expresses that this downsampling to an intermediate frequency, between the ADC oversampled rate and the Nyquist rate, may be advantageous compared to downsampling to the Nyquist rate entirely in one stage. *See id.*, [0020], [0029]-[0030].

205. A POSA therefore would have been motivated to perform first-stage reconstruction/decimation filtering before summing and second-stage reconstruction/decimation filtering after summing, reducing Moquin's summing rate while avoiding full per-channel reconstruction before summation.

206. A POSA would have had a reasonable expectation of success because this Moquin-Swanson-Liu arrangement uses known components for their known functions and provides known benefits: Moquin's oversampled-domain delay elements and beamforming architecture, and Liu's staged reconstruction filters and intermediate-rate multi-bit summer. *See supra* §XI.B.

XII. GROUND 3: CLAIM 10 IS OBVIOUS BASED ON MOQUIN, SWANSON, AND DEAN

207. In my opinion, a POSA would have found claim 10 obvious based on Moquin in view of Swanson and Dean.

A. Motivation to Combine

208. In my opinion, a POSA would have been motivated to combine Moquin and Swanson with Dean to achieve an oversampled beamforming arrangement in which oversampled digital signals are digitized to create multi-bit

deep samples. Such applications may include those where greater per-sample amplitude information, dynamic range, or a lower oversampling-rate/bit-depth tradeoff was desired.

209. As explained for claim 1 above, the Moquin-Swanson combination discloses or suggests a non-transitory computer-readable storage medium storing program code for causing a data processing system to perform steps of oversampled-domain delay and sum beamforming. *Supra* §X.C. Moquin discloses the use of delta-sigma modulators (analog-to-digital converters) that output oversampled single-bit signals and teaches that its beamforming system ultimately outputs an oversampled multi-bit sum. Ex.1006, [0014] (disclosing the formation of a 3-bit word for an 8-element array), Fig.4.

210. Moquin additionally teaches that its core phased array delay-and-sum technology is operable across applications, including in sonar, radar, and ultrasound:

“As one skilled in the art will appreciate, the preferred embodiment is for illustration purposes only and the principles of the invention can be used in any phased array where over-sampling ADCs are used, such as in ultra-sound medical devices, radar, sonar, etc.”

Ex.1006, [0017].

211. Similar to Moquin, Dean discloses a beamforming array for use “in radar applications that used phased array technology.” Ex.1009, Abstract; *see also*

id., 1:10-12 (“In many radar applications there is increasing evidence that the next generation of sensors will use active phased array technology.”).

212. Dean discloses that its beamforming array receives signals from sensor modules and converts these signals to “n-bit” digital signals at an oversampling rate. Ex.1009, Abstract, 1:45-66. Dean discloses that n is less than the number of bits required to represent the full dynamic range of the signal. *Id.*, Abstract, claim 1.

213. Dean further teaches that in high information flow applications, “it is preferable to use a number of bits that is greater than 1.” *Id.*, 3:54-57; *see also id.*, 3:10-30. For such applications, Dean discloses “a noise shaping analogue to digital converter” that includes a sampling loop 24 that outputs “a series of n-bit representations of the signal from the sensor module at an oversampled rate.” *Id.*, 6:17-40, Fig.4.

214. A POSA looking to improve the Moquin-Swanson combination (*supra* §X.C) would have been motivated to implement Moquin’s oversampling analog-to-digital-conversion path using Dean’s noise-shaping analog-to-digital converter, which directly outputs multi-bit samples at an oversampling rate, rather than Moquin’s one-bit delta-sigma output. A POSA would have selected that implementation in higher-information-flow applications, such as radar, when greater per-sample amplitude information, dynamic range, or a different oversampling-rate/bit-depth tradeoff was desired.

B. Reasonable Expectation of Success

215. A POSA would have had a reasonable expectation of success integrating Dean's teachings regarding multi-bit deep digitization into the Moquin-Swanson combination (*supra* §X.C).

216. First, the combination of Moquin and Swanson with Dean addresses the implementation of multi-bit digitizers, which were well-known in the field of beamforming and signal processing long before the earliest claimed priority date. *See, e.g.*, Ex.1023 (J. Yu et al., A low-power multi-bit $\Sigma\Delta$ modulator in 90-nm digital CMOS without DEM, in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2428-2436, Dec. 2005), 1 ("Multi-bit sigma-delta modulators are widely used in analog-to-digital conversion especially in the modern deep-sub-micron CMOS process.").

217. Second, a POSA would have had a reasonable expectation of compatibility between the Moquin-Swanson combination (*supra* §X.C) and Dean's teachings because both Moquin and Dean teach beamforming for use in radar applications that used phased array technology. *See, e.g.*, Ex.1006, [0017] ("the principles of the invention can be used in any phased array where over-sampling ADCs are used, such as in ultra-sound medical devices, radar, sonar, etc."); Ex.1009, Abstract ("A digital beamforming array for use in radar applications and particularly in radar applications that used phased array technology."); *see also id.*,

1:10-12 (“In many radar applications there is increasing evidence that the next generation of sensors will use active phased array technology.”).

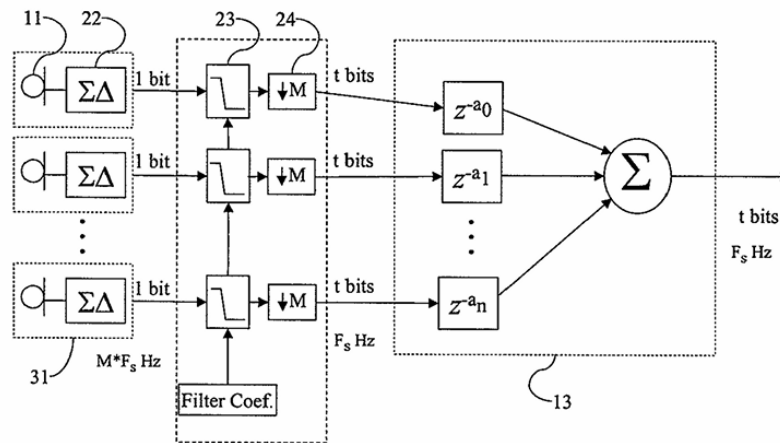
218. Third, both Moquin and Dean teach combining multi-bit signals in their respective beamforming processes. Consider, for example, the below disclosure from Dean:

“In some applications, for example, if a very fast information flow is required. The trade-off between the number of bits in the oversampled domain and the rate of oversampling is such that a lower sampling rate with more bits is preferred. A type of analogue to digital converter with this property is a noise shaping analogue to digital converter, such as is shown in FIG. 4. Such a converter can also be split into a sampling loop 24 and a decimating filter 26 in a similar manner to the sigma delta converter of FIG. 1. The sampling loop 24 comprises a subtraction means 24a, an integrator 24b, an n-bit analogue to digital converter 24c, a latch circuit 24d and a digital to analogue converter 24e, connected in series in a loop. **The output of the latch circuit 24d is a series of n-bit representations of the signal from the sensor module at an oversampled rate. If the first part of a noise shaping analogue to digital converter, the sampling loop 24, is used to produce an output of n-bit data in place of each one of the sampling loops 4₁ to 4_j in the array shown in FIG. 3 then n-bit element shift registers can be used instead of the 1-bit element shift registers 14₁ to 14_j and an n-bit adder can be used in place of the one-bit adder 16.** A suitable decimating filter 26 could then be used to convert the resulting data to the number of bits required to represent the entire dynamic range of the intermediate frequency signal.”

Ex.1009, 6:21-40 (emphasis added); *see also* Ex.1006, Fig.3 (multi-bit (t bits) signals feeding a summer for summation), Ex.1009, claim 1.

219. Fourth, both Moquin and Dean teach delay elements for processing multi-bit signals. *See, e.g.,*

Ex.1006, Fig.3 (showing t bits feeding delay elements $Z^{-a_0}, Z^{-a_1}, \dots Z^{-a_n}$)



Ex.1009, 6:21-40 (emphasis added):

“In some applications, for example, if a very fast information flow is required. The trade-off between the number of bits in the oversampled domain and the rate of oversampling is such that a lower sampling rate with more bits is preferred. A type of analogue to digital converter with this property is a noise shaping analogue to digital converter, such as is shown in FIG. 4. Such a converter can also be split into a sampling loop 24 and a decimating filter 26 in a similar manner to the sigma delta converter of FIG. 1. The sampling loop 24 comprises a subtraction means 24a, an integrator 24b, an n-bit analogue to digital converter 24c, a latch circuit 24d and a digital to analogue converter 24e, connected in series in a loop. The output of the latch circuit 24d is a series of n-bit representations of the signal from the sensor module at an oversampled rate. **If the first part of a noise shaping analogue to digital converter, the sampling loop 24, is used to produce an output of n-bit data in place of each one of the sampling loops 41 to 4j in the array shown in FIG. 3 then n-bit element shift registers can be used instead of the 1-bit element shift registers 141 to 14j and an n-bit adder can be used in place of the one-bit adder 16. A suitable decimating filter 26 could then be used to convert the resulting data to the number of bits required to represent the entire dynamic range of the intermediate frequency signal.”**

220. Fifth, modifying the Moquin-Swanson combination (*supra* §X.C) in view of the teachings of Dean to create multi-bit (n -bit) deep oversampled digital signals would be accomplished using conventional analog-to-digital converters. The modification would also be consistent with the teachings of Dean and with the POSA's understanding that multi-bit digitizers were well-known in the art before the earliest claimed priority date.

221. As such, a POSA would have had a reasonable expectation of success combining the teachings of Dean with the Moquin-Swanson arrangement.

C. Claim 10

- 1. “The non-transitory computer-readable storage medium of claim 7, wherein the first oversampled digital signal is digitized to create samples which are more than one bit deep.”**

222. In my opinion, a POSA would have found claim 10 obvious based on Moquin in view of Swanson and Dean.

223. Claim 10 represents a straightforward combination of well-known elements to achieve well-understood benefits. As a first matter, as explained in the Technical Background section of this declaration, digital beamforming systems which relied on oversampled input signals, followed by various combinations of delays and filters and decimation were well-known and in wide use well before the earliest claimed priority date of the '055 patent. *See supra* §VI. A POSA would have understood that, before that time, different known arrangements of

oversampled ADCs, digital delays, filters/decimators, and combiners involved predictable engineering tradeoffs—including processing rate, memory, circuit complexity, cost, and power—and that selecting an arrangement to meet the input-signal and output-performance requirements was routine design work.

224. As I explained above for claim 7, it is my opinion that a POSA would have found claim 7 obvious based on Moquin in view of Swanson. *Supra* §§X.A-B, G.

225. As I further explained for claim 7 in Ground 1, Moquin and Swanson render obvious delaying the first oversampled digital signal in the oversampled domain and applying low-pass filtering with decimation to output a baseband digital signal delayed by the selected time delay. *Supra* §X.G. In the Figure-3-informed arrangement explained there, the delayed baseband channel signal is then used in the subsequent beamforming/summing processing. Claim 10 further requires that the first oversampled digital signal be digitized into samples more than one bit deep. Dean discloses that feature.

226. Dean discloses a digital beamforming array in which signals from sensor modules are converted to “n-bit” digital signals at an oversampling rate, where n is less than the number of bits required to represent the full dynamic range of the signal:

“The present invention provides a digital beamforming array which enables a significant reduction in complexity and cost and which retains all the advantages of digital beamforming mentioned above.

According to a first aspect of the present invention there is provided a digital beamforming array, comprising;

a plurality of sensor modules for receiving incoming radar signals and converting them to intermediate frequency signals,

a plurality of linear digitising means, one for each module, for converting the intermediate frequency signals to n-bit digital signals at an oversampling rate, where n is less than the number of bits required to represent the dynamic range of the intermediate frequency signal,

a beamforming means, for altering the relative phases of the n-bit signals and combining them to form a resultant digital signal,

and decimating means for converting the resultant digital signal output from the beamforming means to a digital signal of the number of bits required to represent the dynamic range of the intermediate frequency signal.”

Ex.1009, Abstract, 1:45-66, claim 1. Dean explains that in higher-information-flow applications, the tradeoff between bit depth and oversampling rate makes it preferable to use “a number of bits that is greater than 1.” *Id.*, 3:10-30, 3:54-60. Dean further teaches a noise-shaping analog-to-digital converter whose sampling loop outputs “n-bit representations” of the sensor signal at an oversampled rate, and that corresponding n-bit shift registers and an n-bit adder can be used in the beamforming architecture. *Id.*, 6:21-40, Fig.4.

227. A POSA would have been motivated to use Dean’s multi-bit digitizer in Moquin-Swanson’s oversampled beamformer arrangement (*supra* §X.C) in high information flow applications, such as radar, when greater per-sample amplitude

information, dynamic range, or a lower oversampling-rate/bit-depth tradeoff was desired.

228. Moquin discloses oversampled-domain delay-and-sum beamforming using single-bit oversampling ADCs, and its Figure 4 embodiment itself produces a multi-bit oversampled sum—e.g., a 3-bit word for an 8-element array—before filtering/decimation. Ex.1006, [0014]. Moquin also explains that its principles apply to other phased arrays using oversampling ADCs, including ultrasound, radar, and sonar arrays. *Id.*, [0017]. Dean teaches the predictable multi-bit digitizer implementation and corresponding n-bit delay/combining hardware. *See* Ex.1009, 2:63-3:9, 6:21-40, claims 2, 5.

XIII. GROUND 4: CLAIMS 1-5 AND 7-10 ARE OBVIOUS BASED ON LIU

229. In my opinion, a POSA would have found claims 1-5 and 7-10 obvious based on Liu.

230. First, as described above in the Technical Background section, there were many well-known historical examples of digital systems for delay and sum beamforming of signals from microphone arrays, including use of microprocessors that include memory for storing code and that are configured to execute such code, oversampled ADCs for converting analog signals to digital format, and digital signal processors for execution of filtering, delaying, decimating, and combining the signals from a microphone array. *See supra* §VI. A POSA at the time of the

earliest claimed priority date of the '055 patent would have been well-aware of example uses of these elements and the advantages of combining these elements in various ways. All elements of these claims were known long before the earliest claimed priority date of the '055 patent.

A. Motivation for Implementation

231. In my opinion, a POSA would have been motivated to implement Liu's processor-based receive beamformer using a non-transitory computer readable storage medium storing program code for causing Liu's processor-based system to perform the claimed beamforming steps.

232. First, Liu discloses a processor-based beamforming implementation. For example, Liu discloses that its "system 10 for receive beamforming ultrasound information" and related methods may be implemented "using a processor." Ex.1007, [0024] ("**The system 10 is implemented** on one or more integrated circuits.... Other circuit implementations may be provided, such as ... **using a processor,**") (emphasis added), Fig.2.

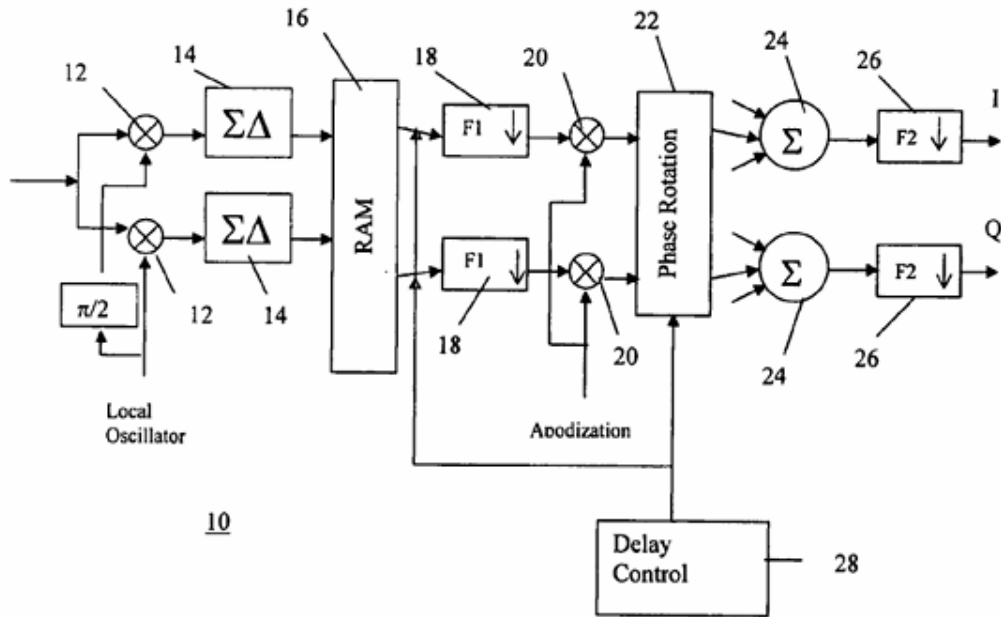


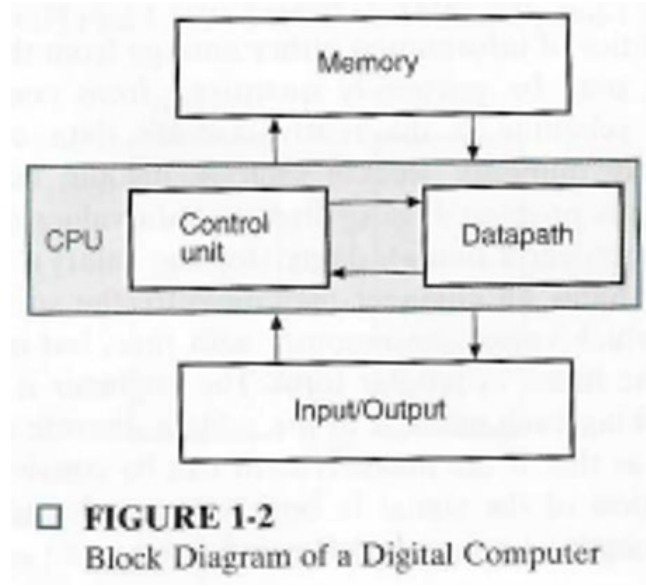
Figure 2

Id., Fig.2; *see also id.*, [0033] (“The delay controller **28** is a processor, control processor, digital signal processor, ...”), [0034] (“The filter **18** is operable to dynamically decimate under control of the dynamic delay controller **28**.”), [0036] (“The multiplier **20** is a[] ... digital processor...”), [0038] (“The summer **24** is a ... digital summer, processor, ...”), [0048] (disclosing that the oversampling rate is “programmable”). Liu’s beamforming methods, which are disclosed with respect to its Figure 7, may be implemented by the system **10** in Figure 2. *See id.*, [0046] (“Fig. 7 shows one embodiment of a method for receive beamforming ultrasound information. The method is implemented by ... the receive beamformer[] of FIG[. 2...”), Fig.7.

233. Liu further teaches that its beamforming implementation may rely on code (e.g., “software”). *See id.*, [0059] (“While the invention has been described above by reference to various embodiments, it should be understood that many changes and modifications can be made without departing from the scope of the invention. As used herein, ‘connected with’ includes direct or indirect connection. For example, one or more hardware or software components may be between two connected components.”).

234. Given the teachings of Liu, a POSA would have been motivated to implement Liu’s processor-based receive beamforming using a non-transitory computer readable storage medium storing program code for causing Liu’s processor-based system to perform the claimed beamforming steps.

235. A POSA would have understood that conventional processors function in part by retrieving code in the form of instructions from memory for performing data-processing operations. *See, e.g.*, Ex.1024 (M. Mano *et al.*, Logic and Computer Design Fundamentals, Prentice Hall, 1997), p.7 (“The control unit in the CPU retrieves the instructions, one by one, from the program stored in the memory.... Both programs and data are stored in memory.”).



Id., Figs.1-2.

236. Liu discusses its processors working in combination with non-transitory memory, e.g., RAM. *See, e.g.*, Ex.1007, [0032] (“Referring again to FIG. 2, the memory **16** is a random access memory,...”), [0033] (“The delay controller **28** is a processor, control processor, digital signal processor, ... memory, or combinations thereof.”), [0034] (“The filter **18** is operable to dynamically decimate under control of the dynamic delay controller **28**.”), [0036] (“The multiplier 20 is a[] ... digital processor...”); Fig.2 (RAM 16).

237. As a POSA would have understood, implementing Liu’s processor-based beamformer using program code (software) stored in conventional non-transitory memory for execution by the disclosed processor, control processor, or digital signal processor would have provided the benefit of flexibility and facilitated the ability to amend or tweak the beamforming-related processing more easily than

if the implementation was hard wired into a fixed integrated circuit. This flexibility would have also resulted in reduced costs over time, as modifications to the beamforming-related processing could be implemented without manufacturing a new chip.

238. Claim 1 is written in computer-readable-medium form. In my opinion, a POSA would not have viewed that form as requiring any unconventional storage-medium technology. Liu expressly contemplates processor-based implementations for its receive beamformer, including a processor, control processor, digital signal processor, memory, RAM 16, processor-implemented filtering/decimation and summing, programmable oversampling-rate control, and software components. *Id.*, [0024], [0032]-[0034], [0036], [0038], [0048], [0059], Figs.2, 7. A POSA implementing those processor-based functions would have used non-transitory memory, such as RAM, ROM, flash, or other conventional physical storage, to store instructions causing the processor/DSP to perform the disclosed oversampling-data handling, delay selection, filtering/decimation, apodization, phase rotation, summing, and beamforming operations. Doing so would have been a routine stored-program implementation of the processor-based architecture that Liu expressly permits, with the expected benefits of programmability, design reuse, and software/firmware updates.

B. Reasonable Expectation of Success

239. In my opinion, a POSA would have had a reasonable expectation of success in implementing Liu's processor-based receive beamformer using a non-transitory computer readable storage medium storing program code for causing Liu's processor-based system to perform the claimed beamforming steps. Liu's teachings provide useful detailed guidance and specific options for the implementation of beamforming in ultrasound imaging applications, in which signals from sensors that respond to analog acoustic fields are digitally sampled, delayed, filtered, decimated and combined in various ways. Those teachings would have provided concrete implementation guidance for programming Liu's processor-based system to carry out the disclosed delay selection, filtering/decimation, and summing operations using conventional processor and memory resources, without requiring more than routine implementation choices by a POSA.

240. The proposed implementation applies Liu's known processor-based beamformer without changing its underlying oversampling, delay selection, reconstruction/decimation, apodization, focusing, or summing operations, and a POSA would have understood that these expressly disclosed operations were conventionally implemented using stored instructions executed by a processor.

241. The proposed implementation presents a predictable application of a known software storage implementation (e.g., RAM memory, as taught by Liu) to

a known digital signal processor-based system (as also taught by Liu) according to their established functions. *See also, e.g.*, Ex.1005, [0054]-[0056], claims 15-20; Ex.1025, [0016]-[0017], [0062], [0064], [0066]-[0068], claims 25-30.

C. Claim 1

1. 1[pre]: “A non-transitory computer-readable storage medium storing program code for causing a data processing system to perform steps comprising:”

242. I have been asked to assume the preamble of claim 1 is limiting. Under that assumption, it is my opinion that examples of a “...non-transitory computer-readable storage medium storing program code for causing a data processing system to perform steps” existed in known prior art for many years prior to the earliest claimed priority date of the '055 patent. For example, a POSA would have found the preamble of claim 1 obvious based on Liu.

243. Before turning to the prior art disclosure, and as discussed above (*supra* §X.C.1), it is my opinion, having reviewed the '055 patent, that the '055 patent does not describe any unique or special technology for claim 1's storage-medium aspect. *See* Ex.1001, 17:62-18:10, 19:4-14. The '055 patent's disclosure, including the above cited excerpts, simply discusses software implementation and machine-readable media in generic, conventional terms, citing as possibilities many known combinations of well-known elements performing expected and well-known functions.

244. In my opinion, that disclosure confirms that the alleged improvement of claim 1 is not limited to or dependent on any particular storage-medium implementation. A POSA would have appreciated that the underlying signal-processing operations disclosed by Liu could be implemented in a broad range of combinations of firmware/software on non-transitory media.

245. Turning to the prior art's disclosure of claim 1, it is my opinion that Liu discloses systems and methods for beamforming. More specifically, Liu discloses "methods, systems, and receive beamformers for receive beamforming ultrasound information." Ex.1007, [0006]. This includes, for example, a system 10 having oversampling converters 14, memory 16, reconstruction filters 18, apodization multipliers 20, phase rotator 22, summer 24, and delay controller 28. *Id.*, [0006], [0022]-[0025]; Fig.2.

246. Liu explains that system 10 may be implemented on one or more integrated circuits, including implementations "using a processor[] or using a field programmable gate array." Ex.1007, [0024]. As further specified, Liu's delay controller 28 may be a "processor," "control processor," "digital signal processor," "application specific integrated circuit," "field programmable gate array," or other circuitry, and it controls output of memory 16 and selects stored data from memory 16 as a function of delay:

“The delay controller **28** is a processor, control processor, digital signal processor, application specific integrated circuit, field programmable gate array, analog circuit, digital circuit, look-up table, memory, or combinations thereof. The controller **28** controls the output of the memory **16**. The controller **28** selects stored data from the memory **16** as a function of a delay for the beam. The controller **28** may include a same or different component for selecting phase rotations associated with the samples for fine focusing with the phase rotator **22**. The selected samples are output to the filter **18**.”

Id., [0033]. Liu further discloses that its summer 24 may also be a “digital summer, processor, digital circuit, or other device for combining digital samples.” *Id.*, [0038].

247. Liu also discloses that its implementation may be in the form of “software.” *See id.*, [0059] (“While the invention has been described above by reference to various embodiments, it should be understood that many changes and modifications can be made without departing from the scope of the invention. As used herein, “connected with” includes direct or indirect connection. For example, one or more hardware or software components may be between two connected components.”).

248. Liu also discloses a receive-beamforming method or sequence that includes, for example, oversampling received signals, relatively delaying samples, partially reconstructing the received signals, summing the delayed/reconstructed

samples, and reconstructing the beam sum. *Id.*, [0032]-[0040], [0046]-[0057], claims 13, 20-23, Figs.2, 7.

249. A POSA would have been motivated to implement Liu's disclosed processor-based receive beamformer using program code stored on a conventional non-transitory computer-readable storage medium for execution by the disclosed processor. Liu expressly identifies processor-based implementations, programmable beamforming functions, memory, and software components, and a stored-program implementation would have been a routine and predictable way to implement and update those functions. *See, e.g.*,

Ex.1007, [0024] (disclosing processor implementation) (emphasis added):

"The system **10** is implemented on one or more integrated circuits. For example, separate chips are provided for groups of channels, such as 16, 128, 256, 512, 1024, or other numbers of channels being implemented on a chip. Cascaded summers may be provided on the same chip, or the summer or summers and downstream components are on one or more different chips. Other circuit implementations may be provided, such as using sequential separation between chips, **using a processor**, or using a field programmable gate array."

Id., [0033] (disclosing processor implementation) (emphasis added):

"**The delay controller 28 is a processor, control processor, digital signal processor**, application specific integrated circuit, field programmable gate array, analog circuit, digital circuit, look-up table, **memory, or combinations thereof**. The controller **28** controls the output of the memory **16**. The controller **28** selects stored data from the memory **16** as a function of a delay for the beam. The controller **28** may include a same or different component for selecting phase rotations associated with the samples for fine focusing

with the phase rotator **22**. The selected samples are output to the filter **18**.”

Id., [0034] (disclosing processor implementation):

“The filter **18** is operable to dynamically decimate under control of the dynamic delay controller **28**.”

Id., [0036] (disclosing processor implementation) (emphasis added):

“The multiplier **20** is an amplifier, **digital processor**, digital circuit, filter, or other device operable to amplify or reduce amplitude of the samples output by the filter **18**. The multiplier **20** applies apodization to the samples. The apodization applied may vary from channel-to-channel and/or depth-to-depth. In alternative embodiments, a subtractor, divider, adder, or other component implements the apodization weighting.”

Id., [0038] (disclosing processor implementation) (emphasis added):

“The summer **24** is a node, **digital summer, processor**, digital circuit, or other device for combining digital samples. The summer **24** sums the relatively apodized and focused signals from a plurality of channels. Multiple input arrows are shown for each summer **24** to reflect inputs from the multiple channels. The summer **24** is a single multiple input summer or a cascade of summers each having two or more inputs. The summer **24** is a multiple bit sample summer, such as summing four or six bit samples.”

See also id., [0048] (disclosing oversampling rate may be programmable). That implementation would have predictably caused Liu’s data-processing system to perform Liu’s disclosed beamforming sequence.

2. 1[a]: “outputting a first oversampled digital signal output from an analog-to-digital converter (ADC), wherein the first oversampled digital signal is responsive to an analog field

and the first oversampled digital signal is created at a sampling clock frequency;”

250. In my opinion, Liu discloses this limitation.

251. As an initial matter, as discussed in the Technical Background section above, beamforming systems that produce oversampled digital signals from received analog signals were widely known and widely used long before the '055 patent's earliest claimed priority date. *See supra* §VI.

252. Liu discloses “oversampling analog-to-digital converters 14.” Ex.1007, [0025]. Liu further explains that converters 14 are “sigma-delta or other converters” that oversample. *Id.*, [0029]-[0030]. More specifically, Liu explains that its converters sample at a rate higher than the Nyquist rate, and that the sampling rate may be “at least 20,” such as “20-200,” times the Nyquist rate. *Id.*, [0029]-[0030]. Liu additionally explains that, in act 72, “sigma-delta analog-to-digital converters oversample,” and “[t]he oversampling converts the received signals into digital samples.” *Id.*, [0048], Figs.2, 7.⁴ Thus, it is my opinion that Liu

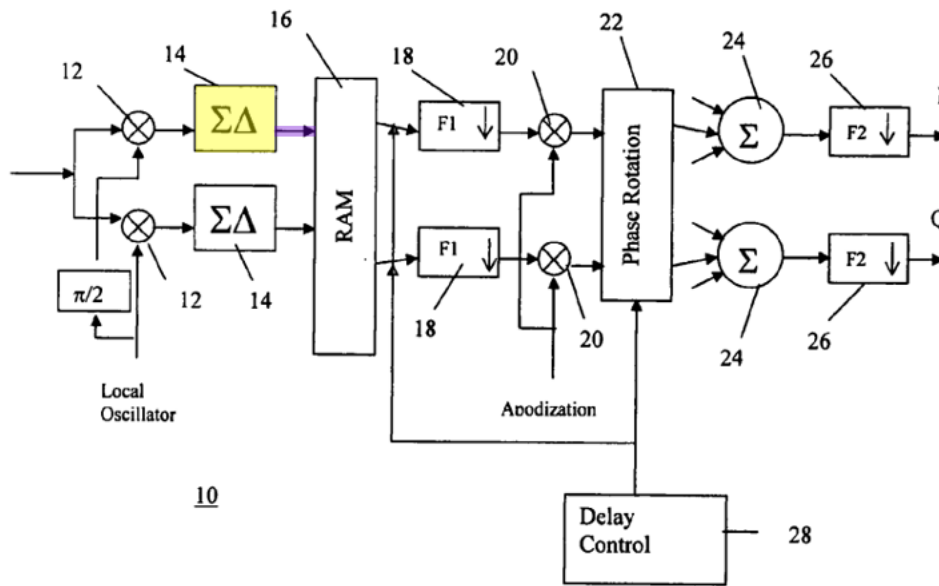
⁴ Liu's beamforming methods, which are disclosed with respect to Figure 7 of Liu, may be implemented by the system 10 in Figure 2. *See* Ex.1007, [0046] (“Fig. 7 shows one embodiment of a method for receive beamforming ultrasound information. The method is implemented by ... the receive beamformer[] of FIG[. 2...”), Fig.7.

discloses outputting a first oversampled digital signal from an analog-to-digital converter (ADC), for example, in the form of one of the oversampled digital signal streams that is output by the converter 14, where the oversampled digital signal is created at a sampling clock frequency, which is a rate higher than the Nyquist rate, and may be “at least 20,” such as “20-200,” times the Nyquist rate.

253. Liu further discloses that this oversampled digital signal output from its ADC is responsive to an analog field. This is understood from the fact that Liu’s system is directed to “receive beam forming ultrasound information,” and Liu explains that its method oversamples “signals received from a transducer element” and “converts the received signals into digital samples.” *Id.*, [0006], [0022]-[0025], [0046]-[0048], Figs.2, 7. A POSA would have understood that “ultrasound” describes analog amplitude acoustic waves propagating through a sample, and that the arrival of these waves at the “transducer” produces analog oscillating forces on the transducer that are converted to analog oscillating analog voltages or currents. These analog electrical signals are converted to digital signals by the ADC in Liu. The fact that Liu uses an ADC supports that the received signal is an analog signal. Further, this analog signal is produced from the sensing of an analog field by a transducer. More specifically, in Liu’s system, a transducer element receives the incident ultrasound/acoustic field and produces an analog receive signal in response to that field. In Liu’s Figure 2 embodiment, analog mixers 12 mix that received

signal with a local oscillation signal to provide I/Q signals at baseband or an intermediate frequency, and converters 14 then oversample those analog I/Q signals. *Id.*, [0026]-[0027], [0047]-[0048], Figs.2, 7. A POSA would have understood that this analog mixing does not break the responsiveness to the analog field. In other words, the mixed I/Q signals remain analog signals derived from, and which preserve information from, the received ultrasound signal pertaining to that ultrasound/acoustic field. Thus, it is my opinion that the analog-to-digital converter 14 (ADC) outputs oversampled digital samples responsive to the incident ultrasound/acoustic field. Liu additionally discloses an alternative embodiment in which the analog mixers are not provided (*id.*, [0028]), in which the incoming RF is oversampled, further confirming that Liu discloses an oversampling converter output that is responsive to the received ultrasound signal pertaining to that ultrasound/acoustic field. *See id.*, [0028].

254. Liu's Figure 2 illustrates converter 14 as the ADC (yellow) and shows its oversampled digital output signal (purple) provided to memory 16:



Id., Fig.2. Liu discloses that its system may be implemented using a processor. *See, e.g., id.*, [0024]; *see also id.*, [0033], [0034], [0036], [0038], [0048]. Liu further discloses that its implementation may be in the form of “software.” *See id.*, [0059].

3. 1[b]: “delaying the first oversampled digital signal by a time delay wherein the time delay is equal to an integer number of sampling clock cycles to produce a time delayed first oversampled digital signal; and”

255. In my opinion, Liu discloses, or at least renders obvious, this limitation.

256. As an initial matter, as discussed in the Technical Background section in this declaration, the use of a time delay that is equal to an integer number of cycles of the sampling clock to produce a time-delayed oversampled signal was widely known and broadly used well before the earliest claimed priority date of the ’055 patent. *See supra* §VI.

257. Liu states that in “beamforming, dynamic receive focusing requires that channel signals be relatively delayed for coherent summation.” Ex.1007, [0004]. And in terms of implementation, Liu further states that “[d]elays are implemented by selecting data from the sample stream.” *Id.*, Abstract.

258. Liu’s method performs this delaying on oversampled received signals. More specifically, Liu discloses performing “Oversampling Received Signals” in act 72, and then “Relatively Delaying Samples” in act 74. *Id.*, [0048]-[0049], Fig.7. Only afterwards does Liu perform “Partially Reconstructing Received Signals” in act 76. *Id.*, [0052], Fig.7; *see also id.*, [0048]-[0052].⁵ Thus, it is my opinion that Liu discloses delaying the oversampled digital signal itself to produce a time-delayed oversampled digital signal.

259. Liu further explains how the delay is implemented. Converter 14 outputs oversampled digital samples:

“The oversampling converters **14** are sigma-delta or other converters operable to sample higher than the Nyquist rate (e.g., two or more

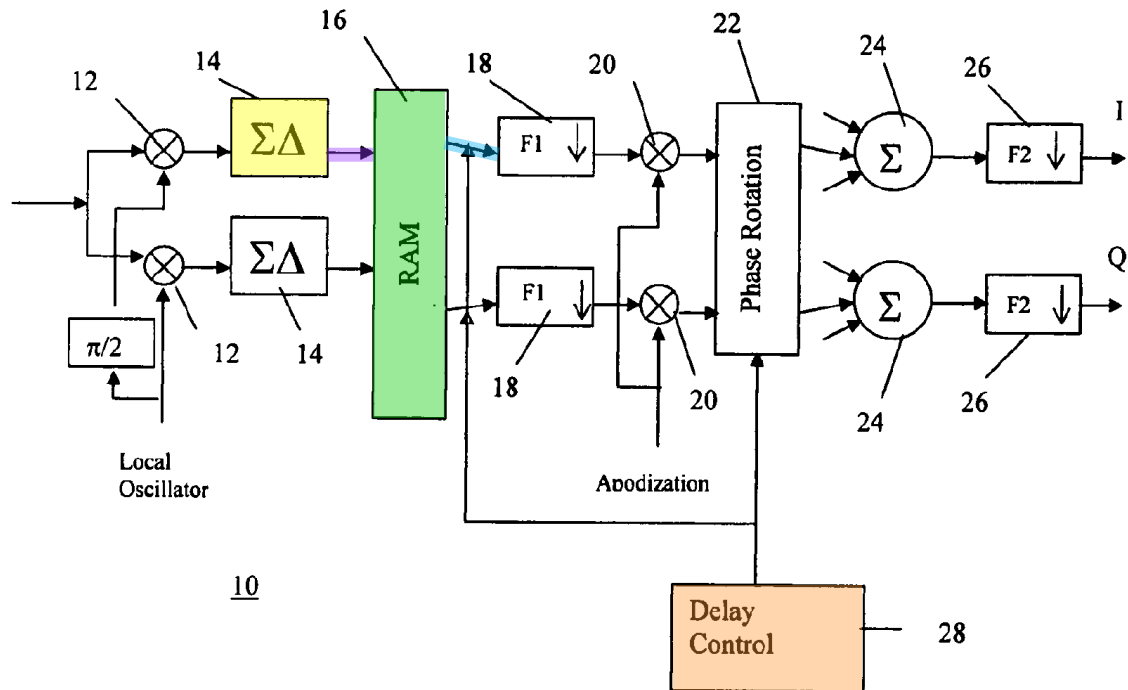
⁵ Liu’s beamforming methods, which are disclosed with respect to Figure 7 of Liu, may be implemented by the system 10 in Figure 2. *See* Ex.1007, [0046] (“Fig. 7 shows one embodiment of a method for receive beamforming ultrasound information. The method is implemented by ... the receive beamformer[] of FIG[. 2...”), Fig.7.

times higher). The oversampling converters **14** are first, second, or higher order converters. For example, a second order converter **14** with two integrators is provided for higher dynamic range. In one embodiment, a 2nd order 240 MHz sampling converter **14** is provided with single bit quantization. In another embodiment, a 1st order 480 MHz sampling converter is provided with single bit quantization. Since base band signals are being sampled in the embodiment of FIG. 2, the converters **14** are low-pass converters. Other oversampling converters may be used. Two converters **14** are provided in each receive channel, one for each of the IQ signals.

In oversampling converters **14**, such as a sigma-delta converter, high dynamic range is achieved by using low-bit-width, high sampling rate, and noise shaping by which the noise energy is pushed away in spectrum from the signal bandwidth. The sampling rate is much higher compared to the Nyquist rate. The Nyquist rate is based on the center frequency of the received signals, such as a center frequency of 1-20 MHz. The converter **14** outputs samples at a rate at least 20, such as 20-200, times the Nyquist rate. The sampling bit width is low, such as one bit. Higher bit widths, such as two, four, or more, may be provided. The converters **14** shape quantization noise and filter to maximize in-band SNR based on the nature of the conversion.”

Id., [0029]-[0030]. Memory 16 “receives samples at the oversampling rate,” stores those samples, and “includes sufficient memory slots to provide the needed delay range.” *Id.*, [0032]. Liu discloses that “memory 16 is a random access memory, buffer, shift register, or other memory.” *Id.* Delay controller 28 “controls the output of the memory 16” and “selects stored data from the memory 16 as a function of a delay for the beam,” with the selected samples then being output to filter 18. *Id.*, [0033]-[0034]. Figure 2 depicts this arrangement, with converter 14 (yellow) outputting oversampled samples (purple) to memory 16 (green), delay controller 28

(orange) controlling delay selection, and selected samples (blue) being output from memory 16 toward filter 18:



Id., Fig.2. Accordingly, Liu discloses delaying the first oversampled digital signal (e.g., output from analog-to-digital converter 14 stored in memory 16) by a time delay to produce a time-delayed first oversampled digital signal (e.g., selected output from memory 16).

260. The delaying implementation is through the control of the delay controller, which is disclosed to be implemented by a processor. *See id.*, [0033] (“The delay controller 28 is a processor, control processor, digital signal processor, ... memory, or combinations thereof. The controller 28 controls the

output of the memory 16. The controller 28 selects stored data from the memory 16 as a function of a delay for the beam . . .The selected samples are output to the filter 18.”) (emphasis added); *see also id.*, [0024], [0034], [0036], [0038], [0048], [0059].

261. In terms of the delays that may be provided, Liu discloses that the delay is equal to an integer number of sampling clock cycles. Liu discloses that converter 14 outputs samples at an oversampling rate, e.g., “at least 20, such as 20-200, times the Nyquist rate,” with example sampling rates of 240 MHz and 480 MHz. *Id.*, [0029]-[0030]. Liu further discloses that those signals at that sampling frequency are what is delayed. *Id.*, [0032]. Because memory 16 receives and stores those samples at that oversampling rate, and delay controller 28 imposes delay by selecting samples from that stored sample stream as a function of beam delay, Liu’s memory-based delay is implemented in discrete increments of the oversampling sample period. *See id.*, [0049]:

“In act 74, the oversampled signals are relatively delayed. A same or different delay is provided for each channel. The focusing profile for steering the beam and determining a focal region dynamically along the beam indicates the desired delay for a given channel. Two or more channels may have a same delay. Since the oversampled signals are provided as a function of time, the samples to be used for a given range are selected as a function of the delay. Earlier or later occurring samples are selected. A buffer or other memory may be used to provide for selecting based on the delay. Any number of samples may be selected for a given delay, such as tens or hundreds.”); *see also id.*, [0032]-[0033], [0051]. In other words, selecting a sample shifted by k

sample positions imposes a delay of k oversampling sample periods, i.e., an integer number of converter sampling-clock cycles.”

262. Liu’s disclosure that memory 16 may be implemented as a “shift register” further confirms this understanding. *See id.*, [0032]. A POSA would have understood that selecting an output from a shift register used as sample memory likewise provides delay in integer sample-clock increments. *See, e.g.*, Exs.1013-1014 (defining “shift register”); *see also supra* §X.C.3 (same). That is because a shift register advances stored samples by one register stage on each sampling-clock cycle, so a sample read from the N th stage or tap is the same sample delayed by N sampling-clock cycles.

4. 1[c]: “combining the time delayed first oversampled digital signal with a second oversampled digital signal to obtain the beamformed digital signal, wherein the second oversampled digital signal is responsive to the analog field.”

263. It is my opinion that Liu discloses this limitation.

264. As a first matter, combining a delayed signal with another signal to form a beamformed signal responsive to an analog field was not new at the time of the earliest claimed priority date of the ’055 patent. As discussed in the Technical Background section, combinations of signals with delays to produce beamformed signals was well established and widely-used long before the earliest claimed priority date of the ’055 patent. *See supra* §VI. More recent combinations of oversampled digital signals responsive to analog fields emerged later, along with

the emergence of digital signal processing, but even these combinations existed well before the '055 patent.

265. Liu's receive beamformer "includes a plurality of receive channels," and "[e]ach channel corresponds to one or more elements." Ex.1007, [0023]. Figure 2 shows one such channel, and Liu explains that "[t]he other channels have the same or different components," including "the oversampling analog-to-digital converters 14." *Id.*, [0025]. Thus, Liu discloses multiple signals, including for example, a first signal on one channel, and additional signals on other channels.

266. Second, Liu further discloses, in act 72, that "the received signals in each channel are oversampled" and that "[t]he oversampling converts the received signals into digital samples." *Id.*, [0048], Fig.7.⁶ In other words, the first channel's oversampling analog-to-digital converter outputs a first oversampled digital signal. The signals on each other channel are also converted to an oversampled digital signal by their respective analog-to-digital converter 14. Thus, it is my opinion that

⁶ Liu's beamforming methods, which are disclosed with respect to Figure 7 of Liu, may be implemented by the system 10 in Figure 2. *See* Ex.1007, [0046] ("Fig. 7 shows one embodiment of a method for receive beamforming ultrasound information. The method is implemented by ... the receive beamformer[] of FIG[. 2..."), Fig.7.

Liu discloses at least first and second oversampled digital signals that are generated in respective receive channels. *See id.*, [0022]-[0023], [0047]-[0048].

267. Third, as I also explained for 1[a] above, Liu discloses that the oversampled digital signal output from each ADC is responsive to an analog field. *See supra* §XIII.C.2. This is the case for each ADC's output on each channel. Thus, it is my opinion that Liu discloses first and second oversampled digital signals generated in respective receive channels, each responsive to the received ultrasound/acoustic field through the corresponding transducer element(s). *See also* Ex.1007, [0022]-[0023], [0047]-[0048].

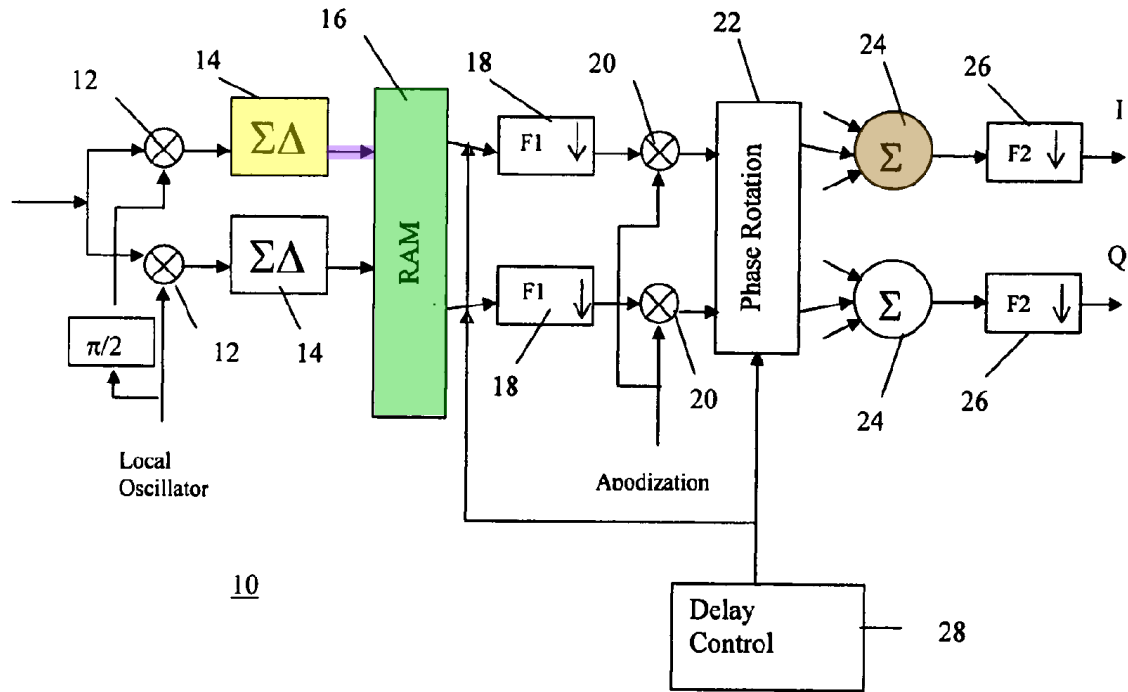
268. Fourth, Liu's summer 24 combines downstream channel signals respectively derived from the time-delayed first oversampled digital signal and the second oversampled digital signal. As I explained for 1[b] above, Liu discloses delaying oversampled channel samples by selecting data from the stored sample stream as a function of beam delay. *Supra* §XIII.C.3; *see also* Ex.1007, [0049], [0032]-[0033]; Figs.2, 7. Filter 18 then partially reconstructs/decimates the selected samples before summation, while maintaining a rate "still oversampled relative to the Nyquist rate." Ex.1007, [0035], [0052], Figs.2, 7.

269. Liu provides additional details on the combining operation. For example, Liu discloses that "[t]he data from the channels is summed to form data representing a beam or sub-array beam." *Id.*, [0023]. Specifically, "summer 24

sums the respectively apodized and focused signals from a plurality of channels,” and Figure 2 illustrates multiple input arrows for each summer 24 “to reflect inputs from the multiple channels.” *Id.*, [0038], Figs.2, 7. Liu also states that in act 80, “[t]he samples from the different channels are summed,” and that “[b]y summing focused samples from the different channels...a beam sum is formed.” *Id.*, [0055]-[0056]; Figs.2, 7.

270. Liu’s intervening apodization and phase/focusing operations likewise occur in those downstream channel paths before summation. Thus, summer 24 combines downstream channel signals respectively derived from the time-delayed first oversampled digital signal with a second oversampled digital signal to obtain a beam sum. *Id.*, [0023], [0037]-[0038], [0054]-[0056].

271. Liu also illustrated such details by way of Figure 2, which shows converter 14 (yellow) outputting oversampled samples (purple) to memory 16 (green), delay controller 28 (orange) controlling delay selection, and summer 24 (tan) combining signals from multiple channels:



Id., Fig.2.

272. Liu's beam sum—i.e., the output of summer 24 produced by summing signals from different channels—and the further-filtered output produced from that beam sum, correspond to the claimed beamformed digital signal obtained by the recited combining. *See also id.*, [0039] (“The summed signal is further filtered...to produce the beamforming output.”), [0019] (“beam sum” formed by summing across channels). A POSA would have understood that the “summer” disclosed by Liu, like the addition and subtraction elements in many prior-art “delay and sum” beamformers, is a “combiner.”

273. The combining operation is further disclosed to be implemented by processor. *See id.*, [0038] (“The summer **24** is a node, **digital summer, processor,**

digital circuit, or other device for combining digital samples.”) (emphasis added); *see also id.*, [0024], [0033], [0036], [0048], [0059].

274. Thus, a POSA would have found claim 1 obvious.

D. Claim 2

1. “The non-transistory [sic] computer-readable storage medium of claim 1, wherein the combining is performed in an oversampled signal domain.”

275. In my opinion, a POSA would have found claim 2 obvious based on Liu.

276. As I explained above for claim 1, it is my opinion that a POSA would have found claim 1 obvious based on Liu. *Supra* §§XIII.A-C.

277. Further, as I mentioned above, oversampled digital beamformers were well-established well before the earliest claimed priority date of the '055 patent, and this included implementations with combining of oversampled signals. Claim 2 represents a straightforward combination of well-known elements to achieve well-understood benefits.

278. As I also explained for 1[c] above, Liu's summer 24 combines downstream channel signals derived from the time-delayed first oversampled digital signal and the second oversampled digital signal. *Supra* §XIII.C.4. Those downstream signals remain oversampled because, in Liu's staged-reconstruction embodiment, filter 18 partially reconstructs the selected samples to a lower rate that

is “still oversampled relative to the Nyquist rate,” and outputs signals “oversampled less than output by the oversampling converters 14 and more than output by the second filter 26”:

“In act 76, the selected samples are partially reconstructed. Partial refers to the reconstruction to a lower rate still oversampled relative to the Nyquist rate. The reconstruction is performed by filtering and/or decimating. The filtering may provide for decimating. Filtering combines information. By combining information, a lesser number of samples may be output. Any decimation rate may be provided, such as by a factor of three or more but less than the oversampling ratio of the converters. Finite or infinite impulse response filtering may be used. Since one filter is provided for each channel, to support a large number of channels on a device, the filter may be kept as simple and compact as possible. For example, the comb filter structure is used. More complex filters may be provided.”

“The filter 18 partially reconstructs the samples. The filter 18 reduces the incoming samples in rate, such as by decimation. Any decimation scale may be used, such as reducing the rate to a half, a quarter, an eighth or more. The filter 18 may increase the samples in bit width, such as by combination in filtering. Any increase in bit width may be used, such as changing from one bit to three, four, five, six, or more bit samples. For example, the filter 18 outputs signals oversampled less than output by the oversampling converters 14 and more than output by the second filter 26. The filter 18 outputs signals with a bit width greater than output by the oversampling converters 14 and less than output by the second filter 26. The beam sum is computed at a high rate but using only a few bits as compared to Nyquist sampling. To improve digitization accuracy or for other purposes such as channel-wise decoding of coded-excitation, the filters 18 are cascaded with additional filters for each channel.”

Ex.1007, [0052], [0035], Fig.7. Additionally, Liu then states that, in act 80, summation is performed “at a data rate less than output by the initial oversampling

and greater than the Nyquist rate or other rate above the Nyquist rate.” *Id.*, [0055], Fig.7. After summation, the rate is decimated in act 82 “to the Nyquist sampling rate or other rate higher than the Nyquist rate.” *See* Ex.1007, [0057] (“In act 82, the beam sum samples are reconstructed.... In one embodiment, the decimation reduces the data rate substantially to the Nyquist sampling rate or other rate higher than the Nyquist rate.”), [0035] (“In one embodiment, the decimation scale is set to provide samples substantially at the Nyquist rate. In alternative embodiments, rates greater than the Nyquist rate may be used.”). Thus, while summation may be performed at a data rate that is less than the initial oversampling rate, a POSA would understand that the summation rate that is “greater than the Nyquist rate or other rate above the Nyquist rate” is a summation performed at an oversampled rate and in an oversampled signal domain.

279. Thus, it is my opinion that Liu’s summer 24 combines signals derived from the delayed channel samples before final reconstruction/decimation while those signals are still oversampled.

E. Claim 3

1. **“The non-transitory computer-readable storage medium of claim 1, wherein the combining is performed at an intermediate sampling rate.”**

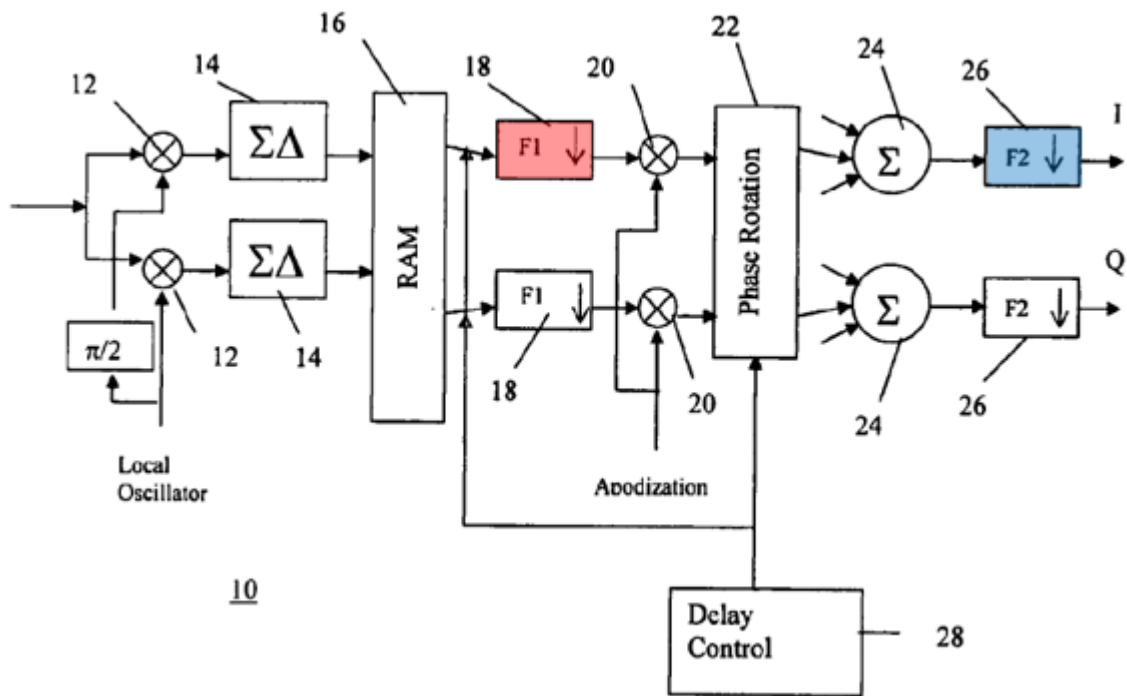
280. In my opinion, a POSA would have found claim 3 obvious based on Liu.

281. As I explained above for claim 1, it is my opinion that a POSA would have found claim 1 obvious based on Liu. *Supra* §§XIII.A-C.

282. As an initial matter, as discussed in the Technical Background section in this declaration, digital beamforming systems which relied on oversampled input signals, followed by various combinations of delays and filters and decimation were well-known and in wide use well before the earliest claimed priority date of the '055 patent. *See supra* §VI. Thus, by that time, it was known that there were benefits to various combinations of these elements depending on the capabilities of each element, the characteristics of the incoming signals, and the requirements for the resulting combined signals. Thus, claim 3 represents a straightforward combination of well-known elements to achieve well-understood benefits. Moreover, cost and power constraints would have motivated a POSA to select and combine these known signal-processing elements—such as oversampled ADCs, digital delays, filters/decimators, and combiners—in such a configuration that provided the desired beamforming performance while avoiding unnecessary processing, memory, and circuit overhead.

283. As I also explained for 1[c] above, Liu discloses combining downstream channel signals at summer 24 to form a beam sum. *Supra* §XIII.C.4. In Liu's Figure 2 embodiment, after delay selection from memory 16, the channel signals are partially reconstructed/decimated by filter 18 (red) and then combined

at summer 24 before second filter 26 (blue) further reconstructs/decimates the beam sum. *See* Ex.1007, [0033]-[0040], Figs.2, 7.⁷



Id., Fig.2.

284. Liu explains that “filter 18 outputs signals oversampled less than output by the oversampling converters 14 and more than output by the second filter

⁷ Liu’s beamforming methods, which are disclosed with respect to Figure 7 of Liu, may be implemented by the system 10 in Figure 2. *See* Ex.1007, [0046] (“Fig. 7 shows one embodiment of a method for receive beamforming ultrasound information. The method is implemented by ... the receive beamformer[] of FIG[. 2...”), Fig.7.

26.” *Id.*, [0035]. Liu further states that summation is performed “at a data rate less than output by the initial oversampling and greater than the Nyquist rate or other rate above the Nyquist rate,” and that later reconstruction reduces the beam-sum data rate. *Id.*, [0055]-[0057]. Thus, it is my opinion that the signals combined at summer 24 are at a rate between the initial oversampling-converter rate and the later post-summation output rate, i.e., at an intermediate sampling rate.

F. Claim 4

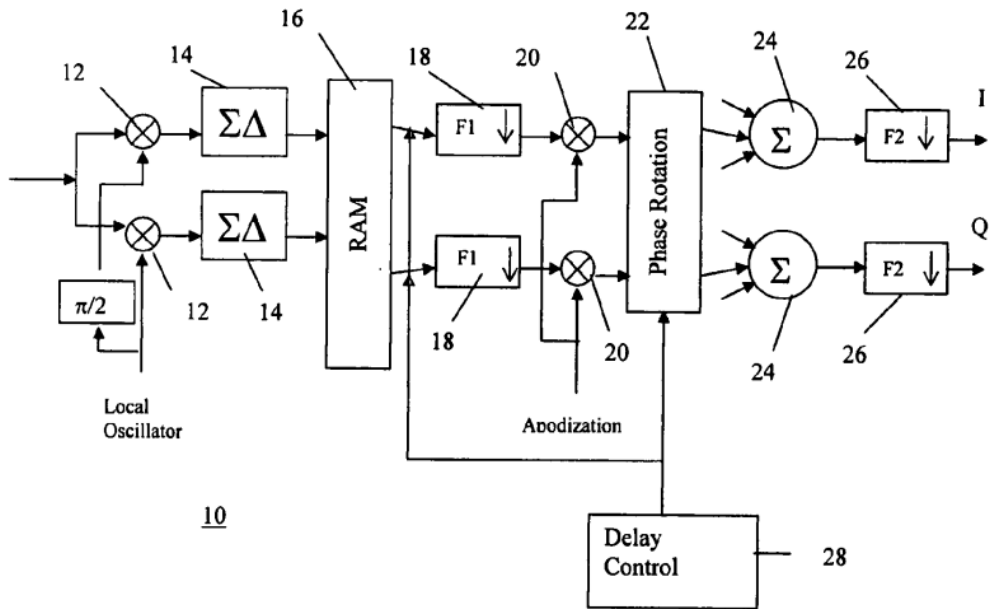
1. “The non-transitory computer-readable storage medium of claim 1, wherein the combining is performed in a baseband signal domain.”

285. In my opinion, a POSA would have found claim 4 obvious based on Liu.

286. As I explained above for claim 1, it is my opinion that a POSA would have found claim 1 obvious based on Liu. *Supra* §§XIII.A-C.

287. Further, as I mentioned above, oversampled digital beamformers were well-established long before the earliest claimed priority date of the ’055 patent. Thus, claim 4 represents a straightforward combination of well-known elements to achieve well-understood benefits.

288. Liu identifies Figure 2 as a “base band receive beamformer system.” Ex.1007, [0013].



Id., Fig.2.

289. In that embodiment, analog mixers 12 provide in-phase and quadrature (I/Q) signals “at a base band frequency for base band beamforming,” and Liu explains that “base band signals are being sampled in the embodiment of FIG. 2.” *Id.*, [0026], [0029]; *see also id.*, [0047] (mixing received signals “to base band”). Those I/Q signals, which Liu characterizes as baseband, are oversampled, delayed by memory 16/delay controller 28, partially reconstructed/decimated by filter 18, and summed by summer 24. *Id.*, [0035], [0038], Fig.2. To the extent Solos asserts that “baseband signal domain” encompasses baseband-frequency I/Q signals represented at an oversampled or intermediate rate, it is my opinion that Liu discloses claim 4 because summer 24 combines those signals.

290. In any event, it is my opinion that Liu also renders claim 4 obvious if “baseband signal domain” requires final-rate channel demodulation/reconstruction before summation. Liu discloses a selectable architecture in which “complete channel demodulation is provided by long low-pass filters for each channel and the beam sum is computed at the signal Nyquist rate.” *Id.*, [0020]. That option sums fully reconstructed baseband channel samples.

291. A POSA would have been motivated to use this Liu-disclosed option when fully reconstructed baseband-rate combining was desired and when the associated filter-length/cost tradeoff was acceptable. Although Liu notes that this option can be more complex for parallel beamforming, Liu identifies it as a known architecture and contrasts it with architectures with no channel demodulation, which can lead to dynamic receive artifacts. *Id.*, [0020]. Liu also contrasts this known architecture with another extreme that Liu discloses can lead to dynamic receive artifacts. *Id.* Implementing Liu’s complete-demodulation option would have predictably preserved Liu’s delay selection from the oversampled sample stream while causing the selected channel signals to be reconstructed/demodulated before summation. *See also id.*, [0019], [0049]-[0056].

G. Claim 5

- 1. “The non-transitory computer-readable storage medium of claim 1, wherein the first oversampled digital signal and**

the second oversampled digital signal are obtained from different sensors.”

292. In my opinion, a POSA would have found claim 5 obvious based on Liu.

293. As I explained above for claim 1, it is my opinion that a POSA would have found claim 1 obvious based on Liu. *Supra* §§XIII.A-C.

294. Further, as I mentioned above, oversampled digital beamformers were well-established long before the earliest claimed priority date of the '055 patent, and this included implementations with two or more distinct microphones. Thus, claim 5 represents a straightforward combination of well-known elements to achieve well-understood benefits.

295. As I also explained for claim 1[c] above, Liu discloses first and second oversampled digital signals in two of its receive channels and combines downstream channel signals respectively derived from those signals at summer 24. *Supra* §XIII.C.4. In fact, Liu's receive beamformer includes “a plurality of receive channels,” each of which “corresponds to one or more elements.” Ex.1007, [0023], [0047] (“transducer element”). Liu additionally explains that “[t]he other channels have the same or different components,” including oversampling converters 14, and that “the received signals in each channel are oversampled.” *Id.*, [0025], [0048].

296. Thus, it is my opinion that Liu's first and second oversampled digital signals are obtained from different transducer elements/sensors, e.g., different receive channels associated with different ultrasound transducer element(s).

H. Claim 7

1. **"The non-transitory computer-readable storage medium of claim 1, further comprising: applying a low pass filter with decimation to the time delayed first oversampled digital signal to output a baseband digital signal that is delayed by the time delay."**

297. In my opinion, a POSA would have found claim 7 obvious based on Liu.

298. As a first matter and as explained in the Technical Background section in this declaration, digital beamforming systems that used combinations of oversampling, delaying, filtering, decimation and combiners were well established long before the earliest claimed priority date of the '055 patent. *See supra* §VI. Thus, claim 7 represents a straightforward combination of well-known elements to achieve well-understood benefits.

299. As I explained above for claim 1, it is my opinion that a POSA would have found claim 1 obvious based on Liu. *Supra* §§XIII.A-C.

300. As I also explained for 1[b] above, Liu discloses that memory 16 and delay controller 28 delay the oversampled digital signal by storing samples at the

oversampling rate and selecting stored data as a function of beam delay for output to filter 18. *Supra* §XIII.C.3.

301. Liu's filter 18 performs decimation. Liu identifies filter 18 as a reconstruction/decimation filter and states that the filter reconstructs selected samples "by filtering and/or decimating." Ex.1007, [0052]; *see also id.*, [0034] ("The filter 18 is a reconstruction filter or other circuit operable as a decimation circuit.... The filter 18 is operable to dynamically decimate under control of the dynamic delay controller 28."), [0035] ("The filter 18 partially reconstructs the samples. The filter 18 reduces the incoming samples in rate, such as by decimation."), [0052] ("In act 76, the selected samples are partially reconstructed.... The reconstruction is performed by filtering and/or decimating. The filtering may provide for decimating. Filtering combines information.... Any decimation rate may be provided, such as by a factor of three or more but less than the oversampling ratio of the converters. Finite or infinite impulse response filtering may be used. Since one filter is provided for each channel, to support a large number of channels on a device, the filter may be kept as simple and compact as possible. For example, the comb filter structure is used....").

302. Liu further discloses that filter 18 is a low pass filter. For example, Liu expressly describes a "first low pass filter" that constructs higher-bit-width samples from the converter output. *Id.*, [0009] ("a first low pass filter operable to

construct first samples with a greater bit width than output from the converter”),
[0009], claims 21, 23.

303. Furthermore, a POSA would have understood that filter 18 is a low-pass filter because the filter must pass the desired relatively low frequency in-band signal and attenuate higher-frequency components in the signal, including out-of-band quantization noise, before reducing the sample rate to F_s . *See, e.g.*, Ex.1022 (G. Moon et al., Design Approach for Decimation Filter for ADC Application, Int’l J. of Eng. Trends and Techn. (IJETT), vol. 10 no. 12 (2014)) at p. 1 (“Decimation is the process of reducing the sampling rate. In practice, this usually implies low-pass filtering a signal, then throwing away some of its samples.”), *id.* (“The main task of a decimation filter is to remove the quantization noise away from the band of interest and avoid aliasing of high frequency components down to low frequency region or within the signal bandwidth.”); Ex.1021 (L. Milic, Multirate Filters: An Overview, *APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, 2006, pp. 912-915), at p. 1 (“The use of an appropriate filter enables one to convert a digital signal of a specified sampling rate into another signal with the desired sampling rate without significantly destroying the signal components of interest.”); *id.* (“Decimating the sampling rate by an integer factor of M means that among the input samples, ... only every M th sample are used as in

the output sequence. For avoiding aliasing, there is a need to use a low-pass anti-aliasing filter before down-sampler....”).

304. To the extent Solos asserts that a partially reconstructed and decimated baseband-frequency I/Q signal constitutes a “baseband digital signal,” it is my opinion that filter 18 outputs such a signal delayed by the selected time delay. Liu identifies Figure 2 as a “base band receive beam former system,” explains that analog mixers 12 provide I/Q signals “at a base band frequency for base band beam forming,” and also states that “base band signals are being sampled in the embodiment of FIG. 2.” Ex.1007, [0013], [0026], [0029]; *see also id.*, [0047]. Because converters 14 oversample those baseband I/Q signals and filter 18 filters/decimates the delayed samples selected from memory 16, filter 18 outputs delayed, lower-rate baseband I/Q channel data. *Id.*, [0035], [0052], Fig.2. That output remains delayed because filter 18 operates on the already-selected delayed samples.

305. Under that interpretation, Liu’s use of filter 26 in its staged embodiment does not change the mapping. Liu discloses reconstructing in stages: filter 18 partially reconstructs and decimates the delayed channel samples, and filter 26 later further reconstructs/decimates the already-summed beam signal. *Id.*, Abstract, [0006], [0035], [0039]-[0040], [0052], [0057]. Thus, the later second-

stage filtering does not alter that filter 18 has already output the delayed, lower-rate baseband I/Q channel data described above.

306. In any event, it is my opinion that Liu also renders claim 7 obvious if the claim requires a fully reconstructed baseband-rate output, for the reasons explained for claim 4. Liu discloses a selectable architecture in which “complete channel demodulation is provided by long low-pass filters for each channel and the beam sum is computed at the signal Nyquist rate.” *Id.*, [0020]. In this Liu-disclosed option, the selected delayed channel samples are fully demodulated/reconstructed by per-channel low-pass filtering with decimation before summation, thereby outputting a delayed baseband digital signal.

307. A POSA would have been motivated to use Liu’s complete-demodulation option when fully reconstructed baseband channel data was desired and the associated filter-length/cost tradeoff, including any parallel beamforming implementation cost, was acceptable. Those circumstances would include implementations not using parallel beamforming, as well as implementations in which the cost of duplicating or time-multiplexing the long per-channel filters was acceptable. While Liu acknowledges that this option can be more complex for parallel beamforming, Liu identifies it as a known architecture and contrasts it with architectures with no channel demodulation, which Liu expresses can lead to dynamic receive artifacts. *Id.* Thus, it is my opinion that Liu’s discussion reflects

a known design tradeoff, not inoperability or a reason a POSA would have avoided the option in suitable designs.

I. Claims 8-9

- 1. Claim 8: “The non-transitory computer-readable storage medium of claim 7, wherein the time delay is equal to a fraction of a baseband sampling period.”**
- 2. Claim 9: “The non-transitory computer-readable storage medium of claim 7, wherein the time delay is greater than a baseband sampling period.”**

308. In my opinion, a POSA would have found claims 8-9 obvious based on Liu.

309. As an initial matter, as discussed in the Technical Background section in this declaration, digital beamforming systems which relied on oversampled input signals, followed by delays and filters and decimation were well-known and in wide use long before the earliest claimed priority date of the '055 patent. *See supra* §VI. Thus, claims 8 and 9 represent straightforward combinations of well-known elements to achieve well-understood benefits.

310. As I explained above for claim 7, it is my opinion that a POSA would have found claim 7 obvious based on Liu. *Supra* §XIII.H.

311. As I explained for 1[b] above, Liu delays the oversampled digital signal by storing samples at the oversampling rate in memory 16 and selecting stored data as a function of beam delay. *Supra* §XIII.C.3.

312. The '055 patent describes the relevant relationships recited in claim 8 (“time delay is equal to a fraction of a baseband sampling period”) and in claim 9 (“the time delay is greater than a baseband sampling period”). Specifically, if we identify a parameter, R , as the ratio of the oversampling clock frequency to baseband sampling frequency, a delay of k oversampling sample-clock periods equals k/R of one baseband sampling period. *See* Ex.1001, 4:50-5:19, 7:1-19, 13:47-14:51. This follows because the baseband sampling period is the inverse of the baseband sampling frequency, and the oversampling period is the inverse of the oversampling clock frequency.

313. Thus, $k < R$ produces a delay equal to a fraction of a baseband sampling period, while $k > R$ produces a delay greater than one baseband sampling period.

314. Liu discloses oversampling rates including “at least 20” and “20-200” times the Nyquist rate, and explains that the oversampling rate may be fixed, programmable, or variable. Ex.1007, [0029]-[0030], [0048]. Liu also selects earlier- or later-occurring stored samples according to the desired focusing delay, with memory 16 sized for the needed delay range. *Id.*, [0032]-[0033], [0049]-[0051]. A nonzero offset $k < R$ therefore provides the fractional-baseband-period delay of claim 8.

315. Liu also renders claim 9 obvious. In the Nyquist-rate baseband option disclosed in Liu, its 20-times oversampling ratio means that one baseband sampling

period spans 20 oversampling sample-clock periods. *Id.*, [0020], [0030]. Selecting an offset $k > 20$ therefore provides a delay greater than one baseband sampling period. Claim 9 requires no particular amount by which the delay must exceed that period.

316. The focusing profile in Liu determines each channel's desired delay, and memory 16 is sized for the needed delay range and largest delay, with controller 28 accordingly selecting earlier- or later-occurring samples. *Id.*, [0004], [0032]-[0033], [0049]-[0051]. A POSA would have considered selecting an offset above 20 as an ordinary, predictable use of the mechanism disclosed in Liu to implement the delay specified by the focusing profile, with expected success because the same memory and controller would implement that offset as with any other integer offset.

J. Claim 10

1. **“The non-transitory computer-readable storage medium of claim 7, wherein the first oversampled digital signal is digitized to create samples which are more than one bit deep.”**

317. In my opinion, a POSA would have found claim 10 obvious based on Liu.

318. As I explained above for claim 7, it is my opinion that a POSA would have found claim 7 obvious based on Liu. *Supra* §XIII.H.

319. As a first matter, as explained in the Technical Background section of this declaration, digital beamforming systems which relied on oversampled input

signals, followed by various combinations of delays and filters and decimation were well-known and in wide use long before the earliest claimed priority date of the '055 patent. *See supra* §VI. Thus, by that time, it was known that there were benefits to various combinations of these elements depending on the capabilities of each element, the characteristics of the incoming signals, and the requirements for the resulting combined signals. Thus, claim 10 represents a straightforward combination of well-known elements to achieve well-understood benefits. Moreover, cost and power constraints would have motivated a POSA to select and combine these known signal-processing elements—such as oversampled ADCs, digital delays, filters/decimators, and combiners—in such a configuration that provided the desired beamforming performance while avoiding unnecessary processing, memory, and circuit overhead.

320. According to the '055 patent, the terms “one bit deep” and “bit depth” refer to the number of bits used to represent a sample. In one example, the '055 patent explains that the oversampled digital signal can be “other than one-bit deep” when other digitization methodologies are used, and that the minimum delay increment can depend on the “bit depth” of the digitization methodology. Ex.1001, 4:59-5:13.

321. As I explained for 1[a] above, analog-to-digital converter 14 in Liu digitizes the received signal to produce the first oversampled digital signal. *Supra*

§XIII.C.2. According to Liu, converters 14 are sigma-delta or other oversampling converters that sample higher than the Nyquist rate and output samples at an oversampling rate. *See id.*; *see also* Ex.1007, [0029]-[0030], [0048]. Liu additionally discloses that, although the sampling bit width may be low, “such as one bit,” “[h]igher bit widths, such as two, four, or more, may be provided.” *Id.*, [0030]; *see also id.*, claim 2.

322. Liu’s two-bit, four-bit, or greater-bit oversampling-converter outputs are samples more than one bit deep. The downstream beamforming path in Liu is further compatible with such multi-bit samples since Liu discloses that memory 16 can be “single or multi-bit” memory and that summer 24 can be a “multiple bit sample summer.” *Id.*, [0032], [0038]. Thus, it is my opinion that in Liu’s higher-bit-width embodiments, the first oversampled digital signal is digitized to create samples which are more than one bit deep.

XIV. GROUND 5: CLAIMS 6-10 ARE OBVIOUS BASED ON LIU AND ANDERSEN

323. In my opinion, a POSA would have found claims 6-10 obvious based on Liu in view of Andersen.

A. Claim 6

1. Motivation to Combine

324. In my opinion, a POSA implementing Liu’s oversampled receive beamformer would have been motivated to adapt its arrangement to incorporate

parallel delay and decimating filter paths extending from the same sensor, consistent with the teachings of Andersen.

325. Liu's system provides dynamic receive focusing utilizing memory as a delay element and phase rotation. *See* Ex.1007, Abstract, [0025], [0029]-[0030], [0032]-[0035], [0038]-[0040], [0043]-[0044], [0049]-[0051], Figs.2, 7.

326. Andersen teaches that at least one microphone channel may include two or more parallel delay and low-pass-filter/decimator paths, with the resulting outputs combined for processing by the DSP. Ex.1008, 4:18-27, Fig.7, claim 11.

327. A POSA would have been motivated to apply Andersen's teachings regarding parallel delay path layout in implementing Liu's receive beamformer, as doing so would have had the benefit of increased directional/focusing flexibility without needing an additional sensor or an additional analog to digital converter and while preserving Liu's oversampling, delay-selection, filtering/decimation, and summing operations. *See id.*, 2:60-62 ("[B]y controlling the various delay devices, other directional patterns could be realized."), 4:18-27, Fig.7, claim 11.

2. Reasonable Expectation of Success

328. A POSA would have had a reasonable expectation of success combining Liu and Andersen. Both disclose similar technology, including sensing analog signals, converting those signals using oversampling sigma-delta analog-to-

digital converters, and delaying the resulting oversampled digital signals with shift registers before filtering, decimating, and combining them.

329. A POSA applying Andersen's parallel delay-path teachings to Liu would have predictably provided multiple delayed sample streams derived from a single Liu receive channel/transducer element, for use in Liu's beamformer, while preserving Liu's oversampling, delay selection, filtering with decimation, and summing operations. A POSA would thus have had a reasonable expectation of success since the combination uses known elements having known functions, including Liu's oversampling analog to digital converter, delay elements, filters with decimation, and summer, along with Andersen's teachings of known parallel delay path arrangements.

3. Claim 6: "The non-transitory computer-readable storage medium of claim 1, wherein the first oversampled digital signal and the second oversampled digital signal are obtained from the same sensor."

330. In my opinion, a POSA would have found claim 6 obvious based on the Liu-Andersen combination.

331. As a first matter, as explained in the Technical Background section of this declaration, digital beamforming systems which relied on oversampled input signals, followed by various combinations of delays and filters and decimation were well-known and in wide use long before the earliest claimed priority date of the '055 patent. *See supra* §VI. A POSA would have understood that before that time,

it was known that there were benefits to various combinations of these elements depending on the capabilities of each element, the characteristics of the incoming signals, and the requirements for the resulting combined signals. Thus, claim 6 represents a straightforward combination of well-known elements to achieve well-understood benefits. Moreover, cost and power constraints would have motivated a POSA to select and combine these known signal-processing elements—such as oversampled ADCs, digital delays, filters/decimators, and combiners—in such a configuration that provided the desired beamforming performance while avoiding unnecessary processing, memory, and circuit overhead.

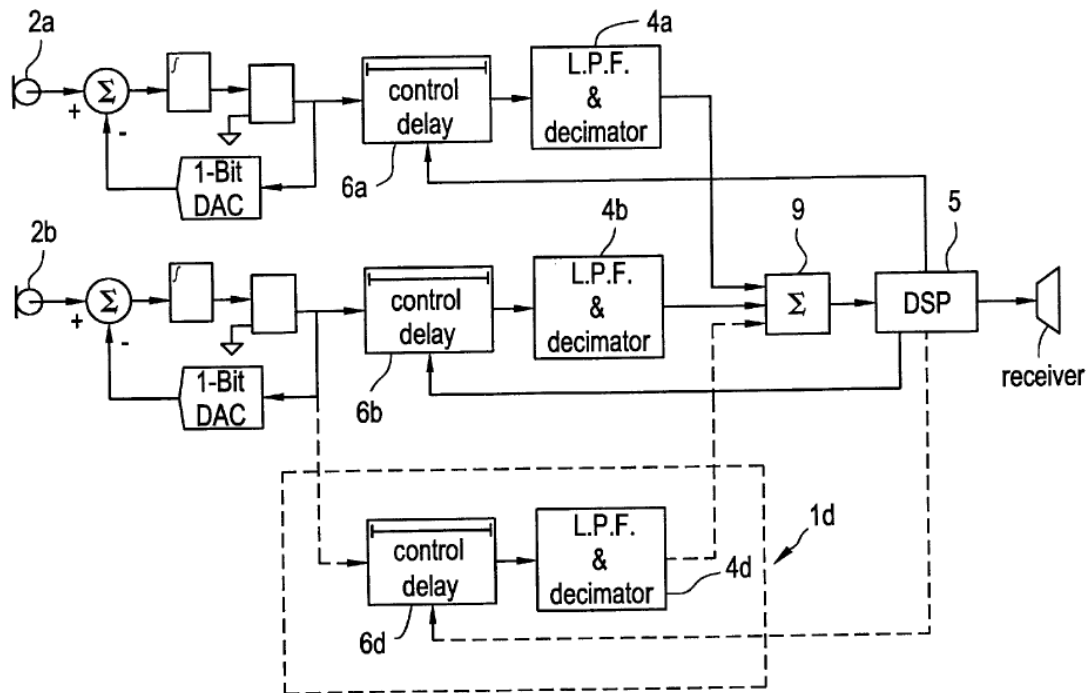
332. To begin, Andersen discloses the same type of sensor architecture as the '055 patent. Andersen's disclosed hearing aid with beamforming properties uses sigma-delta ADC microphone channels, low-pass filters/decimators, controllable delay devices, and summing/combination circuits. Ex.1008, Abstract, 2:5-25, 3:24-45, Fig.3.

333. With respect to its Figure 7 embodiment, Andersen discloses at least one microphone channel with parallel delay/filter paths derived from that same microphone channel. *Id.*, 4:18-27:

“FIG. 7 finally, shows another variation of the inventive circuit in which at least one of the microphone channels has not only one delay device and one digital low pass filter and decimator filter but two of those in parallel. It is also conceivable to have these parallel arrangements in one or more channels, even in all of them.

It is also possible to use more than two delay devices in parallel in at least one of said microphone channels, all connected to their respective digital low pass filter and decimator filter of said at least one of said channels.”

334. For example, as shown below, this includes the additional parallel delay/filter path 1d shown in dotted line:



Id., Fig.7.

335. As Andersen discloses with respect to Figure 7, “at least one of the microphone channels has not only one delay device and one digital low pass filter and decimator filter but two of those in parallel.” *Id.*, 4:18-27. Further, Andersen discloses that more than two delay devices may be used in parallel in the same microphone channel. *Id.* Claim 11 in Andersen likewise recites a microphone

channel equipped with a sigma-delta analog to digital converter “including at least two delay devices in parallel” operating on two low-pass filters/decimators, with the resulting outputs combined in a combination circuit. *Id.*, claim 11.

336. Thus, it is my opinion that Andersen’s parallel paths in the same channel disclose first and second oversampled digital signals obtained from the same sensor, as recited in claim 6 of the ’055 patent and consistent with the ’055 patent’s same-sensor embodiment.

337. In my opinion, a POSA would have been motivated to apply Andersen’s teachings regarding parallel paths in the same channel to Liu’s oversampled receive beamforming architecture. Such an application would have resulted in the benefit of increased directional/focusing flexibility without requiring an additional sensor or analog-to-digital converter. Andersen teaches that using oversampled sigma-delta bitstreams with controllable delay devices provides finely graduated delay control for beamforming and permits different directional characteristics, including through parallel delay/filter paths in a single microphone channel. *Id.*, 1:64-2:25, 2:60-61, 3:25-45, 4:18-27, Fig.7, claim 11. Liu similarly discloses dynamic receive focusing using oversampled sample selection and teaches reusing the same stored oversampled sample data multiple times for different focusing profiles and beamforming paths. Ex.1007, [0032]-[0033], [0043]-[0044], [0049]-[0051].

338. Applying Andersen's same-sensor parallel delay-path teachings to Liu would thus have predictably provided multiple delayed sample streams derived from a single Liu receive channel/transducer element, for use in Liu's beamforming, while preserving Liu's operational flow, including oversampling, delay-selection, filtering/decimation, and summing. A POSA would have had a reasonable expectation of success given that the combination uses known components for their known functions: Liu's oversampling converter, memory/delay controller, filters, and summer, along with Andersen's known same-sensor parallel delay/filter path arrangement. Thus, in the Liu-Andersen combination, first and second oversampled digital signals are obtained from the same sensor.

B. Claim 7

1. Motivation to Combine

339. In my opinion, a POSA implementing Liu's receive beamformer would have been motivated to implement Liu's post-delay filter 18 as a low-pass decimating filter, consistent with Andersen's teachings.

340. Both Liu and Andersen disclose beamforming utilizing a path of an oversampled sigma-delta analog-to-digital converter, time delay element, decimating filter, and beamforming/combination element. *See* Ex.1007, [0006], [0029]-[0035], [0038], [0049]-[0056]; Figs.2, 7; Ex.1008, Abstract, 2:5-25, 3:25-45, Figs.3-4.

341. And both Liu and Andersen further teach locating their decimating filter following the time delay element and before the summation element. Ex.1007, [0032]-[0035], [0049]-[0052], Figs.2, 7; Ex.1008, 3:30-39, Fig.3.

342. As a POSA would have understood, decimating low pass filters would pass the desired relatively low frequency in-band signal and attenuate higher-frequency components in the signal, including out-of-band quantization noise, and this would have been beneficial in Liu's implementation. *See, e.g.*, Ex.1022 (G. Moon et al., Design Approach for Decimation Filter for ADC Application, Int'l J. of Eng. Trends and Techn. (IJETT), vol. 10 no. 12 (2014)) at p. 1 ("Decimation is the process of reducing the sampling rate. In practice, this usually implies low-pass filtering a signal, then throwing away some of its samples."), *id.* ("The main task of a decimation filter is to remove the quantization noise away from the band of interest and avoid aliasing of high frequency components down to low frequency region or within the signal bandwidth."); Ex.1021 (L. Milic, Multirate Filters: An Overview, *APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, 2006, pp. 912-915), at p. 1 ("The use of an appropriate filter enables one to convert a digital signal of a specified sampling rate into another signal with the desired sampling rate without significantly destroying the signal components of interest."); *id.* ("Decimating the sampling rate by an integer factor of M means that among the input samples, ... only every M th sample are used as in

the output sequence. For avoiding aliasing, there is a need to use a low-pass anti-aliasing filter before down-sampler...”).

343. A POSA would have also understood the use of low-pass decimation filters to avoid aliasing. *See, e.g.*, Ex.1021 (L. Milic, Multirate Filters: An Overview, *APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, 2006, pp. 912-915), at p. 1 (“Filtering is required to suppress aliasing when reducing the sampling rate, called as decimation.”); *id.* (“For avoiding aliasing, there is a need to use a low-pass...filter before down-sampler.”).

344. Consistent with this understanding, a POSA would have been further motivated to implement filter 18 as a low-pass decimating filter in light of Andersen’s teachings to perform the ordinary sigma-delta reconstruction function of recovering the in-band/baseband signal from the delayed oversampled bitstream while reducing sample rate and suppressing out-of-band quantization noise. Andersen teaches that the low-pass filter/decimator converts the high-clock-frequency one-bit stream into a lower-clock-frequency digital word sequence, and Liu likewise uses reconstruction/decimation to reduce the incoming oversampled sample rate before further beamforming processing. Ex.1008, 2:5-25, 3:4-45; Ex.1007, [0034]-[0035], [0052].

345. Thus, in my opinion, a POSA would have been motivated to implement Liu's decimating filter 18 as a low-pass decimating filter, especially given the teachings of Andersen.

2. Reasonable Expectation of Success

346. A POSA would have had a reasonable expectation of success combining Liu and Andersen. Liu and Andersen are fundamentally similar technical disclosures, as discussed above, including that they both disclose beamforming utilizing a path of an oversampled sigma-delta analog-to-digital converter, time delay element, decimating filter, and beamforming/combination element. *See supra* §XIV.B.1.

347. A POSA would have had a reasonable expectation of success given this similarity in beamforming arrangement/architecture and because the implementation uses known components for their known functions: Liu's delayed oversampled analog-to-digital converter and post-delay filter 18, implemented in view of Andersen's known low-pass-decimating-filter teachings.

3. "The non-transitory computer-readable storage medium of claim 1, further comprising: applying a low pass filter with decimation to the time delayed first oversampled digital signal to output a baseband digital signal that is delayed by the time delay."

348. In my opinion, a POSA would have found claim 7 obvious based on Liu alone, as I explained in Ground 4 (*supra* §XIII.H). Even if Liu alone did not

render obvious claim 7, it is also my opinion that a POSA would have found claim 7 obvious based on the Liu-Andersen combination.

349. As a first matter, as explained in the Technical Background section of this declaration, digital beamforming systems which relied on oversampled input signals, followed by various combinations of delays and filters and decimation were well-known and in wide use long before the earliest claimed priority date of the '055 patent. *See supra* §VI. A POSA would have understood that before that time, it was known that there were benefits to various combinations of these elements depending on the capabilities of each element, the characteristics of the incoming signals, and the requirements for the resulting combined signals. Thus, claim 7 represents a straightforward combination of well-known elements to achieve well-understood benefits. Moreover, cost and power constraints would have motivated a POSA to select and combine these known signal-processing elements—such as oversampled ADCs, digital delays, filters/decimators, and combiners—in such a configuration that provided the desired beamforming performance while avoiding unnecessary processing, memory, and circuit overhead.

350. As I explained for 1[b] above, Liu delays the first oversampled digital signal by storing samples at the oversampling rate in memory 16 and selecting stored data as a function of beam delay for output to filter 18. *Supra* §XIII.C.3. Liu's filter 18 then reconstructs/decimates the selected delayed samples before

summation. Ex.1007, [0034]-[0035], [0052]. Andersen confirms that the post-delay reconstruction/decimation filter would be implemented as a low-pass filter with decimation.

351. Andersen discloses a hearing aid with beamforming properties using sigma-delta ADC microphone channels, controllable delay devices, digital low-pass filters/decimators, and summing/combination circuitry. Ex.1008, Abstract, 2:5-25, 3:24-45. Andersen's sigma-delta analog-to-digital converter outputs a one-bit stream at a high frequency, e.g., about 1 MHz, and Andersen's digital low-pass decimating filter converts that high-rate bitstream into a lower-clock-frequency digital word sequence. *Id.*, 2:5-25, 3:4-45. Andersen further discloses that the bitstream is delayed by a controllable delay device before being sent to "the digital low pass filter and decimator 4." *Id.*, 3:30-39; *see also id.*, Figs.3-4. Thus, it is my opinion that Andersen discloses applying a low-pass filter with decimation to a time-delayed oversampled digital signal to output a lower-rate digital signal delayed by the selected time delay.

352. In Andersen's beamforming system, that lower-frequency word sequence is a baseband digital signal. Andersen explains that its sigma-delta converters oversample at about 1 MHz and its low-pass decimating filter converts the high-rate bitstream into a lower-rate (e.g., 16kHz, 32 kHz, frequency between 10 and 50 kHz) digital word sequence. Ex.1008, 2:5-25, 3:4-18, 3:24-45. The

output from Andersen's low pass filter with decimation design is the downsampled digital signal having a sampling frequency (e.g., 16kHz, 32 kHz, frequency between 10 and 50 kHz), which corresponds to the final lower-rate representation of the oversampled microphone signal—i.e., a baseband digital signal. That understanding is consistent with the '055 patent, which describes receiver module 220 low-pass filtering and decimating an oversampled digital signal to output baseband digital signal 222 at a baseband sampling rate, with bandwidth prescribed by the application of interest. Ex.1001, 3:55-3:67, 6:22-39.

353. A POSA would have been motivated to implement Liu's post-delay filter 18 as a low-pass decimating reconstruction filter, in view of Andersen's teachings. Both Liu and Andersen use oversampled sigma-delta analog-to-digital converters, delay elements, decimating filters, and beamforming/combination elements. *See* Ex.1007, [0006], [0029]-[0035], [0038], [0049]-[0056]; Ex.1008, Abstract, 2:5-25, 3:25-45, Figs.3-4. And both Liu and Andersen place a decimating filter after delay selection and before summation. Ex.1007, [0032]-[0035], [0049]-[0052]; Ex.1008, 3:30-39.

354. A POSA would have been motivated to implement a low-pass decimating filter as filter 18 in Liu's system in light of Andersen's teachings to perform the function of sigma-delta reconstruction/recovery of the in-band/baseband signal from the delayed oversampled bitstream while

downsampling/decimating and suppressing out-of-band quantization noise. Ex.1008, 2:5-25, 3:4-45; Ex.1007, [0034]-[0035], [0052].

355. As I explained for claim 7 in Ground 4 above, Liu's later filter 26 does not undermine this mapping. *Supra* §XIII.H.

356. A POSA would also have had a reasonable expectation of success because the implementation utilizes known components for their known functions: Liu's delayed oversampled sample stream and post-delay filter 18, with filter 18 implemented as a known low-pass filter/decimator as taught by Andersen. Thus, it is my opinion that in the Liu-Andersen combination, a low-pass filter with decimation is applied to the time-delayed first oversampled digital signal to output a baseband digital signal delayed by the selected time delay.

357. Moreover, it is my opinion that even if claim 7 were to require the signal output from the low-pass-filter with decimation to be at the fully reconstructed signal/baseband Nyquist rate, the Liu-Andersen combination also renders that reading obvious for the reasons I explained in Ground 4. *Supra* §XIII.H. Andersen confirms the known post-delay low-pass decimating filter implementation for Liu's complete-channel-demodulation option: Andersen delays the sigma-delta oversampled digital signal using a controllable delay with the delayed signal being sent to "the digital low pass filter and decimator." *See* Ex.1008, 3:4-45. Thus, applying that understanding to the Liu-Andersen

combination, it is my opinion that a low-pass filter with decimation is applied to the time-delayed first oversampled digital signal, and a baseband digital signal delayed by the selected time delay is accordingly output.

C. Claims 8-9

- 1. Claim 8: “The non-transitory computer-readable storage medium of claim 7, wherein the time delay is equal to a fraction of a baseband sampling period.”**
- 2. Claim 9: “The non-transitory computer-readable storage medium of claim 7, wherein the time delay is greater than a baseband sampling period.”**

358. As I explained for claims 8-9 in Ground 4 above, Liu discloses delays satisfying these claimed timing limitations. *Supra* §XIII.I. Even if Liu alone did not render obvious claims 8-9, it is also my opinion that a POSA would have found these claims obvious based on the Liu-Andersen combination.

359. As a first matter, as explained in the Technical Background section of this declaration, digital beamforming systems which relied on oversampled input signals, followed by various combinations of delays and filters and decimation were well-known and in wide use long before the '055 patent's earliest claimed priority date. *See supra* §VI. A POSA would have understood that before that time, it was known that there were benefits to various combinations of these elements depending on the capabilities of each element, the characteristics of the incoming signals, and the requirements for the resulting combined signals. Thus, claims 8

and 9 represent straightforward combinations of well-known elements to achieve well-understood benefits.

360. Andersen teaches a known shift-register implementation for the Liu-Andersen combination. *See, e.g.*, Ex.1008, 2:17-25, 3:25-38, claim 6. Andersen further places a controllable delay in the oversampled sigma-delta bitstream prior to low-pass filtering/decimation. *Id.*, 1:51-57, 2:5-25, 3:4-18. Andersen also teaches that delay may be implemented using a controllable tapped shift register, and explains that high-rate sampling provides much smaller delay steps than lower-rate processing. *Id.*, 3:25-38, claim 6.

361. In the Liu-Andersen combination, implementing Liu's oversampled-sample delay using Andersen's controllable high-rate delay line/shift register would have provided the same fractional or greater-than-baseband-period delays discussed in Ground 4, depending on the selected tap or sample offset. A POSA would have been motivated to select those offsets as needed for Liu's dynamic receive focusing, and would have had a reasonable expectation of success because changing the selected tap or sample offset merely changes the amount of delay while using the same known fine precision delay implementation prior to filtering/decimation. *See supra* §XIII.I.

D. Claim 10

- 1. “The non-transitory computer-readable storage medium of claim 7, wherein the first oversampled digital signal is**

digitized to create samples which are more than one bit deep.”

362. In my opinion, incorporating a low-pass-filter with decimation in the Liu-Andersen combination in light of Andersen’s teachings does not alter Liu’s upstream multi-bit-width digitization. Thus, it is my opinion that, for the reasons I explained in Ground 4 (*supra* §XIII.J), a POSA would have found claim 10 obvious based on the Liu-Andersen combination.

XV. GROUND 6: CLAIMS 1-5 AND 7-10 ARE OBVIOUS BASED ON LIU AND SWANSON

363. As I explained above, a POSA would have found claims 1-5 and 7-10 obvious based on Ground 4. *Supra* §XIII. Even if Ground 4 did not render the recited non-transitory computer-readable-storage-medium/program-code implementation obvious, it is further my opinion that a POSA would have found claims 1-5 and 7-10 obvious based on Liu in view of Swanson.

A. Motivation to Combine

364. In my opinion, a POSA implementing Liu’s processor-based receive beamforming would have been motivated to further implement Swanson’s teachings regarding storing code including instructions for controlling the operation of such processor-based beamforming on a non-transitory computer-readable medium.

365. First, as described above in the Technical Background section, there were many well-known historical examples of digital systems for delay and sum beamforming of signals from microphone arrays, including use of microprocessors that include memory for storing code and are configured to execute such code, oversampled ADCs for converting analog signals to digital format, and digital signal processors for execution of filtering, delaying, decimating, and combining the signals from a microphone array. *See supra* §VI. A POSA at the time of the earliest claimed priority date of the '055 patent would have been well-aware of example uses of these elements, and the advantages of combining these elements in various ways. All elements of claims 1-5 and 7-10 were known long before the '055 patent.

366. A POSA would have been especially motivated to combine Liu and Swanson because both references provide details related to DSP-based beamforming, which would have helped a POSA by providing useful implementation details that would have reduced the amount of design effort and further confirmed the expectations of success. Further, Swanson provides details on the design and construction of low-cost structures for housing and operating the elements of such a system (Ex.1005, [0051]). All these implementation details would have provided specific guidance to a POSA interested in constructing an effective beamforming system that uses oversampled digital data from a

microphone array, provides filtering, delays, decimation and combining to produce a beamformed output.

367. As I explained in Ground 4 (*supra* §XIII), Liu discloses a processor-based implementation of beamforming. For example, Liu discloses that its “system 10 for receive beamforming ultrasound information” and related methods may be implemented “using a processor.” Ex.1007, [0024] (“**The system 10 is implemented** on one or more integrated circuits.... Other circuit implementations may be provided, such as ... **using a processor,**”) (emphasis added), Fig.2.

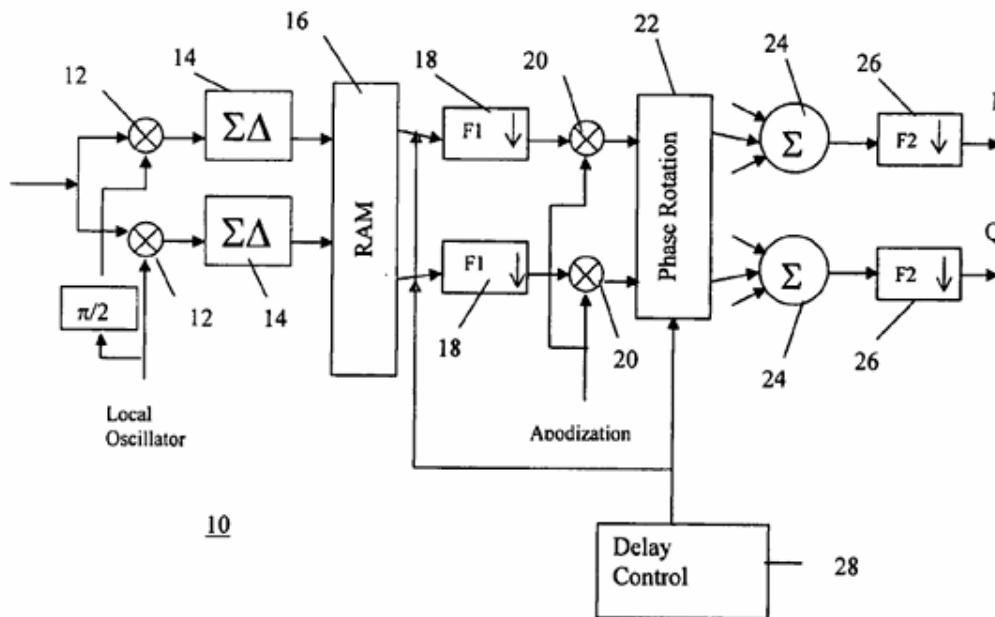


Figure 2

Id., Fig.2; *see also id.*, [0033] (“The delay controller 28 is a processor, control processor, digital signal processor, ...”), [0034] (“The filter 18 is operable to dynamically decimate under control of the dynamic delay controller 28.”), [0036]

(“The multiplier 20 is a[] ... digital processor...”), [0038] (“The summer 24 is a ... digital summer, processor, ...”), [0048] (disclosing that the oversampling rate is “programmable”). Liu’s beamforming methods, which are disclosed with respect to Figure 7 of Liu, may be implemented by system 10 in Figure 2. *See id.*, [0046] (“Fig. 7 shows one embodiment of a method for receive beamforming ultrasound information. The method is implemented by ... the receive beamformer[] of FIG[. 2...”), Fig.7.

368. Liu further teaches that its beamforming implementation may rely on code (e.g., “software”). *See id.*, [0059] (“While the invention has been described above by reference to various embodiments, it should be understood that many changes and modifications can be made without departing from the scope of the invention. As used herein, ‘connected with’ includes direct or indirect connection. For example, one or more hardware or software components may be between two connected components.”).

369. Like Liu, Swanson also discloses processor-based implementations of beamforming. More specifically, Swanson discloses a head-end chip, which “may be a processor, such as a digital signal processor (DSP)” (Ex.1005, [0005]), and that “may include a module 102C for data processing” such as for performing “beamform[ing].” *Id.*, [0035]-[0036], Fig.1.

370. Swanson further teaches a computer program product that comprises a non-transitory computer-readable medium with code for the aforementioned beamforming-related data processing on the DSP (head-end chip). *Id.*, [0054]-[0055]; *see also id.*, [0023]-[0024], claim 15, claim 18.

371. Even though a POSA would have been motivated, in my opinion, to utilize a non-transitory computer-readable medium with code for a digital beamforming system without the disclosure of Swanson, a POSA would have been further motivated to implement Liu's processor-based beamformer using Swanson's conventional stored-program approach for the same reasons explained in Ground 1. *Supra* §§X.A-B.

372. The combination would have enabled a POSA to easily program and control Liu's processor-based receive beamforming implementation using code (software) stored on a non-transitory computer-readable medium. The software (code) implementation would have also provided the benefit of flexibility and would have facilitated the ability to amend or make adjustments to the beamforming-related processing, and reuse the delay-selection and beamforming parameters for different channels, depths, focusing profiles, and beam configurations more easily than if the implementation was hard wired into a fixed integrated circuit. This flexibility would have also resulted in reduced costs over time, as modifications to the beamforming-related processing could be

implemented without manufacturing a new chip. These benefits are consistent with Liu's disclosure that its beamforming system may be implemented using processors, memory, and software. Ex.1007, [0024], [0033], [0034], [0036], [0038], [0046], [0048], [0059], Figs.2, 7.

B. Reasonable Expectation of Success

373. In my opinion, a POSA would have had a reasonable expectation of success in combining Liu with Swanson.

374. First, the combination of Liu and Swanson applies the implementation of Liu's known processor-based beamformer with Swanson's known software/storage medium implementation without changing Liu's underlying beamforming operation using oversampled-domain delay.

375. Second, both Liu and Swanson are directed to processor-based implementations of beamforming and provide details that are relevant to achieving modern implementations of the well-known delay and sum approaches used long before the time of earliest claimed priority date of the '055 patent. More specifically, Liu's beamforming system may be implemented using processor, memory, and software. *See, e.g.*, Ex.1007, [0024], [0032]-[0034], [0059]. Swanson similarly discloses that beamforming functions "implemented in firmware and/or software" and "stored as one or more instructions or code on a computer-readable medium," including "non-transitory computer-readable storage media," are used to

“cause one or more processors” to implement beamforming-related functions. Ex.1005, [0005], [0054]-[0055]; *see also id.*, [0023]-[0024].

376. The proposed modification presents nothing more than a predictable application of a known software storage implementation (as taught by Swanson) to a known signal processing-based system (as taught by Liu) according to their established functions.

C. Claims 1-5 and 7-10

1. 1[pre]: “A non-transitory computer-readable storage medium storing program code for causing a data processing system to perform steps comprising:”

377. I have been asked to assume the preamble of claim 1 is limiting. Under that assumption, it is my opinion that examples of a “...non-transitory computer-readable storage medium storing program code for causing a data processing system to perform steps” existed in known prior art for many years prior to the ’055 patent’s earliest claimed priority date. *See, e.g.*, Ex.1005, [0054]-[0056], claims 15-20; Ex.1025, [0016]-[0017], [0062], [0064], [0066]-[0068], claims 25-30. In particular, it is my opinion that Liu in view of Swanson renders obvious the preamble of claim 1, 1[pre].

378. Before turning to the prior art disclosure, it is my opinion, as discussed above (*supra* §X.C.1), that having reviewed the ’055 patent, the ’055 patent does not describe any unique or special technology for claim 1’s storage-medium aspect.

The '055 patent's disclosure discusses software implementation and machine-readable media in generic, conventional terms. In my opinion, that disclosure confirms that the alleged improvement of claim 1 is not any particular storage-medium implementation, but the underlying signal-processing operations.

379. Further, as discussed above, all elements of this claim have existed and been in use separately and together for many functions long before the earliest claimed priority date of the '055 patent, including to produce beamformed digital signals.

380. Turning to the prior art's disclosure of claim 1, it is my opinion that Liu discloses claim 1's recited signal-processing steps. Liu discloses "methods, systems, and receive beamformers for receive beamforming ultrasound information." Ex.1007, [0006]. This includes, for example, a system 10 having oversampling converters 14, memory 16, reconstruction filters 18, apodization multipliers 20, phase rotator 22, summer 24, and delay controller 28. *Id.*, [0006], [0022]-[0025], Fig.2.

381. Liu also discloses a receive-beamforming method or sequence that includes, for example, oversampling received signals, relatively delaying samples, partially reconstructing the received signals, summing the delayed/reconstructed samples, and reconstructing the beam sum. *Id.*, [0032]-[0040], [0046]-[0057], claims 13, 20-23, Figs.2, 7

382. Liu explains that system 10 may be implemented on one or more integrated circuits, including implementations “using a processor[] or using a field programmable gate array.” *Id.*, [0024]. As further specified, Liu’s delay controller 28 may be a “processor,” “control processor,” “digital signal processor,” “application specific integrated circuit,” “field programmable gate array,” or other circuitry, and it controls output of memory 16 and selects stored data from memory 16 as a function of delay:

“The delay controller **28** is a processor, control processor, digital signal processor, application specific integrated circuit, field programmable gate array, analog circuit, digital circuit, look-up table, memory, or combinations thereof. The controller **28** controls the output of the memory **16**. The controller **28** selects stored data from the memory **16** as a function of a delay for the beam. The controller **28** may include a same or different component for selecting phase rotations associated with the samples for fine focusing with the phase rotator **22**. The selected samples are output to the filter **18**.”

Id., [0033]. Liu further discloses that its summer 24 may also be a “digital summer, processor, digital circuit, or other device for combining digital samples.” *Id.*, [0038].

383. Liu also discloses that its implementation may be in the form of “software.” *See id.*, [0059] (“While the invention has been described above by reference to various embodiments, it should be understood that many changes and modifications can be made without departing from the scope of the invention. As

used herein, ‘connected with’ includes direct or indirect connection. For example, one or more hardware or software components may be between two connected components.”).

384. It is also my opinion that Swanson discloses a non-transitory computer-readable-medium/program-code implementation. Specifically, Swanson explains that, when its microphone-array and related beamforming functions are “implemented in firmware and/or software,” those functions may be “stored as one or more instructions or code on a computer-readable medium,” including “non-transitory computer-readable storage media,” and that such instructions/data cause one or more processors to implement the disclosed functions:

“If implemented in firmware and/or software, the functions described above may be stored as one or more instructions or code on a computer-readable medium. Examples include non-transitory computer-readable media encoded with a data structure and computer-readable media encoded with a computer program. Computer-readable media includes physical computer storage media. A storage medium may be any available medium that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to store desired program code in the form of instructions or data structures and that can be accessed by a computer. Disk and disc includes compact discs (CD), laser discs, optical discs, digital versatile discs (DVD), floppy disks and blu-ray discs. Generally, disks reproduce data magnetically, and discs reproduce data optically. Combinations of the above should also be included within the scope of computer-readable media.

In addition to storage on computer readable medium, instructions and/or data may be provided as signals on transmission media included in a communication apparatus. For example, a communication apparatus may include a transceiver having signals indicative of instructions and data. The instructions and data are configured to cause one or more processors to implement the functions outlined in the claims.”

Ex.1005, [0054]-[0055]; *see also id.*, [0023]-[0024]. Swanson identifies a head-end chip that performs microphone-array processing and explains that “[t]he head-end chip may be a processor, *such as a digital signal processor (DSP)*, located between the array of microphones and other circuitry in an electronic device.” *Id.*, [0005] (emphasis added). Swanson’s claim 15 likewise recites “a computer program product” comprising “a non-transitory computer readable medium comprising code for” receiving data from first and second digital microphone arrays, combining data, and beamforming; claim 18 further recites code for adjusting delay. *Id.*, claims 15, 18 (“The computer program product of claim 15, in which the medium further comprises code for performing the steps comprising at least one of adjusting a delay of a microphone of the first array of digital microphones...”).

385. A POSA would have been motivated to implement Liu’s disclosed processor-based receive beamformer using software or firmware stored on a conventional non-transitory computer-readable medium for execution on a processor, as taught by Swanson. In fact, Liu itself discloses that its beamforming

system may be implemented using a processor, memory, and software. *See* Ex.1007, [0024], [0033], [0034], [0036], [0038], [0046], [0048], [0059], Figs.2, 7.

Id., [0024] (disclosing processor implementation) (emphasis added):

“The system **10** is implemented on one or more integrated circuits. For example, separate chips are provided for groups of channels, such as 16, 128, 256, 512, 1024, or other numbers of channels being implemented on a chip. Cascaded summers may be provided on the same chip, or the summer or summers and downstream components are on one or more different chips. Other circuit implementations may be provided, such as using sequential separation between chips, **using a processor**, or using a field programmable gate array.”

Id., [0033] (disclosing processor implementation) (emphasis added):

“**The delay controller 28 is a processor, control processor, digital signal processor**, application specific integrated circuit, field programmable gate array, analog circuit, digital circuit, look-up table, **memory, or combinations thereof**. The controller **28** controls the output of the memory **16**. The controller **28** selects stored data from the memory **16** as a function of a delay for the beam. The controller **28** may include a same or different component for selecting phase rotations associated with the samples for fine focusing with the phase rotator **22**. The selected samples are output to the filter **18**.”

Id., [0034] (disclosing processor implementation):

“The filter **18** is operable to dynamically decimate under control of the dynamic delay controller **28**.”

Id., [0036] (disclosing processor implementation) (emphasis added):

“The multiplier **20** is an amplifier, **digital processor**, digital circuit, filter, or other device operable to amplify or reduce amplitude of the samples output by the filter **18**. The multiplier **20** applies apodization to the samples. The apodization applied may vary from channel-to-

channel and/or depth-to-depth. In alternative embodiments, a subtractor, divider, adder, or other component implements the apodization weighting.”

Id., [0038] (disclosing processor implementation) (emphasis added):

“The summer **24** is a node, **digital summer, processor**, digital circuit, or other device for combining digital samples. The summer **24** sums the relatively apodized and focused signals from a plurality of channels. Multiple input arrows are shown for each summer **24** to reflect inputs from the multiple channels. The summer **24** is a single multiple input summer or a cascade of summers each having two or more inputs. The summer **24** is a multiple bit sample summer, such as summing four or six bit samples.”

See also id., [0048] (disclosing oversampling rate may be programmable).

386. It is my opinion that Swanson provided a straightforward implementation path for Liu’s processor-based beamformer. This is because Swanson teaches storing digital-microphone-array beamforming-related functions as software/firmware instructions on non-transitory computer-readable media for execution by processors and identifies a digital signal processor as a processor example for its head-end chip. *See* Ex.1005, [0023]-[0024], [0054]-[0055], claims 15, 18. Not only would a POSA have understood that Swanson provided a straightforward path for Liu’s processor option, a POSA would have also had a reasonable expectation of success in such a combination of Liu in view of Swanson given that the proposed implementation simply applies Swanson’s known software/storage-medium implementation to Liu’s known processor-based

beamformer without changing Liu's underlying beamforming operation using oversampled-domain delay. Thus, it is my opinion that applying Swanson's known software-storage implementation to Liu's known processor-based beamformer would have been the predictable use of prior-art elements according to their established functions.

387. In my opinion, a POSA would have found the remaining limitations of claims 1-5 and 7-10 obvious for the reasons explained in Ground 4. The addition of Swanson's stored-program implementation does not change Liu's underlying signal path or the claim-by-claim mappings discussed in Ground 4.

XVI. GROUND 7: CLAIMS 6-10 ARE OBVIOUS BASED ON LIU IN VIEW OF ANDERSEN AND SWANSON

388. As I discussed above, it is my opinion that a POSA would have found claims 6-10 obvious based on Ground 5. *Supra* §XIV. Even if Ground 5 did not render the recited non-transitory computer-readable-storage-medium/program-code implementation obvious, it is further my opinion that a POSA would have found claims 6-10 obvious based on the Liu-Andersen combination in view of Swanson.

A. Motivation to Combine

389. In my opinion, a POSA implementing the Liu-Andersen combination's processor-based receive beamforming arrangement (as discussed above – *supra* §XIV) would have been motivated to further implement Swanson's

teachings regarding storing code including instructions for controlling the operation of such processor-based beamforming on a non-transitory computer-readable medium.

390. A POSA would have been especially motivated to combine Liu and Andersen with Swanson because the descriptions in all three references relate to DSP-based beamforming. Further, Swanson provides details on the construction of low-cost structures for housing and operating the elements of a beamforming system (e.g., Ex.1005, [0051]). All these implementation details would have provided specific guidance to a POSA interested in constructing a system that uses oversampled digital data from a microphone array, provides filtering, delays, decimation and combining to produce a beamformed output. The specifics provided in Swanson would have helped a POSA by providing useful implementation details that would have reduced the amount of design effort and further confirmed the expectations of success.

391. As I explained in Ground 5 (*supra* §XIV), the combination of Liu in view of Andersen satisfies the requirement of a processor-based receive beamformer having parallel delay and low-pass decimating filter paths emanating from the same sensor. *See supra* §XIV.

392. Liu further teaches that its beamforming implementation may rely on code (e.g., “software”). *See* Ex.1007, [0059] (“While the invention has been

described above by reference to various embodiments, it should be understood that many changes and modifications can be made without departing from the scope of the invention. As used herein, 'connected with' includes direct or indirect connection. For example, one or more hardware or software components may be between two connected components.”).

393. Like the Liu-Andersen combination's processor-based implementation, Swanson also discloses processor-based implementations of beamforming. More specifically, Swanson discloses a head-end chip, which “may be a processor, such as a digital signal processor (DSP)” (Ex.1005, [0005]), and that “may include a module 102C for data processing” such as for performing “beamform[ing].” *Id.*, [0035]-[0036], Fig.1.

394. Swanson further teaches a computer program product that comprises a non-transitory computer-readable medium with code for the aforementioned beamforming-related data processing on the DSP (head-end chip). *Id.*, [0054]-[0055]; *see also id.*, [0023]-[0024], claim 15, claim 18.

395. A POSA would have been motivated to implement the Liu-Andersen combination described in Ground 5 (*supra* §XIV) using Swanson's conventional stored-program approach for the same reasons explained in Grounds 1 and 6.

396. Moreover, the Liu-Andersen-Swanson combination would have enabled a POSA to easily program and control the Liu-Andersen combination's

processor-based receive beamforming implementation using code (software) stored on a non-transitory computer-readable medium. The software (code) implementation would have also provided the benefit of flexibility and facilitated the ability to amend or make tweaks to the beamforming-related processing more easily than if the implementation was hard wired into a fixed integrated circuit. This flexibility would have also resulted in reduced costs over time, as modifications to the beamforming-related processing could be implemented without manufacturing a new chip. These benefits are in line with disclosure of the prior art, including that Liu's and Andersen's beamforming system may be implemented using processor, memory, and software. Ex.1007, [0024], [0033], [0034], [0036], [0038], [0046], [0048], [0059], Figs.2, 7; Ex.1008, Abstract, 2:64-3:4, 3:25-29, claim 1.

B. Reasonable Expectation of Success

397. In my opinion, a POSA would have had a reasonable expectation of success in combining Liu and Andersen with Swanson.

398. First, combining the Liu-Andersen combination with Swanson combines the Liu-Andersen combination's known processor-based beamformer with Swanson's known software/storage medium implementation without changing the Liu-Andersen combination's underlying beamforming operation using oversampled-domain delay.

399. Second, Liu, Andersen, and Swanson are directed to processor-based implementations of beamforming. More specifically, the Liu-Andersen combination's beamforming system may be implemented using processor, memory, and software. *See, e.g.*, Ex.1007, [0024], [0032]-[0034], [0059]. Andersen likewise discloses a programmable or program-controlled DSP that controls the delay devices and receives the combined microphone-channel outputs for further beamforming processing. Ex.1008, Abstract, 3:16-18, 3:43-45, 3:57-59. Swanson similarly discloses that beamforming functions "implemented in firmware and/or software" and "stored as one or more instructions or code on a computer-readable medium," including "non-transitory computer-readable storage media" are used to "cause one or more processors" to implement beamforming-related functions. Ex.1005, [0005], [0054]-[0055]; *see also id.*, [0023]-[0024].

400. The proposed modification presents a predictable application of a known software storage implementation (as taught by Swanson) to a known signal processing-based system (the Liu-Andersen combination) according to their established functions. Moreover, the proposed modification would not change Liu's underlying oversampling, delay selection, filtering/decimation, apodization, phase rotation, summing, or beamforming operations. It would use Swanson's known software/firmware storage-medium approach to cause the processor/DSP-

based data-processing system to perform the same disclosed receive-beamforming operations.

401. In my opinion, a POSA would have found the remaining limitations of claims 6-10 obvious for the reasons explained in Ground 5. The addition of Swanson's stored-program implementation likewise does not change the Liu-Andersen combination's signal path or the claim-by-claim mappings discussed in Ground 5.

XVII.GROUND 8: CLAIMS 1-2 AND 4-9 ARE OBVIOUS BASED ON ANDERSEN AND SWANSON

402. In my opinion, a POSA would have found claims 1-2 and 4-9 obvious based on Andersen in view of Swanson.

A. Motivation to Combine

403. In my opinion, a POSA implementing Andersen's digital signal processor (DSP)-based beamformer would have been motivated to further implement Swanson's teachings regarding storing code including instructions for controlling the operation of a DSP-based beamformer on a non-transitory computer-readable medium.

404. Both Andersen and Swanson disclose DSP-based beamformers. Andersen teaches a DSP-based implementation of oversampled delay and sum beamforming. *See* Ex.1008, Abstract, 2:5-14, 3:16-18, 3:43-45, 3:57-59. Swanson similarly teaches a DSP-based beamforming system—more specifically, Swanson

discloses a head-end chip, which “may be a processor, such as a digital signal processor (DSP)” (Ex.1005, [0005]), and that “may include a module 102C for data processing” such as for performing “beamform[ing].” *Id.*, [0035]-[0036], Fig.1.

405. Swanson further teaches a computer program product that comprises a non-transitory computer-readable medium with code for the aforementioned beamforming-related data processing on the DSP (head-end chip). *Id.*, [0054]-[0055]; *see also id.*, [0023]-[0024], claim 15, claim 18. Even though a POSA would have been motivated, in my opinion, to utilize a non-transitory computer-readable medium with code for a digital beamforming system without the disclosure of Swanson, a POSA would have been further motivated to implement Andersen’s DSP-based beamformer using Swanson’s conventional stored-program approach for the reasons explained in Ground 1. *Supra* §X.A. The combination would have enabled a POSA to easily program and control Andersen’s DSP-based beamforming implementation using code (software) stored on a non-transitory computer-readable medium. The software (code) implementation would have also provided the benefit of flexibility and facilitated the ability to amend or make tweaks to the beamforming processing more easily than if the implementation was hard wired into a fixed integrated circuit. This flexibility would have also resulted in reduced costs over time, as modifications to the beamforming processing could be implemented without manufacturing a new chip. That same flexibility would

have motivated a POSA to use stored software or firmware to program, update, or reuse Andersen's delay settings for different directional patterns, microphone-channel configurations, and operating modes. Andersen expressly discloses multiple directional patterns and embodiments with independently controlled or parallel delay paths in one or more microphone channels. *See* Ex.1008, 2:43-62, 3:30-45, 3:52-4:27, Figs.1, 3-7; *see also* Ex.1005, [0019], [0023]-[0024], [0054]-[0055]. These benefits are in line with disclosure of the prior art, including that Andersen's beamforming system may be implemented using a digital signal processor. *See, e.g.*, Ex.1008, Abstract, 1:64-2:4, 2:5-14, 3:30-39, 3:57-62.

B. Reasonable Expectation of Success

406. In my opinion, a POSA would have had a reasonable expectation of success in combining Andersen and Swanson.

407. First, the combination applies Andersen's known DSP-based beamformer with Swanson's known software/storage medium implementation without changing Andersen's underlying beamforming operation using oversampled-domain delay.

408. Second, both Andersen and Swanson are directed to digital signal processor (DSP)-based beamformers. More specifically, Andersen discloses that its beamformer arrangement may be implemented in a digital signal processor (DSP). *See, e.g.*, Ex.1008, Abstract, 3:16-18, 3:43-45, 3:57-59. Swanson similarly

discloses that beamforming functions “implemented in firmware and/or software” and “stored as one or more instructions or code on a computer-readable medium,” including “non-transitory computer-readable storage media” are used to “cause one or more processors,” such as a DSP, to implement beamforming-related functions. Ex.1005, [0005], [0054]-[0055]; *see also id.*, [0023]-[0024].

409. The proposed modification presents nothing more than a predictable application of a known software storage implementation (as taught by Swanson) to a known digital signal processing-based system (as taught by Andersen) according to their established functions.

C. Claim 1

1. 1[pre]: “A non-transitory computer-readable storage medium storing program code for causing a data processing system to perform steps comprising:”

410. I have been asked to assume the preamble of claim 1 is limiting. Under that assumption, it is my opinion that examples of a “...non-transitory computer-readable storage medium storing program code for causing a data processing system to perform steps” existed in known prior art for many years prior to the earliest claimed priority date of the '055 patent. *See, e.g.*, Ex.1005, [0054]-[0056], claims 15-20; Ex.1025, [0016]-[0017], [0062], [0064], [0066]-[0068], claims 25-30. In particular, it is my opinion that Andersen in view of Swanson renders obvious the preamble of claim 1.

411. Before turning to the prior art disclosure, and as discussed above (*supra* §X.C.1), it is my opinion, based on my review of the '055 patent, that the '055 patent does not describe any unique or special technology for claim 1's storage-medium aspect. The '055 patent's disclosure discusses software implementation and machine-readable media in generic, conventional terms. In my opinion, that disclosure confirms that the alleged improvement of claim 1 is not any particular storage-medium implementation, but the underlying signal-processing operations.

412. Turning to the prior art's disclosure of claim 1, it is my opinion that Andersen discloses claim 1's recited signal-processing steps. Andersen discloses that its hearing aid includes at least two microphone channels, sigma-delta analog-to-digital converters (ADCs), low-pass/decimator filters, and "at least one programmable or program controlled signal processor." Ex.1008, Abstract.

413. Andersen additionally explains that the decimated data words from the microphone channels are "normally[] applied to a programmable or program controlled digital signal processor" (DSP), that the DSP controls the delay device(s), and that combined channel outputs are passed to the DSP for further processing. *Id.*, 3:16-18 (explaining that "data words" exiting low pass filter and decimator "are then, normally applied to a programmable or program controlled digital signal processor"), 3:43-45 ("The controllable delay would be controlled by

the DSP so that the DSP direct the beam in the desired directions.”), 3:57-59 (“The output signals of the digital low pass filter and decimator filters 4 *a* and 4 *b* are combined in a summing circuit 7 and passed on to the DSP.”). Thus, Andersen discloses a DSP-controlled beamforming system for performing the underlying signal processing steps.

414. It is also my opinion that Swanson discloses a non-transitory computer-readable-medium/program-code implementation. Specifically, as I explained for 1[pre] in Ground 1, Swanson discloses that, when beamforming functions are implemented in firmware and/or software, those functions may be stored as instructions or code on a computer-readable medium, including non-transitory physical storage media, and may cause one or more processors to implement beamforming functions. *Supra* §X.C.1.

415. A POSA would have been motivated to implement Andersen’s DSP-based beamformer using software or firmware stored on a conventional non-transitory computer-readable medium for execution on a processor, such as a DSP, as taught by Swanson. It is my opinion that Swanson provided a straightforward implementation path for Andersen’s DSP-based beamformer. This is because Swanson teaches storing microphone-array beamforming-related functions as software/firmware instructions on non-transitory computer-readable media for execution by processors, and also identifies a digital signal processor as a processor

example for its head-end chip. *See* Ex.1005, [0023]-[0024], [0054]-[0055], claims 15, 18. Not only would a POSA have understood that Swanson provided a straightforward path for Andersen's DSP implementation, a POSA would have also had a reasonable expectation of success in the Andersen-Swanson combination because the implementation simply applies Swanson's teachings regarding a known software/storage-medium implementation to Andersen's known DSP-based beamformer without changing Andersen's beamforming operation using oversampled-domain delay. Thus, it is my opinion that applying Swanson's known software-storage implementation to Andersen's known DSP-based beamformer would have been nothing more than the predictable use of prior-art elements according to their established functions. A POSA would have been motivated to implement Andersen's programmable/program-controlled DSP beamformer using Swanson's conventional stored-program approach for the same reasons explained for Ground 1. *Supra* §§X.A, B, C.1. Andersen already discloses programmable/program-controlled DSP controlling delay and processing combined beamformed microphone-channel outputs, and Swanson confirms that such beamforming and delay-adjustment functions were conventionally embodied as code stored on non-transitory computer-readable media and executed by processors. *See* Ex.1008, Abstract, 3:16-18, 3:43-45, 3:57-59; Ex.1005, [0023]-[0024], [0054]-[0055]. Thus, in my opinion, applying Swanson's known stored-program

implementation to Andersen's known DSP-controlled beamforming architecture would have been a routine, predictable design choice that would not alter Andersen's disclosed beamforming operation.

2. **1[a]: "outputting a first oversampled digital signal output from an analog-to-digital converter (ADC), wherein the first oversampled digital signal is responsive to an analog field and the first oversampled digital signal is created at a sampling clock frequency;"**

416. In my opinion, Andersen in view of Swanson renders this limitation obvious.

417. As an initial matter, as discussed in this declaration's Technical Background section above, digital oversampling analog signals from microphones has been widely known and widely used since long before the earliest claimed priority date of the '055 patent. *See supra* §VI.

418. Andersen discloses a "hearing aid with beam forming properties, having at least two microphone channels (1a, 1b)." Ex.1008, Abstract. Each microphone channel includes a microphone (2a/2b) and a sigma-delta analog-to-digital converter (3a/3b). *Id.* ("A hearing aid with beam forming properties, having at least two microphone channels (1 a , 1 b) for at least two microphones (2 a , 2 b), the microphone channels each comprising an analog to digital converter (3 a , 3 b) and having at least one programmable or program controlled signal processor (5), as well as a digital to analog converter, and at least one receiver and a battery for

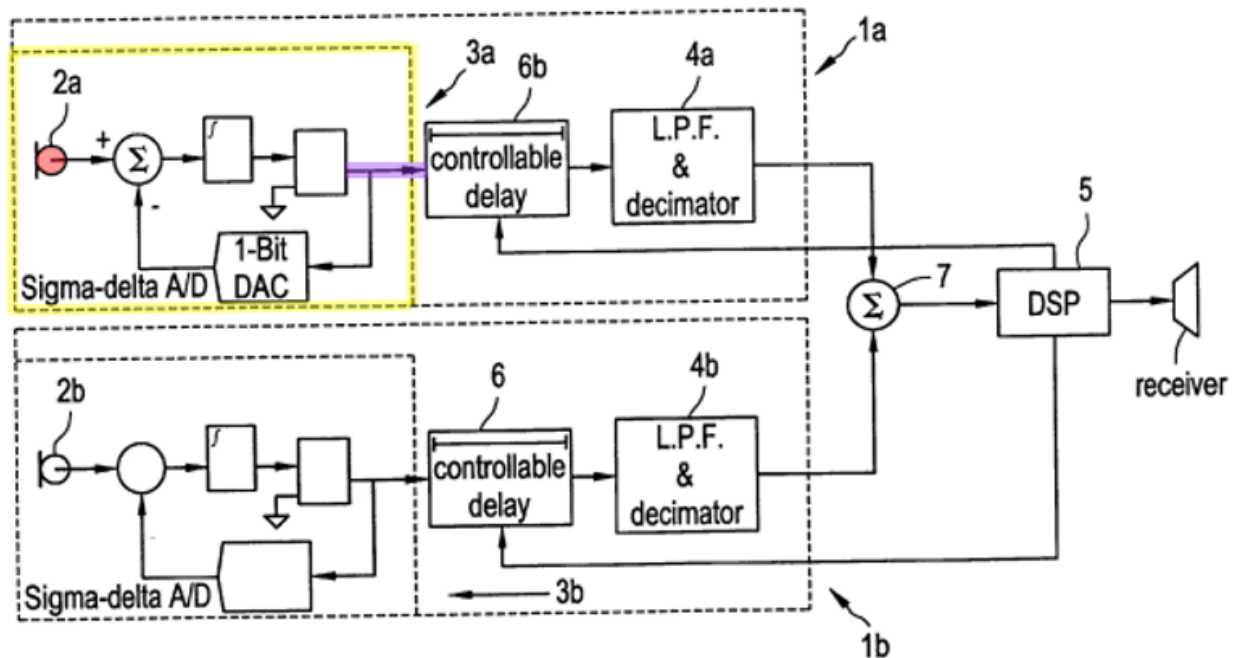
power supply.”); *see also id.*, 2:40-41 (“FIG. 2 shows schematically the general structure of a sigma-delta analog to digital converter (ADC);”), 3:25-29 (“Two microphone channels **1 a** and **1 b** comprise microphones **2 a** and **2 b** and sigma-delta analog to digital converters **3 a**, **3 b** including digital low pass filters and decimator filters **4 a** and **4 b** for supplying data words to a programmable or program controlled digital signal processor **5**.”), Fig.2.

419. Andersen further explains that the analog to digital converter operates at a “high clock frequency,” e.g., “1 MHz or higher,” and produces a “1 bit stream” at the clock frequency, which is oversampled relative to the bandwidth of the input audio signal (e.g., approximately 20 Hz to 20 kHz). *Id.*, 3:4-22; *see also id.*, 1:50-56 (disclosing “sigma-delta converter with a sampling rate or clock frequency of f.i., 1 MHz” and “bit stream”), 3:30-39 (disclosing “sampling rate” of “1 MHz” and “bit stream”). Thus, Andersen’s high-clock-frequency one-bit stream output from the converter is an oversampled digital signal created at a sampling clock frequency.

420. Andersen also discloses that this oversampled digital signal is responsive to an analog field. Andersen’s microphone 2a receives sound—i.e., an analog acoustic-pressure field—and supplies the resulting analog microphone signal to sigma-delta analog-to-digital converter 3a. Ex.1008, Abstract, 3:25-29, 1:40-46, claim 1. The fact that the oversampled digital signal is responsive to sound received by microphone 2a and is output from the analog-to-digital converter 3a is

evidence of the fact that the oversampled digital signal is responsive to an analog field. The one-bit stream generated by converter 3a from that microphone signal is therefore responsive to the analog acoustic field.

421. This arrangement is illustrated in Figure 4 of Andersen, specifically with microphone 2a (red) providing the analog microphone signal to sigma-delta analog-to-digital converter 3a (yellow), which outputs the oversampled one-bit stream (purple) at the sampling clock frequency:



Ex.1008, Fig.4. Thus, it is my opinion that Andersen discloses outputting a first oversampled digital signal output from an analog-to-digital converter (e.g., sigma-delta analog-to-digital converter 3a), where the signal is responsive to an analog field (e.g., acoustic input received by microphone 2a) and is created at a sampling clock frequency.

3. **1[b]: “delaying the first oversampled digital signal by a time delay wherein the time delay is equal to an integer number of sampling clock cycles to produce a time delayed first oversampled digital signal; and”**

422. In my opinion, Andersen in view of Swanson renders this limitation obvious.

423. As an initial matter, as discussed in the Technical Background section in this declaration, the use of a time delay equal to an integer number of cycles of the sampling clock to produce a time-delayed oversampled signal was widely known and broadly used long before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §VI.

424. As I discussed for 1[a], Andersen's sigma-delta analog-to-digital converter outputs an oversampled one-bit stream at a high clock frequency. *Supra* §XVII.C.2. Andersen further discloses that one or both microphone channels include “a controllable delay device 6” positioned on that bit-stream path before the digital low-pass filter/decimator. *See, e.g.,*

Ex.1008, 3:25-29:

“Two microphone channels 1a and 1b comprise microphones 2a and 2b and sigma-delta analog to digital converters **3 a, 3 b** including digital low pass filters and decimator filters **4 a** and **4 b** for supplying data words to a programmable or program controlled digital signal processor **5.**”

Id., 3:30-39:

“In one of the microphone channels a controllable delay device **6** is included. This delay device is typically a multiple tap shift register and the control signal coming from the DSP **5** will decide how many 1 bit stages each sample of the bit stream will go through (and thus be delayed by) before they are tapped and sent furtheron [sic] in the system, in this case to the digital low pass filter and decimator **4**. The resulting delay is equal to the number of stages times the inverse sampling rate, f.i. 1 MHz.”

Id., 3:52-59:

“In FIG. 4 both microphone channels **1 a** and **1 b** contain each a controllable delay device **6 a**, **6 b**. They can, of course, be controlled independently and separately. Although two delay devices are included, only one of the two may be controlled whereas the other is switched off.”

425. Andersen explains that “[t]his delay device is typically a multiple tap shift register” and that digital signal processor (DSP) **5** “will decide how many 1 bit stages each sample of the bit stream will go through (and thus be delayed by)” before being tapped and sent further in the system. *Id.*, 3:31-36. Thus, Andersen delays the oversampled one-bit digital signal output of the sigma-delta analog-to-digital converter, corresponding to the claimed first oversampled digital signal, to produce a time-delayed oversampled digital signal before the signal reaches the low-pass filter and decimator.

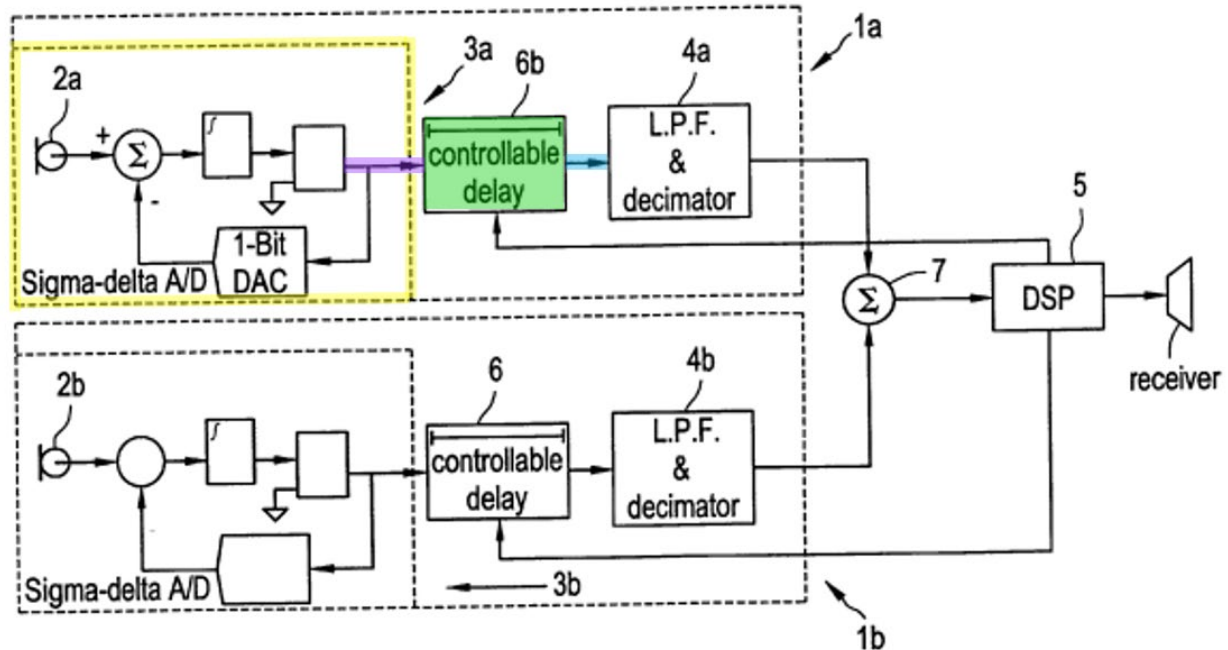
426. Andersen further discloses that the time delay equals an integer number of sampling-clock cycles. Andersen’s sigma-delta analog-to-digital converter operates at a “high clock frequency,” e.g., “1 MHz or higher,” and its

controllable delay device is a one-bit adjustable digital delay line/tapped shift register in the converter bit stream. Ex.1008, 3:4-22, 3:30-38. In that arrangement, selecting N shift-register stages delays the bit stream by N sampling-clock periods—i.e., an integer number of sampling-clock cycles. In fact, Andersen further confirms that relationship, explaining that the high-rate bit-stream delay provides “delayed difference steps of multiples of 1 usec” and that “[t]he resulting delay is equal to the number of stages times the inverse sampling rate.” *Id.*, 1:51-57, 3:31-39; *see also id.*, 2:21-25 (“In order to realize controllable delays as short as 1 usec it is of advantage to use a clock frequency for the sigma delta ADC in the range of 1 MHz or even higher.”). Thus, Andersen discloses a delay equal to $N \times 1/f_s$, where N is an integer number of sampling-clock cycles, and f_s is the sampling frequency.

427. Figure 4 of Andersen illustrates this arrangement. *Id.*, 3:46-56, Fig.4. Specifically, in the upper channel, sigma-delta analog-to-digital converter 3a (yellow) outputs the oversampled digital signal bit stream (purple), controllable delay 6b⁸ (green) is interposed on that bit-stream path before LPF/decimator 4a,

⁸ Andersen appears to contain inconsistent reference numerals. In discussing Fig. 4, Andersen states that “both microphone channels 1a and 1b contain each a

and the bit-stream output of delay device 6b is a time delayed first oversampled digital signal (blue):



Id., Fig.4.

4. 1[c]: “combining the time delayed first oversampled digital signal with a second oversampled digital signal to obtain the

controllable delay device 6a, 6b,” while Figure 4 labels the controllable delay devices 6b and 6. *Compare* Ex.1008, 3:52-53, with *id.*, Fig.4. This apparent typographical/reference-numeral inconsistency does not affect Andersen’s disclosure that each digital microphone channel can include a controllable delay device.

beamformed digital signal, wherein the second oversampled digital signal is responsive to the analog field.”

428. In my opinion, Andersen in view of Swanson discloses, or at least renders obvious, this limitation.

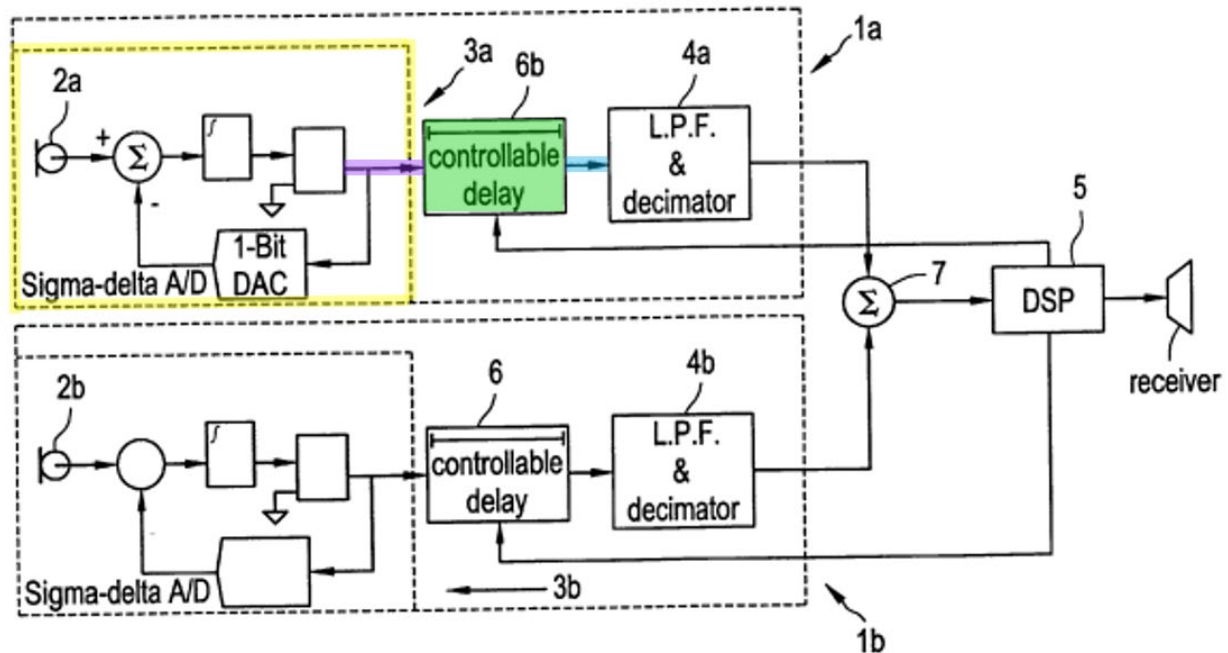
429. As a first matter, combining a delayed signal with another signal to form a beamformed signal responsive to an analog field was not new at the time of the '055 patent's earliest claimed priority date. As discussed in the Technical Background section, combinations of delayed signals to produce beamformed signals were well established and widely-used long before the '055 patent's earliest claimed priority date. *See, e.g., supra* §VI. More recent combinations of oversampled digital signals responsive to analog fields emerged later, along with the emergence of digital signal processing, but also well before the '055 patent's earliest claimed priority date.

430. Andersen describes a hearing aid with “at least two microphone channels (1a, 1b),” each including a microphone (2a/2b) and a sigma-delta analog-to-digital converter (3a/3b). Ex.1008, Abstract, 3:25-29. As I explained for 1[a]-1[b], Andersen's sigma-delta converters output oversampled one-bit streams at a high clock frequency, and those streams are responsive to sound received by the corresponding microphones. *Supra* §§XVII.C.2-3. Thus, the high-clock-frequency one-bit digital signal stream output from analog-to-digital converter 3b in

Andersen's second channel is a second oversampled digital signal responsive to the same analog acoustic field.

431. Andersen discloses 1[c]. As illustrated in Andersen's Figure 4, downstream channel signals respectively derived from the time-delayed first oversampled bit stream and the second oversampled bit stream through the corresponding low-pass filters/decimators are combined in summing circuit 7 and then provided to DSP 5. *Id.*, 3:57-59 ("The output signals of the digital low pass filter and decimator filters 4 *a* and 4 *b* are combined in a summing circuit 7 and passed on to the DSP."), Fig.4. Andersen explains that the controllable delay allows "the DSP [to] direct the beam in the desired directions," and that the hearing aid "can be used for active beamforming." *Id.*, 1:40-47, 3:42-45; *see also id.*, 3:59-62.

432. Figure 4 of Andersen illustrates the relevant channel structure. More specifically, in the upper channel, analog-to-digital converter 3a (yellow) outputs the first oversampled digital signal bit stream (purple) and controllable delay 6b (green) delays that bit stream to output a time delayed first oversampled digital signal (blue); in the lower channel, analog-to-digital converter 3b (yellow) outputs the second oversampled digital signal bit stream (gray); and the channel signals are combined (pink) for beamforming:



Id., Fig.4.

433. To the extent Solos asserts Andersen does not disclose 1[c] because Andersen's express Figure 4 summing occurs only after each channel's low-pass filter/decimator, Andersen at least renders obvious combining the time-delayed first oversampled digital signal with the second oversampled digital signal before a common low-pass filter/decimator. Andersen already provides both high-rate streams at the inputs to the per-channel low-pass filters/decimators, already delays the first stream at that high rate, and already combines the channel signals for beamforming. *See, e.g.,*

Ex.1008, 3:30-45:

“In one of the microphone channels a controllable delay device **6** is included. This delay device is typically a multiple tap shift register and the control signal coming from the DSP **5** will decide how many 1 bit

stages each sample of the bit stream will go through (and thus be delayed by) before they are tapped and sent furtheron [sic] in the system, in this case to the digital low pass filter and decimator **4**. The resulting delay is equal to the number of stages times the inverse sampling rate, f.i. 1 MHz.

With this high resolution of the sigma-delta ADC the time resolution can be 30-40 times higher than would be possible inside the DSP using its clock as a basis for delays. Normally, this setup can only handle beam forming from the front or from the back but not both. The controllable delay would be controlled by the DSP so that the DSP direct the beam in the desired directions.”

Id., 3:52-59:

“In FIG. 4 both microphone channels **1 a** and **1 b** contain each a controllable delay device **6 a**, **6 b**. They can, of course, be controlled independently and separately. Although two delay devices are included, only one of the two may be controlled whereas the other is switched off.

The output signals of the digital low pass filter and decimator filters **4 a** and **4 b** are combined in a summing circuit **7** and passed on to the DSP.”

See also id., Fig.4.

434. In that arrangement, the delayed first oversampled bit stream is combined with the second oversampled bit stream to obtain a beamformed digital signal, which is then low-pass filtered/decimated for downstream DSP processing. A POSA would have been motivated to use one common downstream filter/decimator because doing so would predictably reduce duplicate per-channel filtering while preserving Andersen’s fine high-rate delay control. A POSA would

have had a reasonable expectation of success because the arrangement uses Andersen's known delay, summing, and filtering/decimation functions for the same purposes disclosed in Andersen.

D. Claim 2

1. “The non-transistery [sic] computer-readable storage medium of claim 1, wherein the combining is performed in an oversampled signal domain.”

435. In my opinion, a POSA would have found claim 2 obvious based on Andersen in view of Swanson.

436. As I explained for 1[a]-1[c], Andersen's sigma-delta analog-to-digital converters output high-clock-frequency one-bit streams that are oversampled digital signals, and Andersen applies a controllable delay to the first-channel stream before low-pass filtering and decimation. *Supra* §§XVII.C.2-4. I also explained for 1[c] that a POSA would have found it obvious to combine the delayed first-channel high-rate bit stream with the second-channel high-rate bit stream and then apply a common downstream low-pass filter/decimator to the resulting beamformed signal. *Supra* §XVII.C.4. This arrangement would preserve Andersen's fine oversampled-domain delay control while reducing duplicate per-channel filtering hardware. Ex.1008, 3:4-18, 3:30-45, 3:52-59, Fig.4.

437. In that arrangement, the combining is performed in an oversampled signal domain. At the time of combining, the first and second channel signals

remain high-clock-frequency one-bit streams output by their respective sigma-delta analog-to-digital converters, including the first stream after its oversampled-domain delay. Andersen's low-pass filter/decimator is what subsequently converts such a high-rate one-bit stream, e.g., at about 1 MHz, into lower-rate digital words, e.g., at 16 or 32 kHz. Ex.1008, 3:4-18, 3:30-39. Because the combining occurs before that rate-reducing filtering and decimation, the signals are combined while still in the oversampled signal domain. Thus, it is my opinion that the Andersen-Swanson combination renders claim 2 obvious.

E. Claim 4

1. “The non-transitory computer-readable storage medium of claim 1, wherein the combining is performed in a baseband signal domain.”

438. In my opinion, a POSA would have found claim 4 obvious based on Andersen in view of Swanson.

439. Further, as I mentioned above, oversampled digital beamformers were well-established long before the earliest claimed priority date of the '055 patent. Thus, claim 4 represents a straightforward combination of well-known elements to achieve well-understood benefits.

440. In my opinion, a POSA would have understood “baseband signal domain,” in the context of the '055 patent, to include at least the lower-rate digital signal domain produced after the receiver's low-pass filtering/decimation has

converted an oversampled digital signal to a signal at the baseband sampling rate. *See* Ex.1001, 3:6-7, 7:42-51, 8:55-56, 13:56-58, 15:9-36. For example, the '055 patent describes a receiver that low-pass filters and decimates an oversampled digital signal and outputs a “baseband digital signal,” and elsewhere identifies a 16 kHz post-decimation output as a baseband sample-rate signal. *See id.*, 2:54-59, 3:55-67, 6:44-52, 7:20-32, 8:27-39.

441. Andersen discloses combining signals in that lower-rate post-decimation domain. Specifically, Andersen’s sigma-delta analog-to-digital converters 3a/3b generate one-bit digital signal streams at a high clock frequency, and digital low-pass filter/decimator filters 4a/4b convert the corresponding one-bit streams into digital word sequences at a lower clock frequency, e.g., 16 or 32 kHz. Ex.1008, 3:4-16. Andersen explains that “[t]he output signals of the digital low pass filter and decimator filters 4a and 4b are combined in a summing circuit 7 and passed on to the DSP.” *Id.*, 3:57-59, Fig.4. Thus, Andersen’s combining occurs after low-pass filtering and decimation have converted the high-clock-frequency bit streams into lower-rate digital word sequences that the DSP uses for further processing. Thus, Andersen’s combining is performed in a baseband signal domain, consistent with the disclosure of the '055 patent. *See* above; *see also, e.g.,*

Ex.1001 ('055 patent), 7:20-32:

“FIG. 3 illustrates, generally at **300**, applications of the system from FIG. 2C, according to embodiments of the invention. With reference to FIG. 3, a non-limiting example of a digital microphone system is provided with a four stage PDM receiver module. An analog field quantity e.g., an acoustic field **302** is sensed by a digital microphone **304**. The digital microphone **304** employs a one-bit sigma-delta modulation to perform analog-to-digital conversion (ADC). In one non-limiting embodiment, the digital microphone **304** is driven with a 2.048 MHz sampling clock frequency to output an oversampled digital output signal at **306**. In the example of FIG. 3, the baseband sampling frequency is chosen to be 16 kHz.”

Id., 8:27-39:

“In the example of FIG. 3, the fourth stage of PDM receiver module **314** is a low pass filter **328** which decimates by a factor of 4:1 thereby reducing the input digital signal at **326** from a sample rate of 64 kHz to a baseband sample rate of 16 kHz at **330**. A finite impulse response (FIR) filter structure or an infinite impulse response (IIR) filter structure can be used in the stages of the PDM receiver module **314** described above, such as, for example in low pass filter **328**, etc. Thus, the PDM receiver module receives as an input a time delayed oversampled digital signal at **312** with sampling rate of 2.048 MHz and outputs a baseband signal, which in some embodiments is an acoustic signal, at a baseband sampling rate of 16 kHz at **330**.”), 14:45-51 (“In the oversampled systems described above, in various non-limiting embodiments, the variable R has been used to represent the ratio of the sampling clock frequency (at the digital microphone) to the sampling rate at baseband. In the non-limiting example of FIG. 3, with f_{SF} equal to 2.048 MHz and f_{bb} equal to 16 kHz, then from equation 2 in FIG. 2A, $R=f_{SF}/f_{bb}=128$.”

See also id., claim 26 (16 kHz as a “baseband sampling frequency” or ‘baseband sampling rate”).

F. Claim 5

1. “The non-transitory computer-readable storage medium of claim 1, wherein the first oversampled digital signal and

the second oversampled digital signal are obtained from different sensors.”

442. In my opinion, a POSA would have found claim 5 obvious based on Andersen in view of Swanson.

443. Further, as I mentioned above, oversampled digital beamformers were well-established long before the earliest claimed priority date of the '055 patent, and this included implementations with two or more distinct microphones. Thus, claim 5 represents a straightforward combination of well-known elements to achieve well-understood benefits.

444. Andersen discloses that its hearing aid has “at least two microphone channels (1a, 1b),” with each including a different microphone—microphones “2a and 2b”—and corresponding sigma-delta analog-to-digital converters “3a and 3b.” Ex.1008, Abstract, 3:25-29, Fig.4.

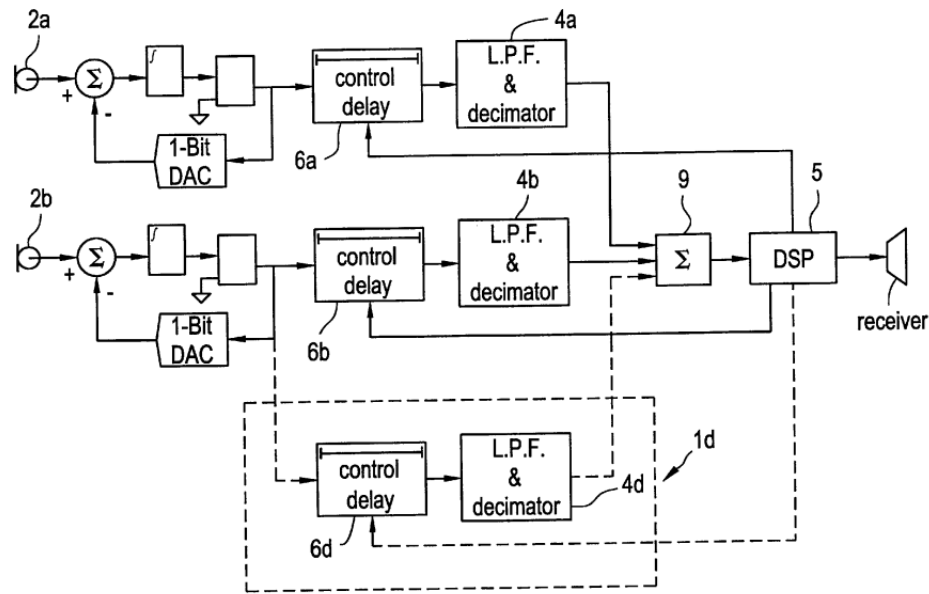
445. As I explained for 1[a]-1[c], Andersen’s first oversampled digital signal is the high-clock-frequency one-bit stream generated from microphone 2a by analog-to-digital converter 3a, and Andersen’s second oversampled digital signal is the high-clock-frequency one-bit stream generated from microphone 2b by analog-to-digital converter 3b. *Supra* §§XVII.C.2-4. Because microphones 2a and 2b are different sensors, Andersen discloses that the first and second oversampled digital signals are obtained from different sensors.

G. Claim 6:

- 1. “The non-transitory computer-readable storage medium of claim 1, wherein the first oversampled digital signal and the second oversampled digital signal are obtained from the same sensor.”**

446. In my opinion, a POSA would have found claim 6 obvious based on Andersen in view of Swanson.

447. Andersen discloses in regard to its Figure 7 that at least one microphone channel includes parallel delay/filter paths derived from the same microphone/sensor, including one path through controllable delay 6b and LPF/decimator 4b and another, dotted-line path through controllable delay 6d and LPF/decimator 4d. Ex.1008, Fig.7, 4:18-27 (“FIG. 7 finally, shows another variation of the inventive circuit in which at least one of the microphone channels has not only one delay device and one digital low pass filter and decimator filter but two of those in parallel. It is also conceivable to have these parallel arrangements in one or more channels, even in all of them. It is also possible to use more than two delay devices in parallel in at least one of said microphone channels, all connected to their respective digital low pass filter and decimator filter of said at least one of said channels.”).



Id., Fig.7.

448. Andersen explains that “at least one of the microphone channels has not only one delay device and one digital low pass filter and decimator filter but two of those in parallel,” and further discloses that more than two delay devices may be used in parallel in the same microphone channel. *Id.*, 4:18-27. Further, Andersen’s claim 11 likewise recites “at least one” microphone channel “equipped with a sigma-delta analog to digital converter including at least two delay devices in parallel operating on two digital low pass filters and decimators,” with the outputs of those parallel paths “being combined in a combination circuit connected to the [DSP].” *Id.*, claim 11.

449. With respect to Andersen’s Figure 7/claim 11 embodiment, the claimed first and second oversampled digital signals correspond to same-channel

high-clock-frequency bit-stream signals derived from the same microphone 2b and sigma-delta converter 3b and provided to the parallel delay paths before the respective LPF/decimators. Thus, Andersen teaches obtaining the first and second oversampled digital signals from the same sensor.

450. This same-sensor mapping remains consistent with claim 1. As I explained for 1[a]-1[b], Andersen outputs and delays oversampled bit streams, and, as I explained for 1[c], Andersen combines corresponding path signals for beamforming and at least renders obvious combining the oversampled bit streams before a common downstream low-pass filtering/decimation. *Supra* §§XVII.C.2-4.

451. For example, regarding 1[a], the signal output from the sigma-delta ADC (connected to microphone 2b) in Figure 7 provides a “first oversampled digital signal output from an analog-to-digital converter (ADC),” with that “first oversampled digital signal” being “responsive to an analog field” (e.g., acoustic input received by microphone 2b) “and the first oversampled digital signal is

created at a sampling clock frequency” of the sigma-delta ADC. *See, e.g.*, Ex.1008, 3:19-22, 3:25-29, 4:18-27, Fig.7.⁹

452. Regarding 1[b], the “first oversampled digital signal” that would pass through “control delay” 6b, in Figure 7, results in “delaying the first oversampled digital signal by a time delay wherein the time delay is equal to an integer number of sampling clock cycles to produce a time delayed first oversampled digital signal.” *See, e.g., id.*, 3:31-36 (explaining that the delay “is typically a multiple tap shift register” and that digital signal processor (DSP) 5 “will decide how many 1 bit stages each sample of the bit stream will go through (and thus be delayed by)” before being tapped and sent further in the system), 3:51-56, Fig.7. Andersen further discloses that the time delay equals an integer number of sampling-clock cycles, namely $N \times 1/f_s$, where N is an integer number of sampling-clock cycles, and f_s is the sampling frequency. *See, e.g., supra* §XVII.C.3; Ex.1008, 3:4-22, 3:30-

⁹ Ex.1008, 3:46-51 (“FIG. 4 shows a further embodiment of the invention. All parts and components which are the same as in FIG. 3 are designated with the same reference numerals and need not to be described again. **This holds true for all other FIGS. as well so that only the differences will be explained in detail.**”) (emphasis added).

38; 1:51-57, 3:31-39; 2:21-25. Thus, Andersen delays the oversampled one-bit digital signal output of the sigma-delta analog-to-digital converter, corresponding to the claimed first oversampled digital signal, to produce a time-delayed oversampled digital signal before the signal reaches the low-pass filter and decimator.

453. Regarding 1[c], Andersen discloses combining the outputs of the two same-sensor parallel delay/filter paths in combination circuit 9. Ex.1008, 4:13-27, Fig.7, claim 11. The second oversampled digital signal is responsive to the acoustic field received by microphone 2b, and the combination produces the beamformed digital signal.

454. In my opinion, a POSA would have been motivated to use Andersen's disclosed Figure 7/claim 11 same-sensor parallel-path embodiment in the Andersen-Swanson combination because Andersen presents that embodiment as another implementation of the same sigma-delta microphone-channel beamformer using the same type of delay, and the parallel paths provide additional delay/beamforming flexibility without requiring another microphone or converter. This combination incorporating the teaching of the Fig.7/claim 11 same-sensor parallel path embodiment would have had the benefit of increased directional/focusing flexibility without needing an additional sensor or an additional analog to digital converter. *See id.*, 2:60-62 (“[B]y controlling the

various delay devices, other directional patterns could be realized.”), 4:18-27, Fig.7, claim 11. A POSA would have had a reasonable expectation of success since the combination uses known elements having known functions, as disclosed by Andersen.

H. Claim 7

1. **“The non-transitory computer-readable storage medium of claim 1, further comprising: applying a low pass filter with decimation to the time delayed first oversampled digital signal to output a baseband digital signal that is delayed by the time delay.”**

455. In my opinion, a POSA would have found claim 7 obvious based on Andersen in view of Swanson.

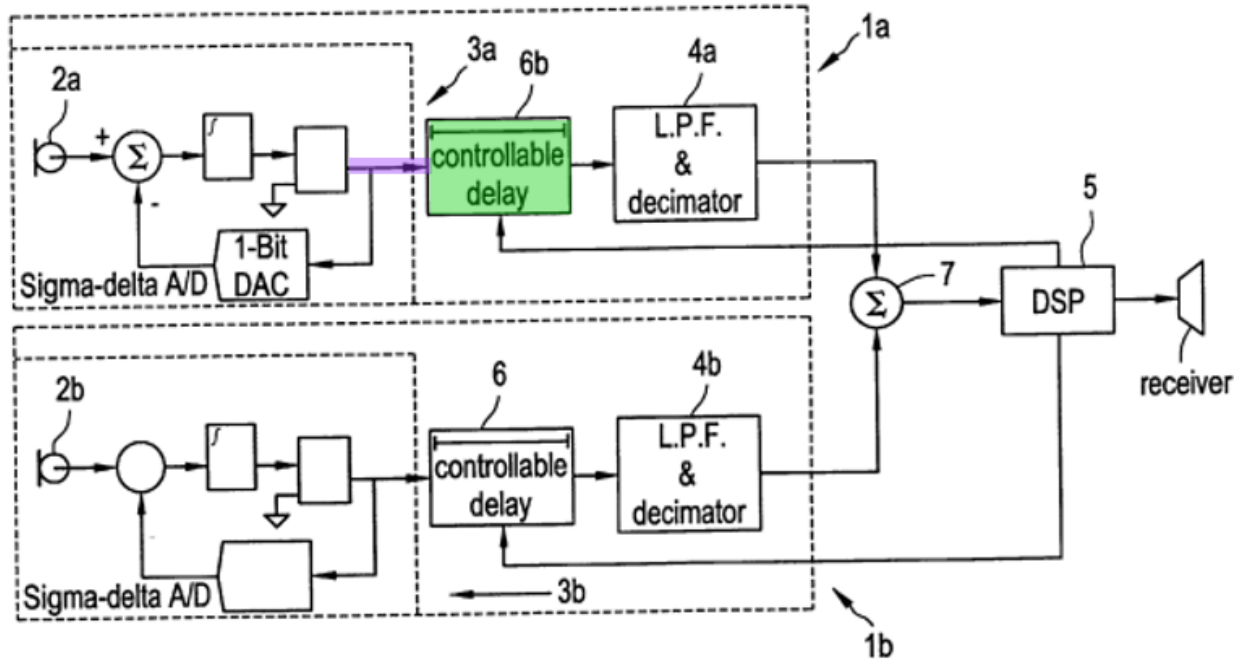
456. As a first matter and as explained in this declaration’s Technical Background section above, digital beamforming systems that used combinations of oversampling, delaying, filtering, decimation and combiners were well established long before the earliest claimed priority date of the ’055 patent. *See supra* §VI. Thus, claim 7 represents a straightforward combination of well-known elements to achieve well-understood benefits.

457. As I explained for 1[a]-1[b], Andersen discloses that controllable delay device 6 delays the first oversampled digital signal—i.e., the sigma-delta analog-to-digital converter’s one-bit output stream—before that delayed signal is sent to the digital low-pass filter and decimator. *Supra* §§XVII.C.2-3. Andersen further

discloses that each microphone channel includes a “digital low pass filter and decimator” 4 that converts the high-clock-frequency one-bit stream into a sequence of digital words at a lower clock frequency, e.g., 16 or 32 kHz. Ex.1008, Abstract, 3:4-18. Thus, Andersen discloses applying a low-pass filter with decimation to the time-delayed first oversampled digital signal.

458. Andersen’s low-pass filter/decimator outputs the claimed baseband digital signal delayed by the time delay. As I explained for claim 4, the ’055 patent’s “baseband” signal domain includes post-low-pass-filter/decimator digital signals at baseband sampling rates, and the ’055 patent identifies 16 kHz as a baseband sampling frequency/rate. *Supra* §XVII.E. Andersen likewise discloses that its LPF/decimator converts the delayed high-clock-frequency bit stream into lower-frequency digital words, including at 16 or 32 kHz. Ex.1008, 3:4-18, 3:30-38. Given that the delay is imposed upstream of the LPF/decimator, the LPF/decimator processes the already-delayed bitstream, and its lower-rate/baseband digital output remains delayed by that same selected time delay.

459. Andersen’s Figure 4 illustrates this arrangement. Specifically, in the upper channel, the first oversampled digital signal (purple) is delayed by controllable delay device 6b (green) before being provided to LPF/decimator 4a, which outputs the corresponding lower-rate/baseband digital signal for downstream processing and beamforming:



Id., Fig.4.

I. Claim 8

1. “The non-transitory computer-readable storage medium of claim 7, wherein the time delay is equal to a fraction of a baseband sampling period.”

460. In my opinion, a POSA would have found claim 8 obvious based on Andersen in view of Swanson.

461. As an initial matter, as discussed in this declaration’s Technical Background section above, digital beamforming systems which relied on oversampled input signals, followed by delays and filters and decimation were well-known and in wide use long before the earliest claimed priority date of the ’055 patent. *See supra* §VI. Thus, claim 8 represents a straightforward combination of well-known elements to achieve well-understood benefits.

462. As I explained for 1[b] and claim 7, Andersen delays the oversampled bit stream before the LPF/decimator, and the LPF/decimator outputs the corresponding baseband digital signal. *Supra* §§XVII.C.3, H. Andersen explains that conventional hearing-aid sampling intervals are “normally 32 usec,” while “desired delay between two or more microphone signals” is “typically less than 32 usec,” e.g., 15 usec. Ex.1008, 1:20-25. To realize such short delays, Andersen uses a sigma-delta converter clocked at, e.g., 1 MHz or higher, together with a controllable digital delay line/tapped shift register in the bit stream, thereby providing controllable delays as short as 1 usec and “delayed difference steps of multiples of 1 usec.” *Id.*, 1:50-56; *see also id.*, 2:21-25 (realizing “delays as short as 1 usec”).

463. That aforementioned disclosure concerns the delay itself, not simply a resolution increment. As acknowledged by Andersen, the “resulting delay” equals the number of delay stages times the inverse sampling rate. Thus, selecting one 1-MHz delay stage yields an actual 1-usec delay. Ex.1008, 3:30-38. Andersen’s LPF/decimator converts the high-clock-frequency bit stream into lower-frequency/baseband digital word sequences, e.g., at 16 or 32 kHz. *Id.*, 3:4-16. Those lower-frequency/baseband output rates correspond to baseband sampling periods of 31.25 usec at 32 kHz and 62.5 usec at 16 kHz. *Id.*; *see* Ex.1008, 1:20-25. Thus, Andersen’s disclosed 1-usec delay, as well as other disclosed delays less

than a baseband period, such as the 15-usec example, are fractions of a baseband sampling period.

J. Claim 9

- 1. “The non-transitory computer-readable storage medium of claim 7, wherein the time delay is greater than a baseband sampling period.”**

464. In my opinion, a POSA would have found claim 9 obvious based on Andersen in view of Swanson.

465. As an initial matter, as discussed in this declaration’s Technical Background section above, digital beamforming systems which relied on oversampled input signals, followed by delays and filters and decimation were well-known and in wide use long before the earliest claimed priority date of the ’055 patent. *See supra* §VI. Thus, claim 9 represents a straightforward combination of well-known elements to achieve well-understood benefits.

466. As Andersen discloses, its controllable delay device is typically a multiple-tap shift register, and the DSP determines how many stages of that shift register the one-bit sigma-delta output samples traverse. Ex.1008, 3:31-36. Andersen also explains that, with a sigma-delta analog-to-digital converter clocked at “f.i. 1 MHz,” the system provides “delayed difference steps of multiple of 1 usec,” and that “[t]he resulting delay is equal to the number of stages times the

inverse sampling rate.” *Id.*, 1:50-56, 3:36-38. Thus, Andersen’s programmable delay is selectable in 1-usec increments.

467. Andersen further discloses that its digital low-pass filter/decimator operates at a lower clock frequency, including “10 to 50 kHz,” and in one example converts the one-bit stream into digital words at “f.i. 16 or 32 kHz.” *Id.*, 2:17-25, 3:12-18. These lower-rate/baseband outputs correspond to baseband sampling periods of 20 usec at 50 kHz, 31.25 usec at 32 kHz, and 62.5 usec at 16 kHz. *See also id.*, 1:20-29, 3:36-38.

468. Given that Andersen’s DSP-controlled delay line selects the number of high-rate shift-register stages used to impose delay, a POSA would have understood that selecting more than the corresponding number of 1-usec stages imposes a delay greater than a baseband sampling period—e.g., more than 20 stages for a 50 kHz baseband output or more than 32 stages for a 32 kHz output.

469. A POSA would have been motivated to select such a number of stages when needed to achieve Andersen’s desired beamforming delay/directional orientation, because Andersen’s delay line is specifically provided so the DSP can actively control beam direction using the high-rate bitstream delay prior to low-pass filtering/decimation. *See id.*, 1:40-57, 3:30-45. Implementing the selected delay in Andersen’s existing high-rate delay line also would avoid needing a separate downstream integer-delay element or moving the decimator upstream of the delay.

470. While Andersen explains that the “desired delay between two or more microphone signals are typically less than 32 usec” in digital hearing aids (*id.*, 1:21-24), a POSA would have understood that this “typical” value was not a hard design ceiling. Because Andersen’s DSP-controlled delay line is the mechanism used to actively control the hearing aid’s beam direction, a POSA would have been motivated to provide delay-range headroom—using additional 1-usec high-rate shift-register stages—to accommodate different microphone spacings, housing geometries, desired directional patterns, and fitting/acoustic conditions, while still avoiding the interpolation, processing, space, and power costs that Andersen sought to avoid. That design margin would have been particularly useful in a hearing aid because insufficient delay range could prevent the device from achieving the intended directional response, reducing the expected speech enhancement and noise-rejection benefits of the beamformer.

471. In any event, implementing the system to accommodate the typical delay (e.g., 32 us) would amount to a 32-stage delay line operating at the oversampled 1 MHz, which would allow for the time delay to be 32 us. This time delay is greater than the baseband sampling period for many baseband frequencies in the range “10 to 50 kHz,” that Andersen discloses for its system. *See id.*, 2:21-25. For example, for a baseband frequency of 50 kHz, the baseband sampling

period equals 20 usec, which is lower than the total delay available for a 32-stage delay line operating with a 1 us/stage accessible delay.

XVIII. GROUND 9: CLAIM 3 IS OBVIOUS BASED ON ANDERSEN, SWANSON, AND LIU

472. In my opinion, a POSA would have found claim 3 obvious based on Andersen in view of Swanson and Liu.

A. Motivation to Combine

473. In my opinion, a POSA would have been motivated to apply Liu's multi-staged reconstruction/decimation teaching to the Andersen-Swanson combination (as discussed in Ground 8 above) to reduce the per-channel data rate to an intermediate sampling frequency before summation and further reconstructing/decimating to the final operating frequency after summation. This implementation would have avoided operation at the two extremes described by Liu, namely summing at the peak oversampled rate or summing at the final desired operational frequency.

474. Andersen discloses a beamforming implementation with multiple microphones, oversampling sigma-delta analog-to-digital converters, and delay elements, and in which per-channel LPF/decimators 4a/4b filter and decimate each delayed channel signal prior to summing at a summing circuit 7. Ex.1008, Abstract, 3:4-18, 3:30-38.

475. Similar to Andersen and Swanson, Liu discloses a system for beamforming that includes oversampling analog-to-digital converters 14, a memory/delay controller 28 for delaying digital samples, reconstruction/decimation filters 18 and 26, and a summer 24 for combining digital samples. Ex.1007, Abstract, [0025], [0029]-[0030], [0032]-[0035], [0038]-[0040], Fig.2.

476. Liu, consistent with the Andersen-Swanson combination (including its performance of LPF/decimation before summing), describes that performing summation/combination at the ADC oversampling rate may result in dynamic receive artifacts. Ex.1007 (Liu), [0020] (“In one extreme, there is no channel demodulation and the beam sum is computed at the sigma delta rate. This first extreme often leads to dynamic receive artifacts.”); *see also* Ex.1008 (Andersen), Abstract, 3:4-18, 3:30-38, 3:57-59.

477. Liu identifies multistage reconstruction/decimation, performed both before and after summation, as an advantageous alternative to summing at the ADC oversampled rate or the final operating frequency.

478. With that staged approach, Liu teaches signal combination/summation being performed “at a data rate less than output by the initial oversampling and greater than the Nyquist rate or other rate above the Nyquist rate,” which occurs prior to summation, and that “[a]fter summation, the samples are reconstructed at a Nyquist or other rate.” Ex.1007, [0055]-[0057], Abstract, [0006], [0052].

479. In other words, Liu's first reconstruction/decimation filter 18 "outputs signals oversampled less than output by the oversampling converters 14 and more than output by the second filter 26," and Liu's summer 24 sums those signals. *Id.*, [0035], [0038]. The second reconstruction/decimation filter 26 receives the summed signal and "filter[s]" and "decimate[s]" to produce the beamforming output." *Id.*, [0039], [0057], Figs.2, 7.

480. A POSA would have recognized based on Liu that reconstructing/decimating to an intermediate frequency before summing reduces the need for "long demodulation filters ... for each channel." *Id.*, [0020] ("In another extreme, complete channel demodulation is provided by long low-pass filters for each channel and the beam sum is computed at the signal Nyquist rate. The second extreme is complicated because of the long demodulation filters required for each channel, making the approach expensive and unsuitable for implementation with parallel beamforming because the long channel filters have to be duplicated or time-multiplexed.").

481. A POSA would have been motivated to incorporate Liu's teachings regarding multi-stage reconstruction/decimation into the Andersen-Swanson architecture. The combination, consistent with the teachings of Andersen, Swanson, and Liu, would have provided the first-stage reconstruction/decimation to an intermediate frequency by so configuring Andersen's LPF/decimators 4a/4b,

which would have allowed a POSA to preserve the Andersen-Swanson combination's fine delay resolution. In that implementation, Andersen's summing circuit 7 combines the delayed first-channel signal and second-channel signal after partial decimation but before final post-summation decimation, at a rate below the sigma-delta converter clock rate and above the later output/baseband rate. Accordingly, the combining would be performed at an intermediate sampling rate.

B. Reasonable Expectation of Success

482. In my opinion, a POSA would have had a reasonable expectation of success in integrating Liu's teachings regarding multi-stage reconstruction/decimation in the Andersen-Swanson system.

483. First, the combination addresses the implementation of decimation filtering, which has been well-known in the field of beamforming and signal processing before the earliest claimed priority date. *See, e.g.*, Ex.1021 (L. Milic, Multirate Filters: An Overview, *APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, 2006, pp. 912-915), at p. 1 (Abstract) ("Multirate filtering techniques are widely used in ... sampling rate conversion systems..."); *id.* ("A multirate filter is a digital filter that changes the input sampling rate of the input signal into another desired one. These filters are of an essential importance in communications, image processing, digital audio, and multimedia.").

484. Both Andersen and Liu, in addition to teaching decimation filtering, teach beamforming summation, including summation of signals at sampling rates decimated (or downsampled) from the ADC oversampled rate. *See, e.g.*, Ex.1008 (Andersen), Fig.4, 3:4-22, 3:46-62; *see also id.*, 3:25-45; Ex.1007 (Liu), [0032]-[0035], [0038]-[0040], Figs.2, 7.

485. Both Andersen and Liu likewise recognize the benefit of performing delay at the ADC oversampled rate, which provides fine delay resolution, and then providing decimating filters to downsample the signals before summation. *See, e.g.*, Ex.1008 (Andersen), Fig.4, 3:30-45, 3:46-62; Ex.1007 (Liu), [0032]-[0035], [0038]-[0040], Figs.2, 7.

486. Andersen already discloses per-channel LPF/decimators feeding a summing circuit, confirming that reducing the sampling rate before summation and summing at that lower rate were already features of the Andersen-Swanson combination. Ex.1008, 3:12-18, 3:57-59. Liu likewise confirms the viability of pre-summation reconstruction/decimation to a frequency below the ADC oversampling rate; summation of reconstructed/decimated signals at that lower sampling rate; and further demonstrates the viability of post-summation reconstruction/decimation to reduce the sampling frequency further. Ex.1007, [0038]-[0040], [0057]. Thus, the modification resulting in the Andersen-Swanson-Liu combination applies known components according to their known functions.

487. Thus, in my opinion, applying Liu's staged-reconstruction teaching to the Andersen-Swanson combination would have yielded predictable results, with a reasonable expectation of success.

C. Claim 3

1. "The non-transitory computer-readable storage medium of claim 1, wherein the combining is performed at an intermediate sampling rate."

488. In my opinion, a POSA would have found claim 3 obvious based on Andersen in view of Swanson and Liu.

489. Further, as mentioned above, oversampled digital beamformers were well-established at the time of the '055 patent's earliest claimed priority date. Claim 3 represents a straightforward combination of well-known elements to achieve well-understood benefits.

490. As I explained for claim 1 in Ground 8, the Andersen-Swanson combination renders obvious claim 1, and discloses a beamforming implementation with multiple microphones, oversampling sigma-delta analog-to-digital converters, and delay elements, and in which per-channel LPF/decimators 4a/4b filter and decimate each delayed channel signal prior to summing at a summing circuit 7. Ex.1008, Abstract, 3:4-18, 3:30-38. *Supra* §XVII.C.

491. As I also explained for claim 3 in Grounds 2 and 4, Liu discloses multi-stage reconstruction/decimation in which pre-summation filter 18 partially

reconstructs/decimates the delayed channel samples to a sampling rate below the initial oversampling analog-to-digital converter rate but above the rate achieved after post-summation reconstruction/decimation, so summation occurs at an intermediate sampling rate. *Supra* §§XI.A-C, XIII.E.

492. A POSA would have been motivated to apply Liu's staged-reconstruction teaching to the Andersen-Swanson combination by configuring Andersen's per-channel LPF/decimators 4a/4b as first, partial reconstruction/decimation filters and using a common post-summation reconstruction (low-pass)/decimation stage—e.g., between summing circuit 7 and DSP 5 or within DSP 5—to complete reconstruction/decimation after summation. In that implementation, Andersen's summing circuit 7 combines (sums) the delayed first-channel digital signal and second-channel digital signal after partial decimation but before final post-summation decimation, and thus at a rate below the sigma-delta ADC clock rate and above the later output/operating frequency. Accordingly, the combining would be performed at an intermediate sampling rate.

493. A POSA would have been motivated to apply Liu's staged-reconstruction/decimation teaching to the Andersen-Swanson combination (as discussed in Ground 8 above) to reduce the per-channel data rate to an intermediate sampling frequency before summation and further reconstructing/decimating to the final operating frequency after summation. *See supra* §XVIII.A. Andersen already

discloses delaying oversampled signals (from a microphone) before the signals are input to per-channel LPF/decimators and output to a summing circuit and downstream DSP, confirming that reducing the frequency to less than the ADC oversampling rate after delay and before summation was already a feature of the Andersen-Swanson combination. Ex.1008, 3:4-18, 3:30-38, 3:57-59.

494. Liu teaches a staged reconstruction/decimation alternative in which a first reconstruction/decimation filter partially reconstructs/decimates each delayed channel before summation, and a common second-stage filter completes reconstruction/decimation after summation, thereby reducing the per-channel filtering burden while avoiding summing directly at the sigma-delta rate. Ex.1007, [0019]-[0020], [0035], [0052], [0055]-[0057]. Applying that teaching to the Andersen-Swanson combination would have predictably reduced per-channel data rate/filter complexity before summing while using a common downstream stage to finish reconstruction/decimation of the beam sum to the desired operating frequency.

495. A POSA would have had a reasonable expectation of success implementing the Andersen-Swanson-Liu combination because the modification uses known components for their known functions: Andersen's sigma-delta analog-to-digital converters, controllable delays, LPF/decimators, summing circuit, and DSP, together with Liu's staged reconstruction/decimation arrangement. Also, the

modification would not create any incompatibility with Andersen's DSP 5 because Andersen already discloses that LPF/decimator outputs digital word sequences for DSP processing, and Liu likewise discloses summing and post-summation reconstruction/decimation. *See* Ex.1008, 3:12-18, 3:57-59; Ex.1007, [0038]-[0040], [0057].

XIX. GROUND 10: CLAIM 9 IS OBVIOUS BASED ON ANDERSEN, SWANSON, AND NOUJAIM

496. In my opinion, a POSA would have found claim 9 obvious based on Andersen in view of Swanson, as I explained in Ground 8 (*supra* §XVII.J). It is also my opinion that a POSA would have found claim 9 obvious based on the Andersen-Swanson combination in view of Noujaim.

A. Motivation to Combine

497. In my opinion, a POSA would have been motivated to apply Noujaim's multi-stage high-rate delay-register teaching to the Andersen-Swanson combination to extend the selectable delay range beyond the baseband sampling period.

498. Andersen discloses a DSP-controlled multiple-tap shift register delay line operating on sigma-delta oversampled bitstreams before low-pass filtering/decimation, with the total delay controlled by selecting the number of high-rate delay stages traversed. Ex.1008, 1:40-57, 2:17-25, 3:30-45; *supra* §XVII.

499. Andersen also explains that, with a sigma-delta analog-to-digital converter clocked at “f.i. 1 MHz,” the system provides “delayed difference steps of multiple of 1 usec,” and that “[t]he resulting delay is equal to the number of stages times the inverse sampling rate.” *Id.*, 1:50-56, 3:36-38. Thus, Andersen’s programmable delay is selectable in 1-usec (1-microsecond) increments. The total delay would be equal to 1 us multiplied by the number of delay stages traversed.

500. Andersen’s LPF/decimator outputs digital word sequences at frequencies of 16 or 32 kHz (e.g., operational or baseband frequencies in this system), and also discloses baseband frequencies as high as 50 kHz. *Id.*, 3:4-18 (disclosing that the “digital low pass filter and decimator filter operates at a clock frequency of f.i. 32 kHz and converts the 1 bit stream of a clock frequency of about 1 MHz into a sequence of data words at the lower frequency, f.i. 16 or 32 kHz.”); *see also id.*, 2:21-25 (“In order to realize controllable delays as short as 1 usec it is of advantage to use a clock frequency for the sigma delta ADC in the range of 1 MHz or even higher and a clock frequency in the area of 10 to 50 kHz for the digital low pass filter and decimator filter.”). These sampling frequencies, 16 and 32 kHz,

correspond to sampling periods of 62.5 us (which equals 1/16kHz) and 31.25 us (which equals 1/32kHz), respectively.¹⁰

501. Noujaim discloses the same general high-rate-delay principle. More specifically, Noujaim discloses the use of delay shift registers up to 80 stages in length operating on oversampled bitstreams prior to decimation, with the desired time delay selected based on the number of shift-register stages through which the signal traverses before it is output. Ex.1010, Abstract, 8:65-9:42, 10:22-40.

502. In my opinion, a POSA would have been motivated, for example, to apply Noujaim's 80-stage delay-register teaching to Andersen's 1 MHz sigma-delta oversampled bitstream delay line to extend Andersen's selectable delay range, up to 80 us, beyond Andersen's 31.25 us and 62.5 us baseband sampling periods (corresponding to operating at a 32 kHz or 16 kHz baseband frequency), to provide more flexibility in terms of being able to accommodate larger delays for

¹⁰ Additionally, operating at the 50 kHz baseband frequency would mean a baseband sampling period of 20 us (which is equal to 1/50kHz).

beamforming, thereby providing a reliable beamforming system for hearing aid applications, as desired by Andersen.¹¹

B. Reasonable Expectation of Success

503. In my opinion, a POSA would have had a reasonable expectation of success combining the Andersen-Swanson combination with Noujaim.

504. Both Andersen and Noujaim disclose the same fundamental architecture: sigma-delta oversampled bitstream delay registers operating before decimation, with delay selected by choosing the output tap. Ex.1008, 1:40-57, 3:30-45; Ex.1010, 8:65-9:42, 10:22-40. Applying Noujaim's multi-stage delay-register teaching to Andersen's sigma-delta bitstream delay line is a straightforward scaling of a known component performing its known function. The combination would have extended the same delay-line implementation in the Andersen-Swanson combination without changing its operation.

¹¹ As discussed above in Ground 8 (*supra* §XVII.J), while Andersen explains that the “desired delay between two or more microphone signals are typically less than 32 usec” in digital hearing aids (Ex.1008, 1:21-24), a POSA would be motivated to design its system, and its accessible delay, to be operable beyond just “typical” conditions. For example, a POSA would design the system to accommodate larger delays.

505. Thus, in my opinion, applying Noujaim's teachings regarding multi-stage delay-register length to Andersen's architecture would have yielded predictable results, with a reasonable expectation of success.

C. Claim 9

1. "The non-transitory computer-readable storage medium of claim 7, wherein the time delay is greater than a baseband sampling period."

506. In my opinion, a POSA would have found claim 9 obvious based on Andersen in view of Swanson, as I explained in Ground 8 (*supra* §XVII.J). It is also my opinion that a POSA would have found claim 9 obvious based on the Andersen-Swanson combination in view of Noujaim.

507. As an initial matter, as discussed in this declaration's Technical Background section above, digital beamforming systems which relied on oversampled input signals, followed by delays and filters and decimation were well-known and in wide use long before the earliest claimed priority date of the '055 patent. *See supra* §VI. Thus, claim 9 represents a straightforward combination of well-known elements to achieve well-understood benefits.

508. As I explained for claim 7 in Ground 8, the Andersen-Swanson combination renders obvious claim 7, with Andersen providing a DSP-controlled multiple-tap shift register delay line operating on sigma-delta oversampled bitstreams prior to low-pass filtering/decimation, with the total delay controlled by

selecting the number of high-rate delay stages traversed. *Supra* §XVII.H. Andersen's LPF/decimator outputs lower-frequency/baseband digital word sequences, e.g., at 16 or 32 kHz, corresponding to baseband sampling periods of 62.5 us and 31.25 us. Ex.1008, 3:4-18.

509. Noujaim teaches the same high-rate-delay principle in beamforming. Noujaim discloses sigma-delta modulators that output one-bit digital signals, variable delay shift registers that delay those signals before summation, and a decimator that later reduces the beam-data sample rate. Ex.1010, Abstract, 3:26-4:5, 8:65-9:42, 10:22-40. Noujaim teaches delay registers that are "80 stages in length," and the desired time delay is selected based on the shift-register stage from which the signal is output. *Id.*, 9:22-42.

510. A POSA would have been motivated to apply Noujaim's multi-stage high-rate delay-register teaching to the Andersen-Swanson combination to provide for situations when the desired beamforming delay exceeded the later lower-rate/baseband sampling period. *See also supra* §XIX.A. Andersen already discloses controlling beam direction by selecting the number of high-rate delay stages traversed before low-pass filtering/decimation, which achieves fine delay resolution without downstream interpolation. Ex.1008, 1:40-57, 3:30-45. Noujaim confirms that, in oversampled beamforming, high-rate delay registers may include many stages—e.g., 80 stages—and that the desired time delay is selected based on

the shift-register stage from which the signal is output. Ex.1010, Abstract, 8:65-9:42, 10:22-40. Applying Noujaim's 80-stage delay-register teaching to Andersen's 1 MHz sigma-delta modulated bitstream delay line would have predictably extended Andersen's selectable delay range up to 80 us, exceeding Andersen's 31.25-us and 62.5-us sampling periods of Andersen's 32-kHz and 16-kHz post-decimation digital-word outputs. *See also supra* §XIX.B.

XX. GROUND 11: CLAIM 10 IS OBVIOUS BASED ON ANDERSEN, SWANSON, AND DEAN

511. In my opinion, a POSA would have found claim 10 obvious based on Andersen in view of Swanson and Dean.

A. Motivation to Combine

512. In my opinion, a POSA would have been motivated to apply Dean's multi-bit oversampled-output teaching to the Andersen-Swanson combination to implement Andersen's oversampled analog-to-digital converter and subsequent delay path with samples more than one bit deep.

513. As I explained for claim 1 above, the Andersen-Swanson combination discloses or suggests a non-transitory computer-readable storage medium storing program code for causing a data processing system to perform the claimed beamforming steps. *Supra* §XVII.C. Andersen discloses oversampled digitization, digital delay, and downstream decimation. Ex.1008, 3:4-18, 3:30-38, 3:57-59.

Andersen discloses that its delta-sigma modulators (analog-to-digital converters) output oversampled single-bit digital signals. *Id.*, 3:4-7 (disclosing “1 bit ADC”).

514. Andersen teaches that its low-pass filters/decimators convert the one-bit oversampled streams into lower-rate multi-bit words, for example 20-bit words at 16 or 32 kHz, and that those lower-rate words are then combined in summing circuit 7. *Id.*, 3:12-18 (“The digital low pass filter and decimator filter operates at a clock frequency of f.i. 32 kHz and converts the 1 bit stream of a clock frequency of about 1 MHz into a sequence of data words at the lower frequency, f.i. 16 or 32 kHz. These data words could e.g. be 20 bit wide. These data words are then, normally, applied to a programmable or program controlled digital signal processor.”), 3:57-59.

515. Andersen also is directed to “hearing aids.” *Id.*, Title (“Hearing aid with beam forming properties”), Abstract, 1:40-47, 1:64-2:15, 2:66-3:3, claims 1-12.

516. Dean teaches a beamforming array in which oversampled signals are delayed and decimated—but Dean’s system may be implemented with multi-bit oversampled outputs rather than one-bit sigma-delta streams, especially where per-sample amplitude information, dynamic range, or a different oversampling-rate/bit-depth tradeoff is desired (e.g., in high-information-flow applications). Ex.1009, 1:44-66, 3:54-60, 6:18-40, claim 8. In such cases, Dean’s system includes multi-

bit shift-register delay elements, multi-bit adders for combining, and a suitable decimating filter. *Id.* To achieve the multi-bit oversampled output, Dean discloses “a noise shaping analogue to digital converter” that includes a sampling loop 24 that outputs “a series of n-bit representations of the signal from the sensor module at an oversampled rate.” *Id.*, 6:17-40, Fig.4. As Dean teaches, n, which is the number of bits, is “less than the number of bits required to represent the dynamic range.” *Id.*, 4:8-12.

517. In my opinion, a POSA would have been motivated to apply Dean’s multi-bit oversampled-output teaching to the Andersen-Swanson combination (*supra* §XVII) so that Andersen’s first oversampled digital signal is digitized into samples more than one bit deep. This combination would have taken advantage of the bit-depth/oversampling-rate design tradeoff disclosed by Dean, while preserving Andersen’s beamforming flow. Also, considering the application that the Andersen-Swanson combination is directed to—hearing aids—a POSA would be especially interested in multi-bit samples because in such applications, as a POSA would have understood, greater dynamic range is desired, and Dean teaches using more than one bit when the bit-depth/oversampling-rate tradeoff favors greater per-sample amplitude information or dynamic range. Ex.1008, 3:4-18, 3:30-38, 3:57-59; Ex.1009, 1:44-57, 6:18-40. That motivation would have been reinforced by Andersen’s hearing-aid application, where a POSA would have

understood usable acoustic dynamic range to be important. Ex.1008, Abstract, 1:64-2:4. Applying Dean's multi-bit oversampled implementation to Andersen would have predictably preserved Andersen's beamforming flow while using a known bit-depth/oversampling-rate design tradeoff.

B. Reasonable Expectation of Success

518. In my opinion, a POSA would have had a reasonable expectation of success in combining Dean's teachings regarding multi-bit deep digitization with the Andersen-Swanson combination (*supra* §XVII).

519. First, the combination of Andersen and Swanson with Dean addresses the implementation of multi-bit digitizers, which were well-known in the field of beamforming and signal processing long before the earliest claimed priority date. *See, e.g.*, Ex.1023 (J. Yu et al., A low-power multi-bit $\Sigma\Delta$ modulator in 90-nm digital CMOS without DEM, in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2428-2436, Dec. 2005), 1 ("Multi-bit sigma-delta modulators are widely used in analog-to-digital conversion especially in the modern deep-sub-micron CMOS process.").

520. Second, both Andersen and Dean teach combining multi-bit signals in their respective beamforming processes. *See, e.g.*, Ex.1008, 3:12-59 (emphasis added):

“The digital low pass filter and decimator filter operates at a clock frequency of f.i. 32 kHz and converts the 1 bit stream of a clock frequency of about 1 MHz into a **sequence of data words at the lower frequency, f.i. 16 or 32 kHz. These data words could e.g. be 20 bit wide.** These data words are then, normally, applied to a programmable or program controlled digital signal processor.

...

The output signals of the digital low pass filter and decimator filters 4 a and 4 b are combined in a summing circuit 7 and passed on to the DSP.”

See also Ex.1008, Fig.4; Ex.1009, 6:21-40 (emphasis added):

“In some applications, for example, if a very fast information flow is required. The trade-off between the number of bits in the oversampled domain and the rate of oversampling is such that a lower sampling rate with more bits is preferred. A type of analogue to digital converter with this property is a noise shaping analogue to digital converter, such as is shown in FIG. 4. Such a converter can also be split into a sampling loop 24 and a decimating filter 26 in a similar manner to the sigma delta converter of FIG. 1. The sampling loop 24 comprises a subtraction means 24a, an integrator 24b, an n-bit analogue to digital converter 24c, a latch circuit 24d and a digital to analogue converter 24e, connected in series in a loop. **The output of the latch circuit 24d is a series of n-bit representations of the signal from the sensor module at an oversampled rate. If the first part of a noise shaping analogue to digital converter, the sampling loop 24, is used to produce an output of n-bit data in place of each one of the sampling loops 4₁ to 4_j in the array shown in FIG. 3 then n-bit element shift registers can be used instead of the 1-bit element shift registers 14₁ to 14_j and an n-bit adder can be used in place of the one-bit adder 16.** A suitable decimating filter 26 could then be used to convert the resulting data to the number of bits required to represent the entire dynamic range of the intermediate frequency signal.”

See also Ex.1009, claim 1.

521. Third, modifying the Andersen-Swanson combination (*supra* §XVII.C) in view of the teachings of Dean would be accomplished using conventional multi-bit digitizers that were well known in the art before the earliest claimed priority date.

522. As such, a POSA would have had a reasonable expectation of success combining the teachings of Dean with the Andersen-Swanson arrangement.

C. Claim 10

- 1. “The non-transitory computer-readable storage medium of claim 7, wherein the first oversampled digital signal is digitized to create samples which are more than one bit deep.”**

523. In my opinion, a POSA would have found claim 10 obvious based on Andersen, Swanson, and Dean.

524. As a first matter, as explained in the Technical Background section of this declaration, digital beamforming systems which relied on oversampled input signals, followed by various combinations of delays and filters and decimation were well-known and in wide use long before the '055 patent's earliest claimed priority date. *See supra* §VI. A POSA would have understood that before the time of the '055 patent's earliest claimed priority date, it was known that there were benefits to various combinations of these elements depending on the capabilities of each element, the characteristics of the incoming signals, and the requirements for the

resulting combined signals. Thus, claim 10 represents a straightforward combination of well-known elements to achieve well-understood benefits.

525. As I explained for claim 7 in Ground 8, Andersen and Swanson render obvious claim 7, and Andersen provides a DSP-controlled tapped delay line in the sigma-delta bitstream before low-pass filtering/decimation. *Supra* §XVII.H.

526. As I explained for claim 10 in Ground 3, Dean teaches implementing oversampled beamforming using n-bit digital signals at an oversampling rate, including samples more than one bit deep, with corresponding n-bit delay/shift-register, adder, and decimation structures when the bit-depth/oversampling-rate tradeoff favors more bits. *Supra* §XII.C.

527. A POSA would have been motivated to implement Andersen's oversampled converter and subsequent delay path using Dean's multi-bit oversampled-output teaching so that Andersen's first oversampled digital signal is digitized into samples more than one bit deep. A POSA would have been motivated to do so for the reasons explained in Ground 3 (*supra* §XII) and because Andersen and Dean both use oversampled digitization, digital delay/beamforming, and downstream decimation; applying Dean's multi-bit oversampled implementation to the Andersen-Swanson combination would have predictably preserved Andersen's beamforming flow while using a known bit-depth/oversampling-rate design tradeoff. *See* Ex.1008, 3:4-18, 3:30-38, 3:57-59; Ex.1009, 1:44-57, 6:18-40. Also,

considering the application that the Andersen-Swanson combination is directed to—hearing aids—a POSA would be especially interested in multi-bit samples because in such applications, as a POSA would have understood, greater dynamic range is desired and could be achieved by digitizing to create samples more than one bit deep. A POSA would have had a reasonable expectation of success because Dean teaches the corresponding multi-bit implementation details—n-bit oversampled outputs, n-bit shift-register elements for delay, n-bit adders for combining, and a suitable decimating filter—while preserving Andersen’s same sequence of oversampling, high-rate delay, low-pass filtering/decimation, and combining. *See* Ex.1009, 6:18-40.

528. Although Dean’s example implementation is a radar phased array, a POSA would not have understood Dean’s n-bit oversampled-output teaching to be limited to radar; Dean’s teaching is similarly directed to the sampled-sensor beamforming architecture used in Andersen—oversampled digitization, high-rate digital delay/beamforming, and downstream decimation. In my opinion, a POSA would have considered that teaching applicable to Andersen’s hearing-aid beamformer because the same bit-depth/oversampling-rate tradeoff would predictably allow greater per-sample amplitude information and usable acoustic dynamic range without changing Andersen’s delay-before-decimation signal flow. *See* Ex.1008, 3:4-18, 3:30-38, 3:57-59; Ex.1009, 1:44-57, 6:18-40.

XXI. SECONDARY CONSIDERATIONS

529. I am not aware of any secondary-considerations evidence that would support a finding of non-obviousness for the '055 patent.

XXII. CONCLUSION

530. For all the reasons stated above, it is my opinion that the challenged claims of the '055 patent are unpatentable.

531. This declaration and my opinions are made to the best of my knowledge and understanding and are based on the material available to me at the time of signing this declaration. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Dated: August 6, 2026

By: /  /

Thomas W. Kenny, Ph.D.