A Low-Power Multi-Bit ΣΔ Modulator in 90-nm Digital CMOS Without DEM

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***Abstract*—Multi-bit sigma-delta modulators are widely used in analog-to-digital conversion especially in the modern deep-submicron CMOS process. As the quantizer resolution of ΣΔ modulators increases, the SNR performance improves. However, the feedback DAC has to maintain high linearity. The general practice to achieve that is to use dynamic element matching (DEM). The methodology proposed in this paper will greatly reduce the complexity or even avoid usage of DEM for multi-bit ΣΔ modulators. The proposed methodology— truncation error shaping and cancellation—reduces the feedback DAC levels for multi-bit quantizers. A prototype was designed in a standard CMOS 90-nm process to demonstrate the proposed methodologies. It achieved targeted performance without DEM at low power consumption with small silicon area.**

***Index Terms*—ADC, dynamic element matching, sigma-delta modulation.**

I. Introduction

THE sigma-delta (ΣΔ) technique is becoming more and more popular for low-power medium resolution telecom applications. The technique originated from delta modulation and differential pulse code modulation (PCM) in the 1950s [1] was used for many years for obtaining high-resolution, low-bandwidth analog-to-digital converters (ADCs). Now the increasing demand for low-power high-bandwidth data converters in system on chip (SoC) favors the use of ΣΔ modulators with limited oversampling ratio (OSR). For many communication applications, the required resolution is not very high [2]–[4]; so, for those cases, the technique does not target accuracy but exploits the benefits of using analog components with limited accuracy and low voltage. The reduced accuracy requirement in the analog section enables the integration of analog circuits with digital cores in a digital CMOS process.

The resolution of a ΣΔ modulator mainly depends on three factors: the oversampling ratio, the order of the modulator, and the number of bits of the quantizer. For a given input bandwidth, it is possible to enhance the resolution by increasing the sampling frequency. However, the increased requirement of bandwidth and slew rate in the operational transconductance amplifier (OTA) augments the power consumption. The use of high-order modulators generally increases the number of OTAs to be used (and, consequently, the power). Moreover, high-order modulators have stability problems that are dealt with by feedback branches and other factors that limit the high-order benefits [5]. This suggests using low-power medium-resolution low-order architectures with low OSR and multi-bit quantization. The use of multi-bit quantizers increases the resolution as well, but the method requires using multi-bit digital-to-analog converters (DACs) in the modulator feedback loop. DAC nonlinearities progress through the modulator with the same transfer function as the signal. Thus, the reduction of nonlinear effects do not benefit from the noise shaping. In order to maintain high linearity to the order of the final precision, the general accepted practice is to utilize element trimming, which is an expensive approach, or dynamic element matching (DEM), which transfers the mismatch of individual elements into noise. DEM has been studied for many years [6]–[11]. It includes several algorithms, for example, a barrel shifter [8], individual level averaging (ILA) [9], [10] and data weighted average (DWA) [11].

One disadvantage of DEM is that if the feedback DAC has high resolution, then it is potentially difficult to achieve an effective DEM. A high-resolution feedback DAC requires a large number of elements. As shown in [6], a 3-bit DAC has 40 320 permutations of input–output connections out of eight elements. With a three-stage butterfly structure, it is reduced to 4096 connections. Too many elements to average can lead to tones in the signal band for low input signals. A second disadvantage of DEM is that the mismatch can be transformed into noise and it is only partially shaped. Also, the in-band residual can possibly affect the SNR of the ΣΔ modulator.

Different methods have been proposed in previous published work [12]–[14] to reduce the sensitivity to DAC nonlinearity. They utilized coarse resolution quantizers and digital cancellation circuitry. Since these methods suffer from inaccurate matching of the analog and digital paths, the quantizer resolution reduction is limited. A recently proposed dual-quantization method [15] employs multiple DACs. Yet one of the multiple DAC resolution might be equivalent to or higher than the ADC. Another point is that minimum unit capacitor size in the switching DAC is limited by the process matching capability and the silicon area increases greatly as the DAC resolution increases. To drive the large load, the OTA power consumption is usually increased correspondingly.

This paper presents a technique that permits a reduction in the number of levels in the DAC with respect to the ones used in the ADC. The resolution of the modulator depends on the number of bits of the ADC, while the limit due to the mismatch depends on the number of levels of the DAC. As a result, the complexity of the DEM is kept low or it may even be eliminated, as we will show in the design demonstrating this method.

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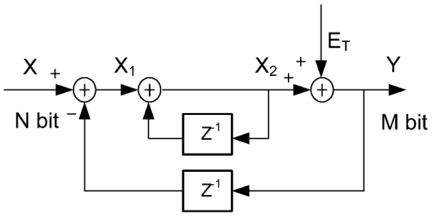

Fig. 1. First order digital ΣΔ modulator.

Section II describes the proposed methodology—truncation error shaping and cancellation. Section III illustrates the implementation of the method for a second-order modulator. The behavior study of the limitations from various nonlinearities allows optimization of the available noise budget. The test circuit implemented in a 90-nm CMOS technology uses a 16-level ADC. This method enables a reduction of the number of DAC levels in the first and second stages to three and five levels, respectively. Section IV provides details on the design and experimental results.

II. Proposed Methodology

The technique for the reduction the DAC levels uses two methods: truncation error shaping and residual cancellation. Both methods require some signal processing, leading to a negligible increase in power consumption. They are combined to achieve a simplified DEM or possibly eliminate it.

A. Truncation Error Shaping

The truncation error shaping method results from the use of a digital ΣΔ modulator (without delay between input and output) before the DAC. Consider the scheme of Fig. 1. It is a digital first-order structure with the delay moved after the output. The word-length at the input X and intermediate stages X_1 and X_2 is N bits while at the output is M bits $(N > M)$. The truncation of the word-length from X_2 to Y corresponds to the injection of the truncation error E_T. Under the same assumption made for the quantization error, we can model the truncation error by additive white noise. The power of the truncation error is spread uniformly over the Nyquist interval. Its value normalized to the full-scale amplitude is $1/(12 \cdot 2^{2M})$. It is easy to verify that the signal at the output of the circuit in Fig. 1 is

$$Y = X + (1 - z^{-1})E_T. \tag{1}$$

The digital processing of a second-order modulation obtains the truncation noise E_T

$$Y = X + (1 - z^{-1})^2 E_T. \tag{2}$$

Observe that the results in (1) and (2) do not have, as required, any delay between input and output. They may also be implemented as in [15]. Higher order modulators shape quantization more aggressively. A high-order shaper with no delay between input and output can have stability problems, and the number of truncation bits cannot be arbitrarily large or it is impossible to have truncation at all. Thus, the designer must study the stability of high-order digital $\Sigma\Delta s$ before their insertion in front of DACs. The effect of the digital ΣΔ is that the output is augmented by the shaped extra additive noise: the truncation noise due to the word-length reduction.

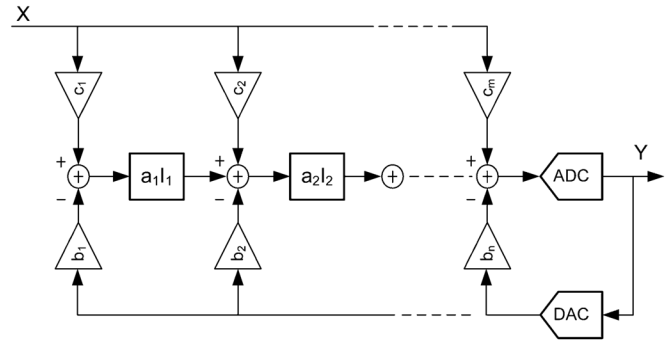

Fig. 2. Generic ΣΔ modulator with multiple feedback.

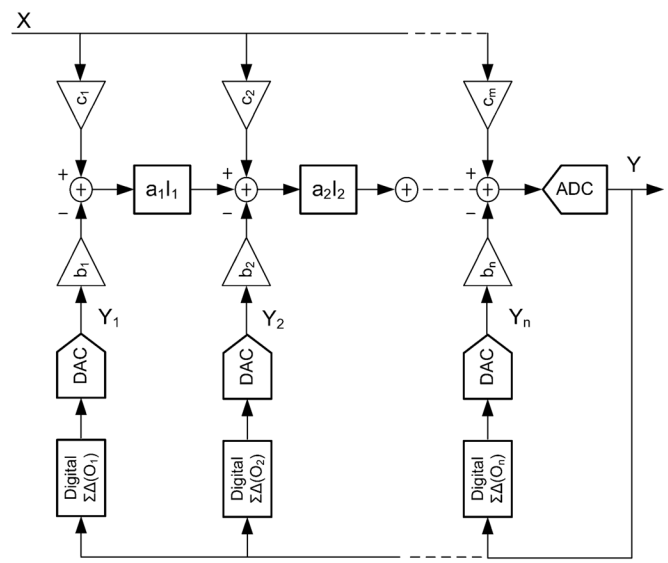

Fig. 3. Generic ΣΔ modulator transformation.

Consider the generic ΣΔ modulator with multiple feedback paths shown in Fig. 2. The N-bit digital output Y is transformed into analog by n DACs and multiplied by a proper coefficient at each integrator input. Used in the figure are separate DACs that assume a switched-capacitor implementation of each DAC with ratioed elements for obtaining the coefficients. Note that the analog signals at the output of each DAC are equal and, therefore, fully correlated.

Fig. 3 shows the proposed transformation. A digital ΣΔ before each DAC reduces the number of bits by a suitable truncation of the word-length and adds shaped truncation noise. The order L_i of the digital ΣΔs and the number of truncated bits can be different. We assumed that the truncation noises E_{Ti} due to different numbers of truncation bits of the ith digital ΣΔ are uncorrelated to each other and that the truncation noises are uncorrelated with the quantization noise E_Q. Moreover, if the truncation is by r bit, the power of E_{Ti} is 2^{2r} times the power of E_Q;

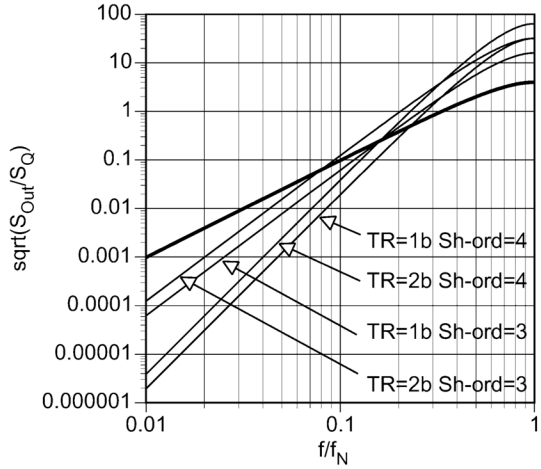

Fig. 4. Shaped spectra of various noise sources.

Let us assume that $H_i(z)$ is the z transfer function between the input of the ith E_{Ti} and the output Y. The Y is

$$Y = S(z)X + N_Q(z)E_Q + \sum_{i=1}^{n} H_i(z)E_{Ti} \tag{3}$$

where $S(z)$ and $N_Q(z)$ are the signal transfer function and quantization noise transfer function. Define $E_{Ti,\mathrm{OUT}}$ as the product of $H_i(z)$ and E_{Ti}

$$E_{Ti,\mathrm{OUT}} = H_i(z)E_{Ti}. \tag{4}$$

It was mentioned above that the truncation by r bit makes the magnitude of E_{Ti} 2^r times the magnitude of E_Q. However, the shaping can be beneficial to SNR. The power spectrum of the output signal $E_{Ti,\mathrm{OUT}}$ is

$$S_{E_{Ti,\mathrm{OUT}}} = 2^{2r}|H_i(f)|^2 S_{E_Q}. \tag{5}$$

When $H_i(z) = (1-z^{-1})^{L_i}$, a standard order L_i modulation, then

$$S_{E_{Ti,\mathrm{OUT}}} = 2^{2r}|1-e^{-j2\pi f T_s}|^{2L_i} S_{E_Q}. \tag{6}$$

If the number of truncated bits and the order of the digital $\Sigma\Delta$ modulator is the same on different paths, they can share the signal processing block. If the integrated noise due to truncation is negligible with respect to the E_Q contribution, then the SNR is not affected by the truncation operation. As shown by (6), the truncation errors are shaped by a given high-pass order. It is higher than the order of the $\Sigma\Delta$ and, despite the larger noise power by 2^{2r}, it is possible to have a negligible truncation contribution with signal bandwidth suitably small (or OSR suitably high).

Fig. 4 shows the spectra of various noise terms for a second-order $\Sigma\Delta$ modulator. The thick line shows the shaped spectrum caused by the 4-bit quantization noise E_Q. The other lines are the shaped spectra for 1-bit and 2-bit reduction, i.e., 3-bit and 2-bit quantization noise, respectively, and truncation noise shaping equals to third order $(1–z^{-1})^3$ and fourth order $(1–z^{-1})^4$. Observe that for 1-bit truncation and fourth order, the spectrum of the truncation noise is below the shaped quantization

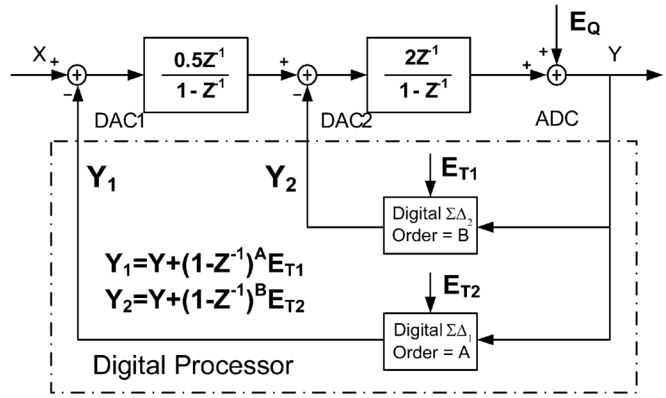

Fig. 5. Truncation error shaping in a second-order $\Sigma\Delta$ modulator.

until $f = 0.23f_N$. By contrast, the spectrum of 1-bit truncation and third order goes under the shaped quantization spectrum at $f = 0.08f_N$. Therefore, an oversampling ratio larger than 4 makes the former situation profitable. For the latter it is required to have more than 12.5 OSR.

Low-power medium-resolution applications should limit the OTAs numbers and must use low oversampling ratios for obtaining low power consumption in active elements. The use of a medium-resolution low-speed flash converter can profitably enhance the SNR. The truncation error shaping determines the reduction of the number of bits in the DAC. However, as the results of Fig. 4 indicate, the number of truncated bits cannot be arbitrarily high: above a given truncation level, the method becomes ineffective. Therefore, it might be necessary to use DEM for reduced levels when the unit elements number is still high after utilization of the truncation shaping method.

Another element to examine is the voltage swing at the output of the OTAs used in the modulator. The use of a large number of bits in the quantizer reduces the quantization error processed within the modulator. As a result, the swing at the output of the OTAs almost equals the one in the equivalent filter (with zero E_Q). The truncation error shaping introduces significant high-frequency noise in the system, thus increasing the required OTA's dynamic range. The problem can be tackled by properly scaling the sampled-data integrators. However, the remedy requires using augmented feedback capacitors and worsens the feedback factor.

B. Truncation Error Cancellation

Since truncation is the result of a logic operation, the digital value of the truncation error is known. It is therefore possible to estimate the effect of the truncation when passed through a given transfer function. Fig. 5 shows the use of the truncation shaping method applied to a second-order modulator. The shaped version of E_{T1} passed through the first integrator $0.5z^{-1}/(1-z^{-1})$ becomes

$$E_{T1,\mathrm{OUT1}} = 0.5z^{-1}(1-z^{-1})^{A-1}E_{T1} \tag{7}$$

while the shaped version of E_{T2} passed through $2z^{-1}/(1-z^{-1})$ becomes

$$E_{T2,\mathrm{OUT2}} = 2z^{-1}(1-z^{-1})^{B-1}E_{T2}. \tag{8}$$

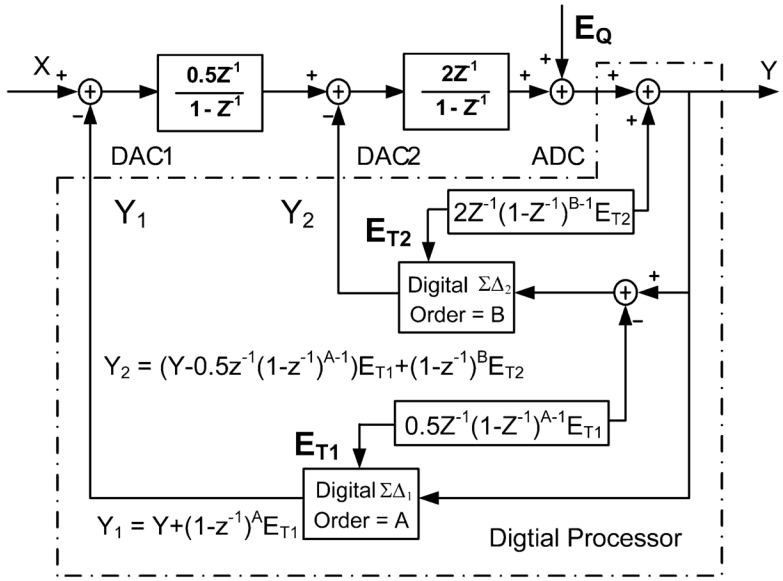

Fig. 6. Example of truncation error cancellation in ΣΔ modulator.

The digital estimation of terms expressed by (7) and (8) enable a cancellation of the effects at the output of the first and second integrators. The cancellation requires using two additional branches, shown in Fig. 6. The first handles $0.5z^{-1}(1-z^{-1})^{A-1}E_{T1}$ combined with the feedback to the second input and passed through the second digital ΣΔ. The result is subtracted at the input of the second integrator, thus passing through a digital-to-analog conversion. $2z^{-1}(1-z^{-1})^{B-1}E_{T2}$ is added directly in the digital domain and produces the digital output. It is easy to verify that the two added branches completely cancel the truncation error if the analog integrators perfectly match the digital processing.

The cancellation of the truncation error is such that the effect of E_{T1} does not extend beyond the first integrator while the truncation error E_{T2} affects the second integrator only. Analysis of the scheme of Fig. 6 leads to

$$Y_1 = Y + (1-z^{-1})^A E_{T1} \tag{9}$$
$$Y_2 = (Y - 0.5z^{-1}(1-z^{-1})^{A-1}E_{T1}) + (1-z^{-1})^B E_{T2}. \tag{10}$$

By linear model analysis, the system transfer function deducted is

$$Y = z^{-2}X + (1-z^{-1})^2 E_Q. \tag{11}$$

A possible mismatch, δ_1 and δ_2, between the analog and digital transfer functions may produce some residual, but that effect is likely negligible thanks to noise shaping. The system transfer function is

$$Y = z^{-2}X + (1-z^{-1})^2 E_Q - \delta_1 z^{-2}(1-z^{-1})^A E_{T1} - 2\delta_2 z^{-1}(1-z^{-1})^{B+1}E_{T2}. \tag{12}$$

Observe that the principle of cancellation is similar to the calculation of the cancellation term in *MASH* architectures [16]. Fig. 7 summarizes the method. If the analog domain transfer function is $I_j(z)$ and the digital modulator transfer function of E_j is $B_j(z)$, then the cancellation term $C_j(z)$ is

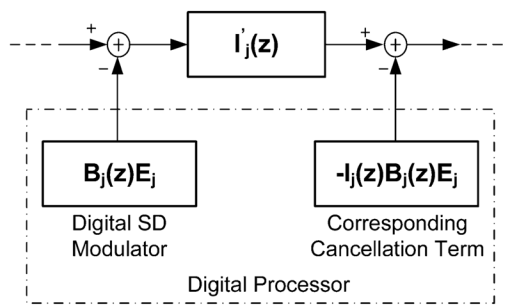

Fig. 7. Generic truncation error cancellation scheme.

$$C_j(z) = -I_j(z)B_j(z). \tag{13}$$

Assume the digital domain implementation of $I_j(z)$ is not a perfect match of the analog integrator $I'_j(z)$ due to the limited DC gain, bandwidth, slew rate, etc., then generally the truncation error residue is

$$I'_j(z)B_j(z)E_j - I_j(z)B_j(z)E_j = \Delta I_j(z)B_j(z)E_j. \tag{14}$$

As $B_j(z)$ is the noise shaping transfer function, with a standard format of $(1-z^{-1})^N$, its in-band magnitude is minimal. Hence, the mismatch of the digital and analog transfer function is usually further suppressed by $|(1-e^{-j\omega})^N|$.

The number of truncation bits can be different along the ΣΔ architecture. They should be verified with the following design criteria:

- The DEM is at a minimal complexity or even avoided.
- The high-frequency noise injection does not seriously penalize the OTA output swing.

III. A Second-Order ΣΔ Modulator Example

The methodology introduced in the previous section is verified by the design of a 4-bit second-order ΣΔ modulator [19].

TABLE I
NOISE DUE TO NON-IDEAL EFFECTS

Specifications	SNDR(dB)	ENOB(bits)
Ideal Case	57.2	9.2
Thermal Noise from Sampling Capacitance (0.1 pF)	54.5	8.75
Aperture jitter ($130ps$)	55.4	8.9
Capacitor Mismatch	57.0	9.1
Opamp input referred noise ($V_{n,rms} = 10uV$)	56.9	9.1
Opamp Finite DC gain ($A_{DC} = 70$ dB)	57.1	9.1
Opamp GBW = 90 MHz, SR = 90 V/μs	56.8	9.0
Modulator Simulated including all non-linearities	51.9	8.33
Prototype Measurement	51.2	8.2

The use of truncation, shaping, and error cancellation enables a three-level DAC in the main feedback loop and a five-level DAC in the second integrator feedback loop. The swing at the output of the OTAs is well controlled and suitable for a low-voltage supply. A second-order loop is a good choice for reducing the digital filter complexity and for low power. A third-order counterpart would require an additional OTA which is a significant source of power consumption [3]. For low OSR, the 4-bit flash is not particularly power hungry, since the comparator current usually is in the order of tens of μA, while OTA is hundreds of μA. The modulator diagram is shown in Fig. 6 by setting $A = 2$ and $B = 1$.

This design uses $f_{\rm CLK} = 40$ MHz. The circuit targets at 50 dB SNDR with $\rm OSR = 10$ and 70 dB SNDR with $\rm OSR = 50$. Accordingly, the architecture meets the requirements of many applications including wireless baseband systems such as WCDMA, GSM, and Bluetooth [2], [4].

The main goal of this design is to obtain low-power consumption. The result is obtained by proper management of the power budget. In generel, a real $\Sigma\Delta$ modulator achieves an SNDR lower than the theoretical quantization noise calculation because of extra noise terms due to various sources and inaccuracies in the circuits performance. This design assigns approximately 50% extra the noise budget (the one due to the shaped quantization noise—with $\rm OSR = 10$) to limitations that help in reducing the power. For instance, the use of small sampling capacitances leads to small loads to the OTAs. The power consumption is reduced but a larger kT/C noise results. Limiting the bandwidth and slew rate of the OTAs also reduces the power but the non-idealities lead to a less effective noise shaping. The result obtained for SNDR will be 6 dB less than the theoretical value, as shown in Table I.

A. Noise Sources and Non-Idealities

A discrete-time implementation of integrators uses switched-capacitor and operational amplifiers. The noise sources and circuit non-idealities that limit the SNR are:

- thermal noise;
- operational amplifier finite DC gain;
- operational amplifier finite gain bandwidth;
- operational amplifier limited slew rate;
- clock aperture jitter.

The reference voltage used is 0.8 V for the fully differential operation. The goal is to obtain a dynamic range of 56 dB (50 dB SNDR @ -6 dBFS) with $\rm OSR = 10$. The power of the signal is 80 mV^2 and the noise power budget is 0.3 μV^2 (550 $\mu\rm V_{rms}$). For a 4-bit ADC the power of the quantization error is $\Delta^2/12 = 833\ \mu\rm V^2$. The quantization noise should be the main noise source. Its contribution is estimated by

$$n_0 = e_{\rm rms}\frac{\pi^L}{\sqrt{2L+1}}\left(\frac{1}{\rm OSR}\right)^{L+0.5} = 2.88\times10^{-2}\times\frac{3.14^2}{\sqrt{5}}(0.1)^{2.5} \longrightarrow 402\ \mu\rm V \quad (15)$$

where $L = 2$.

Thermal noise is an important source of noise. It is mainly due to the kT/C limit set by the the sampling capacitor C_1. The noise power for each sampling phase and each sampling capacitance is kT/C_1. The input-referred noise of the OTA also increases noise power. Its effect is determined by noise simulations at the transistor level and expressed as kT/C_1 multiplied by a given factor. In our design, we roughly assume a factor 8 for the global effect of sampling-capacitor and OTA noise. The total noise is spread over the Nyquist interval and is then attenuated by the OSR. In addition to the kT/C considerations, the capacitor size is important for several reasons, such as switching speed, power consumption of the driving amplifier, etc. In our design, C_1 is set to be 100 fF, leading to a noise power kT/C_1 equal to 4.1 nV^2. The $1/f$ noise of the OTA also possibly affects the SNR. In our design, the limit is assumed negligible.

The clock jitter causes an error in the sampling of the input. Its effect is equivalent to a white noise with the power in the signal band of $(A\omega_{\rm in}\delta_{\rm jitter})^2/\rm OSR$ (A and $\omega_{\rm in}$ are the amplitude and frequency of the input signal, respectively).

The finite gain bandwidth and limited slew rate do not give simple noise equations. The limit to SNDR is estimated by simulations.

B. SIMULINK Model

Calculation of the effects of all the non-idealities listed above was done by behavioral simulations. The results give the designer indications of the specifications requirements for the basic blocks. The model of the modulator is shown in Fig. 8 for a time-domain analysis with SIMULINK. The details of the behavioral descriptions can be found in [18]. Table I summarizes the noise effect of a single non-ideality in terms of SNDR and effective number of bits (ENOB). The available noise budget is traded off among a small sampling capacitance and low bandwidth and slew rate of the first OTA. The limitations of the second OTA are negligible even if the current consumption has been scaled by a factor 2. Observe that since the OSR is

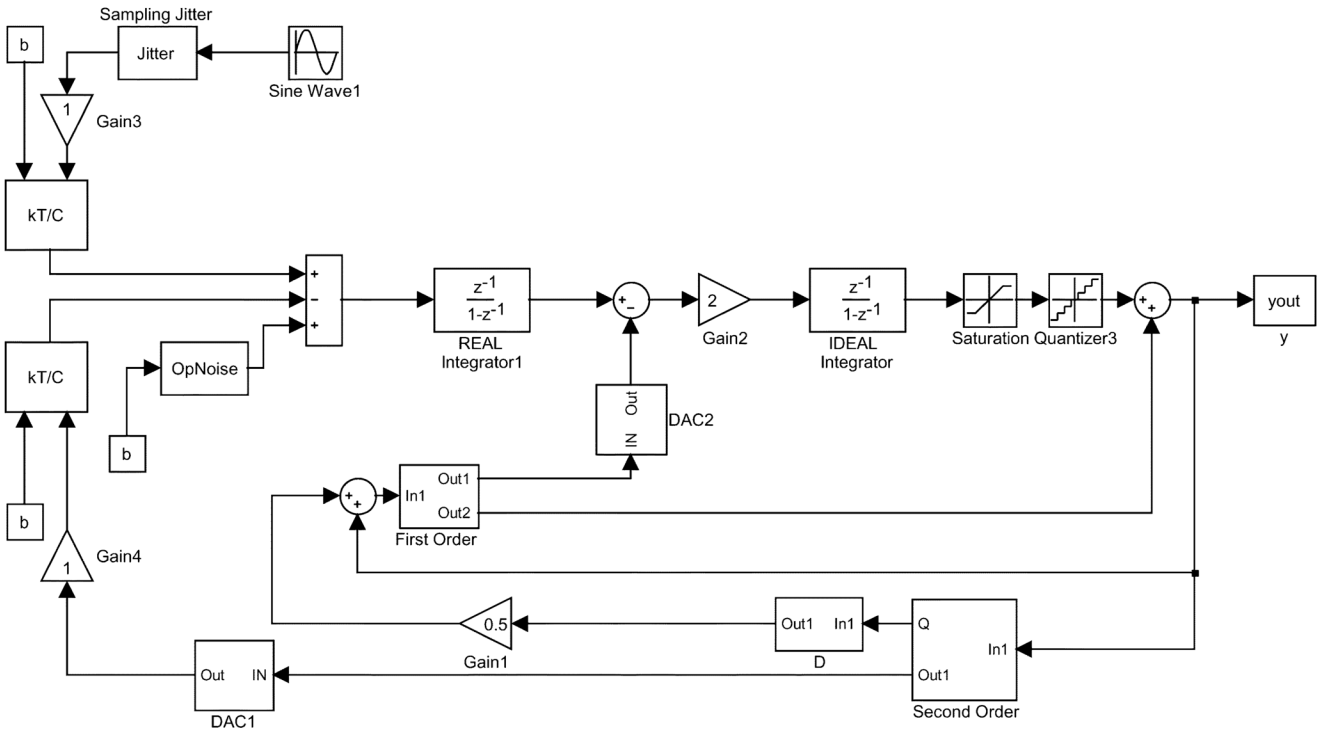

Fig. 8. SIMULINK model including non-idealities.

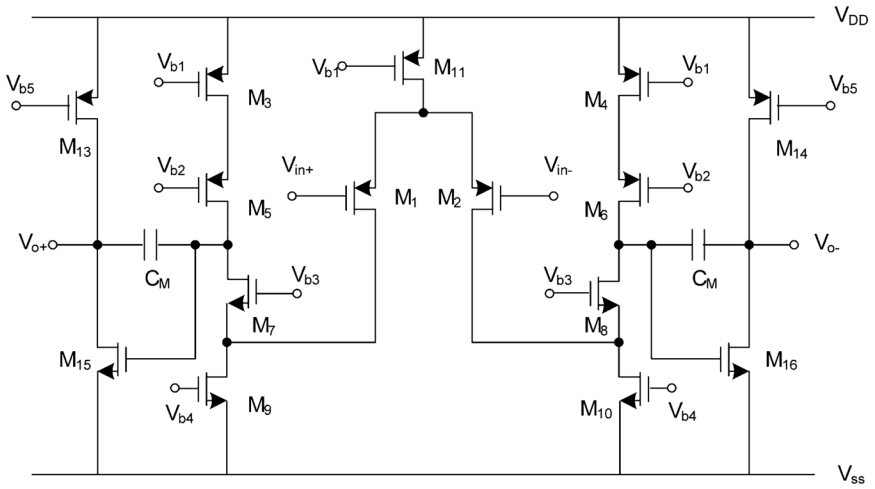

Fig. 9. Two-stage amplifier.

relatively low, the expected high clock jitter in the sampling creates high equivalent noise.

Observe that the standard deviation of the mismatch among capacitances is given by $\sigma_c = A_c/\sqrt{C_u/C_{\rm ox}}$ where A_c is 0.012 for the technology used, C_u is the unity capacitance, and $C_{\rm ox}$ is the specific capacitance. For a 4-bit switched-capacitor DAC, the C_u should become as small as 6 fF. This value, on the one hand, is not practical, and, on the other hand, would lead to $\sigma_c = 0.0035$, which is too large and would require using DEM even for 60 dB SFDR. The unity capacitance should increase by a factor 12.25 to obtain $\sigma_c = 0.001$. If the 16–level switched-capacitor DACs were implemented differentially, the number of capacitors in two integrators would be increased from 10 to 60 plus range; also, the corresponding routing complexity would increase and the required DEM circuitry would be larger.

IV. Circuit Implementation

The modulator is designed in 90-nm digital CMOS process. It requires use of only two operational amplifiers (opamps), 15 comparators, and some digital logic. The reference voltage of the $V_{\rm ref}$ is 800 $\rm mV_{peak}$.

A. Amplifier

System-level simulations show that with single-sampling, an opamp gain larger than 60 dB and unity-gain bandwidth larger than 80 MHz are required. The OTA used for the integrators is a two-stage amplifier; the small output resistance of the sub-micron transistors requires using a folded cascode in the first stage. Miller compensation yields a bandwidth of 100 MHz with an open-loop gain of 70 dB. The total current drawn is about

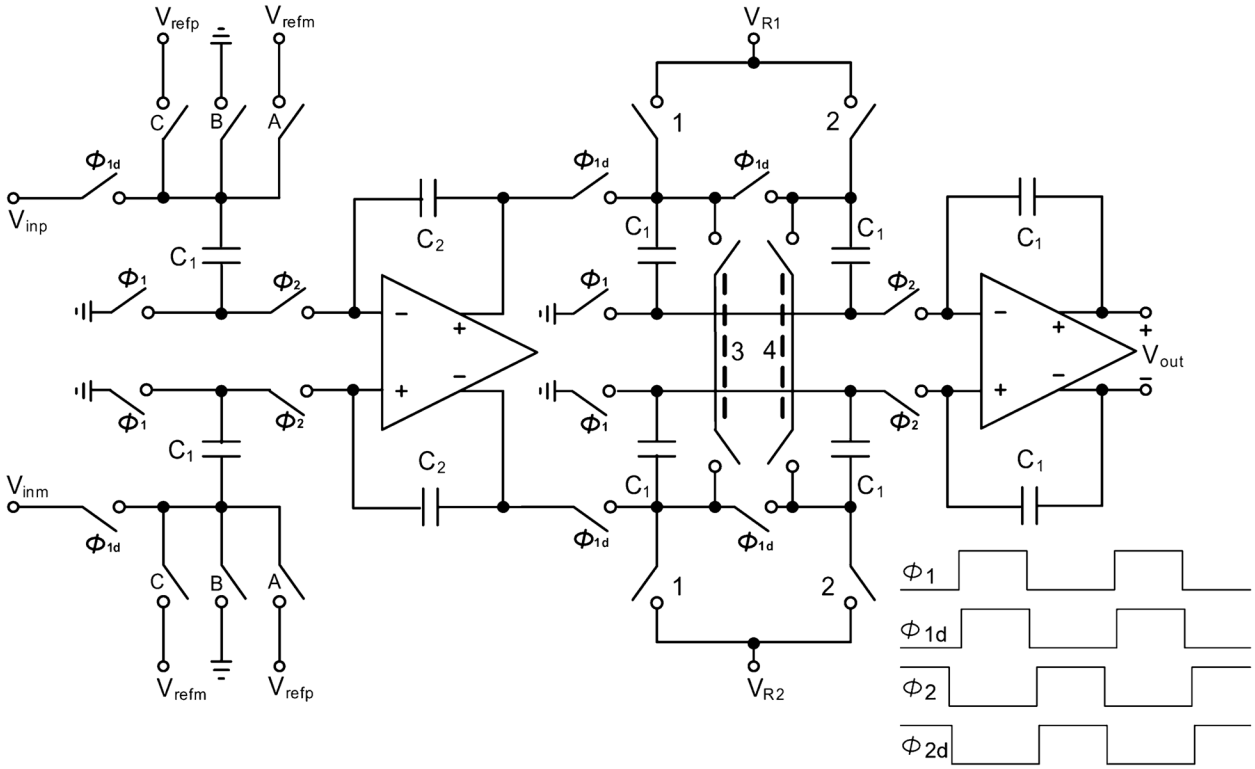

Fig. 10. First and second integrators.

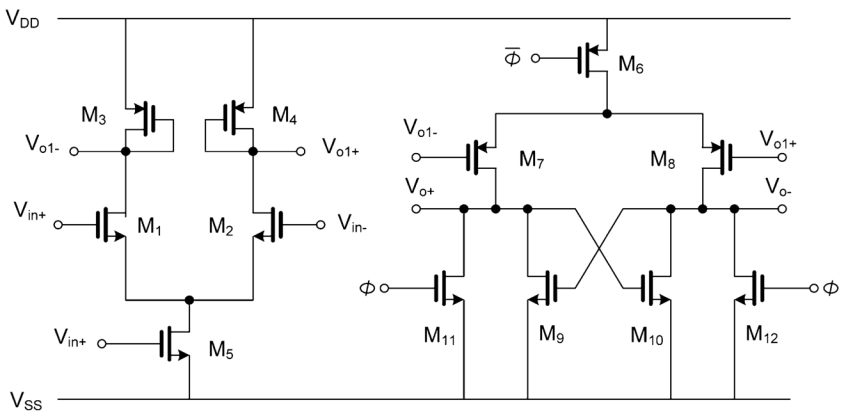

Fig. 11. Two-stage comparator schematic.

0.65 mA for the first-stage integrator and 0.4 mA for the second stage. The amplifier diagram is shown in Fig. 9.

B. Integrator

Fig. 11 shows the modulator scheme with two switched-capacitor integrators. It uses two non-overlap clock phases: ϕ_1 is the sampling phase and ϕ_2 is the integration phase. The difference of the input signal charge and the DAC level are injected into C_2 during ϕ_2. Delayed versions of ϕ_{1d} and ϕ_{2d} minimize the input signal-dependent charge injection. The sampling capacitor C_1 is 100 fF and C_2 is 200 fF. The techniques of minimizing charge injection can be found in [17]. The two DACs use three levels (-1, 0, $+1$) and five levels (-1, -0.5, 0, 0.5, 1), respectively. They are realized through capacitors and switches as shown in Fig. 10. As the quantizer resolution is 0.1 V differential per step, the three-level DAC is 0.8 V differential per step, and for the five-level DAC, it is 0.4 V differential per step.

C. Comparator and Digital $\Sigma\Delta$ Modulator

The 4-bit flash ADC uses 15 comparators made with differential pre-amplifiers and latches as shown in Fig. 11. The current consumption of the 15 comparators is 0.3 mA. A poly resistor string made by 32 equal 250-Ω resistors divides an external reference to produce the reference voltages. The digital $\Sigma\Delta$ modulator processing functions were coded in VHDL, simulated with Modelsim and synthesized in Synopsys. The dynamic current consumption of the digital processor is 0.1 mA.

D. Silicon Test Result

Fig. 12 shows the chip microphotograph. The total area of the modulator including the digital circuits is 0.4 mm^2 and draws

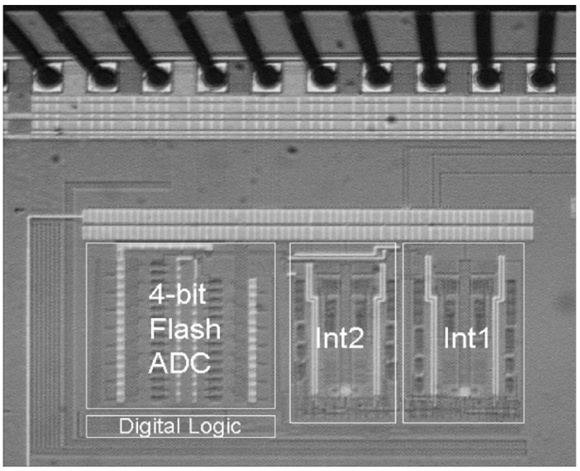

Fig. 12. Prototype die photo.

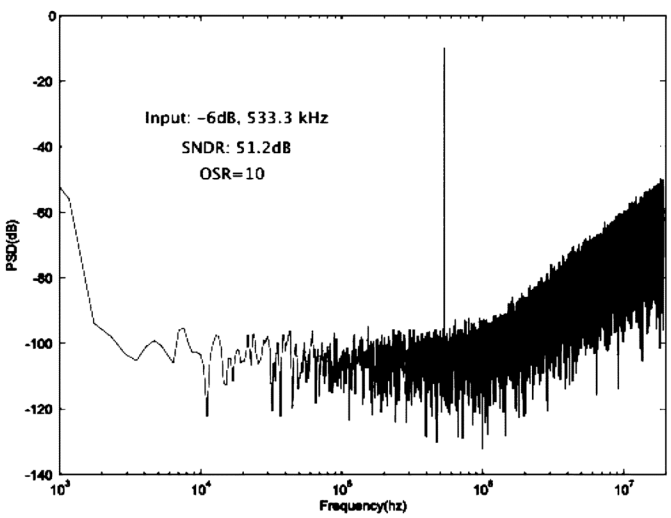

Fig. 13. 65536 points FFT result.

1.6 mA at 1.3 V including dynamic contributions. The supply voltage does not exceed the range supported by the process. A TQFP 64-pin package is used. The measured performance agrees well with the behavioral model simulations. A printed circuit board (PCB) was designed and fabricated to test the prototype. Voltage and current references were generated on the test board. A logic analyzer acquires the multi-bit digital output for off-chip processing using MATLAB.

Fig. 13 shows the 65 536-point fast Fourier transform (FFT) plot of the output data. The input sine wave was set at -6 dBFS at 533.3 kHz. The noise floor is around -100 dB, as expected, which is mainly due to kT/C noise. The gains and bandwidths of the OTAs do not degrade performance. The SNDR is 51 dB with OSR $= 10$. Similar measurements for OSR $= 20$ and OSR $= 50$ show SNDR equal to 61 and 72 dB, respectively. The total power consumption including the digital circuitry is 2.1 mW. Fig. 14 shows the SNDR versus amplitude plots for the three cases. The 0 dB crossings (dynamic range) are at -78 dB, -66 dB, and -58 dB, respectively. Table II summarizes the results.

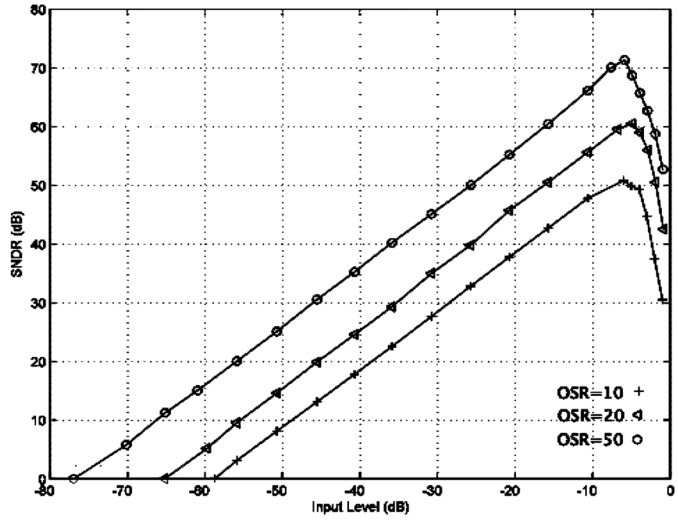

Fig. 14. SNDR curve in three different modes.

TABLE II
ΣΔ MODULATOR PERFORMANCE SUMMARY

Power Supply	1.3 V		
Power Consumption	2.1 mW		
Process Technology	90 nm digital CMOS process		
Silicon Area	$0.4mm^2$		
OSR	10	20	50
Sampling Frequency(MHz)	40	40	20
Signal Bandwidth(MHz)	2	1	0.2
$SNDR_{peak}$	51 dB	61 dB	72 dB
Dynamic Range	58 dB	66 dB	78 dB

V. CONCLUSION

The truncation error shaping and cancellation methodologies proposed in this paper greatly reduce the DEM complexity or even avoid to use it. A 4-bit second-order ΣΔ modulator was designed without DEM to demonstrate it. The silicon test results proved the validity of the methodology.

On the one hand, since the coarse-resolution DAC signal is relatively larger magnitude than the fine-resolution quantizer signal, and the integrator input sees that signal, the dynamic range of the integrator output is increased compared with traditional multi-bit ΣΔ modulators. In the implementation of the second-order ΣΔ modulator, the output swing of both integrators increases about 15% compared with conventional modulators.

On the other hand, as DAC levels are reduced, the use of DEM circuitry was avoided. No visible tones were observed above the noise floor, and that noise floor was maintained throughout more than 70 dB of input range. The benefits are that silicon area has been saved, since a small number of capacitors are needed. The number of capacitors required by 16-level DACs is much greater. The routing complexity and power consumption were reduced as well. This was realized with a less than 0.01 mm^2 digital ΣΔ modulator. Therefore, the proposed method appears to be a cost-effective solution for multi-bit ΣΔ modulators.

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REFERENCES

[1] W. Kester, *Analog-Digital Conversion*. Wilmington, MA: Analog Devices, 2004.

[2] G. Gomez and B. Haroun, "A 1.5 V 2.4/2.9 mW 79/50 dB DR $\Sigma\Delta$ modulator for GSM/WCDMA in a 0.13 μm digital process," in *IEEE Int. Solid-State Conf. Dig. Tech. Papers*, vol. 1, 2002, pp. 306–468.

[3] A. Dezzani and E. Andre, "A 1.2-V dual-mode WCDMA/GPRS $\Sigma\Delta$ modulator," in *IEEE Int. Solid-State Conf. Dig. Tech. Papers*, 2003, pp. 58–59.

[4] K. Muhammad *et al.*, "A discrete-time Bluetooth receiver in a 0.13 μm digital CMOS process," in *IEEE Int. Solid-State Conf. Dig. Tech. Papers*, vol. 1, Feb. 2004, pp. 268–527.

[5] A. Marques, V. Peluso, M. Steyaert, and W. Sansen, "Optimal parameters for cascade $\Sigma\Delta$ modulators," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 1, Jun. 1997, pp. 61–64.

[6] L. R. Carley and J. Kenney, "A 16 bit 4th order noise-shaping D/A converter," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 1988, pp. 21.7.1–21.7.4.

[7] L. R. Carley, "A noise-shaping coder topology for 15+ bit converters," *IEEE J. Solid-State Circuits*, vol. 24, no. 4, pp. 267–273, Apr. 1989.

[8] Y. Sakina, "Multi-bit $\Sigma\Delta$ A/D converters with nonlinearlity correction using dynamic barrel shifting," M.A. thesis, ERL, Univ. California, Berkeley, 1993.

[9] B. H. Leung and S. Sutarja, "Multi-bit $\Sigma\Delta$ A/D converters incorporating a novel class of dynamic element matching technique," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 39, no. 1, pp. 35–51, Jan. 1992.

[10] F. Chen and B. H. Leung, "A high resolution multibit sigma-delta modulator with individual level averaging," *IEEE J. Solid-State Circuits*, vol. 30, no. 4, pp. 453–460, Apr. 1995.

[11] R. T. Baird and T. S. Fiez, "Improved $\Sigma\Delta$ DAC lineraity using data weighted averaging," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 1, May 1995, pp. 13–16.

[12] T. C. Leslie and B. Singh, "An improved sigma-delta modulator architecture," in *IEEE Int. Symp. Circuits and Systems*, vol. 1, May 1990, pp. 372–375.

[13] ——, "Sigma-delta modulators with multibit quantising elements and single-bit feedback," *IEE Proc. G Circuits, Devices and Systems*, vol. 139, no. 3, pp. 356–362, Jun. 1992.

[14] A. Hairapetian, G. C. Temes, and Z. X. Zhang, "Multibit sigma-delta modulator with reduced sensitivity to DAC nonlinearity," *Electron. Lett.*, vol. 27, no. 11, pp. 808–817, 1997.

[15] F. Colodro, A. Torralba, and L. J. Mora, "Digital noise shaping of residues in dual-quantization Sigma-Delta modulators," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 51, no. 2, pp. 225–232, Feb. 2003.

[16] S. Norsworthy, R. Schreier, and G. Temes, *Delta-Sigma Data Converters Theory, Design and Simulation*. New York: IEEE Press, 1996.

[17] F. Maloberti, *Analog Design for CMOS VLSI Systems*. Boston, MA: Kluwer Academic, 2001.

[18] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, "Behavioral modeling of switched-capacitor sigma-delta modulators," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 50, no. 3, pp. 352–364, Mar. 2003.

[19] J. Yu and F. Maloberti, "A low power multi-bit $\Sigma\Delta$ modulator in 90 nm digital CMOS without DEM," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers* , Feb. 2005, pp. 168–169.

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