



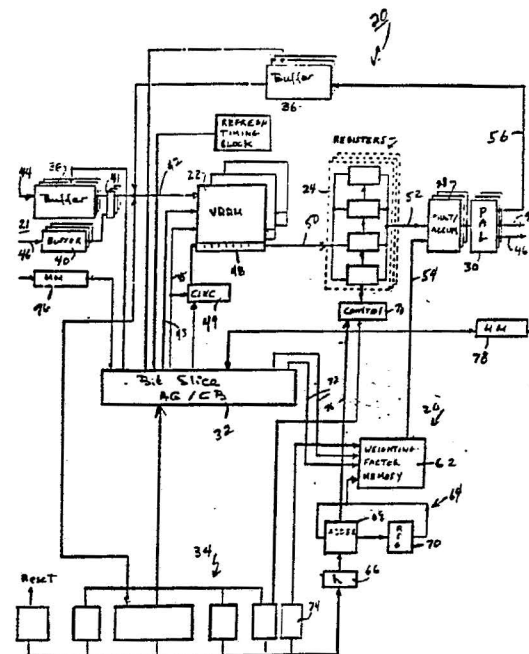
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁴ : G06K 9/36	A1	(11) International Publication Number: WO 90/00780 (43) International Publication Date: 25 January 1990 (25.01.90)
(21) International Application Number: PCT/US89/03061 (22) International Filing Date: 12 July 1989 (12.07.89) (30) Priority data: 218,824 13 July 1988 (13.07.88) US (71) Applicant: ANALOGIC CORPORATION [US/US]; 8 Centennial Drive, Peabody, MA 01961 (US). (72) Inventor: DOLAZZA, Enrico ; 167 Marlborough Street, Boston, MA 02116 (US). (74) Agent: GOMES, David, W.; Analogic Corporation, 8 Centennial Drive, Peabody, MA 01961 (US). (81) Designated States: BE (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, NL (European patent).		Published <i>With international search report.</i>

(54) Title: APPARATUS FOR SIMULTANEOUSLY FILTERING AND RESAMPLING DIGITAL DATA

(57) Abstract

The present invention provides an apparatus for processing a set of digital data, comprising computational circuitry (26, 28) for implementing a modified cubic convolution interpolation for simultaneously resampling and filtering the set of digital data. In a preferred embodiment the set of data represents pixel data for a two dimensional image and the apparatus further includes a memory (22) for storing the pixel data, circuitry (24) for coupling the pixel data from the memory (22) to the computational circuitry, circuitry (30, 36) for outputting and for storing in the memory (22), filtered and resampled pixel data from the computational circuitry (26, 28) and a bit-slice processor (32) for programmably controlling the memory (22), the computational circuitry (26, 28) and the circuitry (30, 36) for outputting and for storing. Such an apparatus provides digital image processing in systems for producing hard copy of the electronic image data and, in particular, color hard copy.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	ES	Spain	MG	Madagascar
AU	Australia	FI	Finland	ML	Mali
BB	Barbados	FR	France	MR	Mauritania
BE	Belgium	GA	Gabon	MW	Malawi
BF	Burkina Faso	GB	United Kingdom	NL	Netherlands
BG	Bulgaria	HU	Hungary	NO	Norway
BJ	Benin	IT	Italy	RO	Romania
BR	Brazil	JP	Japan	SD	Sudan
CA	Canada	KP	Democratic People's Republic of Korea	SE	Sweden
CF	Central African Republic	KR	Republic of Korea	SN	Senegal
CG	Congo	LI	Liechtenstein	SU	Soviet Union
CH	Switzerland	LK	Sri Lanka	TD	Chad
CM	Cameroon	LU	Luxembourg	TG	Togo
DE	Germany, Federal Republic of	MC	Monaco	US	United States of America
DK	Denmark				

APPARATUS FOR SIMULTANEOUSLY FILTERING AND
RESAMPLING DIGITAL DATA

BACKGROUND OF THE INVENTION

Related Applications

5 The present application is directly related to U.S. Patent Application of Leopold Neumann, Enrico Dolazza and Alexander Kolchinsky filed of even date herewith and entitled IMAGE PROCESSOR.

Field of the Invention

10 The present invention generally relates to the processing of digital data representing a mathematically continuous signal and, in particular, to the interpolating, resampling and filtering of such digital data.

Statement of the Prior Art

15 The processing of digital data representing continuous signals is common when digital processing is applied to data directly derived from the analog world. Such data represents continuous signals which must be reduced to a limited number of digital data points for purposes of digital processing.

20 In spite of this limited form for the data, it is still desirous to be able to perform processing techniques on the digital data. Such techniques would include filtering and determining the signal value at other than the originally digitized points. This later process generally involves

25 digital interpolation and is part of a larger technique known as resampling. Resampling generally includes starting with a first set of digital data points $I(d)$, representing a signal and having a digitization interval d , and deriving a second set of digital data points $I(x)$, also representing the same

30 signal and having a digitization interval x . The digitization intervals x and d may be the same or different.

One specific area of application for these techniques is image processing where it is particularly desirous to change the size of an image without interfering with the frequency

35 quality of the analog signal representing the image.

Unfortunately, when digital processing is used to either magnify or demagnify an image represented by pixel values, distortion of the frequency quality of the image occurs. When an image is magnified, the original spatial frequency information of the image is shifted to lower frequencies 5 resulting in a blurring or "washing" of the image. When an image is slightly magnified by a non-integer factor or demagnified, the highest spatial frequencies are aliased. For this reason it is helpful to combine high and low pass 10 digital filtering with the processing steps of magnification and demagnification. Unfortunately, such combinations greatly increase the complexity and cost of such processing and further reduce the flexibility of such processing to vary the processing steps for purposes of handling differently 15 formatted images and purposes of experimentation.

The technique of resampling may include different types of interpolation such as nearest neighbor interpolation, bi-linear interpolation and interpolation using the cubic convolution method. The latter method, cubic convolution, is 20 generally credited with most accurately maintaining the data content after the desired processing is performed. This information retention is directly related to the amount of computation required. One image processing application of cubic convolution interpolation is discussed in U.S. Patent 25 No. 4,578,812 to Yoshio Yui. Yui describes a computational circuit for implementing the cubic convolution function for resampling image data for purposes of both magnification, demagnification and axis reorientation. The cubic convolution method of image processing has been around for 30 some time, and it has been implemented both through the use of main frame computers and through the use of hard wired, high speed processors. The patent to Yui expresses the general interest found in various forms of image processing for speeding up the method by providing processing hardware 35 capable of running a high speed implementation of the convolution.

SUMMARY OF THE INVENTION

Accordingly, the present invention improves data processing techniques by allowing the combination of resampling and filtering in a flexible processing apparatus.

5 The present invention provides an apparatus for processing a set of digital data, comprising computational circuit means for implementing a modified cubic convolution interpolation for simultaneously resampling and filtering the set of digital data. In a preferred embodiment the set of data

10 represents pixel data for a two dimensional image and the apparatus further includes memory means for storing the pixel data, means for coupling the pixel data from the memory means to the computational means, means for outputting and for storing in the memory means, filtered and resampled pixel

15 data from the computational means and a bit-slice processor means for programmably controlling the memory means, the computational means and the means for outputting and for storing. A more specific embodiment includes means for generating weighting factors against which the input pixel

20 values are multiplied. The weighting factors may be programmably varied to achieve a selectable filtering effect. In another embodiment, the simultaneous filtering and resampling is performed by a multiplicity of substantially identical, serially coupled, programmable processing modules,

25 which arrangement provides a very high degree of flexibility in the performance of different types of processing steps and also in the order of their performance while still supporting high speed processing.

BRIEF DESCRIPTION OF THE DRAWINGS

30 The present invention is illustratively described below in reference to the embodiments shown in the accompanying drawings of which:

Fig. 1 is a block circuit diagram of one embodiment of the present invention;

35 Fig. 2 is a block circuit diagram of another embodiment of the present invention;

-4-

Fig. 3 is a plot of cubic convolution weighting factors for four adjacent pixels; and

Fig. 4 is a plot of the cubic convolution response of the embodiment of Fig. 1 for different filtering effects.

5 DETAILED DESCRIPTION OF THE DRAWINGS

Fig. 1 shows the components of a computational module 20 used for the actual computation of the cubic convolution function. The purpose of the computational module 20 is to perform repeated multiplication/accumulation operations with 10 properly corresponding data to calculate resampled pixel data. Generally included are an input buffer means 21, memory means 22, register means 24, weighting factor generator means 26, multiplier/accumulator 28, output PAL 30, bit-slice processor 32, registers 34 and a buffer 36. Input 15 buffer means 21 includes a pair of input buffers 38 and 40 which are alternatively used to input pixel data to the memory 22 over a 12 line data bus 44 and an 8 line data bus 46, respectively. Buffer 38 receives input bus 44 and is used when the data is received from a similar computational 20 module (not shown). Buffer 40 receives input bus 46 which is used if the module 20 is the first computational module in the system and therefore receives pixel data from the processing system. Which buffer 38 or 40 is used is determined by a switch 41. Through the use of buffers 38 and 25 40 the pixel data may be handled as 8 bit words within a processing system and as 12 bit words to maintain higher accuracy between identical computational modules.

The memory means 22 includes a video random access memory in which pixel data entering may be stored in any 30 location and which includes a serial output register 48 capable of receiving an entire memory row of pixels and serially outputting that row, one pixel at a time, over a 12 line output bus 50. Memory means 22 has the capacity to store 16 lines of pixels having 4,096 pixels per line and 12 35 bits per pixel for a total memory capacity of 65,536 pixels at 12 bits per pixel. In practice, memory 22 may be

comprised of three video RAMS each being four bits wide and having 256 rows by 256 columns of addresses.

Pixel data is transferred one pixel at a time from memory 22 to the registers 24 which include four 12 bit registers for holding the data for four pixels to be used by the multiplier/accumulator 28. The pixel data is coupled to the registers 24 and therefrom to the multiplier/accumulator 28 by 12 line data buses 50 and 52.

Multiplier/accumulator 28 may be implemented by any commonly available circuitry for multiplying the pixel data presented on data bus 52 with corresponding weighting factors simultaneously supplied by a data bus 54. In the preferred embodiment, multiplier/ accumulator 28 has the capacity to receive, multiply and accumulate the results of two twelve bit words.

The 24 bit output of multiplier/accumulator 28 is coupled to the PAL 30 which includes programmable array logic for rounding off the data to prevent inaccuracies due to overflow. The data may then be either outputted from module 20 or coupled to buffer 36 via data bus 56. The 12 bit data bus 44 is used for outputting when the data is coupled to subsequent computation modules similar to 20, and the 8 bit data bus 46 is used when the module 20 is the last in the system and pixel data is outputted for other handling by a data processing system.

Buffer 36 holds the data from multiplier/accumulator 28 to allow storage of it back into the memory 22 via data bus 42. In this manner, the same computational module 20 may be used to perform up to four passes of the filtering/interpolating process beginning with a single set of horizontal image lines of pixels. These passes may be of either horizontal or vertical interpolation which determines the addressing method of memory 22 for storage of the data. This addressing is described below.

The registers 24 and the multiplier/accumulator 28 are part of the computational portion of the circuit 20 which portion further includes a weighting factor generator 26.

The generator 26 produces individual weighting factors for each of the pixel values transferred to registers 24. This process is accomplished by addressing a weighting factor memory 62 by means of an accumulator 64. Coordination of
5 weighting factors with the proper pixel data in registers 24 is achieved through timing signals from the bit-slice processor 32. The accumulator 64 works by taking the new digitization interval as stored in a register 66 and repetitively adding it in an adder 68 to an accumulated sum
10 stored in a register 70. Register 70 receives the new sum from the adder 68 and presents that sum back at an input of the adder 68 for the next addition with the digitization interval from register 66. The contents of register 70 are also coupled via a 10 bit bus to the addressing means of the
15 weighting factor memory 62. The new digitization interval stored in register 66 is normalized as a percentage of the old interval of the pixel data being used. In other words, the value stored in register 66 represents the new interval divided by the old interval (x/d). In this form the range of
20 values for registers 66 and 70 and accumulator 68 is constant which facilitates consistent addressing of memory 62 regardless of the actual new and old digitization intervals.

Thusly addressed are a series of four weighting factors which correspond to the positional relationship between the
25 point being interpolated and the known pixels available in registers 24 for computation. The group of four weighting factors are individually addressed by the least significant bit address lines 72 coupled to bit-slice processor 32.

When the sum in accumulator 68 exceeds the 10 bit limit
30 for addressing memory 62, the overflow is transferred by a bus 76 to a control register 78. The amount of overflow depends upon the amount of programmed demagnification. In a four point convolution the maximum demagnification allowed without dropping known pixel data from the computation is
35 four (4) which is therefore the maximum overflow amount. Without demagnification, the maximum overflow is one (1). Thus the overflow amount equals the number of new pixels that

will be transferred from memory 22 to the registers 24 by control register 78 via clock 49. It is also used by the control register 78 to determine which will be the first register to have its pixel transferred to multiplier/
5 accumulator 28 in correlation with a weighting factor from data memory 26. Control register 78 also determines which registers 24 receive new data points.

The weighting factor generator 26 includes means for providing a variable filtering effect in the computational
10 process by having available multiple sets of weighting factors with each set corresponding to a separate selectable filtering effect. These weighting factors and their corresponding filtering effects may be loaded by a control processor 86 in Fig. 2 prior to the computation process and
15 then selected on the fly during processing. Which one of the sets of weighting factors is used from memory 62 is selected by a register 74 in the bank of registers 34, which register 74 is coupled to the most significant addressing bits of memory 62.

20 Bit-slice processor 32 controls the flow of data through the computational circuit 20. Communication for the purpose of data input and output with other portions of the processing circuit are also controlled by processor 32 via a pair of handshake modules 76 and 78.

25 Lastly, registers 34 store information for use during the processing performed by the circuit 20. This information includes selection of one of the weighting factor tables for each of the possible computing passes that may be performed by the circuit 20, an interpolation factor or resampling
30 interval for each computing pass, input line length to the memory 22 for each pass, the number of lines of pixels initially inputted, video RAM status such as address of the first line, address of the next empty line and the number of empty lines and lastly, the address of the data for the last
35 vertical interpolation pass which was performed. The significance of this information is described in greater detail below under THEORY AND OPERATION.

-8-

Fig. 2 shows a block diagram of a plurality of filter/interpolator modules 80-83 coupled in series. This coupling provides the pixel data output from modules 80-82 as the data input for the next sequential module. The data output from module 83 may be otherwise transferred for system use or outputting. The number of filter/interpolator modules serially coupled may be determined by any practical system requirements. The greater the number of modules there are, the fewer passes there are that must be performed by each module. This distributed processing can reduce both the delay time for processing and the overall processing time of an image. Multiple modules also provide great flexibility in the overall processing method. Different orders of processing for horizontal and vertical interpolation and filtering may be used to achieve different end results. Conversely, systems can be produced which use only one or two filter/interpolator modules at a system cost savings while still retaining the processing capabilities, if not the speed and power.

The modules 80-83 are interconnected using the twelve bit data bus 44 to maintain resolution through the calculating process. The input of module 80 and the output of module 83 show the 8 bit data bus 46 for systems interface. A programmer 86 is shown for providing control of the modules. Programmer 86 loads the registers 34 and weighting factor memory 26 of each of the modules 80-83 in response to processing selections by an operator. Any suitable programming may be used which is in accordance with the devices and methods described herein.

THEORY AND OPERATION

The analytical form of the cubic spline convolution function in which a sample of value P located at $x = 0$ is transformed, is given by the formula:

35

-9-

$$\begin{aligned}
 (1) \quad & \left\{ \begin{array}{l} \frac{1}{2} \left| \frac{x}{d} \right|^3 - \left| \frac{x}{d} \right|^2 + \frac{2}{3} \\ \frac{2}{6} \left| \frac{x}{d} \right|^3 + \left| \frac{x}{d} \right|^2 - 2 \left| \frac{x}{d} \right| + \frac{4}{3} \end{array} \right. \quad \text{for } -d \leq x \leq d \\
 & \left\{ \begin{array}{l} -\frac{1}{6} \left| \frac{x}{d} \right|^3 + \left| \frac{x}{d} \right|^2 - 2 \left| \frac{x}{d} \right| + \frac{4}{3} \\ \frac{1}{6} \left| \frac{x}{d} \right|^3 + \left| \frac{x}{d} \right|^2 - 2 \left| \frac{x}{d} \right| + \frac{4}{3} \end{array} \right. \quad \text{for } -2d \leq x \leq -d, \\
 5 \quad F(x) = & \left\{ \begin{array}{l} \frac{1}{6} \left| \frac{x}{d} \right|^3 + \left| \frac{x}{d} \right|^2 - 2 \left| \frac{x}{d} \right| + \frac{4}{3} \\ \frac{1}{6} \left| \frac{x}{d} \right|^3 + \left| \frac{x}{d} \right|^2 - 2 \left| \frac{x}{d} \right| + \frac{4}{3} \end{array} \right. \quad \text{for } d \leq x \leq 2d \\
 & \left\{ \begin{array}{l} 0 \\ 0 \end{array} \right. \quad \text{for } |x| \geq 2d
 \end{aligned}$$

Fig. 3 shows the cubic spline convolution functions of four known pixels P_J , P_{J+1} , P_{J+2} and P_{J+3} having the digitization interval d . The functions shown represent the weighting factor W or functional contribution of each pixel to the interpolation of a new pixel at x , anywhere in the interval d . The actual contribution of each pixel is equal to the weighting factor times the actual pixel value. The value of a new pixel interpolated at the point x within d would equal the sum of the actual contributions of the four adjacent pixels. This may be represented as follows:

$$I(x) = W_J \cdot P_J + W_{J+1} \cdot P_{J+1} + W_{J+2} \cdot P_{J+2} + W_{J+3} \cdot P_{J+3} \quad (2)$$

where $I(x)$ is the new point being interpolated, P are the known pixel values, W are the weighting factors, and J , $J+1$... refer to the four adjacent pixel points. It is the multiplication and addition represented by the above equation (2) that is performed by the circuit of Fig. 1. Further, as shown in Fig. 3, the cubic spline convolution function for each pixel, along with its first and second derivatives, are all equal to zero at distances from each respective pixel greater than $2d$.

When a new set of points is recalculated in accordance with the above function (1), it may be said to have a new resampling interval x and may be represented as follows:

$$I(x) = \sum_j P_j * F(x)$$

where P_j are the originally sampled pixels and $F(x)$ is the general convolution function for the resampling interval x as given in the equation (1) above.

In this representation, $F(x)$ has the form $F(x^3, x^2, x^1, x^0)$ and the coefficients are uniquely defined by the fact that

F(x) is the third order auto-convolution of a rectangle-sample. Among the constraints that determine this, is one that causes F(x) to tail off at both ends, together with its first and second derivative. By removing the constraint that the second derivative of F(x) gets to zero at its tails, a degree of freedom is acquired that can be expressed by a parameter B. A more general cubic convolution function G(x,B) can then be written as follows:

$$\begin{aligned}
 G(x,B) = & \begin{cases} \frac{3|x|^3}{2B|d|} - \frac{9+B|x|^2}{4B|d|} + \frac{B+1}{2B} & \text{for } -d \leq x \leq d \\ \frac{-1|x|^3}{2B|d|} + \frac{9+B|x|^2}{4B|d|} - \frac{3+B|x|}{B|d|} + \frac{B+1}{B} & \text{for } -2d \leq x \leq -d \\ & \text{and } d \leq x \leq 2d \\ 0 & \text{for } |x| \geq 2d \end{cases}
 \end{aligned}$$

Fig. 4 shows the function G(x,B) for B = 3, B = 1, B = 0.8. It shows at least in qualitative terms, that the value of the parameter B affects the filtering behavior of the function. Specifically, for B = 1 the convolution function assumes unity value at the pixel being convolved and zero value at all other pixels. This means that the interpolated pixels at the original sampling points assume values equal to that of the original data samples.

Based upon the analysis of G(x) in the frequency domain it can be shown that: for B = 1 there is no filtering effect on the pixel data; for B < 1 the function acts as a high pass filter; and for B > 1 the function acts as a low pass filter.

It is this general function G(x,B) which is used to calculate weighting factors for the weighting factor memory 62. Alternate tables of weighting factors within memory 62 are used to perform different selectable filtering functions. It is also possible to combine this modified cubic convolution interpolation function with other interpolation

functions based upon up to four pixels. Further, as both the left and right halves of each of the functions are identical, it is only necessary to store half the number of values in memory 62 for each complete function.

5 The filter/interpolator module 20 shown in Fig. 1 is used in identical form for each of the modules 80-83 of Fig. 2. Three colors may be handled by the system and are processed by the module 20 in parallel and under identical programming controls. To accomplish this, the data handling
10 components of the module 20 are triplicated and the control components function to control the operation of all of the triplicated components. These triplicated components are each shown with two additional function blocks located behind the foremost. The module 20 may also be used without the
15 triplicated components to process black and white signals.

 The first step in processing data through the filter/interpolator modules 80-83 is the loading of control code into the bit-slice processor 32 of each module. This control code is programming for the bit-slice processor 32 for
20 performance of the computational and data handling functions described herein. This control code is loaded via the programmer 86 into all of the modules 80-83 present in the system. The nature of this code may be determined by persons of ordinary skill in the art given the circuitry and
25 functions described herein.

 The next step in system operation is the loading of the registers 34 of each module. These registers determine the specific processing to be performed by each module. Once the control code and registers are loaded, processing may be
30 initiated and includes data input, filtering, interpolating, resampling, data transfer and data output.

 Next, the data is inputted via buffer means 21 and is controlled by the handshake module 76 from the bit/slice processor 32. Buffers 38 and 40 are triplicated for handling
35 three separate colors. Inputted data is stored in the video random access memory 22 which is constituted by three, 4 bit wide memories of 256 rows by 256 columns of addresses. Each

memory of this size handles one color channel of the image, and thus, three memories of this size are present in each filter/interpolator module 20. By using parallel processing of all of the colors of the image, it is possible to address and control the video random access memory 22 for all three colors via a single set of address lines 43 and control lines 45 from the bit/slice processor 32. By using the eight bit address line 43, 256 addresses are available so that each of the 256 rows is addressed at once in coordination with a row address signal on control lines 45. Each of the 256 column addresses in each row can then be addressed by line 43 in coordination with a column address signal on control line 45. Memory 22 includes an output register 48 connected to a serial output port controlled by a signal from clock 49. Data can be transferred to register 48 by use of the address lines 43 and a read enable signal on control lines 45. With the data present in output register 48, each of the 256 pixels represented thereby may be clocked out of the serial port as a single 12 bit wide word.

The 12 bits for each color are fed to the separate register means 24. Likewise, a separate multiplier/accumulator 28 is used for each color and receives as an input the 12 bit bus 52 from register means 24. Multiplier/accumulators 28 also receive as an input the weighting factors via a bus 54 from the weighting factor generator 26. Parallel processing of the three colors allows a single weighting factor generator to be used for each of the modules 20 because the spatial relationship between the pixels being used and interpolated is always identical for each of the three colors.

The weighting factor generator 26 functions in response to the digitization interval stored in register 66, the filtering selection stored in register 74 and further clock pulses from the bit/slice processor 32 via lines 72. The digitization interval is repetitively added in the adder 68 with the previous sum stored in register 70 and the result becomes the new sum stored in register 70 for use as an

address by memory 62. Accumulator 68 has a 12 bit result and register 70 receives 10 of those bits which are also passed on to memory 62. An additional two bits are added from processor 32 for addressing memory 62. These are the two
 5 least significant bits which cause a set of four weighting factors to be read from memory 62 once that set of four is identified by the 10 bits from accumulator 68 and the one or more bits of filtering selection from register 74. In reference to Fig. 3, once the position x of a point being
 10 interpolated is determined by the accumulator 68, then all four weighting factors, corresponding to the four adjacent known pixels, are fixed and they may be handled as a group.

The extra two bits from accumulator 68 are fed via the overflow line 76 to control module 78, which controls the
 15 updating of pixel data within the four registers 24 and the order in which that data is fed to the multiplier/accumulator 28. Referring to Fig. 3, as the point x advances from left to right with the interpolation of each sequential new pixel, the point x eventually passes P_{J+2} and so on. Each passing
 20 of a pixel point represents one overflow digit for control module 78. Thereby, when x passes one of the known pixels, control module 78 causes the old and now unused pixel, P in the example above, to be removed and a new pixel, P_{J+4} (not shown) to be stored in its place. This new pixel is always
 25 the next pixel available from memory 22 regardless of whether horizontal or vertical interpolation is being performed. When an image is being shrunk through interpolation, the new digitization interval is always larger than the old interval and thus the overflow bits always contain a count of one or
 30 more, signalling for the replacement of one or more pixels in the registers 24.

Further, control module 78 controls the order in which the data is fed from registers 24 to multiplier/accumulator 28. As in Fig. 3, for each point x , the weighting factors
 35 for each of the four known pixels are read from memory 62 in the order W_J through W_{J+3} . Control module 78 makes sure that the corresponding pixel values are always read from registers

24 in the order P_J , through P_{J+3} . To accomplish this, module 78 simply keeps a running count of the overflow signals which count represents the pixel P_J as the first pixel to be fed to multiplier/accumulator 28 and also the first to be replaced 5 on the next overflow signal.

The output of multiplier/accumulator 28, after rounding by PAL 30, may be either restored in the memory 22 via buffer 36 or outputted from the module 20. By restoring the data, module 20 may be used to perform multiple 10 interpolation/filtering passes on the data first inputted. In the preferred embodiment each module 20 is programmable to handle four passes of the pixel data through the multiplier/accumulator 28. After each of the first three passes, the data is restored in memory 22. After the fourth 15 pass, the data is outputted from module 20. Any of the passes may include one of the selectable filtering effects as determined by the sets of weighting factors stored in memory 62. The selection of weighting factors may be changed from one pass to the next.

20 It is possible to use the present invention and the embodiment shown in the module 20 to perform either horizontal or vertical interpolation in each of the four passes or a combination of both horizontal and vertical interpolation. To achieve this the data is stored in memory 25 22 in the order in which it will be used by multiplier/interpolator 28. For horizontal interpolation, lines of pixel data are stored in rows of memory 22. Thusly the line data may be transferred in row form to output register 48 from where the pixel data is sequentially fed. 30 In order to perform vertical interpolation the data points used are vertically adjacent pixel data points from four adjacent lines of the original pixel data. Thus vertical interpolation requires that four different pixel lines of data be simultaneously accessed. In order to perform this 35 and use the circuitry previously described to maintain the same calculating speed, the data points which are intended for vertical interpolation are stored in memory 22 in the

order in which they will be used. This is accomplished under the control of bit-slice processor 32. Thus the first pixel from the first line is stored first; the first pixel from the second line is stored next; the first pixel from the third line is stored next; and the first pixel from the fourth line is stored next. The fifth pixel position receives the second pixel from the first line followed by the second pixels from the second, third and fourth lines, respectively. This arrangement allows the multiplier/accumulator 28 to serially compute one or more vertically interpolated lines of data. The number of lines produced depends upon the amplification factor controlled by the digitization interval in register 66. Pixel lines vertically interpolated in this manner may be either restored in memory 22 or transferred to the next filtering module or out of the system. Selectable filtering effects are likewise available for vertical interpolation. Each module 20 has the capability of performing four passes of vertical interpolation through the use of memory means 22 each of which is capable of storing 16 horizontal lines of pixel data. As mentioned, the highest order interpolation is always performed first to create room in memory for the results of lower order interpolations.

To perform a combination of horizontal and vertical interpolation, data is restored in memory 22 in the order in which it will be used for the next sequentially interpolating pass. Thus the memory location of data being stored is carefully controlled regardless of the source of the data.

In a typical magnification process, interpolation produces both new pixels on existing pixel lines along with entirely new lines of pixels. Some of the pixels on the new lines are interpolated from known pixels while many more are typically interpolated from newly interpolated pixels. To accomplish this, module 20 may be programmed to first perform horizontal interpolation and store the new line back in memory 22. Once four lines are produced in this manner, horizontal interpolation may be used to produce intermediate lines of pixels. Module 20 is typically programmed to first

-16-

perform the highest order interpolation possible to insure memory space for lower order interpolation. Further, it is intended that the horizontal and vertical interpolation used in magnification of an image be spread over several passes and several modules which received coordinated programming for this purpose. This significantly improves processing speed and flexibility.

SUMMARY

Through the use of the apparatus described herein the 10 filtering and resampling processes may be combined into a single processing step. This combination is independently adjustable in the aspects of resampling interval and filtering effect providing a very powerful processing apparatus. For example, the combination allows the gradual 15 magnification or demagnification of an image with appropriate filtering combined with each step. This minimizes information loss in the processing even with a large change in image size. The independent adjustment further renders the apparatus flexible to change for handling images having 20 different formats. The combination of a multiplicity of filter/interpolator modules provides the most flexible image processing apparatus. Not only, may any calculated effect be easily achieved, but also experimental results may be compared by processing the same image data with the same 25 processing steps but having a different order of application to the image data. Thus, different end results may be achieved by the order of filtering and interpolation performed.

The embodiment of the present invention described above 30 is intended to be taken in an illustrative and not a limiting sense. Various modifications and changes to the described embodiment may be made by persons skilled in the art without departing from the intended scope of the present invention as defined in the appended claims. For example, the weighting 35 factor data may be calculated to represent a linear combination of this modified cubic convolution interpolation and other interpolation functions, for the purpose of

obtaining the most desired result as the practical case may dictate.

WHAT IS CLAIMED IS:

1. An apparatus for processing a set of digital data, comprising:
computational circuit means for implementing a
5 modified cubic convolution interpolation for simultaneously resampling and filtering the set of digital data.
2. The apparatus of claim 1, wherein the set of digital data represents pixel data for a two dimensional image, and further wherein the computational means is adapted
10 to implement the modified cubic convolution interpolation in each of the two dimensions.
3. The apparatus of claim 2, further comprising:
memory means for storing the pixel data;
means for coupling the pixel data from the memory
15 means to the computational means;
means for outputting and for storing in the memory means, filtered and resampled pixel data from the computational means.
4. The apparatus of claim 3, further comprising
20 bit-slice processor means for programmably controlling the memory means, the computational means and the means for outputting and for storing.
5. The apparatus of claim 4, wherein the computational means includes weighting factor generator means and means for
25 multiplying the pixel data from the memory means by weighting factors for computing filtered and resampled pixel data values, the weighting factor generator means including means for providing a selectable filtering effect on the pixel data including means for using alternate weighting factors.
- 30 6. The apparatus of claim 5, wherein the memory means includes parallel memories and the computational means includes parallel means for multiplying for separately, simultaneously and identically processing pixel data representing different colors of the same image in response
35 to a single bit-slice processor means and a single weighting factor generator means.

7. The apparatus of claim 5, wherein the means for multiplying includes a multiplier/accumulator means, and further wherein the computational means further includes register means for receiving from the memory means, pixel data which is to be used by the multiplier/accumulator means and which represents a plurality of pixels, the register means being coupled to the multiplier/accumulator means for providing the pixel data thereto.

8. The apparatus of claim 7, wherein the weighting factor generator means includes a digitization interval generator means and accumulator means for calculating the position of each sequential, filtered and resampled pixel with respect to the pixels represented by pixel data in the register means, and further wherein the accumulator means includes overflow means coupled to the register means for controlling which pixel data is present in the register means for use by the multiplier/accumulator means.

9. The apparatus of claim 8, wherein the weighting factor generator means includes a weighting factor memory having addressing means coupled to the accumulator means and to the bit-slice processor means.

10. An apparatus for processing two-dimensional image pixel data, comprising:

input means for receiving image pixel data in a line-by-line format;

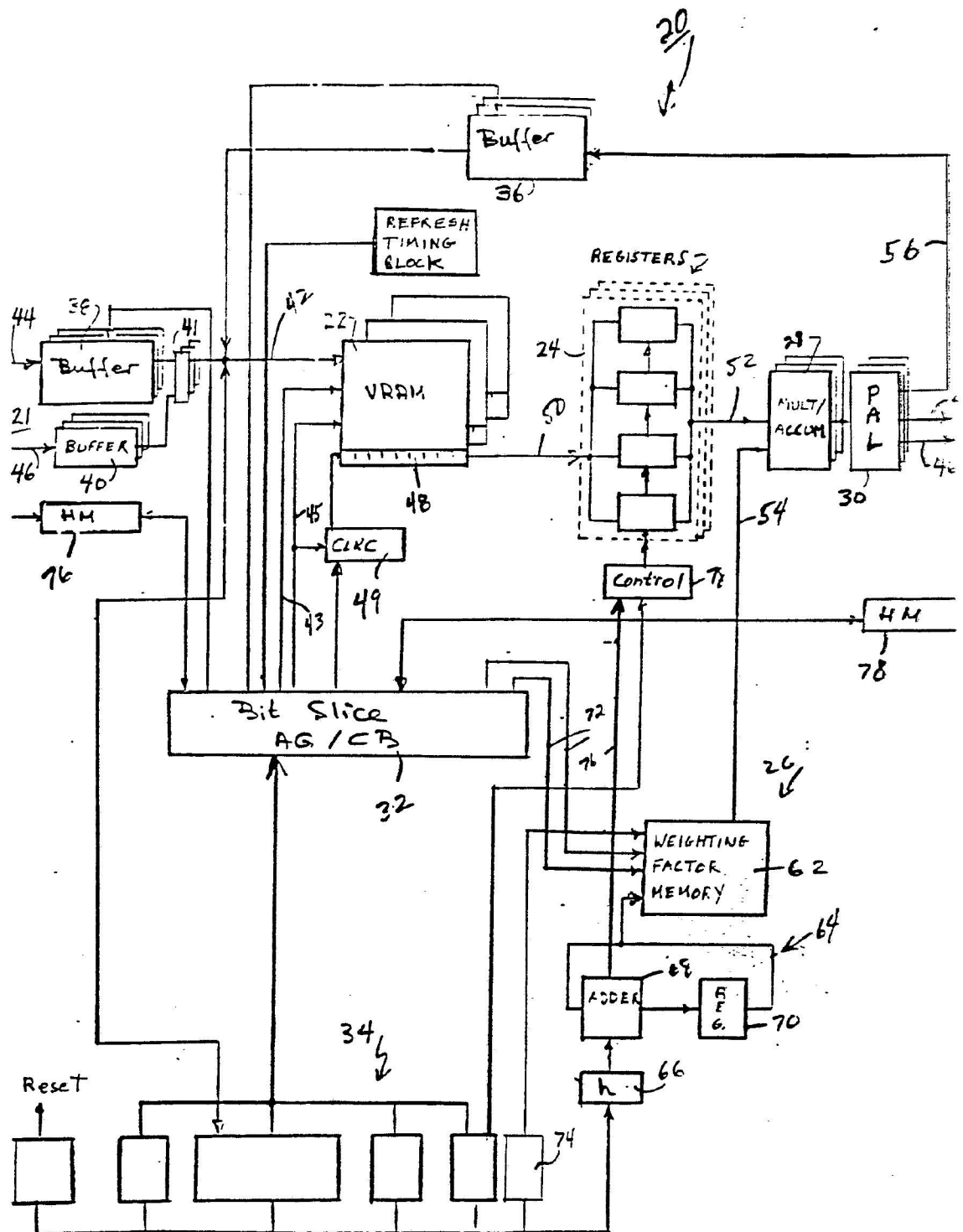
a multiplicity of substantially identical, serially coupled, programmable processing modules for simultaneously filtering and resampling image pixel data coupled therethrough from the input means;

means for separately programming each module to perform horizontal and/or vertical filtering and resampling of the image pixel data as coupled serially through the modules; and

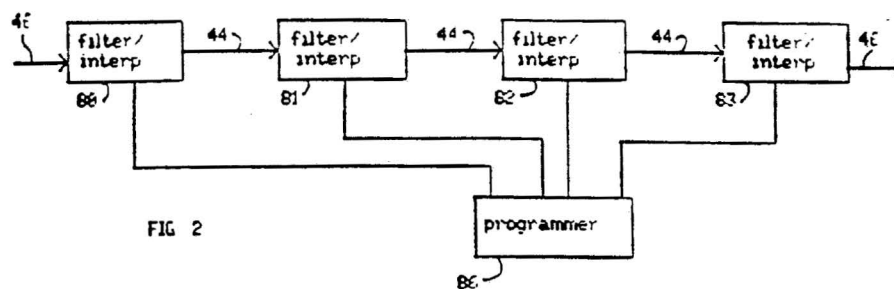
output means for further transmitting the processed image pixel data.

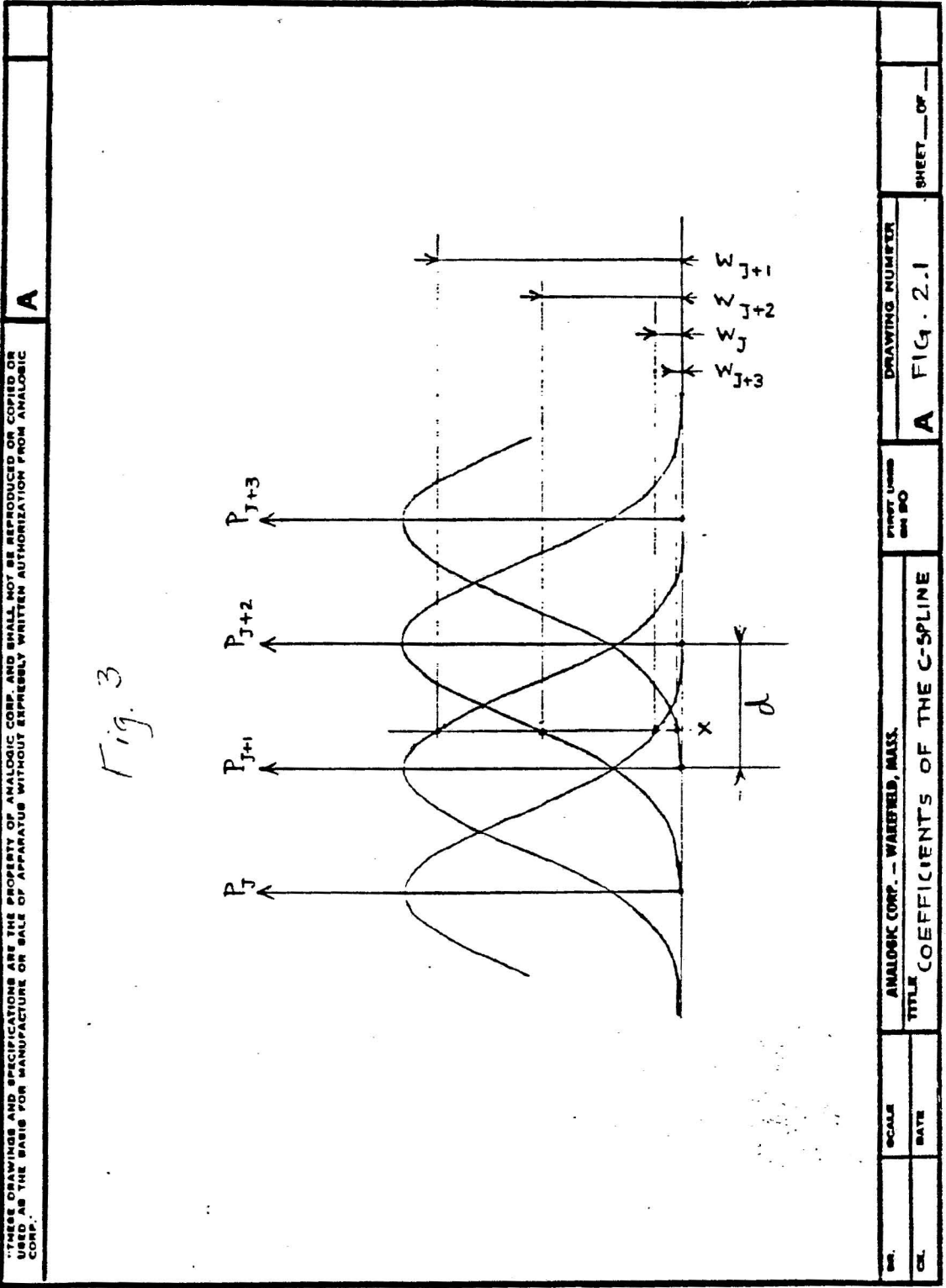
11. The apparatus of claim 10, wherein each processing module includes memory means for storing image pixel data, computational means for implementing a cubic convolution function for simultaneously filtering and resampling the
5 image pixel data, means for outputting from each module and for storing in the respective memory means, image pixel data from the respective computational means and bit-slice processor means for controlling the respective memory means and computational means.

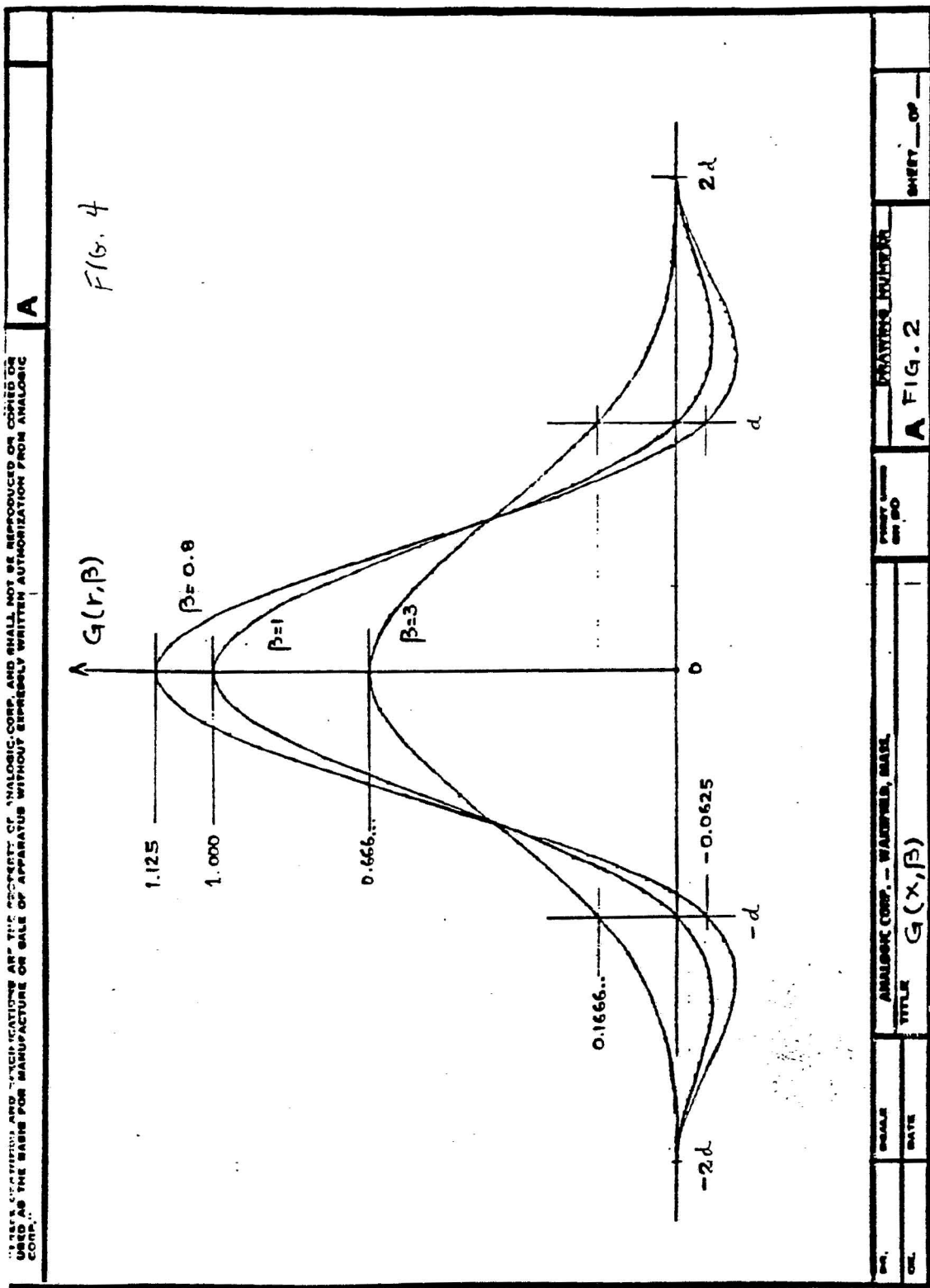
1/4



2/4







INTERNATIONAL SEARCH REPORT

International Application No. PCT/US 89/03061

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ⁶		
According to International Patent Classification (IPC) or to both National Classification and IPC		
INT. Cl. 4 G06K 9/36		
U.S. Cl. 382/41, 42		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
Classification System	Classification Symbols	
U.S.	358/138, 428, 445 382/41, 42 364/723, 724.12, 728.01, 728.02	
Documentation Searched other than Minimum Documentation to the extent that such Documents are included in the Fields Searched ⁸		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ⁹		
Category [*]	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
X	US, A 4,578,812 (Yui) 25 March 1986 see Figures 1-5 and 9 and column 3, lines 13-18, column 9, line 65 through column 10, line 13, column 7, line 61 through column 8, line 6 and column 8, line 53 through column 9, line 42.	1-11
X	US, A 4,468,693 (Fujita et al.) 28 August 1984 see figures 3, 8 and 10-17 and column 16, line 1 through column 20, line 7.	1-9
X,P	US, A 4,819,193 (Imao) 04 April 1989 see Figures 1-11 and column 5, line 48 through column 16, line 56.	1-9
X,P	US, A 4,827,433 (Kamon) 02 May 1989 see Figures 11D-15B and column 5, line 11 through column 48, line 49.	1-9
[*] Special categories of cited documents: ¹⁰ "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search		Date of Mailing of this International Search Report
29 August 1989		24 OCT 1989
International Searching Authority		Signature of Authorized Officer
ISA/US		Jose L. Couso

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)		
Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
Y	US, A 4,395,700 (McCubrey et al.) 26 July 1983 see Figure 1 and column 4, lines 46-60.	10
A	US, A 4,718,104 (Anderson) 05 January 1988 see Figures 2a-b.	10

Form PCT/ISA/210 (extra sheet) (Rev.11-87)