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Filed on behalf of **Meta Platforms, Inc.** and **Luxottica of America Inc.**

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

META PLATFORMS, INC. AND LUXOTTICA OF AMERICA INC.,
Petitioners,

v.

SOLOS TECHNOLOGY LIMITED,
Patent Owner.

Case IPR2026-00420
U.S. Patent No. 11,082,055

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 11,082,055**

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Exhibit No.	Description
1001	U.S. Patent No. 11,082,055 to Fan <i>et al.</i> (“the ’055 Patent”)
1002	File History of U.S. Patent No. 11,082,055
1003	Declaration of Thomas W. Kenny, Ph.D.
1004	Curriculum Vitae of Thomas W. Kenny, Ph.D.
1005	U.S. Patent App. Pub. No. 2013/0121504 (“Adams”)
1006	U.S. Patent App. Pub. No. 2015/0281836 (“Nguyen”)
1007	U.S. Patent App. Pub. No. 2007/0229336 (“Liu”)
1008	U.S. Patent No. 6,339,647 (“Andersen”)
1009	Reserved
1010	U.S. Patent No. 5,203,335 (“Noujaim”)
1011	R. Crochiere <i>et al.</i> , “Interpolation and Decimation of Digital Signals—A Tutorial Review,” in <i>Proc. of the IEEE</i> , vol. 69, no. 3, pp.300-331, March 1981
1012	Tiete <i>et al.</i> , “SoundCompass: A Distributed MEMS Microphone Array-Based Sensor for Sound Source Localization,” 14 Sensors 1918 (2014), available at https://www.mdpi.com/1424-8220/14/2/1918
1013	G.W. Elko and K.P. Harney, “A history of consumer microphones: The electret condenser microphone meets micro-electro-mechanical systems,” <i>Acoustics Today</i> , vol. 5, no. 2, pp. 4–13, 2009

Exhibit No.	Description
1014	R.F. Graf, <i>Modern Dictionary of Electronics</i> Seventh Edition, 1999
1015	M. Brandstein and D. Ward, Eds., <i>Microphone Arrays: Signal Processing Techniques and Applications</i> . Berlin, Germany: Springer-Verlag, 2001 (“Brandstein-Ward”)
1016	R. Kneipfer, “Sonar Beamforming – An Overview of Its History and Status,” NUWC-NL Technical Report, 10,003, 7 April 1992 (“Kneipfer”)
1017	Gannot, Sharon, and Israel Cohen. “Adaptive Beamforming and Postfiltering.” <i>Springer Handbook of Speech Processing</i> , edited by Jacob Benesty, M. Mohan Sondhi, and Yiteng Huang, Springer Berlin Heidelberg, 2008, pp. 945–978 (“Gannot-Cohen”)
1018	B. Van Veen, “Beamforming: A Versatile Approach to Spatial Filtering,” in <i>IEEE ASSP Magazine</i> , vol. 5, no. 2, pp. 4-24, April 1988) (“Van Veen”)
1019	S. R. Freeman <i>et al.</i> , “Delta-sigma oversampled ultrasound beamformer with dynamic delays,” in <i>IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control</i> , vol. 46, no. 2, pp. 320-332, March 1999
1020	C.I.C Nilsen <i>et al.</i> , “Distortion-Free Delta-Sigma Beamforming,” in <i>IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control</i> , vol. 55, no. 8, pp. 1719-1728, 2008
1021	L. Milic <i>et al.</i> , “Multirate Filters: An Overview,” <i>APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems</i> , Singapore, 2006, pp. 912-915

Exhibit No.	Description
1022	G. Moon <i>et al.</i> , “Design Approach for Decimation Filter for ADC Application,” <i>Int’l J. of Eng. Trends and Techn. (IJETT)</i> , vol. 10 no. 12 (2014)
1023	J. Yu <i>et al.</i> , “A low-power multi-bit $\Sigma\Delta$ modulator in 90-nm digital CMOS without DEM,” in <i>IEEE Journal of Solid-State Circuits</i> , vol. 40, no. 12, pp. 2428-2436, Dec. 2005
1024	Analog Devices. ADMP521 datasheet—Ultralow Noise Microphone with Bottom Port and PDM Digital Output; Technical Report; Analog Devices: Norwood, MA, USA, 2012
1025	Reserved
1026	Analog Devices, “Seamlessly Interfacing MEMS Microphones with Blackfin Processors,” Engineer-to-Engineer Note EE-350 Rev 1, August 3, 2010
1027	J. Lewis, “Microphone array beamforming,” Analog Devices, Norwood, MA, USA, Application Note AN-1140, 2012
1028	T. Kite, “Understanding PDM digital audio,” Audio Precision, Beaverton, OR, Tech. Rep., 2012

Petitioners Meta Platforms, Inc. and Luxottica of America Inc. (“Petitioners”) request *inter partes* review (“IPR”) of claims 11-18, 21-22, 34-35, 38-41, 46, and 48-50 of U.S. Patent No. 11,082,055 (“’055 patent,” Ex.1001), which is assigned to Solos Technology Limited (“PO”).

I. INTRODUCTION

The challenged claims of the ’055 patent are generally directed to (i) applying a fractional delay to an oversampled signal, (ii) decimating the fractionally delayed signal to a lower sampling rate, and (iii) applying an integer delay at the lower sampling rate. In beamforming applications, which were well-established before the ’055 patent (*see* Ex.1003, ¶¶40-60(discussing Exs.1015-1018), 74-86), applying a fractional delay in the oversampled digital domain (instead of at baseband) “represents an improvement in spatial resolution over the spatial resolution which could be achieved from integer time delay.” Ex.1001, 14:15-19. However, by August 2016, the claimed features were also well disclosed in the prior art.

Importantly, Adams discloses applying a fractional delay to an oversampled signal, before decimating, and then applying an integer delay. Adams describes the fractional delay as achieving precise steering control in beamforming. Indeed, Adams was cited in the International Search Report and Written Opinion (“ISR/WO”) for the PCT/US2017/015882 counterpart of the ’055 patent. Although

Applicant submitted the ISR/WO during prosecution, Applicant did not submit Adams as a prior-art reference to the USPTO.

As shown herein, the prior art renders all challenged '055 patent claims unpatentable. The Board should institute review and cancel those claims.

II. THE '055 PATENT

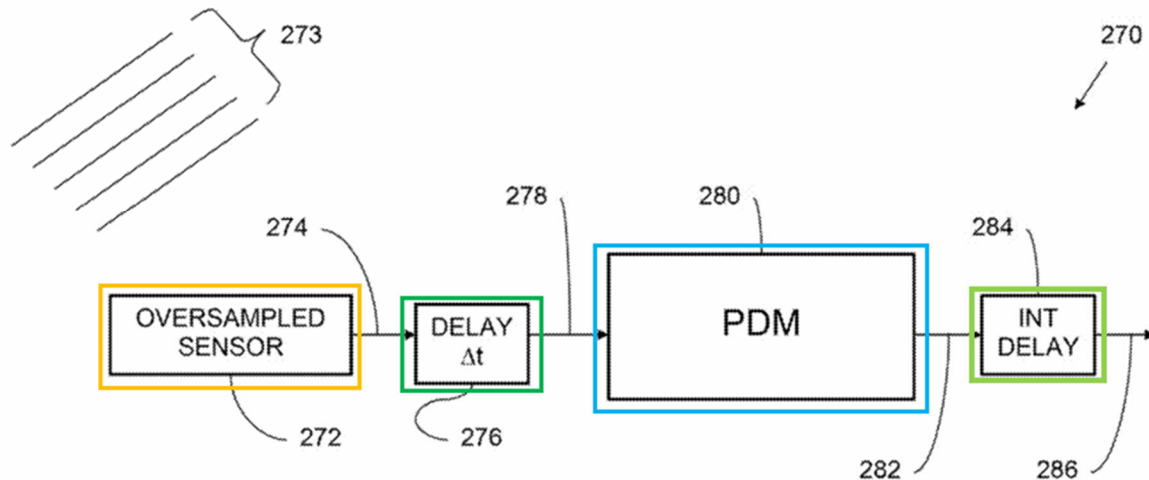
A. Overview

The '055 patent discloses a sensor, such as a digital microphone, that responds to an analog input and outputs an oversampled, high-rate digital signal. Ex.1001, Abstract, 2:49-54, Fig.1; Ex.1003, ¶¶69-72. That oversampled signal is produced by analog-to-digital conversion and later reduced to a lower-rate/baseband signal through filtering and decimation. Ex.1001, 2:54-58. The patent discloses applying delay while the signal is still in that oversampled form, upstream of at least one filter/decimator stage. *Id.*, 2:58-3:2. The patent describes that oversampled-domain delay as an integer number of high-rate sampling-clock cycles. *Id.*, 3:27-32.

Figure 2C illustrates an exemplary system 270 to time delay digital signals. Ex.1001, 5:56-7:19. This system includes a digital sensor 272, which responds to an acoustic field 273 and outputs an oversampled digital signal 274; a first delay element 276, which applies a fractional time delay to the oversampled digital signal to output a time delayed oversampled digital signal; a module 280 that low pass

filters and decimates the time delayed oversampled digital signal to output a baseband digital signal 282; and a second delay element 284, which applies an integer time delay to the baseband signal 282. *Id.*

FIGURE 2C



Ex.1001, Fig.2C(annotated).¹

B. Prosecution History

The Examiner allowed the challenged claims without rejecting them over prior art. Ex.1002, 211-217, 58, 53-55; *see also* Ex.1003, ¶73. The only rejections were non-prior art issues: nonstatutory double patenting and lack of antecedent basis. Ex.1002, 212-216. Nguyen was considered during prosecution, but Adams was not considered, nor were the prior art grounds in this petition.

¹ Petitioners have annotated figures in color throughout.

III. OVERVIEW OF PRIOR ART

A. Adams

Adams is an Analog Devices patent publication, identifying Robert Adams as first-named inventor (Ex.1005, Face), and in the field of “beamforming” including where “[m]icrophone arrays have been used to improve fidelity and reduce effects of ambient noise.” *Id.*, [0002]-[0003].

Adams discloses a multi-stage system with each stage providing both fine and coarse time delay of a respective digital microphone signal. Ex.1005, [0016], [0023]-[0029], Figs.1-6. Each stage includes a microphone, analog-to-digital converter (ADC), multiple time delay elements, a decimating filter between time delay elements, and control for setting the respective delays. *Id.*; Ex.1003, ¶¶74-76.

B. Nguyen

Nguyen is likewise an Analog Devices patent publication identifying Robert Adams as inventor. Ex.1006, Face.

Nguyen, similar to Adams, discloses a signal processing system including a digital microphone and decimating filter, among other features. Ex.1006, [0027], [0030], [0035], Figs.1, 3.

Nguyen teaches that its decimating filter provides low-pass filtering to suppress higher frequency noise components (Ex.1006, [0035], [0037]) and its digital microphone as having an integrated MEMS microphone sensor/sigma-delta

modulator ADC. Ex.1006, [0006]-[0008], [0028]-[0029]; *see also* Ex.1003, ¶¶77-82.

C. Noujaim

Noujaim discloses a shift register-based delay unit operating on oversampled bitstreams before decimation, with the desired delay selected based on the number of shift-register stages traversed. Ex.1010, Abstract, 8:65-9:42, 10:22-40; *see also* Ex.1003, ¶¶83-84.

IV. LEVEL OF ORDINARY SKILL

A hypothetical person of ordinary skill in the art (“POSA”) would have had at least a bachelor’s degree in physics, electrical engineering, computer engineering, or a similar technical field, and at least two years of experience designing or implementing digital signal-processing systems for sensors or sensor arrays. Ex.1003, ¶¶35-36. Work experience could substitute for formal education and additional formal education could substitute for work experience. *Id.*

The claims would have been obvious to a POSA under any reasonable definition. *Id.*, ¶39; *see also* ¶¶35-39.

V. CLAIM CONSTRUCTION

PO sued Petitioners for infringement of the ’055 patent in *Solos Technology Limited v. Meta Platforms, Inc. et al.*, No. 1:26-cv-10304 (D. Mass.) (“the Litigation”). The parties have not yet identified proposed constructions in that case

and, to the best of Petitioners’ current knowledge, no claim terms require express construction to resolve the obviousness challenges here, except for the terms identified below.

Claim terms receive their ordinary and customary meaning in light of the intrinsic record. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc); *see also* Ex.1003, ¶¶87-117.

Claim 46 includes six means-plus-function limitations:

- “sensing means”: The specification discloses a digital sensor (e.g., microphone) element responsive to an analog quantity. Ex.1001, Abstract, Figs.1, 2A, 2C, 1:30-38, 2:50-54, 3:10-15, 5:59-6:21, 7:24-25. The specification provides further examples, disclosing that the element “can take the form of an electret capsule microphone or...be made using microelectromechanical systems (MEMS) technology.” *Id.*, 5:60-6:3. The corresponding structure is a digital sensor element, such as a microphone (e.g., an electret capsule or MEMS microphone element); the corresponding function is “for measuring an analog field quantity.” *Id.*, cl.46.
- “over sampling means”: The specification discloses that the digital sensor “is typically configured to oversample the analog signal” and “output an oversampled digital output signal.” *Id.*, 2:51-54, Abstract; *see also id.*, 3:11-26, 7:7-19. The specification further discloses oversampling in the digital

sensor using an ADC (*id.*, 5:49-55, 14:45-15:5, 4:49-5:6) and a sigma-delta modulator as an exemplary ADC. *Id.*, 4:23-28, 6:4-9, 7:25-30. The corresponding structure is a digital sensor ADC element, such as a sigma-delta modulator; the corresponding function is “to over sample a signal detected by the sensing means resulting in an oversampled digital signal.” *Id.*, cl.46.

- “fractional delaying means”: The specification discloses a “second part 110 [which] can be referred to as a fractional delay where ‘fraction’ refers to a fraction of the baseband sampling rate period” (*id.*, 2:64-66) and a delay element 216 that imparts a time delay “ Δt ” to the oversampled digital signal 214 and “is represented by an integer number of sampling clock cycles” (*id.*, 3:27-37; *see also id.*, 6:40-43, 6:61-62). The specification discloses the delay element may be a buffer, a delay line, or a delay circuit. *Id.*, 3:42-50, 16:45-50, 16:58-60. The corresponding structure is a delay element including a buffer, delay line, or delay circuit; the corresponding function is “to apply a fractional time delay to the oversampled digital signal, the fractional time delay is equal to an integer number of sampling clock cycles, resulting in a delayed oversampled digital signal.” *Id.*, cl.46.
- “decimating means”: The specification discloses a “receiver module 220 [that] performs the functions of low pass filtering and decimation.” *Id.*, 4:57-61. The specification discloses a “filter” (*id.*, Abstract, 8:6-12, 8:14-19, 8:21-

31) or “PDM receiver module” that “decimates and low pass filters.” *Id.*, 6:49-60. The corresponding structure is a filter or PDM receiver module; the corresponding function is “to receive the delayed oversampled digital signal and to low pass filter and to decimate to a lower sampling rate.” *Id.*, cl.46.

- “integer delaying means”: The specification discloses delay “represented by an integer number of sampling clock cycles” applied by a “delay element” to an “oversampled digital signal.” Ex.1001, 3:27-54. The specification further discloses that delay can be applied by a delay element such as a delay circuit (e.g., *id.*, 2:26-27, 3:42-50, 16:58-60, Figs.15A-B) to a delayed digital signal, after decimation, where the delay is “a number of cycles at the lower sample rate.” *Id.*, 11:6-16, 8:46-9:42, Fig.4; *see also id.*, 11:17-12:6, 16:42-50. The corresponding structure is a delay element including a buffer, delay line, or delay circuit; the corresponding function is “to apply an integer time delay to the delayed oversampled digital signal, the integer time delay is a number of lower sampling rate cycles.” *Id.*, cl.46.
- “controlling means”: The specification discloses a “controller 818 [that] provides a control signal 820 to the time delay element 808” and “a control signal at 822 to the time delay element 816” and a “controller 904 [that] is used to adjust time delay(s).” *Id.*, 10:50-11:16, 11:27-29, Fig.8, Figs.15A-B. The corresponding structure is a controller configured to provide those delay

control signals; the corresponding function is “to adjust the fractional time delay and the integer time delay to establish a total time delay, wherein a resulting digital signal is delayed by a total time delay, wherein the total time delay is a sum of the fractional time delay and the integer time delay, and contains a digital representation of the analog field quantity without the noise introduced by the over sampling means.” *Id.*, cl.46.

VI. STATEMENT OF RELIEF REQUESTED

A. Grounds

Petitioners request IPR for the following grounds:

Ground	Reference(s)	Basis	Challenged Claims
1	Adams and Nguyen	§103	11-18, 21-22, 34, 38-39, 41, 46, 48-50
2	Adams, Nguyen, and Noujaim	§103	35, 40

In support of the Petition, Petitioners submit the expert declaration of Dr. Thomas W. Kenny (Ex.1003). *See* Ex.1003, ¶¶1-496; *see also* Ex.1004.

B. Asserted References

The '055 patent's earliest claimed priority date is August 1, 2016. Ex.1001. The references are prior art for the following reasons:

Ex.	Reference	Date	Art Type
1005	Adams	Filed: Mar. 23, 2012 Published: May 16, 2013	§§102(a)(1)-(2)
1006	Nguyen	Filed: Mar. 31, 2014 Published: Oct. 1, 2015	§§102(a)(1)-(2)
1010	Noujaim	Filed: Mar. 2, 1992 Published: Apr. 20, 1993	§§102(a)(1)-(2)

The references are analogous art at least because they are from the same field as the '055 patent, e.g., digital signal processing for sampled sensor systems. Ex.1003, ¶¶74-86; Ex.1001, 1:24-26, 2:44-48; *see also Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1000 (Fed. Cir. 2016). They are also pertinent to a problem the inventors were focused on, e.g., implementing delay-based beamforming in digital sensor systems. Ex.1003, ¶85.

VII. GROUND 1: CLAIMS 11-18, 21-22, 34, 38-39, 41, 46, AND 48-50 ARE OBVIOUS BASED ON ADAMS AND NGUYEN

A. Motivation to Combine

A POSA would have been motivated to combine the teachings of Adams and Nguyen. Ex.1003, ¶¶118-141.

Adams and Nguyen are directed to audio signal processing systems including many of the same features, such as a digital microphone and decimation filter. *Id.*, ¶¶121, 123-124. Both are patent publications from the same company—Analog

Devices—and share Robert Adams as inventor. *Id.*, ¶122. Nguyen was filed ~2 years after Adams. *Id.*

Regarding all challenged claims, to the extent PO argues Adams does not disclose its decimation filter as low-pass, it would have been obvious to modify Adams to provide that implementation in view of Nguyen. Ex.1003, ¶¶125-129, 143-144. To start, a POSA would have understood that decimation filters were generally low-pass to pass desired in-band audio content, suppress aliasing, and attenuate higher-frequency components, including out-of-band quantization noise. *Id.*, ¶¶128, 61-65; Ex.1014, pp.3-4; Ex.1021, p.1; Ex.1022, p.1; Ex.1011, pp.1-3; Exs.1007-1008.

Nguyen, like Adams, discloses a decimation filter in an audio microphone signal processing system to suppress higher frequency noise components, and expressly identifies the filter type as “lowpass.” Ex.1006, [0035], [0037].

A POSA implementing Adams’ system would have been motivated to combine with Nguyen’s teachings so the decimation filter is low pass, because it would have had the benefit of suppressing higher frequency noise from the decimated signal in Adams’ system, consistent with Adams’ aims. Ex.1003, ¶¶128-129, 63-65; Ex.1005, [0002], [0081]; Ex.1006, [0035], [0037].

Regarding claims 12, 13, 15, 18, 22 (and dependents), 41, and 50,² a POSA implementing Adams' system would have been further motivated to combine Nguyen's teachings with Adams so the digital microphone utilizes an integrated MEMS sensor/sigma-delta modulator. Ex.1003, ¶¶134-141.

Nguyen, like Adams, discloses a digital microphone (Ex.1006, [0001], [0004], [0006]), and specifies that it “may comprise a micro-electromechanical (MEMS) transducer element.” *Id.*, [0007]. Nguyen further discloses the MEMS microphone sensor is integrated with a follow-on circuit 100 including a sigma-delta modulator ADC. *Id.*, [0007]-[0008], [0012]-[0013], [0027]-[0030]; *see also id.*, [0001], [0035]. “[C]ircuit 100 may be shaped and sized for integration into a miniature MEMS microphone housing or package.” *Id.*, [0028].

A POSA would have been particularly motivated to combine Nguyen's teachings with Adams so the digital microphone utilizes an integrated MEMS sensor/sigma-delta modulator given the references' overlapping aims. Adams aims to reduce space consumption and costs, and improve reliability (Ex.1005, [0003]-[0004]), which it addresses with its daisy-chain approach reducing wire count. *Id.*, [0006], [0016], [0081], Fig.2.

² This combination is also provided for claims 11 and 46 as an alternative position.

Nguyen’s integrated MEMS sensor/sigma-delta modulator ADC furthers Adams’ aims. Ex.1003, ¶¶135-141. Nguyen teaches the “advantage[s]” of “integrat[ing] multiple functions in a single transducer unit such as a microphone,” e.g., “reduce[d] space consumption and lower assembly costs” (Ex.1006, [0002]-[0003], [0028]), consistent with Adams’ aims. Nguyen also discloses its integration offered “reduce[d] power consumption of active circuitry” (*Id.*, [0002]-[0003]), which Adams acknowledges would be beneficial. Ex.1005, [0067], [0094]. Nguyen, filed ~2 years after Adams, also teaches that MEMS sensors were “[c]ommonly used” by that time, “shaped and sized for portable audio devices.” Ex.1006, [0006]-[0007]; *see also* Exs.1012-1013, 1024, 1026-1027. Sigma-delta modulator ADCs were likewise well known. Ex.1023, Abstract; Exs.1019-1020; Ex.1003, ¶¶54-58, 67-68.

This combination would have implemented Nguyen’s integrated MEMS sensor/sigma-delta modulator-based frontend teachings to Adams’ microphone element/ADC to predictably produce the oversampled digital stream taught by Adams, and leaving Adams’ fine-delay, decimation, coarse-delay, and daisy chain staging unchanged. The combination would have had several benefits—including saving space, lowering assembly costs, improving reliability, and facilitating integrability in Adams’ system, consistent with Adams’ aims. Ex.1003, ¶¶134-141.

B. Reasonable Expectation of Success

A POSA would have had a reasonable expectation of success in combining Adams and Nguyen, and the result would have been predictable. Ex.1003, ¶¶142-146.

Adams and Nguyen are closely related—e.g., they concern audio microphone signal processing systems from the same company and inventor. Their systems include many of the same components, with the more recent reference, Nguyen, providing specificity regarding the type of: decimation filter (i.e., “lowpass”), microphone sensor (i.e., “MEMS”), and ADC (i.e., “sigma-delta modulator”).

Configuring Adams’ decimation filter as low pass would have been straightforward given the similarities between Adams and Nguyen. Ex.1003, ¶144. Further, Nguyen teaches that its decimation filter provides decimation factors “between 16 and 128” (Ex.1006, [0035]), consistent with factors taught by Adams. Ex.1005, [0090], [0088]. Nguyen also teaches its decimation filter downsamples from an ADC oversampled frequency to “a desired final sample rate for the outgoing digital audio stream” (Ex.1006, [0035]), similar to Adams’ downsampling from an ADC oversampled frequency to the digital “audio frame rate.” Ex.1005, [0016], [0022], cls.3, 43. Such combination would have been further facilitated because low-pass decimation filters were well known and established long before the ’055 patent. Ex.1003, ¶¶144, 61-65. A POSA would have had a reasonable expectation

of success because the proposed implementation merely applies Nguyen’s known low-pass decimation filter teachings to Adams’ known decimation filter without changing Adams’ multiple time delay operations and structure. Ex.1003, ¶144. Applying Nguyen’s teachings to Adams’ decimation filter would have been no more than the predictable use of prior-art elements according to their established functions. *Id.*

Implementing Adams’ digital microphone to utilize an integrated MEMS sensor/sigma-delta modulator, as taught by Nguyen, would have been straightforward given the similarities between Adams and Nguyen. Ex.1003, ¶¶145-146. Further, both references teach digital microphones including a sensor and ADC, with Nguyen specifying a MEMS sensor integrated with a sigma-delta modulator ADC. *Id.*, ¶¶143, 145, 123-124. Such combination would have been further facilitated because MEMS microphone sensors and sigma-delta modulator ADCs were well known and established long before the ’055 patent. Ex.1003, ¶¶145, 54-58, 66-68; Ex.1023, Abstract; Ex.1012, p.6. A POSA would have had a reasonable expectation of success because the proposed implementation simply applies Nguyen’s teachings regarding a known digital microphone utilizing an integrated MEMS sensor/sigma-delta modulator to Adams’ known digital microphone without changing Adams’ multiple time delay operations and structure. Ex.1003, ¶145. Nguyen also recognizes that “MEMS capacitive microphones” were

“[c]ommonly used” by that time, “shaped and sized for portable audio devices” (Ex.1006, [0006]-[0007]), and the circuit comprising a sigma-delta modulator “may be shaped and sized for integration into a miniature MEMS microphone housing or package” (*id.*, [0028], [0030]). This would have facilitated the combination, which would have been no more than the predictable use of prior-art elements according to their established functions. Ex.1003, ¶145.

C. Independent Claim 11

Claim 11 recites a system to time delay digital signals comprising a digital sensor, two time delay elements, a filter that low-pass filters and decimates, and a controller. Adams discloses such a system including a digital microphone sensor, two time delay elements, a decimation filter, and a controller. Nguyen similarly discloses a digital microphone sensor and a decimation filter that is “lowpass.” Together, Adams and Nguyen renders claim 11 obvious. Ex.1003, ¶¶147-209.

1. 11[pre]

To the extent limiting, Adams discloses “[a] system to time delay digital signals, comprising.” Ex.1003, ¶¶152-155; *infra* §§VII.C.2-6.

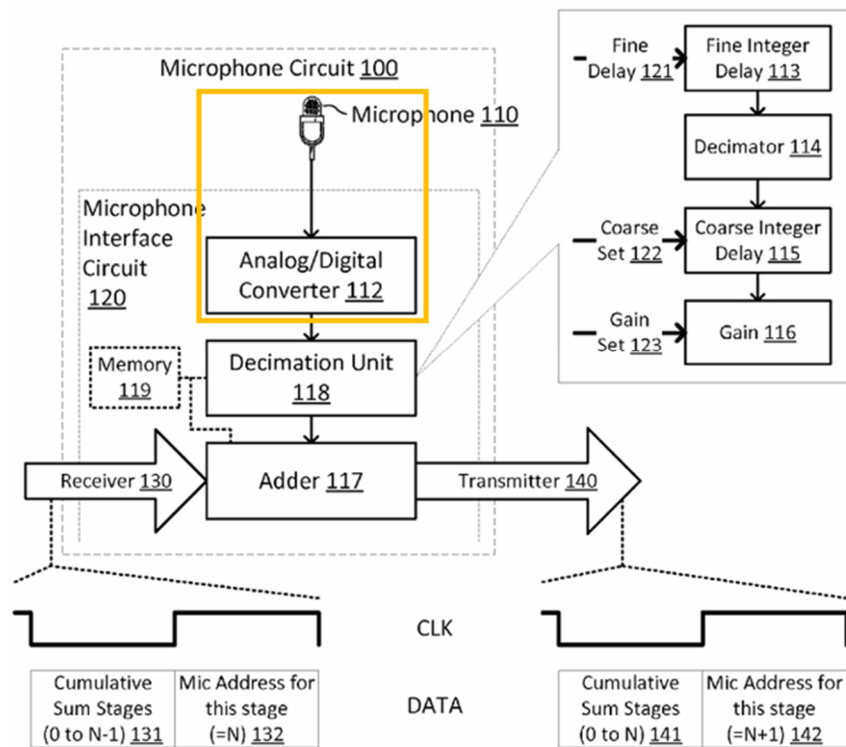
Adams discloses a system comprising circuit 100, which includes a microphone, analog-to-digital converter (ADC), decimation unit, among other elements. Ex.1005, [0016], [0023]-[0031], Figs.1-6.

The ADC “may generate digital code words from the analog audio signal obtained from the microphone.” Ex.1005, [0023]. The “decimation unit...may also include a delay unit to implement a delay.” *Id.*, [0025], [0016], Fig.1. The delays may be “selected to insure [*sic*] that the audio data from its associated microphone corresponding to sound from a particular direction is time-aligned...” *Id.*, [0022].

2. 11[a]

Adams discloses, and/or Adams in view of Nguyen, renders obvious, 11[a], which recites “a digital sensor responsive to an analog field quantity, the digital sensor is configured to output an oversampled digital output signal at a sampling clock frequency.” Ex.1003, ¶¶156-166.

Adams discloses that circuit 100 includes microphone 110 and follow-on ADC 112. Ex.1005, [0016], Fig.1; *see also id.*, Figs.2-6. The “microphone...may be coupled to” the ADC “that may generate digital code words from the analog audio signal obtained from the microphone.” *Id.*, [0023], [0027]. Thus, Adams discloses the claimed “digital sensor” as exemplified by Adams’ digital microphone comprising the microphone 110/ADC 112 combination within circuit 100. Ex.1003, ¶¶158-159. That understanding is consistent with the ’055 patent, which describes a digital microphone including a microphone and follow-on ADC, as an exemplary digital sensor. Ex.1001, 4:23-28, 5:4-6, 5:42-55, 11:19-23, 12:16-22, 13:17-22, 14:53-58, Figs.9A-9B, 10, cl.14; Ex.1003, ¶159.

FIG. 1

Ex.1005, Fig.1(annotated).

Adams' digital sensor (e.g., microphone/ADC combination) is responsive to an analog field quantity (e.g., sound or acoustic pressure) and configured to output a corresponding digital signal. Ex.1005, [0002], [0022] ("audio data from its associated microphone corresponding to sound"), cl.21; Ex.1003, ¶¶160-161; Ex.1014, p.7, p.10. That understanding is consistent with the '055 patent, which describes its microphone responsive to an analog field relating to sound. Ex.1001, 6:4-6, 1:30-33, 7:24-25, 10:34-37, 11:19-23, 12:18-21, 13:17-21, 14:20-30, Figs.8, 9A-9B, 10(analog field quantity 802/902/1002).

Adams’ digital sensor’s ADC “may oversample the analog audio signal” and “convert sampled audio signals from the microphone into digital codes” at the ADC’s oversampled clock rate. Ex.1005, [0016], [0023]-[0024], cl.23.

Thus, Adams discloses a digital sensor (e.g., microphone/ADC combination) responsive to an analog field quantity (e.g., sound or acoustic pressure), the digital sensor configured to output an oversampled digital output signal at a sampling clock frequency (e.g., ADC output signal). Ex.1003, ¶¶156-161.

Alternatively, to the extent PO argues that Adams does not disclose 11[a], Adams in view of Nguyen renders 11[a] obvious. Like Adams, Nguyen discloses a digital microphone responsive to sound (Ex.1006, [0001], [0004], [0006] (“MEMS capacitive microphones are responsive...to...sound.”), [0007] (describing microphone “transducer element...responsive to both impinging audible sound and ultrasonic sound”), [0020]), further specifying it includes an integrated MEMS sensor/sigma-delta modulator ADC. *Id.*, [0007]-[0008], [0012]-[0013], [0027]-[0028], Fig.1; *see also id.*, [0001], [0035]. The “sigma-delta modulators preferably operate[] at an oversampled sampling frequency” and output an oversampled digital signal at that sampling frequency. *Id.*, [0012], [0030].

Adams in view of Nguyen applies Nguyen’s teaching that the digital microphone includes an integrated MEMS sensor/sigma-delta modulator, which would have been obvious. *Supra* §§VII.A-B. Thus, Adams in view of Nguyen

discloses a digital sensor, responsive to an analog field quantity, configured to output an oversampled digital output signal at a sampling clock frequency. Ex.1003, ¶¶162-166.

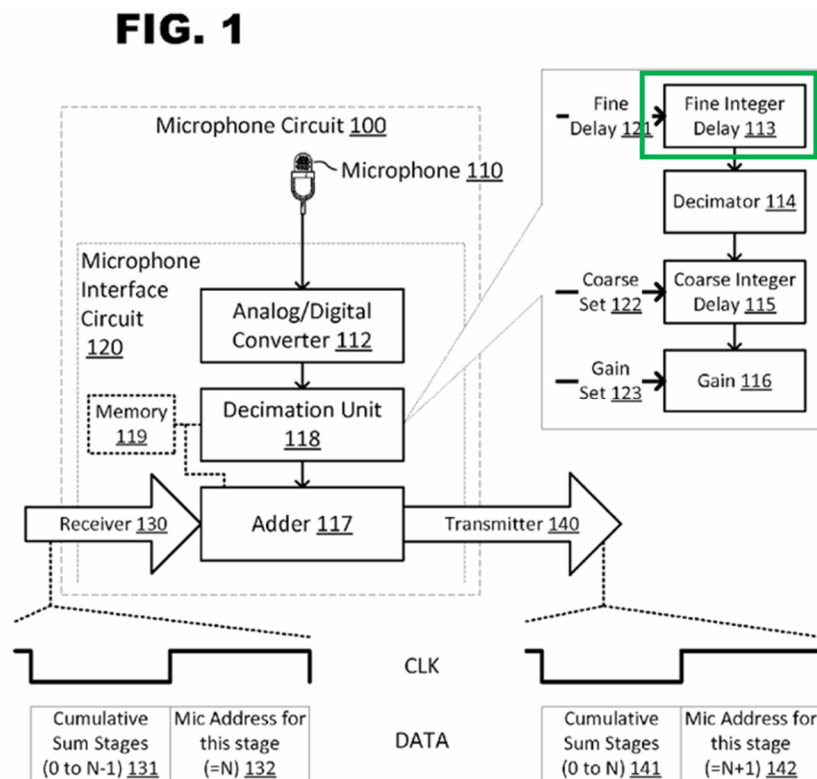
3. 11[b]

Adams discloses 11[b], which recites “a first time delay element, the first time delay element is configured to receive as an input the oversampled digital output signal and to output a time delayed oversampled digital output signal, wherein the time delayed oversampled digital output signal is time delayed by a fractional delay, the fractional delay is equal to an integer number of sampling clock cycles times the sampling clock period.” Ex.1003, ¶¶167-173.

Adams discloses a system including multiple time delay elements. Ex.1005, [0022]-[0029], Fig.1; *see also id.*, Figs.2-6. Adams states that to “achieve precise control over the steering direction, the delay at each microphone node may need to be adjusted in finer steps than can be accomplished by using an integer number of sample-periods, and therefore it may be necessary to set both an integer as well as a fractional delay amount.” *Id.*, [0022].

For this “fractional delay,” Adams relies on a first time delay element, namely “fine integer delay element 113” (hereafter, “fine delay 113”), which “use[s] the higher frequency clock rates used in the oversampling [ADCs] to implement the fractional part of the delay.” Ex.1005, [0022], [0025]-[0027]; *see also id.*, [0089].

ADC 112, which outputs an oversampled digital signal, is coupled to fine delay 113's input, which receives the oversampled digital signal. *Id.*, [0027], [0059]; *see also id.*, Figs.4-5.



Ex.1005, Fig.1(annotated).

Adams discloses that fine delay 113 “may include a fine delay input 121...to select a whole number of cycles at the higher frequency of the [ADC] 112 to delay the generated digital code words outputted by the converter 112.” Ex.1005, [0027]. A “whole number” is an “integer,” as a POSA would have understood. Ex.1003, ¶171; Ex.1014, p.5. Since one sampling clock cycle has a time duration of one sampling clock period, the delay in units of time is an integer number of (ADC)

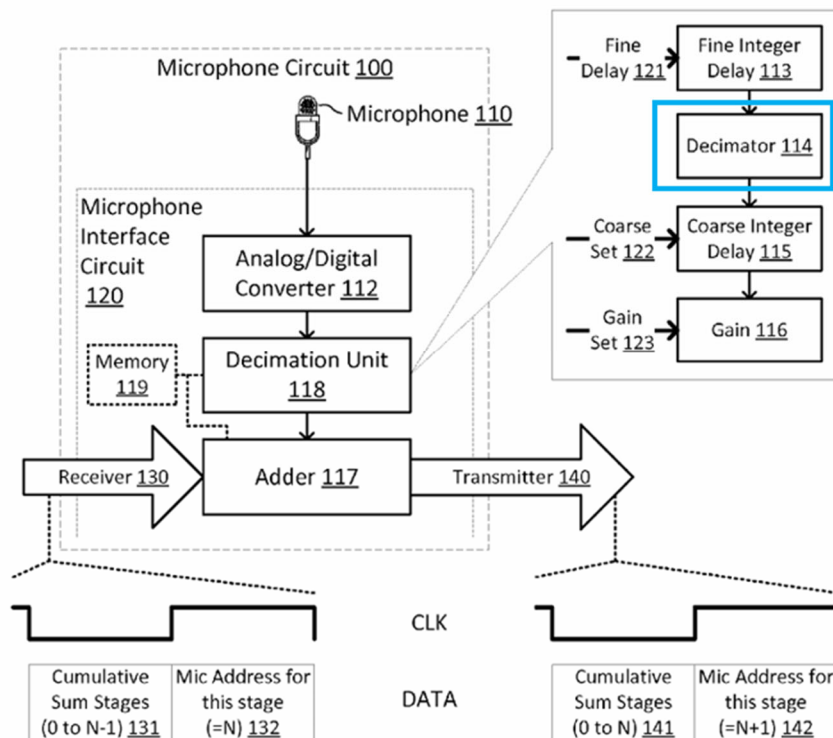
sampling clock cycles times the (ADC) sampling clock period. Ex.1003, ¶¶172-173; Ex.1014, p.8.

Thus, Adams discloses a first time delay element (i.e., fine delay 113) configured to receive as an input the oversampled digital output signal (i.e., ADC output signal) and to output a time delayed oversampled digital output signal, wherein the time delayed oversampled digital output signal is time delayed by a fractional delay, the fractional delay is equal to an integer number of sampling clock cycles times the sampling clock period. Ex.1003, ¶¶167-173.

4. 11[c]

Adams in view of Nguyen renders obvious 11[c], which recites “a filter, the filter is configured to receive as an input the time delayed oversampled digital output signal, the filter to low pass filter and to decimate to a lower sample rate the time delayed oversampled digital output signal and to output a low pass filtered decimated delayed digital output signal, wherein the lower sample rate is less than the sampling clock frequency.” Ex.1003, ¶¶174-182.

Adams discloses a filter, namely “decimator 114,” that “may be coupled to the output of the fine variable integer delay 113.” Ex.1005, [0028]. Decimator 114 is the decimation element within decimator unit 118, referred to by Adams as a “decimation filter.” *Id.*, [0025], [0052], Fig.1; *see also id.*, [0088], Figs.4, 11.

FIG. 1

Ex.1005, Fig.1(annotated). Because fine delay 113 outputs a time delayed oversampled digital output signal (*supra* §VII.C.3(11[b])), Adams' filter (i.e., decimator 114) is configured to receive as an input, the time delayed oversampled digital output signal. Ex.1003, ¶¶176-177.

Adams discloses that the decimator “may decimate the digital code words by first filtering...the ADC output codes before downsampling.” Ex.1005, [0025]. Adams further discloses that decimator 114 “reduce[s] the sampling rate of the digital code words outputted by the converter 112 so that the remaining digital code words correspond to the serial data stream frame rate.” *Id.*, [0028]. Thus, decimator 114 filters and decimates (to a lower sample rate) the time delayed oversampled

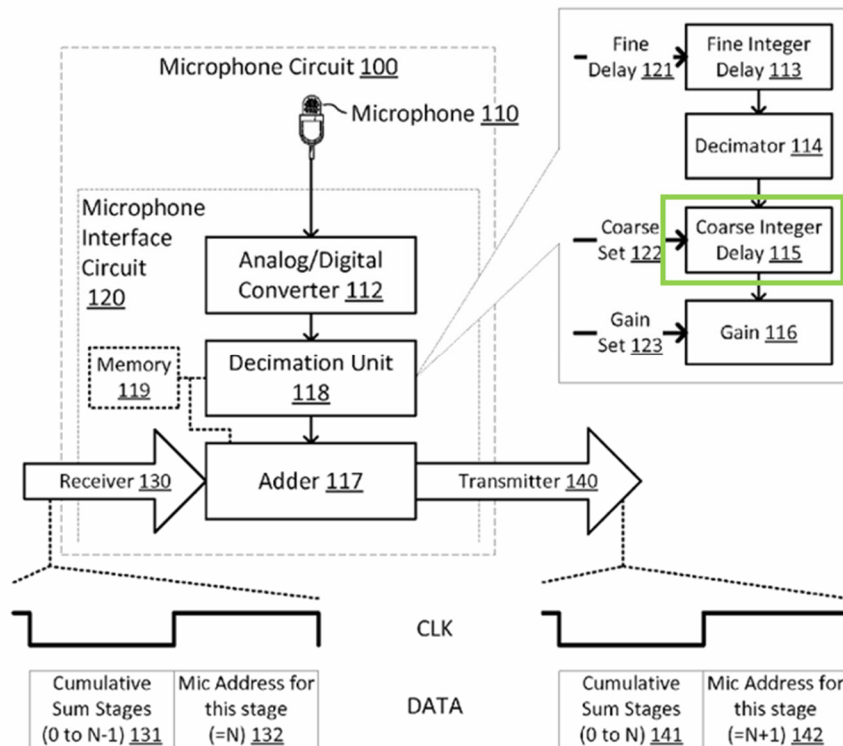
digital output signal and outputs a filtered decimated delayed digital output signal, wherein the lower sample rate is less than the sampling clock frequency. Ex.1003, ¶¶176-178.

To the extent PO argues Adams does not disclose the filtering performed by decimator 114 is “low-pass” filtering, it would have been obvious to implement Adams’ decimation filter as low-pass, as taught by Nguyen. *Supra* §§VII.A-B; Ex.1003, ¶¶179-182, 125-129, 142-144.

5. 11[d]

Adams in view of Nguyen renders obvious 11[d], which recites “a second time delay element, the second time delay element is configured to receive, as an input, the low pass filtered decimated delayed digital output signal and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times the lower sampling rate period, the integer delay is applied to the low pass filtered decimated time delayed digital output signal.” Ex.1003, ¶¶183-194.

Adams discloses a second time delay element, namely “coarse integer delay element 115” (hereafter, “coarse delay 115”) “coupled to the output of the decimator 114,” as shown in Fig.1. Ex.1005, [0029].

FIG. 1

Ex.1005, Fig.1(annotated). Because decimator 114 in the Adams in view of Nguyen system (hereafter, “Adams-Nguyen”) outputs a low pass filtered decimated delayed digital output signal (*supra* §VII.C.4(11[c])), coarse delay 115 is configured to receive, as an input, the low pass filtered decimated delayed digital output signal. Ex.1003, ¶¶188-189.

Adams also discloses that coarse delay 115 “may include a coarse delay input 122...to select a whole number of clock cycles of the serial data stream frame clock to delay the decimated code words.” Ex.1005, [0029]. A “whole number” is an “integer,” as a POSA would have understood. Ex.1003, ¶190; Ex.1014, p.5. Since one clock cycle has a time duration of one clock period, the delay in units of time is

an integer number of (serial data stream) clock cycles times the (serial data stream) clock period. Ex.1003, ¶191; Ex.1014, p.8.

Because “decimator 114...reduce[s] the sampling rate of the digital code words outputted by the [ADC] 112...to the serial data stream frame rate,” the “serial data stream frame clock” is a lower sample rate than the ADC’s oversampled rate. Ex.1005, [0028]. Thus, coarse delay 115 imparts an integer delay to the low pass filtered decimated delayed digital output signal where the integer delay is an integer number of cycles at the lower sample rate times the lower sampling rate period. Ex.1003, ¶¶191-193.

Thus, Adams-Nguyen renders obvious a second time delay element (i.e., coarse delay 115) configured to receive, as an input, the low pass filtered decimated delayed digital output signal (i.e., decimator 114 (modified in view of Nguyen) output signal) and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times the lower sampling rate period, the integer delay is applied to the low pass filtered decimated time delayed digital output signal. Ex.1003, ¶¶183-194.

6. 11[e]

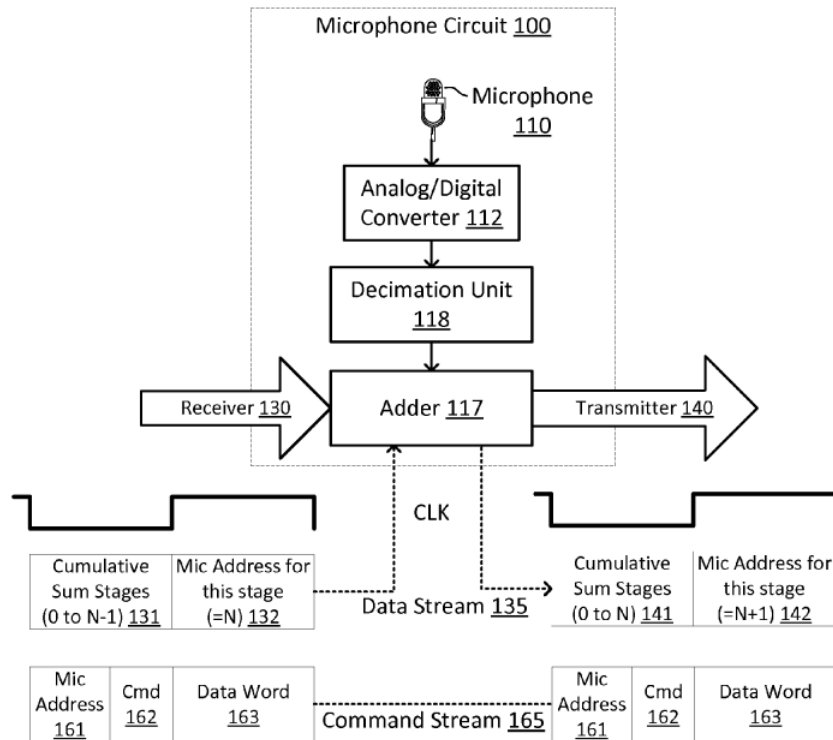
Adams discloses, and/or renders obvious, 11[e], which recites “a controller, the controller is configured to supply a control signal to set the fractional delay and the integer delay.” Ex.1003, ¶¶195-209.

Adams discloses that “[e]ach delay unit may have a delay selected” (Ex.1005, [0022]) and “[t]o achieve precise **control**,...it may be necessary to set both an integer as well as a fractional part of the delay.” *Id.* (emphasis added). Both the fractional delay unit (i.e., fine delay 113) and integer delay unit (i.e., coarse delay 115) have inputs—fine delay input 121 and coarse delay input 122—“to select” their respective delays. *Id.*, [0027], [0029]; Fig.1.

Adams explains that the “integer and the fractional delays can be set using the configuration channel transmitted to each microphone” (Ex.1005, [0022]) with “configuration data” including “delay data to set a variable delay.” *Id.*, [0021]; *see also id.*, [0034] (“inputs 121, 122...may be dynamically configured” or “predetermined”), cl.36(discussing “delay setting over the control channel”).

Adams discloses that “the amount of delay to be applied may be calculated in advance and then encoded into the data words 163 associated with respective set delay commands 162 for each microphone address 161.” Ex.1005, [0050]. This total delay is sent to the delay units via “command stream channel 165.” *Id.*, [0043], [0045].

FIG. 3



Ex.1005, Fig.3 (control format (data word 163, command 162, microphone address 161) transmitted via command stream 165).

Adams discloses that “command stream channel 165 may be used to transmit configuration data and commands to each of the circuits 100 in the array,” with “[t]he packets transmitted over” this channel “formatted to include a microphone address 161, a command code word 162, and a data word 163.” Ex.1005, [0045]. The “command code word 162 may specify a command that the addressed microphone circuit 161 is to execute,” such as “specify[ing] instructions such as setting a digital delay 118” or “gain,” for example. *Id.*, [0047]. “The data

word 163 may specify a value associated with the command code word 162,” e.g., “the value specified in data word 163 may be an amount of delay or gain that is to be set.” *Id.*, [0048].

Thus, Adams discloses a delay control signal, including fine delay input 121 and coarse delay input 122, sent via the configuration channel (e.g., command stream channel 165), to set the fractional and integer delays. *See also* Ex.1005, [0022], [0027], [0029], [0034]. A POSA would have understood that the element sending this control signal is a controller. Ex.1003, ¶202. This understanding is consistent with the '055 patent, which describes control signal 820 provided to a first delay element and control signal 822 provided to a second delay element, by a controller. *Id.*; Ex.1001, 10:32-11:16, 11:27-57, 12:7-16, 13:4-7, 16:45-17:1, Fig.8.

To the extent PO argues that Adams does not disclose 11[e], Adams renders the limitation obvious. Ex.1003, ¶¶203-209. Adams discloses a “microcontroller” that may calculate values of parameters (e.g., gain) and send to a respective circuit 100 element (e.g., amplifier/gain) to set/control the element. Ex.1005, [0087]. Adams’ gain element is on circuit 100, just like fine delay 113/coarse delay 115. *Id.*, [0023], [0026], [0047]-[0048], [0066], [0073], [0087], Fig.1.

A POSA would have been motivated to utilize Adams’ microcontroller to provide the delay control signal because the controller already exists in Adams’ system to provide a control signal to circuit 100; thus, using the same controller to

provide control signals to other elements (e.g., fine delay 113/coarse delay 115) on the circuit 100 would provide efficiencies, cost savings, and space savings from not having to develop/manufacture a separate controller. Ex.1003, ¶¶203-208. These efficiencies would have furthered Adams’ aims. *Id.*, ¶207; Ex.1005, [0003] (lamenting “require[d] additional expense and space” of other approaches). Additional efficiencies would result because the controller already provides a control signal having the same format used for delay control. Ex.1005, [0045]. A POSA would have had a reasonable expectation of success because Adams already discloses the microcontroller providing a gain control signal; the gain element is included on circuit 100 as are fine delay 113/coarse delay 115; the gain control signal is provided via command stream channel 165 with the delay control signal; and the gain control signal format is the same as the delay control signal. Ex.1003, ¶209.

D. Dependent Claims

1. Claim 12

Adams-Nguyen renders obvious claim 12, which depends from claim 11 and adds “wherein the digital sensor utilizes a sigma-delta modulator and the oversampled digital output signal is a pulse density modulated (PDM) signal.” Ex.1003, ¶¶210-220; *supra* §VII.C(cl.11).

Adams discloses the digital sensor, specifically a digital microphone comprising the microphone 110/ADC 112 combination within circuit 100, and

outputting an oversampled digital signal, as explained above for 11[a]. *Supra* §VII.C.2(11[a]).

Nguyen likewise discloses a digital microphone (Ex.1006, [0001], [0004], [0006]) and further specifies its digital signal may be “generate[d]” by a MEMS sensor with follow-on circuit 100 including a sigma-delta modulator ADC, and outputting an oversampled pulse density modulated “PDM” digital signal. *Id.*, [0007]-[0008], [0012]-[0013], [0030] (“sigma- delta modulators 110, 112 are oversampled converters operating at an oversampled sampling rate”); *see also id.*, [0001], [0035], cls.20, 33 (“sigma delta analog to digital converters”), cls.21-25, 27-31, 34-40, 42-43. The “circuit 100 may be shaped and sized for integration into a miniature MEMS microphone housing or package.” *Id.*, [0028]. The “sigma-delta modulators preferably operate[] at an oversampled sampling frequency.” *Id.*, [0012], [0030]. Thus, Nguyen discloses that its digital sensor utilizes a sigma-delta modulator and outputs an oversampled digital output signal that is a PDM signal. Ex.1003, ¶¶214-216.

To the extent PO argues that Adams does not disclose the digital sensor utilizes a sigma-delta modulator and the oversampled digital output signal is a PDM signal, it would have been obvious to provide such implementation in Adams’ system in light of Nguyen’s teachings. *Supra* §§VII.A-B; Ex.1003, ¶¶217-220, 132-143, 145-146.

2. Claim 13

Adams-Nguyen renders obvious claim 13, which depends from claim 11 and adds “wherein the oversampled digital output signal is a pulse density modulated (PDM) signal,” as explained for claim 12. *Supra* §VII.D.1(cl.12); Ex.1003, ¶¶221-223, 132-143, 145-146.

3. Claim 14

Adams-Nguyen renders obvious claim 14, which depends from claim 11, and adds “wherein the digital sensor is a digital microphone” as explained for claim 11. *Supra* §VII.C; Ex.1003, ¶¶224-226.

As explained for 11[a], Adams’ “digital sensor” is a digital microphone comprising microphone 110/ADC112. *Supra* §VII.C.2(11[a]). Alternatively, Adams in view of Nguyen discloses a digital microphone comprising an integrated MEMS sensor/sigma-delta modulator ADC. *Id.*

4. Claim 15

Adams-Nguyen renders obvious claim 15, which depends from claim 14, and adds “wherein the digital microphone utilizes a micro-electromechanical systems (MEMS) sensor.” Ex.1003, ¶¶227-236, 132-143, 145-146; *supra* §VII.D.3(cl.14).

Adams discloses a digital microphone. *Supra* §VII.C.2(11[a]). Nguyen teaches a digital microphone that “may comprise a micro-electromechanical (MEMS) transducer element.” *Id.*; Ex.1006, [0007]; *id.*, [0001], [0004], [0006].

To the extent PO argues that Adams does not disclose the digital microphone utilizes a MEMS sensor, it would have been obvious to provide such implementation, as taught by Nguyen. *Supra* §§VII.A-B; Ex.1003, ¶¶233-236, 134-143, 145-146.

5. Claim 16

Adams-Nguyen renders obvious claim 16, which depends from claim 11, and adds “wherein the analog field quantity is an acoustic pressure field.” Ex.1003, ¶¶237-239; *supra* §VII.C(cl.11).

As explained for 11[a], Adams’ “digital sensor,” comprising microphone 110/ADC 112, is “responsive to an analog field quantity,” namely sound or acoustic pressure. *Supra* §VII.C.2(11[a]). Alternatively, Adams in view of Nguyen discloses a “digital sensor,” comprising an integrated MEMS sensor/sigma-delta modulator ADC, and “responsive to an analog field quantity,” namely sound/acoustic pressure. *Id.*

6. Claim 17

Adams-Nguyen renders obvious claim 17, which depends from claim 11, and adds “wherein the integer number of sampling clock cycles is selected from a range of one to the sampling clock frequency divided by a baseband sample rate.” Ex.1003, ¶¶240-252; *supra* §VII.C(cl.11).

Adams discloses that fine delay 113 delays digital signals output from the ADC by a “select[able]” integer number of sampling clock cycles times the sampling clock period. *Supra* §VII.C.3(11[b]). This delay, which Adams identifies as “fractional” time delay (*id.*; Ex.1005, [0022], [0089]), “may enable the selection of a precise delay amount to maximize alignment of the audio signals received at different times.” Ex.1005, [0027]. The minimum number of sampling clock cycles that may have been selected, when alignment was desired, was the smallest “whole number”—one—sampling clock cycle. Ex.1003, ¶250.

Following fine delay 113, the sampling frequency is decimated “to reduce the sampling rate of the digital code words outputted by the converter 112 so that the remaining digital code words correspond to the serial data stream frame rate.” Ex.1005, [0028], [0060]; *supra* §VII.C.4(11[c]).

The “serial data stream frame rate” (also called “audio frame rate”—Ex.1005, [0016], [0022], cls.3, 43) is the rate that “audio data” is transmitted “between...each of the microphone stages.” *Id.*, [0020], [0032], [0033]; *see also id.*, Abstract, [0016], [0024], Figs.1-5. Audio is Adams’ application of interest, and the “audio frame rate” (i.e., “serial data stream frame rate”) is that application of interest’s rate or frequency. Ex.1003, ¶246; Ex.1005, Abstract, [0002], [0016]. Adams’ post-decimation “serial data stream frame rate” is a baseband sample rate. Ex.1003, ¶246. That understanding is consistent with the ’055 patent, which describes a module that

low-pass filters and decimates an oversampled digital signal as outputting a baseband digital signal at a baseband sampling rate. Ex.1001, 3:55-3:67, 6:22-39. The decimation factor equals the sampling frequency divided by the serial data stream frame rate. Ex.1003, ¶247; Ex.1005, Fig.11 (disclosing “ADC output” sampling rate as “(x) Hz,” a “decimate-by-16” stage having a “(x/16) Hz”).

One serial data stream period (i.e., one baseband sample period) includes a number of sampling clock periods (i.e., sampling periods of converter 112) equal to the decimation factor (i.e., sampling clock frequency divided by baseband sample rate). Ex.1003, ¶¶251-252; Ex.1005, [0089] (“decimation factor [of 128] indicates that 128 samples of the original ADC output code may cycled through in same time as one sample of the serial data stream”).

Adams discloses an example employing a decimation factor of 128 (Ex.1005, [0088]) and states “it would be possible to select a fractional delay amount in increments of 1/128th the sample rate of the serial data stream.” *Id.*, [0089]. With such decimation, there are 128 fractional delay steps within one sample (or period) of the serial data stream. *Id.* Thus, a one sampling clock cycle selection, as discussed above, is within claim 17’s recited range of one to the sampling clock frequency divided by the baseband sample rate (i.e., 128).

7. Claim 18

Adams-Nguyen renders obvious claim 18, which depends from claim 13, and adds “wherein the filter is a PDM receiver.” Ex.1003, ¶¶253-259, 132-143, 145-146; *supra* §VII.D.2(cl.13).

As explained for claims 12-13, Adams-Nguyen’s digital microphone outputs a PDM signal. *Supra* §§VII.D.1-2(cls.12-13). Indeed, Nguyen teaches that where the sigma-delta modulator comprises a “single-bit or one bit quantizer,” its digital output “may be conveniently supplied as [a] PDM signal[.]” Ex.1006, [0012].

As explained for 11[b], Adams-Nguyen’s fine delay 113 takes as input, and delays, the digital microphone output signal. *Supra* §VII.C.3(11[b]). Thus, fine delay 113 outputs a time delayed PDM signal. Ex.1003, ¶¶255-257.

As explained for 11[c], Adams-Nguyen’s filter is configured to receive as input, the time delayed signal output from fine delay 113. *Supra* VII.C.4(11[c]). The input received by the filter is thus a PDM signal; Nguyen indeed discloses that the digital microphone signal is received and processed by a decimation filter (decimator 306) which “comprises a lowpass filter 308” to reduce its sample rate and produce a lower-rate “outgoing digital audio stream.” Ex.1006, [0035]. Adams-Nguyen’s decimating low-pass filter is configured to receive a PDM signal and is thus a PDM receiver. Ex.1003, ¶¶257-259. That understanding is consistent with the ’055 patent, which describes elements receiving a PDM signal, including after

time delay, as a PDM receiver. *Id.*, ¶259; Ex.1001, 7:20-8:45, 9:43-10:55, Figs.3, 5-8.

8. Claim 21

Adams-Nguyen renders obvious claim 21, which depends from claim 17, and adds “wherein the lower sample rate is a baseband sample rate and the low pass filtered decimated time delayed digital output signal is used in a beam forming process with a second signal, wherein the second signal is a digital measurement of the analog field quantity.” Ex.1003, ¶¶260-271; *supra* §VII.D.6(cl.17).

As explained for 11[c], Adams’ “serial data stream frame rate” corresponds to the claimed “lower sample rate” (*supra* §VII.C.4(11[c])), and is a baseband sample rate, as explained for claim 17. *Supra* §VII.D.6(cl.17). Adams-Nguyen discloses the low pass filtered decimated time delayed digital output signal, as explained in 11[c]-[d]. *Supra* §§VII.C.4-5(11[c]-[d]).

Adams further discloses an array of microphone stages. *Supra* §III.A. Each stage includes a circuit 100 having a microphone, ADC, multiple time delay elements, a decimating filter between time delay elements, and control for setting the respective delays. Ex.1005, [0016]-[0030]; Fig.1; *see also id.*, Figs.2-6. The “microphone...may be coupled to” the ADC “that may generate digital code words from the analog audio signal obtained from the microphone.” *Id.*, [0023]. Thus, each stage’s oversampled digital signal is a digital measurement of the analog field

quantity (e.g., sound or acoustic pressure received by microphone 110) and configured to output a corresponding digital signal. Ex.1005, [0002], [0022], cl.21; Ex.1003, ¶¶268-270. That understanding is consistent with the '055 patent, which describes an analog field relating to sound. *Supra* §VII.C.2(11[a]). Each stage's "output code" thus corresponds to a filtered, decimated, and delayed (by the combined time delay) version of the respective oversampled digital signal received from the stage's ADC. Ex.1003, ¶¶268-270; *supra* §§VII.C.4-5(11[c]-[d]).

Adams further discloses that the low pass filtered decimated time delayed digital signal output from filter 114 (i.e., low-pass decimating filter as modified in view of Nguyen—*supra* §VII.C.4-5(11[c])) is further delayed by coarse delay 115 (*supra* §VII.C.5(11[d])) and subsequently combined with an "output code" from a "prior [microphone] stage[]," as described above, in a "beamform[ing]" operation in adder 117. Ex.1005, [0031], Fig.1; *see also id.*, [0037]-[0039], [0064], [0080], Fig.2; Ex.1003, ¶¶266-267.

E. Independent Claim 22

Adams-Nguyen renders obvious claim 22. Ex.1003, ¶¶272-300.

1. 22[pre]

To the extent limiting, Adams discloses "[a] system to time delay signals, comprising," as explained for 11[pre]. Ex.1003, ¶¶273-276; *supra* §VII.C.1(11[pre]); *infra* §§VII.E.2-7.

2. 22[a]

Adams discloses, and/or Adams-Nguyen renders obvious, 22[a], which recites “a sensor element, the sensor element is responsive to an analog field quantity.” Ex.1003, ¶¶277-282.

Adams discloses a sensor element (microphone 110) responsive to an analog field quantity (sound or acoustic pressure). *Supra* §VII.C.2(11[a]); Ex.1005, [0002], [0022], cl.21. Adams-Nguyen’s MEMS sensor element is likewise responsive to an analog field quantity (sound or acoustic pressure). *Supra* §VII.C.2(11[a]); Ex.1006, [0007], [0027].

3. 22[b]

Adams-Nguyen renders obvious 22[b], which recites “a sigma-delta modulator, the sensor element is electrically coupled to the sigma-delta modulator and is configured to produce a pulse density modulated (PDM) output signal at a sampling clock frequency responsive to the analog field quantity.” Ex.1003, ¶¶283-286, 132-143, 145-146.

As explained for claims 12-13 (and alternatively for 11[a]), Adams-Nguyen’s digital sensor includes an integrated MEMS sensor/sigma-delta modulator ADC, responsive to the analog field quantity, and configured to output an oversampled digital output signal at a sampling clock frequency. *Supra* §§VII.D.1-2(cls.12-13), VII.A-B, VII.C.2(11[a]). As the MEMS microphone sensor and sigma-delta

modulator ADC are integrated and electrical signals (e.g., “analog audio signal”) travel from the sensor to the ADC, Adams-Nguyen’s microphone element (MEMS sensor) is electrically coupled to the ADC (sigma-delta modulator). Ex.1003, ¶285; *see also* Ex.1005, [0024] (“The microphone...may be coupled to an [ADC] 112 that may generate digital code words from the analog audio signal obtained from the microphone 110.”); Ex.1006, [0001]. As explained, the oversampled digital output signal is a PDM signal. *Supra* §§VII.D.1-2(cls.12-13).

4. 22[c]

Adams-Nguyen renders obvious 22[c], which recites “a first time delay element, the first time delay element is electrically configured to receive the PDM output signal, and to output a delayed PDM output signal, wherein the delayed PDM output signal is delayed by a fractional time delay equal to a number of cycles of the sampling clock frequency times a period of the sampling clock.” Ex.1003, ¶¶287-289.

As explained for 11[b], Adams discloses a first time delay element (fine delay 113) that provides a fractional time delay. *Supra* §VII.C.3(11[b]). More specifically, fine delay 113 is configured to receive the oversampled digital output signal (ADC output signal) and output a time delayed oversampled digital output signal, wherein the time delayed oversampled digital output signal is time delayed by a fractional delay equal to an integer number of sampling clock cycles times the

sampling clock period. *Id.* As explained for claims 12-13, Adams-Nguyen’s oversampled digital output signal is a PDM signal. *Supra* §§VII.D.1-2(cls.12-13).

Thus, Adams-Nguyen includes fine delay 113 electrically configured to receive the PDM output signal and output a PDM output signal delayed by a fractional time delay equal to a number of cycles of the sampling clock frequency times a period of the sampling clock. Ex.1003, ¶¶287-289.

5. 22[d]

Adams-Nguyen renders obvious 22[d]. Ex.1003, ¶¶290-296.

Adams-Nguyen renders obvious “a digital sensor...configured to output an oversampled digital output signal” and “a filter, the filter is configured to receive as an input the time delayed oversampled digital output signal, the filter to low pass filter and to decimate to a lower sample rate the time delayed oversampled digital output signal and to output a low pass filtered decimated delayed digital output signal, wherein the lower sample rate is less than the sampling clock frequency.” *Supra* §§VII.C.2(11[a]), 4(11[c]). Adams-Nguyen’s filter corresponds to the claimed “decimation module,” as it provides low-pass filtering and decimation. *Id.*

As explained for claims 12-13, Adams-Nguyen’s “oversampled digital output signal” is a PDM signal. *Supra* §§VII.D.1-2(cls.12-13); Ex.1006, [0012].

Thus, Adams-Nguyen renders obvious “a decimation module, the decimation module is configured to receive as an input the delayed PDM output signal, the

decimation module to low pass filter and to decimate to a lower sample rate the delayed PDM output signal and to output a low pass filtered decimated delayed PDM output signal, wherein the lower sample rate is less than the sampling clock frequency,” for the same reasons provided for 11[a], 11[c], 12-13.

Adams-Nguyen further renders obvious “the decimation module to convert to pulse code modulation (PCM) format.” Ex.1003, ¶296. Nguyen teaches PCM conversion, starting from the native single-bit sigma-delta “PDM” output (Ex.1006, [0012]; *supra* §§VII.D.1-2(cls.12-13)), where “each of the...digital signals may be converted from native PDM format to a multi-bit or PCM format.” Ex.1006, [0012]. Adams-Nguyen includes a filter that low pass filters and decimates a time delayed PDM signal from fine delay 113 to a lower frequency, serial data stream rate (*supra* §VII.D.7(cl.18)), thus converting the PDM input into a PCM format output. Ex.1003, ¶296; Ex.1028, p.8. This understanding is consistent with the ’055 patent, which describes a PDM signal input into a module that low pass filters and decimates, as being converted to PCM format. Ex.1001, 6:49-55.

6. 22[e]

Adams-Nguyen renders obvious 22[e]. Ex.1003, ¶¶297-299.

As explained, Adams-Nguyen’s digital microphone outputs a PDM signal. *Supra* §§VII.D.1-2(cls.12-13).

As explained for 11[b], Adams-Nguyen's fine delay 113 takes as input the digital microphone output signal and delays it. *Supra* §VII.C.3(11[b]). Thus, given the digital microphone outputs a PDM signal, fine delay 113 outputs a time delayed PDM signal. Ex.1003, ¶299.

As explained for 11[c], Adams-Nguyen's decimation filter receives as input, the time delayed signal output from fine delay 113 and outputs a low pass filtered decimated delayed digital output signal. *Supra* §VII.C.4(11[c]). Thus, given fine delay 113 outputs a time delayed PDM signal, the filter outputs a low pass filtered decimated delayed PDM signal. Ex.1003, ¶299; *supra* §VII.E.5(22[d]).

As explained for 11[d], Adams-Nguyen's second time delay element (coarse delay 115) is configured to receive, as an input, the low pass filtered decimated delayed digital output signal, from the filter, and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times the lower sampling rate period, the integer delay is applied to the low pass filtered decimated time delayed digital output signal. *Supra* §VII.C.5(11[d]).

Thus, Adams-Nguyen renders obvious “a second time delay element, the second time delay element is configured to receive, as an input, the low pass filtered decimated delayed PDM output signal and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times a period at the lower sampling rate, the integer delay is applied to the low pass filtered decimated

delayed PDM output signal” for the same reasons provided for claims 11[b]-[d], 12-13. Ex.1003, ¶299.

7. 22[f]

Adams discloses and/or renders obvious 22[f], which recites “a controller, the controller is configured to supply a control signal to set the fractional delay and the integer delay” as explained for 11[e]. Ex.1003, ¶¶300, 195-209; *supra* §VII.C.6(11[e]).

F. Dependent Claims

1. Claim 34

Adams-Nguyen renders obvious claim 34, which depends from claim 22, and adds “wherein the fractional time delay is equal to a fraction of a baseband sampling period.” Ex.1003, ¶¶301-313.

As explained for 22[c], Adams-Nguyen’s fine delay 113 provides the fractional time delay. *Supra* §VII.E.4(22[c]); Ex.1005, [0022]. Adams discloses this delay may be “select[ed]” as “a whole number of cycles at the higher frequency of the” ADC.³ Ex.1005, [0027].

³ As explained for claim 22, Adams-Nguyen’s ADC is a sigma-delta modulator outputting an oversampled PDM signal at a sampling clock frequency. *Supra* §VII.E.3(22[b]).

Adams-Nguyen’s decimation module low pass filters and decimates a time delayed signal to a lower frequency—the “serial data stream frame rate” (*supra* §VII.E.5(22[d]); Ex.1005, [0028])—which is a baseband digital signal rate. *Supra* §§VII.D.6(c1.17); Ex.1003, ¶305.

A POSA would have understood sampling period can be calculated from sampling rate (or frequency)—specifically, $\text{sampling period} = (1/\text{sampling rate})$. Ex.1003, ¶306. Given Adams-Nguyen’s ADC sampling rate is larger than the baseband sampling rate, the ADC sampling period is less than (and thus a fraction of) the baseband sampling period. Ex.1003, ¶307.

Adams further states that “[t]o achieve precise control over the steering direction, the delay at each microphone node may need to be adjusted in finer steps than can be accomplished by using an integer number of sample-periods, and therefore it may be necessary to set both an integer as well as a fractional delay amount.” Ex.1005, [0022]. Further, “[i]n these conditions it is possible **to use the higher frequency clock rates used in the oversampling [ADCs] to implement the fractional part of the delay.**” *Id.* (emphasis added); Ex.1003, ¶309.

In such implementation, the fine delay provided by fine delay 113 corresponds to the fractional part of the delay (i.e., fraction of baseband sampling period), whereas the coarse delay provided by coarse delay 115 corresponds to the integer

part of the delay (i.e., whole number multiple of baseband sampling periods). *Supra* §VII.E.6(22[e]); Ex.1003, ¶¶308-310.

Further, as explained for claim 17, Adams discloses an example employing a decimation factor (=ADC sampling frequency/baseband sample rate) of 128. *Supra* §VII.D.6(cl.17); Ex.1005, [0088]. With such decimation, “it would be possible to select a fractional delay amount in increments of 1/128th the sample rate of the serial data stream.” *Id.*, [0089]. The minimum number of ADC sampling clock cycles that may have been selected, when fine alignment was desired, was the smallest “whole number”—one—sampling clock cycle. Ex.1003, ¶311; *supra* §VII.D.6(cl.17). A selection of one sampling clock cycle is (1/128) of the baseband sampling period and thus “a fraction of a baseband sampling period.” *Supra* §VII.D.6(cl.17); Ex.1003, ¶¶312-313.

G. Independent Claim 38

Adams-Nguyen renders obvious claim 38. Ex.1003, ¶¶314-340.

1. 38[pre]

To the extent limiting, Adams discloses “[a] method to delay digital signals, comprising.” Ex.1003, ¶¶315-319; *supra* §VII.C.1(11[pre]); *infra* §§VII.G.3-6.

Adams discloses that its ADC “may generate digital code words from the analog audio signal obtained from the microphone” (Ex.1005, [0023]) and its

downstream “decimation unit may also include a delay unit to implement a delay.”

Id., [0016], [0025], [0022], Fig.1.

2. 38[a]

Adams discloses 38[a], which recites “sensing an analog field.” Ex.1003, ¶¶320-322; *supra* §VII.C.2(11[a]).

Adams discloses microphone 110 that outputs an “analog audio signal.” Ex.1005, [0023], Abstract. The analog audio signal corresponds to the audio signal “capture[d]” by the microphone. *Id.*, [0002]. Microphones sense an analog field relating to sound. *Id.*, [0002], [0022], cl.21; Ex.1003, ¶322. That understanding is consistent with the ’055 patent. *Supra* §VII.C.2(11[a]).

3. 38[b]

Adams discloses 38[b], which recites “outputting an oversampled digital signal responsive to the sensing, wherein the oversampled digital signal is created at a sampling clock rate.” Ex.1003, ¶¶323-325; *supra* §VII.C.2(11[a]).

Adams discloses an ADC that “may generate digital codes from the analog audio signal.” Ex.1005, [0023]. The ADC “oversample[s] the analog audio signal,” which is “obtained from the microphone” at the ADC’s sampling clock rate. *Id.*, [0023]-[0024] (disclosing sampling “frequencies, such as 2.4 MHz or higher”), [0016]; Figs.1-6. Since the analog audio signal is generated by the microphone’s sensing of the analog field relating to sound, Adams’ ADC outputs an oversampled

digital signal responsive to the sensing, wherein the oversampled digital signal is created at the ADC sampling clock rate. Ex.1003, ¶325.

4. 38[c]

Adams discloses 38[c], which recites “delaying the oversampled digital signal by a fractional time delay wherein the fractional time delay is equal to an integer number of sampling clock cycles to produce a delayed oversampled digital signal.” Ex.1003, ¶¶326-330; *supra* §VII.C.3(11[b]).

Adams discloses fine delay 113 following and “coupled to” ADC 112, and thus fine delay 113 accepts as input, the oversampled digital signal output from the ADC. *Supra* §VII.C.3(11[b]); Ex.1005, [0027]. Adams further discloses that fine delay 113 is for “delay[ing],” by “a whole number of cycles at the higher frequency of [ADC] 112,” the “generated digital code words outputted by the converter 112.” Ex.1005, [0027], Figs.1-6. A “whole number” is an “integer,” as a POSA would have understood. Ex.1003, ¶¶328-330; Ex.1014, p.5. The “cycles at the higher frequency of the [ADC]” corresponds to the “sampling clock cycles.” *Supra* §VII.C.3(11[b]). Adams further identifies the delay provided by fine delay 113 as “fractional” time delay. *Id.*; Ex.1005, [0022], [0089]. Fine delay 113 outputs a time delayed oversampled digital signal. *Supra* §VII.C.3(11[b]).

Thus, Adams discloses delaying the oversampled digital signal by a fractional time delay wherein the fractional time delay is equal to an integer number of

sampling clock cycles to produce a delayed oversampled digital signal. Ex.1003, ¶330.

5. 38[d]

Adams-Nguyen renders obvious 38[d], which recites “applying a low pass filter with decimation to the delayed oversampled digital signal to output a baseband digital signal that is delayed by the fractional time delay.” Ex.1003, ¶¶331-336.

Adams discloses that decimation filter 114 is “coupled to the output of” fine delay 113 to receive as an input the time delayed oversampled digital signal output from fine delay 113. Ex.1005, [0028]; *supra* §VII.C.4(11[c]). This input is time delayed by the fractional time delay provided by fine delay 113. *Supra* §VII.C.3(11[b]). Decimation filter 114, as modified in view of Nguyen (*supra* §§VII.A-B, C.4(11[c])), outputs a low pass filtered decimated delayed digital output signal. *Id.*

Decimation filter 114 “reduce[s] the sampling rate of the digital code words to the serial data stream frame rate.” Ex.1005, [0028]; Figs.1, 4. Adams’ post-decimation “serial data stream frame rate” output is a baseband sample rate, as explained for claim 17. *Supra* §VII.D.6(cl.17). Thus, Adams-Nguyen applies a low-pass decimation filter to the delayed oversampled digital signal to output a baseband digital signal delayed by the fractional time delay. Ex.1003, ¶¶334-335.

6. 38[e]

Adams-Nguyen renders obvious 38[e], which recites “delaying the baseband digital signal by an integer time delay, wherein the integer time delay is equal to a number of cycles at a baseband sampling rate times the baseband sampling rate period.” Ex.1003, ¶¶337-340.

As explained for 38[d], Adams-Nguyen’s decimation filter 114 outputs a baseband digital signal. *Supra* §VII.G.5(38[d]).

Adams further discloses coarse delay 115 following and “coupled to” decimation filter 114 for “delay[ing]” the “decimated code words” output by decimator 114 by “a whole number of cycles of the serial data stream frame clock” (which is at the baseband sampling rate). Ex.1005, [0029]; Figs.1-6; *supra* §VII.C.5(11[d]). Since a “whole number” is an “integer,” as a POSA would have understood, coarse delay 115 delays the baseband digital signal by an integer number of baseband clock cycles. Ex.1003, ¶340; Ex.1014, p.5. Since each clock cycle has a one period duration, the delay, in time units, is an integer number of baseband clock cycles times the baseband sampling rate period. Ex.1003, ¶340; Ex.1014, p.8. Thus, Adams-Nguyen discloses “delaying the baseband digital signal by an integer time delay, wherein the integer time delay is equal to a number of cycles at a baseband sampling rate times the baseband sampling rate period.” Ex.1003, ¶340.

H. Dependent Claims

1. Claim 39

Adams-Nguyen renders obvious claim 39, which depends from claim 38, and adds “wherein the fractional time delay is equal to a fraction of a baseband sampling period.” Ex.1003, ¶¶341-353; *supra* §VII.G(cl.38).

As explained for 38[c], Adams’ fine delay (provided by fine delay 113) corresponds to the claimed “fractional time delay.” *Supra* §VII.G.4(38[c]). This delay equals a fraction of a baseband sampling period, as explained for claim 34. *Supra* §VII.F.1(cl.34); Ex.1003, ¶¶301-313, 348-353.

2. Claim 41

Adams-Nguyen renders obvious claim 41, which depends from claim 38, and adds “wherein the oversampled digital signal is digitized to create samples which are more than one bit deep.” Ex.1003, ¶¶354-364, 132-142, 145-146; *supra* §VII.G(cl.38).

The ’055 patent uses “one bit deep” and “bit depth” to refer to the number of bits used to represent a sample. Ex.1003, ¶357; Ex.1001, 4:59-5:13. To the extent PO argues that Adams-Nguyen, as described for claim 38, does not disclose the oversampled digital signal digitized to create samples more than one bit deep, a POSA would have been motivated by Nguyen’s teachings to provide such implementation. Ex.1003, ¶¶356-364, 119-124, 132-143, 145-146.

Specifically, Adams-Nguyen’s digital microphone, as explained alternatively for 11[a], included a MEMS sensor and sigma-delta ADC that sensed an analog field and in response output oversampled digital signals at the sampling rate, respectively. *Supra* §§VII.C.2(11[a]), VII.A-B. Ex. 1003, ¶358.

Nguyen further discloses its “sigma-delta modulators...may comprise a...multi-bit quantizer.” Ex.1006, [0012], [0030]. Thus, the oversampled digital signal is digitized, by the quantizer, to create “multi-bit” (i.e., more than one bit deep) samples. Ex.1003, ¶¶358-359.

I. Independent Claim 46

Adams-Nguyen renders obvious claim 46. Ex.1003, ¶¶365-437.

1. 46[pre]

To the extent limiting, Adams discloses “[a] system to delay digital signals, comprising,” as explained for 11[pre]. Ex.1003, ¶366; *supra* §VII.C.1(11[pre]); *infra* §§VII.I.2-7.

2. 46[a]

Adams discloses, and/or Adams-Nguyen renders obvious, 46[a], which recites “sensing means for measuring an analog field quantity.” Ex.1003, ¶¶367-373.

As explained for 11[a], Adams discloses a digital sensor microphone 110 responsive to an analog field quantity. *Supra* §VII.C.2(11[a]).

Adams' microphone 110 performs the function “for measuring an analog field quantity” because microphone 110 is responsive to an analog field quantity (e.g., sound or acoustic pressure). Ex.1005, [0002], [0022][0023], cl.21; Ex.1003, ¶¶367-369; Ex.1014, p.7, p.10; *supra* §VII.C.2(11[a]). That understanding is consistent with the '055 patent, which describes an analog field relating to sound, and “measurement...accomplished with” a “sensor.” *Id.*; Ex.1001, 1:30-35, 7:24-25, 10:34-37, 11:19-23, 12:18-21, 13:17-21, 14:20-30, Figs.8, 9A-9B, 10.

Adams' microphone 110 corresponds to the claimed “sensing means” because it is a microphone. Ex.1005, [0023], Fig.1; *supra* §§VII.C.2(11[a]), V.

Alternatively, to the extent PO argues that Adams does not disclose 46[a], Adams-Nguyen renders 46[a] obvious. Adams-Nguyen applies Nguyen's teaching that the digital microphone includes an integrated MEMS sensor/sigma-delta modulator, which would have been obvious. *Supra* §§VII.A-B. Adams-Nguyen's digital microphone MEMS sensor element is responsive to an analog field quantity (e.g., sound or acoustic pressure) (*Supra* §VII.C.2(11[a]); Ex.1006, [0006] (“MEMS capacitive microphones are responsive...to...sound”), [0007] (describing microphone “transducer element...responsive to both impinging audible sound and ultrasonic sound”), [0020]; *see also* Ex.1005, [0002], [0022]-[0023], cl.21; Ex.1003, ¶¶371-372; Ex.1014, p.7, p.10) and thus performs the function “for measuring an

analog field quantity.” That understanding is consistent with the ’055 patent, as described above.

Adams-Nguyen’s MEMS sensor corresponds to the claimed “sensing means” because it is a microphone, specifically a MEMS microphone. Ex.1006, [0006]-[0007]; *supra* §§VII.C.2(11[a]), V.

3. 46[b]

Adams discloses, and/or Adams-Nguyen renders obvious, 46[b], which recites “over sampling means, the over sampling means to over sample a signal detected by the sensing means resulting in an oversampled digital signal.” Ex.1003, ¶¶374-382. As explained for 11[a], Adams discloses a digital sensor ADC 112 that “may oversample the analog audio signal” received by the microphone and “convert sampled audio signals from the microphone into digital codes.” Ex.1005, [0016], [0023]-[0024], cl.23; *supra* §VII.C.2(11[a]). Thus, Adams’ ADC 112 performs the function “to over sample a signal detected by the sensing means resulting in an oversampled digital signal.”

Adams’ ADC 112 corresponds to the claimed “over sampling means” because it is an ADC, as described above. *Supra* §§VII.C.2(11[a]), V.

Alternatively, to the extent PO argues that Adams does not disclose 46[b], Adams-Nguyen renders 46[b] obvious. More specifically, as explained for claims 12-13 (and alternatively for 11[a]), Adams-Nguyen applies Nguyen’s teaching that

the digital microphone includes an integrated MEMS sensor/sigma-delta modulator, which would have been obvious. *Supra* §§VII.D.1-2(cls.12-13), VII.A-B. Thus, Adams-Nguyen’s digital microphone includes a sigma delta modulator ADC. *Id.*; *supra* §VII.C.2(11[a]).

Adams-Nguyen’s sigma-delta modulator ADC “operat[es] at an oversampled sampling rate or frequency,” and is “configured to sample” the signal from the transducer (i.e., microphone sensor) and output an oversampled digital transducer signal. Ex.1006, [0012], [0001], [0004], [0030], cl.20; *supra* §§VII.C.2(11[a]), V. Thus, Adams-Nguyen’s sigma-delta modulator ADC performs the function “to over sample a signal detected by the sensing means resulting in an oversampled digital signal.”

Adams-Nguyen’s sigma-delta modulator ADC corresponds to the claimed “over sampling means” because it is an ADC, specifically a sigma-delta modulator ADC, as described above. *Supra* §§VII.C.2(11[a]), V.

4. 46[c]

Adams discloses, and/or Adams-Nguyen renders obvious, 46[c], which recites “fractional delaying means, the fractional delaying means to apply a fractional time delay to the oversampled digital signal, the fractional time delay is equal to an integer number of sampling clock cycles, resulting in a delayed oversampled digital signal.” Ex.1003, ¶¶383-401.

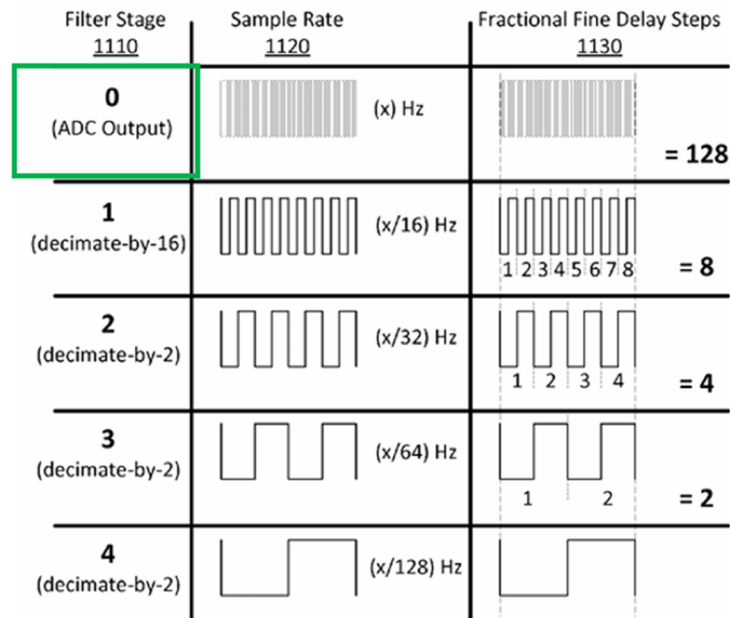
As explained for 11[b], Adams' fine delay 113, whose input is "coupled to" the ADC output (Ex.1005, [0027], Fig.1; *supra* §VII.C.3(11[b])), thus receives as input the oversampled digital output signal from the ADC and provides a time delay of "a whole number of cycles at the higher [oversampled] frequency of the [ADC]" to delay the oversampled digital output signal. *Id.*; Ex.1005, [0027], Fig.1. A "whole number" is an "integer," as a POSA would have understood. *Supra* §VII.C.3(11[b]). The oversampled digital output signal clock cycles correspond to the "sampling clock cycles." *Id.* As explained for 46[b], this oversampled digital output signal is from either Adams' over sampling means (Adams' ADC) or Adams-Nguyen's over sampling means (Adams-Nguyen's sigma-delta modulator ADC). *Supra* §VII.I.3(46[b]); Ex.1003, ¶396.

Adams further discloses that the delay provided by fine delay 113 is a "fractional" delay. *Supra* §VII.C.3(11[b]); Ex.1005, [0022], [0089]. As explained for 11[b], fine delay 113 outputs a time delayed oversampled digital signal, where the delay is the fractional time delay. *Supra* §VII.C.3(11[b]).

Thus, fine delay 113 is configured to apply a fractional time delay to the oversampled digital signal (of the ADC), the fractional time delay is equal to an integer number of sampling clock cycles, resulting in a delayed oversampled digital signal. Ex.1003, ¶¶384-388.

Adams also discloses a decimation unit in its Figure 1 time delay system, and discloses, in Figure 11, “how delay elements may be used between different filter stages” of such a multi-stage decimation unit in its system. Ex.1005, [0023], [0025], [0088]-[0095]; Ex.1003, ¶389. A POSA would have been motivated to apply Adams’ Figure 11 decimation architecture teachings in implementing the decimation unit 18 in Figure 1’s system. Ex.1003, ¶390. Adams teaches that Figure 11’s architecture provides flexibility by having multi-stage decimation, allowing the selection of different time delay resolution depending on the desired delay. Ex.1005, [0094]; *see also id.*, [0088]-[0093]. Adams teaches this has the advantage that it may “reduce the size of the delay unit and conserve power.” Ex.1005, [0094]. A POSA would have had a reasonable expectation of success in this implementation because it simply uses Adams’ known Figure 1 time delay system, including a microphone, ADC, decimation unit 118, and adder, with Adams’ Figure 11 exemplary decimation unit implementation. Ex.1003, ¶391.

Consistent with Adams’ disclosures and such implementation (i.e., Adams’ Figure 1 system with decimation unit 118 modified in view of Adams’ Figure 11 teachings), “the fractional delay [i.e., delay provided by fine delay 113] is associated with the original ADC output sample rates 1120.” Ex.1005, [0089]; Ex.1003, ¶392.

FIG. 11

Ex.1005, Fig.11(annotated). Thus, fine delay 113, including in Figure 1's system modified to employ Figure 11's decimation architecture teachings, performs the function of "to apply a fractional time delay to the oversampled digital signal, the fractional time delay is equal to an integer number of sampling clock cycles, resulting in a delayed oversampled digital signal." Ex.1003, ¶¶393-396.

Fine delay 113 also corresponds to the claimed "fractional delaying means." *Supra* §V. First, fine delay 113 is located within "circuit 100" (Ex.1005, [0023], [0025], Fig.1; *see also id.*, [0034], Figs.3-5) and is thus a delay circuit. Second, fine delay 113 provides its "delay using memory or storage units," allowing sample retention for a selected number of ADC clock cycles to ensure time alignment. Ex.1005, [0025]. Third, Adams explains this delay may be "select[ed]" and is

“programm[able].” Ex.1005, [0022], [0027], [0050]-[0051]. Thus, fine delay 113 is the same or at least structurally equivalent to the claimed “fractional delaying means.” Ex.1001, 3:42-54; Ex.1003, ¶¶397-401.

5. 46[d]

Adams-Nguyen renders obvious 46[d], which recites “decimating means, the decimating means to receive the delayed oversampled digital signal and to low pass filter and to decimate to a lower sampling rate.” Ex.1003, ¶¶402-412.

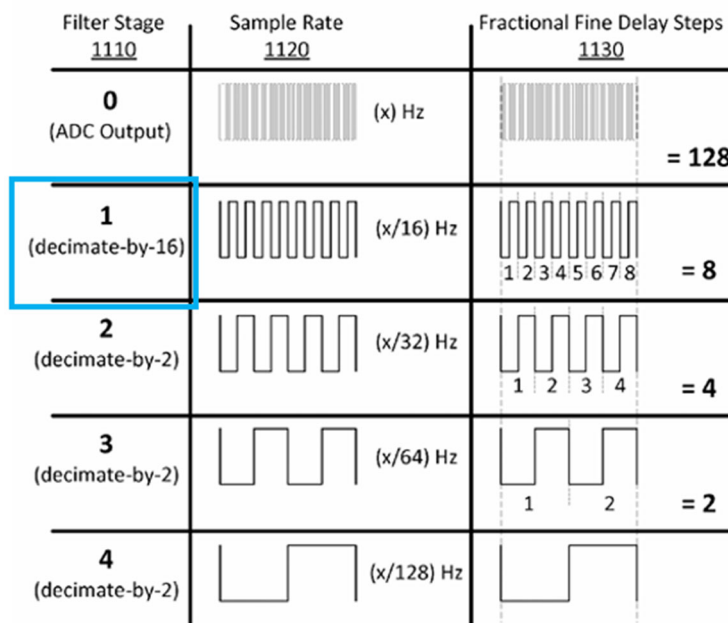
Adams’ Figure 1 system modified to implement Figure 11 decimation teachings includes a decimation unit, namely Figure 1’s Decimation unit 118 modified in view of Figure 11’s teachings regarding how its system may employ “[d]ecimation filters” in such a unit, “in a sequence of successive stages to complete the decimation process.” Ex.1005, [0025], [0088], Figs.1, 11. Adams discloses a unit employing “four filter stages” providing a total decimation factor of 128, with the first stage decimating-by-16, second stage decimating-by-2, third stage decimating-by-2, and fourth stage decimating-by-2. *Id.*, [0088]-[0093].

For this analysis, the first stage corresponds to the recited “decimating means.” Ex.1003, ¶¶403-406.

As explained, “the fractional delay” provided by fine delay 113 “is associated with the original ADC output sample rates 1120” (*supra* §VII.I.4(46[c])) and thus applies a fractional time delay to the ADC oversampled digital signal and outputs a

delayed oversampled digital signal. *Id.* The output of the fractional delaying means (i.e., fine delay 113) is coupled to the input of the multi-stage decimation circuit. Ex.1005, [0088]-[0089], Fig.11.

As Adams discloses, “[i]n the first stage” of decimation circuit 1110, “the sample rate 1120 of the ADC output codes may be decimated by a factor of 16.” Ex.1005, [0090]. Thus, the first stage receives the delayed oversampled “ADC output codes” from the fractional delaying means, and filters and decimates that signal to a lower sampling rate—specifically, the ADC oversampled rate divided by 16. Ex.1005, [0089], [0090].

FIG. 11

Ex.1005, Fig.11(annotated).

To the extent PO argues Adams does not disclose the filtering performed by decimator circuit 1110 is “low-pass” filtering, it would have been obvious to implement the filtering of Adams’ decimation circuit (i.e., “[d]ecimation filters...in a sequence of successive stages”) as low-pass, as taught by Nguyen. Ex.1003, ¶¶407-412, 119-129, 142-144; *supra* §§VII.A-B.

Thus, Adams’ first decimation filter stage, as modified in view of Nguyen, performs the function “to receive the delayed oversampled digital signal and to low pass filter and to decimate to a lower sampling rate.” Ex.1003, ¶411. This stage likewise corresponds to the claimed “decimating means” because it is a “[d]ecimation filter” that provides low-pass filtering and decimation to a lower sampling rate. Ex.1005, [0088]-[0090], Fig.11; Ex.1003, ¶412; *supra* §§VII.A-B, V.

6. 46[e]

Adams-Nguyen renders obvious 46[e], which recites “integer delaying means, the integer delaying means to apply an integer time delay to the delayed oversampled digital signal, the integer time delay is a number of lower sampling rate cycles.” Ex.1003, ¶¶413-421.

The first decimation filter stage (corresponding to 46[d]’s “decimating means”) outputs a delayed oversampled digital signal. Ex.1003, ¶415. That signal is delayed because it passed through “fractional delaying means.” *Id.*; *supra*

§VII.I.4(46[c])). That signal is oversampled because after the first stage, the sampling rate is the ADC oversampled rate divided by 16 (*supra* §VII.I.5(46[d])); Ex.1003, ¶¶414-415; Ex.1005, [0088], Fig.11), which is eight times larger than the sampling rate after stages 2-4 (*id.*), and thus still larger than, and thus oversampled, relative to the rates after stages 2-4, and oversampled relative to the baseband rate output from stage 4. Ex.1003, ¶415.

Adams discloses “delay...associated with the output of the first stage.” Ex.1005, [0090]. Further, “it would be possible to select” this “delay amount in increments of 1/8th the sample rate of the serial data stream” (*id.*), where the serial data stream rate is the ADC oversampled rate divided by 128. *Id.*, [0089]. Because the “lower sampling rate” (*supra* §VII.C.5(46[d])) is eight times the serial data stream rate, delay amounts in integer increments of lower sampling rate clock cycles may have been selected. Ex.1003, ¶416. An “integer,” as a POSA would have understood, is a number. *Id.*; Ex.1014, p.5. Thus, this “delay...associated with the output of the first stage” performs the function “to apply an integer time delay to the delayed oversampled digital signal, the integer time delay is a number of lower sampling rate cycles.” Ex.1003, ¶¶416-417.

This delay unit corresponds to the claimed “integer delaying means” because it provides the delay, as explained above, and is a circuit, given its location within the “decimation circuit.” Ex.1005, [0088], [0090], Fig.11; *see also id.*, [0034], Fig.1.

Thus, it is a delay circuit. Further, Adams discloses that its delay units provide “delay using memory or storage units,” which allow retention of samples for a selected number of lower sampling rate clock cycles “to ensure that the output codes from the decimation unit 118 align” with codes from other microphone stages. Ex.1005, [0025]. Adams further explains that this delay may be “select[ed]” and is “programmed.” Ex.1005, [0022], [0027], [0050]-[0051]. Thus, the “delay...associated with the output of the first stage” is the same or at least structurally equivalent to the claimed “integer delaying means.” Ex.1001, 2:26-27, 3:27-54, 16:45-50, Figs.15A-B; Ex.1003, ¶¶418-421; *supra* §V.

7. 46[f]

Adams-Nguyen renders obvious, 46[f], which recites “controlling means, the controlling means to adjust the fractional time delay and the integer time delay to establish a total time delay, wherein a resulting digital signal is delayed by a total time delay, wherein the total time delay is a sum of the fractional time delay and the integer time delay, and contains a digital representation of the analog field quantity without the noise introduced by the over sampling means.” Ex.1003, ¶¶422-437; *supra* §VII.C.6(11[e]).

Adams explains that “to achieve precise control...it may be necessary to set both an integer as well as a fractional delay amount” and “[e]ach delay unit may have a delay selected to insure [*sic*] that the audio data...is time-aligned.” Ex.1005,

[0022]. Adams specifies that the fractional and integer time delays may be “select[ed]” “in increments of $1/128^{\text{th}}$ ” and “increments of $1/8^{\text{th}}$ ” “the sample rate of the serial data stream,” respectively. *Id.*, [0089]-[0090].

Adams explains that the “integer and the fractional delays can be set using the configuration channel transmitted to each microphone” (Ex.1005, [0022]) with “configuration data” including “delay data to set a variable delay.” *Id.*, [0021], cl.36(discussing “delay setting over the control channel”). Adams further discloses its fractional and integer delay units have inputs “to select” their delays, which may be “programmed” and “adjusted.” *Supra* §VII.C.6(11[e]); Ex.1005, [0027], [0029], [0034], [0051].

Adams also discloses a “microcontroller” that calculates and sends control signals to set/control elements (e.g., amplifier/gain) on circuit 100. Ex.1005, [0087].

A POSA would have been motivated to utilize Adams’ microcontroller to provide the delay control signal. Ex.1003, ¶¶427-430. This is because the controller already exists in Adams’ system to provide a control signal to circuit 100 (Ex.1005, [0087], [0022]); thus, using the same controller to provide control signals to additional elements (e.g., fractional delay/integer delay) on the same circuit 100 would provide efficiencies, cost savings, and space savings from not having to develop/manufacture a separate controller. These efficiencies would have furthered Adams’ aims. Ex.1005, [0003]. Additional efficiencies would result because the

controller already provides a control signal having the same format used for delay control. Ex.1005, [0045], [0022]. A POSA would have had a reasonable expectation of success because Adams already discloses the microcontroller providing a gain control signal; the gain element is included on the same circuit 100 as the delay elements and its control signal is provided via the command stream channel and using the same control signal format as the delay control signal. Ex.1003, ¶431.

Adams' microcontroller is the same or at least structurally equivalent to the claimed "controlling means" because Adams' "microcontroller," as modified as explained above, is configured to provide control signals to adjust the fractional and integer time delays, as recited. A microcontroller also was a known structure, and the '055 patent discloses its controlling means as a controller configured to provide the aforementioned delay control signals. Ex.1003, ¶¶432-437; Ex.1014, p.6; Ex.1001, 10:50-11:16, 11:27-57, 12:7-16, 13:4-7, 16:45-17:1. Adams' "microcontroller" provides control signals to adjust the fractional and integer time delays, and accordingly establish the total time delay, which is the sum of the "fractional time delay" and "integer time delay." Ex.1003, ¶¶433-435, 437.

The digital signal output from integer delaying means is delayed by the total time delay, and includes a digital representation of the analog field quantity (sound pressure) because it corresponds to the delayed, low-pass filtered, and decimated version of the signal output from the sensing means, as explained for 46[a]. *Supra*

§VII.I.2(46[a]); Ex.1003, ¶¶436-437; *supra* §§VII.C.1-5(11[pre]-11[d]). This digital representation is without the noise introduced by the oversampling means, because the low pass filtering of the first decimation filter stage acts to remove the noise introduced by the oversampling means. *Supra* §§VII.I.5(46[d]), VII.A; Ex.1014, pp.3-4, Ex.1021, p.1, Ex.1022, p.1; Ex.1011, pp.2-3; Exs.1007-1008; Ex.1003, ¶436. This understanding is consistent with the '055 patent, which acknowledges that “[l]ow pass filtering removes the high frequency noise resulting from the oversampling process.” *Id.*; Ex.1001, 3:58-60.

Thus, Adams’ microcontroller performs the function “to adjust the fractional time delay and the integer time delay to establish a total time delay, wherein a resulting digital signal is delayed by a total time delay, wherein the total time delay is a sum of the fractional time delay and the integer time delay, and contains a digital representation of the analog field quantity without the noise introduced by the oversampling means.”

J. Dependent Claims

1. Claim 48

Adams-Nguyen renders obvious claim 48, which depends from claim 46, and adds “wherein the total time delay is equal to a fraction of a baseband sampling period.” Ex.1003, ¶¶438-447; *supra* §VII.I(cl.46).

As explained for 46[f], Adams discloses a total time delay equal to the sum of the delays provided by fractional delaying means and integer delaying means. *Supra* §VII.I.7(46[f]). Both delays are separately configurable. *Id.*; Ex.1005, [0022], [0089]-[0090].

As explained for claim 46[c], the fractional time delay provided by fine delay 113 in Adams-Nguyen’s system equals a fraction of a baseband sampling period. *Supra* §VII.I.4(46[c]).

Adams further explains that the total time delay is set “to insure [*sic*] that the audio data from its associated microphone corresponding to sound from a particular direction is time-aligned.” Ex.1005, [0022], [0025]. Thus, a POSA would have understood that the desired delay may be less than one baseband period depending on array geometry, sensor spacing, propagation speed, steering angle, and focusing requirements. Ex.1003, ¶¶443-447. For such fine delays, only fractional time delay, as discussed above for claim 46, would be set, and the integer time delay (*supra* §VII.I.6(46[e])) would be set to zero. *Id.*

2. Claim 49

Adams-Nguyen renders obvious claim 49, which depends from claim 46, and adds “wherein the total time delay is greater than a baseband sampling period.” Ex.1003, ¶¶448-454; *supra* §VII.I(c1.46).

As explained for 46[f], Adams discloses a total time delay equal to the sum of the fractional time delay and integer time delay. *Supra* §VII.I.7(46[f]).

As explained for 46[c], fractional delaying means provides delay equal to “a whole number of cycles at the higher frequency of [ADC] 112.” *Supra* §VII.I.4(46[c]).

Adams explains that total time delay is set “to insure [*sic*] that the audio data from its associated microphone corresponding to sound from a particular direction is time-aligned.” Ex.1005, [0022], [0025]. A POSA would thus have understood that the desired delay may exceed one baseband period depending on array geometry, sensor spacing, propagation speed, steering angle, and focusing requirements, and would have been motivated to have the total delay set to greater than the baseband sampling period when the requisite delay was greater than the baseband sampling period. Ex.1003, ¶¶450-453. Adams discloses total time delay being greater than a baseband sampling period in an example where total time delay is 3 ms; the decimated sample rate (baseband sample rate) is 44.1 kHz (corresponding to a baseband sampling period of ~22 us). Ex.1005, [0050]; Ex.1003, ¶454.

3. Claim 50

Adams-Nguyen renders obvious claim 50, which depends from claim 46, and adds “wherein the oversampled digital signal is digitized to create samples which are more than one bit deep.” Ex.1003, ¶¶455-465, 132-142, 145-146.

As explained, Adams-Nguyen renders obvious claim 46. *Supra* §VII.I. Adams-Nguyen further renders obvious “wherein the oversampled digital signal is digitized to create samples which are more than one bit deep,” as explained for claim 41. *Supra* §VII.H.2(c1.41); Ex.1003, ¶¶457-465.

VIII. GROUND 2: CLAIMS 35 AND 40 ARE OBVIOUS BASED ON ADAMS, NGUYEN, AND NOUJAIM

Adams-Nguyen in view of Noujaim renders obvious claims 35 and 40. Ex.1003, ¶¶466-493.

A. Motivation to Combine

A POSA would have been motivated to apply Noujaim’s multi-stage high-rate delay-register teaching to Adams-Nguyen to extend the selectable fractional time delay range, including further beyond the baseband sampling period. Ex.1003, ¶¶467-474; *supra* §VII.

Adams discloses a first time delay element configured to receive as input the oversampled digital output signal from the ADC and to output a time delayed oversampled digital output signal that is time delayed by a fractional delay equal to

an integer number of sampling clock cycles times the sampling clock period. *Supra* §§VII.E.4(22[c]), VII.G.4(38[c]), VII.C.3(11[b]); Ex.1003, ¶469.

Adams discloses an ADC sampling clock frequency of 2.4MHz. (Ex.1005, [0024], cl.23), and thus provides fractional time delays in steps of $(1/2.4\text{MHz})$, which is the sampling clock period, and equals ~ 0.416 us. Adams provides any “whole number” multiple of sampling clock periods, as the fractional delay (*supra* §§VII.E.4(22[c]), VII.G.4(38[c]), VII.C.3(11[b])), and thus is selectable in ~ 0.416 -us increments. Ex.1003, ¶470.

Following fine delay 113 (i.e., fractional delay unit) in Adams-Nguyen’s system is a filter that low pass filters and decimates to a lower sampling rate of 44kHz (i.e., system’s baseband frequency) (*supra* §§VII.E.5(22[d]), VII.G.5(38[d]), VII.C.4(11[c])), which corresponds to a baseband sampling period of ~ 22 us ($=1/44\text{kHz}$). Ex.1003, ¶471.

Noujaim discloses the same general high-rate-delay principle as Adams-Nguyen. More specifically, Noujaim discloses a delay unit (i.e., shift registers up to 80 stages in length) operating on oversampled bitstreams before decimation, with the desired delay selected based on the number of stages through which the signal traverses before being output. Ex.1010, Abstract, 8:65-9:42, 10:22-40; Ex.1003, ¶472.

A POSA would have been motivated to apply Noujaim’s 80-stage delay-register teaching to Adams-Nguyen’s 2.4MHz oversampled bitstream delay unit to extend Adams-Nguyen’s selectable delay range, up to ~33.3 us, thus beyond Adams-Nguyen’s ~22 us baseband sampling period, to provide flexibility to accommodate larger delays with fine delay 113, and retain the higher precision fine delay over a larger selectable delay range. Such implementation would have been consistent with Adams-Nguyen, as Adams does not limit the fine delay extent. Ex.1003, ¶¶473-474.

A POSA would have recognized that there are instances where the total delay required for a given microphone stage may exceed a baseband sampling period, and would have appreciated in such instances, an advantage of fine delay 113 providing a delay larger than one baseband sampling period—specifically, to maintain the higher precision delay resolution provided by fine delay 113 over a larger desired delay range. It thus would have been obvious to a POSA to set the fine delay (provided by fine delay 113) to exceed a baseband sampling period. *Id.*

B. Reasonable Expectation of Success

A POSA would have had a reasonable expectation of success in combining Adams-Nguyen and Noujaim. Ex.1003, ¶¶475-477.

Adams-Nguyen and Noujaim disclose the same fundamental architecture: ADC oversampled bitstream delay selectable units before decimation. *Supra* §§VII.E.4-5(22[c]-[d]), VII.G.4-5(38[c]-[d]), VII.C.3-4(11[b]-[c]); Ex.1010, 8:65-

9:42, 10:22-40. It is a straightforward application of a known component performing its known function to apply Noujaim’s multi-stage delay-register teaching to Adams-Nguyen’s ADC oversampled bitstream fine delay 113, and it would have extended the same delay implementation in Adams-Nguyen without changing its operation. Ex.1003, ¶476.

Thus, applying Noujaim’s teachings regarding multi-stage delay-register length to Adams-Nguyen’s architecture would have yielded predictable results, with a reasonable expectation of success. Ex.1003, ¶477.

C. Dependent Claims

1. Claim 35

Adams-Nguyen in view of Noujaim renders obvious claim 35, which depends from claim 22, and adds “wherein the fractional time delay is greater than a baseband sampling period.” Ex.1003, ¶¶478-486; *supra* §VII.E(cl.22).

Adams discloses that fine delay (corresponding to claimed “fractional time delay”) provided by fine delay 113 may be “select[ed]” as “a whole number of cycles at the higher frequency of the [ADC].” Ex.1005, [0027]; *supra* §VII.E.4(22[c]); Ex.1003, ¶481.

Adams further discloses a 2.4MHz ADC sampling clock frequency (Ex.1005, [0024], cl.23) and thus provides fractional time delays in increments of the sampling clock period (i.e., 1/2.4MHz), which equals ~0.416 us. Adams provides any “whole

number” multiple of the sampling clock periods, as the fractional time delay. *Supra* §§VII.E.4(22[c]), VII.G.4(38[c]), VII.C.3(11[b]); Ex.1003, ¶482.

As explained, Adams-Nguyen’s decimation module low pass filters and decimates a time delayed oversampled digital signal to a lower frequency (“serial data stream frame rate”), which is 44kHz (*supra* §VII.E.5(22[d]); Ex.1005, [0024], [0028]; *see also id.* [0050], [0059], cl.23) and is a baseband signal rate. *Supra* §VII.D.6(cl.17).

Noujaim teaches the same high-rate-delay principle as in Adams-Nguyen. *Supra* §VIII.A. Specifically, Noujaim teaches delay registers “80 stages in length,” with desired time delay selected based on the shift-register stage from which the signal is output. Ex.1010, 9:22-42; Ex.1003, ¶484.

To the extent PO argues that Adams-Nguyen does not disclose that the fractional time delay is greater than a baseband sampling period, a POSA would have been motivated by Noujaim’s teachings to implement such a feature in Adams-Nguyen and had a reasonable expectation of success. *Supra* §§VIII.A-B; Ex.1003, ¶¶483-486, 467-477.

A POSA would have been motivated to apply Noujaim’s multi-stage high-rate delay-register teaching to Adams-Nguyen to accommodate desired delays exceeding the lower-rate/baseband sampling period, while maintaining high precision delay resolution. *Supra* §VIII.A; Ex.1003, ¶485.

Noujaim discloses that in delay implementations using oversampled rates, high-rate delay registers may include many stages—e.g., 80—with the desired delay selected based on the stage from which the signal is output. Ex.1010, Abstract, 8:65-9:42, 10:22-40. Applying Noujaim’s 80-stage delay-register teaching to Adams-Nguyen’s 2.4MHz bitstream fine delay 113 would have predictably extended Adams-Nguyen’s selectable delay range up to ~33.3 us, exceeding Adams-Nguyen’s ~22 us baseband sampling period. *Supra* §VII.B; Ex.1003, ¶486.

2. Claim 40

Adams-Nguyen in view of Noujaim renders obvious claim 40, which depends from claim 38, and adds “wherein the fractional time delay is greater than a baseband sampling period.” Ex.1003, ¶¶487-493; *supra* §VIII.G(cl.38). A POSA would have been motivated by Noujaim’s teachings to implement such a feature in Adams-Nguyen and had a reasonable expectation of success, as explained for claim 35. *Supra* §§VIII.A-B, C.1(cl.35); Ex.1003, ¶¶493, 467-477.

IX. SECONDARY CONSIDERATIONS

Petitioners are not aware of any evidence of secondary considerations. If PO identifies evidence of secondary considerations, Petitioners request an opportunity to respond. *See* Ex.1003, ¶494.

X. STIPULATION

Petitioners stipulate that, if *inter partes* review is instituted, Petitioners will not pursue in the Litigation against any challenged claim of the '055 patent: (1) any invalidity ground that was raised or reasonably could have been raised in this IPR; or (2) any invalidity ground under 35 U.S.C. §§ 102 or 103 that relies on any prior-art reference asserted in Grounds 1-2 of the Petition, whether alone or with system art or other prior art unavailable in IPR. If institution is denied or later vacated, this stipulation has no effect.

XI. MANDATORY NOTICES

A. Real Parties-in-Interest (37 C.F.R. §42.8(b)(1))

The real parties in interest for Petitioners are: Meta Platforms, Inc.; and Luxottica of America Inc.; Oakley, Inc.; EssilorLuxottica USA Inc.

Meta Platforms, Inc. further identifies the following entity without conceding that this entity is, in fact, a real party in interest: Meta Platforms Technologies, LLC (formerly known as Facebook Technologies, LLC, which was formerly known as Oculus VR, LLC).

Luxottica of America Inc. further identifies the following entities without conceding that these entities are, in fact, real parties in interest: EssilorLuxottica America SAS; Luxottica Group SPA; Essilor International SAS; EssilorLuxottica

S.A.; Luxottica SRL; Luxottica Tristar (Dongguan) Optical Co. Ltd.; and EssilorLuxottica (Thailand) Ltd.

B. Related Matters (37 C.F.R. §42.8(b)(2))

The parties are engaged in district court litigation in *Solos Technology Limited v. Meta Platforms, Inc. et al.*, No. 1:26-cv-10304 (D. Mass.). In that action, PO asserted the '055 patent and U.S. Pat. Nos. 10,306,389 (“the '389 patent”), 10,651,866 (“the '866 patent”), 11,871,174 (“the '174 patent”), and 12,216,339 (“the '339 patent”). The '866 patent claims priority to the '055 patent. The '339 patent is currently the subject of AIA Review No. IPR2026-00376.

C. Notice of Counsel and Service Information

Petitioner provides the following designation of counsel:

Lead Counsel
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Pursuant to 37 C.F.R. § 42.10(b), Powers of Attorney accompanies this petition. Petitioners also consent to electronic service by email to PH-Meta-Solos-IPR@paulhastings.com and MLB-Luxottica-IPR-055-2@morganlewis.com.

D. Standing

The '055 patent is available for IPR, and no bar or estoppel applies.

The Office may charge any fees due to Deposit Account 50-2613.

XII. CONCLUSION

Petitioners request institution and cancellation of claims 11-18, 21-22, 34-35, 38-41, 46, and 48-50 of the '055 patent.

IPR Petition – Patent No. 11,082,055

Meta Platforms, Inc. and Luxottica of America Inc. v. Solos Technology Limited

Dated: August 7, 2026

Respectfully submitted,

By: / Lisa K. Nguyen/

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META PLATFORMS, INC.

APPENDIX: LISTING OF CLAIMS FROM U.S. PATENT NO. 11,082,055

Claim 11

- 11[pre]** A system to time delay digital signals, comprising:
- 11[a]** a digital sensor responsive to an analog field quantity, the digital sensor is configured to output an oversampled digital output signal at a sampling clock frequency;
- 11[b]** a first time delay element, the first time delay element is configured to receive as an input the oversampled digital output signal and to output a time delayed oversampled digital output signal, wherein the time delayed oversampled digital output signal is time delayed by a fractional delay, the fractional delay is equal to an integer number of sampling clock cycles times the sampling clock period;
- 11[c]** a filter, the filter is configured to receive as an input the time delayed oversampled digital output signal, the filter to low pass filter and to decimate to a lower sample rate the time delayed oversampled digital output signal and to output a low pass filtered decimated delayed digital output signal, wherein the lower sample rate is less than the sampling clock frequency;
- 11[d]** a second time delay element, the second time delay element is configured to receive, as an input, the low pass filtered decimated delayed digital output signal and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times the lower sampling rate period, the integer delay is applied to the low pass filtered decimated time delayed digital output signal; and
- 11[e]** a controller, the controller is configured to supply a control signal to set the fractional delay and the integer delay.

Claim 12

The system of claim 11, wherein the digital sensor utilizes a sigma-delta modulator and the oversampled digital output signal is a pulse density modulated (PDM) signal.

Claim 13

The system of claim 11, wherein the oversampled digital output signal is a pulse density modulated (PDM) signal.

Claim 14

The system of claim 11, wherein the digital sensor is a digital microphone.

Claim 15

The system of claim 14, wherein the digital microphone utilizes a micro-electromechanical systems (MEMS) sensor.

Claim 16

The system of claim 11, wherein the analog field quantity is an acoustic pressure field.

Claim 17

The system of claim 11, wherein the integer number of sampling clock cycles is selected from a range of one to the sampling clock frequency divided by a baseband sample rate

Claim 18

The system of claim 13, wherein the filter is a PDM receiver.

Claim 21

The system of claim 17, wherein the lower sample rate is a baseband sample rate and the low pass filtered decimated time delayed digital output signal is used in a beam forming process with a second signal, wherein the second signal is a digital measurement of the analog field quantity

Claim 22

22[pre] A system to time delay signals, comprising:

- 22[a]** a sensor element, the sensor element is responsive to an analog field quantity;
- 22[b]** a sigma-delta modulator, the sensor element is electrically coupled to the sigma-delta modulator and is configured to produce a pulse density modulated (PDM) output signal at a sampling clock frequency responsive to the analog field quantity;
- 22[c]** a first time delay element, the first time delay element is electrically configured to receive the PDM output signal, and to output a delayed PDM output signal, wherein the delayed PDM output signal is delayed by a fractional time delay equal to a number of cycles of the sampling clock frequency times a period of the sampling clock;
- 22[d]** a decimation module, the decimation module is configured to receive as an input the delayed PDM output signal, the decimation module to low pass filter and to decimate to a lower sample rate the delayed PDM output signal and to output a low pass filtered decimated delayed PDM output signal, wherein the lower sample rate is less than the sampling clock frequency, the decimation module to convert to pulse code modulation (PCM) format;
- 22[e]** a second time delay element, the second time delay element is configured to receive, as an input, the low pass filtered decimated delayed PDM output signal and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times a period at the lower sampling rate, the integer delay is applied to the low pass filtered decimated delayed PDM output signal; and
- 22[f]** a controller, the controller is configured to supply a control signal to set the fractional delay and the integer delay.

Claim 34

The system of claim 22, wherein the fractional time delay is equal to a fraction of a baseband sampling period.

Claim 35

The system of claim 22, wherein the fractional time delay is greater than a baseband sampling period.

Claim 38

- 38[pre]** A method to delay digital signals, comprising:
- 38[a]** sensing an analog field;
- 38[b]** outputting an oversampled digital signal responsive to the sensing, wherein the oversampled digital signal is created at a sampling clock rate:
- 38[c]** delaying the oversampled digital signal by a fractional time delay wherein the fractional time delay is equal to an integer number of sampling clock cycles to produce a delayed oversampled digital signal;
- 38[d]** applying a low pass filter with decimation to the delayed oversampled digital signal to output a baseband digital signal that is delayed by the fractional time delay; and
- 38[e]** delaying the baseband digital signal by an integer time delay, wherein the integer time delay is equal to a number of cycles at a baseband sampling rate times the baseband sampling rate period.

Claim 39

The method of claim 38, wherein the fractional time delay is equal to a fraction of a baseband sampling period

Claim 40

The method of claim 38, wherein the fractional time delay is greater than a baseband sampling period.

Claim 41

The method of claim 38, wherein the oversampled digital signal is digitized to create samples which are more than one bit deep.

Claim 46

- 46[pre]** A system to delay digital signals, comprising:
- 46[a]** sensing means for measuring an analog field quantity;
- 46[b]** over sampling means, the over sampling means to over sample a signal detected by the sensing means resulting in an oversampled digital signal;
- 46[c]** fractional delaying means, the fractional delaying means to apply a fractional time delay to the oversampled digital signal, the fractional time delay is equal to an integer number of sampling clock cycles, resulting in a delayed oversampled digital signal;
- 46[d]** decimating means, the decimating means to receive the delayed oversampled digital signal and to low pass filter and to decimate to a lower sampling rate;
- 46[e]** integer delaying means, the integer delaying means to apply an integer time delay to the delayed oversampled digital signal, the integer time delay is a number of lower sampling rate cycles; and
- 46[f]** controlling means, the controlling means to adjust the fractional time delay and the integer time delay to establish a total time delay, wherein a resulting digital signal is delayed by a total time delay, wherein the total time delay is a sum of the fractional time delay and the integer time delay, and contains a digital representation of the analog field quantity without the noise introduced by the over sampling means.

Claim 48

The system of claim 46, wherein the total time delay is equal to a fraction of a baseband sampling period

Claim 49

The system of claim 46, wherein the total time delay is greater than a baseband sampling period.

Claim 50

The system of claim 46, wherein the oversampled digital signal is digitized to create samples which are more than one bit deep.

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that foregoing
**PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO.
11,082,055** exclusive of the parts exempted as provided in 37 C.F.R. §42.24(a),
contains 13,997 words and therefore complies with the type-volume limitations of
37 C.F.R. §42.24(a).

Dated: August 7, 2026

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the foregoing **Petition for *Inter Partes* Review of U.S. Patent No. 11,082,055 and Exhibits 1001-1028** are being served on August 7, 2026 via Federal Express overnight mail on counsel of record for U.S. Patent No. 11,082,055 as addressed below:

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