

Filed on behalf of **Meta Platforms, Inc. and Luxottica of America Inc.**

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

META PLATFORMS, INC. AND LUXOTTICA OF AMERICA INC.,
Petitioners,

v.

SOLOS TECHNOLOGY LIMITED,
Patent Owner.

Case No. IPR2026-00420
U.S. Patent No. 11,082,055

**DECLARATION OF THOMAS W. KENNY, PH.D.
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 11,082,055**

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	BACKGROUND AND QUALIFICATIONS.....	2
III.	UNDERSTANDING OF GOVERNING LAW	7
IV.	MATERIALS REVIEWED.....	10
V.	PERSON OF ORDINARY SKILL IN THE ART.....	14
VI.	TECHNICAL BACKGROUND.....	15
A.	Beamforming Generally	20
B.	Delay-and-Sum Beamforming	22
C.	Beamforming Using Oversampled Digital Signals.....	24
D.	Decimation Filtering	30
E.	Micro-Electro-Mechanical Systems (MEMS) Sensors.....	33
VII.	THE '055 PATENT	36
A.	Description	36
B.	The Prosecution History	38
VIII.	OVERVIEW OF THE PRIOR ART	38
A.	Adams.....	38
B.	Nguyen	41
C.	Noujaim	43
D.	Analogous Art	43

IX.	CLAIM CONSTRUCTION.....	44
A.	General Understanding and Approach	44
B.	Means-Plus-Function Terms of Claim 46	45
1.	“sensing means...”	46
2.	“over sampling means...”	51
3.	“fractional delaying means...”	56
4.	“decimating means...”	59
5.	“integer delaying means...”	61
6.	“controlling means...”	65
X.	GROUND 1: CLAIMS 11-18, 21, 22, 34, 38-39, 41, 46, AND 48-50 ARE OBVIOUS BASED ON ADAMS AND NGUYEN.....	67
A.	Motivation to Combine	67
B.	Reasonable Expectation of Success	77
C.	Claim 11	80
1.	11[pre]: “A system to time delay digital signals, comprising:”	82
2.	11[a]: “a digital sensor responsive to an analog field quantity, the digital sensor is configured to output an oversampled digital output signal at a sampling clock frequency;”	83
3.	11[b]: “a first time delay element, the first time delay element is configured to receive as an input the oversampled digital output signal and to output a time delayed oversampled digital output signal, wherein the time delayed oversampled digital output signal is time delayed by a fractional delay, the fractional delay is equal	

	to an integer number of sampling clock cycles times the sampling clock period;”	90
4.	11[c]: “a filter, the filter is configured to receive as an input the time delayed oversampled digital output signal, the filter to low pass filter and to decimate to a lower sample rate the time delayed oversampled digital output signal and to output a low pass filtered decimated delayed digital output signal, wherein the lower sample rate is less than the sampling clock frequency;”	94
5.	11[d]: “a second time delay element, the second time delay element is configured to receive, as an input, the low pass filtered decimated delayed digital output signal and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times the lower sampling rate period, the integer delay is applied to the low pass filtered decimated time delayed digital output signal; and”	99
6.	11[e]: “a controller, the controller is configured to supply a control signal to set the fractional delay and the integer delay.”	103
D.	Claim 12	115
1.	“The system of claim 11, wherein the digital sensor utilizes a sigma-delta modulator and the oversampled digital output signal is a pulse density modulated (PDM) signal.”	115
E.	Claim 13	120
1.	“The system of claim 11, wherein the oversampled digital output signal is a pulse density modulated (PDM) signal.”	120
F.	Claim 14	121

1.	“The system of claim 11, wherein the digital sensor is a digital microphone.”.....	121
G.	Claim 15	121
1.	“The system of claim 14, wherein the digital microphone utilizes a micro-electromechanical systems (MEMS) sensor.”	121
H.	Claim 16	124
1.	“The system of claim 11, wherein the analog field quantity is an acoustic pressure field.”	124
I.	Claim 17	125
1.	“The system of claim 11, wherein the integer number of sampling clock cycles is selected from a range of one to the sampling clock frequency divided by a baseband sample rate.”	125
J.	Claim 18	132
1.	“The system of claim 13, wherein the filter is a PDM receiver.”	132
K.	Claim 21	136
1.	“The system of claim 17, wherein the lower sample rate is a baseband sample rate and the low pass filtered decimated time delayed digital output signal is used in a beam forming process with a second signal, wherein the second signal is a digital measurement of the analog field quantity.”	136
L.	Claim 22	140
1.	22[pre]: “A system to time delay signals, comprising:”	140
2.	22[a]: “a sensor element, the sensor element is responsive to an analog field quantity;”	142

3.	22[b]: “a sigma-delta modulator, the sensor element is electrically coupled to the sigma-delta modulator and is configured to produce a pulse density modulated (PDM) output signal at a sampling clock frequency responsive to the analog field quantity;”	145
4.	22[c]: “a first time delay element, the first time delay element is electrically configured to receive the PDM output signal, and to output a delayed PDM output signal, wherein the delayed PDM output signal is delayed by a fractional time delay equal to a number of cycles of the sampling clock frequency times a period of the sampling clock;”	148
5.	22[d]: “a decimation module, the decimation module is configured to receive as an input the delayed PDM output signal, the decimation module to low pass filter and to decimate to a lower sample rate the delayed PDM output signal and to output a low pass filtered decimated delayed PDM output signal, wherein the lower sample rate is less than the sampling clock frequency, the decimation module to convert to pulse code modulation (PCM) format;”	149
6.	22[e]: “a second time delay element, the second time delay element is configured to receive, as an input, the low pass filtered decimated delayed PDM output signal and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times a period at the lower sampling rate, the integer delay is applied to the low pass filtered decimated delayed PDM output signal; and”	153
7.	22[f]: “a controller, the controller is configured to supply a control signal to set the fractional delay and the integer delay.”	154
M.	Claim 34	154

1.	“The system of claim 22, wherein the fractional time delay is equal to a fraction of a baseband sampling period.”	154
N.	Claim 38	158
1.	38[pre]: “A method to delay digital signals, comprising:”	159
2.	38[a]: “sensing an analog field;”	161
3.	38[b]: “outputting an oversampled digital signal responsive to the sensing, wherein the oversampled digital signal is created at a sampling clock rate:”	162
4.	38[c]: “delaying the oversampled digital signal by a fractional time delay wherein the fractional time delay is equal to an integer number of sampling clock cycles to produce a delayed oversampled digital signal;”	164
5.	38[d]: “applying a low pass filter with decimation to the delayed oversampled digital signal to output a baseband digital signal that is delayed by the fractional time delay; and”	165
6.	38[e]: “delaying the baseband digital signal by an integer time delay, wherein the integer time delay is equal to a number of cycles at a baseband sampling rate times the baseband sampling rate period.”	167
O.	Claim 39	168
1.	“The method of claim 38, wherein the fractional time delay is equal to a fraction of a baseband sampling period.”	168
P.	Claim 41	172
1.	“The method of claim 38, wherein the oversampled digital signal is digitized to create samples which are more than one bit deep.”	172

Q.	Claim 46	177
1.	46[pre]: “A system to delay digital signals, comprising:”	177
2.	46[a]: “sensing means for measuring an analog field quantity;”	177
3.	46[b]: “over sampling means, the over sampling means to over sample a signal detected by the sensing means resulting in an oversampled digital signal;”	180
4.	46[c]: “fractional delaying means, the fractional delaying means to apply a fractional time delay to the oversampled digital signal, the fractional time delay is equal to an integer number of sampling clock cycles, resulting in a delayed oversampled digital signal;”	182
5.	46[d]: “decimating means, the decimating means to receive the delayed oversampled digital signal and to low pass filter and to decimate to a lower sampling rate;”	192
6.	46[e]: “integer delaying means, the integer delaying means to apply an integer time delay to the delayed oversampled digital signal, the integer time delay is a number of lower sampling rate cycles; and”	197
7.	46[f]: “controlling means, the controlling means to adjust the fractional time delay and the integer time delay to establish a total time delay, wherein a resulting digital signal is delayed by a total time delay, wherein the total time delay is a sum of the fractional time delay and the integer time delay, and contains a digital representation of the analog field quantity without the noise introduced by the over sampling means.”	202
R.	Claim 48	208
1.	“The system of claim 46, wherein the total time delay is equal to a fraction of a baseband sampling period.”	208

S.	Claim 49	210
1.	“The system of claim 46, wherein the total time delay is greater than a baseband sampling period.”	210
T.	Claim 50	212
1.	“The system of claim 46, wherein the oversampled digital signal is digitized to create samples which are more than one bit deep.”	212
XI.	GROUND 2: CLAIMS 35 AND 40 ARE OBVIOUS BASED ON ADAMS, NGUYEN, AND NOUJAIM	217
A.	Motivation to Combine	217
B.	Reasonable Expectation of Success	220
C.	Claim 35	221
1.	“The system of claim 22, wherein the fractional time delay is greater than a baseband sampling period.”	221
D.	Claim 40	224
1.	“The method of claim 38, wherein the fractional time delay is greater than a baseband sampling period.”	224
XII.	SECONDARY CONSIDERATIONS	226
XIII.	CONCLUSION	227

I. INTRODUCTION

1. I have been retained as an expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 11,082,055 (“the ’055 patent”) (Ex.1001).¹ I have been asked to analyze the scope and content of ’055 patent relative to the state of the art at the time of the earliest application to which the ’055 patent claims priority. My analysis relates to claims 11-18, 21-22, 34-35, 38-41, 46, and 48-50 (“the challenged claims”). I have also been retained to provide analysis regarding what a person of ordinary skill in the art (“POSA”) would have understood at the time of the earliest application underlying the ’055 patent.

2. This declaration summarizes the opinions I have formed to date. I reserve the right to modify or amend my opinions, if necessary, based on further review and analysis of information that I receive subsequent to the filing of this declaration, including in response to positions taken by Solos Technology Limited (“Solos”) or its experts that I have not yet seen, including any secondary considerations evidence that Solos or its expert may consider and present.

¹ In this declaration, I refer to exhibits that I understand are to be attached to the petition for *Inter Partes* Review of the ’055 patent.

3. I am being compensated for my time at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study and analysis, the substance of my opinions, or the outcome of any proceeding involving the challenged claims. I have no financial interest in the outcome of this matter or in any litigation involving the '055 patent.

II. BACKGROUND AND QUALIFICATIONS

4. My qualifications generally are set forth in my curriculum vitae ("CV"), which is attached as Ex.1004 and also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

5. My academic and professional background is in Physics, Mechanical Engineering, Sensing, and Robotics, with a research specialization focused on microfabricated physical sensors, and I have been working in those fields since the completion of my Ph.D. more than 35 years ago. The details of my background and education and a listing of all publications I have authored in the past 40 years are provided in my CV. Below I provide a short summary of my education and experience which I believe to be most pertinent to the opinions that I express here.

6. I received a B.S. in Physics from University of Minnesota, Minneapolis in 1983, and a Ph.D. in Physics from University of California at Berkeley in 1989.

I was educated as a Physicist specializing in sensors and measurement. My Physics Ph.D. thesis involved measurements of the heat capacity of monolayers of atoms on surfaces, and relied on precision measurements of temperature and power using time-varying electrical signals, and also on the design and construction of miniature sensor components and associated electrical circuits for conditioning and conversion to digital format.

7. After completion of my Ph.D. in Physics at U.C. Berkeley in 1989, I joined the Jet Propulsion Laboratory (JPL) in Pasadena, CA, as a staff scientist, and began working on miniature sensors and instruments for small spacecraft. This work involved the use of silicon microfabrication technologies for miniaturization of the sensors, and served as my introduction to the field of micro-electromechanical systems (MEMS), or the study of very small mechanical sensors powered by electricity and used for detection of physical and chemical signals.

8. While at JPL, we developed accelerometers, uncooled infrared sensors, magnetometers, seismometers, force and displacement sensors, soil chemistry sensors, miniature structures for trapping interstellar dust, and many other miniature devices. Some of these projects led to devices that were launched with spacecraft headed for Mars and for other interplanetary missions. Much of this work involved the use of physical sensors for detection of small forces and displacements using micromechanical sensors.

9. I am presently the Richard Weiland Professor at the Department of Mechanical Engineering at Stanford University, where I have taught for the past 32 years. I am also currently the Senior Associate Dean of Engineering for Student Affairs at Stanford.

10. For almost all of these 32 years, I have taught courses on Sensors and Mechatronics at Stanford University. The “Introduction to Sensors” course is a broad overview of all sensing technologies, from thermometers, to inertial sensors, ultrasound devices, flow sensors, optical and IR sensors, chemical sensors, microphones, pressure sensors, and many others, and has included sensors based on changes in capacitance, resistance, piezoelectricity. I first taught this course at Stanford in the Spring of 1994, and I offered this course at least annually until 2016, when my duties as Senior Associate Dean made this impractical, yet have continued to offer this course periodically since, including last year.

11. The “Introduction to Mechatronics” course is a review of the mechanical, electrical and computing technologies necessary to build systems with these contents, which include everything from cars and robots to cellphones and other consumer electronics devices. In this class, we routinely use IR, LEDs, ultrasound sensors, and photosensors as a way of detecting proximity to objects in the space around miniature robots. We also use inertial sensors to detect movement, and a number of sensors, such as encoders to measure changes in position and

trajectory. I was one of the instructors for the first offering of this course in 1995, and this course has been offered at least once each year ever since, except for the pandemic year of 2021. The 2026 offering was highly successful with 80 undergraduate and graduate students from many engineering and science disciplines.

12. I am co-author of a textbook titled “Introduction to Mechatronic Design,” which broadly covers the topic of integration of mechanical, electronic and computer systems design into “smart products.” This textbook includes chapters on Microprocessors, Programming Languages, Software Design, Electronics, Sensors, Signal Conditioning, and Motors, as well as topics such as Project Management, Troubleshooting, and Synthesis.

13. My research group at Stanford has focused on the area of microsensors and microfabrication—a domain in which we design and build micromechanical sensors using silicon microfabrication technologies. The various applications for these technologies are numerous.

14. I have advised 75 Ph.D. students that have completed Ph.D. degrees and many more M.S. and B.S. students in Engineering during my time at Stanford.

15. I have published over 250 technical papers in refereed journals and conferences in the field of sensors, MEMS, and measurements. I have further presented numerous conference abstracts, posters, and talks in my field. I am a named inventor on 50 patents in my areas of work.

16. From 2020 to 2022 I served as CEO of Applaud Medical (now Avvio Medical), a startup that I co-founded in 2015. Avvio is developing improved methods for ultrasonic treatment of kidney stones, and during my time as CEO, we initiated a FDA-regulated pivotal clinical trial on our first product, concluded an Australian clinical study on our second product, and positioned the company for onboarding of an experienced CEO with resources to guide the company through all remaining trials and to a successful outcome.

17. I received the Office of the Secretary of Defense Award for Exceptional Public Service in 2010, the IEEE Sensors Council Technical Achievement Award in 2011, and was named Fellow of the ASME in 2014. I was awarded the 2018 IEEE Daniel Noble Award for Emerging Technologies. In 2022, I was elected to the National Academy of Engineering.

18. I have previously served as an expert on a patent infringement case involving the mounting and use of pressure sensors on guidewire catheters for cardiovascular procedures that included a number of sensing aspects, such as recording static and dynamic pressure signals, and compensating for electrical and mechanical errors. I have also previously served as an expert on a patent infringement case involving the design and use of miniature inertial sensors. That case involved the design and operations of micromechanical sensors, and particularly the use of inertial sensors for detection of states of movement and rest.

I have also served as an expert in a patent infringement case involving the use of sensors on athletic shoes for determining athletic performance. More recently, I served as an expert in a patent infringement case involving optical proximity sensors in smartphones. I also served as an expert witness in an IPR proceeding describing the use of microphones and signal processing circuits for processing and cancellation of noise in wearable electronic devices. My CV, Appendix A, includes a full listing of recent cases in which I have testified at deposition or trial in the preceding several years.

III. UNDERSTANDING OF GOVERNING LAW

19. I understand that statutory and judicially created standards must be considered to determine the validity of a patent claim. I am not an attorney and, consequently, will offer no opinion on the law itself. My understanding of the pertinent law is described in this section and is the result of explanations provided by counsel. I have applied this understanding in my analysis.

20. I understand that a patent claim is unpatentable if it is obvious in view of the prior art. I further understand that the frame of reference for determining whether a claim is obvious is from the perspective of a POSA at the time of the invention. I have been asked to assume that the effective priority date is August 1, 2016. I have not been asked to determine whether this date is appropriate.

21. In analyzing obviousness in light of the prior art I understand that it is important to understand the scope of the claims, the level of skill in the relevant art, the scope and content of the prior art, the differences between the prior art and the claims, and any objective indicia of non-obviousness (also called secondary considerations).

22. I understand that a patent claim is unpatentable for obviousness if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a POSA to which said subject matter pertains. I understand that obviousness may be based on one reference or a combination of references. I understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.

23. In determining the scope and content of the prior art, it is my understanding that a reference is considered appropriate (e.g., analogous) prior art if it falls within the field of the inventor's endeavor. In addition, a reference is prior art if it is reasonably pertinent to the particular problem with which the inventor was involved. A reference is reasonably pertinent if it logically would have commended itself to an inventor's attention in considering his problem. If a reference relates to the same problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

24. To assess the differences between prior art and the claimed subject matter, it is my understanding that the law requires the claimed invention to be considered as a whole. This “as a whole” assessment requires showing that one of ordinary skill in the art at the time of invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would have selected the elements from the prior art and combined them in the claimed manner.

25. It is my understanding that something is “inherent in,” and therefore taught by, the prior art, if it necessarily flows from the explicit disclosure of the prior art. I understand that the fact that a certain result or characteristic may be present in the prior art is not sufficient to establish inherency. However, if the result or characteristic is necessarily present based upon the explicit disclosure in the prior art, it is inherent in the prior art and is therefore disclosed.

26. I understand that when a patented invention is a combination of known elements, the Board must determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue by considering the teachings of prior art references, the effects of demands known to people working in the field or present in the marketplace, and the background knowledge possessed by a POSA.

27. I have been informed that the Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness

of the claimed subject matter. I understand that several of these rationales are: (1) combining prior art elements according to known methods to yield predictable results; (2) simple substitution of one known element for another to obtain predictable results; (3) use of a known technique to improve a similar device (method or product) in the same way; (4) applying a known technique to a known device (method or product) ready for improvement to yield predictable results; (5) choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and (6) some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

28. I understand that in order to prove that a claimed invention is not patentable for obviousness, a petitioner must (1) identify the differences between the claim and particular disclosures in the prior art references, singly or in combination, (2) specifically explain how the prior art references could have been combined in order to arrive at the subject matter of the claimed invention, and (3) specifically explain why a POSA would have had reasons to so combine the prior art references.

IV. MATERIALS REVIEWED

29. The opinions contained in this declaration are based on the documents I reviewed, my professional judgment, as well as my education, experience, and

knowledge regarding sensors, sensor arrays, digital signal processing, beamforming, oversampled analog-to-digital conversion, digital delay, filtering, and decimation.

30. In forming my opinions expressed in this declaration, I reviewed the following materials:

Exhibit No.	Description
1001	U.S. Patent No. 11,082,055 to Fan <i>et al.</i> (“’055 patent”)
1002	File History of U.S. Patent No. 11,082,055
1005	U.S. Patent App. Pub. No. 2013/0121504 (“Adams”)
1006	U.S. Patent App. Pub. No. 2015/0281836 (“Nguyen”)
1007	U.S. Patent App. Pub. No. 2007/0229336 (“Liu”)
1008	U.S. Patent No. 6,339,647 (“Andersen”)
1009	Reserved
1010	U.S. Patent No. 5,203,335 (“Noujaim”)
1011	R. Crochiere <i>et al.</i> , “Interpolation and Decimation of Digital Signals—A Tutorial Review,” in <i>Proc. of the IEEE</i> , vol. 69, no. 3, pp. 300-331, March 1981
1012	Tiete <i>et al.</i> , “ <i>SoundCompass: A Distributed MEMS Microphone Array-Based Sensor for Sound Source Localization</i> ,” 14 Sensors 1918 (2014), available at https://www.mdpi.com/1424-8220/14/2/1918
1013	G.W. Elko and K.P. Harney, “A history of consumer microphones: The electret condenser microphone meets micro-electro-mechanical systems,” <i>Acoustics Today</i> , vol. 5, no. 2, pp. 4–13, 2009
1014	Rudolf F. Graf, Excerpts from Modern Dictionary of Electronics Seventh Edition, 1999

Exhibit No.	Description
1015	M. Brandstein and D. Ward, Eds., <i>Microphone Arrays: Signal Processing Techniques and Applications</i> . Berlin, Germany: Springer-Verlag, 2001 (“Brandstein-Ward”)
1016	R. Kneipfer, “Sonar Beamforming – An Overview of Its History and Status,” NUWC-NL Technical Report, 10,003, 7 April 1992 (“Kneipfer”)
1017	Gannot, Sharon, and Israel Cohen. “Adaptive Beamforming and Postfiltering.” <i>Springer Handbook of Speech Processing</i> , edited by Jacob Benesty, M. Mohan Sondhi, and Yiteng Huang, Springer Berlin Heidelberg, 2008, pp. 945–978 (“Gannot-Cohen”)
1018	B. Van Veen, “Beamforming: A Versatile Approach to Spatial Filtering,” in <i>IEEE ASSP Magazine</i> , vol. 5, no. 2, pp. 4-24, April 1988) (“Van Veen”)
1019	S. R. Freeman et al., “Delta-sigma oversampled ultrasound beamformer with dynamic delays,” in <i>IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control</i> , vol. 46, no. 2, pp. 320-332, March 1999
1020	C.I.C Nilsen <i>et al.</i> , “Distortion-Free Delta-Sigma Beamforming,” in <i>IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control</i> , vol. 55, no. 8, pp. 1719-1728, 2008
1021	L. Milic <i>et al.</i> , “Multirate Filters: An Overview,” <i>APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems</i> , Singapore, 2006, pp. 912-915
1022	G. Moon <i>et al.</i> , “Design Approach for Decimation Filter for ADC Application,” in <i>Int’l J. of Eng. Trends and Techn. (IJETT)</i> , vol. 10 no. 12 (2014)
1023	J. Yu et al., A low-power multi-bit $\Sigma\Delta$ modulator in 90-nm digital CMOS without DEM, in <i>IEEE Journal of Solid-State Circuits</i> , vol. 40, no. 12, pp. 2428-2436, Dec. 2005

Exhibit No.	Description
1024	Analog Devices. ADMP521 datasheet—Ultralow Noise Microphone with Bottom Port and PDM Digital Output; Technical Report; Analog Devices: Norwood, MA, USA, 2012
1025	Reserved
1026	Analog Devices, “Seamlessly Interfacing MEMS Microphones with Blackfin Processors,” Engineer-to-Engineer Note EE-350 Rev 1, August 3, 2010
1027	J. Lewis, “Microphone array beamforming,” Analog Devices, Norwood, MA, USA, Application Note AN-1140, 2012
1028	T. Kite, “Understanding PDM digital audio,” Audio Precision, Beaverton, OR, Tech. Rep., 2012

31. I also considered any other documents and materials I refer to in this declaration.

32. My opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a POSA would have understood the state of the art, the prior art, and the claims and the specification of the '055 patent at the time of the alleged invention, which I discuss below.

33. I have been asked to assume that the time of the alleged invention of the '055 patent was no later than August 1, 2016, which I understand is the earliest claimed priority date asserted for the '055 patent.

34. Based on my experience and expertise, it is my opinion that certain references disclose or would have suggested to a POSA all the features recited in the challenged claims of the '055 patent, as I discuss in detail below.

V. PERSON OF ORDINARY SKILL IN THE ART

35. I understand that in determining the level of ordinary skill in the art, several factors are considered. Those factors may include: (i) the type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) the rapidity with which innovations are made; (iv) the sophistication of the technology; and (v) the educational level of active workers in the field. A POSA must have the capability of understanding the scientific and engineering principles applicable to the pertinent art.

36. I am familiar with the level of ordinary skill in the art regarding the '055 patent as of around August 1, 2016. Considering the '055 patent, the technology, the educational level and experience of workers in the field relating to the patent, and problems and solutions in that field, and drawing on my own experience, I believe a person of ordinary skill in the art at the time of the alleged invention (around August 1, 2016) (which I refer herein as "POSA") would have had at least a bachelor's degree in physics, electrical engineering, computer engineering, or a similar technical field, and at least two years of experience designing or implementing digital signal-processing systems for sensors or sensor

arrays. Work experience could substitute for formal education and additional formal education could substitute for work experience.

37. My opinions in this declaration regarding the '055 patent and the prior art (including the state of the art) are from the perspective of one of ordinary skill in the art as I defined above, during the relevant timeframe including the '055 patent's earliest claimed priority date of August 1, 2016.

38. I can make this assessment because, before and around August 1, 2016, I was familiar with the design and implementation of sensor systems, sensor arrays, digital signal-processing systems, analog-to-digital conversion, filtering, and related signal-processing techniques. Through my teaching, research, and work with students and engineers, I was familiar with what engineers and researchers in this field would have known and been able to implement at that time.

39. As discussed below, it is my opinion that claims 11-18, 21-22, 34-35, 38-41, 46, and 48-50 of the '055 patent are rendered obvious in view of the prior art discussed below. It is also my opinion that the claims would have been obvious from the perspective of a POSA under any reasonable definition of a POSA.

VI. TECHNICAL BACKGROUND

40. Below, I present a brief overview of certain features relating to those discussed and claimed in the '055 patent that were known to a POSA prior to and at the time of the earliest claimed priority date of the '055 patent. The features,

techniques, and concepts I describe below in this Technical Background section reflect the knowledge of state of the art that a POSA would have had prior to and at the time of the earliest claimed priority date of the '055 patent. I rely on, and incorporate as applicable (even if not expressly mentioned below), the following disclosures and opinions to support my opinions in this declaration, including those opinions relating to how the prior art discloses or would have suggested the challenged claims of the '055 patent and how and why a POSA would have been motivated to consider and combine the disclosures and suggestions from one or more prior art references as I explain below in §§X-XI.

41. The prior-art references and technical background discussed in this section provide factual support for my opinions regarding the state of the art as of the earliest claimed priority date of the '055 patent. They also provide support for my opinions regarding why a POSA would have been motivated to use, modify, and combine the teachings of the prior-art references discussed below, and why a POSA would have had a reasonable expectation of success in doing so. The references identified in this section are exemplary in nature and are not intended to limit the scope of the state of the art.

42. Claim 11 of the '055 patent recites:

A system to time delay digital signals, comprising:

- a digital sensor responsive to an analog field quantity, the digital sensor is configured to output an oversampled digital output signal at a sampling clock frequency;
- a first time delay element, the first time delay element is configured to receive as an input the oversampled digital output signal and to output a time delayed oversampled digital output signal, wherein the time delayed oversampled digital output signal is time delayed by a fractional delay, the fractional delay is equal to an integer number of sampling clock cycles times the sampling clock period;
- a filter, the filter is configured to receive as an input the time delayed oversampled digital output signal, the filter to low pass filter and to decimate to a lower sample rate the time delayed oversampled digital output signal and to output a low pass filtered decimated delayed digital output signal, wherein the lower sample rate is less than the sampling clock frequency;
- a second time delay element, the second time delay element is configured to receive, as an input, the low pass filtered decimated delayed digital output signal and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times the lower sampling rate period, the integer delay is applied to the low pass filtered decimated time delayed digital output signal; and
- a controller, the controller is configured to supply a control signal to set the fractional delay and the integer delay.

43. Claim 22 of the '055 patent recites:

A system to time delay signals, comprising:

- a sensor element, the sensor element is responsive to an analog field quantity;
- a sigma-delta modulator, the sensor element is electrically coupled to the sigma-delta modulator and is configured to produce a pulse density modulated (PDM) output signal at a sampling clock frequency responsive to the analog field quantity;

- a first time delay element, the first time delay element is electrically configured to receive the PDM output signal, and to output a delayed PDM output signal, wherein the delayed PDM output signal is delayed by a fractional time delay equal to a number of cycles of the sampling clock frequency times a period of the sampling clock;
- a decimation module, the decimation module is configured to receive as an input the delayed PDM output signal, the decimation module to low pass filter and to decimate to a lower sample rate the delayed PDM output signal and to output a low pass filtered decimated delayed PDM output signal, wherein the lower sample rate is less than the sampling clock frequency, the decimation module to convert to pulse code modulation (PCM) format;
- a second time delay element, the second time delay element is configured to receive, as an input, the low pass filtered decimated delayed PDM output signal and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times a period at the lower sampling rate, the integer delay is applied to the low pass filtered decimated delayed PDM output signal; and
- a controller, the controller is configured to supply a control signal to set the fractional delay and the integer delay.

44. Claim 38 of the '055 patent recites:

A method to delay digital signals, comprising:

sensing an analog field;

outputting an oversampled digital signal responsive to the sensing, wherein the oversampled digital signal is created at a sampling clock rate:

delaying the oversampled digital signal by a fractional time delay wherein the fractional time delay is equal to an integer number of sampling clock cycles to produce a delayed oversampled digital signal;

applying a low pass filter with decimation to the delayed oversampled digital signal to output a baseband digital signal that is delayed by the fractional time delay; and

delaying the baseband digital signal by an integer time delay, wherein the integer time delay is equal to a number of cycles at a baseband sampling rate times the baseband sampling rate period.

45. Claim 46 of the '055 patent recites:

A system to delay digital signals, comprising:

sensing means for measuring an analog field quantity;

over sampling means, the over sampling means to over sample a signal detected by the sensing means resulting in an oversampled digital signal;

fractional delaying means, the fractional delaying means to apply a fractional time delay to the oversampled digital signal, the fractional time delay is equal to an integer number of sampling clock cycles, resulting in a delayed oversampled digital signal;

decimating means, the decimating means to receive the delayed oversampled digital signal and to low pass filter and to decimate to a lower sampling rate;

integer delaying means, the integer delaying means to apply an integer time delay to the delayed oversampled digital signal, the integer time delay is a number of lower sampling rate cycles; and

controlling means, the controlling means to adjust the fractional time delay and the integer time delay to establish a total time delay, wherein a resulting digital signal is delayed by a total time delay, wherein the total time delay is a sum of the fractional time delay and the integer time delay, and contains a digital representation of the analog field quantity without the noise introduced by the over sampling means.

46. A POSA would have recognized all of these very familiar elements of these claims, which include “sigma-delta modulator”, “oversampled digital signal”,

“sensor responsive to an analog field”, “sampling clock frequency”, “time delay”, “time delayed...signal”, “integer number of sampling clock cycles”, “filter”, and “controller”, and would have appreciated that each and every term recited here had existed in the prior art since long before the earliest claimed priority date of the ’055 patent. Further, a POSA would have recognized that the combination of these terms in the claims, in which a signal is oversampled, delayed, low pass filtered and decimated, and further delayed had existed in the prior art since long before the earliest claimed priority date of the ’055 patent.

A. Beamforming Generally

47. Beamforming, which is an established signal processing technique often described as spatial filtering, generally involves processing and preparing signals from multiple sensors to be combined so as to emphasize signals from a desired location or direction. *See, e.g.,* Ex.1015 (M. Brandstein and D. Ward, Eds., *Microphone Arrays: Signal Processing Techniques and Applications*. Berlin, Germany: Springer-Verlag, 2001) (hereafter, “Brandstein-Ward”), p. 102 (“Beamforming is a technique which extracts the desired signal contaminated by interference based on directivity, i.e. spatial signal selectivity. This extraction is performed by processing the signals obtained by multiple sensors such as microphones, antennas, and sonar transducers located at different positions in the

space. **The principle of beamforming has been known for a long time.**”) (internal citations omitted) (emphasis added).

48. Beamforming has been around for nearly a century, since long before the '055 patent. For example, beamforming was used in sonar applications as far back as the 1940s when single beam beamforming systems were used in World War II (“WWII”) for detection of submarines. *See, e.g.*, Ex.1016 (R. Kneipfer, Sonar Beamforming – An Overview of Its History and Status, NUWC-NL Technical Report, 10,003, 7 April 1992), pp. 10-15 (Kneipfer, 5-10). At that time, submarines were outfitted with sonar equipment utilizing rotatable horizontal line hydrophones (e.g., sensors). During WWII, German engineers developed a way to change the time delays applied to the hydrophone outputs. *See id.*, pp. 13-14 (Kneipfer, 8-9) (discussing German development of “compensator system”), Fig. 9. This time delay capability allowed sonar operators to manually scan a beam without moving the sensor array, and accordingly to adjust the steer direction of the beamformer, thus allowing the operators to scan the beam in any direction. *Id.*, pp. 13-14. Here, all the way back to the 1940s, more than seven decades before the 2016 priority date, we see an example of a system capable of analog “delay and sum beamforming.”

49. Beamforming in other areas, such as radar, communications, imaging, geophysical and astrophysical exploration, and biomedical applications, became well known in the decades since, as well as long before the '055 patent. *See* Ex.1018

(B. Van Veen, Beamforming: A Versatile Approach to Spatial Filtering, in *IEEE ASSP Magazine*, vol. 5, no. 2, pp. 4-24, April 1988) (hereafter, “Van Veen”), p. 2, Table 1.1; *see also* Brandstein-Ward, p. 102.

50. Beamforming including microphone array processing was adopted by the speech community by the mid-1980s. *See, e.g.*, Ex.1017 (Gannot, Sharon, and Israel Cohen. “Adaptive Beamforming and Postfiltering.” *Springer Handbook of Speech Processing*, edited by Jacob Benesty, M. Mohan Sondhi, and Yiteng Huang, Springer Berlin Heidelberg, 2008, pp. 945–978) (hereafter, “Gannot-Cohen”), p. 2 (“Over the last four decades, array processing has become a well-established discipline, *see e.g.*, [47.1-14]. In the mid 1980s, array processing and beamforming methods were adopted by the speech community to deal with data received by microphone arrays.”); Van Veen, p. 2-3 (“Papers devoted to beamforming are often found in the IEEE Transactions on: *Antennas and Propagation, Acoustics, Speech, and Signal Processing, Aerospace and Electronic Systems*, and in the *Journal of the Acoustical Society of America*. There is a vast body of literature on various aspects of beamforming and we can only reference a subset in support of our discussions.”).

B. Delay-and-Sum Beamforming

51. The delay-and-sum beamformer is often considered the simplest of the beamforming structures. *See, e.g.*, Gannot-Cohen, p. 2 (“The simplest structure is the delay-and-sum beamformer, which compensates for the relative delay between

distinct microphone signals and then sums the steered signal to form a single output.”); Brandstein-Ward, p. 297 (“the most basic beamforming method, the delay-and-sum beamformer”); Ex.1006, [0002] (“The simplest filtering technique is the ubiquitous ‘delay and sum’ beamformer which sums the inputs together with an appropriate delay to obtain a desired beamshape and direction.”). The underlying principle of the delay-and-sum beamformer is to compensate for the propagation delay differences from a single source to each of the sensors in an array. Because a signal arriving from a specific angle or direction reaches different sensors at different times, the individual sensor outputs need to be relatively delayed in order to align them coherently before they are summed together.

52. Kneipfer and Van Veen both describe applications and examples of beamforming dating back many decades. The earlier implementations relied on analog signal conditioning, delay lines and other now-obsolete components to provide beamforming, but the basic concept of “delay and sum” was very well established many years before the ’055 patent. With the advent of the modern microprocessor and A/D converters, analog delay and sum beamforming became digital delay and sum beamforming.

53. For a digital implementation of a delay-and-sum beamformer, each sensor’s analog output is first converted to a digital signal by an analog-to-digital converter (ADC). The digitized sensor signals may be delayed by an integer number

of sample clock cycles and summed to produce the beamformed output. *See, e.g.*, Van Veen, pp. 3-4 (“Each sensor is assumed to have any necessary receiver electronics and an A/D converter if beamforming is performed digitally.”), Fig. 2.2; Ex.1006, [0012] (“In digital systems, the delay can only take on values that are integer multiples of the sample time ($1/F_s$).”). The delay resolution and the steering precision of the beamformer is governed by the sampling rate. *See id.* A higher sampling rate yields finer delay resolution and more precise beam steering. Overall, the adoption of A/D converters and subsequent digital implementations of delays, filters and summers began decades ago, coincident with the emergence of microprocessors and the recognition that digital delays, digital filters, and digital combiners were available, efficient, inexpensive, adaptable, and powerful, and were a perfect upgrade to beamforming. This opportunity was recognized by Van Veen in 1988, almost 30 years prior to the earliest claimed priority date of the ’055 patent, and work on modifications to digital delay and sum beamformers, including combinations and re-ordering of computational steps, has been underway throughout the time since Van Veen.

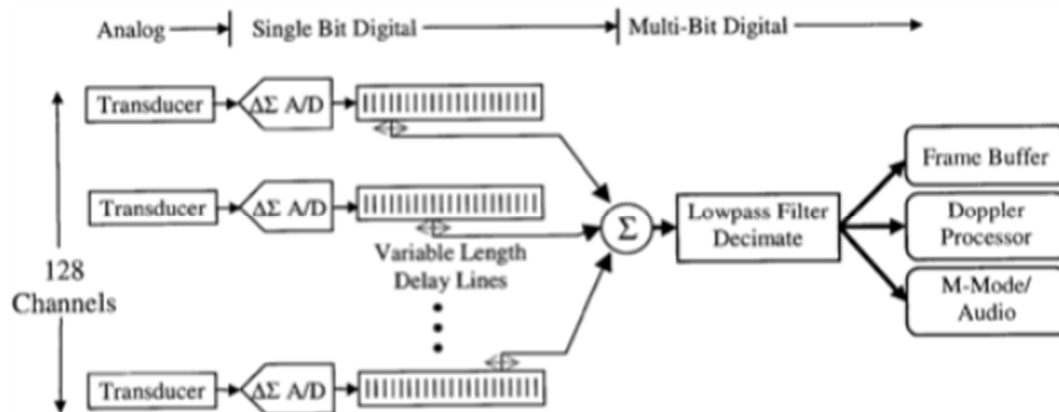
C. Beamforming Using Oversampled Digital Signals

54. Digital beamforming using oversampled analog-to-digital converters has also been around for decades, since long before the ’055 patent. *See, e.g.*, Ex.1019 (S. R. Freeman *et al.*, “Delta-sigma oversampled ultrasound beamformer

with dynamic delays,” in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 46, no. 2, pp. 320-332, March 1999) (“Freeman”), Title, p. 1 (“digital beamforming is well established”), p. 1 (“In the late 1980s, advances in analog-to-digital conversion led many manufacturers to perform more beamformer processing digitally.”), p. 2; Exs.1007-1008.

55. One particularly efficient oversampling analog-to-digital converter (ADC) that was well-known for use in digital beamforming is the delta-sigma (also called sigma-delta) modulator. *See, e.g.,* Freeman, p. 2. A delta-sigma modulator uses one or more integration stages within a feedback loop such that a two-level, single-bit quantizer output tracks the average of the analog input, thus shaping quantization noise to higher frequencies outside the signal band where it can be rejected by a subsequent low-pass filter and decimation stage. *See id.*, pp. 321-322, Fig. 1. A delta-sigma ADC may sample at a rate far exceeding the Nyquist rate of the input signal, and is often called the oversampling rate. Its high-rate single-bit output stream enables accurate and fine-tuned beamforming delays to be implemented by manipulating individual samples using a variable-length shift register, without the need for complex interpolation or baseband circuitry. *See id.*, pp. 323-325, Fig. 3; Ex.1006, [0014]-[0016], Fig. 4; *see also* Ex.1023 (J. Yu et al., A low-power multi-bit $\Sigma\Delta$ modulator in 90-nm digital CMOS without DEM, in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2428-2436, Dec. 2005), Abstract

(“Multi-bit sigma-delta modulators are widely used in analog-to-digital conversion especially in the modern deep-sub micron CMOS process.”). As explained by Freeman, “...accurate delays can be achieved simply by manipulating individual samples at the high sampling rate. The complicated basebanding or interpolate/decimate circuits may be replaced by a variable length shift register determining the delay of the signal prior to summation...” Ex.1019, p. 5.



56. Freeman illustrates this process for digital oversampling and precision delay and sum in Figure 3, shown above. Here, the signal from the “Transducer” is converted to a single-bit digital data stream using a delta-sigma oversampling A/D converter. These signal streams pass through a variable length delay line, which transfers the signal through the line at the oversampled sample rate, and selects data at taps corresponding to an integer number of sample intervals. These extracted signals are delayed by integer numbers of elements in the sample stream, which are

sampled at the oversampling rate, and therefore the resulting delays represent integer multiples of the oversampling interval.

57. The delayed single-bit outputs from each channel are summed across the array to form the beamformed signal, and a low-pass filter and decimator then converts the oversampled beamformed output to a conventional lower-rate digital signal. *See, e.g.*, Freeman, pp. 5-6, Fig. 3; Ex.1006, [0014]-[0016]. The use of delta-sigma modulators in oversampled delay-and-sum beamforming was thus well-known in the art for decades before the '055 patent. *See, e.g.*, Freeman, Fig. 3; Ex.1006, Abstract, [0002], [0014]-[0016], Fig. 4; *see also* Exs. 1007-1008.

58. So, by 1999, more than 16 years before the earliest claimed priority date of the '055 patent, there were already demonstrations of delay and sum beamforming of acoustic signals, including oversampling A/D converters, digital delays at integer multiples of the sampling interval, and combining to form a digitally beamformed signal.

59. Of course, there are many options for the sequencing of the processing of the oversampled digital signal. For example, Nilsen (Ex.1020, C.I.C Nilsen et al., “Distortion-Free Delta-Sigma Beamforming”, in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 55, no. 8, pp. 1719-1728, 2008) describes beamforming implementations with oversampling followed by filtering, delaying, decimating and then combining. As explained by Nilsen, “Down-sampling to the Nyquist rate should not take place until after the delays have been applied, to achieve maximum resolution in time and a suitably low degree of delay quantization”. Ex.1020, p.4. In this description of the Figure 3 embodiment shown



below,

digital delays are implemented on the oversampled signal by adding delays equal to an integer multiple of the oversampling interval.

60. A key point in all of this is that there were more than 80 years of intense interest in beamforming of analog signals, first in sonar and radar, then in ultrasound imaging, and more recently for operation of audio signal processing in consumer

electronic devices. Each of these application domains was deemed of critical importance at various times, and so there was substantial investment across academia, military, medical and consumer electronics sectors, and as a result, a lengthy historical record of innovation in which new ideas and concepts from all sectors were applied quickly and comprehensively. A POSA would have appreciated that the challenged claims of the '055 patent simply present well-known elements of these prior art systems, all performing well-known functions in a variety of arrangements that have all also been disclosed in the prior art. In particular, a POSA would recognize that the combination of these terms in claim 11, in which a signal is oversampled, delayed, filtered and decimated, and then delayed again, as preparation for combining with a second signal to beamform, has existed in the prior art since long before the earliest claimed priority date of the '055 patent. A POSA would also recognize that independent claims 22, 38, and 46 represent different arrangements or other minor modifications to the elements present in claim 11, and that dependent claims (12-18, 21, 34-35, 39-41, and 48-50) also represent ordinary rearrangements of the elements described above, which were all also well-known and widely used in beamforming systems long before and at the time of the earliest claimed priority date of the '055 patent. A POSA would appreciate that this subject matter was well-established and well-known long before the '055 patent.

D. Decimation Filtering

61. The use of decimation filters, including, for example, in digital beamforming and other digital processing systems, has also been around for decades, since long before the '055 patent. *See, e.g.*, Ex.1019 (S. R. Freeman *et al.*, “Delta-sigma oversampled ultrasound beamformer with dynamic delays,” in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 46, no. 2, pp. 320-332, March 1999) (“Freeman”), Fig.3 (illustrating “Lowpass filter Decimate” element in oversampled beamformer), pp. 1-2; Ex.1008 (U.S. Patent No. 6,339,647 (filed Feb. 1999)), 3:25-39, 3:57-59; Ex.1007 (U.S. Patent App. Pub. No. 2007/0229336 (filed Mar. 2007)), [0009], [0035], [0052], Fig.2; Ex.1011 (R. Crochiere *et al.*, “Interpolation and Decimation of Digital Signals—A Tutorial Review,” in *Proc. of the IEEE*, vol. 69, no. 3, pp. 300-331, March 1981), pp. 2-3 (“Sampling Rate Reduction—Decimation by an Integer Factor M...Based on well known sampling theory, in order to lower the sampling rate and to avoid aliasing at this lower rate, it is necessary to filter the signal $x(n)$ with a digital low-pass filter...”); Exs.1021-1022.

62. Decimation, as a POSA would have understood, is a process in which a higher sampling rate signal is reduced to a lower sampling rate signal. *See, e.g.*, Ex.1022 (G. Moon *et al.*, Design Approach for Decimation Filter for ADC Application, *Int’l J. of Eng. Trends and Techn. (IJETT)*, vol. 10 no. 12 (2014)) at p.

1 (“Decimation is the process of reducing the sampling rate.”); Ex.1011 (R. Crochiere at al., “Interpolation and Decimation of Digital Signals—A Tutorial Review,” in *Proc. of the IEEE*, vol. 69, no. 3, pp. 300-331, March 1981), pp. 1-2 (“The process of digitally converting the sample rate of a signal from a given rate F to a lower rate F' ...is called *decimation*.”).

63. Aside from reducing the sampling frequency to a lower rate, decimation filters are intended to pass the desired relatively low frequency in-band signal and attenuate higher-frequency components in the signal, including out-of-band quantization noise, as a POSA would have understood. *See, e.g.*, Ex.1022 (G. Moon et al., Design Approach for Decimation Filter for ADC Application, *Int’l J. of Eng. Trends and Techn. (IJETT)*, vol. 10 no. 12 (2014)), p. 1 (“The main task of a decimation filter is to remove the quantization noise away from the band of interest...”); Ex.1021 (L. Milic, Multirate Filters: An Overview, *APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, 2006, pp. 912-915), p. 1 (“The use of an appropriate filter enables one to convert a digital signal of a specified sampling rate into another signal with the desired sampling rate without significantly destroying the signal components of interest.”); *id.* (“Decimating the sampling rate by an integer factor of M means that among the input samples, ... only every M th sample are used as in the output sequence.”).

64. Decimation filters are also intended to suppress aliasing, as a POSA would have also understood. Aliasing occurs in the process of decimating (or downsampling) where non-attenuated high frequency signals can fold back into the low-frequency passband and contribute to the amplitudes of lower frequency components. *See, e.g.*, Ex.1014, pp. 3-4 (Rudolf F. Graf, Excerpts from Modern Dictionary of Electronics Seventh Edition, 1999, at 16-17) (“aliasing –...A phenomenon arising as a result of the sampling process in which high-frequency components of the original analog signal (whether information or noise) appear as lower frequencies in the sampled signal. Aliasing occurs when the sampling rate is less than twice the highest frequency existing in the original analog signal.”).

65. Given those purposes, decimation filters generally perform low-pass filtering, as a POSA would have also understood. *See, e.g.*, Ex.1021 (L. Milic, Multirate Filters: An Overview, *APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, 2006, pp. 912-915), at p. 1 (“Filtering is required to suppress aliasing when reducing the sampling rate, called as decimation.”); *id.* (“Decimating the sampling rate by an integer factor of M means that among the input samples, ... only every M th sample are used as in the output sequence. For avoiding aliasing, there is a need to use a low-pass...filter before down-sampler...”); Ex.1022 (G. Moon et al., Design Approach for Decimation Filter for ADC Application, *Int’l J. of Eng. Trends and Techn. (IJETT)*, vol. 10 no. 12

(2014)) at p. 1 (“Decimation is the process of reducing the sampling rate. In practice, this usually implies low-pass filtering a signal, then throwing away some of its samples.”); *id.* (“The main task of a decimation filter is to remove the quantization noise away from the band of interest and avoid aliasing of high frequency components down to low frequency region or within the signal bandwidth.”); Ex.1011 (R. Crochiere et al., “Interpolation and Decimation of Digital Signals—A Tutorial Review,” in *Proc. of the IEEE*, vol. 69, no. 3, pp. 300-331, March 1981), p. 3 (“Based on well known sampling theory, in order to lower the sampling rate and to avoid aliasing at this lower rate, it is necessary to filter the signal $x(n)$ with a digital low-pass filter...”).

E. Micro-Electro-Mechanical Systems (MEMS) Sensors

66. The use of MEMS microphone sensors dates back several decades, since long before the '055 patent, and also commercialized well before the '055 patent. *See, e.g.*, Ex.1013, (G.W. Elko and K.P. Harney, “A history of consumer microphones: The electret condenser microphone meets micro-electro-mechanical systems,” *Acoustics Today*, vol. 5, no. 2, pp. 4–13, 2009), pp. 6-8 (discussing work on MEMS microphone sensors in the 1980s and 1990s, and “commercialization of MEMS microphones...in 2003”); *id.*, p. 8 (describing that “Knowles has shipped in excess of 300 million MEMS microphones into general consumer applications including cell phones, digital cameras and Bluetooth headsets”); Ex.1012

(Soundcompass), p. 9 (“The SoundCompass has a planar microphone array geometry consisting of 52 digital MEMS microphones arranged in four concentric rings (Figure 5). This array is capable of performing spatial sampling of the surrounding sound field by using beamforming techniques.”); Ex.1024 (Analog Devices. ADMP521 datasheet—Ultralow Noise Microphone with Bottom Port and PDM Digital Output; Technical Report; Analog Devices: Norwood, MA, USA, 2012); Ex.1027 (J. Lewis, “Microphone array beamforming,” Analog Devices, Norwood, MA, USA, Application Note AN-1140, 2012), pp. 1, 7 (discussing “Analog Devices, Inc., MEMS microphones”); Ex.1026 (Analog Devices, “Seamlessly Interfacing MEMS Microphones with Blackfin Processors,” Engineer-to-Engineer Note EE-350 Rev 1, August 3, 2010), p. 1 (“This EE-Note describes a novel way of interfacing ADI’s industry-leading high-performance ADMP421 MEMS microphone to the Blackfin processor family.”).

67. To illustrate further, in the SoundCompass publication, the use of “digital MEMS microphones—**off-the-shelf components commonly found in mobile phones**” was disclosed. *See, e.g.*, Ex.1012 (Soundcompass), p. 6 (“The digital MEMS microphones—**off-the-shelf components commonly found in mobile phones**—used on the SoundCompass have two main advantages: high value (low-cost/high-quality) and a small package size. These microphones integrate an acoustic transducer, a preamplifier and a sigma-delta converter into a single chip.”)

(emphasis added). The SoundCompass publication discloses that the specific digital microphones used were the "[m]icrophones designed by Analog Devices (part number: ADMP521)." *Id.*, p. 7 ("Microphones designed by Analog Devices (part number: ADMP521) were used in the SoundCompass prototype, because of their fairly good wide-band frequency response from 100 Hz up to 16 kHz and their omnidirectional polar response [18]"), p. 31 ("18. Analog Devices. ADMP521 datasheet—Ultralow Noise Microphone with Bottom Port and PDM Digital Output; Technical Report; Analog Devices: Norwood, MA, USA, 2012."). The ADMP521 is an example of a commercial digital microphone utilizing a MEMS sensor available well before the '055 patent. *See id.*; Ex.1024 (Analog Devices. ADMP521 datasheet—Ultralow Noise Microphone with Bottom Port and PDM Digital Output; Technical Report; Analog Devices: Norwood, MA, USA, 2012).

68. The ADMP521 digital microphone not only included a MEMS microphone sensor, but also included a follow-on sigma-delta modulator ADC. *Id.*, p. 1 ("The ADMP521 consists of a MEMS microphone element and impedance converter amplifier followed by a fourth-order sigma-delta (Σ - Δ) modulator. The digital interface allows for the pulse density modulated (PDM) output of two microphones to be time-multiplexed on a single data line using a single clock.").

VII. THE '055 PATENT

A. Description

69. The '055 patent is titled “Beamforming Using Fractional Time Delay in Digitally Oversampled Sensor Systems, Apparatuses, and Methods.” Ex.1001, Title. It cites a number of related patent applications for priority, with the earliest claimed priority date being August 1, 2016.

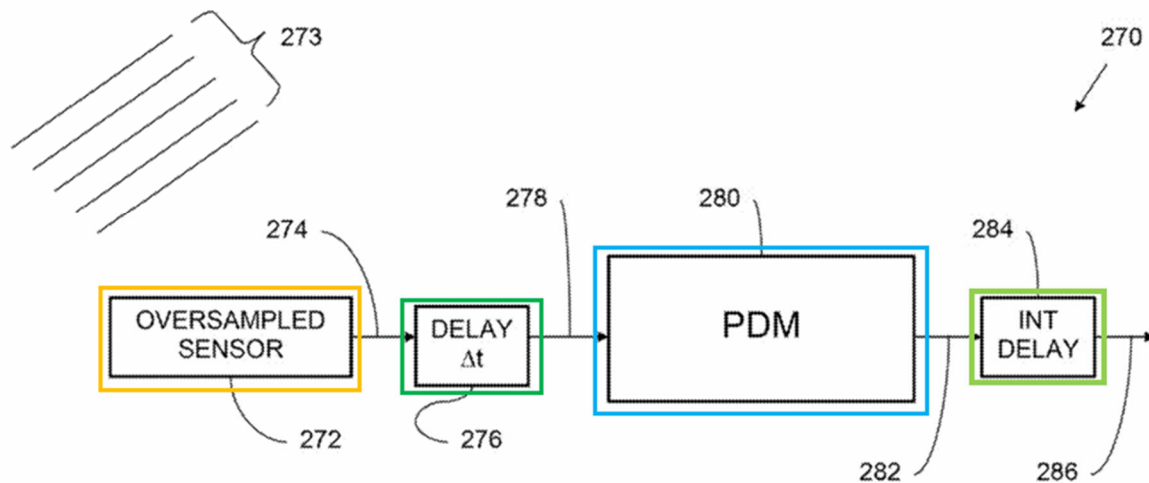
70. The '055 patent states in its background: “Field quantities which exist in the natural world are generally analog signals which have continuously varying amplitude as a function of time. Examples of these field quantities are sound pressure, vibration, light, etc. Measurement of a field quantity is accomplished with an analog sensor or a digital sensor. Digital electronics work with digital signals. Interfacing analog signals with digital electronics presents a technical problem for which a technical solution using technical means is needed.” Ex.1001, 1:30-39. This statement of the background overlooks that the “technical problem” of interfacing analog and digital electronics has existed since the advent of digital electronics more than 50 years ago, and further overlooks 40 years of the development of technical solutions using technical means.

71. The '055 patent's specification describes applying a time delay to an oversampled digital signal from a sensor, such as a digital microphone, before or within the signal-processing path that later performs low-pass filtering and

decimation. *Id.*, 2:43-48, 3:1-31, 3:55-65. The patent explains that, when delay is applied in the oversampled domain, the delay is represented by an integer number of high-rate sampling-clock cycles. *Id.*, 3:28-31, 4:50-65, 13:42-58.

72. Figure 2C of the '055 patent illustrates an exemplary system 270 to time delay digital signals. Ex.1001, 5:56-7:19. This system includes a digital sensor 272 (orange), which responds to an acoustic field 273 and outputs an oversampled digital signal 274; a first delay element 276 (dark green), which applies a fractional time delay to the oversampled digital signal to output a time delayed oversampled digital signal; a module 280 (blue) that decimates and low pass filters the time delayed oversampled digital signal to output a baseband digital signal 282; and a second delay element 284 (light green), which applies an integer time delay to the baseband signal 282. *Id.* As discussed above and below, every single element of this exemplary system, and complete instances of this exemplary system as well as other exemplary systems presented and covered by the claims of the '055 patent, all existed in the art for many years prior to the earliest claimed priority date of the '055 patent.

FIGURE 2C



Ex.1001, Fig.2C (annotated in color).

B. The Prosecution History

73. I reviewed the prosecution history of the '055 patent (Ex.1002). From that review, it is my understanding that during prosecution before the U.S. Patent and Trademark Office (Office), the Examiner allowed the challenged claims without rejecting them over prior art. Ex.1002, 211-217, 58, 53-55. The only rejections were non-prior art issues, namely nonstatutory double patenting and lack of antecedent basis. *Id.*, 212-216.

VIII. OVERVIEW OF THE PRIOR ART

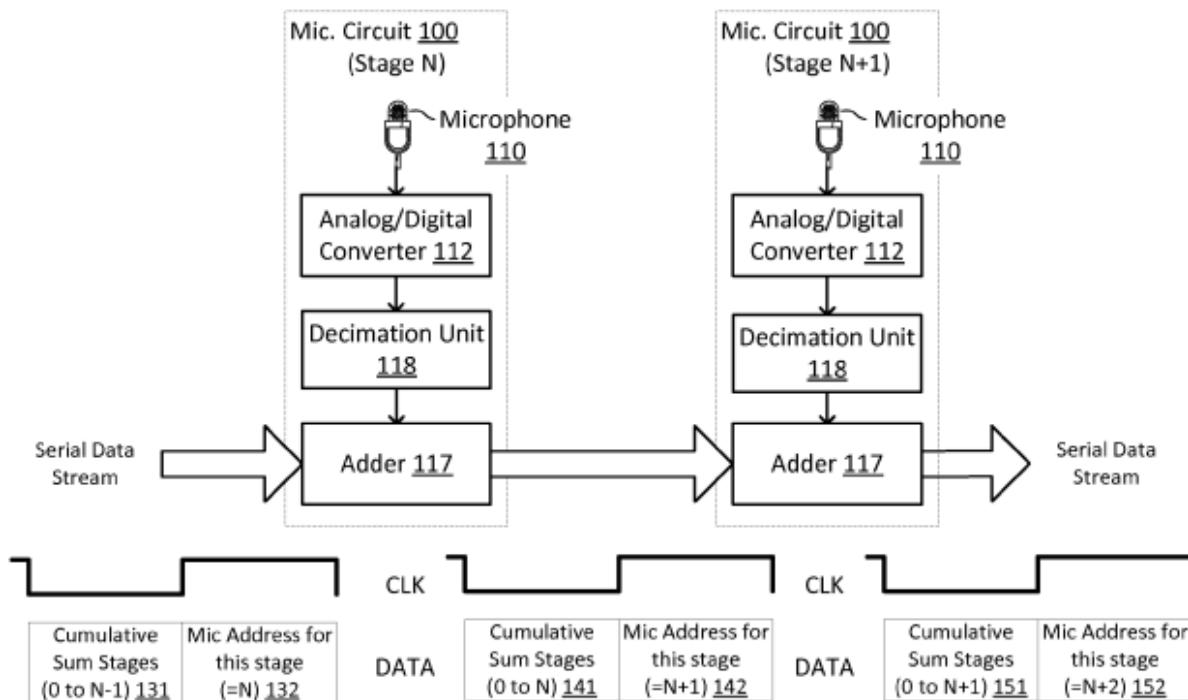
A. Adams

74. Adams (U.S. Patent Application Publication No. 2013/0121504) published May 16, 2013, which is before the earliest claimed priority date of the '055 patent (August 1, 2016). Adams is a patent publication of the company, Analog

Devices, and identifies Robert Adams as the first named inventor. Ex.1005, Face. Adams explains the context of its disclosure in the field of “beamforming” including where “[m]icrophone arrays have been used to improve fidelity and reduce effects of ambient noise.” Ex.1005, [0002]-[0003]. In that context, Adams identifies a drawback of “signal processing devices, which required each of the microphones to be individually wired to separate inputs of the...device.” *Id.*, [0003]. According to Adams, “[i]ncorporating these extra wires requires additional expense and space in the device” and “may affect the overall reliability of the system.” *Id.* Adams identifies a “need for a microphone array supporting a large number of microphones with a limited number of connecting wires.” *Id.*, [0003].

75. Adams thereafter discloses a system divided in stages (e.g., Stages N and N+1) with each stage providing for both fine and coarse time delaying of a digital microphone signal. E.g., Ex.1005, [0016], [0023]-[0029], Figs.1-6.

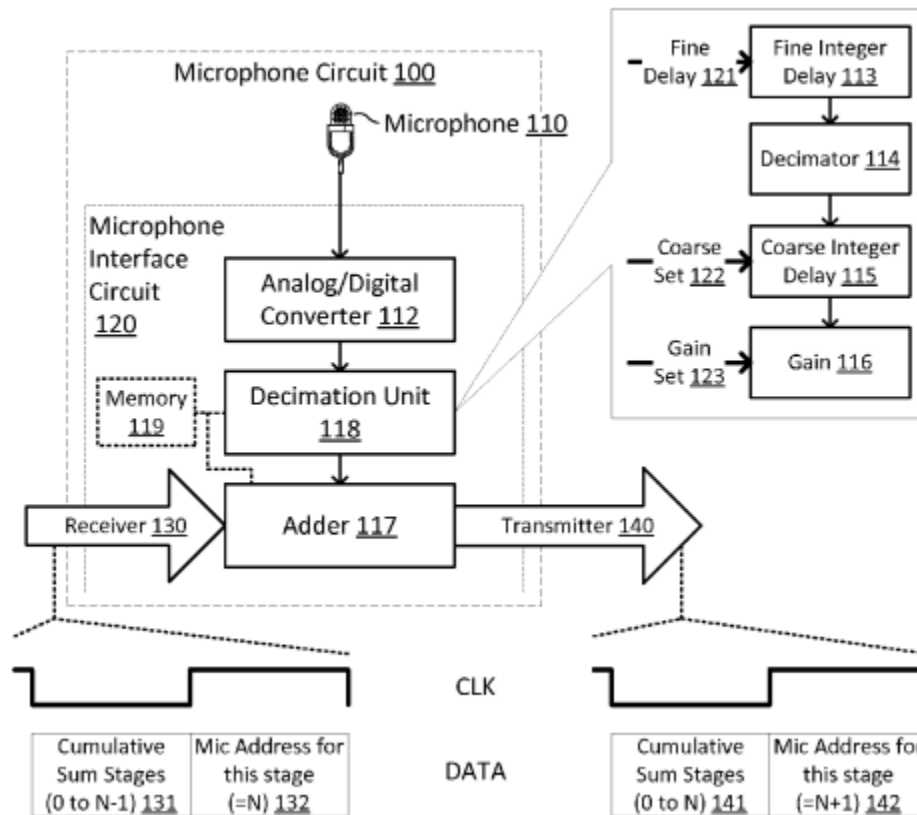
FIG. 2



Ex.1005, Fig.2.

76. Each stage (e.g., Stage N including Mic. Circuit 100) comprises a microphone, an analog-to-digital converter (ADC), multiple time delay elements, a decimating filter located between time delay elements, and a controller configured to supply control signals to set the delays of the delay elements.

FIG. 1



Ex.1005, Fig.1.

B. Nguyen

77. Nguyen (U.S. Patent Application Publication No. 2015/0281836) published October 1, 2015, which is before the earliest claimed priority date of the '055 patent (August 1, 2016). Like Adams, Nguyen is also an Analog Devices patent publication identifying Robert Adams as an inventor. Ex.1006, Face. Nguyen was filed approximately two years after Adams was filed.

78. In my opinion, Nguyen, is similar to Adams, and discloses a system for signal processing comprising a digital microphone, an analog-to-digital converter (ADC), and a decimating filter. E.g., Ex.1006, [0027], [0030], [0035], Figs.1, 3.

79. Nguyen teaches that its decimating filter is low-pass to suppress higher frequency noise components. Ex.1006, [0035], [0037].

80. Nguyen further teaches that its digital microphone includes a MEMS sensor, which was “[c]ommonly used” by that time, “shaped and sized for portable audio devices such as smartphones, tablets and mobile phones etc.,” and “integra[ble] into a miniature MEMS microphone housing or package.” Ex.1006, [0006]-[0007], [0028].

81. Nguyen’s MEMS sensor is followed by and integrated with “sigma-delta modulators preferably operate[d] at an oversampled sampling frequency.” Ex.1006, [0012] [0030]. Nguyen further discloses that its “sigma-delta modulators may comprise a single-bit quantizer or a multi-bit quantizer.” *Id.*, [0012].

82. Nguyen’s use of this sensor and follow on sigma-delta modulator and such a structure’s accompanying benefits are consistent with Nguyen’s recognition that it is “advantageous to integrate multiple functions in a single transducer unit such as a microphone.” *Id.*, [0002] (discussing benefits of “reduce[d] power consumption of active circuitry, reduce[d] space consumption and lower assembly costs”).

C. Noujaim

83. Noujaim issued April 20, 1993, before the earliest claimed priority date of the '055 patent. Noujaim described ultrasonic beamforming in which sigma-delta modulators separately digitize transducer-element echo signals into oversampled one-bit digital representations. The oversampled one-bit representations are delayed as required for beam steering and focusing, summed together, and then provided to a decimator filter that reduces the sample rate of the digitized receive beam. Ex.1010, Abstract, 8:65-10:3, Fig.5.

84. Regarding delay, Noujaim discloses a shift register-based delay unit that operates on oversampled signals prior to decimation, with the desired delay selected based on the number of shift-register stages through which the signal passes before being output. Ex.1010, Abstract, 8:65-9:42, 10:22-40.

D. Analogous Art

85. In my opinion, the asserted prior-art references discussed in this declaration are analogous art to the '055 patent. Adams, Nguyen, and Noujaim are in the same field as the '055 patent because they concern digital signal processing for sampled sensor systems, including, e.g., systems using oversampled ADC outputs, delay, filtering, and decimation. They also are reasonably pertinent to problems addressed by the '055 patent, including implementing delay-based beamforming in digital sensor systems.

86. We see throughout these disclosures a variety of systems which produce an oversampled and delayed digital signal that has a time delay equal to an integer multiple of the sampling rate intervals and digital filters which include decimation and low-pass filters. The oversampled and delayed signals are thus prepared for combination with other digital signals to form a beamformed digital signal. A POSA would appreciate that this subject matter was well-established and well-known long before the '055 patent.

IX. CLAIM CONSTRUCTION

A. General Understanding and Approach

87. It is my understanding that in determining whether a patent claim is obvious in view of the prior art, the Patent and Trademark Office construes the claim by giving the claim terms their plain and ordinary meaning, as they would have been understood by a POSA at the time of the invention in view of the intrinsic record (patent claims, patent specification, and file history). For the purposes of this review, and to the extent necessary, I have interpreted each claim term in accordance with its plain and ordinary meaning as it would have been understood by a POSA, in view of the intrinsic record.

88. I understand that a patent and its prosecution history are considered “intrinsic evidence” and are the most important sources for interpreting claim language in a patent. I also understand that in reading the claim, I must not import

limitations from the specification into the claim terms; in other words, I must not narrow the scope of the claim terms by implicitly adding disclosed limitations that have no express basis in the claims. The prosecution history of related patents and applications can also be relevant.

89. I understand that sources extrinsic to a patent and its prosecution history (such as dictionary definitions and technical publications) may also be used to help interpret the claim language, but that such extrinsic sources cannot be used to contradict the unambiguous meaning of the claim language that is evident from the intrinsic evidence.

90. Unless expressly stated herein, I have applied the plain and ordinary meaning of the claim terms, which I understand is the meaning that a POSA would have given to terms at the time of the claimed invention based on a review of the intrinsic evidence.

B. Means-Plus-Function Terms of Claim 46

91. I have been asked to provide my interpretation of the following terms recited in claim 46 of the '055 patent:

- “sensing means for measuring an analog field quantity;”
- “over sampling means, the over sampling means to over sample a signal detected by the sensing means resulting in an oversampled digital signal;”
- “fractional delaying means, the fractional delaying means to apply a fractional time delay to the oversampled digital signal, the fractional

time delay is equal to an integer number of sampling clock cycles, resulting in a delayed oversampled digital signal;”

- “decimating means, the decimating means to receive the delayed oversampled digital signal and to low pass filter and to decimate to a lower sampling rate;”
- “integer delaying means, the integer delaying means to apply an integer time delay to the delayed oversampled digital signal, the integer time delay is a number of lower sampling rate cycles; and”
- “controlling means, the controlling means to adjust the fractional time delay and the integer time delay to establish a total time delay, wherein a resulting digital signal is delayed by a total time delay, wherein the total time delay is a sum of the fractional time delay and the integer time delay, and contains a digital representation of the analog field quantity without the noise introduced by the over sampling means.”

92. I understand that these limitations are written in means-plus-function format. I have been informed that construing a means-plus function claim term is a two-step process. First, the claimed function is identified. Second, an identification is made of the structure disclosed in the patent’s specification corresponding to the claimed function.

93. I have been informed that structure disclosed in the patent specification qualifies as “corresponding structure” if the specification clearly links or associates that structure to the function recited in the claim.

1. “sensing means...”

94. The “sensing means” term has a recited function “for measuring an analog field quantity.”

95. Regarding structure, the '055 patent specification discloses a digital sensor, such as a digital microphone, that is responsive to an analog field quantity. For example, the specification discloses “a digital sensor responsive to an analog field quantity.”

96. The specification discloses such a “digital sensor” as responsive to an analog field quantity. For example:

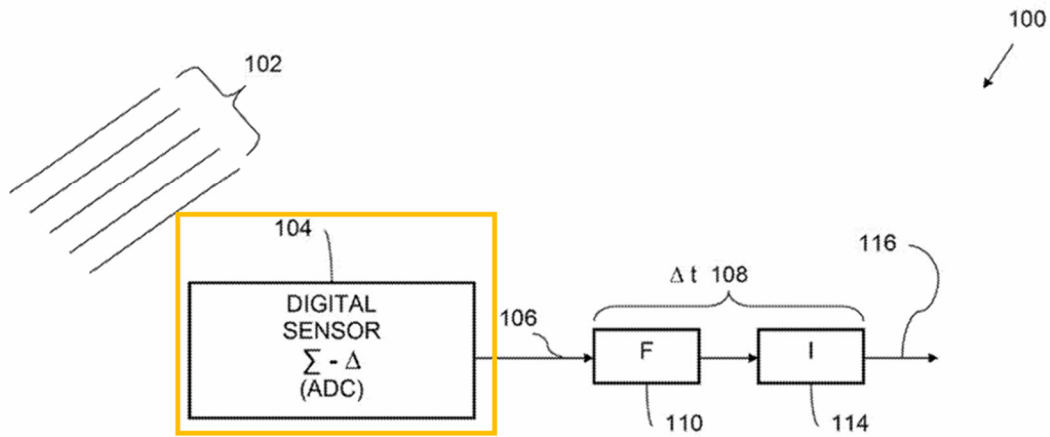
“Field quantities which exist in the natural world are generally analog signals which have continuously varying amplitude as a function of time. Examples of these field quantities are sound pressure, vibration, light, etc. **Measurement of a field quantity is accomplished with an analog sensor or a digital sensor. Digital electronics work with digital signals. Interfacing analog signals with digital electronics presents a technical problem for which a technical solution using a technical means is needed.**”

Ex.1001, 1:30-38 (emphasis added).

“With reference to FIG. 1, **an analog field quantity 102 is sensed by a digital sensor system 104.** As represented in FIG. 1 at 104, the digital sensor system includes a digital sensor which is typically configured to oversample the analog signal 102.”

Ex.1001, 2:50-54 (emphasis added).

FIGURE 1

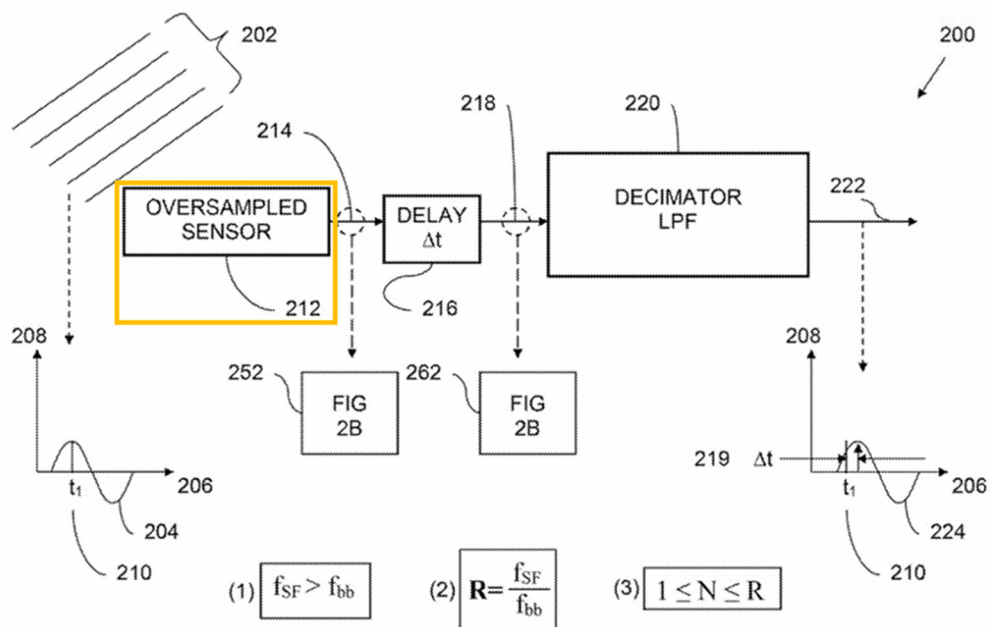


Id., Fig.1 (annotated).

“In operation, an analog field quantity 202 is incident upon a digital sensor 212. The digital sensor 212 converts the incident analog field to an oversampled digital output signal at 214 which preserves phase information of the signal within the bit stream of the signal 214.”

Id., 3:10-15 (emphasis added).

FIGURE 2A



Id., Fig.2A (annotated).

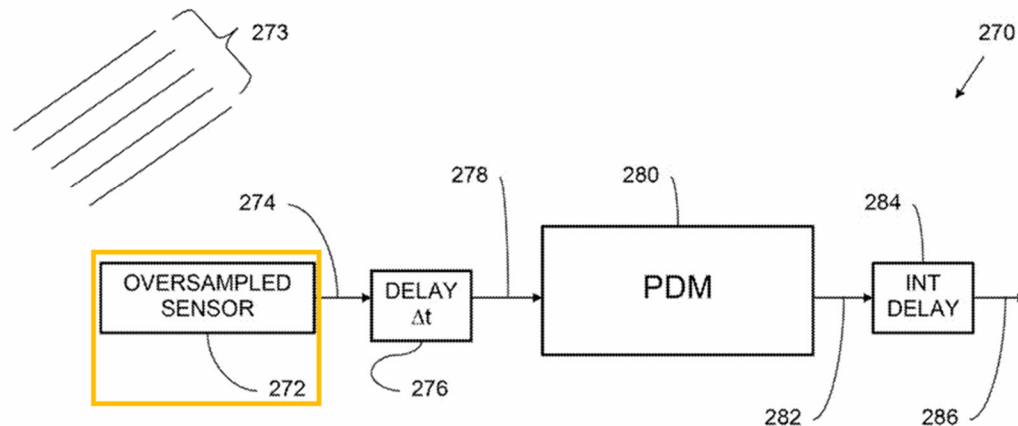
“With reference to FIG. 2C, a digital microphone is indicated at 272. **Digital microphone 272 responds to an acoustic field 273.** The digital microphone 272 can take the form of an electret capsule microphone or it can be made using microelectromechanical systems (MEMS) technology as a component on an integrated circuit. In some embodiments, MEMS digital microphones are made as a structure on an integrated circuit which uses a membrane that forms a capacitor with a base plate. Sound waves cause a vibration of the membrane which causes variations in capacitance which are sensed, amplified, and processed in the integrated circuit.

The MEMS digital microphones can be configured with a sigma-delta modulator which produces an oversampled digital output of the analog signal sensed by the microphone. A digital MEMS microphone configured with a sigma-delta modulator is supplied with power and a sampling clock signal. In various embodiments, the digital microphone outputs a pulse density modulated (PDM) oversampled signal. A clock signal can be provided as an external clock signal from a digital data processing system or the sampling clock signal can be provided locally as part of the integrated circuit package that houses the digital microphone. Digital microphones using MEMS technology and sigma-delta modulators for analog-to-digital conversion can be designed to operate at a variety of sampling clock frequencies. Common sampling clock frequencies are in the range of 1 MHz to 5 MHz. The sampling clock frequencies listed here are given merely for illustration and do not limit embodiments of the invention.”

Id., 5:59-6:21 (emphasis added). From this description in the '055 patent, a POSA would have understood that the digital sensor comprises at least: a transducer element (such as an electret or MEMS element, for example) which converts the analog acoustic field into an analog electrical signal, followed by analog signal processing circuits such as an amplifier, and an ADC (such as a

sigma-delta modulator, for example) capable of producing an oversampled digital signal representative of the input analog acoustic field.

FIGURE 2C



Id., Fig.2C.

“An analog field quantity e.g., an acoustic field **302** is sensed by a digital microphone **304**.”

Id., 7:24-25.

97. The '055 patent specification discloses that the element of the digital sensor that senses and accordingly measures the analog field is a microphone element and can take the form of an electret capsule microphone or be made using MEMS technology, for example. *See* Ex.1001, 5:60-6:3:

“Digital microphone **272** responds to an acoustic field **273**. The **digital microphone 272 can take the form of an electret capsule microphone or it can be made using microelectromechanical systems (MEMS) technology as a component on an integrated circuit.** In some embodiments, MEMS digital microphones are made as a structure on an integrated circuit which uses a membrane that forms a capacitor with a base plate. **Sound waves cause a vibration of the**

membrane which causes variations in capacitance which are sensed, amplified, and processed in the integrated circuit.”

98. From the disclosure of the '055 patent specification, a POSA would have recognized the corresponding structure of the “sensing means” to be a digital sensor element, such as a microphone (e.g., an electret capsule or MEMS microphone element).

2. “over sampling means...”

99. The “over sampling means” term has a recited function “to over sample a signal detected by the sensing means resulting in an oversampled digital signal.”

100. Regarding structure, the '055 patent specification discloses that the digital sensor “is typically configured to oversample the analog signal” and “output an oversampled digital output signal at a sampling clock frequency.” *See*:

“As represented in FIG. 1 at 104, the digital sensor system includes a digital sensor which is typically configured to oversample the analog signal 102.”

Ex.1001, 2:51-54 (emphasis added).

“The digital sensor is configured to output an oversampled digital output signal at a sampling clock frequency”

Id., Abstract.

“The digital sensor 212 converts the incident analog field to an oversampled digital output signal at 214 which preserves phase information of the signal within the bit stream of the signal 214. In various embodiments, the oversampled signal 214 is provided as a pulse density modulated (PDM) signal. In other embodiments, other digitizing methodologies can be employed to digitize the oversampled

signal. **The oversampling which occurs in the oversampled sensor 212** occurs at a sampling clock frequency. The sampling clock signal is often provided externally by the data processing system or a dedicated digital signal processing system (DSP) clock which is divided down to the desired sampling clock frequency used to sample the digital sensor 212. In other embodiments, the sampling clock can be provided locally even on the same integrated circuit with a digital sensor.”

Id., 3:11-26 (emphasis added).

“Here the digital microphone 272 is driven by a sampling clock frequency f_{SF} the baseband sampling frequency is given by f , therefore from equation (1) $f_{SF} > f_{bb}$. The ratio of the sampling clock frequency to the baseband sampling frequency is given by equation (2) as $R = f_{SF}/f_{bb}$. Equation (3) indicates that a fractional delay can be selected based on a number of sampling clock cycles N from the range $1 \leq N \leq R$, and the time delay which is applied by delay element 276 is given by equation (4) as: $\Delta t = N * \tau_{SF}$. Where τ_{SF} is the period of the sampling clock. In various embodiments, the PDM receiver module 280 is constructed with a sequence of stages as explained below in conjunction with the figures that follow.”

Id., 7:7-19 (emphasis added).

101. The '055 patent specification also discloses that the oversampling in the sensor utilizes an analog-to-digital converter, such as a sigma-delta modulator.

For example:

“ Systems and methods are described for applying a time delay to an oversampled digital signal. In various embodiments the time delay is applied in various locations within the oversampled domain of the digital signal during signal processing in an analog-to-digital converter (ADC).”

Id., 2:44-48 (emphasis added).

“The following description and the associated figures are set in the context of a digital microphone however; the description is applicable to sensors other than digital microphones and is generally applicable to oversampled sensors used **during analog-to-digital conversion (ADC) where a time delay is introduced in the oversampled digital domain.**”

Id., 5:49-55 (emphasis added).

“Referring back to FIG. 2A, as described above the sampling clock frequency is represented by a variable f_{SF} ; the baseband sampling frequency is given by the variable f_{bb} . Equation (1) is the requirement for the oversampling condition where $f_{SF} > f_{bb}$. The ratio of the sampling clock frequency to the baseband sampling frequency is given by equation (2) as $R = f_{SF}/f_{bb}$. **In analog-to-digital conversion methodologies** that are one-bit deep, R will represent the number of subintervals that a baseband sampling period can be divided into for the purpose of applying a “fractional” time delay to the oversampled digital signal **214**. Pulse density modulation (PDM) is such a digital conversion methodology that is one-bit deep where the sign is carried by the bit value where a “1” corresponds to a pulse of plus polarity (+A) and a “0” corresponds with a pulse of negative polarity (−A). Equation (3) indicates that a fractional delay can be selected based on a number of sampling clock cycles N from the range $1 \leq N \leq R$, and the time delay which is applied by delay element **216** is given by equation (4) as: $\Delta t = N * \tau_{SF}$. Where τ_{SF} is the period of the sampling clock. Where as described above, “fractional delay” refers to a fraction of a baseband sampling rate cycle.

Note that when other analog-to-digital digitization methodologies are used in the digital sensor **212** the resulting digital bit stream can be other than one-bit deep.”

Id., 4:49-5:6 (emphasis added).

“In the oversampled systems described above, in various non-limiting embodiments, the variable R has been used to represent the ratio of the sampling clock frequency (at the digital microphone) to the sampling rate at baseband. In the non-limiting example of FIG. 3, with f_{SF} equal

to 2.048 MHz and f_{bb} equal to 16 kHz, then from equation 2 in FIG. 2A, $R=f_{SF}/f_{bb}=128$. From equation (10) in FIG. 11A in this non-limiting example a minimum fraction that R represents with respect to the integer sampling rate is $1/128$. Other fractional time delay values are achieved by the techniques described herein, such as by time delaying for additional clock cycles at f_{SF} or additional intermediate sampling rate cycles or by changing the sampling clock frequency that is used to drive the ADC in the digital sensor.

FIG. 12 illustrates, generally at **1200**, a process to impart a time delay to an oversampled system, according to embodiments of the invention. With reference to FIG. 12, a process begins at a block **1202**. At a block **1204** a relationship is established between sampling clock cycles and the digital representation of the analog signal produced by the digitization methodology employed **in an analog-to-digital converter (ADC) process**. In some instances, this is a one-bit deep process such as with Pulse Density Modulation (PDM) described above. In other embodiments, the process is other than one-bit deep but is then multiple bits deep. At a block **1206** a number of clock cycles needed for a given time delay is computed taking into consideration the bit depth of the encoding methodology used in the ADC.”

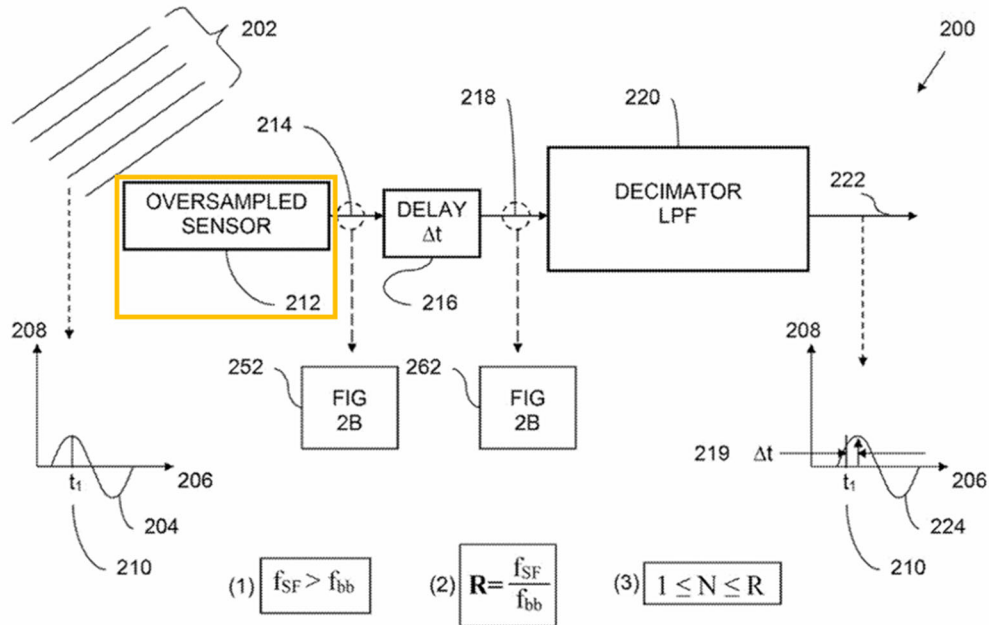
Id., 14:45-15:5 (emphasis added).

“FIG. 2A illustrates, generally at 200, time delaying **an oversampled signal within an analog-to-digital converter (ADC) system**, according to embodiments of the invention. With reference to FIG. 2A, a time delay is inserted in **the oversampled domain of the ADC.**”

Id., 3:3-7 (emphasis added).

102. The '055 patent specification also discloses a sigma-delta modulator as an example of an exemplary analog-to-digital converter (ADC). *See*:

FIGURE 2A



Id., Fig.2A (annotated).

“In various embodiments, **the oversampling performed in the digital sensor 212 is accomplished with a sigma-delta modulator in an analog-to-digital conversion (ADC) process** which outputs at 214 a one-bit deep pulse density modulated (PDM) oversampled digital signal representing the digitization of the analog signal 256 (FIG. 2B).”

Id., 4:23-28 (emphasis added).

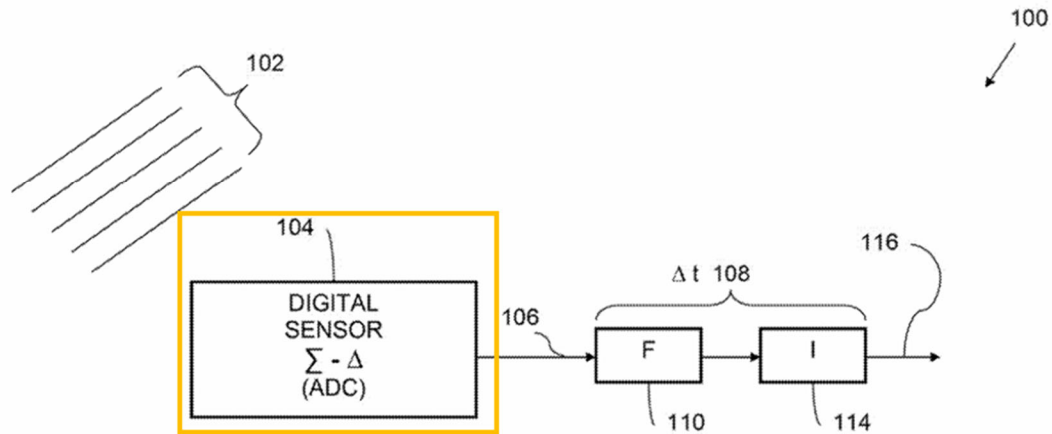
“The MEMS digital microphones can be configured with **a sigma-delta modulator which produces an oversampled digital output** of the analog signal sensed by the microphone.”

Id., 6:4-9 (emphasis added).

“The digital microphone **304** employs a one-bit **sigma-delta modulation to perform analog-to-digital conversion (ADC)**. In one non-limiting embodiment, the digital microphone **304** is driven with a 2.048 MHz sampling clock frequency to output an oversampled digital output signal at **306**.”

Id., 7:25-30 (emphasis added).

FIGURE 1



Id., Fig.1 (annotated).

103. From the disclosure of the '055 patent specification, a POSA would have recognized the corresponding structure of the “over sampling means” to be a digital sensor analog-to-digital converter (ADC) element, such as a sigma-delta modulator.

3. “fractional delaying means...”

104. The “fractional delaying means” term has a recited function “to apply a fractional time delay to the oversampled digital signal, the fractional time delay is equal to an integer number of sampling clock cycles, resulting in a delayed oversampled digital signal.”

105. Regarding structure, the '055 patent specification discloses that the fractional time delay equal to an integer number of sampling clock cycles, and is provided by a buffer, delay line, or delay circuit. For example:

“The time delay 108 can be of various lengths and is sometimes expressed in two parts, i.e., an integer part and a fractional part. A first part 114 can be referred to as an integer delay where ‘integer’ refers to an integer number of baseband sampling rate cycles. A second part 110 can be referred to as a fractional delay where ‘fraction’ refers to a fraction of the baseband sampling rate period. A time delayed digital version of the digital signal 106 is output at 116.”

Id., 2:60-66 (emphasis added).

“The oversampled digital signal 214 is input into a delay element 216 and is output at 218 after a time delay ‘ Δt ’ is imparted to the oversampled digital signal. The time delay Δt imparted to the oversampled digital signal 214 at delay element 216 is represented by an integer number of sampling clock cycles. When it is desirable to impart a “fractional delay” at delay element 216, then the maximum number of sampling clock cycles that would be imparted at 216 is equal to the ratio of sampling clock frequency divided by the baseband sampling rate, indicated herein by the variable ‘R.’”

Id., 3:27-37 (emphasis added).

“The oversampled digital output 274 is input to a delay element 276 as described previously. The delay element 276 applies a time delay to the oversampled digital signal and outputs a time delayed oversampled digital signal at 278.”

Id., 6:40-43 (emphasis added).

“As described above, the time delay element 276 can apply a fractional time delay to the oversampled digital signal 274.”

Id., 6:61-62 (emphasis added).

“In various embodiments, **the delay element 216 is implemented as a buffer**, which can be programmable. In other embodiments, **the delay element is implemented with a delay line**; the delay line can be a programmable delay line. In yet other embodiments, **the delay element is implemented with a circuit constructed to provide a delay** and the delay can be programmable.”

Id., 3:42-50 (emphasis added).

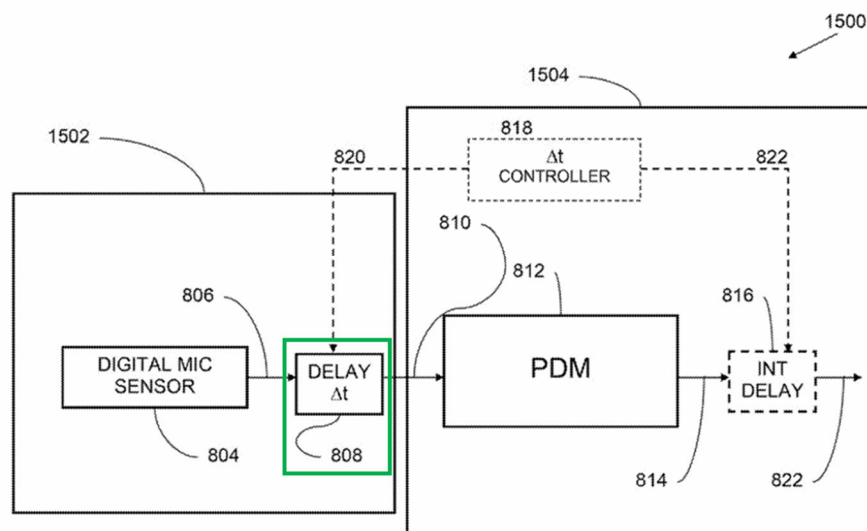
“FIG. 15A-15B illustrates **integrated circuit dies in which embodiments of the invention may be implemented.**”

Id., 2:26-27 (emphasis added).

“With reference to 1500, **a first integrated circuit die 1502 includes the digital sensor 804 and time delay element 808**; a second integrated circuit die 1504 includes one or more of the PDM receiver module 812, time delay controller 818, and time delay element 816.”

Id., 16:45-50 (emphasis added).

FIGURE 15A

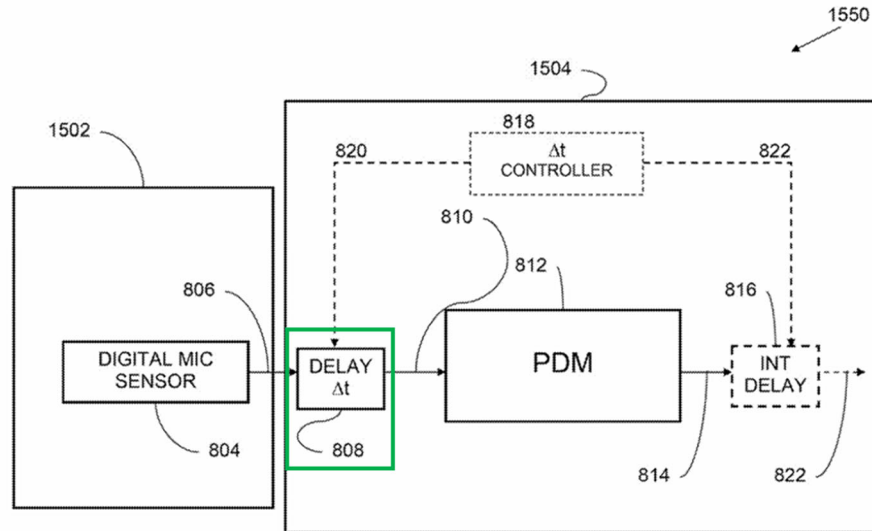


Id., Fig.15A (showing fractional delay 808 within circuit 1502) (annotated).

“With reference to 1550 a first integrated circuit die 1502 includes the digital sensor 804; **a second integrated circuit die 1504 includes the PDM receiver module 812, the time delay element 808, and one or more of the time delay controller 818, and time delay element 816.**”

Id., 16:58-60 (emphasis added).

FIGURE 15B



Id., Fig.15B (showing fractional delay 808 within circuit 1504) (annotated); *see also* Fig.2C (showing fractional delay 276).

106. From the disclosure of the '055 patent specification, a POSA would have recognized the corresponding structure of the “fractional delaying means” to be a delay element including a buffer, delay line, or delay circuit.

4. “decimating means...”

107. The “decimating means” term has a recited function “to receive the delayed oversampled digital signal and to low pass filter and to decimate to a lower sampling rate.”

108. Regarding structure, the '055 patent specification discloses a receiver module in the form of a filter or PDM receiver as providing low pass filtering and decimation to a lower sampling rate. For example:

“A filter is configured to receive as an input the delayed oversampled digital output signal. The filter low pass filters and decimates to a lower sample rate the delayed oversampled digital output signal.”

Id., Abstract (emphasis added).

“In the example of FIG. 3, the CIC filter provides 8:1 decimation which reduces the sampling clock frequency of 2.048 MHz to 256 kHz at 318 following the CIC 316 stage. The CIC stage 316 low pass filters the input digital signal 312 thereby providing an increase to the dynamic range of the output digital signal at 318.”

Id., 8:6-12.

“Half-band filter 320 decimates by a factor of 2:1 thereby reducing the sampling rate of the input signal 318 from 256 kHz to 128 kHz at the output 322. Half-band filter 320 provides further low pass filtering and a further increase in dynamic range of the signal at 322.”

Id., 8:14-19; *see also id.*, 8:21-26.

“In the example of FIG. 3, the fourth stage of PDM receiver module 314 is a low pass filter 328 which decimates by a factor of 4:1 thereby reducing the input digital signal at 326 from a sample rate of 64 kHz to a baseband sample rate of 16 kHz at 330.”

Id., 8:27-31 (emphasis added).

“The PDM receiver module 280 decimates and low pass filters the time delayed oversampled digital signal 278 and outputs a time delayed PCM baseband digital signal at 282. Those of ordinary skill in the art will recognize that PCM format is a digital data format in use with digital signals such as digital audio signals. PDM receiver modules

such as 280, as well as other receiver modules described in the other figures in this description of embodiments, can be implemented with conversion to a format other than PCM format and the description given herein with conversion to PCM format does not impose any limitation on embodiments of the invention.”

Id., 6:49-60 (emphasis added).

109. From the disclosure of the '055 patent specification, a POSA would have recognized the corresponding structure of the “decimating means” to be a filter or PDM receiver module.

5. “integer delaying means...”

110. The “integer delaying means” term has a recited function “to apply an integer time delay to the delayed oversampled digital signal, the integer time delay is a number of lower sampling rate cycles.”

111. Regarding structure, the '055 patent specification discloses a delay element providing an integer number of sampling clock cycles delay to an “oversampled digital signal.” *See, e.g.,*:

“The oversampled digital signal **214** is input into a delay element **216** and is output at **218** after a time delay “ Δt ” is imparted to the oversampled digital signal. The **time delay Δt imparted to the oversampled digital signal 214 at delay element 216 is represented by an integer number of sampling clock cycles.**”

Id., 3:27-33 (emphasis added).

112. The '055 patent specification also discloses that such delay can be applied by a “delay element” to a delayed oversampled digital signal, after

decimation, where the delay is equal to “a number of cycles at the lower sample rate.” *See, e.g.,*

“In various embodiments, the time delay element 816 can be configured to provide a fixed time delay to the input digital signal 814 or the time delay element 816 can be programmable. In operation, the controller 818 provides a control signal 822 which is used to specify **a number of cycles at the lower sample rate which will be used by the time delay element 816 to provide the time delay to the input signal 814.**”

Id., 11:6-16 (emphasis added); *see also id.*, 11:17-12:6, 16:42-50, Figs.8, 15A-B.

“FIG. 4 illustrates, generally at **400**, a pulse density modulation (PDM) receiver architecture, according to embodiments of the invention. With respect to FIG. 4, alternative locations for the time delay element **308** from FIG. 3 are illustrated. **An initial position for the time delay element 416 corresponds with the position of the time delay element 308 in FIG. 3. In this initial position, as described above the time delay element 416 delays the oversampled digital signal and outputs a time delayed digital signal at 312.**

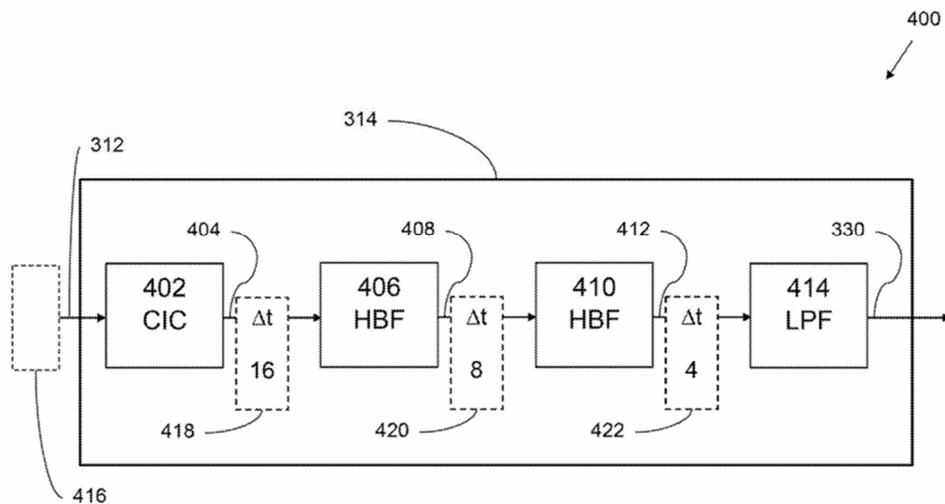
The time delay element can be located throughout the oversampled domain of the PDM module 314. In FIG. 4, a first alternative location of the delay element is indicated at **418** between the first stage **402** and the second stage **406** at location **418**...

In FIG. 4, a second alternative location of the delay element is indicated at **420** between the second stage **406** and the third stage **410** at location **420**. ...

In FIG. 4, a third alternative location of the delay element is indicated at **422** between the third stage **410** and the fourth stage **414** at location **422**... In other embodiments, **a time delay element can be located in a plurality of locations, i.e., one or more of 416, 418, 420, and 422.**”

Id., 8:46-9:42 (emphasis added).

FIGURE 4



Id., Fig.4.

113. The '055 patent specification also discloses that the time delay provided by a buffer, delay line, or delay circuit. For example:

“The time delay 108 can be of various lengths and is sometimes expressed in two parts, i.e., an integer part and a fractional part. A first part 114 can be referred to as an integer delay where ‘integer’ refers to an integer number of baseband sampling rate cycles. A second part 110 can be referred to as a fractional delay where ‘fraction’ refers to a fraction of the baseband sampling rate period. A time delayed digital version of the digital signal 106 is output at 116.”

Id., 2:60-66 (emphasis added).

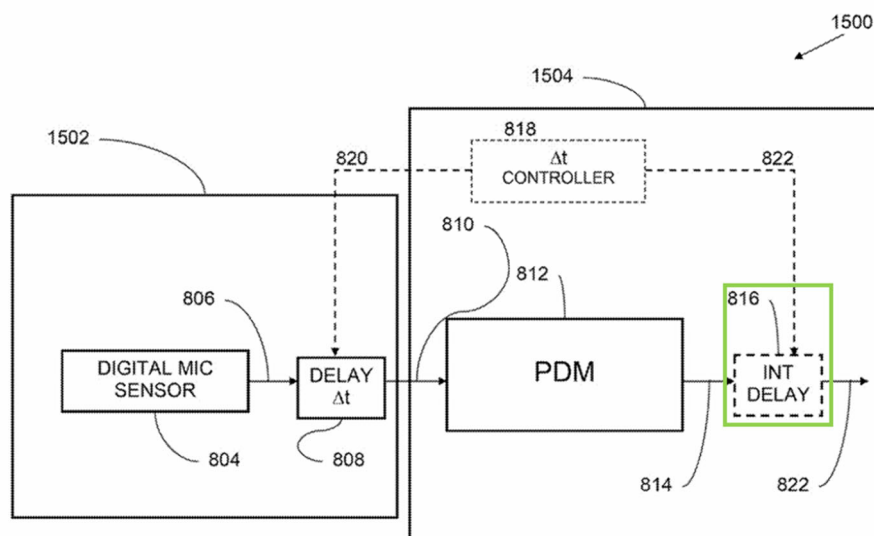
“FIG. 15A-15B illustrates integrated circuit dies in which embodiments of the invention may be implemented.”

Id., 2:26-27 (emphasis added).

“With reference to 1500, a first integrated circuit die 1502 includes the digital sensor 804 and time delay element 808; a second integrated circuit die 1504 includes one or more of the PDM receiver module 812, time delay controller 818, and time delay element 816.”

Id., 16:45-50 (emphasis added).

FIGURE 15A

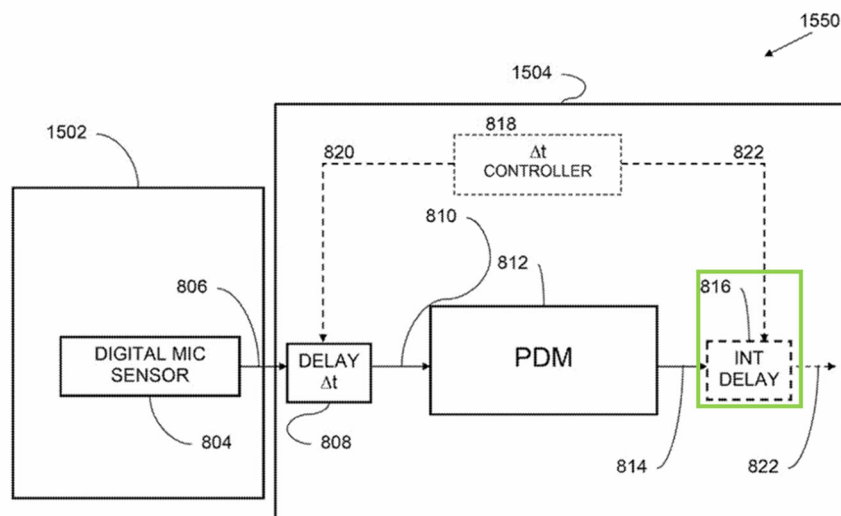


Id., Fig.15A (showing integer delay 816 within circuit 1504) (annotated).

“With reference to 1550 a first integrated circuit die 1502 includes the digital sensor 804; **a second integrated circuit die 1504 includes** the PDM receiver module 812, the time delay element 808, and one or more of the time delay controller 818, and **time delay element 816.**”

Id., 16:58-60 (emphasis added).

FIGURE 15B



Id., Fig.15B (showing integer delay 816 within circuit 1504) (annotated); *see also* 3:27-54, Fig.2C (showing integer delay 284); *supra* §IX.B.3.

114. From the disclosure of the '055 patent specification, a POSA would have recognized the corresponding structure of the “integer delaying means” to be a delay element including a buffer, delay line, or delay circuit.

6. “controlling means...”

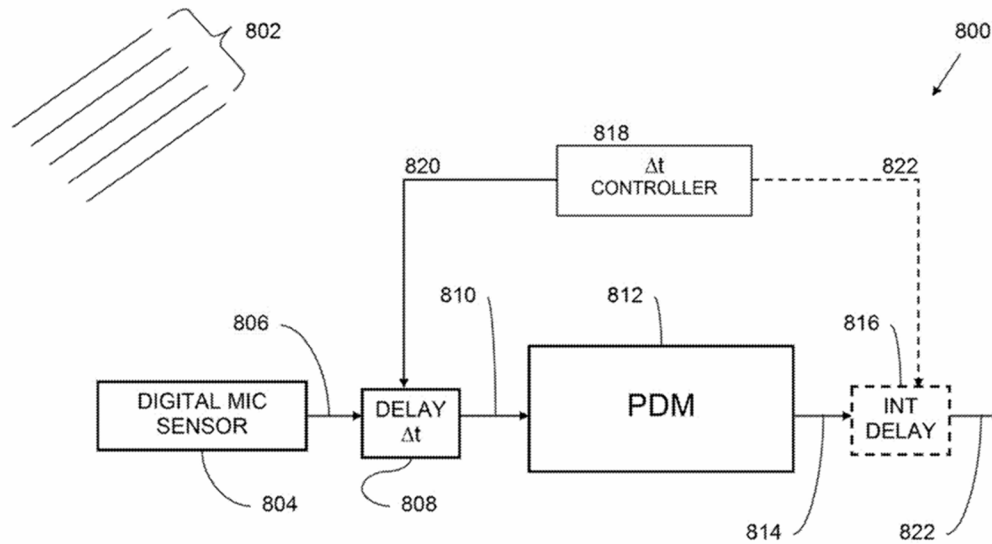
115. The “controlling means” term has a recited function “to adjust the fractional time delay and the integer time delay to establish a total time delay, wherein a resulting digital signal is delayed by a total time delay, wherein the total time delay is a sum of the fractional time delay and the integer time delay, and contains a digital representation of the analog field quantity without the noise introduced by the over sampling means.”

116. Regarding structure, the '055 patent specification discloses that the controller provides a control signal to the fractional time delay unit and a control signal to the integer time delay unit, with the total time delay being the sum of the fractional and integer delays. For example:

“In some embodiments, a controller 818 provides a control signal 820 to the time delay element 808. In some embodiments, when the time delay element 816 is configured with the system, the controller 818 or a separate controller provides a control signal at 822 to the time delay element 816.”

Ex.1001., 10:50-55 (emphasis added); *see also id.*, 11:27-29.

FIGURE 8



Id., Fig.8 (showing controller providing a control signal to fractional delay 808 and a control signal to integer delay 816); *see also id.*, Figs.15A-15B.

“In operation, the **controller 818 provides a control signal 820 which is used to specify a number of sampling clock cycles which will be used by the time delay element 808 to provide the time delay to the input signal 806.**

Similarly, when present in the system, the time delay element such as 816 can be configured as a buffer or to include a buffer which has a number of values, where each value corresponds to a different number of cycles at the lower sample rate corresponding to the output of the PDM receiver module 812. In various embodiments, the time delay element 816 can be configured to provide a fixed time delay to the input digital signal 814 or the time delay element 816 can be programmable. **In operation, the controller 818 provides a control signal 822 which is used to specify a number of cycles at the lower sample rate which will be used by the time delay element 816 to provide the time delay to the input signal 814. Thus, the total time delay imparted by the system at the output 822 relative to the input 806 is the sum of the time delay imparted by the time delay element 808 and the time delay element 816.”**

Id., 10:63-11:16 (emphasis added).

117. From the disclosure of the '055 patent specification, a POSA would have recognized the corresponding structure of the “controlling means” to be a controller configured to provide those delay control signals.

X. GROUND 1: CLAIMS 11-18, 21, 22, 34, 38-39, 41, 46, AND 48-50 ARE OBVIOUS BASED ON ADAMS AND NGUYEN

118. In my opinion, a POSA would have found claims 11-18, 21, 22, 34, 38-39, 41, 46, and 48-50 obvious based on Adams in view of Nguyen.

A. Motivation to Combine

119. In my opinion, a POSA implementing Adams’ system for time delay would have looked to and been motivated to further implement Nguyen’s teachings regarding low pass decimation filters, and digital microphones including a MEMS sensor integrated with a sigma-delta modulator analog-to-digital converter (ADC), as explained below.

120. First, as described above in the Technical Background section, there were many well-known historical examples of digital processing systems for processing of signals from microphone arrays, including e.g., in delay and sum beamforming of signals from microphone arrays, including use of microprocessors that include memory for storing code and are configured to execute such code, oversampled ADCs for converting analog signals to digital format, and digital signal processors for execution of filtering, delaying, decimating, and combining the

signals from a microphone array. *See supra* §VI. A POSA at the time of the earliest claimed priority date of the '055 patent would have been well-aware of exemplary uses of these elements, and the advantages of combining these elements in various ways. All elements of claims 11-18, 21, 22, 34-35, 38-41, 46, and 48-50 were known since long before the '055 patent.

121. A POSA would have been particularly motivated to combine the teachings of Adams and Nguyen given that both are directed to audio microphone signal processing systems, and the systems taught in Adams and Nguyen include many of the same features, such as a digital microphone, analog-to-digital converter (ADC), and decimation filter, for example.

122. Further, both Adams and Nguyen are patent publications from the same company, Analog Devices, and both name Robert Adams as an inventor. Nguyen, in fact, was filed approximately two years after Adams was filed. These facts would have provided a POSA, considering Adams, with reason and further motivation to consider Nguyen for further developments from Analog Devices and the inventor Robert Adams on audio microphone signal processing systems.

123. Adams teaches a system to time delay comprising a digital microphone (comprising a microphone and follow-on analog-to-digital converter), two time delay elements, a decimation filter located between the two time delay elements, and

a controller supplying a control signal to set the delays of the two delay elements. E.g., Ex.1005, [0023]-[0029], Figs.1-6.

124. Nguyen similarly teaches a digital signal processing system including a digital microphone and decimation filtering. E.g., Ex.1006, [0027], [0030], [0035], [0037], Figs.1, 3. Nguyen further provides details, including that the decimation filter is low pass. Ex.1006, [0035] (“The decimator 306 preferably comprises a lowpass filter 308 which may be...integrated with the decimator.”), [0037] (“unwanted” higher “frequency components are attenuated by passing the...signal...through a combined lowpass filter and decimator []”). Nguyen also details that its digital microphone sensor is a MEMS sensor, and ADC is a sigma-delta modulator. E.g., Ex.1006, [0007] (“The transducer signal may accordingly be generated by one of the above mentioned microphone devices. The MEMS capacitive microphone may comprise a micro-electromechanical (MEMS) transducer element, e.g. shaped and sized for portable audio devices such as smartphones, tablets and mobile phones etc.”), [0006], [0027]-[0030]. All these implementation details would provide specific guidance to a POSA interested in constructing a system that uses oversampled digital data from a microphone and provides time delays, filtering, and decimation.

125. Regarding all claims of the '055 patent addressed in this declaration, even if Adams did not disclose or otherwise render obvious the type of filtering

performed by its system's decimation filter to be low-pass filtering, a POSA would have at least been motivated by Nguyen's teachings to implement Adams' decimation filter as a low-pass decimation filter.

126. First, a POSA would have naturally considered the teachings of Nguyen, especially given that it overlaps in subject matter with Adams; it relates to the same company and inventor as Adams; and it reflects more recent work of that company and inventor, having been filed approximately two years after Adams.

127. Second, Nguyen, like Adams, discloses the use of a decimation filter in an audio microphone signal processing system to suppress higher frequency noise components, and expressly identifies the decimation filter type as low pass.

128. In my opinion, a POSA would have been motivated to combine the teachings of Nguyen with Adams in implementing Adams' system so that the decimation filter is low pass, which would have had the beneficial result of suppressing higher frequency noise from the decimated signal in Adams' system. Decimation filters are generally low pass filters, as a POSA would have understood, in order to pass the desired relatively low frequency in-band signal and attenuate higher-frequency components in the signal, including out-of-band quantization noise, as well as to suppress aliasing in systems. *See supra* §VI.D. A POSA would have also understood that both Adams and Nguyen seek to minimize signal distortion and achieve low-noise performance. *See, e.g.,* Ex.1005, [0002]

(acknowledging that as “background,” “[m]icrophone arrays have been used to improve fidelity and reduce effects of ambient noise.”); Ex.1006, [0002] (“[v]arious beamforming algorithms may be used to combine the signals from each of the microphones in the array so that audio signals originating from a particular direction constructively interfere and generate a highest magnitude response over audio signals originating from other directions”).

129. The resulting system would help reduce unwanted noise in Adams’ system, which in my opinion is consistent with Adams’ aims. E.g.,

Ex.1005, [0002]:

“Microphone arrays have been used to improve fidelity and reduce effects of ambient noise. Arrays of two or more microphones may be used to capture specific audio signals while reducing the effects of background noise and other undesirable sounds. Various beamforming algorithms may be used to combine the signals from each of the microphones in the array so that audio signals originating from a particular direction constructively interfere and generate a highest magnitude response over audio signals originating from other directions.”

Id., [0081]:

“[M]icrophone arrays may create a beamformed output to reduce the effects of ambient noises, such as vehicle engine sounds, third party conversations, background sounds, and other unwanted noise when communicating in a hands-free mode.”

See also Ex.1006, [0035], [0037]; *supra* §VI.D.

130. With respect to claim 15 of the '055 patent, even if Adams did not expressly disclose or otherwise render obvious a MEMS microphone sensor, a POSA would have at least been motivated by Nguyen's teachings to implement such a sensor in Adams, as such microphones were well established and commercially available. *See supra* §VI.E.

131. Nguyen discloses a digital microphone (Ex.1006, [0001], [0004], [0006]), and further specifies that it "may comprise a micro-electromechanical (MEMS) transducer element, e.g. shaped and sized for portable audio devices such as smartphones, tablets and mobile phones etc." *Id.*, [0007]. The "electromechanical (MEMS) transducer element may function as a single element audio and ultrasonic microphone responsive to both impinging audible sound and ultrasonic sound due to its broad-band frequency response." *Id.* Thus, Nguyen discloses that the digital microphone utilizes a MEMS sensor, as recited in claim 15 of the '055 patent.

132. With respect to claims 12, 13, 18, 22 (and its dependents), 41, and 50, for example, even if Adams did not disclose or otherwise render obvious its digital microphone sensor as utilizing a sigma-delta modulator ADC to output a pulse density modulated (PDM) signal or alternatively output samples that are more than one bit deep (e.g., multi-bit), a POSA would have at least been motivated by Nguyen's teachings to implement such an ADC in Adams, as microphones

integrated with sigma-delta modulator ADCs were well-established and, in fact, commercially available before the earliest claimed priority date of the '055 patent.

133. Nguyen discloses that its MEMS microphone sensor is integrated with a follow-on circuit 100 including a sigma-delta modulator ADC. E.g., Ex.1006, [0007]-[0008], [0012], [0013], [0027]-[0030]; *see also id.*, [0001], [0035]. The “circuit 100 may be shaped and sized for integration into a miniature MEMS microphone housing or package.” *Id.*, [0028]. Further, the sigma-delta modulator ADC, as Nguyen teaches, may include a single-bit quantizer and output a pulse density modulated (PDM) signal, or alternatively, a multi-bit quantizer. *See, e.g.*,

Id., [0012]:

“Each of the first and second sigma-delta modulators may comprise a single-bit quantizer or a multi-bit quantizer with their respective well-known advantages and disadvantages. If each of the first and second sigma-delta modulators comprises the single-bit or one bit quantizer the first and second digital signals may be conveniently supplied as first and second PDM signals, respectively. Alternatively, each of the first and second digital signals may be converted from native PDM format to a multi-bit or PCM format. Each of the first and second sigma-delta modulators preferably operates at an oversampled sampling frequency such as a sampling frequency between 1 MHz and 10 MHz.”

see also id., [0030] (“The skilled person will appreciate that each of the first and second sigma- delta modulators 110, 112 may comprise a single-bit quantizer or a multi-bit quantizer.”).

134. Regarding claims 12, 13, 15, 18, 22 (and dependents), 41, and 50 (as well as claims 11 and 46 as an alternative position), as addressed in this declaration, a POSA would have been motivated to combine the teachings of Nguyen with Adams so that the system's digital microphone utilizes a MEMS sensor integrated with a sigma-delta modulator ADC.

135. Adams and Nguyen have similar aims. A POSA would have also understood that both Adams and Nguyen seek to reduce the assembly costs and space required to implement its digital microphones. For example, Adams expresses a desire to reduce space consumption and costs, and improve reliability (Ex.1005, [0003]-[0004]). *See*:

“These beamforming algorithms were originally implemented in signal processing devices, which required each of the microphones to be individually wired to separate inputs of the signal processing device, typically an integrated circuit. The number of wires therefore increases proportionally with the number of microphones in the array. **Incorporating these extra wires requires additional expense and space in the device. Additionally, the extra wires may affect the overall reliability of the system as the likelihood of a defect, malfunction, or problem with one or more of the wire sets tends to increase as the number of wires increases.**”

Ex.1005, [0003] (emphasis added).

136. Adams addresses its desire for reduced space consumption and costs, and improved reliability with a staged daisy chain approach reducing the number of wires in its system. *See id.*, [0016], [0081].

“Embodiments of the invention provide a system having an array of microphone stages in which each of the microphone stages may be coupled together in a daisy chain.”

Id., [0016].

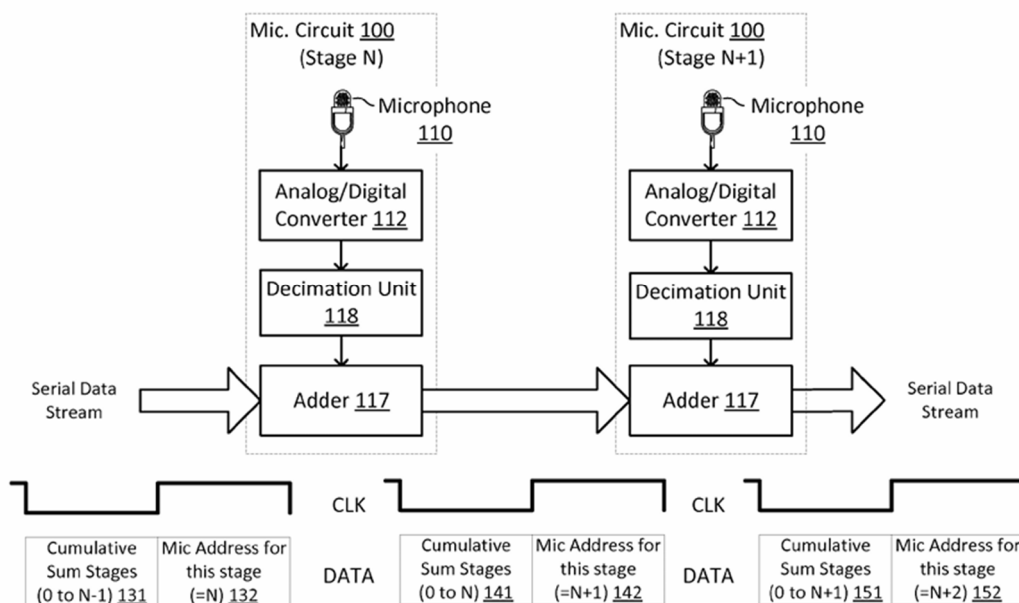
“FIG. 9 shows an exemplary devices in embodiments of the invention. For example, microphone arrays **901** including several daisy chained microphone circuits **100** as previously discussed may be embedded in vehicles **910**, hands-free communication devices **920**, laptops and other computers **930**, and televisions **940**, among other devices. In these devices, the microphone arrays may create a beamformed output to reduce the effects of ambient noises, such as vehicle engine sounds, third party conversations, background sounds, and other unwanted noise when communicating in a hands-free mode.”

Id.

“FIG. 2 shows an exemplary daisy chaining of two microphone circuits in a microphone array.”

Id., [0006].

FIG. 2



Id., Fig.2.

137. Nguyen similarly recognized the same problem/need as Adams and taught a solution which implemented a MEMS sensor integrated with a follow-on circuit 100 comprising a sigma-delta modulator ADC. *See* above discussion. Such integration provided a number of advantages, as taught by Nguyen:

“Hence, it is advantageous to integrate multiple functions in a single transducer unit such as a microphone. **This type of integration may reduce power consumption of active circuitry, reduce space consumption and lower assembly costs** of the portable communication or computing device in question. Portable communication devices furthermore often comprise a plurality of transducers such as microphones for voice and sound pick-up, recording and transmission which adds to the advantages of integrating multiple functions in a single transducer device.”

Ex.1006, [0002] (emphasis added); *see also, id.*, [0003].

138. For example, as stated by Nguyen, such integration “reduce[d] space consumption and lower[ed] assembly costs.” Ex.1006, [0002]-[0003], [0028]. Additionally, Nguyen discloses that its integration offered “reduce[d] power consumption of active circuitry” (Ex.1006, [0002]-[0003]), which is further notable because reduced power consumption is something that Adams also acknowledges would have benefits. Ex. 1005, [0067], [0094].

139. Further, Nguyen, filed approximately two years after Adams, teaches that such MEMS sensors were “[c]ommonly used” by that time, “shaped and sized for portable audio devices such as smartphones, tablets and mobile phones etc.,” and

“integra[ble] into a miniature MEMS microphone housing or package.” Ex.1006, [0006]-[0007], [0028]. The use of sigma-delta modulator ADCs in digital signal processing was also prevalent and well known. *See supra* §§VI.C, E.

140. Given the overlapping aims of Adams and Nguyen, as well as Nguyen’s solution resulting in the integration of the MEMS microphone sensor and follow-on sigma-delta modulator ADC, the combination of Adams and Nguyen would provide the abovementioned benefits in Adams’ system, in line with Adams’ aims.

141. In my opinion, this combination would have had a number of beneficial results, including saving space, reducing assembly costs, improving reliability, and facilitating integrability in Adams’ system, in line with Adams’ aims, and Nguyen’s teachings.

B. Reasonable Expectation of Success

142. In my opinion, a POSA would have had a reasonable expectation of success in combining Adams and Nguyen.

143. Adams and Nguyen are similar disclosures, in that they both concern audio microphone signal processing systems; they are also disclosures from the same company and share the same inventor. Further, Adams’ and Nguyen’s systems include many of the same components, as discussed above. With respect to a number of relevant features here, the more recent (Nguyen) publication provides additional express disclosure. For example, Nguyen provides such express disclosure

regarding the decimation filter being a low pass decimation filter, the digital microphone sensor being a MEMS sensor, and the digital microphone ADC being a sigma-delta modulator.

144. Configuring Adams' decimation filter as low pass would have been straightforward given the similarities in Adams and Nguyen, including those mentioned above. Further, Nguyen teaches that its decimation filter provides decimation factors "between 16 and 128" (Ex.1006, [0035]), which is similar to factors taught by Adams. Ex.1005, [0090] (decimation factor of 16), [0088] (decimation factor of 128). Nguyen also teaches the use of its decimation filter to downsample from an ADC oversampled frequency to "a desired final sample rate for the outgoing digital audio stream" (Ex.1006, [0035]), which is similar to Adams, which discloses downsampling from an ADC oversampled frequency to the digital "audio frame rate." Ex.1005, [0016], [0022], claims 3, 43. A POSA would have had a reasonable expectation of success because the proposed implementation merely applies Nguyen's known decimation filter low-pass teachings to Adams' known decimation filter without changing Adams' multiple time delay operations and structure. In addition, the use/configuration of low pass decimation filters was well-known and generally used for decades before the '055 patent. *See supra* §VI.D. In my opinion, a POSA applying Nguyen's known low-pass decimation filter

teachings to Adams' decimation filter would have been no more than the predictable use of prior-art elements according to their established functions.

145. Implementing Adams' digital microphone to utilize a MEMS sensor and the follow-on ADC as a sigma-delta modulator, as taught by Nguyen, would have likewise been straightforward given the similarities in Adams and Nguyen, including those mentioned above. Further, both Adams and Nguyen teach the use of digital microphones, with Nguyen expressly specifying as including a MEMS sensor integrated with follow-on sigma-delta modulator ADC. The use of MEMS microphone sensors and sigma-delta modulator ADCs were well-known and used long before the '055 patent. *See supra* §§VI.C, E. A POSA would have had a reasonable expectation of success because the proposed implementation merely applies Nguyen's known (and expressly disclosed) digital microphone utilizing a MEMS sensor integrated with a sigma-delta modulator ADC teachings to Adams' known digital microphone without changing Adams' multiple time delay operations and structure. Nguyen, filed two years after Adams, in fact, also discloses that "MEMS capacitive microphones" were "[c]ommonly used" by that time, "shaped and sized for portable audio devices such as smartphones, tablets and mobile phones etc." Ex.1006, [0006]-[0007]. Further, the follow-on sigma-delta modulator circuit also "may be shaped and sized for integration into a miniature MEMS microphone housing or package." *Id.*, [0028], [0030]. A POSA would have understood this,

consistent with these teachings, and the implementation in Adams would accordingly have been facilitated. In my opinion, such an implementation would therefore have been no more than the predictable use of prior-art elements according to their established functions.

146. Further, Analog Devices, the company associated with both disclosures, was already well-known for success at developing MEMS devices with integrated circuits, including accelerometers, gyroscopes and others, all featuring integration of the MEMS and the circuitry, and that the family of circuits available for integration at this time would include the entire product portfolio of digital circuits produced by ADI. Based on this history, there is every reason to expect success at developing a product based on the teachings in these two disclosures, especially for practitioners working at ADI at the time.

C. Claim 11

147. It is my opinion that a POSA would have found claim 11 obvious based on Adams in view of Nguyen (“Adams-Nguyen”).

148. In my opinion, claim 11 is directed to a system to time delay digital signals, whereby the system includes a digital sensor responsive to an analog field quantity and outputting an oversampled digital signal; a first delay element that receives the oversampled digital signal as input and outputs a time delayed oversampled digital signal; a filter, which low pass filters and decimates the time

delayed oversampled digital signal received from the first delay element; a second delay element that receives the low pass filtered decimated delayed digital signal as input and further delays this signal; and a controller configured to supply a control signal to set the delays of the two delay elements.

149. Consistent with my discussion in the Technical Background and Overview of the Prior Art sections of this declaration, all elements of this claim have existed and been in use separately and together for many functions, including to form beamformed digital signals, well before the '055 patent. *See supra* §§VI, VIII.

150. Regarding the prior art discussed in Ground 1, it is my opinion that Adams is directed to a system to time delay comprising a digital microphone (comprising a microphone and follow-on analog-to-digital converter), two time delay elements, a decimation filter located between the two time delay elements, and a controller configured to supply a control signal to set the delays of the two delay elements.

151. It is also my opinion that Nguyen is similarly directed to an audio processing (e.g., microphone) system and includes features such as a digital microphone (including a MEMS capacitive sensor and analog-to-digital converter integrated in the same package) and a low-pass decimation filter. In my opinion, consistent with my discussion above (*see supra* §§X.A.B and below), it would have

been obvious to a POSA to apply Nguyen's teachings of a decimating filter that is low pass to the decimation filter in Adams' system.

1. 11[pre]: "A system to time delay digital signals, comprising:"

152. I have been asked to assume the preamble of claim 11 is limiting. Under that assumption, it is my opinion that Adams discloses claim 1's preamble, 1[pre], which recites "[a] system to time delay digital signals, comprising."

153. In my opinion, Adams discloses a system in which each microphone stage includes delay units that implement time delays on signals that had been converted from analog to digital form. Specifically, Adams discloses that "[e]ach delay unit may have a delay selected to insure [sic] that the audio data from its associated microphone corresponding to sound from a particular direction is time-aligned with the data represented by the cumulative sum arriving at the receiver of that microphone stage." *See* Ex.1005, [0022]. Adams further explains that "[t]o achieve precise control over the steering direction, the delay at each microphone node may need to be adjusted in finer steps than can be accomplished by using an integer number of sample-periods, and therefore it may be necessary to set both an integer as well as a fractional delay amount." *Id.* A POSA would have understood the use of the phrase "time-aligned" and the description of delays measured in sample periods makes clear that the delays described in Adams are time delays

applied to digital signals. Such a skilled person would have also understood Adams' delay units as implementing time delays.

154. Adams discloses a microphone circuit 100. Ex.1005, [0023]-[0031], Figs.1-5. The microphone circuit 100 includes a microphone, analog to digital converter, decimation unit, among other elements. *Id.*, [0016]; Fig.1; *see also id.*, Figs.2-6.

155. The “analog to digital converter...may generate digital code words from the analog audio signal obtained from the microphone.” Ex.1005, [0023]. The “decimation unit...may also include a delay unit to implement a delay with one or more delay elements.” *Id.*, [0025], [0022], [0016], Fig.1(Decimation Unit 118 including fine integer delay 113 and coarse integer delay 115).

2. 11[a]: “a digital sensor responsive to an analog field quantity, the digital sensor is configured to output an oversampled digital output signal at a sampling clock frequency;”

156. In my opinion, Adams discloses this limitation. Also, it is my opinion that Adams in view of Nguyen renders this limitation obvious.

157. As an initial matter, as discussed in the Technical Background and Overview of the Prior Art sections of this declaration above, systems that utilize a digital sensor to output oversampled digital signals from received analog signals were widely known and used long before the '055 patent's earliest claimed priority date. *See, e.g., supra* §§VI, VIII.

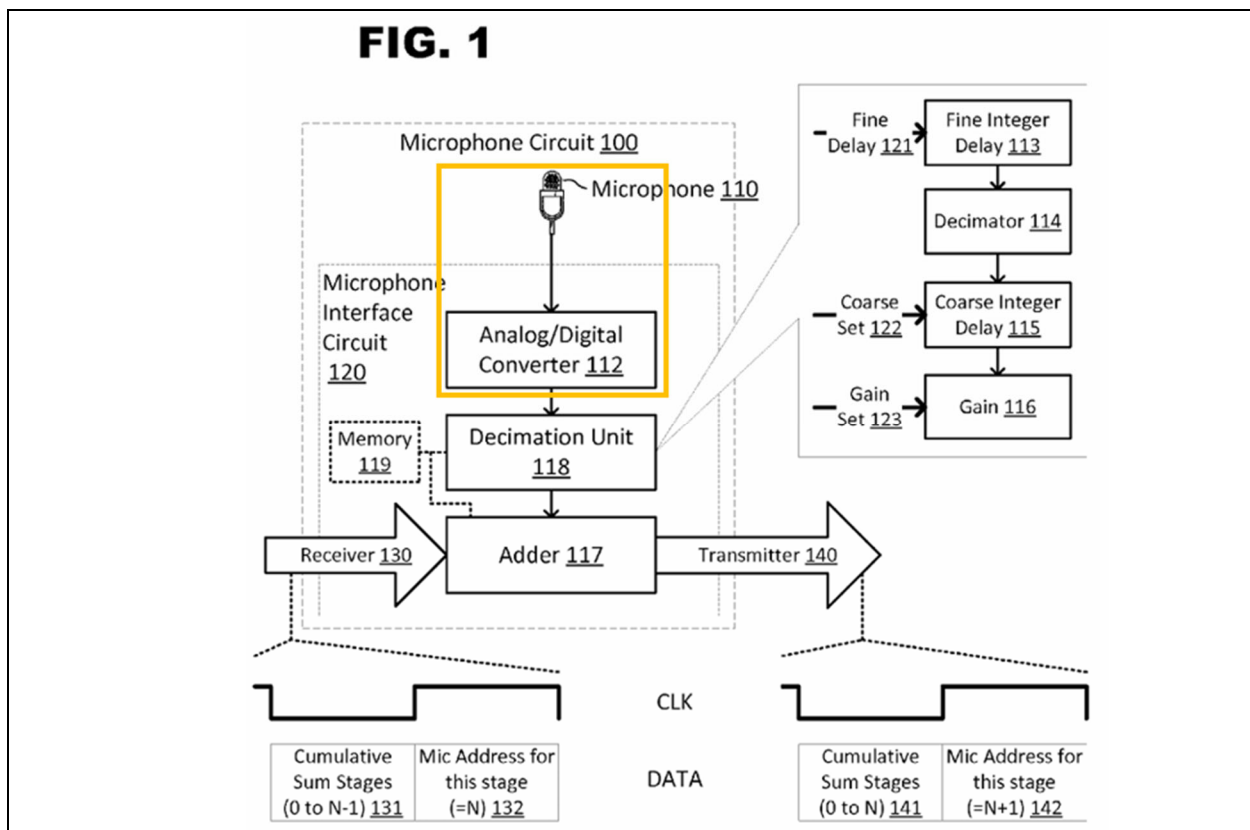
158. Referring specifically to the prior art cited in this section of my declaration, Adams discloses a digital microphone as part of its microphone circuit 100, which includes a microphone and a follow-on analog-to-digital converter (ADC). Ex.1005, [0016]; Fig.1 (showing microphone 110 connected to ADC 112). Adams discloses that the “microphone...may be coupled to” the ADC “that may generate digital code words from the analog audio signal obtained from the microphone.” *See*:

“A microphone 110 may be coupled to a microphone interface circuit 120, which may include a preamplifier (not shown) to initially boost an analog signal from the microphone, an analog to digital converter 112, decimation unit 118, and adder 117. **The microphone and/or preamplifier may be coupled to an analog to digital converter 112 that may generate digital code words from the analog audio signal obtained from the microphone 110.**”

Id., [0023] (emphasis added), [0027] (discussing “the generated digital code words outputted by the converter 112”); *see also id.*, Figs.2-6 (showing microphone 110 connected to ADC 112).

159. Thus, Adams discloses the claimed “digital sensor” as exemplified by Adams’ combination of microphone 110 and ADC 112 within microphone circuit 100. In my opinion, that understanding is consistent with the disclosure of the ’055 patent, which describes a “digital sensor” as responsive to an analog field and outputting a digital signal. *See* Ex.1001, 3:10-15 (“an analog field quantity 202 is incident upon a digital sensor 212. The digital sensor 212 converts the incident

analog field to an oversampled digital output signal at 214 which preserves phase information of the signal within the bit stream of the signal 214”). That understanding is further consistent with the ’055 patent disclosure of a digital microphone as an example of a digital sensor, and that includes an ADC. Ex.1001, 4:23-28, 5:4-6, 5:42-55, 11:19-23, 12:16-22, 13:17-22, 14:53-58, Figs.9A-9B, 10, claim 14.



Ex.1005, Fig.1 (annotated).

160. Adams' digital sensor (corresponding to Adams' microphone 110 and ADC 112 combination) is responsive to an analog field quantity (e.g., sound or acoustic pressure) and configured to output a corresponding digital signal, as

indicated by the output of the microphone 110 being connected to the input of an analog/digital converter in Fig.1. Ex.1005, [0002] (“microphones may be used to capture specific audio signals while reducing the effects of background noise and other undesirable sounds”), [0022] (“audio data from its associated microphone corresponding to sound”), claim 21 (discussing “sound...represented as the...digital code outputted by the decimation unit of a respective microphone stage”). A POSA would have understood that a microphone is responsive to sounds (or acoustic pressure), an analog field quantity, which is a continuously varying analog signal that the microphone senses and converts into a corresponding electrical signal. *See also* Ex.1014, p. 7 (Graf, 471) (“**microphone**—1. An electroacoustic transducer that responds to sound waves and delivers essentially equivalent electric waves. 2. A device for converting sound waves or sound-producing vibrations (as from the strings of a guitar) into corresponding electrical impulses...”), p. 10 (Graf, 714) (“**sound**—1. Also called a sound wave. An alteration in pressure, stress, particle displacement or velocity, etc., propagated in an elastic material or the superposition of such propagated alterations.”). In my opinion, that understanding is consistent with the disclosure of the ’055 patent, which describes, as an example, its microphone being responsive to an analog field relating to sound. E.g., Ex.1001, 6:4-6 (“The MEMS digital microphones can be configured with a sigma-delta modulator which produces an oversampled digital output of the **analog signal**

sensed by the microphone”) (emphasis added); *see also id.*, 1:30-33 (“Field quantities which exist in the natural world are generally analog signals which have continuously varying amplitude as a function of time. Examples of these field quantities are sound pressure, vibration, light, etc.”), 7:24-25 (“An analog field quantity e.g., an acoustic field 302 is sensed by a digital microphone 304.”), 10:34-37 (“FIG. 8 illustrates, generally at 800, programmable time delay in an analog-to-digital converter (ADC) system, according to embodiments of the invention. With respect to FIG. 8, an analog field quantity is represented by 802 incident on a digital sensor 804, which in various embodiments, is a digital microphone,...”), 11:19-23 (“With respect to FIG. 9A, an analog field quantity is represented by 902, which is incident on digital sensors 920, 940, up to a general number of n sensors indicated by 960, which in various embodiments is a digital microphone,...”), 12:18-21 (“With respect to FIG. 9B, an analog field quantity is represented by 902, which is incident on a digital sensor 920, which in various embodiments is a digital microphone, vibration sensor, electromagnetic energy sensor, etc.”), 13:17-21 (“With respect to FIG. 10, an analog field quantity is represented by 1002, which is incident on digital sensors 1004 and 1006. In one or more embodiments, the digital sensors 1004 and 1006 are digital microphones...”), 5:42-47, 14:20-30, Figs.8, 9A-9B, 10 (analog field quantity 802/902/1002).

161. Adams' digital sensor's ADC is also configured to output an oversampled digital output signal at the sampling clock frequency of the ADC (i.e., the ADC's oversampled clock rate) given Adams' disclosure that its system "may oversample the analog audio signal" and "convert sampled audio signals from the microphone into digital codes." Ex.1005, [0016]; *see also*:

"FIG. 1 shows an exemplary block diagram of a microphone circuit 100 in an embodiment of the invention. A microphone 110 may be coupled to a microphone interface circuit 120, which may include a preamplifier (not shown) to initially boost an analog signal from the microphone, an analog to digital converter 112, decimation unit 118, and adder 117. **The microphone and/or preamplifier may be coupled to an analog to digital converter 112 that may generate digital code words from the analog audio signal obtained from the microphone 110.**"

Id., [0023] (emphasis added).

"The analog digital converter 112 may **oversample the analog audio signal at higher frequencies**, such as 2.4 MHz or higher in some embodiments, than are used to transmit the serial audio data between microphone circuits 100 in the microphone array, which may transmit data at 44 kHz."

Id., [0024] (emphasis added), claim 23 ("the ADC clock frequency is at least 2.4 MHz and the serial data stream frame clock frequency is about 44 kHz"); *see also id.*, [0022] (discussing "the higher frequency clock rates used in the oversampling analog-to-digital converter"), [0028] ("sampling rate of the digital code words outputted by the converter **112**").

162. Even if Adams did not disclose or otherwise render obvious that “a digital sensor responsive to an analog field quantity, the digital sensor is configured to output an oversampled digital output signal at a sampling clock frequency,” a POSA would have found it obvious to provide such implementation, at least in light of the teachings of Nguyen. *See supra* §§X.A-B.

163. Nguyen discloses a digital microphone for responding to sound. Ex.1006, [0001], [0004], [0006], [0007] (“The electromechanical (MEMS) transducer element may function as a single element audio and ultrasonic microphone responsive to both impinging audible sound and ultrasonic sound due to its broad-band frequency response.”), [0020].

164. Nguyen further discloses its digital microphone as including a MEMS sensor integrated with a follow-on sigma-delta modulator ADC. *Id.*, [0007]-[0008], [0012]-[0013], [0027]-[0028], Fig.1; *see also id.*, [0001], [0035].

165. Additionally, Nguyen discloses that the “sigma-delta modulators preferably operate[] at an oversampled sampling frequency” and output an oversampled “digital signal” at that sampling frequency. *Id.*, [0012] (“Each of the first and second sigma-delta modulators may comprise a single-bit quantizer or a multi-bit quantizer with their respective well-known advantages and disadvantages. If each of the first and second sigma-delta modulators comprises the single-bit or one bit quantizer the first and second digital signals may be conveniently supplied

as first and second PDM signals, respectively. Alternatively, each of the first and second digital signals may be converted from native PDM format to a multi-bit or PCM format. Each of the first and second sigma-delta modulators preferably operates at an oversampled sampling frequency such as a sampling frequency between 1 MHz and 10 MHz.”), [0030].

166. Accordingly, Adams in view of Nguyen includes an integrated MEMS sensor/sigma-delta modulator (*supra* §§X.A-B), and renders obvious a digital sensor, responsive to an analog field quantity, configured to output an oversampled digital output signal at a sampling clock frequency.

3. **11[b]: “a first time delay element, the first time delay element is configured to receive as an input the oversampled digital output signal and to output a time delayed oversampled digital output signal, wherein the time delayed oversampled digital output signal is time delayed by a fractional delay, the fractional delay is equal to an integer number of sampling clock cycles times the sampling clock period;”**

167. In my opinion, Adams discloses this limitation.

168. As an initial matter, as discussed in the Technical Background and Overview of the Prior Art sections above, the use of a time delay element to output a time-delayed oversampled digital output signal where the time delay is equal to an integer number of cycles of the sampling clock times the sampling clock period was widely known and broadly used long before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §§VI, VIII.

169. Referring specifically to the prior art cited in this section of my declaration, Adams discloses that its time delay system includes multiple time delay elements. Ex.1005, [0022]-[0029], Fig.1; *see also id.*, Figs.2-6. For example, Adams discloses that “[e]ach delay unit may have a delay selected to insure [sic] that the audio data from its associated microphone corresponding to sound from a particular direction is time-aligned with the data represented by the cumulative sum arriving at the receiver of that microphone stage.” *Id.*, [0022].

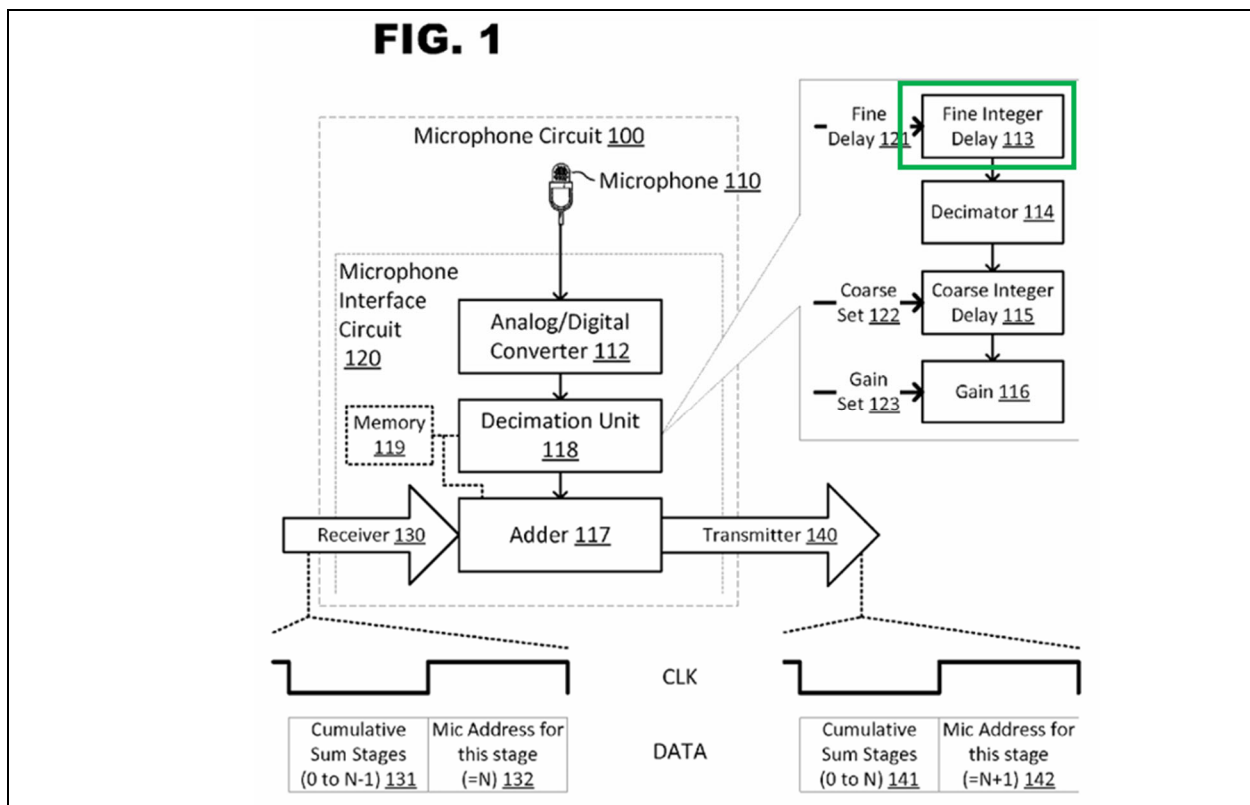
170. Adams discloses a first time delay element, which it refers to as “fine integer delay element 113.”² Ex.1005, [0025]-[0026]. ADC 112, which outputs an oversampled digital signal, is coupled to the input of fine integer delay element 113, which receives the oversampled digital signal:

“A fine variable integer delay 113 may be coupled to the analog to digital converter 112. The fine variable integer delay 113 may include a fine delay input 121, which may be used to select a whole number of cycles at the higher frequency of the analog to digital converter 112 to delay the generated digital code words outputted by the converter 112. Since the analog to digital converter 112 may operate at frequencies many times higher than the serial data stream, the fine variable integer delay 113 may enable the selection of a precise

² Adams uses the terminology “fine integer delay 113,” “fine integer delay element 113,” “fine variable integer delay 113,” “fine variable integer delay unit 113” and “fine integer variable delay 113” to refer to the same element. *See, e.g.*, Ex.1005, [0026]-[0028], [0059], [0060], Figs.1, 4-6.

delay amount to maximize alignment of the audio signals received at different times at each microphone in the microphone array.”

Id., [0027], Fig.1; *see also id.*, [0059] (“A fine variable integer delay unit **113** may be coupled to the converter **112** to delay the digital output from the converter **112** an integer number of converter clock cycles.”), [0089], Figs.4-5.



Ex.1005, Fig.1 (annotated).

171. Further, Adams discloses that “fine integer delay 113 may include a fine delay input 121, which may be used to select a whole number of cycles at the higher frequency of the analog to digital converter 112 to delay the generated digital code words outputted by the converter 112.” Ex.1005, [0027]. As a POSA would have understood, a “whole number” is an “integer.” *See, e.g.*, Ex.1014. p. 5 (Graf,

381) (“**integer** – A whole number, which may be positive, negative, or zero.”). Adams further identifies this delay implemented by fine integer delay 113 as a “fractional” time delay. *See* Ex.1005, [0022] (“[I]t is possible to use the higher frequency clock rates used in the oversampling analog-to-digital converters to implement the fractional part of the delay,”); *see also id.*, [0089] (“if the fractional delay is associated with the original ADC output sample rates [], it would be possible to select a fractional delay amount”).

172. As I discussed above, Adams discloses “a whole number of cycles at the higher frequency of the analog to digital converter 112” may be “select[ed]” “to delay the generated digital code words outputted by the converter 112.” Ex.1005, [0027]. A POSA would have understood that a whole number (i.e., integer) number of (ADC) sampling clock cycles can also be expressed in time units. Specifically, given that each sampling clock cycle has a duration of one period of the sampling clock, the delay in time units equals an integer number of (ADC) sampling clock cycles times the (ADC) sampling clock period. *See also* Ex.1014, p. 8 (Graf, 547) (**period**... 1. The time required for one complete cycle of a regular, repeating signal, function, or series of events.”).

173. Thus, it is my opinion that Adams’ fine integer delay element 113 is a “first delay element” that “is configured to receive as an input the oversampled digital output signal and to output a time delayed oversampled digital output signal,

wherein the time delayed oversampled digital output signal is time delayed by a fractional delay, the fractional delay is equal to an integer number of sampling clock cycles times the sampling clock period.”

4. **11[c]: “a filter, the filter is configured to receive as an input the time delayed oversampled digital output signal, the filter to low pass filter and to decimate to a lower sample rate the time delayed oversampled digital output signal and to output a low pass filtered decimated delayed digital output signal, wherein the lower sample rate is less than the sampling clock frequency;”**

174. In my opinion, Adams in view of Nguyen renders this limitation obvious.

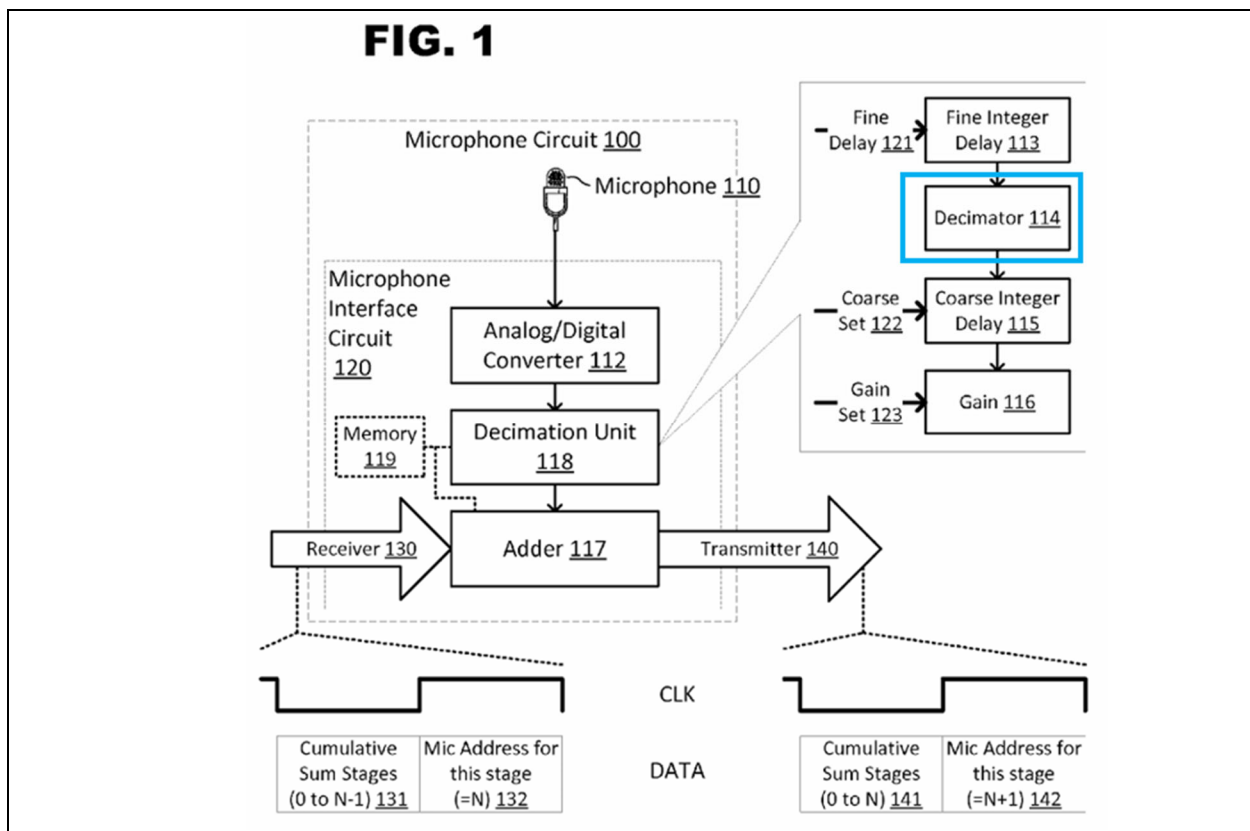
175. As an initial matter, as discussed in the Technical Background and Overview of the Prior Art sections above, the use of a decimating filter to low pass filter and decimate to a lower sampling rate was widely known and used long before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §§VI, VIII.

176. Referring specifically to the prior art cited in this section of my declaration, Adams, as I discussed above, discloses that its fine variable integer delay 113 element outputs a time delayed oversampled digital output signal. *See supra* §X.C.3(11[b]).

177. Adams also discloses that a filter, namely “decimator 114 may be coupled to the output of the fine variable integer delay 113.” Ex.1005, [0028]. Decimator 114 is referred to, by Adams, as a “decimation filter”:

“A decimation unit 118 may be coupled to the converter 112 and may decimate the digital code words generated at the converter 112. In some instances, the decimation unit 118 may decimate the digital code words by first filtering or otherwise transforming the ADC output codes before downsampling the codes. In other instances, the decimation unit 118 may decimate the digital code words by directly downsampling the ADC output codes. The decimation unit 118 may include a delay unit with one or more delay elements 113 and/or 115 that may implement a delay using memory or storage units at various locations within the structure of the decimation filter to ensure that the output codes from the decimation unit 118 align with the decimated code words at the other microphone stages from audio signals received at different times at each of the other microphones.”

Id., [0025], Fig.1; *see also id.*, [0088], Figs.4, 11.



Ex.1005, Fig.1 (annotated). This further follows from the fact that decimator 114 is the only decimation element in decimator unit 118, and decimator 118 is referred to in Adams as a “decimation filter.” *Id.*, [0025], [0052], Fig.1; *see also id.*, [0088], Figs. 4, 11. Thus, it is my opinion that Adams discloses decimator 114, which is a filter configured to receive as an input, the time delayed oversampled digital output signal.

178. Adams further discloses that its decimator “may decimate the digital code words by first filtering...the ADC output codes before downsampling the codes.” Ex.1005, [0025]. Explaining further, Adams discloses that decimator 114 “reduce[s] the sampling rate of the digital code words outputted by the converter 112 so that the remaining digital code words correspond to the serial data stream frame rate.” *Id.*, [0028]. Thus, it is my opinion that Adams discloses that decimator 114 filters and decimates (to a lower sample rate) the time delayed oversampled digital output signal and outputs a filtered decimated delayed digital output signal, wherein the lower sample rate is less than the sampling clock frequency.

179. Even if Adams did not disclose or otherwise render obvious that the filtering performed by decimator 114 is “low pass” filtering, a POSA would have found it obvious to implement Adams’ decimation filter as low pass, at least in light of the teachings of Nguyen. *See supra* §§X.A-B.

180. First, decimation filters are (and would have been) generally low pass filters, as a POSA would have understood, in order to pass the desired relatively low frequency in-band signal and attenuate higher-frequency components in the signal, including out-of-band quantization noise, as well as to suppress aliasing in systems.

See supra §VI.D.

181. Second, Adams acknowledges that microphone-based systems, like its own, aim to reduce effects of “noise and other undesirable sounds”:

“Microphone arrays have been used to improve fidelity and reduce effects of ambient noise. Arrays of two or more microphones may be used to capture specific audio signals while reducing the effects of background noise and other undesirable sounds. Various beamforming algorithms may be used to combine the signals from each of the microphones in the array so that audio signals originating from a particular direction constructively interfere and generate a highest magnitude response over audio signals originating from other directions.”

Ex.1005, [0002]; *see also id.*, [0081]. In line with this aim, Adams specifies that its decimation element does not just downsample, but “first filter[s]” the incoming signal “before downsampling.” Ex.1005, [0025], claim 28. Like Adams, Nguyen³ discloses the use of a decimation filter in a microphone-based system to suppress higher frequency noise components, and expressly identifies the filter as a “lowpass

³ Adams and Nguyen share the same author, Robert Adams. Ex.1005, Inventors; Ex.1006, Inventors.

filter.” Ex.1006, [0035] (“The decimator 306 preferably comprises a lowpass filter 308 which may be...integrated with the decimator.”), [0037] (“unwanted” higher frequency components are attenuated by passing the...signal...through a combined lowpass filter and decimator []”).

182. In my opinion, a POSA configuring Adams’ decimation filter as low pass would have appreciated such configuration to be straightforward given the similarities in Adams and Nguyen. As an example, Adams and Nguyen both concern audio microphone signal processing systems; they are also disclosures from the same company and share the same inventor; their systems include many of the same components, as discussed above. Nguyen also teaches that its decimation filter provides decimation factors “between 16 and 128” (Ex.1006, [0035]), which is similar to factors taught by Adams. Ex.1005, [0090] (decimation factor of 16), [0088] (decimation factor of 128). Nguyen also teaches the use of its decimation filter to downsample from an ADC oversampled frequency to “a desired final sample rate for the outgoing digital audio stream” (Ex.1006, [0035]), which is similar to Adams which discloses downsampling from an ADC oversampled frequency to the digital “audio frame rate”:

“Embodiments of the invention provide a system having an array of microphone stages in which each of the microphone stages may be coupled together in a daisy chain. Each microphone stage may include a microphone, an analog to digital converter, a decimation unit, a receiver, an adder, and a transmitter. The analog to digital converter may

convert sampled audio signals from the microphone into digital codes. **The decimation unit may decimate digital codes from the analog to digital converter output to an audio frame rate of a serial interface used to transmit data between microphone stages.** The decimation unit may also include a delay unit to implement a delay at each microphone stage.”

Ex.1005, [0016]; *see also id.*, [0022], claims 3, 43. A POSA would have had expected success in the aforementioned combination of Adams’ and Nguyen’s teachings given that the proposed implementation merely applies Nguyen’s known decimation filter implementation teaching to Adams’ known decimation filter without changing Adams’ multiple time delay operations and structure. In my opinion, a POSA applying Nguyen’s well-known low-pass decimation filter teaching to Adams’ known decimation filter would have been no more than the predictable use of prior-art elements according to their established functions. *See supra* §§VI.D, X.A-B.

5. 11[d]: “a second time delay element, the second time delay element is configured to receive, as an input, the low pass filtered decimated delayed digital output signal and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times the lower sampling rate period, the integer delay is applied to the low pass filtered decimated time delayed digital output signal; and”

183. In my opinion, Adams in view of Nguyen renders this limitation obvious.

184. As an initial matter, as discussed in the Technical Background section above, the use of a time delay element to output a time-delayed digital output signal where the time delay is equal to an integer number of cycles of the sampling clock was widely known and broadly used long before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §§VI, VIII.

185. Referring specifically to the prior art cited in this section of my declaration, Adams discloses that its time delay system includes multiple time delay elements. Ex.1005, [0022]-[0029], Fig.1; *see also id.*, Figs.2-6. For example, Adams discloses that “[e]ach delay unit may have a delay selected to insure [sic] that the audio data from its associated microphone corresponding to sound from a particular direction is time-aligned with the data represented by the cumulative sum arriving at the receiver of that microphone stage.” *Id.*, [0022].

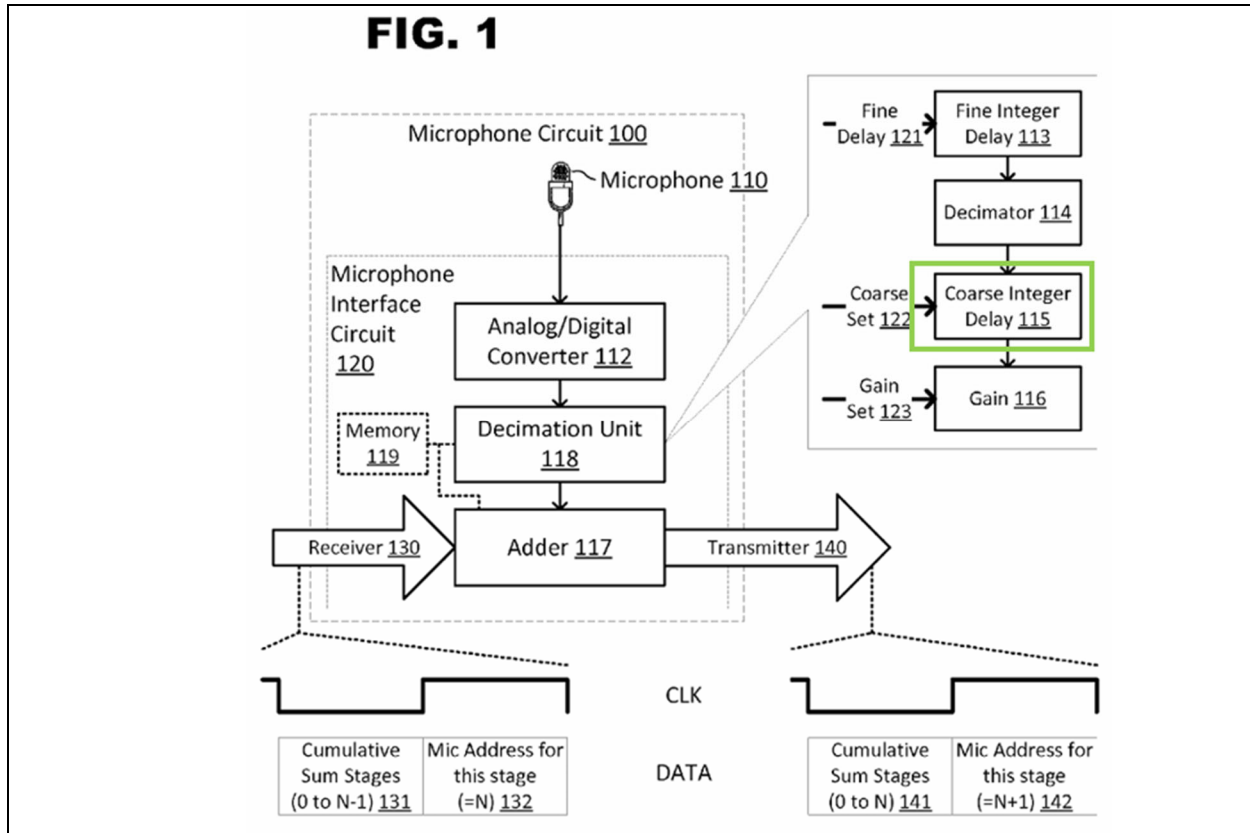
186. As discussed above, Adams discloses a first time delay element, which it refers to as “fine integer delay element 113.” *See supra* §X.C.3(11[b]).

187. Adams also discloses a second time delay element, which it refers to as “coarse variable integer delay element 115.” *See, e.g.,*

“A coarse variable integer delay 115 may be coupled to the output of the decimator 114. The coarse variable integer delay 115 may include a coarse delay input 122, which may be used to select a whole number of clock cycles of the serial data stream frame clock to delay the decimated code words.”

Ex.1005, [0029], Fig.1.

188. Adams discloses that this “coarse integer delay element 115 may be coupled to the output of the decimator 114.” *Id.*, [0029], Fig.1.



Ex.1005, Fig.1 (annotated).

189. As I discussed above, Adams-Nguyen’s decimator 114 outputs a low pass filtered decimated delayed digital output signal. *Supra* §X.C.4(11[c]). Given that the output of decimator 114 is connected to the input of coarse integer delay

115⁴ (*see* above disclosures in Adams, e.g., Ex.1005, [0029], Fig.1), coarse variable integer delay element 115 is configured to receive, as an input, the low pass filtered decimated delayed digital output signal.

190. Adams further discloses that “coarse variable integer delay 115 may include a coarse delay input 122, which may be used to select a whole number of clock cycles of the serial data stream frame clock to delay the decimated code words.” Ex.1005, [0029]. As a POSA would have understood, a “whole number” is an “integer.” *See, e.g.*, Ex.1014. p. 5 (Graf, 381) (“**integer** – A whole number, which may be positive, negative, or zero.”). Since the “decimated code words” received by coarse variable integer delay 115 is a low pass filtered decimated delayed digital output signal, the coarse variable integer delay 115 applies its integer delay to the low pass filtered decimated delayed digital output signal.

191. As I discussed above, Adams discloses “a whole number of clock cycles of the serial data stream frame clock” may be “select[ed]” “to delay the decimated code words.” Ex.1005, [0029]. A POSA would have understood that a whole number (i.e., integer) number of (serial data stream) clock cycles can also be

⁴ Adams uses the terminology “coarse integer delay 115,” “coarse integer delay element 115,” and “coarse variable integer delay 115” to refer to the same element. *See, e.g.*, Ex.1005, [0026], [0029], [0052], [0054], Figs.1, 4, 5.

expressed in time units, as the integer number of (serial data stream) clock cycles times the (serial data stream) clock period. *See also* Ex.1014, p. 8 (Graf, 547) (**period**... 1. The time required for one complete cycle of a regular, repeating signal, function, or series of events.”).

192. As a POSA would have understood, the “serial data stream frame clock” is a lower sample rate than the oversampled rate of the ADC because it is the rate to which the decimator 114 reduces (or decimates) the oversampled rate of the ADC. Ex.1005, [0028] (“The decimator 114 may be used to reduce the sampling rate of the digital code words outputted by the converter 112 so that the remaining digital code words correspond to the serial data stream frame rate.”).

193. Thus, consistent with these disclosures, it is my opinion that coarse integer delay element 115 imparts an integer delay to the low pass filtered decimated time delayed digital output signal where the integer delay is an integer number of cycles at the lower sample rate times the lower sampling rate period.

194. Thus, it is my opinion that Adams in view of Nguyen renders claim element 11[d] obvious.

6. 11[e]: “a controller, the controller is configured to supply a control signal to set the fractional delay and the integer delay.”

195. In my opinion, Adams discloses this limitation. Also, it is my opinion that Adams renders this limitation obvious.

196. As an initial matter, the use of a controller to supply a control signal to set a time delay was widely known and broadly used long before the earliest claimed priority date of the '055 patent. *See, e.g.,* Ex.1007, [0033] (“The delay controller 28 is a processor, control processor, digital signal processor, application specific integrated circuit, field programmable gate array, analog circuit, digital circuit, look-up table, memory, or combinations thereof. The controller 28 controls the output of the memory 16. The controller 28 selects stored data from the memory 16 as a function of a delay for the beam.”), Ex.1008, Abstract (“the delay device (6) being controllable by the at least one signal processor”), 3:31-37 (“In one of the microphone channels a controllable delay device 6 is included. This delay device is typically a multiple tap shift register and the control signal coming from the DSP 5 will decide how many 1 bit stages each sample of the bit stream will go through (and thus be delayed by) before they are tapped and sent furtheron [sic] in the system, in this case to the digital low pass filter and decimator 4.”), 3:43-45, 3:52-56, Figs.3-4; Ex.1012, p. 8 (“[T]he delay values of the different PDM streams are adjusted by the control block in such a way that the focus of the sensor points to the correct direction.”), p. 9; Ex.1005, [0022], [0027], [0029], [0034], [0043], [0045], [0047] (“The command code word 162 may specify a command that the addressed microphone circuit 161 is to execute. These commands may specify instructions such as setting a digital delay 118,”), [0050] (“[T]he amount of delay to

be applied may be calculated in advance and then encoded into the data words 163 associated with respective set delay commands 162 for each microphone address 161.”), [0050] (“[T]he data word 163 may be set to ‘10001000’ (corresponding to the decimal number 136), to specify a delay value of 136 cycles associated with the set delay command 162 for the last microphone in the array.”).

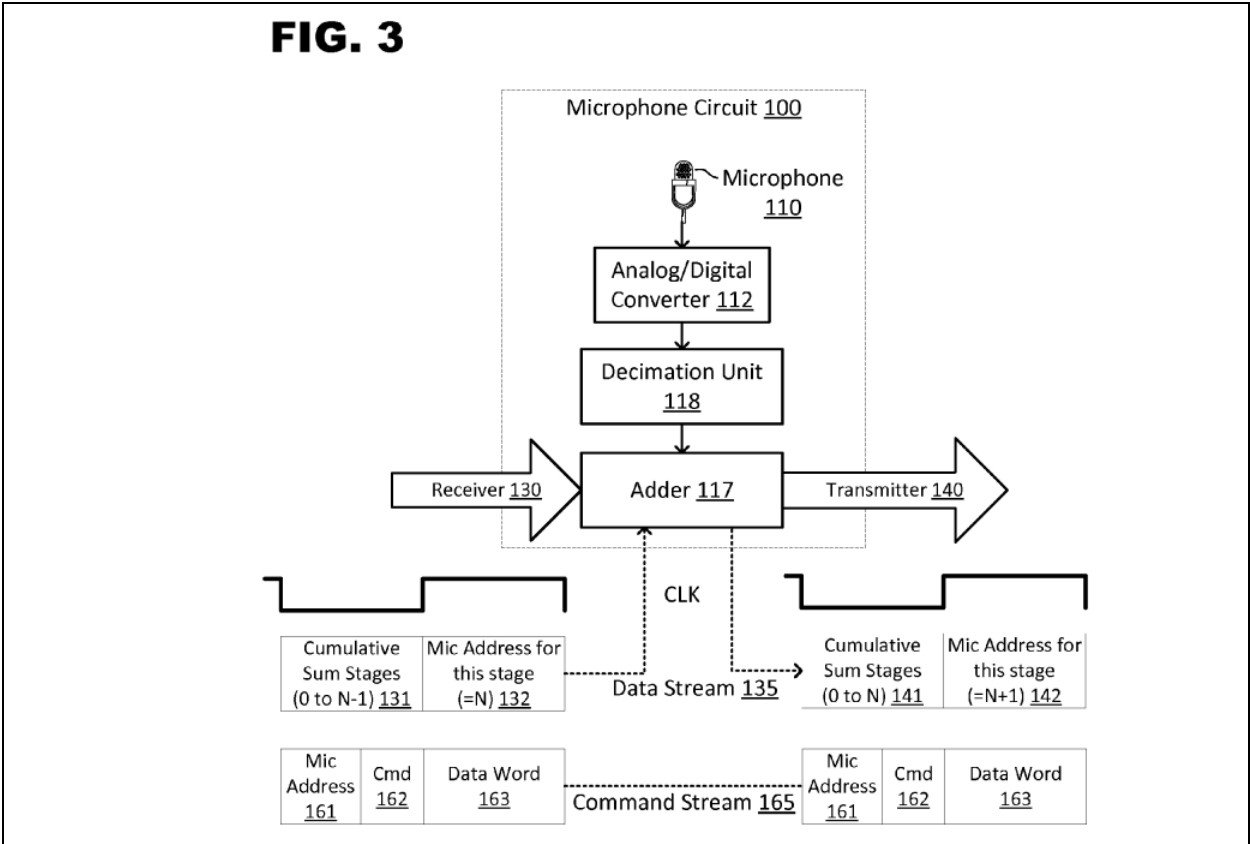
197. Referring specifically to the prior art cited in this section of my declaration, Adams discloses that its time delay system includes multiple time delay elements or units. *See supra* §§X.C.3(11[b]), 5(11[d]). These delay elements include a first time delay element (Adams’ fine variable integer delay 113) that provides the fractional delay, and a second time delay element (Adams’ coarse variable integer delay 115) that provides the integer delay. *See supra* §§X.C.3(11[b]), 5(11[d]).

198. In addition, Adams further discloses that “[e]ach delay unit may have a delay selected.” Ex.1005, [0022]. More specifically, Adams discloses that “[t]o achieve precise **control**,...it may be necessary **to set both an integer as well as a fractional part of the delay.**” *Id.* (emphasis added). This ability to control both the integer and fractional time delays is, as Adams discloses, “to insure [sic] that the audio data from its associated microphone corresponding to sound from a particular direction is time-aligned with the data represented by the cumulative sum arriving at the receiver of that microphone stage.” *Id.*

199. As Adams further discloses, this delay control is implemented whereby both the fractional delay unit (*i.e.*, fine variable integer delay 113) and the integer delay unit (*i.e.*, coarse variable integer delay 115) have an control signal input—namely, a fine delay input 121 in the case of the fractional delay unit 113 that is “used to select a whole number of cycles at the higher frequency of the [ADC] 112 to delay the generated digital code words outputted by the converter 112” and a coarse delay input 122 in the case of the integer delay unit 115 that is “used to select a whole number of clock cycles of the serial data stream frame clock.” *Id.*, [0027], [0029]. In light of these teachings, a POSA would have understood that the signal input to the delay units to “set” the delay “[t]o achieve precise control over the steering direction” corresponds to the control signal for setting the time delays of the delay units.

200. Thus, in my opinion, the time delay control signal comprises the signals input to fine delay input 121 and coarse delay input 122 that are used to set the fractional and integer delays. *See* above discussion; Ex.1005, [0022] (“The integer and the fractional delays can be set using the configuration channel transmitted to each microphone.”), [0027], [0029]. The “inputs 121, 122, and 123 may be dynamically configured” or “predetermined” as “optimized based on the intended use of the microphone array.” *Id.*, [0034].

201. Further, Adams discloses that “the amount of delay to be applied may be calculated in advance and then encoded into the data words 163 associated with respective set delay commands 162 for each microphone address 161.” Ex.1005, [0050]. This total delay is sent to the delay units via the “command stream channel 165.” *Id.*, [0043], [0045].



Ex.1005, Fig.3.

202. Adams also discloses that “command stream channel 165 may be used to transmit configuration data and commands to each of the microphone circuits 100 in the array. The packets transmitted over the command stream channel 165 may be formatted to include a microphone address 161, a command

code word 162, and a data word 163.” Ex.1005, [0045]. The “command code word 162 may specify a command that the addressed microphone circuit 161 is to execute,” such as “specify[ing] instructions such as setting a digital delay 118.” Ex.1005, [0047]. “The data word 163 may specify a value associated with the command code word 162. For example, the value specified in data word 163 may be an amount of delay...that is to be set.” *Id.*, [0048]. Accordingly, the control signal to set the fractional delay and integer delay (e.g., those fine delay 121 and coarse delay 122 inputs) would have been understood by a POSA to be included in this command signal that is comprised of command code word 162 specifying a command that the addressed microphone circuit 161 is to execute,” (e.g., such as “specify[ing] instructions such as setting a digital delay 118”) and data word 163 (e.g., such as specifying “an amount of delay...that is to be set.”). The element sending this configuration data and commands over the command stream channel 165 corresponds to the controller configured to supply a control signal to set the fractional delay and the integer delay, as a POSA would have understood. That understanding is also consistent with the disclosure of the ’055 patent. More specifically, the ’055 patent discloses the control signal being send by a “control element.” For example, the ’055 patent discloses:

“In some embodiments, **a controller 818 provides a control signal 820 to the time delay element 808.** In some embodiments, when the time delay element **816** is configured with the system,

the controller **818** or a separate controller provides a control signal at **822** to the time delay element **816**.

In various embodiments, the time delay element such as **808** can be configured as a buffer or to include a buffer which has a number of values, where each value corresponds to a different number of clock cycles of the sampling clock used within the digital sensor **804**. In various embodiments, the time delay element **808** can be configured to provide a fixed time delay to the input digital signal **806** or the time delay element **808** can be programmable. **In operation, the controller 818 provides a control signal 820 which is used to specify a number of sampling clock cycles which will be used by the time delay element 808 to provide the time delay to the input signal 806.**

Similarly, when present in the system, the time delay element such as **816** can be configured as a buffer or to include a buffer which has a number of values, where each value corresponds to a different number of cycles at the lower sample rate corresponding to the output of the PDM receiver module **812**. In various embodiments, the time delay element **816** can be configured to provide a fixed time delay to the input digital signal **814** or the time delay element **816** can be programmable. **In operation, the controller 818 provides a control signal 822 which is used to specify a number of cycles at the lower sample rate which will be used by the time delay element 816 to provide the time delay to the input signal 814.** Thus, the total time delay imparted by the system at the output **822** relative to the input **806** is the sum of the time delay imparted by the time delay element **808** and the time delay element **816**.”

Ex.1001, 10:50-11:16 (emphasis added).

“A controller **904** is used to adjust time delay(s), which are used to delay each of the microphone signal paths.

In operation, a time delay Δt_1 is associated with the digital signal output at **912** for the digital microphone **920**. Similarly, a time delay Δt_2 is associated with the digital signal output at **914** for the digital microphone **940**. And a time delay Δt_n is associated with the digital

signal output at **916** for the digital microphone **960**. A controller **904** is used to supply one or more control signals to each signal path **906**, **908**, up to **910**. As described above in the preceding figures, a control signal **922** supplied to a time delay element **924** is used to specify a time delay applied by the time delay element **924** to the oversampled digital signal received from the microphone **920**. Optionally, the controller **904** can supply a control signal **928** to a time delay element **930** (if present in a given system configuration). Similarly, a control signal **942** supplied to a time delay element **944** is used to specify a time delay applied by the time delay element **944** to the oversampled digital signal received from the microphone **940**. Optionally, the controller **904** can supply a control signal **948** to a time delay element **950** (if present in a given system configuration). Control signals are supplied as need to successive microphone signal paths, and finally within microphone signal path **910** a control signal **962** supplied to a time delay element **964** which is used to specify a time delay applied by the time delay element **964** to the oversampled digital signal received from the microphone **960**. Optionally, the controller **904** can supply a control signal **968** to a time delay element **970** (if present in a given system configuration).”

Id., 11:27-57 (emphasis added).

“In various embodiments, the controller **904** is used to steer the array of microphones **920**, **940**, through **960** as needed in order to perform beamforming with the time delayed microphone signals **912**, **914**, through **916**. As described in FIG. 9A, a general number of *n* microphones has been described; however, beamforming can be performed with as few as two microphones as described below in conjunction with FIG. 10.”

Id., 12:7-16.

“In various embodiments, the controller **904** is used to steer the array of signals obtained from the single microphone **920** as needed in order to perform beamforming with the time delayed microphone signals **912** through **916**.”

Id., 13:4-7.

“With reference to **1500**, a first integrated circuit die **1502** includes the digital sensor **804** and time delay element **808**; a second integrated circuit die **1504** includes one or more of the PDM receiver module **812**, time delay controller **818**, and time delay element **816**. In some embodiments the second integrated circuit die **1504** does not include time delay controller **818** and time delay element **816**. PDM receiver module **812** together with one or more of time delay controller **818** and time delay element **816** can also be referred to as an Application Processor. In another non-limiting embodiment, as illustrated by the example of FIG. 8 and FIG. 15B, the components of the system are implemented in more than one integrated circuit die. With reference to **1550** a first integrated circuit die **1502** includes the digital sensor **804**; a second integrated circuit die **1504** includes the PDM receiver module **812**, the time delay element **808**, and one or more of the time delay controller **818**, and time delay element **816**. In some embodiments the second integrated circuit die **1504** does not include time delay controller **818** and time delay element **816**. PDM receiver module **812** and time delay element **808** together with one or more of time delay controller **818** and time delay element **816** can also be referred to as an Application Processor.”

Id., 16:45-17:1.

203. Even if the above-described disclosure did not disclose the recited “controller,” Adams, in my opinion, have been rendered such feature obvious. For example, Adams discloses a “microcontroller” that may calculate values of parameters (e.g., gain) and send to the respective circuit 100 element (e.g., amplifier/gain) to set/control the element. Ex.1005, [0087]:

“The microcontroller may calculate a subsequent gain **1030** to be applied to each of the variable amplifiers **1011** based on the identified highest audio level. The calculated gain **1030** may then be sent to a gain

set input of each variable amplifier **1011** coupled to the microcontroller.”

204. Additionally, gain is an element on the same circuit 100 as fine variable integer delay 113 and coarse variable integer delay 115 are on. Ex.1005, [0023], [0026], [0047]-[0048], [0066], [0073], [0087], Fig.1.

205. Furthermore, the gain control signal like the delay control signal (including fine delay input 121 and coarse delay input 122) is provided via command stream channel 165. *Id.*, [0045] (“The command stream channel **165** may be used to transmit configuration data and commands to each of the microphone circuits **100** in the array. The packets transmitted over the command stream channel **165** may be formatted to include a microphone address **161**, a command code word **162**, and a data word **163**.”), [0047] (describing that the “command code word 162 may specify a command that the addressed microphone circuit 161 is to execute,” “such as **setting a digital delay 118**, setting a gain, ... **or setting an analog preamplifier gain.**”) (emphasis added), [0048] (describing that the “data word 163 may specify a value associated with the command code word 162. For example, **the value specified in data word 163 may be an amount of delay or gain that is to be set.**”) (emphasis added), Figs.1-3.

206. Additionally, the gain control signal has the same format—including “a microphone address 161, a command code word 162, and a data word 163”—as the delay control signal. *See*:

Ex.1005, [0045]:

“The packets transmitted over the command stream channel **165** may be formatted to include a microphone address **161**, a command code word **162**, and a data word **163**.”

Id., [0046]:

“The microphone address **161** may specify the assigned address of the microphone circuit **100** for which the corresponding command code word **162** and data word **163** is intended.”

Id., [0047] (emphasis added):

“The command code word **162** may specify a command that the addressed microphone circuit **161** is to execute. These commands may specify instructions **such as setting a digital delay 118, setting a gain, bypassing a microphone circuit, muting a microphone, or setting an analog preamplifier gain.**”

Id., [0048] (emphasis added):

“The data word **163** may specify a value associated with the command code word **162**. For example, **the value specified in data word 163 may be an amount of delay or gain that is to be set.**”

207. It is my opinion that a POSA would have been motivated to use Adams’ microcontroller to provide the delay control signal. There are several reasons for this. First, the controller already exists in Adams’ system, and in fact, also already provides a control signal to the same circuit 100 on which the delay elements (fine

variable integer delay 113 and coarse variable integer delay 115) reside. Therefore, using the already existing controller to provide control signals to the delay elements (fine variable integer delay 113 and coarse variable integer delay 115) would predictably offer efficiency. A separate controller would not need to be developed and manufactured, which therefore would lead to cost savings. Not having a separate controller, but controlling both delay and gain using the same controller would further provide space savings. Those efficiencies resulting from using the same microcontroller to provide both gain and delay control signals, would have been consistent with and furthered Adams' aims, in my opinion. *See* Ex.1005, [0003] (speaking negatively of "require[d] additional expense and space" using other approaches).

208. Second, the existing controller provides control signals having the same format as the control signals used to control delay. *See* Ex.1005, [0045]-[0048] discussed above. Thus, using the same controller to provide both delay and gain control signals would have resulted in further efficiencies, as the controller is already configured to output control signals have the same format as would have been used to control delay

209. It is also my opinion that a POSA would have had a reasonable expectation of success in the aforementioned implementation. This is because first, as discussed above, Adams already discloses the microcontroller providing a gain

control signal. Thus, the microcontroller is already established to send control signals in Adams' system. Second, as also discussed above, Adams already discloses the microcontroller providing a control signal to circuit 100, and further discloses control signal input ports for fine integer delay 113 and coarse integer delay 115, on the same circuit 100. Thus, the microcontroller already has an established interface with circuit 100, and could predictably provide further control signals to other elements on the circuit 100, for which control signal input ports already are established. Third, Adams discloses that the gain control signal provided by the microcontroller is provided via command stream channel 165, which is the same channel 165 along which the delay control signal is provided, as already disclosed by Adams, as discussed above. Fourth, the format of the gain control signal provided by the microcontroller is the same format as the delay control signal, as discussed above.

D. Claim 12

- 1. “The system of claim 11, wherein the digital sensor utilizes a sigma-delta modulator and the oversampled digital output signal is a pulse density modulated (PDM) signal.”**

210. In my opinion, a POSA would have found claim 12 obvious based on Adams in view of Nguyen.

211. As I explained above, it is my opinion that a POSA would have found claim 11 obvious based on Adams in view of Nguyen. *Supra* §X.C(claim 11).

212. As a first matter and as explained in the Technical Background section above, digital sensors utilizing a sigma-delta modulator to output an oversampled pulse density modulated (PDM) signal were well known long before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §§VI.C, VI.E.

213. Referring specifically to the prior art cited in this section of my declaration, Adams discloses a digital sensor in the form of a digital microphone, as discussed above. *See supra* §X.C.2(11[a]).

214. Nguyen similarly disclosed a digital microphone comprised of a microphone sensor and follow-on analog-to-digital converter. *See, e.g.,* Ex.1006, [0006]-[0008]; *see also id.*, [0001] (disclosing that its sensor and follow-on ADC “generate[s]” a “digital transducer signal”), [0004] (disclosing “generation of” a “digital transducer signal”).

215. Nguyen specifies that its microphone, which generate[s] a “digital transducer signal,” comprises a MEMS sensor followed by a circuit comprising a sigma-delta modulator ADC (*id.*, [0007]-[0008], [0030] (“sigma- delta modulators **110, 112** are oversampled converters operating at an oversampled sampling rate or frequency which may lie between 2.4 MHz and 10 MHz”), and further that the output is a pulse density modulated “PDM” signal. *See:*

“Each of the first and second sigma-delta modulators may comprise a single-bit quantizer or a multi-bit quantizer with their respective well-known advantages and disadvantages. If each of the

first and second sigma-delta modulators comprises the single-bit or one bit quantizer the first and second digital signals may be conveniently supplied as first and second PDM signals, respectively.”

Ex.1006, [0012] (emphasis added); *see also id.*, [0013], claim 20 (“sigma delta analog to digital converters ($\Sigma\Delta$ ADCs)”), claim 33 (same), claims 21-25, 27-31, 34-40, 42-43 (“ $\Sigma\Delta$ ADCs”). As Nguyen also discloses, the “circuit 100” which includes the follow-on sigma-delta modulator ADC, “may be shaped and sized for integration into a miniature MEMS microphone housing or package.” *Id.*, [0028].

216. Nguyen further discloses that its “sigma-delta modulators preferably operate[] at an oversampled sampling frequency.” *Id.*, [0012], [0030]. Thus, it is my opinion that Nguyen discloses that its digital sensor utilizes a sigma-delta modulator and outputs an oversampled digital output signal that it is a pulse density modulated (PDM) signal, as recited in claim 12.

217. Thus, even if Adams did not disclose or otherwise render obvious that the digital sensor utilizes a sigma-delta modulator and the oversampled digital output signal is a pulse density modulated (PDM) signal, it would, in my opinion, have been obvious to provide such an implementation in Adams’ system in light of Nguyen’s teachings. *See supra* §§X.A-B.

218. First, a POSA implementing Adams would have been motivated to combine the teachings of Adams with those of Nguyen to arrive at a structure where

the microphone sensor was a MEMS sensor and the ADC was a sigma-delta modulator ADC, as taught by Nguyen. This follows from the fact that Adams and Nguyen have similar aims. A POSA would have also understood that both Adams and Nguyen seek to reduce the assembly costs and space required to implement its digital microphones. For example, Adams expresses a desire to reduce space consumption and costs, and improve reliability (Ex.1005, [0003]-[0004]). Adams addresses its desire for reduced space consumption and costs, and improve reliability with a staged daisy chain approach reducing the number of wires in its system. *See id.*, [0016], [0081], [0006], Fig.2. Nguyen similarly recognized the same problem/need as Adams and taught a solution which implemented a MEMS sensor integrated with a follow-on circuit 100 comprising a sigma-delta modulator ADC. *See* above discussion. Such integration provided a number of advantages, as taught by Nguyen, such as “reduce[d] space consumption and lower[ed] assembly costs.” Ex.1006, [0002]-[0003], [0028]. Additionally, Nguyen discloses that its integration offered “reduce[d] power consumption of active circuitry,” (Ex.1006, [0002]-[0003]), which Adams also acknowledges would have benefits. Ex. 1005, [0067], [0094]. Further, Nguyen, filed approximately two years after Adams, teaches that such MEMS sensors were “[c]ommonly used” by that time, “shaped and sized for portable audio devices such as smartphones, tablets and mobile phones etc.,” and “integra[ble] into a miniature MEMS microphone housing or package.” Ex.1006,

[0006]-[0007], [0028]. Sigma-delta modulator ADC usage in digital signal processing was also prevalent and well known. *See supra* §§VI.C, E. Given the overlapping aims of Adams and Nguyen, as well as Nguyen's solution resulting in the integration of the MEMS microphone sensor and follow-on sigma-delta modulator ADC, the combination of Adams and Nguyen would provide the abovementioned benefits in Adams' system, in line with Adams' aims. In my opinion, this combination would have had a number of beneficial results, including saving space, reducing assembly costs, improving reliability, and facilitating integrability in Adams' system, in line with Adams' aims, and Nguyen's teachings.

219. Second, a POSA combining the teachings of Adams and Nguyen, as described above, would have had a reasonable expectation of success given just how closely related Nguyen's and Adams' disclosures are. For example, both concern audio microphone signal processing systems from the same company and share the same inventor. The two systems also include many of the same components, and with respect to the relevant features here, the more recent (Nguyen) publication provides more specificity regarding the type of digital microphone sensor (*i.e.*, MEMS) and analog-to-digital converter (*i.e.*, sigma-delta modulator) utilized than the slightly earlier (Adams) publication. These similarities would have facilitated the aforementioned combination.

220. A POSA would have had a reasonable expectation of success because the proposed implementation merely applies Nguyen's teachings regarding a known digital microphone utilizing a MEMS sensor integrated with a sigma-delta modulator ADC to Adams' known digital microphone without changing Adams' multiple time delay operations and structure. Additionally, the combination simply involves the use of prior art elements, e.g., MEMS sensors and sigma-delta modulators, according to their well-known functions, and draws these elements from a pair of patent publications that include overlapping authorship, and are assigned to ADI, which has the technical capabilities and existing products supporting success.

E. Claim 13

- 1. "The system of claim 11, wherein the oversampled digital output signal is a pulse density modulated (PDM) signal."**

221. In my opinion, a POSA would have found claim 13 obvious based on Adams in view of Nguyen.

222. As I explained above, it is my opinion that a POSA would have found claim 11 obvious based on Adams in view of Nguyen. *Supra* §X.C(claim 11).

223. It is further my opinion that a POSA would have found claim 13 obvious based on the disclosure of Adams in view of Nguyen for the same reasons I discussed above for claim 12. *See supra* §X.D(claim 12).

F. Claim 14

1. “The system of claim 11, wherein the digital sensor is a digital microphone.”

224. In my opinion, a POSA would have found claim 14 obvious based on Adams in view of Nguyen.

225. As I explained above, it is my opinion that a POSA would have found claim 11 obvious based on Adams in view of Nguyen. *Supra* §X.C(claim 11).

226. Both Adams and Nguyen (as well as the combination Adams in view of Nguyen) disclose that the digital sensor is a digital microphone, as I discussed above for claim element 11[a] and claim 12. *Supra* §§X.C.2(11[a], X.D(claim 12).

G. Claim 15

1. “The system of claim 14, wherein the digital microphone utilizes a micro-electromechanical systems (MEMS) sensor.”

227. In my opinion, a POSA would have found claim 15 obvious based on Adams in view of Nguyen.

228. As I explained above, it is my opinion that a POSA would have found claim 14 obvious based on Adams in view of Nguyen. *Supra* §X.F(claim 14).

229. As a first matter, and as explained in the Technical Background section above, MEMS sensors were well known and used in digital microphones long before the earliest claimed priority date of the '055 patent. *See supra* §VI.E.

230. Referring specifically to the prior art cited in this section of my declaration, Adams discloses a digital sensor in the form of a digital microphone, as discussed above. *See supra* §X.C.2(11[a]).

231. Nguyen similarly discloses a digital microphone comprised of a sensor and follow-on analog-to-digital converter. *See, e.g.*, Ex.1006, [0006]-[0008]; *see also id.*, [0001] (disclosing that its sensor and follow-on ADC “generate[s]” a “digital transducer signal”), [0004] (disclosing “generation of” a “digital transducer signal”).

232. Nguyen further specifies that its digital microphone “may comprise a micro-electromechanical (MEMS) transducer element, e.g. shaped and sized for portable audio devices such as smartphones, tablets and mobile phones etc.” *Id.*, [0007]. Thus, Nguyen discloses that the digital microphone utilizes a MEMS sensor, as recited in claim 15 of the ’055 patent.

233. Even if Adams did not disclose or otherwise render obvious that the digital microphone utilizes a micro-electromechanical systems (MEMS) sensor, it would, in my opinion, have been obvious to provide such an implementation in Adams’ system in light of Nguyen’s teachings. *See supra* §§X.A-B.

234. First a POSA implementing Adams would have been motivated to combine the teachings of Adams with those of Nguyen to arrive at a structure where the microphone sensor was a MEMS sensor and the ADC was a sigma-delta

modulator ADC, as taught by Nguyen, as discussed above for claim 12. *See supra* §X.D.

235. A POSA combining the teachings of Adams and Nguyen, as described above, would have had a reasonable expectation of success given just how closely related Nguyen's and Adams' disclosures are. For example, both concern audio microphone signal processing systems from the same company and share the same inventor. The two systems also include many of the same components, and with respect to the relevant features here, the more recent (Nguyen) publication provides more specificity regarding the type of digital microphone sensor (*i.e.*, MEMS) and analog-to-digital converter (*i.e.*, sigma-delta modulator) utilized than the slightly earlier (Adams) publication. These similarities would have facilitated the aforementioned combination. A POSA would have also appreciated that ADI, where both references originated, was already well-known for success at development of digital MEMS devices, and would have the experience and resources to implement the combination of Adams and Nguyen. Nguyen also recognizes that "MEMS capacitive microphones" were "[c]ommonly used" by that time, "shaped and sized for portable audio devices such as smartphones, tablets and mobile phones etc.," and "integra[ble] into a miniature MEMS microphone housing or package." Ex.1006, [0006]-[0007], [0028].

236. Further, a POSA would have had a reasonable expectation of success because the proposed implementation merely applies Nguyen’s teachings regarding a known digital microphone utilizing a MEMS sensor integrated with a sigma-delta modulator ADC to Adams’ known digital microphone without changing Adams’ multiple time delay operations and structure. Additionally, the combination simply involves the use of prior art elements, e.g., MEMS sensors and sigma-delta modulators, according to their well-known functions, and draws these elements from a pair of patent publications that include overlapping authorship, and are assigned to ADI, which has the technical capabilities and existing products supporting success.

H. Claim 16

1. “The system of claim 11, wherein the analog field quantity is an acoustic pressure field.”

237. In my opinion, a POSA would have found claim 16 obvious based on Adams in view of Nguyen.

238. As I explained above, it is my opinion that a POSA would have found claim 11 obvious based on Adams in view of Nguyen. *Supra* §X.C(claim 11).

239. As I also discussed above in claim element 11[a], Adams discloses a digital sensor in the form of a “digital microphone,” as does Nguyen (and Adams-Nguyen). *See supra* §X.C.2(11[a]). As further discussed above, a “microphone,” as a POSA would have understood, is responsive to an analog field quantity, namely sound or acoustic pressure. *See supra* §X.C.2(11[a]); *see also* Ex.1005, [0002]

(“microphones may be used to capture specific audio signals”), [0022] (“audio data from its associated microphone corresponding to sound”), claim 21 (reciting that the system includes “a delay unit in each microphone stage...to time-align sound”); *see also* Ex.1014, pp. 7, 10 (Graf, 471, 714). In my opinion, that understanding is consistent with the disclosure of the ’055 patent, which describes, as an example, an analog field relating to sound. *See supra* §X.C.2(11[a]); Ex.1001, 6:4-6, 1:30-33, 7:24-25, 10:34-37, 11:19-23, 12:18-21, 13:17-21, 5:42-47, 14:20-30, Figs.8, 9A-9B, 10.

I. Claim 17

- 1. “The system of claim 11, wherein the integer number of sampling clock cycles is selected from a range of one to the sampling clock frequency divided by a baseband sample rate.”**

240. In my opinion, a POSA would have found claim 17 obvious based on Adams in view of Nguyen.

241. As I explained above, it is my opinion that a POSA would have found claim 11 obvious based on Adams in view of Nguyen. *Supra* §X.C(claim 11).

242. As an initial matter, the ’055 patent simply recites the claimed range of “one to the sampling clock frequency divided by a baseband sample rate” without further explanation and does not provide any description that the specific claimed range is critical. In addition, the ’055 patent provides no evidence that the claimed

range produces a new or unexpected result, and given this, the claimed range cannot form the basis of patentability in light of the teachings of Adams.

243. Turning to the prior art at issue here, as I discussed above, Adams discloses that the first delay element, namely fine variable integer delay 113, delays the digital signals output from ADC by an integer number (*i.e.*, a “whole number”) of sampling clock cycles times the sampling clock period. *Supra* §X.C.3(11[b]). Adams further discloses that this integer number of sampling clock cycles is “select[ed].” Ex.1005, [0027] (“fine integer delay 113 may include a fine delay input 121, which may be used to select a whole number of cycles at the higher frequency of the analog to digital converter 112 to delay the generated digital code words outputted by the converter 112.”).

244. Adams identifies the delay implemented by the first delay element (*i.e.*, fine variable integer delay 113) as a “fractional” time delay. *See* Ex.1005, [0022] (“[I]t is possible to use the higher frequency clock rates used in the oversampling analog-to-digital converters to implement the fractional part of the delay,”); *see also id.*, [0089] (“if the fractional delay is associated with the original ADC output sample rates [], it would be possible to select a fractional delay amount”). By “fractional,” Adams means a fraction of an audio frame rate period (*i.e.*, serial data stream rate period). *See, e.g.*, Ex.1005, [0022] (“To achieve precise control over the steering direction, **the delay at each microphone node may need to be adjusted**

in finer steps than can be accomplished by using an integer number of sample-periods, and therefore it may be necessary to set both an integer as well as a fractional delay amount. In these conditions it is possible to use the higher frequency clock rates used in the oversampling analog-to-digital converters to implement the fractional part of the delay, and the integer part of the delay can be implemented at the lower sample rates that correspond to the audio frame rate. The integer and the fractional delays can be set using the configuration channel transmitted to each microphone.”) (emphasis added). As I discuss further below, the audio frame rate (i.e., serial data stream rate) corresponds to the claimed “baseband sample rate,” and the audio frame rate period (i.e., serial data stream rate period) corresponds to the baseband sampling period.

245. Following the fine variable integer delay 113 element, the signal sampling rate is decimated “to reduce the sampling rate of the digital code words outputted by the converter 112 so that the remaining digital code words correspond to the serial data stream frame rate.” Ex.1005, [0028], [0060]; *supra* §X.C.4(11[c]).

246. Adams describes that the “serial data stream frame rate” (also referred to as the “audio frame rate”—*see* Ex.1005, [0016], [0022], claims 3, 43)—is the rate at which “audio data and configuration data” is transmitted “between...each of the microphone stages” (i.e., microphone circuits 100). *Id.*, [0020], [0032], [0033]; *see also id.*, Abstract (“A serial interface may be used to connect the transmitters and

receivers of each of the stages.”), [0016], [0024] (providing example of “44 kHz” as rate used to transmit data between microphone circuits 100); Figs.1-5. Audio is the application of interest in Adams’ system, and the “audio frame rate” (i.e., “serial data stream frame rate”) is the rate or frequency of that application of interest. *See, e.g.,* Ex.1005, Abstract, [0002], [0016]. Adams’ post-decimation “serial data stream frame rate” output is a baseband sample rate. In my opinion, that understanding is consistent with the disclosure of the ’055 patent, which describes a receiver module that low-pass filters and decimates an oversampled digital signal to output a baseband digital signal at a baseband sampling rate. Ex.1001, 3:55-3:67, 6:22-39.

Ex.1001 (’055 patent), 3:55-67:

“The output signal from the delay element 216 is a delayed oversampled digital signal 218 which is input into a receiver module 220. The receiver module 220 performs the functions of low pass filtering and decimation. Low pass filtering removes the high frequency noise resulting from the oversampling process and decimation reduces the sampling frequency to a baseband sampling rate. A baseband digital signal is output at 222 from the receiver module 220. The baseband signal 222 is a digital signal having a bandwidth as prescribed by an application of interest and, depending on the digitization methodology, an increased dynamic range relative to the oversampled digital signal 214 output from the digital sensor 212.”

Ex.1001 (’055 patent), 6:22-39:

“Some baseband audio signal applications have established frequency ranges and these ranges together with a desired dynamic range for the audio signal place requirements on the sampling clock frequency used to with the digital microphone 272. For example, telephony, compact

disk (CD) format, etc. all have requirements for the baseband audio signal that can be accommodated through embodiments of the invention as described herein. Some non-limiting examples are, for example, pulse code modulated (PCM) audio which can be provided at various dynamic ranges and sample rates, which could be provided at 16 bits per sample at 48 kHz in one or more embodiments. Another non-limiting example is 16 bit CD quality stereo PCM at 44.1 kHz. Telephony can be accommodated at different specifications. A non-limiting example is PCM audio at 12 bits per sample at 8 kHz. The foregoing examples of baseband audio formats are provided merely for example and do not limit embodiments of the invention.”

247. Given that the signal sampling rate before decimation is the sampling clock frequency (i.e., the sampling clock frequency of the ADC – *see supra* §§X.C.3-4), and the sampling rate after decimation is the serial data stream frame rate (i.e., the baseband sample rate), the decimation factor is the sampling clock frequency divided by the serial data stream frame rate (or in other words, the sampling clock frequency divided by the baseband sample rate). *See id.*; *see also* Ex.1005, Fig.11 (disclosing “ADC output” sampling rate as “(x) Hz,” a “decimate-by-16” stage having a “(x/16) Hz”).

248. Adams further discloses the use of the delay provided by fine variable integer delay 113 (i.e., “fractional” time delay) is “[t]o achieve precise control over the steering direction.” Ex.1005, [0022]. Adams explains that the fractional time delay allows the delay to be adjusted in finer steps than the integer delay (which, as explained above, is provided by the coarse variable integer delay 115 and equals a

whole number of periods of the serial data stream frame rate (i.e., baseband sample rate). *See*:

“To achieve precise control over the steering direction, the delay at each microphone node may need to be adjusted in finer steps than can be accomplished by using an integer number of sample-periods, and therefore it may be necessary to set both an integer as well as a fractional delay amount. In these conditions it is possible **to use the higher frequency clock rates used in the oversampling analog-to-digital converters to implement the fractional part of the delay**, and the integer part of the delay can be implemented at the lower sample rates that correspond to the audio frame rate.”

Id. (emphasis added).

249. Thus, the fractional delay, which corresponds to “the integer number of sampling clock cycles” is generally intended to be a finer (or smaller) delay than a period of the baseband sample rate, as discussed. Specifically, the fractional delay is generally intended to correspond to a fraction of a baseband sample rate period.⁵

250. In fact, in instances where “precise control over the steering direction” is desired to be “achieve[d]”, as described in Adams (*see, e.g.*, Ex.1005, [0022]), the fractional delay would have been set. The finest increment of fractional delay that may be set, when such “precise” delay is desired or required (*id.*), was one sampling

⁵ In contrast, the integer delay (corresponding to the delay provided by the coarse variable integer delay 115) is an integer number of baseband sample rate periods. *See* above discussion; *see also* Ex.1005, [0022]; *supra* §§X.C.4(11[c])-5(11[d]).

clock cycle (which corresponds to the smallest “whole number” (i.e., one) of sampling clock cycles).

251. As a POSA would have understood, one period of the baseband sample rate includes a number of sampling clock periods (i.e., sampling periods of the ADC) equal to the decimation factor (i.e., sampling clock frequency divided by the baseband sample rate), as discussed above. *See also* Ex.1005, [0089] (“the decimation factor [of 128] indicates that 128 samples of the original ADC output code may cycled through in same time as one sample of the serial data stream”).

252. Adams discloses an example where a decimation factor of 128 is employed. Ex.1005, [0088]. Regarding this example, Adams explains that “it would be possible to select a fractional delay amount in increments of 1/128th the sample rate of the serial data stream.” *Id.*, [0089]. In other words, with such decimation, there are 128 fractional delay steps within one sample (or one period) of the serial data stream. *Id.* Thus, a one sampling clock cycle selection, as discussed above, is within claim 17’s recited range of one to the sampling clock frequency divided by the baseband sample rate (i.e., 128). Thus, it is my opinion that Adams in view of Nguyen renders obvious the system of claim 11, wherein the integer number of sampling clock cycles is selected from a range of one to the sampling clock frequency divided by a baseband sample rate.

J. Claim 18

1. “The system of claim 13, wherein the filter is a PDM receiver.”

253. In my opinion, a POSA would have found claim 18 obvious based on Adams in view of Nguyen.

254. As I explained above, it is my opinion that a POSA would have found claim 13 obvious based on Adams in view of Nguyen. *Supra* §X.E(claim 13).

255. As I also discussed above, it is my opinion that Adams in view of Nguyen renders obvious “a filter, the filter is configured to receive as an input the time delayed oversampled digital output signal, the filter to low pass filter and to decimate to a lower sample rate the time delayed oversampled digital output signal and to output a low pass filtered decimated delayed digital output signal, wherein the lower sample rate is less than the sampling clock frequency.” *See supra* §X.C.4(11[c]). Thus, in the Adams-Nguyen system, the filter is configured to receive, as input, the time delayed oversampled digital output signal. *See id.*

256. This time delayed oversampled digital output signal input into the filter, in the Adams-Nguyen system, is a PDM signal. This follows from the fact that, as I discussed above, the oversampled digital output signal that is output by the digital sensor is a pulse density modulated (PDM) signal in the Adams-Nguyen system. *See supra* §X.E(claim 13). In fact, Nguyen teaches that where the sigma-delta modulator ADC comprises a “single-bit or one bit quantizer,” its digital output “may be

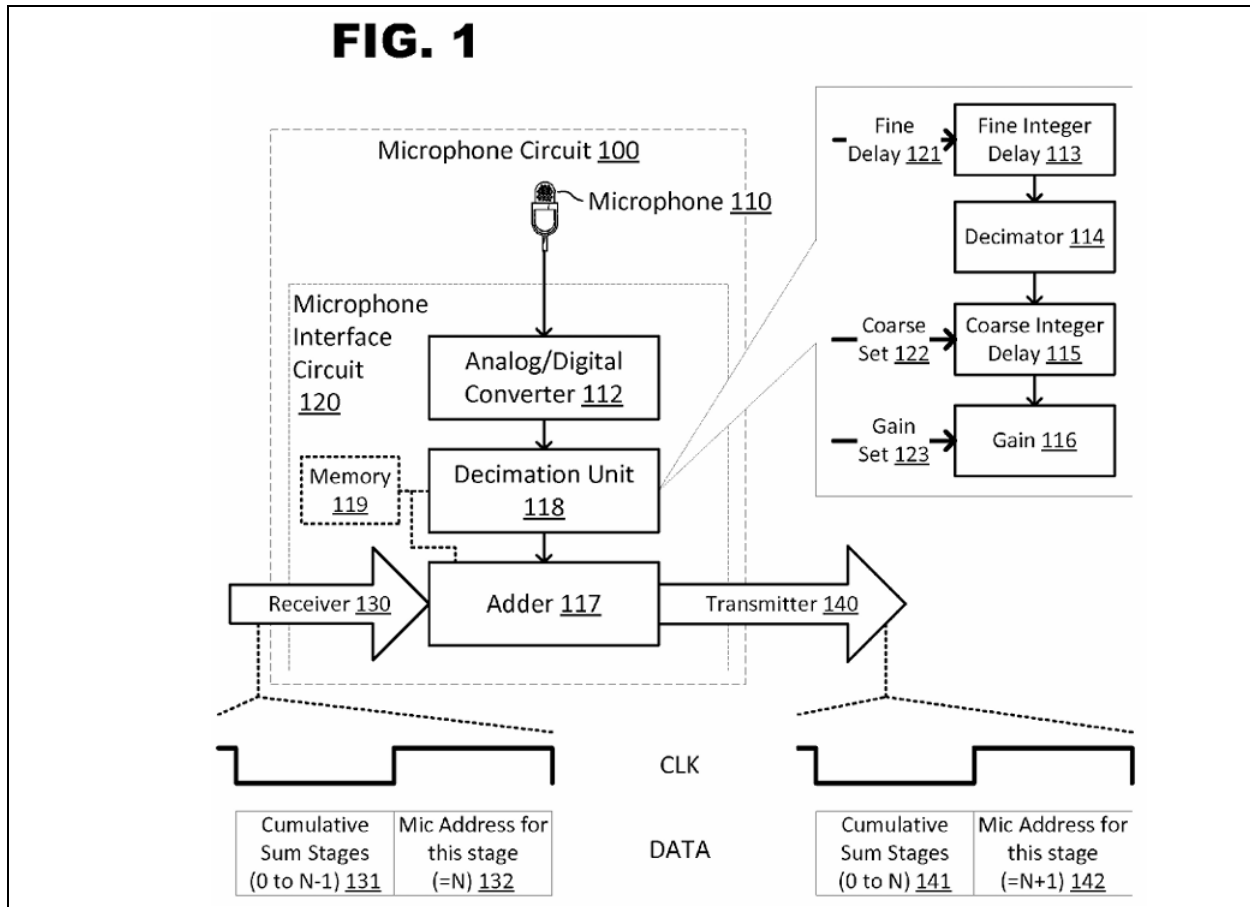
conveniently supplied as [a] PDM signal[.]” Ex.1006, [0012]. This PDM signal (output by the ADC of the digital sensor) is input to the fine variable integer delay 113, given that the digital sensor’s ADC output is coupled to the input of fine variable integer delay 113, and thus receives the oversampled digital signal from the ADC.⁶ See Ex.1005, [0027] (“A fine variable integer delay 113 may be coupled to the analog to digital converter 112.”), Fig.1; *see also id.*, [0059] (“A fine variable integer delay unit 113 may be coupled to the converter 112 to delay the digital output from the converter [] an integer number of converter clock cycles.”), Figs.4-5.

257. The fine variable integer delay 113 time delays the PDM signal input and thus outputs a time delayed PDM signal. See *supra* §X.E(claim 13); Ex.1005, [0027] (“A fine variable integer delay 113 may be coupled to the analog to digital converter 112. The fine variable integer delay 113 may include a fine delay input 121, which may be used to select a whole number of cycles at the higher frequency of the analog to digital converter 112 to **delay the generated digital code words outputted by the converter []**.”) (emphasis added), Fig.1; *see also id.*,

⁶ As I discussed above for claim 13, the Adams-Nguyen system includes a sigma-delta modulator ADC within the digital sensor that outputs a pulse density modulated (PDM) signal. See *supra* §X.E(claim 13).

[0059] (“A fine variable integer delay unit 113 may be coupled to the converter 112 to delay the digital output from the converter [] an integer number of converter clock cycles.”), Figs.4-5.

258. Given that the input to the filter in the Adams-Nguyen system is coupled to the output of the fine variable integer delay 113 (*see, e.g.*, Ex.1005, [0027] (“A decimator 114 may be coupled to the output of the fine variable integer delay 113.”); *supra* §X.C.4(11[c])), the filter receives, as input, the time delayed PDM signal that is output by the fine variable integer delay 113. The filter low pass filters and decimates to a lower sample rate the time delayed PDM signal. *See supra* §X.C.4(11[c]). In fact, Nguyen teaches that the digital microphone signal is received and processed by a decimation filter (decimator 306) which “comprises a lowpass filter 308” to reduce its sample rate and produce a lower-rate “outgoing digital audio stream.” Ex.1006, [0035].



Ex.1005, Fig.1.

259. Accordingly, Adams-Nguyen discloses/suggests that the filter is a PDM receiver. In my opinion, that understanding is consistent with the disclosure of the '055 patent, which describes elements, such as a low pass decimation filter, that receives a PDM signal, including after time delay, as a PDM receiver. *See, e.g.,* Ex.1001, 7:20-8:45, 9:43-10:55, Figs.3, 5-8.

K. Claim 21

- 1. “The system of claim 17, wherein the lower sample rate is a baseband sample rate and the low pass filtered decimated time delayed digital output signal is used in a beam forming process with a second signal, wherein the second signal is a digital measurement of the analog field quantity.”**

260. In my opinion, a POSA would have found claim 21 obvious based on Adams in view of Nguyen.

261. As I explained above, it is my opinion that a POSA would have found claim 17 obvious based on Adams in view of Nguyen. *Supra* §X.I(claim 17).

262. Adams also discloses that decimator 114 “reduce[s] the sampling rate of the digital code words outputted by the converter 112 so that the remaining digital code words correspond to the serial data stream frame rate.” Ex.1005, [0028].

263. As I discussed above, the “serial data stream frame rate” is a lower sample rate. *See supra* §X.C.4(11[c]).

264. As I also discussed above, the serial data stream frame rate is a baseband sample rate. *See supra* §X.I(claim 17).

265. The Adams-Nguyen system further discloses the low pass filtered decimated time delayed digital output signal, as discussed in claim elements 11[c] and 11[d]. *Supra* §X.C.4-5(11[c]-[d]).

266. The low pass filtered decimated time delayed digital output signal is used in a beamforming process with a second signal. To explain, the low pass

filtered decimated time delayed digital signal from filter 114 is further delayed by coarse variable integer delay 115 (*supra* §X.C.5(11[d])) and then, at adder 117, is combined with an output code from another microphone stage. Ex.1005, [0029]-[0031]. Adams discloses an array of microphone stages. *See* Ex.1005, [0031], Fig.2. “[E]ach microphone stage in the microphone array may add its output code to that of the prior stages to eventually create a single cumulative beamformed output code.” *See*:

Ex.1005, [0031] (emphasis added):

“An adder 117 may be coupled to the output of the decimation unit 118. **The adder 117 may add the output of the decimation unit 118 to a cumulative sum 131 of prior microphone circuit stages 0 to N-1 (assuming the microphone stage 100 in FIG. 1 is the Nth stage) that is received 130 at the data stream input.** After the adder 117 adds the output of the decimation unit 118 to the cumulative sum 131, the resulting sum may then be transmitted 140 as a new cumulative sum 141 of microphone stages 0 to N to the next microphone stage N+1. **Thus, each microphone stage in the microphone array may add its output code to that of the prior stages to eventually create a single cumulative beamformed output code.**”

See also id., [0064], [0080], [0037]-[0039], Fig.2.

267. Thus, the low pass filtered decimated time delayed digital output signal of one respective microphone stage of the Adams-Nguyen system is used in a beamforming process with at least one other low pass filtered decimated time

delayed digital output signal (e.g., a second signal) of another respective microphone stage. *See id.* The result is a “a single cumulative beamformed output code.” *Id.*

268. The low pass filtered decimated time delayed digital output signal (e.g., a second signal) of another respective microphone stage is a digital measurement of the analog field quantity. This follows from the fact that Adams discloses that each respective microphone stage includes a microphone circuit 100 comprising a microphone 110 and follow-on analog-to-digital converter (ADC). *See* Ex.1005, [0016]; Fig.1; *see also id.*, Figs.2-6. This microphone and follow-on ADC “generate digital code words from the analog audio signal obtained from the microphone.” *Id.*, [0023].

269. These digital code words output from each stage’s ADC correspond to a digital measurement of the analog field quantity (e.g., sound or acoustic pressure). Ex.1005, [0002], [0022] (“audio data from its associated microphone corresponding to sound”), claim 21. More specifically, as a POSA would have understood, a microphone is responsive to sounds (or acoustic pressure), an analog field quantity, which is a continuously varying analog signal that the microphone senses and converts into a corresponding electrical signal. *See also* Ex.1014, pp. 7, 10 (Graf, 471, 714); *supra* §X.C.2(11[a]). In my opinion, that understanding is consistent with the disclosure of the ’055 patent, which describes, as an example, an analog field relating to sound. E.g., Ex.1001, 6:4-6 (“The MEMS digital microphones can be

configured with a sigma-delta modulator which produces an oversampled digital output of the **analog signal sensed by the microphone**)” (emphasis added); *see also id.*, 1:30-33 (“Field quantities which exist in the natural world are generally analog signals which have continuously varying amplitude as a function of time. Examples of these field quantities are sound pressure, vibration, light, etc.”), 7:24-25 (“An analog field quantity e.g., an acoustic field 302 is sensed by a digital microphone 304.”), 10:34-37 (“FIG. 8 illustrates, generally at 800, programmable time delay in an analog-to-digital converter (ADC) system, according to embodiments of the invention. With respect to FIG. 8, an analog field quantity is represented by 802 incident on a digital sensor 804, which in various embodiments, is a digital microphone,...”), 11:19-23 (“With respect to FIG. 9A, an analog field quantity is represented by 902, which is incident on digital sensors 920, 940, up to a general number of n sensors indicated by 960, which in various embodiments is a digital microphone,...”), 12:18-21 (“With respect to FIG. 9B, an analog field quantity is represented by 902, which is incident on a digital sensor 920, which in various embodiments is a digital microphone, vibration sensor, electromagnetic energy sensor, etc. “), 13:17-21 (“With respect to FIG. 10, an analog field quantity is represented by 1002, which is incident on digital sensors 1004 and 1006. In one or more embodiments, the digital sensors 1004 and 1006 are digital

microphones...”), 5:42-47, 14:20-30, Figs.8, 9A-9B, 10 (analog field quantity 802/902/1002).

270. The digital signal output by each stage’s ADC, which again is a digital measurement of the analog field quantity, is subjected to delay and low pass decimation filtering to create a respective low pass filtered decimated time delayed digital output signal before the signal addition process at adder 117 where the respective stage “add[s] its output code to that of the prior stages to eventually create a single cumulative beamformed output code.” *See supra* §X.C(claim 11); *see also* Ex.1005, [0023]-[0031], Figs.1-2.

271. Thus, it is my opinion that Adams-Nguyen renders obvious the “system of claim 17, wherein the lower sample rate is a baseband sample rate and the low pass filtered decimated time delayed digital output signal is used in a beam forming process with a second signal, wherein the second signal is a digital measurement of the analog field quantity.”

L. Claim 22

272. It is my opinion that a POSA would have found claim 22 obvious based on Adams in view of Nguyen (“Adams-Nguyen”).

1. 22[pre]: “A system to time delay signals, comprising:”

273. I have been asked to assume the preamble of claim 22 is limiting. Under that assumption, it is my opinion that Adams discloses claim 22’s preamble,

22[pre], which recites “[a] system to time delay digital signals, comprising,” for the reasons discussed above for claim element 11[pre]. *See supra* §X.C.1(11[pre]).

274. In my opinion, Adams discloses a system in which each microphone stage includes delay units that implement time delays on signals that had been converted from analog to digital form. Specifically, Adams discloses that “[e]ach delay unit may have a delay selected to insure [sic] that the audio data from its associated microphone corresponding to sound from a particular direction is time-aligned with the data represented by the cumulative sum arriving at the receiver of that microphone stage.” *See* Ex.1005, [0022]. Adams further explains that “[t]o achieve precise control over the steering direction, the delay at each microphone node may need to be adjusted in finer steps than can be accomplished by using an integer number of sample-periods, and therefore it may be necessary to set both an integer as well as a fractional delay amount.” *Id.* A POSA would have understood the use of the phrase “time-aligned” and the description of delays measured in sample periods makes clear that the delays described in Adams are time delays applied to digital signals. Such a skilled person would have also understood Adams’ delay units as implementing time delays.

275. Adams discloses a microphone circuit 100. Ex.1005, [0023]-[0031], Figs.1-5. The microphone circuit 100 includes a microphone, analog to digital

converter, decimation unit, among other elements. *Id.*, [0016]; Fig.1; *see also id.*, Figs.2-6.

276. The “analog to digital converter...may generate digital code words from the analog audio signal obtained from the microphone.” Ex.1005, [0023]. The “decimation unit...may also include a delay unit to implement a delay with one or more delay elements.” *Id.*, [0025], [0022], [0016], Fig.1(Decimation Unit 118 including fine integer delay 113 and coarse integer delay 115).

2. 22[a]: “a sensor element, the sensor element is responsive to an analog field quantity;”

277. In my opinion, Adams discloses this limitation. Also, it is my opinion that Adams in view of Nguyen renders this limitation obvious.

278. As an initial matter, as discussed in the Technical Background section above, systems that utilize a sensor responsive to an analog field quantity were widely known and used long before and at the time of the '055 patent's earliest claimed priority date. *See, e.g., supra* §§VI, VIII.

279. Referring specifically to the prior art cited in this section of my declaration, Adams discloses a microphone 110 sensor as part of its microphone circuit 100. Ex.1005, [0016]; Fig.1 (showing microphone 110), [0023]; *see also id.*, Figs.2-6 (showing microphone 110). Thus, Adams discloses a sensor in the form of microphone 110. Adams' microphone 110 is responsive to an analog field quantity (sound or acoustic pressure), as I discussed above. *See supra* §X.C.2(11[a]).

280. In the Adams-Nguyen system, the microphone sensor element is further specified as a MEMS microphone sensor. *See supra* §§X.D(claim 12), X.G(claim 15).

281. Adams-Nguyen's sensor (corresponding to Adams' microphone 110, further specified as a MEMS microphone sensor, in view of Nguyen's teachings) is responsive to an analog field quantity (e.g., sound or acoustic pressure). Ex.1005, [0002], [0022] ("audio data from its associated microphone corresponding to sound"), claim 21; Ex.1006, [0007] ("The MEMS capacitive microphone may comprise a micro-electromechanical (MEMS) transducer element....The electromechanical (MEMS) transducer element may function as a single element audio and ultrasonic microphone **responsive to both impinging audible sound and ultrasonic sound** due to its broad-band frequency response.") (emphasis added), [0027].

282. A POSA would have understood that a microphone is responsive to sounds (or acoustic pressure), an analog field quantity, which is a continuously varying analog signal that the microphone senses and converts into a corresponding electrical signal. *See supra* §X.C.2(11[a]); Ex.1014, pp. 7, 10 (Graf, 471, 714). In my opinion, that understanding is consistent with the disclosure of the '055 patent, which describes, as an example, an analog field relating to sound. E.g., Ex.1001, 6:4-6 ("The MEMS digital microphones can be configured with a sigma-delta

modulator which produces an oversampled digital output of the **analog signal sensed by the microphone**)” (emphasis added); *see also id.*, 1:30-33 (“Field quantities which exist in the natural world are generally analog signals which have continuously varying amplitude as a function of time. Examples of these field quantities are sound pressure, vibration, light, etc.”), 7:24-25 (“An analog field quantity e.g., an acoustic field 302 is sensed by a digital microphone 304.”), 10:34-37 (“FIG. 8 illustrates, generally at 800, programmable time delay in an analog-to-digital converter (ADC) system, according to embodiments of the invention. With respect to FIG. 8, an analog field quantity is represented by 802 incident on a digital sensor 804, which in various embodiments, is a digital microphone,...”), 11:19-23 (“With respect to FIG. 9A, an analog field quantity is represented by 902, which is incident on digital sensors 920, 940, up to a general number of n sensors indicated by 960, which in various embodiments is a digital microphone,...”), 12:18-21 (“With respect to FIG. 9B, an analog field quantity is represented by 902, which is incident on a digital sensor 920, which in various embodiments is a digital microphone, vibration sensor, electromagnetic energy sensor, etc.”), 13:17-21 (“With respect to FIG. 10, an analog field quantity is represented by 1002, which is incident on digital sensors 1004 and 1006. In one or more embodiments, the digital sensors 1004 and 1006 are digital microphones...”), 5:42-47, 14:20-30, Figs.8, 9A-9B, 10 (analog field quantity 802/902/1002).

3. **22[b]: “a sigma-delta modulator, the sensor element is electrically coupled to the sigma-delta modulator and is configured to produce a pulse density modulated (PDM) output signal at a sampling clock frequency responsive to the analog field quantity;”**

283. In my opinion, Adams in view of Nguyen renders this limitation obvious, consistent with my discussion above. *See supra* §X.D(claim 12).

284. As I discussed above, it is my opinion that Adams in view of Nguyen renders obvious “[t]he system of claim 11, wherein the digital sensor utilizes a sigma-delta modulator and the oversampled digital output signal is a pulse density modulated (PDM) signal.” *See supra* §X.D(claim 12). Thus, in the Adams-Nguyen system, the analog-to-digital converter (ADC) is a sigma-delta modulator that outputs an oversampled digital output signal that is a pulse density modulated (PDM) output signal, in light of the teachings of Nguyen. *See id.* The PDM signal is at a sampling clock frequency of the sigma-delta modulator. *See id.*; Ex.1006, [0012], [0030]. Adams-Nguyen thus discloses a sigma-delta modulator, which serves as the ADC, with the sigma-delta modulator configured to produce a pulse density modulated (PDM) output signal as a sampling clock frequency.

285. As I also discussed above, Adams discloses a sensor element in the form of microphone 110. *See supra* §X.L.2(22[a]). In the Adams-Nguyen system, the microphone 110 sensor element is further specified as a MEMS microphone sensor. *See supra* §§X.D(claim 12), X.G(claim 15). Electrical signals (the “analog

audio signal”) travel from the sensor element (microphone element) to the ADC. Ex.1005, [0024] (“The microphone...may be coupled to an [ADC] 112 that may generate digital code words from the analog audio signal obtained from the microphone 110.”). This sensor element is followed by the ADC; sends electrical signals to the ADC; is integrated with the ADC; and accordingly is coupled (both physically coupled and electrically coupled) to the ADC. *See supra* §X.C.2(11[a]); *see also* Ex.1005, [0023] (“The microphone and/or preamplifier may be coupled to an analog to digital converter 112 that may generate digital code words from the analog audio signal obtained from the microphone 110.”), Fig.1 (showing microphone 110 and follow-on ADC 112), Ex.1006, Abstract (describing sigma-delta modulators “configured to sample and quantize the amplified transducer signal”), [0001] (same), [0004] (same), [0006], [0007] (“**The transducer signal may accordingly be generated by one of the above mentioned microphone devices. The MEMS capacitive microphone may comprise a micro-electromechanical (MEMS) transducer element**, e.g. shaped and sized for portable audio devices such as smartphones, tablets and mobile phones etc. The electromechanical (MEMS) transducer element may function as a single element audio and ultrasonic microphone responsive to both impinging audible sound and ultrasonic sound due to its broad-band frequency response”) (emphasis added), [0027]. Again, in the Adams-Nguyen system, the ADC is further specified as a

sigma-delta modulator that outputs an oversampled PDM output signal at a sampling clock frequency. *See supra* §§X.D(claim 12), X.G(claim 15). Thus, there is physical coupling between the MEMS microphone and the sigma-delta modulator ADC, and electrical coupling between the MEMS microphone and the sigma-delta modulator ADC, as electrical signals travel from the MEMS microphone to the sigma-delta ADC.

286. As I also discussed above, Adams-Nguyen's sensor (corresponding to Adams' microphone 110, further specified as a MEMS microphone sensor, in view of Nguyen's teachings) is responsive to an analog field quantity (e.g., sound or acoustic pressure). *See supra* §X.L.2(22[a]). The analog signal detected by the microphone 110 sensor, further specified as a MEMS microphone sensor (in view of Nguyen's teachings), is converted to a digital signal by the ADC (which is further specified as a sigma-delta modulator, in view of Nguyen's teachings) and outputs a PDM signal at a sampling clock frequency responsive to the analog field quantity.

4. **22[c]: “a first time delay element, the first time delay element is electrically configured to receive the PDM output signal, and to output a delayed PDM output signal, wherein the delayed PDM output signal is delayed by a fractional time delay equal to a number of cycles of the sampling clock frequency times a period of the sampling clock;”**

287. In my opinion, Adams in view of Nguyen renders this limitation obvious, consistent with my discussion above. *See supra* §§X.C.3(11[b]), X.D(claim 12), X.E(claim 13).

288. As I discussed above, Adams discloses a first time delay element (fine variable integer delay 113), the first time delay element is configured to receive as an input the oversampled digital output signal from the ADC and to output a time delayed oversampled digital output signal, wherein the time delayed oversampled digital output signal is time delayed by a fractional delay, the fractional delay is equal to an integer number of sampling clock cycles times the sampling clock period. *See supra* §X.C.3(11[b]).

289. As I also discussed above, in the Adams-Nguyen system, the oversampled digital output signal (from the ADC) is a PDM output signal. *See supra* §X.L.3(22[b]). Thus, in the Adams-Nguyen system, the first time delay element (fine variable integer delay 113) is electrically configured to receive as an input the PDM output signal from the ADC and to output a time delayed PDM output signal, wherein the time delayed oversampled digital output signal is time delayed by a

fractional delay, the fractional delay is equal to an integer number of sampling clock cycles times the sampling clock period. *See id.; supra* §X.C.3(11[b]).

5. 22[d]: “a decimation module, the decimation module is configured to receive as an input the delayed PDM output signal, the decimation module to low pass filter and to decimate to a lower sample rate the delayed PDM output signal and to output a low pass filtered decimated delayed PDM output signal, wherein the lower sample rate is less than the sampling clock frequency, the decimation module to convert to pulse code modulation (PCM) format;”

290. In my opinion, Adams in view of Nguyen renders this limitation obvious, consistent with my discussion above. *See supra* §§X.C.4(11[c]), X.D(claim 12), X.E(claim 13).

291. As an initial matter, as discussed in the Technical Background section above, the use of a decimating filter to low pass filter and decimate to a lower sampling rate was widely known and used well before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §VI.D.

292. As I discussed above, Adams in view of Nguyen renders obvious “a filter, the filter is configured to receive as an input the time delayed oversampled digital output signal, the filter to low pass filter and to decimate to a lower sample rate the time delayed oversampled digital output signal and to output a low pass filtered decimated delayed digital output signal, wherein the lower sample rate is less than the sampling clock frequency.” *See supra* §X.C.4(11[c]). The filter in the

Adams-Nguyen system performs decimation and is thus a decimation module. *See id.*

293. As I also discussed above, in the Adams-Nguyen system, the oversampled digital output signal (from the ADC) is a PDM output signal. *See supra* §X.L.3(22[b]). Also, in the Adams-Nguyen system, the first time delay element is electrically configured to output a time delayed PDM output signal. *See supra* §X.L.4(22[c]).

294. As I also discussed above, in the Adams-Nguyen system, the input of the filter (decimation module) is “coupled to the output” of the first time delay element. *See supra* §X.C.4(11[c]); Ex.1005, [0028] (“decimator 114 may be coupled to the output of the fine variable integer delay 113”), Fig.1. Given that, and the fact that the first time delay element is electrically configured to output a time delayed PDM output signal, the decimation module is configured to receive as an input the delayed PDM output signal.

295. As I discussed above, in the Adams-Nguyen system, “the filter” (i.e., decimation module) is configured “to low pass filter and to decimate to a lower sample rate the time delayed oversampled digital output signal and to output a low pass filtered decimated delayed digital output signal, wherein the lower sample rate is less than the sampling clock frequency.” *See supra* §X.C.4(11[c]). Given that, and the fact that, in the Adams-Nguyen system, the time delayed oversampled digital

output signal is a time delayed PDM output signal, the Adams-Nguyen system's decimation module is configured to low pass filter and to decimate to a lower sample rate the time delayed PDM output signal and to output a low pass filtered decimated delayed PDM output signal, wherein the lower sample rate is less than the sampling clock frequency. *See supra* §X.C.4(11[c]).

296. Adams-Nguyen further renders obvious “the decimation module to convert to pulse code modulation (PCM) format,” as recited in 22[d]. To explain, the Adams-Nguyen system's decimation module low pass filters and decimates a time delayed PDM signal to a lower frequency, namely the “serial data stream frame rate.” *See supra* §X.C.4(11[c]); Ex.1005, [0028]. Adams further describes that that the “serial data stream frame rate” (also referred to as the “audio frame rate”—*see* Ex.1005, [0016], [0022], claims 3, 43)—is the rate at which “audio data and configuration data” is transmitted “between...each of the microphone stages” (i.e., microphone circuits 100). *Id.*, [0020], [0032]; *see also id.*, Abstract (“A serial interface may be used to connect the transmitters and receivers of each of the stages.”), [0016], [0024] (providing example of “44 kHz” as rate used to transmit data between microphone circuits 100); Figs.1-5. Nguyen further teaches PCM conversion, starting from the native single-bit sigma-delta “PDM” output (Ex.1006, [0012]; *supra* §§X.D-E(cls.12-13)), where “each of the...digital signals may be converted from native PDM format to a multi-bit or PCM format.” Ex.1006, [0012].

Thus, the Adams-Nguyen system's decimation module converts the PDM input into a pulse code modulation (PCM) format output, as a POSA would have understood. *See above; see also* Ex.1028 (T. Kite, "Understanding PDM digital audio," Audio Precision, Beaverton, OR, Tech. Rep., 2012), p. 8 ("**Converting PDM to PCM is more involved. The sample rate needs to be reduced by the oversampling factor. This is accomplished in a digital filtering operation called decimation.** Decimation is the counterpart to interpolation: samples are removed from the signal to reduce the sampling rate. It is important that the noise above the audio band in the 1-bit representation not be allowed to alias into the audio band. The decimation filters are designed to filter out this noise, leaving the baseband audio signal intact. **The output of the decimator is a PCM audio stream at the baseband (non-oversampled) rate.**"). This understanding is consistent with the disclosure of the '055 patent, which describes, a PDM signal input into a module that low pass filters and decimates, as being converted into a PCM format. E.g., Ex.1001, 6:49-55:

"The PDM receiver module 280 decimates and low pass filters the time delayed oversampled digital signal 278 and outputs a time delayed PCM baseband digital signal at 282. Those of ordinary skill in the art will recognize that PCM format is a digital data format in use with digital signals such as digital audio signals."

6. **22[e]: “a second time delay element, the second time delay element is configured to receive, as an input, the low pass filtered decimated delayed PDM output signal and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times a period at the lower sampling rate, the integer delay is applied to the low pass filtered decimated delayed PDM output signal; and”**

297. In my opinion, Adams in view of Nguyen renders this limitation obvious, consistent with my discussion above. *See supra* §§X.C.5(11[d]), X.D(claim 12), X.E(claim 13).

298. As I discussed above, Adams in view of Nguyen renders obvious “a second time delay element, the second time delay element is configured to receive, as an input, the low pass filtered decimated delayed digital output signal and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times the lower sampling rate period, the integer delay is applied to the low pass filtered decimated time delayed digital output signal.” *See supra* §X.C.5(11[d]).

299. As I discussed above for claims 12 and 13, the digital microphone output signal in the Adams-Nguyen system is a PDM signal. *See supra* §§X.D-E(cls.12-13). As I also discussed above for 22[c], the first time delay element (fine variable integer delay 113) receives as an input the PDM output signal from the ADC and outputs a time delayed PDM signal. *See supra* §X.L.4(22[c]). As I also discussed above for 22[d], in the Adams-Nguyen system, the output signal from the

decimation module is a low pass filtered decimated delayed PDM output signal. *See supra* §X.L.5(22[d]). Thus, in the Adams-Nguyen system, the second time delay element (coarse variable integer delay 115) is configured to receive as an input the low pass filtered decimated delayed PDM output signal, and to impart an integer delay, the integer delay is an integer number of cycles at the lower sample rate times the lower sampling rate period, the integer delay is applied to the low pass filtered decimated delayed PDM output signal. *Id.*; *see also supra* §X.C.5(11[d]). Thus, Adams in view of Nguyen renders 22[e] obvious in my opinion.

7. 22[f]: “a controller, the controller is configured to supply a control signal to set the fractional delay and the integer delay.”

300. In my opinion, Adams discloses and/or renders obvious this limitation for same reasons I discussed above for claim element 11[e]. *See supra* §X.C.6(11[e]).

M. Claim 34

1. “The system of claim 22, wherein the fractional time delay is equal to a fraction of a baseband sampling period.”

301. In my opinion, a POSA would have found claim 34 obvious based on Adams in view of Nguyen.

302. As I explained above, it is my opinion that a POSA would have found claim 22 obvious based on Adams in view of Nguyen. *Supra* §X.L(claim 22).

303. As I discussed above, Adams discloses that fine delay 113 provides fractional time delay. *See supra* §X.L.4(22[c]). Adams discloses that the fine delay (corresponding to claim 22’s “fractional time delay”) provided by “fine integer delay 113” may be “select[ed]” as “a whole number of cycles at the higher frequency of the analog to digital converter.”⁷ Ex.1005, [0027]; *supra* §X.L.4(22[c]). Thus, the fine delay is a whole number multiplied by the ADC (*i.e.*, sigma-delta modulator in Adams-Nguyen’s system) sampling period.

304. Adams identifies this delay implemented by fine integer delay 113 as a “fractional” time delay. *See* Ex.1005, [0022] (“[I]t is possible to use the higher frequency clock rates used in the oversampling analog-to-digital converters to implement the fractional part of the delay,”); *see also id.*, [0089] (“if the fractional delay is associated with the original ADC output sample rates [], it would be possible to select a fractional delay amount”); *see supra* §X.C.3(11[b]).

305. The Adams-Nguyen system’s decimation module low pass filters and decimates a time delayed PDM signal to a lower frequency, namely the “serial data

⁷ In the Adams-Nguyen system discussed for claim 22, the ADC is further specified as a sigma-delta modulator that outputs an oversampled PDM output signal at a sampling clock frequency. *See supra* §X.L(22[b]); *see also supra* §§X.D(claim 12), X.G(claim 15).

stream frame rate.” *See supra* §X.L.5(22[d]); Ex.1005, [0028]. This serial data stream frame rate is a baseband digital signal rate, as I discussed for claims 17 and 21. *See supra* §§X.I(claim 17), X.K(claim 21).

306. As a POSA would have understood, if one knows the sampling rate or frequency, the sampling period can be calculated. Specifically, the sampling period = (1 / sampling rate). Thus, the baseband sampling period = (1 / baseband sampling rate). The ADC sampling period = (1 / ADC sampling rate).

307. Thus, given that the ADC sampling rate in the Adams-Nguyen system is larger than the baseband sampling rate, the ADC sampling period is less than the baseband sampling period. In other words, the ADC sampling period is a fraction of the baseband sampling period.

308. The fractional delay is disclosed by Adams to equal a whole number of ADC sampling periods. *Supra* §X.L.4(22[c]). Given that an ADC sampling period is a fraction of the baseband sampling period, the fractional delay is equal to a whole number times a fraction of the baseband sampling period.

309. Adams further states that “[t]o achieve precise control over the steering direction, the delay at each microphone node may need to be adjusted in finer steps than can be accomplished by using an integer number of sample-periods, and therefore it may be necessary to set both an integer as well as a fractional delay amount.” Ex.1005, [0022]. Adams further states that “[i]n these conditions it is

possible to use the higher frequency clock rates used in the oversampling analog-to-digital converters to implement the fractional part of the delay, and the integer part of the delay can be implemented at the lower sample rates that correspond to the audio frame rate.” *Id.* (emphasis added).

310. In such an implementation, the fine delay (corresponding to claim’s 22’s “fractional delay” – *see supra* §X.L.4(22[c])) provided by fine variable integer delay 113 corresponds to the fractional part of the delay (i.e., fraction of baseband sampling period), in contrast to the coarse delay (corresponding to claim 22’s “integer delay” which corresponds to the integer part of the delay (i.e., whole number multiple of baseband sampling period) – *see supra* §X.L.6(22[e])). Thus, the fine delay is generally intended to be a fraction of a baseband sampling period, while the coarse delay corresponds to a whole number multiple of baseband sampling periods.

311. In fact, in instances where “precise control over the steering direction” is desired to be “achieve[d]”, as described in Adams (*see, e.g.*, Ex.1005, [0022]), the fractional delay would have been set. The finest increment of fractional delay that may be set, when such “precise” delay is desired or required (*id.*), was one sampling clock cycle (which corresponds to the smallest “whole number” (i.e., one) of sampling clock cycles).

312. As a POSA would have understood, one period of the baseband sample rate includes a number of sampling clock periods (i.e., sampling periods of the ADC)

equal to the decimation factor (i.e., sampling clock frequency divided by the baseband sample rate), as discussed above. *See also* Ex.1005, [0089] (“the decimation factor [of 128] indicates that 128 samples of the original ADC output code may cycled through in same time as one sample of the serial data stream”).

313. Adams discloses an example where a decimation factor of 128 is used. Ex.1005, [0088]; *supra* §X.I(claim 17). Regarding this example, Adams explains that “it would be possible to select a fractional delay amount in increments of 1/128th the sample rate of the serial data stream.” Ex.1005, [0089]. In other words, with such decimation, there are 128 fractional delay steps within one sample (or one period) of the serial data stream. *Id.* Thus, in line with Adams’ disclosure that any “whole number of cycles at the higher frequency of the” ADC sampling clock can be selected as the fractional delay, a one sampling clock cycle selection, as discussed above, is 1/128 of the baseband sampling period, and accordingly “a fraction of a baseband sampling period,” as recited in claim 34 of the ’055 patent.

N. Claim 38

314. It is my opinion that a POSA would have found claim 38 obvious based on Adams in view of Nguyen (“Adams-Nguyen”).

1. 38[pre]: “A method to delay digital signals, comprising:”

315. I have been asked to assume the preamble of claim 38 is limiting. Under that assumption, it is my opinion that Adams discloses claim 38’s preamble, 38[pre], which recites “[a] method to delay digital signals, comprising.”

316. In my opinion, Adams discloses a system in which each microphone stage includes delay units that implement time delays on signals that had been converted from analog to digital form. Use of such a system to delay digital signals involves performance of a method to delay digital signals. *See, e.g.,* Ex.1005, Claims 45 (“The method ... further comprising delaying the digital code until an audio signal represented in the digital code is time aligned with an audio signal represented in the cumulative sum of decimated digital codes from any prior microphones in the array.”), 46 (“The method ... wherein the delaying of the digital code includes at least one of delaying the digital code before the decimating and delaying the digital code after the decimating”), 47 (“The method ... wherein the delaying of the digital code includes initially delaying the digital code before the decimating and then delaying the digital code again after the decimating.”), 43; *see also supra* §X.C.

317. Specifically, Adams discloses that “[e]ach delay unit may have a delay selected to insure [sic] that the audio data from its associated microphone corresponding to sound from a particular direction is time-aligned with the data

represented by the cumulative sum arriving at the receiver of that microphone stage.” Ex.1005, [0022]. Adams further explains that “[t]o achieve precise control over the steering direction, the delay at each microphone node may need to be adjusted in finer steps than can be accomplished by using an integer number of sample-periods, and therefore it may be necessary to set both an integer as well as a fractional delay amount.” *Id.* A POSA would have understood the use of the phrase “time-aligned” and the description of delays measured in sample periods makes clear that the delays described in Adams are time delays applied to digital signals. Such a skilled person would have also understood Adams’ delay units as implementing time delays.

318. Adams discloses a microphone circuit 100. Ex.1005, [0023]-[0031], Figs.1-5. The microphone circuit 100 includes a microphone, analog to digital converter, decimation unit, among other elements. *Id.*, [0016]; Fig.1; *see also id.*, Figs.2-6.

319. The “analog to digital converter...may generate digital code words from the analog audio signal obtained from the microphone.” Ex.1005, [0023]. The “decimation unit...may also include a delay unit to implement a delay with one or more delay elements.” *Id.*, [0025] (“**The decimation unit 118 may include a delay unit with one or more delay elements 113 and/or 115 that may implement a delay using memory or storage units at various locations within the structure of the decimation filter to ensure that the output codes from the decimation**

unit 118 align with the decimated code words at the other microphone stages from audio signals received at different times at each of the other microphones”) (emphasis added), [0022], [0016], Fig.1(Decimation Unit 118 including fine integer delay 113 and coarse integer delay 115).

2. 38[a]: “sensing an analog field;”

320. In my opinion, Adams discloses this limitation.

321. As an initial matter, as discussed in the Technical Background section above, systems that utilize a sensor responsive to an analog field quantity, and thus involve sensing an analog field, were widely known and used long before the ’055 patent’s earliest claimed priority date. *See, e.g., supra* §§VI, VIII.

322. Referring specifically to the prior art cited in this section of my declaration, Adams discloses that its system includes a microphone that “obtain[s]” an “analog audio signal.” Ex.1005, [0023]. Microphones sense an analog field relating to sound. *Id.*, [0002] (“[M]icrophones may be used to capture specific audio signals while reducing the effects of background noise and other undesirable sounds.”), [0022] (“audio data from its associated microphone corresponding to sound”), claim 21; *see also supra* §X.L.2(22[a]); Ex.1014, pp. 7, 10 (Graf, 471, 714). In my opinion, that understanding is consistent with the disclosure of the ’055 patent, which describes, as an example, an analog field relating to sound. Ex.1001, 1:30-33 (“Field quantities which exist in the natural world are generally analog signals which

have continuously varying amplitude as a function of time. Examples of these field quantities are sound pressure, vibration, light, etc.”), 7:24-25 (“An analog field quantity e.g., an acoustic field 302 is sensed by a digital microphone 304.”), 10:34-37 (“FIG. 8 illustrates, generally at 800, programmable time delay in an analog-to-digital converter (ADC) system, according to embodiments of the invention. With respect to FIG. 8, an analog field quantity is represented by 802 incident on a digital sensor 804, which in various embodiments, is a digital microphone,...”), 11:19-23 (“With respect to FIG. 9A, an analog field quantity is represented by 902, which is incident on digital sensors 920, 940, up to a general number of n sensors indicated by 960, which in various embodiments is a digital microphone,...”), 12:18-21, 13:16-21, 14:20-30, Figs.8, 9A-9B, 10 (analog field quantity 802/902/1002).

3. 38[b]: “outputting an oversampled digital signal responsive to the sensing, wherein the oversampled digital signal is created at a sampling clock rate:”

323. In my opinion, Adams discloses this limitation.

324. As an initial matter, as discussed in the Technical Background section above, systems that output an oversampled digital signal responsive to sensing, and thus involved outputting an oversampled digital signal responsive to the sensing, wherein the oversampled digital signal is created at a sampling clock rate were widely known and used long before the '055 patent's earliest claimed priority date. *See, e.g., supra* §§VI, VIII.

325. Referring specifically to the prior art cited in this section of my declaration, Adams discloses that its system includes an analog-to-digital converter (ADC) that “may generate digital codes from the analog audio signal.” Ex.1005, [0023]. Further, Adams discloses that the ADC “oversample[s] the analog audio signal,” which is “obtained from the microphone,” at the sampling clock frequency of the ADC (the ADC’s oversampled clock rate, e.g. “higher frequencies, such as 2.4 MHz or higher”):

“FIG. 1 shows an exemplary block diagram of a microphone circuit 100 in an embodiment of the invention. A microphone 110 may be coupled to a microphone interface circuit 120, which may include a preamplifier (not shown) to initially boost an analog signal from the microphone, an analog to digital converter 112, decimation unit 118, and adder 117. **The microphone and/or preamplifier may be coupled to an analog to digital converter 112 that may generate digital code words from the analog audio signal obtained from the microphone 110.**

The analog digital converter 112 may oversample the analog audio signal at higher frequencies, such as 2.4 MHz or higher in some embodiments, than are used to transmit the serial audio data between microphone circuits 100 in the microphone array, which may transmit data at 44 kHz.”

Ex.1005, [0023]-[0024] (emphasis added); Figs.1-6; *see also id.*, [0022] (referring to “higher frequency clock rates used in the oversampling analog-to-digital converters”), [0028] (“sampling rate of the digital code words outputted by the converter **112**”). Since the analog audio signal is the signal generated by the microphone’s sensing of the analog field relating to sound, Adams discloses its ADC

112 outputting an oversampled digital signal responsive to the sensing, where the oversampled digital signal is created at the sampling clock rate.

4. **38[c]: “delaying the oversampled digital signal by a fractional time delay wherein the fractional time delay is equal to an integer number of sampling clock cycles to produce a delayed oversampled digital signal;”**

326. In my opinion, Adams discloses this limitation.

327. As an initial matter, as discussed in the Technical Background section above, the use of a time delay element to output a time-delayed oversampled digital output signal where the time delay is equal to an integer number of cycles of the sampling clock was widely known and broadly used well before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §§VI, VIII.

328. Referring specifically to the prior art cited in this section of my declaration, Adams discloses that its system includes a fine delay 113 following the ADC 112 for “delay[ing],” by “*a whole number of cycles* at the higher frequency of the analog to digital converter 112,” the “generated digital code words outputted by the converter 112.” Ex.1005, [0027] (emphasis added); Figs.1-6. As a POSA would have understood, a “whole number” is an “integer.” *See, e.g.,* Ex.1014. p. 5 (Graf, 381) (“**integer** – A whole number, which may be positive, negative, or zero.”). As I discussed for claim element 38[b], the ADC outputs an oversampled digital signal. *See supra* §X.N.3(38[b]). As I discussed for claim element 11[b], fine delay 113 outputs a time delayed oversampled digital output signal. *See supra* §X.C.3(11[b]).

329. Adams identifies the delay implemented by fine integer delay 113 as a “fractional” time delay. *See* Ex.1005, [0022] (“[I]t is possible to use the higher frequency clock rates used in the oversampling analog-to-digital converters to implement the fractional part of the delay,”); *see also id.*, [0089] (“if the fractional delay is associated with the original ADC output sample rates [], it would be possible to select a fractional delay amount”); *see supra* §X.C.3(11[b]).

330. Thus, it is my opinion that fine variable integer delay 113 is used to perform delaying the oversampled digital signal by a fractional time delay wherein the fractional time delay is equal to an integer number of sampling clock cycles to produce a delayed oversampled digital signal.

5. 38[d]: “applying a low pass filter with decimation to the delayed oversampled digital signal to output a baseband digital signal that is delayed by the fractional time delay; and”

331. In my opinion, Adams in view of Nguyen renders this limitation obvious.

332. As an initial matter, as discussed in the Technical Background section above, the use of a decimating filter to low pass filter and decimate to a lower sampling rate (including a baseband digital signal) was widely known and used well before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §VI.D.

333. Referring specifically to the prior art cited in this section of my declaration, Adams discloses that its system includes decimation filter 114 that

“reduce[s] the sampling rate of the digital code words outputted by the converter 112” which is at an oversampled rate, “so that the remaining digital code words correspond to the serial data stream frame rate.” Ex.1005, [0028]; Figs.1, 4. Adams’ post-decimation “serial data stream frame rate” output is a baseband sample rate. *Supra* §X.I(claim 17).

334. As I discussed for claim element 11[c], the input of the decimation filter “114 may be coupled to the output of the fine variable integer delay 113.” *See supra* §X.C.4(11[c]); Ex.1005, [0028]. As I also discussed above for 38[c], fine variable integer delay 113 outputs a time delayed oversampled digital signal. *See supra* §X.N.4(38[c]). As I also discussed above for 38[c], fine variable integer delay 113 provides a fractional time delay. *Id.*

335. Thus, it is my opinion that Adams discloses applying a filter with decimation (decimation filter 114) to the delayed oversampled digital signal to output a baseband digital signal (output from decimation filter 114) that is delayed by the fractional time delay.

336. Even if Adams did not disclose that the filtering performed by decimator 114 is “low pass” filtering, a POSA would have found it obvious to implement Adams’ decimation filter as low pass, at least in light of the teachings of Nguyen. *See supra* §§X.A-B, C.4(11[c]).

6. 38[e]: “delaying the baseband digital signal by an integer time delay, wherein the integer time delay is equal to a number of cycles at a baseband sampling rate times the baseband sampling rate period.”

337. In my opinion, Adams in view of Nguyen renders this limitation obvious.

338. As an initial matter, as discussed in the Technical Background section above, the use of a time delay element to output a time-delayed digital output signal where the time delay is equal to an integer number of cycles of the sampling clock was widely known and broadly used well before the earliest claimed priority date of the '055 patent. *See, e.g., supra* §VI.

339. Referring specifically to the prior art cited in this section of my declaration, Adams discloses that decimation filter 114 outputs a baseband digital signal. *Supra* §X.N.5(38[d]). Decimation filter 114 would have been low pass in view of the teachings of Nguyen, as discussed above. *See supra* §§X.A-B, C.4(11[c]).

340. Adams discloses that coarse delay 115 follows and is “coupled to” the decimation filter 114 for “delay[ing],” the “decimated code words” outputted by the decimator 114 by “a whole number of cycles of the serial data stream frame clock” (which is at the baseband sampling rate). Ex.1005, [0029]; Figs.1-6. As a POSA would have understood, a “whole number” is an “integer.” *See, e.g.,* Ex.1014. p. 5 (Graf, 381) (“**integer** – A whole number, which may be positive, negative, or zero.”).

Since the baseband digital signal is received by coarse variable integer delay 115, the coarse variable integer delay 115 applies its integer delay to the baseband digital signal. *See also supra* §X.C.5(11[d]) (integer delay is applied by coarse delay 115 to the signal input into coarse delay 115). Accordingly, coarse variable integer delay 115 delays the baseband digital signal by an integer number of cycles of the baseband clock. A POSA would have understood that a whole number (i.e., integer) number of baseband clock cycles can also be expressed in time units. Specifically, given that each baseband clock cycle has a duration of one period of the baseband sampling rate, the delay in time units equals an integer number of baseband clock cycles times the baseband sampling rate period. Thus, Adams discloses “delaying the baseband digital signal by an integer time delay, wherein the integer time delay is equal to a number of cycles at a baseband sampling rate times the baseband sampling rate period.”

O. Claim 39

- 1. “The method of claim 38, wherein the fractional time delay is equal to a fraction of a baseband sampling period.”**

341. In my opinion, a POSA would have found claim 39 obvious based on Adams in view of Nguyen. *See below; see also supra* §X.M(claim 34).

342. As I explained above, it is my opinion that a POSA would have found claim 38 obvious based on Adams in view of Nguyen. *Supra* §X.N(claim 38).

343. As I discussed above, Adams discloses that fine delay 113 provides fractional time delay. *See supra* §§X.L.4(22[c]), X.N.4(38[c]). Adams discloses that the fine delay (corresponding to claimed “fractional time delay”) provided by “fine integer delay 113” may be “select[ed]” as “a whole number of cycles at the higher frequency of the analog to digital converter.” Ex.1005, [0027]; *supra* §X.N.4(38[c]). Thus, the fine delay is a whole number multiplied by the ADC sampling period.

344. Adams identifies the delay implemented by fine integer delay 113 as a “fractional” time delay. *See* Ex.1005, [0022] (“[I]t is possible to use the higher frequency clock rates used in the oversampling analog-to-digital converters to implement the fractional part of the delay,”); *see also id.*, [0089] (“if the fractional delay is associated with the original ADC output sample rates [], it would be possible to select a fractional delay amount”); *see supra* §X.C.3(11[b]).

345. The Adams-Nguyen system’s filter low pass filters and decimates a time delayed oversampled digital signal to a lower frequency, namely the “serial data stream frame rate.” *See supra* §X.N.5(38[d]); Ex.1005, [0028]. This serial data stream frame rate is a baseband digital signal rate. *See supra* §§X.I(claim 17), X.K(claim 21).

346. As a POSA would have understood, if the sampling rate or frequency is known, the sampling period can be calculated. Specifically, the sampling period

= (1 / sampling rate). Thus, the baseband sampling period = (1 / baseband sampling rate). The ADC sampling period = (1 / ADC sampling rate).

347. Thus, given that the ADC sampling rate in the Adams-Nguyen system is larger than the baseband sampling rate, the ADC sampling period is less than the baseband sampling period. In other words, the ADC sampling period is a fraction of the baseband sampling period.

348. The fractional delay is disclosed by Adams to equal a whole number of ADC sampling periods. *Supra* §X.N.4(38[c]). Given that an ADC sampling period is a fraction of the baseband sampling period, the fractional delay is equal to a whole number times a fraction of the baseband sampling period.

349. Adams further states that “[t]o achieve precise control over the steering direction, the delay at each microphone node may need to be adjusted in finer steps than can be accomplished by using an integer number of sample-periods, and therefore it may be necessary to set both an integer as well as a fractional delay amount.” Ex.1005, [0022]. Adams further states that “[i]n these conditions it is possible **to use the higher frequency clock rates used in the oversampling analog-to-digital converters to implement the fractional part of the delay**, and the integer part of the delay can be implemented at the lower sample rates that correspond to the audio frame rate.” *Id.* (emphasis added).

350. In such an implementation, the fine delay (corresponding to claim's 38's "fractional time delay" – *see supra* §X.N.4(38[c])) provided by fine variable integer delay 113 corresponds to the fractional part of the delay (i.e., fraction of baseband sampling period), in contrast to the coarse delay (corresponding to claim 38's "integer time delay" which corresponds to the integer part of the delay (i.e., whole number multiple of baseband sampling period) – *see supra* §X.N.6(38[e])). Thus, the fine delay is generally intended to be a fraction of a baseband sampling period, while the coarse delay corresponds to a whole number multiple of baseband sampling periods.

351. In fact, in instances where "precise control over the steering direction" is desired to be "achieve[d]", as described in Adams (*see, e.g.*, Ex.1005, [0022]), the fractional delay would have been set. The finest increment of fractional delay that may be set, when such "precise" delay is desired or required (*id.*), was one sampling clock cycle (which corresponds to the smallest "whole number" (i.e., one) of sampling clock cycles).

352. As a POSA would have understood, one period of the baseband sample rate includes a number of sampling clock periods (i.e., sampling periods of the ADC) equal to the decimation factor (i.e., sampling clock frequency divided by the baseband sample rate), as discussed above for claim 17. *See supra* §X.I(claim 17); *see also* Ex.1005, [0089] ("the decimation factor [of 128] indicates that 128 samples

of the original ADC output code may be cycled through in same time as one sample of the serial data stream”).

353. Adams discloses an example where a decimation factor of 128 is used. Ex.1005, [0088]; *supra* §X.I(claim 17). Regarding this example, Adams explains that “it would be possible to select a fractional delay amount in increments of 1/128th the sample rate of the serial data stream.” Ex.1005, [0089]. In other words, with such decimation, there are 128 fractional delay steps within one sample (or one period) of the serial data stream. *Id.* Thus, in line with Adams’ disclosure that any “whole number of cycles at the higher frequency of the” ADC sampling clock can be selected as the fractional delay, a one sampling clock cycle selection, as discussed above, is 1/128 of the baseband sampling period, and accordingly “a fraction of a baseband sampling period,” as recited in claim 39 of the ’055 patent.

P. Claim 41

- 1. “The method of claim 38, wherein the oversampled digital signal is digitized to create samples which are more than one bit deep.”**

354. In my opinion, a POSA would have found claim 41 obvious based on Adams in view of Nguyen.

355. As I explained above, it is my opinion that a POSA would have found claim 38 obvious based on Adams in view of Nguyen. *Supra* §X.N(claim 38).

356. Even if the Adams-Nguyen system, as described for claim 38, did not disclose or otherwise render obvious that the oversampled digital signal is digitized to create samples which are more than one bit deep, a POSA would have at least been motivated by Nguyen's teachings to implement such a feature in the Adams-Nguyen system discussed for claim 38 above.

357. The '055 patent uses the terminology "one bit deep" and "bit depth" to refer to the number of bits used to represent a sample. Ex.1001, 4:59-5:13:

"Pulse density modulation (PDM) is such a digital conversion methodology that is **one-bit deep** where the sign is carried by the bit value where a "1" corresponds to a pulse of plus polarity (+A) and a "0" corresponds with a pulse of negative polarity (-A). Equation (3) indicates that a fractional delay can be selected based on a number of sampling clock cycles N from the range $1 \leq N \leq R$, and the time delay which is applied by delay element **216** is given by equation (4) as: $\Delta t = N * \tau_{SF}$. Where τ_{SF} is the period of the sampling clock. Where as described above, "fractional delay" refers to a fraction of a baseband sampling rate cycle.

Note that when other analog-to-digital digitization methodologies are used in the digital sensor **212** the resulting digital bit stream can be other than **one-bit deep**. In such cases, the oversampled digital signal at **212** can still be delayed with delay element **216**, where the delay will be a multiple of a "sample" regardless of **how many bits are used to encode the "sample"** at the digital sensor **212**. The minimum time delay increment will depend on the **bit depth** of the analog-to-digital digitization methodology used in the digital sensor **212**."

358. Nguyen discloses that its MEMS microphone sensor is integrated with a follow-on circuit 100 including a sigma-delta modulator ADC. E.g., *supra* §X.C.2(11[a]); Ex.1006, [0007]-[0008], [0012], [0013], [0027]-[0030]; *see also id.*,

[0001], [0035]. The “circuit 100 may be shaped and sized for integration into a miniature MEMS microphone housing or package.” *Id.*, [0028]. Adams-Nguyen’s MEMS microphone sensor senses an analog field quantity. *See supra* §X.C.2; Ex.1006, [0006] (“MEMS capacitive microphones are responsive...to sound.”), [0007], [0020]; *see also* Ex.1005, [0002], [0022]-[0023], cl.21; Ex.1014, pp. 7, 10 (Graf, 471, 714). In response to the sensing, Adams-Nguyen’s sigma-delta modulator ADC outputs an oversampled digital signal at the sampling rate. *See supra* §X.C.2; Ex.1006, [0012], [0001], [0004], [0030], [0007]-[0008], cl.20. Further, the sigma-delta modulator ADC, as Nguyen teaches, may include a multi-bit quantizer. Nguyen’s multi-bit quantizer provides samples represented by multiple bits, whereas its single-bit quantizer provides samples represented by single bits. *See, e.g.,*

Id., [0012]:

“Each of the first and second sigma-delta modulators may comprise a single-bit quantizer or a multi-bit quantizer with their respective well-known advantages and disadvantages. If each of the first and second sigma-delta modulators comprises the single-bit or one bit quantizer the first and second digital signals may be conveniently supplied as first and second PDM signals, respectively. Alternatively, each of the first and second digital signals may be converted from native PDM format to a multi-bit or PCM format. Each of the first and second sigma-delta modulators preferably operates at an oversampled sampling frequency such as a sampling frequency between 1 MHz and 10 MHz.”

see also id., 30 (“The skilled person will appreciate that each of the first and second sigma- delta modulators 110, 112 may comprise...a multi-bit quantizer.”).

359. A POSA would have been motivated to combine the teachings of Nguyen in implementing Adams’ system so that the digital microphone utilizes a MEMS sensor integrated with a circuit comprising a sigma-delta modulator ADC, with the ADC including a multi-bit quantizer, as discussed above, and a POSA would have had a reasonable expectation of success. *Supra* §§X.A-B; Ex.1006, [0012], [0030] (“The skilled person will appreciate that each of the first and second sigma-delta modulators 110, 112 may comprise a...multi-bit quantizer.”).

360. A POSA would have also understood that both Adams and Nguyen seek to reduce the assembly costs and space required to implement its digital microphones. For example, Adams in discussing the background art, complains about microphones to be individually wired to separate inputs of the signal processing device, which “requires additional expense and space” and “may affect the overall reliability of the system”:

“These beamforming algorithms were originally implemented in signal processing devices, which required each of the microphones to be individually wired to separate inputs of the signal processing device, typically an integrated circuit. The number of wires therefore increases proportionally with the number of microphones in the array. **Incorporating these extra wires requires additional expense and space in the device. Additionally, the extra wires may affect the overall reliability of the system as the likelihood of a defect,**

malfunction, or problem with one or more of the wire sets tends to increases as the number of wires increases.”

Ex.1005, [0003] (emphasis added).

361. Nguyen similarly recognized an aim to reduce space consumption and power consumption, as well as lower assembly costs and taught an approach which implemented a MEMS sensor integrated with a follow-on circuit 100 comprising a sigma-delta modulator ADC. *See* above discussion. Such integration provided a number of advantages:

“Hence, it is advantageous to integrate multiple functions in a single transducer unit such as a microphone. **This type of integration may reduce power consumption of active circuitry, reduce space consumption and lower assembly costs** of the portable communication or computing device in question. Portable communication devices furthermore often comprise a plurality of transducers such as microphones for voice and sound pick-up, recording and transmission which adds to the advantages of integrating multiple functions in a single transducer device.”

Ex.1006, [0002] (emphasis added); *see also, id.*, [0003].

362. Further, Nguyen, filed approximately two years after Adams, teaches that such MEMS sensors were “[c]ommonly used” by that time, “shaped and sized for portable audio devices such as smartphones, tablets and mobile phones etc.,” and “integra[ble] into a miniature MEMS microphone housing or package.” *Id.*, [0006]-[0007], [0028]. The use of sigma-delta modulator ADCs in digital signal processing was also prevalent and well known. *See supra* §§VI.C, E.

363. Given the overlapping aims of Adams and Nguyen, as well as Nguyen's solution resulting in the integration of the MEMS microphone sensor and follow-on sigma-delta modulator ADC, the combination of Adams and Nguyen would provide the abovementioned benefits in Adams' system, consistent with Adams' aims.

364. In my opinion, this combination would have had a number of beneficial results, including saving space, reducing assembly costs, improving reliability, and facilitating integrability in Adams' system, in line with Adams' identified need, and Nguyen's teachings.

Q. Claim 46

365. It is my opinion that a POSA would have found claim 46 obvious based on Adams in view of Nguyen ("Adams-Nguyen").

1. 46[pre]: "A system to delay digital signals, comprising:"

366. I have been asked to assume the preamble of claim 46 is limiting. Under that assumption, it is my opinion that Adams discloses claim 46's preamble, 46[pre], which recites "[a] system to delay digital signals, comprising" for the same reasons provided for 11[pre] above. *See supra* §X.C.1(11[pre]).

2. 46[a]: "sensing means for measuring an analog field quantity;"

367. In my opinion, Adams discloses this limitation and Adams-Nguyen also renders obvious this limitation. *See supra* §§X.C.2, IX.B.1. As I discussed above

for claim element 11[a], Adams discloses a digital sensor microphone 110 element that is responsive to an analog field quantity, namely sound or acoustic pressure. *See supra* §X.C.2; Ex.1005, [0002], [0022] (“audio data from its associated microphone corresponding to sound”) [0023] (“The microphone and/or preamplifier may be coupled to an analog to digital converter 112 that may generate digital code words from **the analog audio signal obtained from the microphone 110.**”) (emphasis added), cl.21; *see also* Ex.1014, p. 7 (Graf, 471) (“**microphone**—1. An electroacoustic transducer that responds to sound waves and delivers essentially equivalent electric waves. 2. A device for converting sound waves or sound-producing vibrations (as from the strings of a guitar) into corresponding electrical impulses...”), p. 10 (Graf, 714) (“**sound**—1. Also called a sound wave. An alteration in pressure, stress, particle displacement or velocity, etc., propagated in an elastic material or the superposition of such propagated alterations.”).

368. In my opinion, that understanding is consistent with the disclosure of the '055 patent. *See, e.g.*, Ex.1001, 1:30-33, 7:24-25, 10:34-37, 11:19-23, 12:18-21, 13:17-21, 14:20-30, Figs.8, 9A-9B, 10 (analog field quantity 802/902/1002).

369. Adams' microphone is responsive to sound or acoustic pressure, and thus provides a measure of such analog field quantity. This understanding is consistent with the disclosure of the '055 patent. *See, e.g.*, Ex.1001, 1:33-35 (“Measurement of a field quantity is accomplished with an analog sensor or a digital

sensor.”). Thus, it is my opinion that Adams’ microphone 110 element performs the function “for measuring an analog field quantity.” *See supra* §IX.B.1.

370. It is also my opinion that Adams’ microphone 110 is the same or at least structurally equivalent to the claimed “sensing means” because it is a microphone. *See* Ex.1005, [0023], Fig.1; *supra* §§X.C.2, IX.B.1.

371. Also, even if Adams did not disclose or otherwise render obvious that “sensing means,” a POSA would have found it obvious to implement it, at least in light of the teachings of Nguyen that the digital microphone includes an integrated MEMS sensor/sigma-delta modulator. As I discussed above for claim element 11[a], the digital sensor in the Adams-Nguyen system includes a MEMS microphone element (in place of the microphone 110 element) that is likewise responsive to an analog field quantity, namely sound or acoustic pressure. *See supra* §X.C.2. Adams-Nguyen’s MEMS microphone sensor is responsive to sound or acoustic pressure, and thus provides a measure of such analog field quantity. This understanding is consistent with the disclosure of the ’055 patent. *See, e.g.*, Ex.1001, 1:33-35 (“Measurement of a field quantity is accomplished with an analog sensor or a digital sensor.”).

372. Thus, it is my opinion that Adams-Nguyen’s MEMS microphone element performs the function “for measuring an analog field quantity.” *See supra* §IX.B.1; Ex.1006, [0006] (“MEMS capacitive microphones are responsive...to

sound.”), [0007], [0020]; *see also* Ex.1005, [0002], [0022]-[0023], cl.21; Ex.1014, pp. 7, 10 (Graf, 471, 714).

373. It is also my opinion that Adams-Nguyen’s MEMS microphone sensor is the same or at least structurally equivalent to the claimed “sensing means” because it is a microphone, specifically a MEMS microphone. *See supra* §§X.C.2, IX.B.1.

3. 46[b]: “over sampling means, the over sampling means to over sample a signal detected by the sensing means resulting in an oversampled digital signal;”

374. In my opinion, Adams discloses this limitation and Adams-Nguyen renders obvious this limitation. *See supra* §§X.C.2, IX.B.2.

375. As I discussed above for claim element 11[a], Adams discloses a digital sensor analog-to-digital converter (ADC) 112 element that “may oversample the analog audio signal” received by the microphone 110 element and “convert[s] sampled audio signals from the microphone into digital codes.” *See supra* §X.C.2; Ex.1005, [0016], [0023] (“The microphone and/or preamplifier may be coupled to an analog to digital converter 112 that may generate digital code words from the analog audio signal obtained from microphone 110.”), [0024] (“The analog digital converter 112 may oversample the analog audio signal, such as 2.4 MHz or higher...”), cl.23. As I discussed above for claim element 46[a], Adams’ microphone 110 element corresponds to the claimed “sensing means.” *See supra* §X.Q.2.

376. Thus, it is my opinion that Adams' digital sensor ADC element performs the function "to over sample a signal detected by the sensing means resulting in an oversampled digital signal."

377. It is also my opinion that Adams' digital sensor ADC is the same or at least structurally equivalent to the claimed "over sampling means" because Adams discloses a digital sensor analog-to-digital converter (ADC). *See supra* §IX.B.2.

378. Also, even if Adams did not disclose or otherwise render obvious that "over sampling means," a POSA would have found it obvious to implement it, at least in light of the teachings of Nguyen. The Adams-Nguyen combination applies Nguyen's teaching that the digital microphone includes an integrated MEMS sensor/sigma-delta modulator. *See supra* §§X.A-B. Thus, the ADC element is a sigma-delta modulator in this Adams-Nguyen system.

379. The sigma-delta modulator ADC element in the Adams-Nguyen system also "operat[es] at an oversampled sampling rate or frequency," and is "configured to sample" the signal from (and detected by) the MEMS microphone transducer, which is Adams-Nguyen's sensing means (*see supra* §X.Q.2), and output an oversampled digital transducer signal. *See supra* §X.C.2; Ex.1006, [0012], [0001], [0004], [0030], cl.20; *see also* Ex.1006, [0007] (emphasis added):

"The transducer signal may accordingly be generated by one of the above mentioned microphone devices. The MEMS capacitive microphone may comprise a micro-electromechanical (MEMS)

transducer element, e.g. shaped and sized for portable audio devices such as smartphones, tablets and mobile phones etc. The electromechanical **(MEMS) transducer element** may function as a single element audio and ultrasonic microphone responsive to both impinging audible sound and ultrasonic sound due to its broad-band frequency response.”

See also id., [0008].

380. As I discussed above for claim element 46[a], Adams-Nguyen’s MEMS microphone element (in place of microphone 110 element) corresponds to the claimed “sensing means.” *See supra* §X.Q.2.

381. Thus, it is my opinion that Adams-Nguyen’s sigma-delta modulator ADC element performs the function “to over sample a signal detected by the sensing means resulting in an oversampled digital signal.”

382. It is also my opinion that Adams-Nguyen’s digital sensor sigma-delta modulator ADC is the same or at least structurally equivalent to the claimed “over sampling means” because it is an analog-to-digital converter (ADC), and specifically a sigma-delta modulator analog-to-digital converter, as I discussed above. *See supra* §§IX.B.2, X.C.2.

4. **46[c]: “fractional delaying means, the fractional delaying means to apply a fractional time delay to the oversampled digital signal, the fractional time delay is equal to an integer number of sampling clock cycles, resulting in a delayed oversampled digital signal;”**

383. In my opinion, Adams discloses this limitation. It is also my opinion that Adams-Nguyen renders obvious this limitation.

384. Adams discloses that its fine variable integer delay 113 is coupled to the output of the ADC and thus receives as an input, the oversampled digital output signal from the ADC. *See supra* §X.C.3(11[b]); Ex.1005, [0027], Fig.1.

385. Adams also discloses that its fine variable integer delay 113 provides a time delay of “a whole number of cycles at the higher frequency of the [ADC] 112 to delay the generated digital code words outputted by the converter 112.” Ex.1005, [0027]. As a POSA would have understood, a “whole number” is an integer. *See, e.g.,* Ex.1014, p. 5 (Graf, 381) (“**integer** – A whole number, which may be positive, negative, or zero.”).

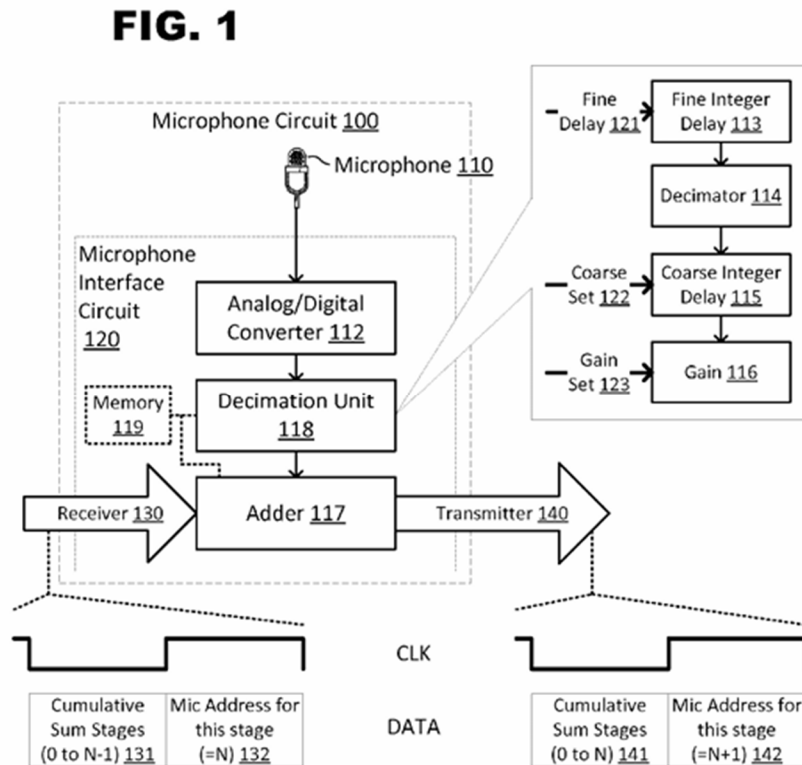
386. Adams further identifies this delay implemented by fine integer delay 113 as a “fractional” time delay. *See* Ex.1005, [0022] (“[I]t is possible to use the higher frequency clock rates used in the oversampling analog-to-digital converters to implement the fractional part of the delay,”); *see also id.*, [0089] (“if the fractional delay is associated with the original ADC output sample rates [], it would be possible to select a fractional delay amount”); *see supra* §X.C.3(11[b]).

387. As I discussed for claim element 11[b], the “cycles at the higher frequency of the [ADC]” corresponds to the “sampling clock cycles.” *See supra* §X.C.3(11[b]).

388. Thus, fine variable integer delay 113 is configured to apply a fractional time delay equal to an integer number of sampling clock cycles to the oversampled

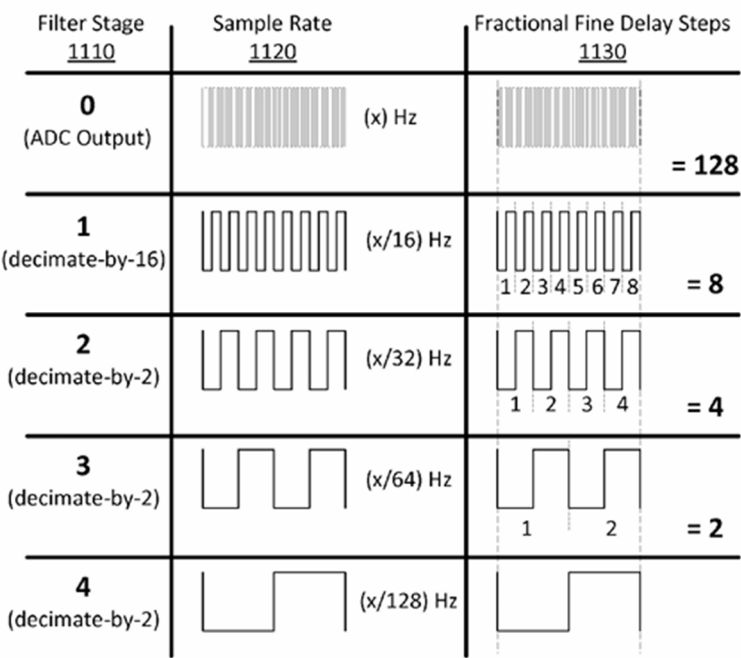
digital signal output from the ADC, with the result being the fine variable integer delay 113 outputting a delayed oversampled digital signal.

389. Adams discloses a decimation unit (i.e., Decimation unit 118), in its Figure 1 system for time delay, and further discloses, in its Figure 11, an architecture for such a decimation unit in its system, including disclosing “how delay elements may be used between different filter stages” of a multi-stage decimation unit. Ex.1005, [0023], [0025], [0088]-[0095], Figs.1, 11.



Ex.1005, Fig.1.

FIG. 11



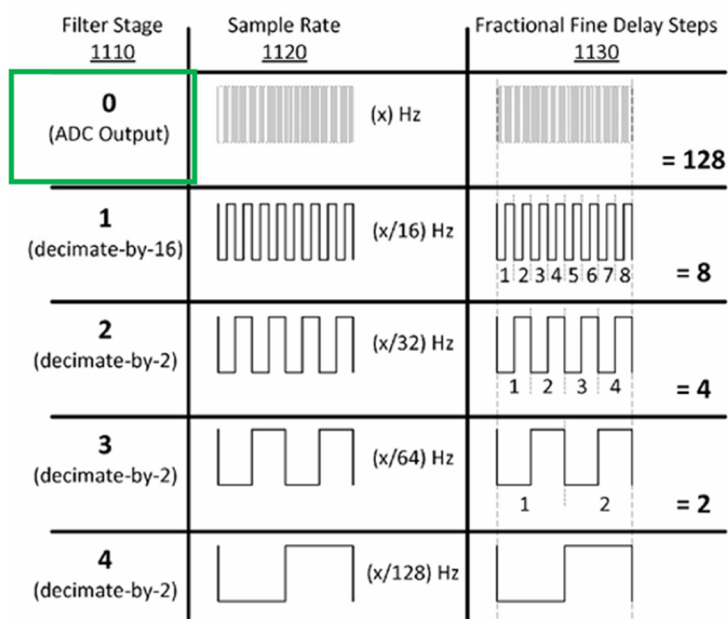
Ex.1005, Fig.11.

390. It is my opinion that a POSA would have been motivated to apply Adams’ Figure 11 decimation unit architecture teachings in implementing the decimation unit in its Figure 1 system for time delay. Adams’ Figure 1 system for time delay already has a place for a decimation unit, and Adams teaches a specific architecture in Figure 11 for such a decimation unit. Adams further teaches that its Figure 11 architecture provides flexibility by having multiple stages of decimation, allowing the possibility of selecting different time delay resolution depending on the desired delay. Adams further teaches this has the advantage that it “may, in some instances, reduce the size of the delay unit and conserve power.” Ex.1005, [0094].

391. It is also my opinion that a POSA would have had a reasonable expectation of success in the aforementioned implementation. This is because first, as discussed above, Adams already discloses the exemplary Figure 11 implementation in the context of its systems for time delay. And the combination simply uses Adams' known Figure 1 system for time delay, including a microphone, ADC, decimation unit 118, and adder, with Adams' Figure 11 exemplary implementation for a decimation unit.

392. Consistent with my discussion for claim element 11[b], Adams discloses that "the fractional delay is associated with the original ADC output sample rates 1120." Ex.1005, [0089]. Thus, Adams' fractional delay unit, including in Adams' Figure 1 system for time delay modified in view of Adams' Figure 11 decimation unit architecture teachings, corresponds to fine variable integer delay 113, and is associated with the original analog-to-digital converter (ADC) output sample rates 1120, as indicated in Figure 11. *Id.*; *see also id.*, [0027]; *supra* §X.C.3(11[b]).

FIG. 11



Ex.1005, Fig.11 (annotated).

393. As Adams discloses, with such a “delay” implementation, “it would be possible to select a fractional delay amount” from this delay “associated with the original ADC output sample rates 1120” that is “in increments of 1/128th the sample rate of the serial data stream.” Ex.1005, [0089]. In other words, this “delay...associated with the original ADC output sample rates 1120” is an integer number of ADC sampling rate cycles (or in other words, an integer number of

“sampling clock cycles”).⁸ This follows from the fact that the serial data stream rate is 1/128th the ADC sampling rate, and the period equals 1/rate.

394. The serial data stream rate is also the baseband sampling rate. This follows from the fact that Adams describes that the “serial data stream frame rate” (also referred to as the “audio frame rate”—see Ex.1005, [0016], [0022], claims 3, 43)—is the rate at which “audio data and configuration data” is transmitted “between...each of the microphone stages” (*i.e.*, microphone circuits 100). *Id.*, [0020]; see also *id.*, Abstract (“A serial interface may be used to connect the transmitters and receivers of each of the stages.”), [0016], [0024] (providing example of “44 kHz” as rate used to transmit data between microphone circuits 100); Figs.1-5. Adams’ post-decimation “serial data stream frame rate” output is a baseband sample rate. In my opinion, that understanding is consistent with the disclosure of the ’055 patent, which describes a receiver module that low-pass filters and decimates an oversampled digital signal to output a baseband digital signal at a baseband sampling rate. Ex.1001, 3:55-3:67, 6:22-39. This also means that the “delay...associated with the original ADC output sample rates 1120” is provided in increments of (1/128) times the baseband sampling period. See also Ex.1005, [0089]

⁸ Stated differently, the delay is equal to integer increments of the stage 1 output period (which is equal to integer increments of the baseband period divided by 8).

(“128 samples of the original ADC output code may cycled through in same time as one sample of the serial data stream”), Fig.11 (showing 128 fractional fine delay increments in one serial data stream period).

395. It is thus my opinion that the fractional delay unit in Adams’ Figure 1 system for time delay modified in view of Adams’ Figure 11 decimation unit architecture teachings corresponds to fine delay 113 and performs the function of “to apply a fractional time delay to the oversampled digital signal, the fractional time delay is equal to an integer number of sampling clock cycles, resulting in a delayed oversampled digital signal.”

396. The oversampled digital signal received by fine delay 113 can be either from Adams’ over sampling means or Adams-Nguyen’s over sampling means, as I discussed above for claim element 46[b]. *See supra* §X.Q.3(46[b]).

397. It is also my opinion that the fractional delay unit (i.e., fine variable integer delay 113) in Adams’ Figure 1 system for time delay modified in view of Adams’ Figure 11 decimation unit architecture teachings corresponds to the claimed “fractional delaying means.” Fine variable integer delay 113 is a delay circuit given that it provides fractional delay, as I discussed above, and the fact it is within circuit 100 and thus is implemented in a circuit. Ex.1005, [0023], [0025], Fig.1; *see also id.*, [0034], Figs.3-5; *see also supra* §IX.B.3.

398. Adams also discloses that fine variable integer delay 113 provides its “delay using memory or storage units.” Ex.1005, [0025]. As a POSA would have understood, use of such memory or storage unit allows the retention of samples for a selected number of analog-to-digital (ADC) clock cycles “to ensure that the output codes from the decimation unit...align” with codes from other microphone stages.
Id.

399. Additionally, Adams further explains that this delay may be “select[ed]” and is “programm[able].” *See*:

Ex.1005, [0022] (emphasis added):

“Each delay unit may have a delay selected to insure that the audio data from its associated microphone corresponding to sound from a particular direction is time-aligned with the data represented by the cumulative sum arriving at the receiver of that microphone stage.”

Id., [0027] (emphasis added):

“A fine variable integer delay 113 may be coupled to the analog to digital converter 112. The fine variable integer delay 113 may include a fine delay input 121, which may be used to select a whole number of cycles at the higher frequency of the analog to digital converter 112 to delay the generated digital code words outputted by the converter 112. Since the analog to digital converter 112 may operate at frequencies many times higher than the serial data stream, the fine variable integer delay 113 may enable the selection of a precise delay amount to maximize alignment of the audio signals received at different times at each microphone in the microphone array.”

Id., [0050]-[0051] (emphasis added):

“In some embodiments, **the amount of delay to be applied may be calculated in advance and then encoded into the data words 163 associated with respective set delay commands 162 for each microphone address 161.** For example, if a microphone array has a total length of 3 feet, sound may arrive at the first microphone at the beginning of the array approximately 3 ms before arriving at the last microphone at the end of a linear array (assuming sound travels at roughly 1 ms/ft). In the case of a decimated sample rate of 44.1 KHz, a one sample delay would last approximately 22 μ s. To obtain the 3 ms delay, a delay of 136 sample cycles would be needed (3 ms/22 μ s). Thus, the data word **163** may be set to ‘10001000’ (corresponding to the decimal number 136), to specify a delay value of 136 cycles associated with the set delay command **162** for the last microphone in the array.

In some instances buffering the cumulative audio data **131** from prior stages in order to perform the addition at adder **117** may cause an additional delay in each node. In these instances **the programmed delay** may be adjusted to account for this delay. For example, if a one sample delay per stage is caused by the buffering of the cumulative data, a corresponding sample offset could be subtracted from **the programmed delay** depending on the position of the stage in the array.”

400. Regarding this latter point, Adams discloses that a delay control signal “formatted to include a microphone address 161, a command code word 162, and a data word 163” (Ex.1005, [0045]) is sent to the respective delay unit. *Supra* §X.C.6(11[e]). As Adams further explains, the “command code word 162 may specify a command that the addressed microphone circuit 161 is to execute,” such as “specify[ing] instructions such as setting a digital delay 118.” Ex.1005, [0047]. “The data word 163 may specify a value associated with the command code

word 162. For example, the value specified in data word 163 may be an amount of delay...that is to be set.” *Id.*, [0048].

401. In my opinion, fine variable integer delay 113 is the same or at least structurally equivalent to the claimed “fractional delaying means” because the specification simply discloses the delay element providing such fractional delay as “a delay element...implemented as a buffer” or “delay line,” or “delay circuit,” any of which “can be programmable.” *See supra* §IX.B.3; Ex.1001, 3:42-54:

“In various embodiments, the delay element **216** is implemented as a buffer, which can be programmable. In other embodiments, the delay element is implemented with a delay line; the delay line can be a programmable delay line. In yet other embodiments, the delay element is implemented with a circuit constructed to provide a delay and the delay can be programmable. A programmable delay element **216** will allow the magnitude of the delay Δt to be adjusted as desired. In the context of beamforming, a programmable delay(s) will allow a beam formed with two or more sensors to be steered to different directions. Beamforming will be discussed more completely below in conjunction with the figures that follow.”

5. 46[d]: “decimating means, the decimating means to receive the delayed oversampled digital signal and to low pass filter and to decimate to a lower sampling rate;”

402. In my opinion, Adams in view of Nguyen renders this limitation obvious.

403. As I discussed above, Adams’ Figure 1 system for time delay modified in view of Adams’ Figure 11 decimation architecture teachings includes a decimation unit, specifically decimation unit 118 in Figure 1, modified in view of

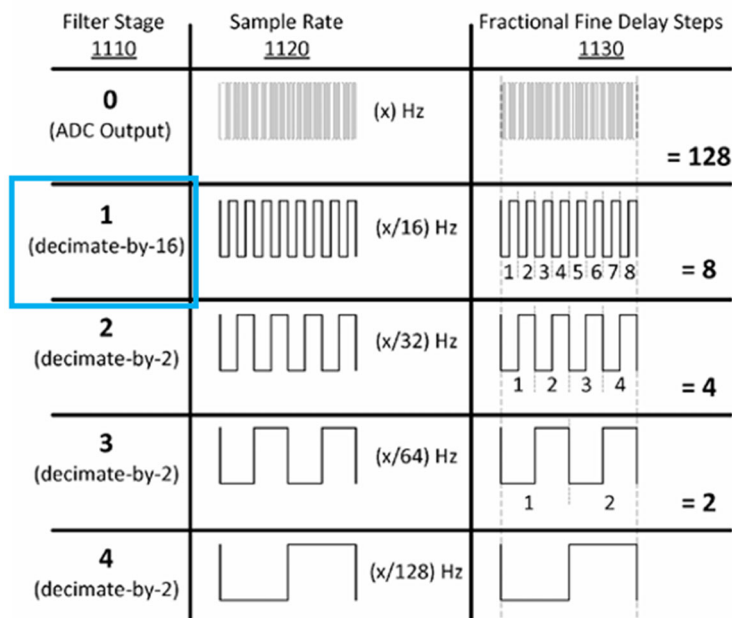
Adams' Figure 11 related teachings to provide a "sequence of successive stages to complete the decimation process." Ex.1005, [0025], [0088], Figs.1,11. More specifically, Adams discloses, and illustrates in Figure 11, "four filter stages" to provide a total decimation factor of 128. *Id.*, [0088]-[0093], Fig.11.

404. In this example, the first stage provides by 16 decimation; the second stage provides by 2 decimation; the third stage provides by 2 decimation; and the fourth stage provides by 2 decimation. *See id.*

405. In my opinion, the first stage is an example of a "decimating means," as recited in claim 46. To explain, Adams discloses that "the fractional delay is associated with the original ADC output sample rates 1120" (*supra* §X.Q.4(46[c])) and therefore applies a fractional time delay to the ADC oversampled digital signal and outputs a delayed oversampled digital signal. Ex.1005, [0089]. The output of the fractional delaying means (i.e., fine delay 113) is coupled to the input of the multi-stage decimation filter circuit. Ex.1005, [0088]-[0089], Fig.11.

406. Adams further discloses that "[i]n the first stage" of decimation circuit 1110, "the sample rate 1120 of the ADC output codes may be decimated by a factor of 16." Ex.1005, [0090]. Accordingly, the first stage (or in other words, stage 1) receives the delayed oversampled "ADC output codes" from the fractional delaying means, and filters and decimates that signal to a lower sampling rate, which in this example is the ADC sampling rate divided by 16. Ex.1005, [0089], [0090].

FIG. 11



Ex.1005, Fig.11 (annotated).

407. Even if Adams did not disclose or otherwise render obvious that the filtering performed by decimator circuit 1110 is “low pass” filtering, a POSA would have found it obvious to implement it so as to provide low-pass filtering, at least in light of the teachings of Nguyen. *See supra* §§X.A-B.

408. First, decimation filters are (and would have been) generally low pass filters, as a POSA would have understood, in order to pass the desired relatively low frequency in-band signal and attenuate higher-frequency components in the signal, including out-of-band quantization noise, as well as to suppress aliasing in systems. *See supra* §VI.D.

409. Second, Adams acknowledges that microphone-based systems, like its own, aim to reduce effects of “noise and other undesirable sounds”:

“Microphone arrays have been used to improve fidelity and reduce effects of ambient noise. Arrays of two or more microphones may be used to capture specific audio signals while reducing the effects of background noise and other undesirable sounds. Various beamforming algorithms may be used to combine the signals from each of the microphones in the array so that audio signals originating from a particular direction constructively interfere and generate a highest magnitude response over audio signals originating from other directions.”

Ex.1005, [0002]; *see also id.*, [0081]. In line with this aim, Adams specifies that its decimation element does not just downsample, but “first filter[s]” the incoming signal “before downsampling.” Ex.1005, [0025], claim 28. Like Adams, Nguyen⁹ discloses the use of a decimation filter in a microphone-based system to suppress higher frequency noise components, and expressly identifies the filter as a “lowpass filter.” Ex.1006, [0035] (“The decimator 306 preferably comprises a lowpass filter 308 which may be...integrated with the decimator.”), [0037] (“unwanted” higher frequency components are attenuated by passing the...signal...through a combined lowpass filter and decimator []”).

⁹ Adams and Nguyen share the same author, Robert Adams. Ex.1005, Inventors; Ex.1006, Inventors.

410. In my opinion, a POSA configuring Adams' decimation filter as low pass would have appreciated such configuration to be straightforward given the similarities in Adams and Nguyen. As an example, Adams and Nguyen both concern audio microphone signal processing systems; they are also disclosures from the same company and share the same inventor; their systems include many of the same components, as discussed above. Nguyen also teaches that its decimation filter provides decimation factors "between 16 and 128" (Ex.1006, [0035]), which is similar to factors taught by Adams. Ex.1005, [0090] (decimation factor of 16), [0088] (decimation factor of 128). Nguyen also teaches the use of its decimation filter to downsample from an ADC oversampled frequency to "a desired final sample rate for the outgoing digital audio stream" (Ex.1006, [0035]), which is similar to Adams which discloses downsampling from an ADC oversampled frequency to the digital "audio frame rate":

"Embodiments of the invention provide a system having an array of microphone stages in which each of the microphone stages may be coupled together in a daisy chain. Each microphone stage may include a microphone, an analog to digital converter, a decimation unit, a receiver, an adder, and a transmitter. The analog to digital converter may convert sampled audio signals from the microphone into digital codes. **The decimation unit may decimate digital codes from the analog to digital converter output to an audio frame rate of a serial interface used to transmit data between microphone stages.** The decimation unit may also include a delay unit to implement a delay at each microphone stage."

Ex.1005, [0016]; *see also id.*, [0022], claims 3, 43. A POSA would have had a reasonable expectation of success in the aforementioned combination of Adams' and Nguyen's teachings given that the proposed implementation merely applies Nguyen's known decimation filter implementation teaching to Adams' known decimation filter without changing Adams' multiple time delay operations and structure. In my opinion, a POSA applying Nguyen's well-known low-pass decimation filter teaching to Adams' known decimation filter would have been no more than the predictable use of prior-art elements according to their established functions. *See supra* §§VI.D, X.A-B.

411. Accordingly, it is my opinion that the decimation filter stage 1 of circuit 1110 performs the function “to receive the delayed oversampled digital signal and to low pass filter and to decimate to a lower sampling rate.”

412. It is also my opinion that decimation filter stage 1, as modified in view of Nguyen, corresponds to the claimed “decimating means” because it is a “[d]ecimation filter” that provides low-pass filtering and decimation to a lower sampling rate. *See supra* §IX.B.4; Ex.1005, [0088]-[0090], Fig.11.

6. 46[e]: “integer delaying means, the integer delaying means to apply an integer time delay to the delayed oversampled digital signal, the integer time delay is a number of lower sampling rate cycles; and”

413. In my opinion, Adams in view of Nguyen renders this limitation obvious.

414. As I discussed above, Adams' Figure 1 system for time delay modified in view of Adams' Figure 11 decimation architecture teachings includes a decimation unit, specifically decimation unit 118 in Figure 1, modified in view of Adams' Figure 11 related teachings to provide a "sequence of successive stages to complete the decimation process." Ex.1005, [0025], [0088], Figs.1, 11.

415. Further, as I discussed above for claim element 46[d], the output of decimation filter stage 1 (the stage which in my opinion corresponds to the "decimating means" claimed in 46[d]) is a delayed oversampled digital signal. *See supra* §X.Q.5. The output of that decimation filter stage 1 is delayed is because of the fact that the fractional delay unit (fine variable integer delay 113) is located upstream of that stage, and thus the oversampled digital signal from the ADC that is input into the fine variable integer delay 113 is then delayed by fine variable integer delay 113 before being decimated and low pass filtered by decimation filter stage 1. *See supra* §X.Q.5. The output of decimation filter stage 1 is still "oversampled" because decimation filter stage 1 only decimates by 16. Ex.1005, [0090] ("In the first stage, the sample rate **1120** of the ADC output codes may be decimated by a factor of 16."), Fig.11. Thus, the decimation filter stage 1 does not fully decimate to the baseband rate (serial stream frame rate) in my opinion. As Adams discloses, subsequent decimation occurs in decimation filter stages 2 through 4 which in total decimate the signal output by decimation filter stage 1 by a factor of 8. After the

fourth stage, the output frequency is the serial stream frame rate, which I discussed above, corresponds to the baseband sampling frequency. *See:*

Id., [0091]:

“In the second stage, the sample rate of the output of the first stage may be decimated by a factor of 2. This may reduce the delay step increments **1130** from 8 to 4, as now only 4 samples may be cycled through in the same time as one sample of the serial data stream.”

Id., [0092]:

“In the third stage, the sample rate of the output of the second stage may be decimated by a factor of 2. This may reduce the delay step increments **1130** from 4 to 2, as now only 2 samples may be cycled through in the same time as one sample of the serial data stream.”

Id., [0093]:

“In the fourth stage, the sample rate of the output of the third may be decimated by a factor of 2 generating the final desired sample rate of the serial data stream.”

416. Adams discloses that a “delay” may be associated with the output of the first stage.” Ex.1005, [0090]. With such a “delay” implementation, “it would be possible to select a fractional delay amount” from this delay associated with the output of the first stage “in increments of $1/8^{\text{th}}$ the sample rate of the serial data stream.” *Id.* In other words, this “delay...associated with the output of the first stage” is an integer number of stage 1 sampling rate cycles (or in other words, an

integer number of “lower sampling rate clock cycles”).¹⁰ This follows from the fact that the serial data stream rate is one eighth (i.e., 1/8) the rate output from the decimation filter stage 1, and the period equals 1/rate. As a POSA would have understood, an “integer” is a number. Ex.1014, p. 5 (Graf, 381) (“**integer** – A whole number, which may be positive, negative, or zero.”).

417. Therefore, it is my opinion that the “delay...associated with the output of the first stage” performs the function “to apply an integer time delay to the delayed oversampled digital signal, the integer time delay is a number of lower sampling rate cycles.”

418. It is also my opinion that this delay unit associated with output of decimation filter stage 1 corresponds to the “integer delaying means” claimed in 46[e] because this delay element provides the delay, as I discussed above, and it is a circuit, as indicated by it being located within the “decimation circuit.” Ex.1005, [0088] (“a decimation circuit with a decimation factor of 128 may include four filter stages 1110 as shown in Fig. 11.”), [0090], Fig.11; *see also id.*, [0034] (“the fine delay 121, coarse delay 122, and gain set 123 inputs in each microphone circuit 100”).

¹⁰ Stated differently, the delay is equal to integer increments of the stage 1 output period (which is equal to integer increments of the baseband period divided by 8).

419. Additionally, Adams generally discloses delay units providing “delay using memory or storage units,” further supporting the circuit implementation. Ex.1005, [0025]. Such utilization would have allowed Adams’ delay units the ability to retain samples for a selected number for lower sampling rate clock cycles to time align the output codes from other microphone stages. Ex.1005, [0025].

420. Additionally, Adams explains that the delay may be “select[ed]” and is “program[able].” Ex.1005, [0022] (“Each delay unit may have a delay selected to insure that the audio data from its associated microphone corresponding to sound from a particular direction is time-aligned with the data represented by the cumulative sum arriving at the receiver of that microphone stage.”), [0027], [0050] (“In some embodiments, the amount of delay to be applied may be calculated in advance and then encoded into the data words 163 associated with respective set delay commands 162 for each microphone address 161.”), [0051] (“the programmed delay may be adjusted”).

421. For these reasons, it is my opinion that the delay unit associated with the output of the decimation filter stage 1 is the same or at least structurally equivalent to the claimed “integer delaying means.” *See supra* §IX.B.5. Ex.1001, 2:26-27, 3:27-54, 16:45-50, Figs.15A-B.

7. **46[f]: “controlling means, the controlling means to adjust the fractional time delay and the integer time delay to establish a total time delay, wherein a resulting digital signal is delayed by a total time delay, wherein the total time delay is a sum of the fractional time delay and the integer time delay, and contains a digital representation of the analog field quantity without the noise introduced by the over sampling means.”**

422. In my opinion, Adams in view of Nguyen renders this limitation obvious.

423. Adams discloses that “to achieve precise control...it may be necessary to set both an integer as well as a fractional delay amount.” Ex.1005, [0022]. Further, Adams discloses that “[e]ach delay unit may have a delay selected to insure [*sic*] that the audio data...is time-aligned.” *Id.*

424. Adams also discloses that the fractional time delay may be “select[ed]” “in increments of $1/128^{\text{th}}$ the sample rate of the serial data stream.” Ex.1005, [0089]; Fig.11(showing 128 ADC sampling periods in one serial data stream period). Adams discloses that the integer time delay may be “select[ed]” “in increments of $1/8^{\text{th}}$ the sample rate of the serial data stream.” *Id.*, [0090], Fig.11(showing 8 lower sampling rate periods in one serial data stream period).

425. In terms of selecting/setting the delay to have such “precise control,” Adams discloses that the “integer and the fractional delays can be set using the configuration channel transmitted to each microphone.” Ex.1005, [0022]. Further, Adams discloses that the “configuration data” transmitted can include “delay data to

set a variable delay.” *Id.*, [0021], cl.36(disclosing transmitting “delay setting over the control channel”).

426. Adams further discloses that the “delay” may be “programmed” and “adjusted” (*id.*, [0051]), and in describing its Figure 1 structure, discloses the fractional and integer delay units having inputs “to select” their respective delays. *Supra* §X.C.6(11[e]); Ex.1005, [0027], [0029], [0034].

427. Adams also discloses a “microcontroller.” Ex.1005, [0087]. The controller performs calculations and sends control signals to circuit 100 elements (e.g., amplifier/gain) to set/control the elements. Ex.1005, [0087]:

“The microcontroller may calculate a subsequent gain **1030** to be applied to each of the variable amplifiers **1011** based on the identified highest audio level. The calculated gain **1030** may then be sent to a gain set input of each variable amplifier **1011** coupled to the microcontroller.”

See also id., claim 36 (“a control channel and control inputs of the preamplifier and the analog delay unit, wherein the receiver receives a gain setting and a delay setting over the control channel, provides the gain setting to the preamplifier through its control input, and provides the delay setting to the analog delay unit through its control input.”).

428. Adams also discloses its system using a memory to implement its delay, which a POSA would have understood would have been consistent with control by a microcontroller. Ex.1005, [0025] (“The decimation unit **118** may include a delay unit with one or more delay elements **113** and/or **115** that may implement a delay using memory or storage units at various locations within the structure of the

decimation filter to ensure that the output codes from the decimation unit **118** align with the decimated code words at the other microphone stages from audio signals received at different times at each of the other microphones”), [0034] (“In some embodiments, the fine delay **121**, coarse delay **122**, and gain set **123** inputs in each microphone circuit **100** may be pre-configured before the microphone array is used. During the pre-configuration, each circuit **100** may be supplied with predetermined input values that have been optimized based on the intended use of the microphone array. In other embodiments, these inputs **121**, **122**, and **123** may be dynamically configured. In some instances this configuration data may be stored in a memory **119**.”); *see also* Ex.1014, p. 6 (Graf, 470) (“**microcontroller** – A complete microprocessor system on a chip. Includes on-chip the CPU, local RAM, local ROM or EPROM, clock and control circuits, and serial and parallel I/O ports that can be programmed for various control functions.”).

429. In my opinion, a POSA would have been motivated to use Adams’ microcontroller to provide the delay control signal to adjust the fractional and integer time delay (*See supra* §§X.Q.4, 6). There are multiple reasons for this.

430. First, the controller already exists in Adams’ system. Ex.1005, [0087], Fig.10. Second, the controller already provides a control signal to circuit 100 in Adams’ system. *Id.*, [0087] (“The output of the last logic circuit 1015 in **the last circuit stage 100 may be coupled to a microcontroller.**”), (emphasis added),

[0022] (“FIG. 1 shows an exemplary block diagram of a **microphone circuit 100** in an embodiment of the invention. A microphone 110 may be coupled to a microphone interface circuit 120, which may include a preamplifier (not shown) to initially boost an analog signal from the microphone, an analog to digital converter 112, **decimation unit 118**, and adder 117.”) (emphasis added). Therefore, it would have been advantageous to use the same controller to provide control signals to additional elements (e.g., fractional delay/ integer delay) on the same circuit 100, in my opinion. This would provide efficiencies, cost savings, and space savings from not having to develop/manufacture a separate controller. These efficiencies would have, in my opinion, furthered Adams’ aims. *See, e.g.*, Ex.1005, [0003]. Additionally, other efficiencies would have also resulted because the controller already provides a control signal having the same format used for delay control. *Id.*, [0045].

431. In my opinion, a POSA would have had a reasonable expectation of success because Adams already discloses the microcontroller being used to provide a gain control signal; the gain element, for which the microcontroller is used to provide a control signal, is included on the same circuit 100 as the delay elements and its control signal is provided via the command stream channel and using the same format for the control signal as for the delay control signal.

432. Adams' microcontroller, as modified, provides control signals to adjust the fractional and integer time delays, as explained above. It is my opinion that the microcontroller in Adams-Nguyen's system, as modified, so it provides the control signals to set the fractional and integer delays is the same or at least structurally equivalent to the claimed "controlling means" because it is a controller configured to provide such delay control signals, which is the same structure disclosed by the '055 patent specification. Ex.1001, 10:50-11:16, 11:27-57, 12:7-16, 13:4-7, 16:45-17:1. Additionally, a "microcontroller," such as disclosed by Adams, is a known structure. *See also* Ex.1014, p. 6 (Graf, 470) ("**microcontroller** – A complete microprocessor system on a chip. Includes on-chip the CPU, local RAM, local ROM or EPROM, clock and control circuits, and serial and parallel I/O ports that can be programmed for various control functions.").

433. The time delay provided in the Adams-Nguyen system, as described above (*supra* §§X.Q.4-6) is the "fractional time delay" and "integer time delay." Thus, the total time delay is the sum of the "fractional time delay" and "integer time delay."

434. As I discussed above, the microcontroller in the Adams-Nguyen system provides the delay control signal to adjust the "fractional time delay" and "integer time delay," and thus adjust the total time delay. Providing this control signal to

adjust the “fractional time delay” and “integer time delay” would result in the establishment of the total time delay.

435. Consistent with my discussion above, the digital signal output from the integer delaying means, is delayed by the total time delay, because the digital signal will have traversed both the fractional delaying means (which provides the fractional time delay) and the integer delaying means (which provides the integer time delay). *See supra* §§X.Q.4-6.

436. Also, the digital signal output from the integer delaying means includes a digital representation of the analog field quantity (sound or acoustic pressure) because it corresponds to the delayed, low-pass filtered, and decimated version of the signal output from the sensing means, which is for measuring the analog field quantity, as explained for 46[a]. *See supra* §X.Q.2(46[a]); *see also supra* §§X.Q.3-6(46[b]-46[d]). This digital representation is without the noise introduced by the oversampling means, given that the decimating low pass filtering of decimation filter stage 1 acts to remove the noise introduced by the oversampling means. *Supra* §§X.Q.5(46[d]), X.A; Ex.1014, pp. 3-4, Ex.1021, p. 1, Ex.1022, p. 1; Ex.1011, pp. 2-3; Exs.1007-1008. This understanding is consistent with the disclosure of the '055 patent, which acknowledges that “[l]ow pass filtering removes the high frequency noise resulting from the oversampling process.” Ex.1001, 3:58-60.

437. It is therefore my opinion that the microcontroller in Adams-Nguyen system performs the function “to adjust the fractional time delay and the integer time delay to establish a total time delay, wherein a resulting digital signal is delayed by a total time delay, wherein the total time delay is a sum of the fractional time delay and the integer time delay, and contains a digital representation of the analog field quantity without the noise introduced by the over sampling means.”

R. Claim 48

1. “The system of claim 46, wherein the total time delay is equal to a fraction of a baseband sampling period.”

438. In my opinion, a POSA would have found claim 48 obvious based on Adams in view of Nguyen.

439. As I explained above, it is my opinion that a POSA would have found claim 46 obvious based on Adams in view of Nguyen. *Supra* §X.Q(claim 46).

440. As I discussed above, Adams discloses fractional delaying means, namely fine variable integer delay 113, that delays the oversampled digital signal output from ADC by an integer number (*i.e.*, a “whole number”) of sampling clock cycles times the sampling clock period. *Supra* §X.Q.4(46[c]). Adams further discloses that this integer number of sampling clock cycles is “select[ed].” *Id.* Thus, the fractional delaying means provides a fine delay equal to a whole number multiplied times the ADC sampling clock period. *Id.*

441. As I discussed for claim element 46[c], “it would be possible to select a fractional delay amount” from this delay “associated with the original ADC output sample rates 1120” that is in increments of $1/128^{\text{th}}$ times the baseband sampling period. *See supra* §X.Q.4(46[c]).

442. As I also discussed for claim element 46[c], “it would be possible to select” a delay (which is referred to as an integer time delay) from the delay unit “associated with the output of the first stage” (i.e., integer delaying means) that is in increments of $1/8^{\text{th}}$ times the baseband sampling period. *See supra* §X.Q.6(46[e]).

443. In the Adams-Nguyen system (as described for claim 46), the total time delay is thus equal to the sum of the fractional time delay and the integer time delay. Both of these time delays are configurable, as I discussed above. *See supra* §§X.Q.4(46[c]), 6(46[e]).

444. As Adams further explains, the amount of time delay required corresponds to the delay “to insure [sic] that the audio data from its associated microphone corresponding to sound from a particular direction is time-aligned with the data represented by the cumulative sum arriving at the receiver of that microphone stage.” Ex.1005, [0022], [0025].

445. A POSA would have recognized that there are instances, including in Adams’ system, where the total delay required for a given microphone stage may be less than a baseband sampling period, depending on the microphone array geometry,

spacing of the microphones, signal propagation speed, steering angle, and focusing requirements.

446. In such instances, it would have been obvious to a POSA to set the fractional delay to be less than a baseband sampling period (and the integer delay to zero), for example. Adams in fact explains that “[l]ogic may be used to determine which of the filter stages a delay unit should be associated with.” Ex.1005, [0094]. For example, the “logic may be configured to select the filter stage having a lowest possible sample rate to provide a predetermined minimum fractional step size.” *Id.*

447. Thus, in such aforementioned instances, a POSA would have been motivated to set the fractional delay to less than a baseband sampling period, and the integer delay to zero. A POSA would have had a reasonable expectation of success because Adams expressly discloses having multiple delay units (e.g., fractional and integer delay units) and being able to selectively decide which stage a delay should be associated with. Adams also does not limit the minimum size of the integer delay. Accordingly, a POSA would have understood that zero (an example of a whole number) could be selected.

S. Claim 49

- 1. “The system of claim 46, wherein the total time delay is greater than a baseband sampling period.”**

448. In my opinion, a POSA would have found claim 49 obvious based on Adams in view of Nguyen.

449. As I explained above, it is my opinion that a POSA would have found claim 46 obvious based on Adams in view of Nguyen. *Supra* §X.Q(claim 46).

450. As I explained above, in the Adams-Nguyen system (as described for claim 46), the total time delay is equal to the sum of the fractional time delay and the integer time delay. *See supra* §X.R(claim 48). That means the total time delay is equal to the sum of a whole number multiplied times the ADC sampling clock period (which is the fractional delay) and a whole number multiplied times the lower sampling period (which is the integer delay). *See id.; supra* §§X.Q.4(46[c]), 6(46[e]). Both whole numbers of the fractional and integer delays may be selected. *See id.*

451. As Adams explains, the amount of time delay required corresponds to the delay “to insure [sic] that the audio data from its associated microphone corresponding to sound from a particular direction is time-aligned with the data represented by the cumulative sum arriving at the receiver of that microphone stage.” Ex.1005, [0022]; *see also id.*, [0025].

452. A POSA would have recognized that there are instances, including in Adams-Nguyen’s system, where the total delay required for a given microphone stage may be greater than a baseband sampling period, depending on the microphone array geometry, spacing of the microphones, signal propagation speed, steering angle, and focusing requirements.

453. In such instances, it would have been obvious to a POSA to set the sum of the fractional delay and integer delay to provide the requisite delay, greater than a baseband period. A POSA would have had a reasonable expectation of success because Adams expressly discloses having multiple delay units and being able to selectively decide which stage a delay should be associated with.

454. The total time delay being greater than a baseband sampling period is further disclosed in an example in Adams. *See* Ex.1005, [0050]. Specifically, in an example, the fully decimated sampling rate (and thus the baseband sampling rate) is 44.1 kHz. *Id.* This sample rate corresponds to a baseband sampling period equal to $(1 / \text{baseband sampling rate})$ and thus equal to $(1 / 44 \text{ kHz})$, which approximately equals 22 us (in other words, 22 microseconds). In this example, the total time delay is disclosed to be 3 ms (i.e., 3 milliseconds). *Id.* Thus, the total time delay (i.e., 3 ms) is greater than a baseband sampling period (i.e., 22 us).

T. Claim 50

- 1. “The system of claim 46, wherein the oversampled digital signal is digitized to create samples which are more than one bit deep.”**

455. In my opinion, a POSA would have found claim 50 obvious based on Adams in view of Nguyen.

456. As I explained above, it is my opinion that a POSA would have found claim 46 obvious based on Adams in view of Nguyen. *Supra* §X.Q(claim 46).

457. Even if the Adams-Nguyen system, as described for claim 46, did not disclose or otherwise render obvious that the oversampled digital signal is digitized to create samples which are more than one bit deep, a POSA would have at least been motivated by Nguyen's teachings to implement such a feature in the Adams-Nguyen system discussed for claim 46 above. *See supra* §X.P.1(claim 41).

458. The '055 patent uses the terminology "one bit deep" and "bit depth" to refer to the number of bits used to represent a sample. Ex.1001, 4:59-5:13 (emphasis added):

"Pulse density modulation (PDM) is such a digital conversion methodology that is **one-bit deep** where the sign is carried by the bit value where a "1" corresponds to a pulse of plus polarity (+A) and a "0" corresponds with a pulse of negative polarity (−A). Equation (3) indicates that a fractional delay can be selected based on a number of sampling clock cycles N from the range $1 \leq N \leq R$, and the time delay which is applied by delay element 216 is given by equation (4) as: $\Delta t = N * \tau_{SF}$. Where τ_{SF} is the period of the sampling clock. Where as described above, "fractional delay" refers to a fraction of a baseband sampling rate cycle.

Note that when other analog-to-digital digitization methodologies are used in the digital sensor 212 the resulting digital bit stream can be other than **one-bit deep**. In such cases, the oversampled digital signal at 212 can still be delayed with delay element 216, where the delay will be a multiple of a "sample" regardless of **how many bits are used to encode the "sample"** at the digital sensor 212. The minimum time delay increment will depend on the **bit depth** of the analog-to-digital digitization methodology used in the digital sensor 212."

459. Nguyen discloses that its MEMS microphone sensor is integrated with a follow-on circuit 100 including a sigma-delta modulator ADC. E.g., *supra*

§X.C.2(11[a]); Ex.1006, [0007]-[0008], [0012], [0013], [0027]-[0030]; *see also id.*, [0001], [0035]. The “circuit 100 may be shaped and sized for integration into a miniature MEMS microphone housing or package.” *Id.*, [0028]. Further, the sigma-delta modulator ADC, as Nguyen teaches, may include alternatively, a multi-bit quantizer. Nguyen’s multi-bit quantizer provides samples represented by multiple bits, whereas its single-bit quantizer provides samples represented by single bits. *See, e.g.*,

Id., [0012]:

“Each of the first and second sigma-delta modulators may comprise a single-bit quantizer or a multi-bit quantizer with their respective well-known advantages and disadvantages. If each of the first and second sigma-delta modulators comprises the single-bit or one bit quantizer the first and second digital signals may be conveniently supplied as first and second PDM signals, respectively. Alternatively, each of the first and second digital signals may be converted from native PDM format to a multi-bit or PCM format. Each of the first and second sigma-delta modulators preferably operates at an oversampled sampling frequency such as a sampling frequency between 1 MHz and 10 MHz.”

see also id., 30 (“The skilled person will appreciate that each of the first and second sigma- delta modulators 110, 112 may comprise a single-bit quantizer or a multi-bit quantizer.”).

460. A POSA would have been motivated to combine the teachings of Nguyen in implementing Adams’ system so that the digital microphone utilizes a MEMS sensor integrated with a circuit comprising a sigma-delta modulator ADC,

with the ADC including a multi-bit quantizer, as discussed above, and a POSA would have had a reasonable expectation of success. *Supra* §§X.A-B.

461. A POSA would have also understood that both Adams and Nguyen seek to reduce the assembly costs and space required to implement its digital microphones. For example, Adams in discussing the background art, complains about microphones to be individually wired to separate inputs of the signal processing device, which “requires additional expense and space” and “may affect the overall reliability of the system”:

“These beamforming algorithms were originally implemented in signal processing devices, which required each of the microphones to be individually wired to separate inputs of the signal processing device, typically an integrated circuit. The number of wires therefore increases proportionally with the number of microphones in the array. **Incorporating these extra wires requires additional expense and space in the device. Additionally, the extra wires may affect the overall reliability of the system as the likelihood of a defect, malfunction, or problem with one or more of the wire sets tends to increase as the number of wires increases.**”

Ex.1005, [0003] (emphasis added).

462. Nguyen similarly recognized an aim to reduce space consumption and power consumption, as well as lower assembly costs, and taught an approach which implemented a MEMS sensor integrated with a follow-on circuit 100 comprising a sigma-delta modulator ADC. *See* above discussion. Such integration provided a number of advantages:

“Hence, it is advantageous to integrate multiple functions in a single transducer unit such as a microphone. **This type of integration may reduce power consumption of active circuitry, reduce space consumption and lower assembly costs** of the portable communication or computing device in question. Portable communication devices furthermore often comprise a plurality of transducers such as microphones for voice and sound pick-up, recording and transmission which adds to the advantages of integrating multiple functions in a single transducer device.”

Ex.1006, [0002] (emphasis added); *see also, id.*, [0003].

463. Further, Nguyen, filed approximately two years after Adams, teaches that such MEMS sensors were “[c]ommonly used” by that time, “shaped and sized for portable audio devices such as smartphones, tablets and mobile phones etc.,” and “integra[ble] into a miniature MEMS microphone housing or package.” *Id.*, [0006]-[0007], [0028]. The use of sigma-delta modulator ADCs in digital signal processing was also prevalent and well known. *See supra* §§VI.C, E.

464. Given the overlapping aims of Adams and Nguyen, as well as Nguyen’s solution resulting in the integration of the MEMS microphone sensor and follow-on sigma-delta modulator ADC, the combination of Adams and Nguyen would provide the abovementioned benefits in Adams’ system, consistent with Adams’ aims.

465. In my opinion, this combination would have had a number of beneficial results, including saving space, reducing assembly costs, improving reliability, and facilitating integrability in Adams’ system, in line with Adams’ identified need, and Nguyen’s teachings.

XI. GROUND 2: CLAIMS 35 AND 40 ARE OBVIOUS BASED ON ADAMS, NGUYEN, AND NOUJAIM

466. It is my opinion that a POSA would have found claims 35 and 40 obvious based on the Adams-Nguyen combination in view of Noujaim.

A. Motivation to Combine

467. In my opinion, a POSA would have been motivated to apply Noujaim's multi-stage high-rate delay-register teaching to the Adams-Nguyen combination to extend the selectable fractional time delay range, including further beyond the baseband sampling period.

468. First, as discussed above, a POSA would have been motivated to combine Adams and Nguyen, and would have had a reasonable expectation of success. *See supra* §X.

469. Adams discloses a first time delay element, the first time delay element configured to receive as an input the oversampled digital output signal from the ADC and to output a time delayed oversampled digital output signal, wherein the time delayed oversampled digital output signal is time delayed by a fractional delay, the fractional delay is equal to an integer number of sampling clock cycles times the sampling clock period. *See supra* §§X.L.4(22[c]), X.N.4(38[c]), X.C.3(11[b]).

470. The sampling clock frequency of the ADC in the Adams-Nguyen system is also disclosed, as an example, to be 2.4 MHz. *See* Ex.1005, [0024] (“**The analog digital converter 112 may oversample the analog audio signal at higher**

frequencies, such as 2.4 MHz or higher in some embodiments, than are used to transmit the serial audio data between microphone circuits 100 in the microphone array, which may transmit data at 44 kHz.”) (emphasis added), claim 23 (“The system of claim 22, wherein **the ADC clock frequency is at least 2.4 MHz** and the serial data stream frame clock frequency is about 44 kHz.”) (emphasis added); Ex.1006, [0012] (“Each of the first and second sigma-delta modulators preferably operates at an oversampled sampling frequency such as a sampling frequency between 1 MHz and 10 MHz.”). Thus, given this exemplary oversampling frequency of 2.4 MHz, the Adams-Nguyen system provides fractional time delays in steps of $(1/2.4\text{MHz})$, which corresponds to the sampling clock period, and is approximately 0.416 us. Adams-Nguyen provides any “whole number” multiple of the sampling clock periods, as the fractional time delay. *See supra* §§X.L.4(22[c]), X.N.4(38[c]), X.C.3(11[b]). Thus, the fractional time delay in the Adams-Nguyen system is selectable in $\sim 0.416\text{-us}$ increments.

471. Following the fine variable integer delay 113 in the Adams-Nguyen system is a filter that low pass filters and decimates to a lower sampling rate of 44kHz (which is a baseband frequency in this system). *See supra* §§X.L.5(22[d]), X.N.5(38[d]), X.C.4(11[c]). This baseband frequency, 44kHz, corresponds to a baseband sampling period of $1/44\text{kHz}$ (or in other words approximately 22 us).

472. More than 20 years prior to the '055 patent, Noujaim discloses the same general high-rate-delay principle as Adams-Nguyen. More specifically, Noujaim discloses the use of delay unit (which are shift registers up to 80 stages in length) operating on oversampled bitstreams prior to decimation, with the desired time delay selected based on the number of shift-register stages through which the signal passes through before it is output. Ex.1010, Abstract, 8:65-9:42, 10:22-40.

473. In my opinion, a POSA would have been motivated, for example, to apply Noujaim's 80-stage delay-register teaching to Adams-Nguyen's 2.4 MHz oversampled bitstream delay unit to extend Adams-Nguyen's selectable delay range, up to approximately 33.3 us, which is beyond Adams-Nguyen's baseband sampling period (which approximately equals 22 us and corresponds to operating at a 44 kHz baseband frequency as I discussed above), to provide more flexibility to accommodate larger delays with its fine variable integer delay 113 unit, and accordingly retain the notably higher precision fine delay over a larger beam-steering selectable delay range. Such an implementation would have been consistent with Adams-Nguyen, given that Adams does not limit the size of the fine delay; Adams simply specifies that it is a whole number of ADC sampling periods. Adams also discloses that its fine delay provides "precise control over the steering direction." Ex.1005, [0022].

474. A POSA would have recognized that there are instances in which the total delay required for a given microphone stage may be greater than a baseband sampling period. In such instances, a POSA would have also recognized the advantage of the fine variable integer delay 113 unit providing a delay portion larger than one baseband sampling period, namely, that doing so would allow the higher precision delay resolution provided by the fine delay 113 to be utilized over a larger desired delay range. In such instances, it would have been obvious to a POSA to set the fine delay (provided by fine variable integer delay 113) to be greater than a baseband sampling period. In my opinion, using the fine variable integer delay 113 unit to provide the delay greater than a baseband period provides for a more flexible system for time delay and would have the benefit of maintaining the fractional delay precision over a larger beam-steering selectable time delay range. A POSA would thus have been motivated to combine Adams-Nguyen with Noujaim.

B. Reasonable Expectation of Success

475. In my opinion, a POSA would have had a reasonable expectation of success in combining Adams-Nguyen and Noujaim.

476. Both Adams-Nguyen and Noujaim disclose the same fundamental architecture: ADC oversampled bitstream delay units operating before decimation, with delay selected. *Supra* §§X.L.4-5(22[c]-22[d]), X.N.4-5(38[c]-38[d]), X.C.3-4(11[b]-11[c]); Ex.1010, 8:65-9:42, 10:22-40. Applying Noujaim's multi-stage

delay-register teaching to Adams-Nguyen's ADC oversampled bitstream delay unit is a straightforward application of a known component performing its known function. The combination would have extended the same delay implementation in the Adams-Nguyen combination, and it would not have changed its fundamental operation.

477. Thus, in my opinion, applying Noujaim's teachings regarding multi-stage delay-register length to Adams-Nguyen's architecture would have yielded predictable results, and would have had a reasonable expectation of success.

C. Claim 35

1. "The system of claim 22, wherein the fractional time delay is greater than a baseband sampling period."

478. It is my opinion that a POSA would have found claim 35 obvious based on the Adams-Nguyen combination in view of Noujaim.

479. As I explained above, it is my opinion that a POSA would have found claim 22 obvious based on Adams in view of Nguyen. *Supra* §X.L(claim 22).

480. As an initial matter, as discussed in the Technical Background section above, systems which relied on oversampled input signals, followed by delays and filters and decimation were well-known and in wide use long before the earliest claimed priority date of the '055 patent. *See supra* §VI. Thus, claim 35 represents a straightforward combination of well-known elements to achieve well-understood benefits.

481. As I also discussed above, Adams discloses that the fine delay (corresponding to claimed “fractional time delay”) provided by “fine integer delay 113” may be “select[ed]” as “a whole number of cycles at the higher frequency of the analog to digital converter 112.” Ex.1005, [0027]; *supra* §X.L.4(22[c]).

482. The sampling clock frequency of the ADC in the Adams-Nguyen system is also disclosed, as an example, to be 2.4 MHz. *See* Ex.1005, [0024] (“**The analog digital converter 112 may oversample the analog audio signal at higher frequencies, such as 2.4 MHz or higher** in some embodiments, than are used to transmit the serial audio data between microphone circuits 100 in the microphone array, which may transmit data at 44 kHz.”) (emphasis added), claim 23; Ex.1006, [0012]. Thus, the Adams-Nguyen system provides fractional time delays in steps of (1/2.4MHz), which corresponds to the sampling clock period, and is approximately 0.416 us. Adams-Nguyen provides any “whole number” multiple of the sampling clock periods, as the fractional time delay. *See supra* §§X.L.4(22[c]), X.N.4(38[c]), X.C.3(11[b]). Thus, the fractional time delay in Adams-Nguyen system is selectable in ~0.416-us increments. Adams does not limit the size of the fine delay; Adams simply specifies that it is a whole number of ADC sampling periods.

483. As I also discussed above, the decimation module in the Adams-Nguyen system low pass filters and decimates a time delayed oversampled digital signal to a lower frequency, namely the “serial data stream frame rate,” which is

44kHz. *See supra* §X.L.5(22[d]); Ex.1005, [0024], [0028]; *see also id.* [0050], [0059], claim 23. This serial data stream frame rate is a baseband digital signal rate. *See supra* §§X.I(claim 17), X.K(claim 21).

484. Noujaim teaches the same high-rate-delay principle as in Adams-Nguyen. Noujaim discloses ADCs that output one-bit digital signals, variable delay shift registers that delay those signals before summation, and a decimator that later reduces the sample rate. Ex.1010, Abstract, 3:26-4:5, 8:65-9:42, 10:22-40. Noujaim teaches delay registers that are “80 stages in length,” and the desired time delay is selected based on the shift-register stage from which the signal is output. *Id.*, 9:22-42.

485. A POSA would have been motivated to apply Noujaim’s multi-stage high-rate delay-register teaching to the Adams-Nguyen combination to advantageously allow the higher precision delay resolution provided by the fine variable integer delay 113 to be utilized over a larger desired delay range, including over a delay range greater than one baseband period. *See also supra* §XI.A.

486. Noujaim discloses that in delay implementations using oversampled signal rates, high-rate delay registers may include many stages—e.g., 80 stages—and that the desired time delay is selected based on the shift-register stage from which the signal is output. Ex.1010, Abstract, 8:65-9:42, 10:22-40. Applying Noujaim’s 80-stage delay-register teaching to Adams-Nguyen’s 2.4MHz bitstream

fine variable integer delay 113 unit would have predictably extended Adams-Nguyen's selectable high-precision delay range up to approximately 33.3 us, exceeding Adams-Nguyen's baseband sampling period (~22us, which corresponds to operating at a 44 kHz baseband frequency, as I discussed above). *See also supra* §XI.B.

D. Claim 40

1. “The method of claim 38, wherein the fractional time delay is greater than a baseband sampling period.”

487. It is my opinion that a POSA would have found claim 40 obvious based on the Adams-Nguyen combination in view of Noujaim.

488. As I explained above, it is my opinion that a POSA would have found claim 38 obvious based on Adams in view of Nguyen. *Supra* §X.N(claim 38).

489. As an initial matter, as discussed in the Technical Background section above, systems which relied on oversampled input signals, followed by delays and filters and decimation were well-known and in wide use long before the earliest priority date of the '055 patent. *See supra* §VI. Thus, claim 40 represents a straightforward combination of well-known elements to achieve well-understood benefits.

490. As I also discussed above, Adams discloses that the fine delay (corresponding to claimed “fractional time delay”) provided by “fine integer delay

113” may be “select[ed]” as “a whole number of cycles at the higher frequency of the analog to digital converter 112.” Ex.1005, [0027]; *supra* §X.N.4(38[c]).

491. The sampling clock frequency of the ADC in the Adams-Nguyen system is also disclosed, as an example, to be 2.4 MHz. *See* Ex.1005, [0024] (“**The analog digital converter 112 may oversample the analog audio signal at higher frequencies, such as 2.4 MHz or higher...**”) (emphasis added), claim 23; Ex.1006, [0012]. Thus, the Adams-Nguyen system provides fractional time delays in steps of (1/2.4MHz), which is the sampling clock period), and equals ~0.416 us. Adams-Nguyen provides any “whole number” multiple of the sampling clock periods, as the fractional time delay. *See supra* §§X.L.4(22[c]), X.N.4(38[c]), X.C.3(11[b]). Thus, the fractional time delay in Adams-Nguyen system is selectable in ~0.416-us increments. Adams does not limit the size of the fine delay; Adams simply specifies that it is a whole number of ADC sampling periods.

492. As I also discussed above, the filter in the Adams-Nguyen system low pass filters and decimates a time delayed oversampled digital signal to a lower frequency, namely the “serial data stream frame rate,” which is 44kHz. *See supra* §X.N.5(38[d]); Ex.1005, [0024], [0028]; *see also id.* [0050], [0059], claim 23. This serial data stream frame rate is a baseband digital signal rate. *See supra* §§X.N.5(38[d]), X.I(claim 17), X.K(claim 21).

493. A POSA would have been motivated by Noujaim's teachings to implement Noujaim's multi-stage high-rate delay-register teaching to the Adams-Nguyen combination and had a reasonable expectation of success, for all the reasons discussed above for claim 35. *See supra* §XI.C(claim 35).

XII. SECONDARY CONSIDERATIONS

494. I am not aware of any secondary-considerations evidence that would support a finding of non-obviousness for the '055 patent.

XIII. CONCLUSION

495. For all the reasons stated above, it is my opinion that the challenged claims of the '055 patent are unpatentable.

496. This declaration and my opinions are made to the best of my knowledge and understanding and are based on the material available to me at the time of signing this declaration. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Dated: August 6, 2026

By: 
Thomas W. Kenny, Ph.D.