

Filed on behalf of Petitioners

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

META PLATFORMS, INC. AND SAMSUNG ELECTRONICS CO., LTD.,
Petitioners,

v.

GAEA, LLC,
Patent Owner.

Case No. IPR2026-00426
U.S. Patent No. 11,907,553

**Petition for *Inter Partes* Review of
U.S. Patent No. 11,907,553**

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TABLE OF EXHIBITS

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1001	U.S. Patent No. 11,907,553 to Johnson, et al. (“the ’553 Patent”)
1002	File History of U.S. Patent No. 11,907,553
1003	Declaration of Heiner Litz (“Litz Decl.”)
1004	Curriculum Vitae of Heiner Litz
1005	U.S. Patent Application Publication No. 2015/0052167 to Olster et al. (“Olster”)
1006	U.S. Patent Publication No. 2016/0313943 to Hashimoto et al. (“Hashimoto”)
1007	U.S. Patent No. 9,075,851 to Kilian et al. (“Kilian”)
1008	U.S. Patent No. 8,874,835 to Davis et al. (“Davis”)
1009	U.S. Patent Application Publication No. 2012/0166749 to Eleftheriou et al. (“Eleftheriou”)
1010	U.S. Patent Application Publication No. 2012/0246435 to Meir et al. (“Meir”)
1011	U.S. Patent Application Publication No. 2015/0032938 to Salessi (“Salessi”)
1012	U.S. Patent Application Publication No. 2015/0146364 to Chou et al. (“Chou”)
1013	RESERVED

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1015	U.S. Patent Application Publication No. 2014/0089278 to Lovinger et al. (“Lovinger”)
1016	File History of U.S. Patent No. 10,776,023
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1018	Timothy Feldman and Garth A. Gibson, ‘Shingled Magnetic Recording’ ACM Queue / CMU, 2013.
1019	Albert Chen and Jim Malina, ‘Addressing Shingled Magnetic Recording Drives with Linear Tape File System’ SNIA Storage Developer Conference, 2013
1020	Jorge Campello, ‘SMR: The Next Generation of Storage Technology’ SNIA Storage Developer Conference, 2015.
1021	Samarth Bhargava, ‘Lowering HAMR Near-Field Transducer Temperature via Inverse Electromagnetic Design’ IEEE Transactions on Magnetics, Apr. 2015.
1022	Yu Cai et al., ‘Read Disturb Errors in MLC Nand Flash Memory: Characterization, Mitigation, and Recovery’ DSN 2015.
1023	Nitin Agrawal et al., ‘Design Tradeoffs for SSD Performance’ USENIX Annual Technical Conference, 2008
1024	Feng Chen, David A. Koufaty, and Xiaodong Zhang; ‘Understanding Intrinsic Characteristics and System Implications of Flash Memory Based Solid State Drive’ SIGMETRICS 2009

Exhibit No.	Description
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1034	NVM Express, 'NVM Express Revision 1.0' Mar. 1, 2011
1035	NVM Express, 'NVM Express Revision 1.2' Nov. 3, 2014
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Exhibit No.	Description
1037	Trusted Computing Group, ‘Storage Security Subsystem Class: Opal Specification Version 2.00’ Feb. 24, 2012
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1039	Fred Knight and David L. Black, ‘SBC-3 Thin Provisioning Commands’ T10 proposal 08-356r5, Jan. 14, 2009
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1043	John Colgrove et al., 'Purity: Building Fast, Highly-Available Enterprise Flash from Commodity Components,' SIGMOD 2015
1044	EMC Corporation, 'XtremIO Data Protection (XDP): Flash-Specific Data Protection,' White Paper, July 2014
1045	U.S. Patent Application Publication No. 2004/0230795 to Armitano (“Armitano”)
1046	U.S. Patent Application Publication Nos. 2007/0244939 and 2007/0244940 to Devarakonda (“Devarakonda”)
1047	U.S. Patent Application Publication No. 2011/0022642 to deMilo (“deMilo”)

Exhibit No.	Description
1048	U.S. Patent Application Publication No. 2010/0145917 to Bone (“Bone”)
1049	U.S. Patent Application Publication No. 2010/0332401 to Prahlad (“Prahlad”)
1050	U.S. Patent Application Publication No. 2014/0297695 to Dejana (“Dejana”)
1051	IBM, ‘Understanding Hard Drive Media Defects White Paper – Servers’ IBM Product Documentation, Dec. 1997

I. INTRODUCTION

Meta Platform, Inc. (“Meta”) and Samsung Electronics Co., Ltd. (“Samsung”) (together, “Petitioners”) respectfully request *inter partes* review of claims 1-7, 9-20, and 26-31 of U.S. Patent No. 11,907,553 (EX1001, “’553 Patent”).

For decades, storage devices have used storage policies to determine how to store data. In the 1970s, for example, IBM implemented centralized, policy-based rules for its storage systems, which freed administrators from manually managing files. As storage systems advanced, so did storage policies, eventually allowing hosts (such as administrators, users, and client devices) to set storage policies by sending the policy to the storage device as opposed to relying on a policy set at manufacture. By 2016, storage policies, including user-configurable policies, were common and well-known.

During prosecution of the ancestor patent that originated the family of the ’553 Patent, the Examiner repeatedly rejected the pending claims as anticipated and obvious. Critically, the Examiner found an apparatus nearly identical to those claimed in the ’553 Patent—a storage device with a programmable processor, device controller, and solid-state memory that stores content based on a policy—anticipated by the prior art. The Examiner only allowed the claims after the Applicant amended the claims to recite receiving a storage policy “from a host” that “indicates a recording method for writing data in a storage media.” But this limitation is found

nowhere in the claims of the '553 Patent. Thus, the '553 Patent incorrectly issued—erroneously omitting the allowable subject matter of its ancestor.¹ *See Activision Blizzard, Inc. v. Milestone Entertainment, LLC*, IPR2025-00708, Paper 13, 2 (Aug. 14, 2025) (referring ultimately-instituted petition where “the challenged claims omit limitations added during prosecution of the parent patent that appear to have been the patent examiner’s reason for allowing the parent patent’s claims”).

As such, Meta respectfully requests that the Director institute *inter partes* review, and the Board find all the challenged claims of the '553 Patent unpatentable, as the Examiner found during the prosecution of the ancestor patent.

II. MANDATORY NOTICES

A. Real Parties-in-Interest

The real parties-in-interest are Meta Platforms, Inc. and Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

B. Related Matters

U.S. Patent Office records indicate that the '553 Patent is assigned to Gaea,

¹ Though the challenged claims would still be unpatentable even if they did include this limitation, as shown in the Petitioner’s challenge against the ancestor patent. *See* IPR2026-00425, Paper 1 (challenging certain claims in U.S. Patent No. 10,776,023).

LLC (“Patent Owner”), which is currently asserting the ’553 Patent in the following concurrent litigations: *Gaea, LLC v. Meta Platforms, Inc.*, 4:26-cv-00348 (N.D. Tex.) (filed on March 23, 2026) and *Gaea, LLC v. Samsung Electronics Co., Ltd.*, 2:26-cv-00264 (E.D. Tex.) (filed on March 31, 2026).

There are three patents asserted in the concurrent litigation. Petitioners have filed petitions for *inter partes* review against the other asserted patents at substantially the same time: U.S. Patent No. 10,776,023 (IPR2026-00425), and U.S. Patent No. 12,265,715 (IPR2026-00427).

C. Notice of Counsel and Service Information

Petitioners provide the following designation of counsel:

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Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney accompanies this petition. Petitioners consent to electronic service by e-mail.

D. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a) to Deposit Account 50-2613.

E. Grounds for Standing

Petitioners certify pursuant to 37 C.F.R. § 42.104(a) that the '553 Patent is available for *inter partes* review and that Petitioners are not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this Petition.

III. IDENTIFICATION OF CHALLENGES

Ground	Claims	Statute	Prior Art
1	1-2, 5-7, 16-17, 19-20, 26-27, 30-31	35 U.S.C. § 103	Meir ² in view of Salessi ³
2	3-4, 18, 28-29	35 U.S.C. § 103	Meir in view of Salessi and Chou ⁴
3	9-10, 13-15	35 U.S.C. § 103	Meir in view of Salessi and Lovinger ⁵

² Meir is prior art under 35 U.S.C. §§ 102(a)(1), 102(a)(2), and 102(b)(1).

³ Salessi is prior art under 35 U.S.C. §§ 102(a)(1), 102(a)(2), and 102(b)(1).

⁴ Chou is prior art under 35 U.S.C. §§ 102(a)(1), 102(a)(2), and 102(b)(1).

⁵ Lovinger is prior art under 35 U.S.C. §§ 102(a)(1), 102(a)(2), and 102(b)(1).

4	11-12	35 U.S.C. § 103	Meir in view of Salesi, Lovinger, and Chou
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IV. BACKGROUND

A. Technology Overview

For decades, storage devices have used storage policies to determine how to store data. EX1003, ¶¶25-27. In the 1980s, user-configurable storage policies garnered popularity with the advent of hierarchical storage management. *Id.* These systems allowed users or administrators to define rules for automatically migrating data. *Id.*, ¶¶35-38. For example, IT administrators could direct storage devices to store data in different tiers, storing hot data (frequently used data) in the more expensive disk drives in one tier, while cold data (less frequently used or LFU data) in cheaper, long-term tape archives in another tier. *Id.*

In the late 1980s and 1990s, the invention of NAND memory (the chip inside SSDs) revolutionized data storage, allowing data to be written in large blocks rather than individually, leading to cheaper, higher-capacity storage. *Id.*, ¶¶25-27. With cheaper storage, more storage policies included rules and instructions related to redundancy schemes like RAID (Redundant Arrays of Independent Disks), which defined how content is stored, protected, and accessed across multiple drives. *Id.*, ¶¶39-40. Specifically, RAID can process content for storage by mirroring content (storing an exact copy of data in another drive), striping data (dividing data into

blocks for storage), and calculating parity information (information that can be used to rebuild the data if a drive fails). *Id.* The advent of SSDs allowed RAID, which increased reliability, to be implemented more cost-effectively, particularly when used in conjunction with compression (which reduced the size of the data) and encryption (which allowed failed drives to be discarded without risk that a third party could recover the data). *Id.*

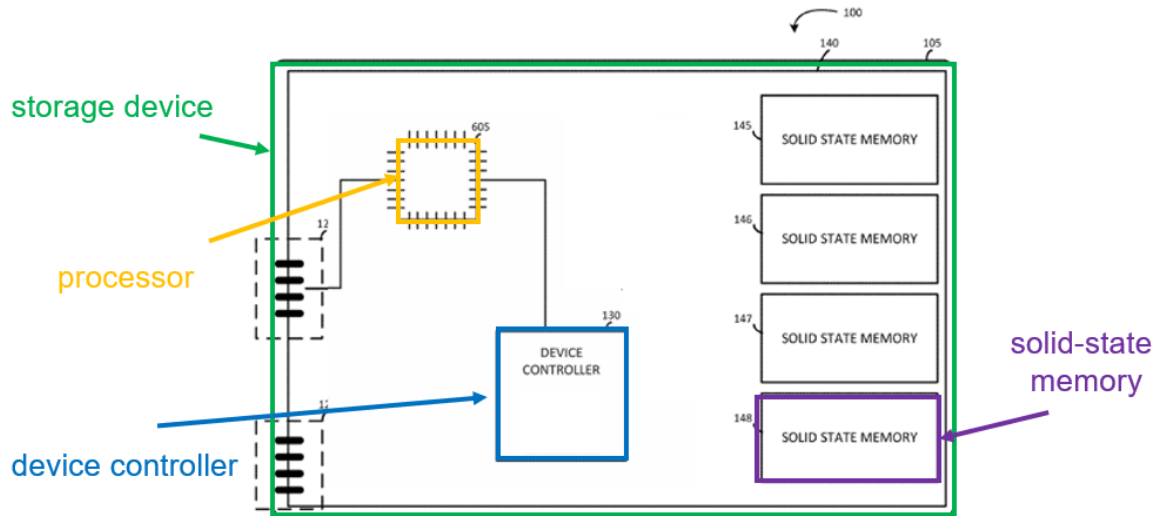
But a primary drawback of NAND memory is its limited lifespan—each memory cell can only endure a finite number of write and erase cycles before it wears out. *Id.*, ¶¶32-34. By the late 2000s when SSDs became mainstream, wear-leveling (evenly distributing write and erase cycles across all NAND memory cells) and bad block (defect) management became an important recording method for any NAND memory storage policy. *Id.*

Thus, by 2016 (the priority date of the '553 Patent), storage policies (including those defining RAID, compression, and encryption) were well-known, routine, and conventional.

B. '553 Patent

The '553 Patent describes well-known “data storage devices with configurable policy-based read and write behavior.” EX1001, 1:22-24. The '553 Patent complains that in prior art storage devices, storage decisions were “largely made by the manufacturer at the time of design and/or manufacture” providing users

“very little to no influence” on how data is stored. *Id.*, 1:40-44. The ’553 Patent purportedly addresses that problem using a routine storage device policy that allows “a user to customize the operation of the storage device.” *Id.*, 3:14-15.



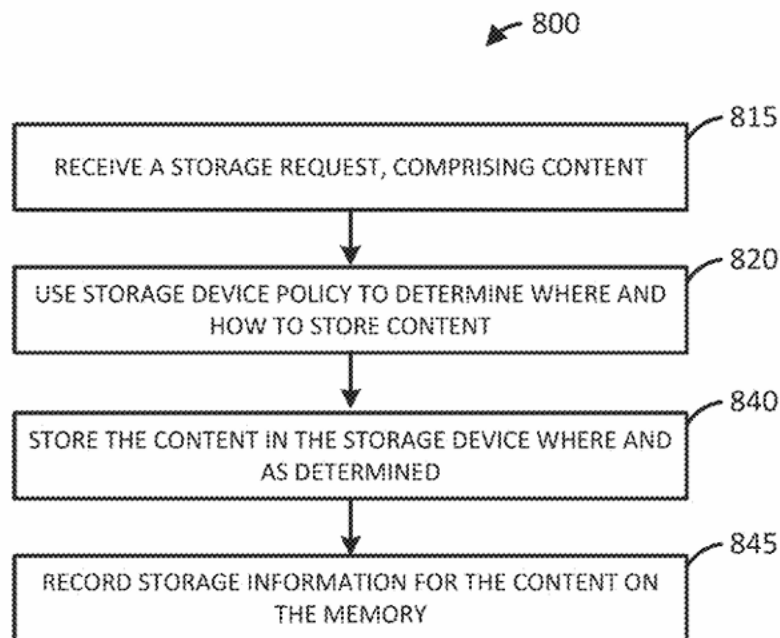
EX1001, Figs. 1B and 6 (modified and annotated)

The claimed **storage devices** include a **processor**, **device controller**, and **solid-state memory** such as solid-state memory 45 (Figure 1B). *Id.*, FIGS. 1B, 6, 1:47-48. The ’553 Patent discloses that the storage drive “uses a storage device policy...to determine where to store the content.” *Id.*, 14:41-43. “This determination can relate partially to the content being stored, and partially to the storage media.” *Id.*, 14:43-45.

The **processor**, such as programmable logic device 605, “can be programmed by user of the drive 600 for any operation need that is desired.” *Id.*, 11:21-23. Accordingly, the programmable processor processes the data according to the

storage policy, but can also implement other processing operations such as “custom encryption through hardware” or “compression.” *Id.*, 11:23-41. The claims recite an application (comprising code or program instructions) stored on a **device memory** coupled to the programmable processor, that directs the programmable processor on how to operate.

The **processor** transfers and receives data to and from the **solid-state memory** through the **device controller**. The “programmable logic device 605 is shown connected between interface connector 125 and device controller 130.” *Id.*, 11:42-44.



EX1001, Fig. 8A

In Figure 8A, the '553 Patent describes one implementation of writing content

according to a storage device policy. *Id.*, FIG. 8A, 14:31-15:5. “A user sends a request to store content in step 815.” *Id.*, 14:33-34. The ’553 Patent explains that “this request comprises content to be stored.” *Id.*, 14:37-38. At step 820, the programmable processor “uses a storage device policy...to determine where to store the content.” *Id.*, 14:41-43. The programmable processor will also process the content based on the storage policy such as compressing or encrypting the content. *Id.*, 11:21-36. At step 840, “the device controller can write the content to the storage media 110 as determined in step 820.” *Id.*, 14:59-60.

The claimed solid-state drive can further include “case 105, which physically supports” the hardware components of the drive (*id.*, 4:39-40).

C. The Challenged Claims

The challenged claims are entitled to an effective date of no earlier than November 7, 2016.⁶ The ’553 Patent has 36 claims, including 6 independent claims (apparatus claims 1, 9, 16, 21, 26, 32) and 30 dependent claims. The Petition challenges four independent claims and 21 dependent claims.

Independent claims 1, 9, 16, and 26 each recite an apparatus with four

⁶ Petitioners do not concede that any challenged claim is entitled to this priority date. For the purpose of this petition, it is unnecessary to break the priority chain to a later date.

components: a solid-state memory, a device memory, a programmable processor, and a device controller, together with an application stored on the device memory.

For claims 1 and 9, the application's instructions direct the programmable processor to perform a write operation: to process content for storage based on a storage policy, and transfer the content to the device controller, which receives the content and stores it on the solid-state memory. For claim 1, the storage policy is stored in the device memory, and retrieved in response to a storage request. For claim 9, the storage device policy is received as part of the storage request.

For claim 16, the application's instructions directs the programmable processor to perform a read operation: to retrieve a storage device policy from the device memory, direct the device controller to read the requested content from the solid-state memory, receive the requested content from the device controller and process the requested content based on a storage policy, and (5) transfer the requested content to the host.

Claim 26 is directed to responding to a storage request (similar to claim 1) and then responding to a content request (similar to claim 16).

D. Prosecution History

The Examiner materially erred in at least two ways during the prosecution of the '553 Patent. *First*, the Examiner allowed the Applicant to omit the subject matter added during the grandparent prosecution that allowed the grandparent's claims.

Second, the Examiner failed to perform an adequate search on the subject matter added to the claims of the '553 Patent for allowance—"process the content for storage based on the storage device policy."

1. The Grandparent '023 Patent

The '553 Patent is a second continuation of the '023 Patent, which originated this patent family. During the prosecution of the '023 Patent, the Applicant struggled to identify allowable subject matter. Specifically, the pending claims of the '023 Patent were repeatedly rejected on both §§ 102 and 103 grounds over U.S. Patent App. Pub. No. 2015/0052167 to Olster et al. ("Olster"). Notably, the Examiner found Olster anticipated pending claim 26, which substantially mirrors claim 1 of the '553 Patent:

26. An apparatus comprising:

a storage device;

a device controller operatively coupled with the storage device, comprising a memory, the device controller configured to receive content to be stored on the storage device;

a programmable processor, communicatively coupled with the device controller such that the content received by the device controller to be stored on the storage media must pass through the programmable processor; and

an application stored on the memory and comprising instructions that, when executed, direct the device controller to at least store the content on the storage media after the content has been processed by the programmable processor.

EX1016, 12. After some back and forth, the Examiner eventually allowed the claims after the Applicant amended them to require that the device controller receives “from a host” a storage policy that “indicates at least a recording method for writing content to the storage media.” *Id.*, 224. The ’023 Patent subsequently issued on September 15, 2020.

2. The ’553 Patent

Although the Examiner only allowed the claims of the ’023 Patent after the Applicant amended the claims to recite that the device controller receives “from a host” a storage policy that “indicates at least a recording method for writing content to the storage media,” none of the continuations following the ’023 Patent included this limitation. Indeed, just as in the ’023 Patent, the Examiner found Olster rendered obvious the pending claims of the ’553 Patent.

On May 25, 2023, the Applicant amended the claims to recite that the “programmable processor” not only store data based on the storage policy (as in the ’023 Patent) but also “process the content for storage based on the storage device policy.” *Id.*, 300. Grossly mischaracterizing Olster as merely a “distributed search method patent,” the Applicant argued that the Olster “does not suggest that the controller or any processing element...perform any specific data processing operations like encryption,” incorrectly asserting that Olster’s controller only

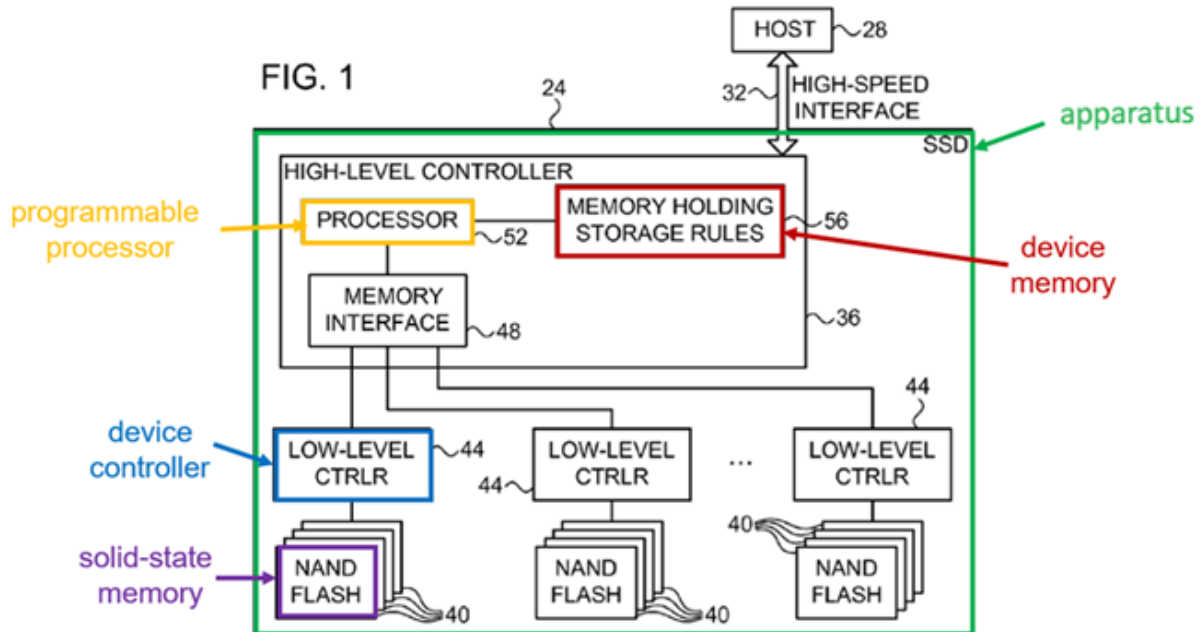
“participates in a distributed search process for data.” *Id.*, 273-274. Thus, the Applicant argued that Olster does not store data, let alone process data for storage.

On June 23, 2023, the Examiner issued a notice of allowance with no reasons for allowance. *Id.*, 321. And though the Examiner only allowed the claims after the Applicant amended the claims to include the limitation “process the content for storage based on the storage device policy,” the Examiner did not search for “process,” “encrypt,” or any other equivalent term in the EAST Search History to identify prior art disclosing that limitation.

V. THE PRIOR ART

A. Meir (EX1010)

Meir discloses each limitation of the independent claims of the '553 Patent except that it does not explicitly disclose that the application directs the programmable processor to *process content for storage* using *compression* and *decompression* or *encryption* and *decryption*. Like the '553 Patent, Meir discloses data storage devices with configurable policy-based read and write behavior. EX1010, Abstract (“A data storage method includes...holding a definition of a policy to be applied by the memory controller in the execution of the memory access commands in the memory unit”), [0055] (“one or more of the rules in the memory controller policy may be configurable”).



EX1010, Fig. 1 (annotated)

Meir discloses a **solid-state disk** (“SSD”) 24 which comprises a high-level controller 36 which includes **processor** 52, and **low-level controller** 44 which is coupled with **memory units** 40. EX1010, FIG. 1, [0030] (“SSD 24 comprises a high-level controller 36, which stores data in one or more non-volatile memory units 40”), [0033] (“[h]igh-level controller 36 comprises a memory interface 48 for communicating with memory units 40 (in the present example via low-level controllers 44), and a processor 52 that carries out the various functions of the high-level controller. High-level controller 36 comprises a memory 56...memory 56 holds a definition of a policy that the memory controller applies in storing data in memory units 40”).

Like the '553 Patent, Meir describes a solid-state drive with configurable policy-based read and write behavior. EX1010, [0013] (“a data storage method including receiving from a memory controller a communication...reporting a definition of a policy to be applied by the memory controller in accessing one or more memory units”). As Meir explains, “one or more of the rules in the memory controller policy may be configurable.” *Id.*, [0055].

Like the '553 Patent, the processor 52 is “programmed in software to carry out the functions described.” *Id.*, [0034]. Accordingly, the programmable processor processes the data for storage according to the storage policy including rules applied to the data such as “applying a redundant storage scheme such as Redundant Array of Inexpensive Disks.” *Id.*, [0025]. “[R]edundancy rules may specify whether such a scheme is applied or not, as well as various parameters of the redundant storage scheme.” *Id.*, [0048]. For example, the parameters may include “the formulas or rules used by the memory controller in calculating parity information over the data.” *Id.* Software (comprising program instructions) can be stored along with the storage device policy in memory 56, which is coupled to processor 52 and can direct processor 52 how to operate. *Id.*, [0034] (“The software may be downloaded to the processors...and/or stored on non-transitory tangible media, such as magnetic, optical, or electronic memory”).

B. Salessi (EX1011)

Salessi discloses *process[ing] the content*, including compressing or encrypting the content for storage and decompressing or decrypting the content upon retrieval.

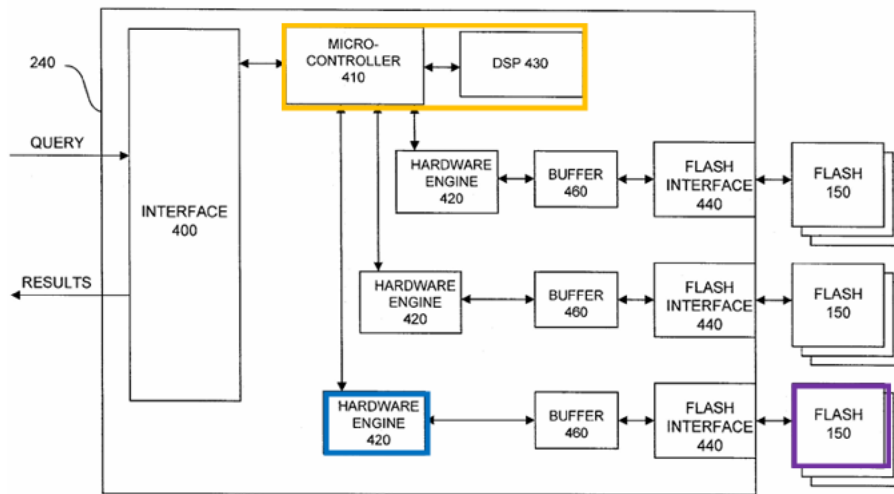


FIG. 7

EX1011, Fig. 7 (annotated)

Like the '553 Patent and Meir, Salessi's SSD "includes flash memory and an SSD processing unit." EX1011, FIG. 7, [0006]. Salessi's processing unit "process[es] the data...being stored or retrieved from the flash memory." *Id.*, [0006]. "Processing capabilities incorporated into the SSD may include encryption and decryptions [and] compression and decompression." *Id.* Salessi further teaches that the processing unit "us[es] a processing algorithm[] to generate processed data." *Id.*, [0023].

C. Chou (EX1012)

Chou discloses a printed circuit board mounting components within a case, as required in certain dependent claims. Like the '553 Patent and Meir, Chou discloses a solid-state drive (SSD). Chou's SSD includes a printed circuit board assembly ("PCBA") and a housing that supports the PCBA. EX1012, [0006] ("A SSD generally includes a printed circuit board assembly (PCBA) within a metallic housing."), [0034] ("To assemble the SSD 100, the PCBA 112 is placed inside the upper and lower covers 114a and 114b"). Chou also describes "[o]ne or more memory modules and other electronic components 122," which can be the solid-state memory, device memory, programmable processor, device controller and other components, are mounted "on the PCBA." *Id.*, [0033].

D. Lovinger (EX1015)

Lovinger discloses a storage request that includes a policy, as required by claim 9. Like the '553 Patent and Meir, Lovinger discloses a storage device for storing data. EX1015, Abstract. Lovinger discloses a method "for storing content based on one or more attributes associated with the content." EX1015, [0003]. The client "may transmit content...with information corresponding to the retention policy." *Id.*, [0040]. "[W]hen the content and retention policy have been received, the server 120 writes the content 112 to one or more storage devices associated with the server 120 according to the retention policy." *Id.* This enables a client "to store

content according to the retention policy without reprogramming device firmware.”
Id., [0041].

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) in 2016 would have had at least a bachelor’s degree in electrical engineering, computer science, computer engineering, or a similar technical field, with at least two years of experience in the field of data storage systems. Additional experience could substitute for less education, and additional education could likewise substitute for less experience. EX1003, ¶¶57-59.

This Petition does not turn on this precise definition, and the challenged claim would be unpatentable from the perspective of any reasonable person of ordinary skill in the art at the relevant time. *Id.*

VII. CLAIM CONSTRUCTION

The Board construes the claims “using the same claim construction standard that would be used” in district courts. 37 C.F.R. §42.100(b). This Petition establishes the prior art meets each of the claim limitations under its plain and ordinary meaning.⁷ Thus, the claim terms require no express construction. *Nidec*

⁷ Petitioners reserve the right to provide an express construction consistent with that applied in this proceeding and the Parallel Litigation. *See Caption Health, Inc. v.*

Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd., 868 F.3d 1013, 1017 (Fed. Cir. 2017); *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

VIII. GROUND 1: MEIR IN VIEW OF SALESSI RENDERS OBVIOUS CLAIMS 1-2, 5-7, 16-17, 19-20, 26-27, AND 30-31

The data storage system resulting from the combination of the teachings of Meir and Salessi is a SSD including a processor that executes access commands from a host according to a policy that includes algorithms and rules for compression, decompression, encryption, and decryption. EX1003, ¶72.

A. Motivation to Combine

A POSITA would have been motivated to modify the software (*application*) and policy (*policy*) stored in memory 56 (*device memory*) of Meir to direct the processor 52 to compress and encrypt the data to be stored according to algorithms and rules in the policy as taught by Salessi. EX1003, ¶¶73-84.

First, Salessi expressly teaches that compression and encryption rules may be used in the implementation of redundancy schemes like the one taught in Meir. EX1011, [0057] (compression and encryption “may be used in a redundant array of independent disks (RAID) to achieve similar advantages in optimizing performance

The Univ. of British Columbia, IPR2025-01422, Paper 15, 3 (Director Dec. 18, 2025).

and resource utilization.”); EX1010, [0025]. A POSITA implementing Meir’s system would have naturally looked at teachings improving the performance of solid-state drives, particularly, those implementing RAID schemes. EX1003, ¶¶74-76.

Second, it would have been well-understood by a POSITA that modifying policies to include compression and encryption would improve the performance and security of the data storage system, respectively. EX1010, [0036]; EX1011, [0050]; EX1003, ¶¶77-78.

Third, modifying Meir’s policy to include Salessi’s compression and encryption algorithm and rules would also result in cost and resource savings. EX1003, ¶¶80-81. Because compression allows the data storage system to store more data, an administrator could use compression to expand the storage capacity of the system without expending resources on additional drives. *Id.* Further, encryption conserves resources that may be expended in ensuring that sensitive data is protected when a drive fails. *Id.*

Fourth, storing less data through compression reduces wear on SSDs. EX1003, ¶82. A major drawback of NAND memory (the chip inside SSDs) is its limited lifespan—each memory cell can only endure a finite number of write and erase cycles before it wears out. *Id.* Reducing wear will increase the life of the drives and reduce drive failure.

Fifth, modifying the policy to include encryption would have been driven by regulatory compliance requirements. EX1003, ¶¶83-84. At the relevant time, privacy mandates such as GDPR had just been enacted. *Id.* Encryption would have provided an efficient approach to render certain personal data requiring protection to be unreadable. *Id.*

B. Reasonable Expectation of Success

A POSITA would have been able to modify Meir's processor 52 to perform compression, decompression, encryption, and decryption according to the storage policy with a reasonable expectation of success. EX1003, ¶¶85-91.

First, the storage drives of Meir and Salessi have similar structures and components. EX1010, FIG.1; EX1011, FIGS. 2, 4, 7; EX1003, ¶¶85-88. Meir and Salessi's SSDs both include memory controller or processing unit that interfaces with the solid-state memory. EX1010, [0031], [0033]; EX1011 [0047], [0055].

Second, Meir and Salessi both teach optimization of performance through parallelism and pipeline rules utilizing multiple processors. EX1010, [0042]; EX1011, [0055]; EX1003, ¶¶87-89. Specifically, Meir teaches a high-controller 36 including processor 52 (*programmable processor*) that interfaces with low-level controllers 44 (*device controller*) and Salessi teaches a microcontroller 410 (*programmable processor*) that interfaces with hardware engines 420 (*device controller*), where the one processor executes various operations including

processing data and the other interfaces with memory. EX1010, [0030], [0033]; EX1011, [0042], [0047], [0055].

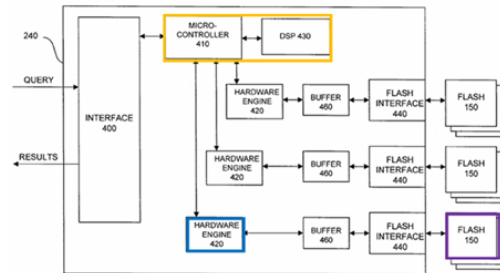
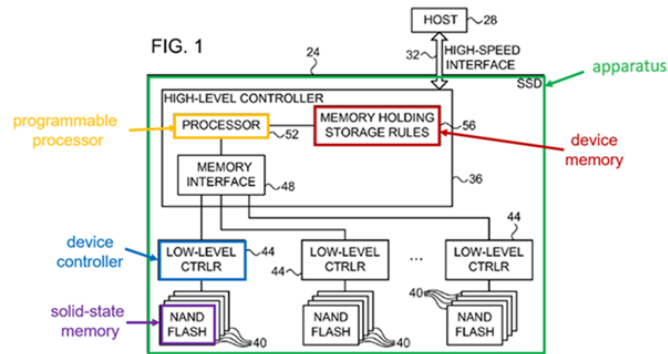


FIG. 7

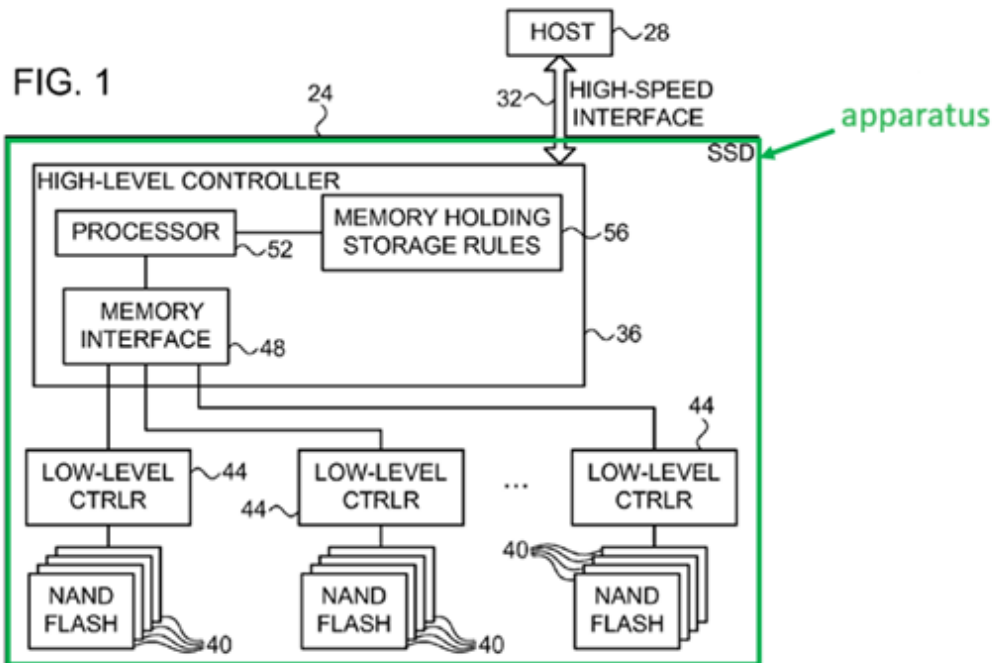
EX1010, Fig. 1 (annotated); EX1011, Fig. 7 (annotated)

Third, the modification would be a simple change of programming. Indeed, Meir teaches that “a given rule in the policy is configurable.” EX1010, [0011]. Further, Salessi teaches that compression, decompression, encryption, and decryption are implemented through “processing algorithm[s].” EX1011, [0007]-[0011]. Updating the policy of Meir to include the processing algorithms of Salessi would have been well within the skill set of a POSITA at the relevant time. EX1003, ¶91.

C. Independent Claim 1:

1. 1[pre]: “An apparatus comprising”

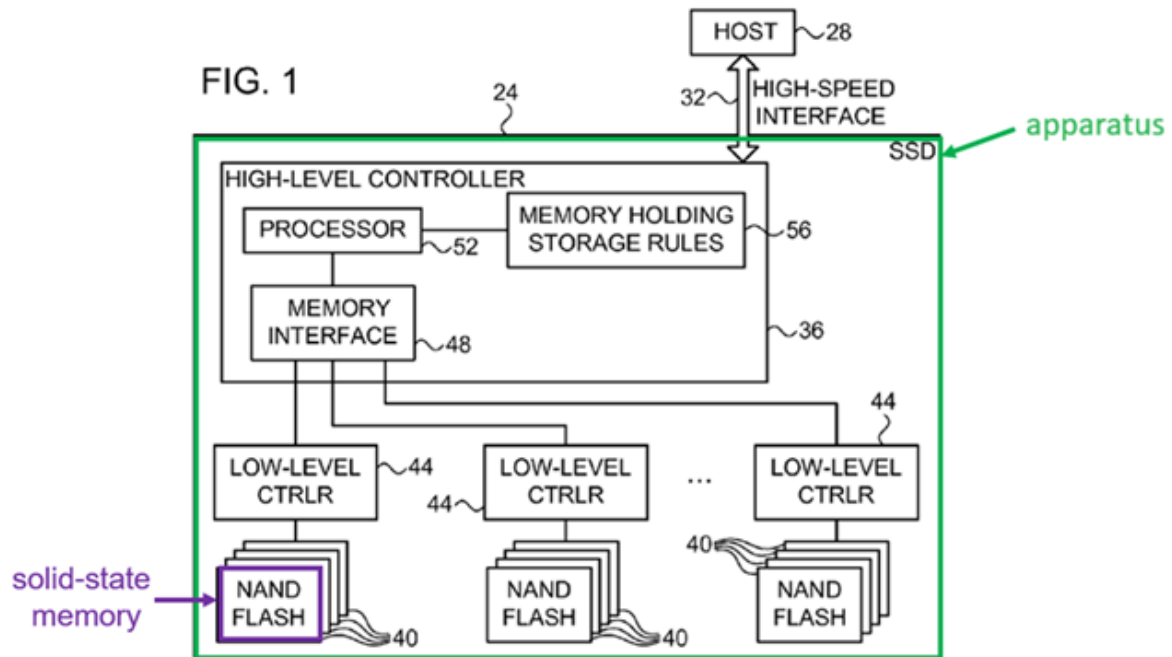
To the extent limiting, Meir discloses the preamble. EX1003, ¶92. Meir discloses a solid-state drive (“SSD”) 24 (*apparatus*). EX1010, FIG. 1, [0029].



EX1010, Fig. 1 (annotated)

2. 1[a]: “a solid-state memory;”

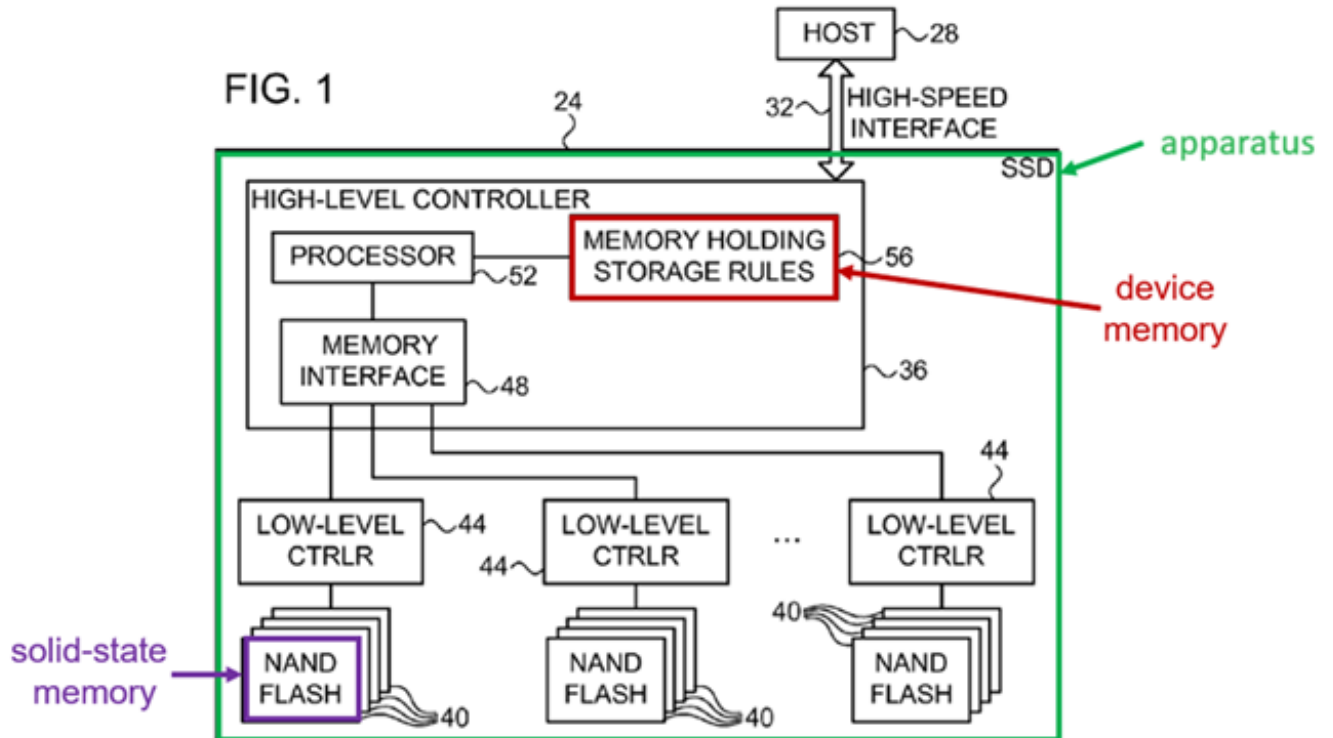
Meir discloses this limitation. EX1003, ¶93. Meir’s SSD 24 comprises memory units 40 (*solid-state memory*). EX1010, FIG. 1, [0030]. “[M]emory units 40 comprise NAND Flash devices or dies” or “any other suitable type of non-volatile memory units.” *Id.* NAND Flash and other non-volatile memories are types of solid-state memories. EX1003, ¶93.



EX1010, Fig. 1 (annotated)

3. 1[b]: “a device memory;”

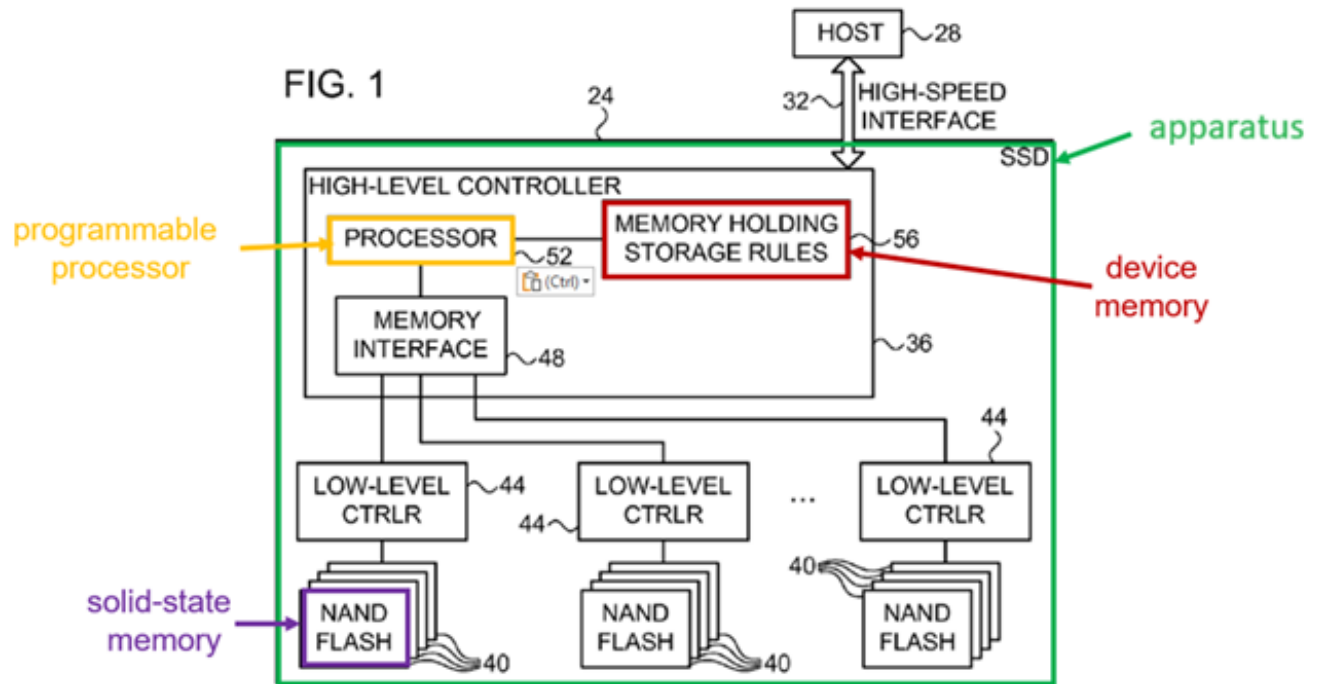
Meir discloses this limitation. EX1003, ¶94. Meir discloses memory 56 (*device memory*). EX1010, FIG. 1, [0033] (“memory 56 holds a definition of a policy that the memory controller applies in storing data in memory units 40”).



EX1010, Fig. 1 (annotated)

4. 1[c]: “a programmable processor operatively coupled to the device memory;”

Meir discloses this limitation. EX1003, ¶95. Meir discloses processor 52 (*programmable processor*). EX1010, FIG. 1, [0033] (“a processor 52 that carries out the various functions of the high-level controller”). Processor 52 (*programmable processor*) is *operatively coupled to* memory 56 (*device memory*) as shown by the connection between these two components in Figure 1. *Id.*; EX1003, ¶95.

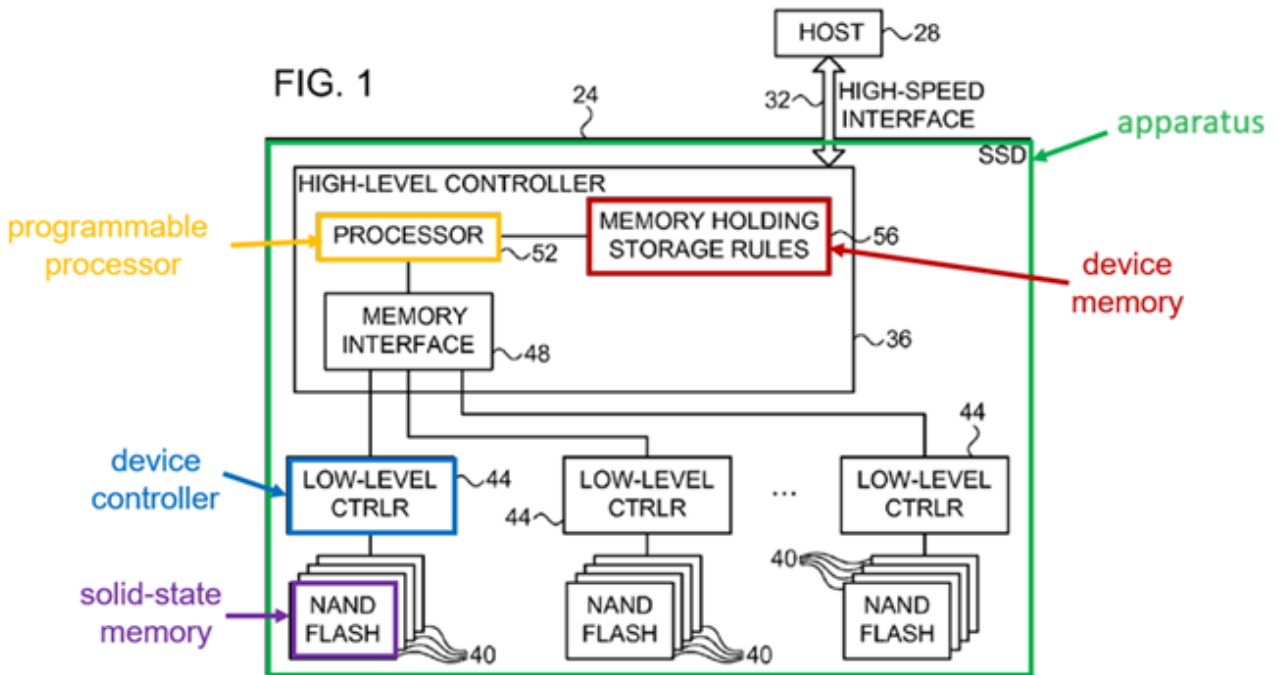


EX1010, Fig. 1 (annotated)

5. 1[d]: “a device controller operatively coupled with the solid-state memory and the programmable processor; and”

Meir discloses this limitation. EX1003, ¶¶96-97. Meir discloses a low-level controller 44 (*device controller*). *Id.*, FIG. 1, [0031]. Low-level controller 44 (*device controller*) is *operatively coupled with* memory unit 40 (*solid-state memory*) as shown by the connection between these two components in Figure 1. *Id.*; EX1003, ¶96. Low-level controller 44 (*device controller*) is also *operatively coupled to* processor 52 (*programmable processor*) through memory interface 48 which allows processor 52 to communicate with memory units 40 via the low-level controller 44. *Id.*; EX1003, ¶97; *see also* EX1010, [0033] (“High-level

controller 36 comprises a memory interface 48 for communicating with memory units 40 (in the present example via low-level controllers 44), and a processor 52 that carries out the various functions of the high-level controller.”).



EX1010, Fig. 1 (annotated)

6. 1[e]: “an application stored on the device memory and comprising instructions that, when executed by the programmable processor, direct the programmable processor to at least:”

Meir in view of Salessi renders obvious this limitation. EX1003, ¶¶98-101. Meir discloses “the memory controller may...run suitable software” (*an application...when executed by the programmable processor, direct the programmable processor*). EX1010, [0034]; see also [0034] (“programmed in software to carry out the functions described”), [0032] (“the high-level controller,

the low-level controllers and the processing circuitry in the memory units are referred to collectively as a memory controller”). Meir further discloses that “[t]he software may be downloaded to the processors in electronic form, over a network, for example, or it may, alternatively or additionally, be provided and/or stored on non-transitory tangible media, such as magnetic, optical, or electronic memory,” confirming that it can be stored in the memory 56 (*device memory*) for processor 52 to execute. *Id.*, [0034]; EX1003, ¶99. Software comprises program instructions (*comprising instructions*) that perform processes when executed. EX1003, ¶100.

As discussed further in 1[e.ii], a POSITA would have been motivated to modify the software (*application*) to direct the processor 52 to perform compression/decompression and encryption/decryption in accordance with algorithms and rules defined by the policy. EX1010, [0027] (“The host may...modify the memory controller’s policy and thus improve performance.”); EX1011, [0057] (“these embodiments can be used to make RAID controllers and subsystems more efficient”); *see* Section VIII.C.8; EX1003, ¶101.

7. 1[e.i]: “in response to receiving a storage request comprising content, retrieve a storage device policy from the device memory;”

Meir discloses this limitation. EX1003, ¶¶102-104. Meir discloses that the software (*application*) directs the processor 52 *in response to receiving a write command including the data for storage (storage request comprising content)*, to

retrieve the policy (*a storage device policy*) from memory 56 (*device memory*). EX1010, [0004], [0025], [0030]; EX1003, ¶103.

Meir discloses “memory access commands (e.g., read and write commands)” (*storage request*). EX1010, [0030]. Meir discloses “[h]ost 28 typically sends memory access commands (e.g., read and write commands) to SSD 24” (*receiving a storage request*). *Id.*, [0030]; *see also id.*, [0004] (“accept[ing] memory access commands from a host”). Specifically, Meir discloses “receiving the memory access commands in the memory controller and executing the received memory access commands in the memory units.” *Id.*, [0054], Fig. 2; EX1003, ¶103.

The write command includes data and a logical address identifying the data to be written (*storage request comprising content*). *Id.*, [0040] (“the host sends each memory access command along with a logical address to which the command is to be applied”). The processor 52 retrieves the policy from memory 56, so that it “translates the logical addresses to respective physical storage locations” “[a]ccording to the policy.” *Id.*, [0040], [0033] (“memory 56 holds a definition of a policy that the memory controller applies in storing data in memory units 40”), [0048] (“the policy defines a redundant storage scheme (e.g., a RAID-like scheme) that the memory controller applies among the memory units while store the data”); EX1003, ¶103. Because the “memory controller executes the memory access commands...in accordance with a predefined policy,” it must necessarily retrieve

the policy from the memory 56 to apply it to the memory access command. *Id.*, [0036]; EX1003, ¶103.

As discussed above, the memory controller includes the high-level controller. EX1010, [0032]; *see also* Section VIII.C.6. Meir discloses that “processor 52” (*programmable processor*) “carries out the various functions of the high-level controller” that “stores data” for the SSD 24. *Id.*, [0032], [0033]. As shown in Figure 1, Meir discloses the processor 52 (*programmable processor*) is connected to the memory 56 (*device memory*) in which the policy (*storage device policy*) is stored. *Id.*, FIG. 1. The software (*application*) that directs processor 52 (*programmable processor*) is the component in the memory controller that, *in response to receiving a storage request comprising content, retrieves a storage device policy from the device memory*. EX1003, ¶104.

8. 1[e.ii]: “process the content for storage based on the storage device policy; and”

Meir in view of Salessi renders obvious this limitation. EX1003, ¶¶105-114. Meir discloses that the software (*application*) directs the processor 52 to *process* the data for storage (*content for storage*) according to the policy (*based on the storage device policy*), such as by applying a redundancy scheme. *Id.*

Meir teaches that “SSD 24 comprises a high-level controller 36, which stores data in one or more non-volatile memory units 40.” EX1010, [0030]. This data is *content for storage*. EX1003, ¶106. Meir explains that “[h]ost 28 typically sends

memory access commands (e.g., read and write commands) to SSD 24 over interface 32” and “[t]he memory system comprises a memory controller, which receives from the host memory access commands (e.g., read and write commands) and executes the commands in the memory units.” EX1010, [0030], [0020].

Meir discloses that the memory controller will *process* commands *based on a storage device policy* because “[t]he memory controller typically executes the memory access commands received from the host in accordance with a certain policy.” EX1010, [0021], [0033]; EX1003, ¶107. “The policy comprises a set of rules, for example parallelization rules, pipeline rules, prioritization rules, redundancy rules, power consumption rules and/or memory unit characteristics rules.” *Id.*, [0037].

When applying the redundancy rules from the policy, the software (*application*) can direct the processor 52 to *process* the data (*content for storage*) by making a copy of the data to store a redundant copy in other memory units, striping the data dividing it into blocks, or calculating parity information on the data. *Id.*, [0025] (“[t]he memory controller policy involves storing the data while applying a redundant storage scheme such as Redundant Array of Inexpensive Disks (RAID) among the memory units”); EX1003, ¶107.

To the extent that Meir does not disclose that the software (*instructions*) executed directs the processor 52 (*programmable processor*) to process the data (*content for storage*) included with the commands *based on a storage policy*, this is rendered obvious by the system resulting from the combination of the teachings of Meir and Salessi. EX1003, ¶108.

Like Meir's SSD (which includes memory units 40 and a memory controller), Salessi's SSD "includes flash memory and an SSD processing unit." EX1011, FIG. 7, [0006]; *see also* EX1010, FIG. 1. Salessi's processing unit can *process content for storage* because it is "capable of processing the data...being stored or retrieved from the flash memory." EX1011, [0006]. Salessi's data includes *content*, such as social media posts and pictures and video content, among other types of content. EX1011, [0002]. "Processing capabilities incorporated into the SSD may include encryption and decryptions [and] compression and decompression." *Id.* Salessi further teaches that the processing unit "process[es], using a processing algorithm, to generate processed data." *Id.*, [0023]; EX1003, ¶¶109-111.

In the combination, Meir's policy stored in memory 56 includes Salessi's compression, decompression, decryption, and encryption algorithms and instructions. Specifically, Meir teaches that the "one or more of the rules in the memory controller policy may be configurable" and "the host may issue to the memory controller a command that configures or modifies the memory controller,

so as to improve performance.” EX1010, [0055]. A POSITA would therefore modify the memory controller policy of Meir to incorporate the processing algorithms and instructions of Salessi, so that Meir’s policy would define to which data to apply Salessi’s processing algorithms and where the data would be transferred and stored. EX1011, [0006]; EX1003, ¶¶112-113.

As discussed, a POSITA would have been motivated to modify the software (*application*) and *policy* stored in memory 56 (*device memory*) of Meir to direct the processor 52 (*programmable processor*) to compress and encrypt the data to be stored according to algorithms and rules in the policy because it would optimize the performance and improve the security of the system. *See* Section VIII.A; EX1010, [0036]; EX1011, [0050]; EX1003, ¶113. Further, as discussed, a POSITA would have had a reasonable expectation of success since the SSDs of Meir and Salessi have similar structures and components, and Salessi expressly teaches that the use of its processing algorithms in such similar systems. *See* Section VIII.B; EX1010, FIG. 1, [0033]; EX1011, FIG. 7, [0004]; EX1003, ¶114.

**9. 1[e.iii]: “transfer the content to the device controller;
and”**

Meir discloses this limitation. EX1003, ¶¶115-120. In Meir, processor 52’s software (*application*) sends the data (*transfer the content*) to the low-level controller 44 (*device controller*) to store. *Id.* In certain embodiments, Meir teaches that the storage device policy defines parallelism rules. EX1010, [0037].

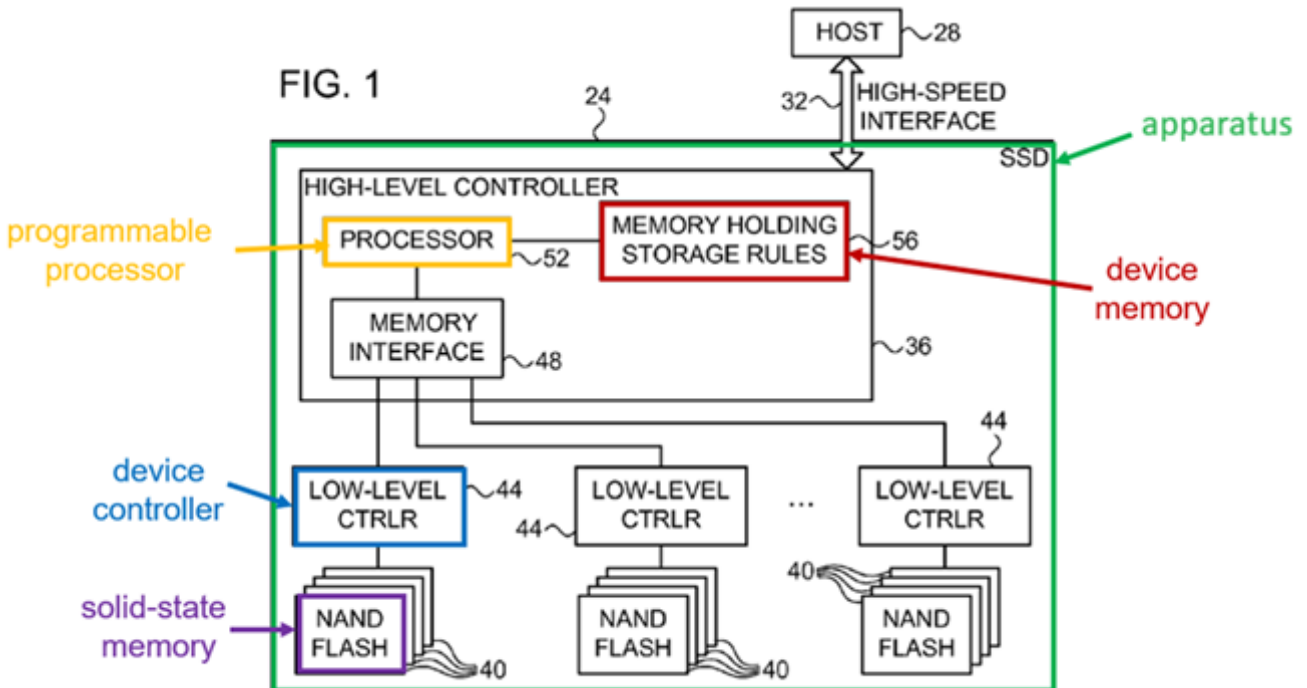
“Parallelism rules define how the memory controller distributes the memory access commands among the memory units.” *Id.*

When a write command is received, the processor 52 will process the command according to the policy and transfer the data to the assigned low-level controller 44. *Id.*, [0005], [0041]. Specifically, the parallelism rules defined by the policy will “specify distribution of the memory access commands among the memory units.” *Id.*, [0005]. “[A] mapping, defined in the memory controller, between logical addresses associated with the memory access commands and respective physical storage location in the memory units” will be used by processor 52 via its software to direct the access command to the appropriate low-level controller 44 (the low-level controller assigned to those memory addresses). *Id.*, [0007], [0031]; *see also* [0009], [0023], [0031] (“logical-to-physical address translation is performed by the high-level controller”); EX1003, ¶¶116-118.

Because the data to be stored is transferred from the host to high-level controller 56, the software (*application*) of processor 52 necessarily send the data (*transfers the content*) to the low-level controller 44 (*device controller*). *Id.*, FIG. 1, [0033]. As Meir explains, “[h]igh-level controller 36 comprises a memory interface 48 for communicating with memory units 40 (in the present example *via low-level controllers 44*).” *Id.*, [0033] (emphasis added); EX1003, ¶¶119-120.

10. 1[f]: “the device controller configured to:”

Meir discloses this limitation. EX1003, ¶121. As explained for 1[d], the solid-state drive 24 includes low-level controller 44. *See* Section VIII.C.5; EX1010, FIG. 1; EX1003, ¶121.



EX1010, Fig. 1 (annotated)

11. 1[f.i]: “receive the content from the programmable processor and store the content on the solid-state memory.”

Meir discloses this limitation. EX1003, ¶¶122-125. As explained for 1[e.iii], the software (*application*) of processor 52 (*programmable processor*) necessarily sends the data to the assigned low-level controller 44 (*device controller*). *See* Section VIII.C.9; EX1010, FIG. 1; EX1003, ¶123. In doing so, the low-level

controller 44 (*device controller*) necessarily receives the data for storage (*receive the content*) from processor 52 (*programmable processor*). EX1010, FIG. 1; EX1003, ¶123.

Meir explains that the “memory controller...executes the commands in the memory units.” EX1010, [0020]; EX1003, ¶123. In the embodiment where the memory controller comprises high-level controller 36 and low-level controller 44 (*device controller*), the high-level controller 36 communicates with memory units 40 (*solid-state memory*) via low-level controller 44 (*device controller*). *Id.*, [0033]. Accordingly, when the memory controller executes a write command, the low-level controller 44 (*device controller*) writes the data (*stores the content*) to the memory unit 40 (*on the solid-state memory*) according to the logical-to-physical address mapping defined by the parallelism rule that is part of the policy. *Id.*, [0040] (“According to the policy, the memory controller translates the logical addresses to respective physical storage locations in memory units 40, and executes the commands in the memory units according to the logical-to-physical address mapping.”).

A POSITA would have been motivated to use the implementation of Meir from Figure 1, because Meir explains that advantages of partitioning the execution of a command between the high-level controller 36 (as executed by processor 52 or

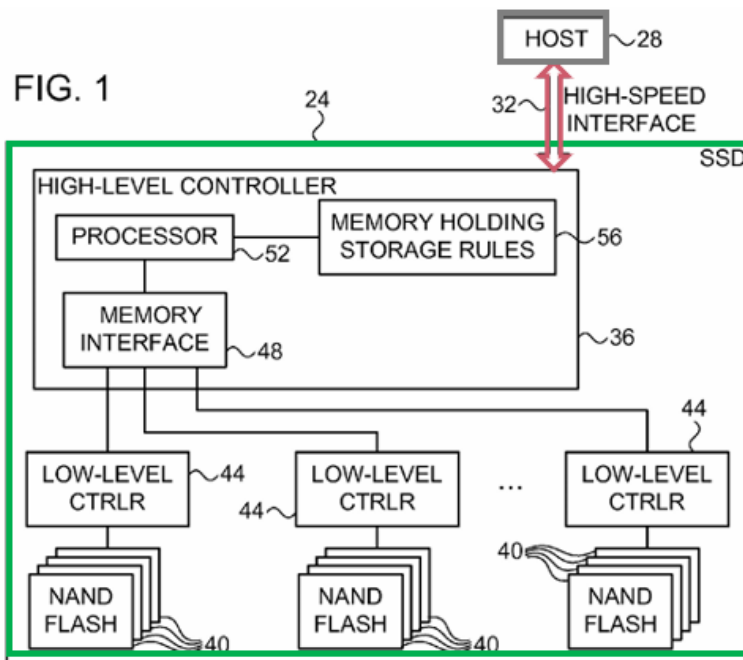
programmable processor) and low-level controller 44. EX1010, [0037], [0042]; EX1003, ¶¶124-125.

D. Dependent Claim 2, 5-7:

1. Claim 2

Meir discloses this limitation. EX1003, ¶¶126-128. As discussed, Meir discloses SSD 24 (*apparatus*) as recited in claim 1. *See* Section VIII.C.1.

Meir discloses a *high-speed interface* 32 (*interface connector*) that transitively connects (*communicatively couples*) SSD 24 (*apparatus*) to host 28 (*host computer*) as shown by the connection between these two components in Figure 1; EX1010, FIG. 1; *see also id.*, [0029] (“Host 28 and SSD 24 communicate over a high-speed interface 32, for example a SATA, SAS or NVM express interface.”), EX1003, ¶128. Host 28 sends memory access commands “to SSD 24 over interface 32,” and the SSD “executes the commands in memory units 40” (*solid-state memory*). EX1010, [0029]-[0030]; EX1003, ¶128. Execution is “partitioned among high-level controller 36, low-level controllers 44,” (*device controller*), the commands being received and executed by processor 52 (*programmable processor*). *Id.*, [0014], [0031]. And the policy held in memory 56 (*device memory*) is communicated to the host “over interface 32.” *Id.*, [0051]. Meir explains that “host 28 may comprise...a host processor in computing device such as a notebook or laptop computer” (*host computer*). *Id.*, [0029]; EX1003, ¶128.



EX1010, FIG. 1 (annotated)

2. Claim 5

a. 5[pre]

As discussed, Meir discloses SSD 24 (*apparatus*) as recited in claim 1. *See* Section VIII.C.1. Meir in view of Salessi renders obvious this limitation. EX1003, ¶¶129-130. As discussed in 1[e], Meir discloses software comprising *instructions stored on* memory 56 (*device memory*), *that when executed by* processor 52 (*programmable processor*), *direct the programmable processor to* execute the access commands according to a policy stored on the memory 56. *See* Section VIII.C.6; EX1010, FIG. 1, [0034]; EX1003, ¶130.

b. 5[a]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶¶131-134. As discussed, Meir discloses, and Meir in view of Salessi renders obvious, that the memory controller will process commands *based on a storage device policy*. See Section VIII.C.8. Although Meir does not disclose that the software executed by processor 52 (*instructions*) *compresses* the data (*requested content*) included with the commands *based on a storage policy*, this is rendered obvious by the system resulting from the combination of the teachings of Meir and Salessi. EX1003, ¶¶131-134.

Salessi's processing unit can *compress content for storage* because “[p]rocessing capabilities incorporated into the SSD may include encryption and decryptions [and] compression and decompression.” EX1011, [0006]; see Section VIII.C.8. Salessi further teaches that the processing unit “us[es] a processing algorithm[] to generate processed data.” EX1011, [0023]; EX1003, ¶132.

In the combination, Meir's policy stored in memory 56 includes Salessi's compression. Specifically, Meir teaches that the “one or more of the rules in the memory controller policy may be configurable” and “the host may issue to the memory controller a command that configures or modifies the memory controller, so as to improve performance.” EX1010, [0055]. A POSITA would therefore modify the memory controller policy of Meir to incorporate the compression

algorithms and instructions of Salessi, wherein Meir's policy would define which data to apply Salessi's compression algorithms to. EX1011, [0006]; EX1003, ¶¶133.

As discussed, a POSITA would have been motivated to modify the software (*application*) and policy store in memory 56 (*policy*) of Meir to direct the processor 52 to compress the data to be stored according to algorithms and rules in the policy because it would optimize the performance and improve the security of the system. *See* Section VIII.A; EX1010, [0036]; EX1011, [0050]; EX1003, ¶134. Further, as discussed, a POSITA would have had a reasonable expectation of success since the SSDs of Meir and Salessi have similar structures and components, and Salessi expressly teaches that the use of its processing algorithms in such similar systems. *See* Section VIII.B; EX1010, FIG. 1, [0033]; EX1011, FIG. 7, [0004]; EX1003, ¶¶85-91, 134.

c. 5[b]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶135. Meir discloses *transferring the content to the device controller*. *See* Section VIII.C.9. Salessi discloses that the *content is compressed*. *See* Section VIII.D.2.b. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.2.c; EX1003, ¶¶73-91, 135.

d. 5[c]

As discussed for 1[d], Meir discloses low-level controller 44 (*device*

controller) “that executes the memory access commands issued by host 28.” *See* Section VIII.C.5; EX1003, ¶136.

e. 5[d]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶137. Meir discloses *receiving the content from the programmable processor and storing the content on the solid-state memory*. *See* Section VIII.C.11. Salessi discloses that the *content is compressed*. *See* Section VIII.D.2.b. A POSITA would have been motivated to combine Meir with Salessi for the reasons discussed above. *See* Sections VIII.A-B, VIII.D.2.b; EX1003, ¶¶73-91, 137.

3. Claim 6

a. 6[pre]

As discussed, Meir discloses SSD 24 (*apparatus*) as recited in claim 1. *See* Section VIII.C.1. Meir in view of Salessi renders obvious this limitation. EX1003, ¶¶138-139. As discussed in 1[e], Meir discloses software comprising *instructions stored on memory 56 (device memory), that when executed by processor 52 (programmable processor), direct the programmable processor to execute the access commands according to a policy stored on the memory 56*. *See* Section VIII.C.6; EX1010, FIG. 1, [0034]; EX1003, ¶¶98-101, 139.

b. 6[a]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶¶140-143. As discussed, Meir discloses, and Meir in view of Salessi renders obvious, that the memory controller will process commands *based on a storage device policy*. See Section VIII.C.8. Although Meir does not disclose that the software executed by processor 52 (*instructions*) *encrypt* the data (*requested content*) included with the commands *based on a storage policy*, this is rendered obvious by the system resulting from the combination of the teachings of Meir and Salessi. EX1003, ¶140.

Salessi's processing unit can *encrypt content for storage* because "[p]rocessing capabilities incorporated into the SSD may include encryption and decryptions [and] compression and decompression." EX1011, [0006], [0023] ("Salessi further teaches that the processing unit "us[es] a processing algorithm[] to generate processed data."); see Section VIII.C.8; EX1003, ¶141.

In the combination, the Meir's policy stored in memory 56 includes Salessi's encryption. Specifically, Meir teaches that the "one or more of the rules in the memory controller policy may be configurable" and "the host may issue to the memory controller a command that configures or modifies the memory controller, so as to improve performance." EX1010, [0055]. A POSITA would therefore modify the memory controller policy of Meir to incorporate the encryption

algorithms and instructions of Salessi, wherein Meir's policy would define which data to apply Salessi's encryption algorithms to. EX1011, [0006]; EX1003, ¶142.

As discussed, a POSITA would have been motivated to modify the software (*application*) and policy store in memory 56 (*policy*) of Meir to direct the processor 52 to encrypt the data to be stored according to algorithms and rules in the policy because it would optimize the performance and improve the security of the system. *See* Section VIII.A; EX1010, [0036]; EX1011, [0050]; EX1003, ¶¶72-84, 143. Further, as discussed, a POSITA would have had a reasonable expectation of success since the SSDs of Meir and Salessi have similar structures and components, and Salessi expressly teaches that the use of its processing algorithms in such similar systems. *See* Section VIII.B; EX1010, FIG. 1, [0033]; EX1011, FIG. 7, [0004]; EX1003, ¶¶85-91, 143.

c. 6[b]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶144. Meir discloses *transferring the content to the device controller*. *See* Section VIII.C.9. Salessi discloses that the *content is encrypted*. *See* Section VIII.D.3.b. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.3.b; EX1003, ¶¶72-91, 144.

d. 6[c]

As discussed for 1[d], Meir discloses low-level controller 44 (*device*

controller) “that executes the memory access commands issued by host 28.” See Section VIII.C.5; EX1003, ¶145.

e. 6[d]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶146. Meir discloses *receiving the content from the programmable processor and storing the content on the solid-state memory*. See Section VIII.C.11. Salessi discloses that the *content is encrypted*. See Section VIII.D.3.b. A POSITA would have been motivated to combine Meir with Salessi. See Sections VIII.A-B, VIII.D.3.b; EX1003, ¶¶72-84, 146.

4. Claim 7

Meir in view of Salessi renders obvious this limitation. EX1003, ¶¶147-150.

Salessi discloses that the data to be stored in the flash memory (*content for storage*) is *medical records, video data, image data, on-line temporal video data, financial data, or online transaction data*. Specifically, Salessi teaches a data storage system for “data [that] comes from everywhere: posts to social media sites, digital pictures and video, purchase transaction records, bank transactions, sensors used to gather data and intelligence, like climate information, cell phone GPS signal, and many others.” EX1011, [0002]. “This vast amount of data eventually is stored and maintained in storage nodes, such like... solid-state storage drives (SSD), and the like.”). *Id.*

Salessi further discloses that the data to be stored (*content for storage*) is *cached data*. EX1011, [0006], [0023]. A POSITA would have understood that the data being stored or retrieved is *cached data* in embodiments where the data is being stored in cache devices. EX1003, ¶¶150. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B; EX1003, ¶¶72-84, 150.

E. Independent Claims 16 and 26:

1. 16[pre]/26[pre]: “An apparatus comprising”

To the extent limiting, Meir discloses the preamble. *See* Section VIII.C.1; EX1003, ¶151.

2. 16[a]/26[a]: “a solid-state memory[;]”

Meir discloses this limitation. *See* Section VIII.C.2; EX1003, ¶152.

3. 16[b]/26[b]: “a device memory;”

Meir discloses this limitation. *See* Section VIII.C.3; EX1003, ¶153.

4. 16[c]/26[c]: “a programmable processor operatively coupled to the device memory;”

Meir discloses this limitation. *See* Section VIII.C.4; EX1003, ¶154.

5. 16[d]/26[d]: “a device controller operatively coupled with the solid-state memory and the programmable processor; and”

Meir discloses this limitation. *See* Section VIII.C.5; EX1003, ¶155.

6. **16[e]/26[e]: “an application stored on the device memory and comprising instructions that, when executed by the programmable processor, direct the programmable processor to at least:”**

Meir discloses this limitation. *See* Section VIII.C.6; EX1003, ¶156.

7. **26[e.i]: “in response to receiving a storage request comprising content, retrieve a storage device policy from the device memory;”**

Meir discloses this limitation. EX1003, ¶¶157-159. Meir discloses “memory access command (e.g., read and write commands)” (*storage request*). EX1010, [0030]. Meir discloses “[h]ost 28 typically sends memory access commands (e.g., read and write commands) to SSD 24” (*receiving a storage request comprising content*). *Id.*, [0030]; *see also id.*, [0004] (“accept[ing] memory access commands from a host”).

Meir discloses the “SSD execut[ing] the commands” *in response to* “[h]ost 28...send[ing] memory access commands (e.g., read and write commands) to SSD 24” (*receiving a storage request comprising content*). *Id.*, [0030]; *see also id.*, [0054], FIG. 2. Meir discloses that “the memory controller executes the memory access commands received from host 28 in accordance with a predefined policy” (*storage device policy*). *Id.*, [0036]; *see also id.*, [0021]. Meir discloses that “memory 56” (*device memory*) holds a definition of a policy” (*storage device policy*) “that the memory controller applies in storing data in memory units 40.” *Id.*, [0033], FIG. 1; *see also id.*, [0004]. A POSITA would have understood that because the

“memory controller executes the memory access commands...in accordance with a predefined policy,” it must necessarily retrieve the policy from the memory 56 to apply it to the memory access command. EX1003, ¶158.

As discussed above, the memory controller includes the high-level controller. EX1010, [0032]; *see also* Section VIII.C.6. Meir discloses that “processor 52” (*programmable processor*) “carries out the various functions of the high-level controller” that “stores data” for the SSD 24. *Id.*, [0032], [0033]. As shown in Figure 1, Meir discloses the processor 52 (*programmable processor*) is connected to the memory 56 (*device memory*) in which the policy (*storage device policy*) is stored. *Id.*, FIG. 1. A POSITA would have recognized that Meir discloses processor 52 (*programmable processor*) is the component in the memory controller that, *in response to receiving a storage request comprising content, retrieves a storage device policy from the device memory*. EX1003, ¶159.

8. 26[e.ii]: “process the content for storage based on the storage device policy; and”

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.C.8; EX1003, ¶¶160-161.

A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.C.8; EX1003, ¶¶72-84, 161.

**9. 26[e.iii]: “transfer the content to the device controller;
and”**

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.C.9; EX1003, ¶162.

**10. 16[e.i]: “in response to receiving a content request to
retrieve content, retrieve a storage device policy from
the device memory;”**

Meir discloses this limitation. EX1003, ¶¶163-165. Meir discloses that the software (*application*) directs the processor 52 *in response to receiving a read command* including the data for storage (*content*), to *retrieve* the policy (*a storage device policy*) from memory 56 (*device memory*). EX1010, [0004], [0025], [0030]; EX1003, ¶163.

Meir discloses “memory access command (e.g., read and write commands)” (*content request*). EX1010, [0030]. Meir discloses “[h]ost 28 typically sends memory access commands (e.g., read and write commands) to SSD 24” (*receiving a content request to retrieve content*). *Id.*, [0030]; *see also id.*, [0004] (“accept[ing] memory access commands from a host”); EX1003, ¶163.

Meir discloses the “SSD execut[ing] the commands” *in response to* “[h]ost 28...send[ing] memory access commands (e.g., read and write commands) to SSD 24” (*receiving a content request to retrieve content*). *Id.*, [0030]; *see also id.*, [0054], FIG. 2. Meir explains that the memory controller executes the memory access commands in accordance with policy and that the memory 56 (*device memory*)

stores the policy. *Id.*, [0033], [0036], FIG. 1; *see also* Section VIII.C.7. A POSITA would have understood that because the “memory controller executes the memory access commands...in accordance with a predefined policy,” it must necessarily *retrieve the policy* from the memory 56 to apply it to the memory access command. EX1010, [0036]; EX1003, ¶164. For example, Meir teaches that “the policy defines a redundant storage scheme (e.g., a RAID-like scheme),” and if the data is striped (divided into blocks), the redundant storage scheme would need to be retrieved to rebuild the requested data. EX1010., [0048]; EX1003, ¶164.

Meir discloses that processor 52 (*programmable processor*) carries out functions for the high-level controller and that the processor 52 (*programmable processor*) is connected to the memory 56 (*device memory*). *Id.*, [0030], [0033], FIG. 1; *see also* Section VIII.C.7. The software (*application*) that directs processor 52 (*programmable processor*) is the component in the memory controller that, *in response to receiving a content request to retrieve content, retrieves a storage device policy from the device memory*. EX1003, ¶165.

11. 16[e.ii]/26[e.iv]: “[subsequent to storing the content on the solid-state memory and in response to receiving a content request,] direct the device controller to read the requested content from the solid-state memory;”

Meir discloses this limitation. EX1003, ¶¶166-169.

Meir explains that the “memory controller...executes the commands in the memory units.” EX1010, [0020]. In the embodiment where the memory controller comprises high-level controller 36 and low-level controller 44 (*device controller*), the high-level controller 36 communicates with memory units 40 (*solid-state memory*) via low-level controller 44 (*device controller*). *Id.*, [0033]. Accordingly, when the memory controller executes a read command received by the host (*in response to receiving a content request*), the high-level controller 36 “translates the logical addresses to respective physical storage locations in memory units 40, and executes the commands in the memory units according to the logical-to-physical address mapping.” *Id.* [0040]. In one embodiment, “a certain subset of bits in the logical address may indicate the...low-level controller in which this address is assigned” and after translation, the high-level controller 36 will direct that assigned low-level controller 44 (*device controller*), to execute the access command, here the read command (*read requested content from the solid-state memory*). *Id.*, [0041], [0044]; EX1003, ¶166.

As Meir further explains, in certain embodiments, the SSD 24 may use error correction code (“ECC”) to encode the data (*content*) to prevent errors. *Id.*, [0045]. When a read command is received, the low-level controller 44 will use the processing circuitry in the memory units 40 to fetch the ECC-encoded data (*read*

requested content from the solid-state memory). *Id.* The low-level controller 44 will then decode the data. *Id.*; EX1003, ¶167.

In order to subsequently read the requested content from the solid-state memory, a POSITA would have recognized it is inherent that the content was previously stored in the solid-state memory. EX1003, ¶168. Thus, a POSITA would have understood that Meir teaches *directing the device controller to read the requested content from the solid-state memory is subsequent to storing the content on the solid-state memory*. *Id.*

Thus, a POSITA would have recognized that Meir discloses processor 52 (*programmable processor*) *subsequent to storing the content on the solid-state memory and in response to receiving a storage request comprising content, direct the device controller to read the requested content from the solid-state memory*. EX1003, ¶169.

12. 16[e.iii]/26[e.v]: “receive the requested content from the device controller [and]/[;]”

Meir discloses this limitation. EX1003, ¶¶170-171. Meir discloses that the software comprising *instructions further directs processor 52 (programmable processor) to receive the decoded data (requested content) from low-level controller 44 (device controller)*. EX1010, [0044] (“the policy defines that the memory controller executes the memory access commands in a pipelined manner...[where] the different pipeline stages may be executed by different controllers in the memory

controller.”), [0045] (“For example, a read command typically involves fetching ECC-encoded data from memory units 40, decoding the ECC and sending the decoded data to the host”). Meir explains that when a “read command is broken into three pipeline stages,” “decoding the ECC” can be performed by the low-level controller 44, which then sends the decoded data to the processor 52 (*programmable processor*) of the high-level controller 36. *Id.*, [0045]; EX1003, ¶171. The step of “sending the data to the host” can then be performed by processor 52 (*programmable processor*) as directed by the software comprising *instructions*. *Id.*

13. 16[e.iv]/26[e.vi]: “process the requested content for transfer based on the storage device policy; and”

Meir in view of Salessi renders obvious this limitation. EX1003, ¶¶172-178. Meir discloses that the memory controller will *process* commands *based on a storage device policy* because “[t]he memory controller typically executes the memory access commands received from the host in accordance with a certain policy.” EX1010, [0021], [0033]; EX1003, ¶173. “The policy comprises a set of rules, for example parallelization rules, pipeline rules, prioritization rules, redundancy rules, power consumption rules and/or memory unit characteristics rules.” *Id.*, [0037]; *see also id.*, [0025] (“[t]he memory controller policy involves storing the data while applying a redundant storage scheme such as Redundant Array of Inexpensive Disks (RAID) among the memory units”). In addition, a POSITA would have understood that a RAID implementation would have involved

processing when reading data, such as recomputing data from redundancy information. EX1003, ¶173.

The software (*application*) can direct the processor 52 to *process* the received data (*requested content for transfer*) based on the redundant storage scheme. *Id.*, [0025]. For example, when the data has been striped, the processor 52 splits the read request and pulls different parts of the requested data from multiple drives. *Id.*, [0038], [0045]; EX1003, ¶174. Processor 52 (*programmable processor*) will reassemble the different parts to transfer to the host. EX1003, ¶174. Similarly, when a drive failure has been identified, processor 52 will use the parity data to rebuild the requested data. EX1003, ¶174.

To the extent that Meir does not disclose that the software executed by processor 52 (*instructions*) *process* the data (*requested content*) included with the commands *based on a storage device policy*, this is rendered obvious by the system resulting from the combination of the teachings of Meir and Salessi. EX1003, ¶175.

Like Meir's SSD (which includes memory units 40 and a memory controller), Salessi teaches an SSD that "includes flash memory and an SSD processing unit." EX1011, FIG. 7, [0006]; *see also* EX1010, FIG. 1. Salessi's processing unit can *process requested content* because it is "capable of processing the data...being stored or retrieved from the flash memory." EX1011, [0006]. "Processing capabilities incorporated into the SSD may include encryption and decryptions [and]

compression and decompression.” *Id.* Salessi further teaches that the processing unit “process[es], using a processing algorithm, data received from the flash memory to form processed data.” *Id.*, [0007]; *see also id.*, [0016].

In the combination, the policy stored in memory 56 as taught by Meir includes compression, decompression, decryption, and encryption algorithms and instructions as taught by Salessi. Specifically, Meir teaches that the “one or more of the rules in the memory controller policy may be configurable” and “the host may issue to the memory controller a command that configures or modifies the memory controller, so as to improve performance.” EX1010, [0055]. A POSITA would therefore modify the memory controller policy of Meir to incorporate the processing algorithms and instructions of Salessi, wherein Meir’s policy would define to which data to apply Salessi’s processing algorithms. EX1011, [0006]; EX1003, ¶177.

As discussed, a POSITA would have been motivated to modify the software (*application*) and *policy* stored in memory 56 (*device memory*) of Meir to direct the processor 52 (*programmable processor*) to decompress and decrypt the data read from storage according to algorithms and rules in the policy because it would optimize the performance and improve the security of the system. *See* Section VIII.A; EX1010, [0036]; EX1011, [0050]; EX1003, ¶178. Further, as discussed, a POSITA would have had a reasonable expectation of success since the SSDs of Meir and Salessi have similar structures and components, and Salessi expressly teaches

that the use of its processing algorithms in such similar systems. *See* Section VIII.B; EX1010, FIG. 1, [0033]; EX1011, FIG. 7, [0004]; EX1003, ¶178.

14. 16[e.v]/26[e.vii]: “transfer the requested content; and”

Meir discloses this limitation. EX1003, ¶179. Meir discloses “sending the data” (*transfer the requested content*) “to the host (e.g., by the high-level controller).” EX1010, [0045].

15. 16[f]/26[f]: “the device controller configured to:”

Meir discloses this limitation. *See* Section VIII.C.10; EX1003, ¶180.

16. 26[f.i]: “receive the content from the programmable processor and store the content on the solid-state memory.”

Meir discloses this limitation. *See* Section VIII.C.11; EX1003, ¶181.

17. 16[f.i]/26[f.ii]: “read the requested content from the solid-state memory in response to the direction from the programmable processor; and”

Meir discloses this limitation. EX1003, ¶182.

As discussed, Meir discloses *in response to receiving a content request, the programmable processor directing the device controller to read the requested content from the solid-state memory*. *See* Section VIII.E.11. A POSITA would have understood that it necessarily follows that the device controller *reads the requested content from the solid-state memory in response to the direction from the programmable processor*. EX1003, ¶182.

18. 16[f.ii]/26[f.iii]: “transfer the [requested] content to the programmable processor”

Meir discloses this limitation. EX1003, ¶183. Meir discloses that after the low-level controller 44 (*device controller*) decodes the requested data (*requested content*), the low-level controller 44 will send the decoded data to the processor 52 (*programmable processor*) of high-level controller 36. *Id.*, [0045]; EX1003, ¶183.

F. Dependent Claims 17, 19, 20, 27, 30, 31:

1. Claims 17/27

Meir discloses this limitation as discussed for claim 2. *See* Section VIII.D.1; EX1003, ¶184.

2. Claim 19

a. 19[pre]

As discussed, Meir discloses SSD 24 (*apparatus*) as recited in claim 1. *See* Section VIII.C.1; EX1003, ¶¶185-186.

b. 19[a]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶187. As discussed, Meir discloses that requested content is read from, and therefore stored on, the solid-state memory. *See* Section VIII.E.17. Salessi discloses that the *content* is *compressed*. *See* Section VIII.D.2.b. Thus, a POSITA would have recognized that the requested content stored on the solid-state memory is compressed. EX1003,

¶187. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.2.b; EX1003, ¶¶72-84, 187.

c. 19[b]

Meir discloses this limitation. *See* Section VIII.C.10; EX1003, ¶188.

d. 19[b.i]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶189. Meir discloses *reading the content from the solid-state memory in response to the direction from the programmable processor*. *See* Section VIII.E.17. Salessi discloses that the *content is compressed*. *See* Section VIII.D.2.b. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.2.b; EX1003, ¶¶72-84, 189.

e. 19[b.ii]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶190. Meir discloses *transferring the content to the programmable processor*. *See* Section VIII.E.18. Salessi discloses that the *content is compressed*. *See* Section VIII.D.2.b. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.2.b; EX1003, ¶¶72-84, 190.

f. 19[c]

Meir discloses this limitation. *See* Sections VIII.C.10, VIII.E.12-13; EX1003, ¶191.

g. 19[c.i]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶¶192-195. As discussed, Meir discloses, and Meir in view of Salessi renders obvious, that the memory controller will process commands *based on a storage policy*. See Section VIII.C.8. Although Meir does not disclose that the software executed by processor 52 (*instructions*) *decompresses* the data (*compressed content*) included with the commands *based on a storage policy*, this is rendered obvious by the system resulting from the combination of the teachings of Meir and Salessi. EX1003, ¶192.

Salessi's processing unit can *decompress compressed content* because "[p]rocessing capabilities incorporated into the SSD may include encryption and decryptions [and] compression and decompression." EX1011, [0006], [0023]; see Section VIII.C.8.

In the combination, Meir's policy stored in memory 56 includes Salessi's decompression. Specifically, Meir teaches that the "one or more of the rules in the memory controller policy may be configurable" and "the host may issue to the memory controller a command that configures or modifies the memory controller, so as to improve performance." EX1010, [0045]. A POSITA would therefore modify the Meir's policy to incorporate the decompression algorithms and instructions of Salessi, wherein Meir's policy would define to which data to apply Salessi's decompression algorithms. EX1011, [0006]; EX1003, ¶194.

As discussed, a POSITA would have been motivated to modify the software (*application*) and policy store in memory 56 (*policy*) of Meir to direct the processor 52 to decompress the data to be stored according to algorithms and rules in the policy because it would optimize the performance and improve the security of the system. *See* Section VIII.A; EX1010, [0036]; EX1011, [0050]; EX1003, ¶¶72-84, 195. Further, as discussed, a POSITA would have had a reasonable expectation of success since the SSDs of Meir and Salessi have similar structures and components, and Salessi expressly teaches that the use of its processing algorithms in such similar systems. *See* Section VIII.B; EX1010, FIG. 1, [0033]; EX1011, FIG. 7, [0004]; EX1003, ¶¶85-91, 195.

h. 19[c.ii]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶196. Meir discloses *transferring the requested content*. *See* Section VIII.E.14. Salessi discloses that the *content* is *decompressed*. *See* Section VIII.F.2.g. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.F.2.g; EX1003, ¶¶72-84, 196.

3. Claim 20

a. 20[pre]

As discussed, Meir discloses SSD 24 (*apparatus*) as recited in claim 1. *See* Section VIII.C.1; EX1003, ¶197.

b. 20 [a]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶198. As discussed, Meir discloses that requested content is read from, and therefore stored on, the solid-state memory. *See* Section VIII.E.17. Salessi discloses that the *content* is *encrypted*. *See* Section VIII.D.3.b. Thus, a POSITA would have recognized that the requested content stored on the solid-state memory is encrypted. EX1003, ¶198. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.3.b; EX1003, ¶¶72-84, 198.

c. 20[b]

Meir discloses this limitation. *See* Section VIII.C.10; EX1003, ¶199.

d. 20[b.i]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶200. Meir discloses *reading the content from the solid-state memory in response to the direction from the programmable processor*. *See* Section VIII.E.17. Salessi discloses that the *content* is *encrypted*. *See* Section VIII.D.3.b. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.3.b; EX1003, ¶¶72-84, 200.

e. 20[b.ii]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶201. Meir discloses *transferring the content to the programmable processor*. *See* Section

VIII.E.18. Salessi discloses that the *content* is *encrypted*. See Section VIII.D.3.b. A POSITA would have been motivated to combine Meir with Salessi. See Sections VIII.A-B, VIII.D.3.b; EX1003, ¶¶72-84, 201.

f. 20[c]

Meir discloses this limitation. See Sections VIII.C.10, VIII.E.12-13; EX1003, ¶202.

g. 20[c.i]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶¶203-206.

Salessi's processing unit can *decrypt encrypted content* because "[p]rocessing capabilities incorporated into the SSD may include encryption and decryptions [and] compression and decompression." EX1011, [0006], [0023] ("Salessi further teaches that the processing unit "us[es] a processing algorithm[] to generate processed data."); see Section VIII.C.8.

In the combination, the Meir's policy stored in memory 56 includes Salessi's decryption. Specifically, Meir teaches that the "one or more of the rules in the memory controller policy may be configurable" and "the host may issue to the memory controller a command that configures or modifies the memory controller, so as to improve performance." EX1010, [0055]. A POSITA would therefore modify the memory controller policy of Meir to incorporate the decryption algorithms and instructions of Salessi, wherein Meir's policy would define which

data to apply Salessi's decompression algorithms to. EX1011, [0006]; EX1003, ¶205.

As discussed, a POSITA would have been motivated to modify the software (*application*) and policy store in memory 56 (*policy*) of Meir to direct the processor 52 to decrypt the data to be stored according to algorithms and rules in the policy because it would optimize the performance and improve the security of the system. *See* Section VIII.A; EX1010, [0036]; EX1011, [0050]; EX1003, ¶206. Further, as discussed, a POSITA would have had a reasonable expectation of success since the SSDs of Meir and Salessi have similar structures and components, and Salessi expressly teaches that the use of its processing algorithms in such similar systems. *See* Section VIII.B; EX1010, FIG. 1, [0033]; EX1011, FIG. 7, [0004]; EX1003, ¶206.

h. 20[c.ii]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶207. Meir discloses *transferring the requested content*. *See* Section VIII.E.14. Salessi discloses that the *content* is *decrypted*. *See* Section VIII.F.3.g. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.F.3.g; EX1003, ¶¶72-84, 207.

4. Claim 30

a. 30[pre]

Meir discloses this limitation. *See* Sections VIII.E.10-13, 15-18; EX1003, ¶208.

b. 30[a]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.D.2.b; EX1003, ¶209.

c. 30[b]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.D.2.c; EX1003, ¶210.

d. 30[c]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶211. Meir discloses *subsequent to storing the content on the solid-state memory and in response to receiving a content request, directing the device controller to read the content from the solid-state memory*. *See* Section VIII.E.11. Salessi discloses that the *content is compressed*. *See* Section VIII.D.2.b. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.2.b; EX1003, ¶¶72-84, 211.

e. 30[d]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶212. Meir discloses *receiving the requested content from the device controller*. *See* Section

VIII.E.12. Salessi discloses that the *content* is *compressed*. See Section VIII.D.2.b.

A POSITA would have been motivated to combine Meir with Salessi. See Sections VIII.A-B, VIII.D.2.b; EX1003, ¶¶72-84, 212.

f. 30[e]

Meir in view of Salessi renders obvious this limitation. See Section VIII.F.2.g; EX1003, ¶213.

g. 30[f]

Meir in view of Salessi renders obvious this limitation. See Section VIII.F.2.h; EX1003, ¶214.

h. 30[g]

Meir discloses this limitation. See Section VIII.C.10; EX1003, ¶215.

i. 30[g.i]

Meir in view of Salessi renders obvious this limitation. See Section VIII.D.2.e.; EX1003, ¶216.

j. 30[g.ii]

Meir in view of Salessi renders obvious this limitation. See Section VIII.F.2.d; EX1003, ¶217.

k. 30[g.iii]

Meir in view of Salessi renders obvious this limitation. See Section VIII.F.2.e; EX1003, ¶218.

5. Claim 31

a. 31[pre]

Meir discloses this limitation. *See* Sections VIII.E.10-13, 15-18; EX1003, ¶219.

b. 31[a]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.D.3.b; EX1003, ¶220.

c. 31[b]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.D.3.c; EX1003, ¶221.

d. 31[c]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶222. Meir discloses *subsequent to storing the content on the solid-state memory and in response to receiving a content request, directing the device controller to read the content from the solid-state memory*. *See* Section VIII.E.11. Salessi discloses that the *content* is *encrypted*. *See* Section VIII.D.3.b. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.3.b; EX1003, ¶¶72-84, 222.

e. 31[d]

Meir in view of Salessi renders obvious this limitation. EX1003, ¶223. Meir discloses *receiving the requested content from the device controller*. *See* Section

VIII.E.12. Salessi discloses that the *content* is *encrypted*. *See* Section VIII.D.3.b. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.3.b; EX1003, ¶¶72-84, 223.

f. 31[e]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.F.3.g; EX1003, ¶224.

g. 31[f]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.F.3.h; EX1003, ¶225.

h. 31[g]

Meir discloses this limitation. *See* Section VIII.C.10; EX1003, ¶226.

i. 31[g.i]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.D.3.e; EX1003, ¶227.

j. 31[g.ii]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.F.3.d; EX1003, ¶228.

k. 31[g.iii]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.F.3.e; EX1003, ¶229.

**IX. GROUND 2: MEIR IN VIEW OF SALESSI AND CHOU RENDERS
OBVIOUS CLAIMS 3-4, 18, AND 28-29**

A. Motivation to Combine

A POSITA would have been motivated to modify Meir's system, including the memory unit 40 (*solid-state memory*), the processor 52 (*programmable processor*), the memory 56 (*device memory*), the low-level controller 44 (*device controller*), and the high-speed interface 32 (*interface connector*), to be mounted on Chou's printed circuit board that is supported by a case. EX1003, ¶¶230-232.

First, such modification would optimize the performance of the system by reducing over-the-air interference from nearby signals, thereby reducing the likelihood of errors and retransmission. EX1010, [0009] (“maximiz[ing] a throughput of the execution [and] minimiz[ing] a latency of the execution”); EX1003, ¶233. *Second*, such modification would improve the resiliency and extend the life-time of the components. EX1003, ¶231. A case provides protection for the internal components from external environmental conditions. *Id.*

Nothing in Salessi teaches away from this combination because Salessi also taught better performance in data storage in SSDs like Meir and Chou. EX1003, ¶232.

B. Reasonable Expectation of Success

A POSITA would have been able to modify Meir's system to incorporate Chou's printed circuit board and case with a reasonable expectation of success.

EX1003, ¶¶233-234. The storage systems of Meir and Chou are both SSDs that include controllers and solid-state memory. EX1010, FIG.1; EX1012, [0004]; EX1003, ¶233. Using printed circuit boards and cases as taught in Chou was a well-known and common design option that was routinely used to provide better stability and protection for hardware. *Id.*

Nothing in Salessi prevents this combination because the Salessi SSD has similar structure and components to the Meir and Chou SSDs. EX1003, ¶234.

C. Dependent Claims 3, 4, 18, 28, and 29

- 1. Claims 3/18[pre]/18[a]/28: “The apparatus of claim [2]/[17/27] further comprising a printed circuit board communicatively coupled to the interface connector that mounts the solid-state memory, the device memory, the device controller, and the programmable processor.”**

Meir in view of Salessi and Chou renders obvious this limitation. EX1003, ¶¶235-239.

Meir discloses *solid-state memory* (See Section VIII.C.2), *device memory* (See Section VIII.C.3), a *device controller* (See Section VIII.C.5), a *programmable processor* (See Section VIII.C.4) and an *interface connector* (See Section VIII.D.1).

To the extent that Meir and Salessi do not explicitly disclose a *printed circuit board to mount* those components, this would have been obvious in view of Chou. EX1003, ¶237.

Chou discloses a printed circuit board assembly (PCBA) (*printed circuit board*). EX1012, [0006]. Chou also discloses that “[o]ne or more memory modules and other electronic components 122 are on the PCBA 112.” *Id.*, [0033]. A POSITA would then understand that the *solid-state memories*, *device memories*, *device controllers*, and *programmable processors* are all either “memory modules” or “other electronic components” that would be on the PCBA. EX1003, ¶238.

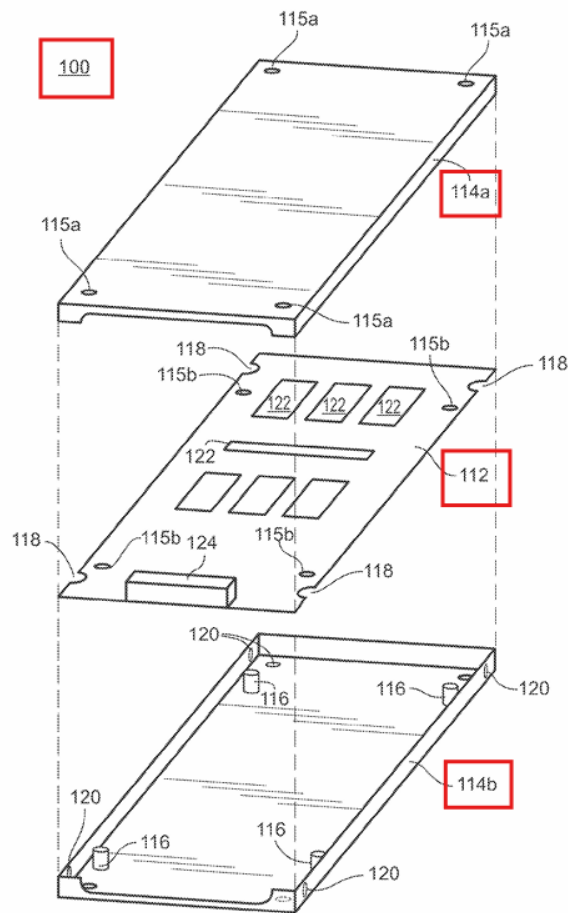
A POSITA would have combined the Meir-Salessi data storage system with Chou’s PCBA because this would have furthered Meir’s goal of “maximiz[ing] a throughput of the execution [and] minimiz[ing] a latency of the execution” because having the different components on a single PCB would reduce the amount of time and distance that data has to travel from one component to another. EX1010, [0009]; *see* Sections IX.A-B. In order to have a data storage system (like Meir-Salessi) that is composed of a solid-state memory, a device memory, a device controller, and a programmable processor, a POSITA would have understood that a printed circuit board would be used for mounting the components. EX1003, ¶239.

2. Claims 4/18[b]/29: “The apparatus of claim [3]/[17/28] further comprising a case that supports the printed circuit board.”

Meir in view of Salessi and Chou renders obvious this limitation. EX1003, ¶¶240-243.

To the extent that Meir and Salessi do not explicitly disclose *a case that supports the printed circuit board*, this would have been obvious in view of Chou. EX1003, ¶241.

Chou discloses a solid-state drive (SSD) that includes a printed circuit board assembly (“PCBA”) (*printed circuit board*) and a “housing” (*case*). EX1012, [0025]. The “housing” (*case*) *supports* the “PCBA” (*printed circuit board*) because “[t]o assemble the SSD 100, the PCBA 112 is placed inside the upper and lower covers 114a and 114b.” *Id.*, [0034], FIG. 2.



EX1012, Fig. 2

A POSITA would have combined the Meir-Salessi data storage system with Chou’s housing because this would have furthered Meir’s goal of “maximiz[ing] a throughput of the execution [and] minimiz[ing] a latency of the execution” because having a case mounting the PCB would reduce over-the-air interference from nearby signals, thereby reducing the likelihood of errors and retransmission. EX1010, [0009]; *see* Sections IX.A-B; EX1003, ¶243.

**X. GROUND 3: MEIR IN VIEW OF SALESSI AND LOVINGER
RENDERS OBVIOUS CLAIMS 9-10 AND 13-15**

A. Motivation to Combine

A POSITA would have been motivated to modify Meir-Salessi's SSD to receive a write command that includes the policy as taught by Lovinger. EX1003, ¶¶244-248.

First, such a modification would enhance the goals of Meir. One of Meir's goals is to make policies configurable. EX1010, [0011]. Lovinger teaches transmitting a storage request that includes information associated with the storage policy. EX1015, [0040], [0043]. A POSITA would have understood that including a storage policy in Meir's storage request would have increased performance because the host would not need to send a separate prior command to set the policy. EX1003, ¶245.

Second, Lovinger's approach is a natural extension of Meir's configurable policy. Lovinger teaches that including the policy with the storage request enables a client "to store content according to the retention policy without reprogramming device firmware." *Id.*, [0041]. A POSITA improving on the system of Meir would have looked at ways to configure the policy without reprogramming device firmware. EX1003, ¶246.

Third, such a modification would provide more flexibility, particularly as to the compression or encryption algorithm used. Indeed, Salessi teaches that "[t]he

algorithm used by the application layer may be communicated to the DSP by the host CPU.” EX1011, [0050]. A POSITA would have looked at known ways to communicate the Meir-Salessi compression and encryption policy from the host to the storage system as taught in Lovinger. EX1003, ¶247.

Fourth, including the policy with the storage request as taught by Lovinger was a well-known design option. By 2016, this approach was a common option among multiple specifications. EX1003, ¶248. For example, the Open-Channel SSD Interface Rev. 1.2 specifies a write command that includes the content to be stored as well as a per-write policy word that instructs the device on the recording method that should be performed. *Id.*; EX1036.

B. Reasonable Expectation of Success

A POSITA would have been able to modify Meir-Salessi’s system to incorporate the policy in a storage request as taught by Lovinger with a reasonable expectation of success. EX1003, ¶¶249-251.

The storage devices of Meir, Salessi, and Lovinger have similar structures and components. EX1010, FIG.1; EX1011, FIGS. 2, 4, 7, EX1015, [0029], [0037]-[0040], [0069], FIGS. 1, 6; EX1003, ¶250. Meir, Salessi, and Lovinger’s storage devices each include memory controller or processing unit that interfaces with the solid-state memory. EX1010, [0031] (“SSD 24 comprises multiple low-level controllers 44, each low-level controller assigned to a group of one or more memory

units 40.”), [0033]; EX1011 [0047] (“[t]he SSD processing unit 240 includes...a hardware engine 420 [and] there may be a separate hardware engine 420 for each flash channel”), [0055] (“the microcontroller 410 may be connected to a plurality of hardware engines 420.”); EX1015, [0069] (“the computing device 600 may include at least one processing unit 602 [and] data storage devices”); EX1003, ¶250.

Given the similar structures, the modification would simply be a change of the storage request flow. Figure 2 of Meir shows “a flow chart that schematically illustrates a method of data storage.” EX1010, [0019], Fig. 2. Further, Lovinger teaches sending the policy as part of the memory access command. EX1015, [0040]. Instead of the host formatting the commands at step 68, the host can include the policy with the command, and check whether there is an updated policy before executing the commands at step 76. EX1010, [0019], Fig. 2. Updating the storage request flow would have been well within the skill set of a POSITA at the relevant time. EX1003, ¶251.

C. Independent Claim 9

1. 9[pre]: “An apparatus comprising”

To the extent limiting, Meir discloses the preamble. *See* Section VIII.C.1; EX1003, ¶252.

2. 9[a]: “a solid-state memory;”

Meir discloses this limitation. *See* Section VIII.C.2; EX1003, ¶253.

3. **9[b]: “a device memory;”**

Meir discloses this limitation. *See* Section VIII.C.3; EX1003, ¶254.

4. **9[c]: “a programmable processor operatively coupled to the device memory;”**

Meir discloses this limitation. *See* Section VIII.C.4; EX1003, ¶255.

5. **9[d]: “a device controller operatively coupled with the solid-state memory and the programmable processor; and”**

Meir discloses this limitation. *See* Section VIII.C.5; EX1003, ¶256.

6. **9[e]: “an application stored on the device memory and comprising instructions that, when executed by the programmable processor, direct the programmable processor to at least:”**

Meir discloses this limitation. *See* Section VIII.C.6; EX1003, ¶257.

7. **9[e.i]: “receive a storage request comprising content and a storage device policy;”**

Meir in view of Salessi and Lovinger renders obvious this limitation. EX1003, ¶¶258-262.

Meir discloses *receiving a storage request comprising content*. *See* Section VIII.C.7; EX1003, ¶¶259. Meir and Salessi disclose a *storage device policy*. *See* Section VIII.C.8. To the extent that Meir and Salessi do not explicitly disclose a *storage request comprising...a storage device policy*, this would have been obvious in view of Lovinger. EX1003, ¶259.

Lovinger discloses that “the client 110 may store content 112 on a server 120.”

EX1015, [0029]. A POSITA would have understood that storing *content* 112 requires the client to send a *storage request* that the storage device can execute to store the *content* 112. EX1003, ¶260. Lovinger further teaches a retention policy which is a *storage device policy* because “the content is written to the one or more storage devices based on the retention policy.” EX1015, [0003]; *see also id.* [0029] (“the storage attributes and capabilities of the one or more storage devices utilized by the server 120 may include retention policies”); EX1003, ¶260.

Lovinger discloses *storage request comprising a storage device policy*: “the client 110 may transmit the content 112 to the server 120 with information corresponding to the retention policy 130.” *Id.*, [0040]; *see also id.*, FIG. 1. Specifically, “when the content and retention policy have been received, the server 120 writes the content 112 to one or more storage devices associated with the server 120 according to the retention policy 130.” *Id.*, [0040]; EX1003, ¶261.

As discussed, a POSITA would have been motivated to modify the Meir-Salessi system to include the storage policy in the storage request as taught by Lovinger with a reasonable expectation of success. *See* Section X.A-B; EX1003, ¶262.

8. **9[e.ii]: “in response to receiving the storage request and the storage device policy, process the content for storage based on the storage device policy; and”**

Meir in view of Salessi renders obvious this limitation. *See* Sections VIII.C.7-

8; EX1003, ¶263.

**9. 9[e.iii]: “transfer the content to the device controller;
and”**

Meir discloses this limitation. *See* Section VIII.C.9; EX1003, ¶264.

10. 9[f]: “the device controller configured to:”

Meir discloses this limitation. *See* Section VIII.C.10; EX1003, ¶265.

**11. 9[f.i]: “receive the content from the programmable
processor and store the content on the solid-state
memory.”**

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.C.11;
EX1003, ¶266.

D. Dependent Claims 10, 13-15

1. Claim 10

Meir discloses this limitation. *See* Section VIII.D.1; EX1003, ¶267.

2. Claim 13

a. 13[pre]

Meir discloses this limitation. *See* Section VIII.D.2.a; EX1003, ¶268.

b. 13[a]

Meir in view of Salessi renders obvious this limitation. *See* Section
VIII.D.2.b; EX1003, ¶269. A POSITA would have been motivated to combine Meir
with Salessi. *See* Sections VIII.A-B, VIII.D.2.b; EX1003, ¶269.

c. 13[b]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.D.2.c; EX1003, ¶270. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.2.b; EX1003, ¶270.

d. 13[c]

Meir discloses this limitation. *See* Section VIII.D.2.d; EX1003, ¶271.

e. 13[d]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.D.2.e; EX1003, ¶272. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.2.b; EX1003, ¶272.

3. Claim 14

a. 14[pre]

Meir discloses this limitation. *See* Section VIII.D.3.a; EX1003, ¶273.

b. 14[a]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.D.3.b; EX1003, ¶274. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.3.b; EX1003, ¶274.

c. 14[b]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.D.3.c; EX1003, ¶275. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.3.b; EX1003, ¶275.

d. 14[c]

Meir discloses this limitation. *See* Section VIII.D.3.d; EX1003, ¶276.

e. 14[d]

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.D.3.e; EX1003, ¶277. A POSITA would have been motivated to combine Meir with Salessi. *See* Sections VIII.A-B, VIII.D.3.b; EX1003, ¶277.

4. Claim 15

Meir in view of Salessi renders obvious this limitation. *See* Section VIII.D.4; EX1003, ¶278.

**XI. GROUND 4: MEIR IN VIEW OF SALESSI, LOVINGER, AND CHOU
RENDERS OBVIOUS CLAIMS 11 AND 12**

A. Motivation to Combine

A POSITA would have been motivated to combine Meir-Lovinger with Chou for the reasons discussed above. *See* Sections IX.A-B, X.A-B; EX1003, ¶¶279-280. Nothing in Lovinger would have taught away from this combination as Lovinger also taught a data storage system which would have benefited from the use of PCBs and cases to protect its hardware components.

B. Reasonable Expectation of Success

A POSITA would have combined Meir-Lovinger with Chou with a reasonable expectation of success for the reasons discussed above. *See* Sections IX.A-B, X.A-B; EX1003, ¶¶281-282.

Nothing in Lovinger would have prevented this combination, as a POSITA would have modified the Meir-Lovinger system with software changes which would not have impacted the hardware.

1. Claims 11

Meir in view of Lovinger and Chou renders obvious this limitation. *See* Section IX.C.1; EX1003, ¶¶283. A POSITA would have been motivated to combine Meir-Lovinger with Chou for the reasons discussed above. *See* Sections IX.A-B; EX1003, ¶283.

2. Claims 12

Meir in view of Lovinger and Chou renders obvious this limitation. *See* Section IX.C.2; EX1003, ¶284. A POSITA would have been motivated to combine Meir-Lovinger with Chou. *See* Sections IX.A-B; EX1003, ¶284.

XII. SECONDARY CONSIDERATIONS

There are no secondary considerations known to Petitioners that affect, let alone overcome—this strong case of obviousness. Should PO proffer any relevant evidence of secondary considerations, Petitioners reserve their rights to address.

XIII. CONCLUSION

For these reasons, Petitioners respectfully request institution.

U.S. Patent No. 11,907,553
Petition for *Inter Partes* Review

Dated: August 5, 2026

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CLAIM LISTING APPENDIX

Claim 1

- 1 [pre] An apparatus comprising:
- 1 [a] a solid-state memory;
- 1 [b] a device memory;
- 1 [c] a programmable processor operatively coupled to the device memory;
- 1 [d] a device controller operatively coupled with the solid-state memory and the programmable processor; and
- 1 [e] an application stored on the device memory and comprising instructions that, when executed by the programmable processor, direct the programmable processor to at least:
- 1 [e.i] in response to receiving a storage request comprising content, retrieve a storage device policy from the device memory;
- 1 [e.ii] process the content for storage based on the storage device policy; and
- 1 [e.iii] transfer the content to the device controller; and
- 1 [f] the device controller configured to:
- 1 [f.i] receive the content from the programmable processor and store the content on the solid-state memory.

Claim 2

- 2 The apparatus of claim 1 further comprising an interface connector that communicatively couples the solid-state memory, the device controller, the programmable processor, and the device memory to a host computer.

Claim 3

- 3 The apparatus of claim 2 further comprising a printed circuit board communicatively coupled to the interface connector that mounts the solid-state memory, the device memory, the device controller, and the programmable processor.

Claim 4

- 4 The apparatus of claim 3 further comprising a case that supports the printed circuit board.

Claim 5

- 5 [pre] The apparatus of claim 1 wherein the instructions that, when executed, direct the programmable processor to process the content for storage based on the storage device policy and transfer the content to the device controller comprise the instructions that, when executed, direct the programmable processor to:

- 5 [a]: compress the content based on the storage device policy;
- 5 [b]: transfer the compressed content to the device controller; and wherein:
- 5 [c]: the device controller is configured to:
- 5 [d]: receive the compressed content from the programmable processor and store the compressed content on the solid-state memory.

Claim 6

- 6 [pre] The apparatus of claim 1 wherein the instructions that, when executed, direct the programmable processor to process the content for storage based on the storage device policy and transfer the content to the device controller comprise the instructions that, when executed, direct the programmable processor to:
- 6 [a] encrypt the content based on the storage device policy;
- 6 [b] transfer the encrypted content to the device controller; and wherein:
- 6 [c] the device controller is configured to:
- 6[d] receive the encrypted content from the programmable processor and store the encrypted content on the solid-state memory.

Claim 7

- 7 The apparatus of claim 1 wherein the content comprises one or more of medical records, video data, image data, on-line temporal video data, cached data, financial data, online transaction data, credit card data, or medical data.

Claim 9

- 9 [pre] An apparatus comprising:
- 9 [a] a solid-state memory;
- 9 [b] a device memory;
- 9 [c] a programmable processor operatively coupled to the device memory;

- 9 [d] a device controller operatively coupled with the solid-state memory and the programmable processor; and
- 9 [e] an application stored on the device memory and comprising instructions that, when executed by the programmable processor, direct the programmable processor to at least:
 - 9 [e.i] receive a storage request comprising content and a storage device policy;
 - 9 [e.ii] in response to receiving the storage request and the storage device policy, process the content for storage based on the storage device policy; and
 - 9 [e.iii] transfer the content to the device controller; and
- 9 [f] the device controller configured to:
 - 9 [f.i] receive the content from the programmable processor and store the content on the solid-state memory.

Claim 10

- 10 The apparatus of claim 9 further comprising an interface connector that communicatively couples the solid-state memory, the device controller, the programmable processor, and the device memory to a host computer.

Claim 11

- 11 The apparatus of claim 10 further comprising a printed circuit board communicatively coupled to the interface connector that mounts the solid-state memory, the device memory, the device controller, and the programmable processor.

Claim 12

- 12** The apparatus of claim 11 further comprising a case that supports the printed circuit board.

Claim 13

- 13 [pre]** The apparatus of claim 9 wherein the instructions that, when executed, direct the programmable processor to process the content for storage based on the storage device policy and transfer the content to the device controller comprise the instructions that, when executed, direct the programmable processor to:
- 13 [a]** compress the content based on the storage device policy;
- 13 [b]** transfer the compressed content to the device controller; and wherein:
- 13 [c]** the device controller is configured to:
- 13 [d]** receive the compressed content from the programmable processor and store the compressed content on the solid-state memory.

Claim 14

- 14 [pre]** The apparatus of claim 1 wherein the instructions that, when executed, direct the programmable processor to process the content for storage based on the storage device policy and transfer the content to the device controller comprise the instructions that, when executed, direct the programmable processor to:
- 14 [a]** encrypt the content based on the storage device policy;

- 14 [b] transfer the encrypted content to the device controller; and wherein:
- 14 [c] the device controller is configured to:
- 14 [d] receive the encrypted content from the programmable processor and store the encrypted content on the solid-state memory.

Claim 15

- 15 The apparatus of claim 9 wherein the content comprises one or more of medical records, video data, image data, on-line temporal video data, cached data, financial data, online transaction data, credit card data, or medical data.

Claim 16

- 16 [pre] An apparatus comprising:
- 16 [a] a solid-state memory
- 16 [b] a device memory;
- 16 [c] a programmable processor operatively coupled to the device memory;
- 16 [d] a device controller operatively coupled with the solid-state memory and the programmable processor; and
- 16 [e] an application stored on the device memory and comprising instructions that, when executed by the programmable processor, direct the programmable processor to at least:

- 16 [e.i] in response to receiving a content request to retrieve content, retrieve a storage device policy from the device memory;
- 16 [e.ii] direct the device controller to read the requested content from the solid-state memory;
- 16 [e.iii] receive the requested content from the device controller and process the requested content for transfer based on the storage device policy; and
- 16 [e.iv] transfer the requested content; and
- 16 [f] the device controller configured to:
 - 16 [f.i] read the requested content from the solid-state memory in response to the direction from the programmable processor; and
 - 16 [f.ii] transfer the requested content to the programmable processor.

Claim 17

- 17 The apparatus of claim 16 further comprising an interface connector that communicatively couples the solid-state memory, the device controller, the programmable processor, and the device memory to a host computer.

Claim 18

- 18 [pre] The apparatus of claim 17 further comprising:

- 18 [a]** a printed circuit board communicatively coupled to the interface connector that mounts the solid-state memory, the device memory, the device controller, and the programmable processor; and
- 18 [b]** a case that supports the printed circuit board.

Claim 19

- 19 [pre]** The apparatus of claim 16 wherein:
- 19 [a]** the requested content stored on the solid-state memory is compressed;
- 19 [b]** the device controller is configured to:
- 19 [b.i]** read the compressed content from the solid-state memory in response to the direction from the programmable processor; and
- 19 [b.ii]** transfer the compressed content to the programmable processor; and
- 19 [c]** the instructions that, when executed, direct the programmable processor to process the requested content for transfer based on the storage device policy and transfer the requested content comprise the instructions that, when executed, direct the programmable processor to:
- 19 [c.i]** decompress the compressed content based on the storage device policy; and
- 19 [c.ii]** transfer the decompressed content.

Claim 26

- 26 [pre]** An apparatus comprising:
- 26 [a]** a solid-state memory;
- 26 [b]** a device memory;
- 26 [c]** a programmable processor operatively coupled to the device memory;
- 26 [d]** a device controller operatively coupled with the solid-state memory and the programmable processor; and
- 26 [e]** an application stored on the device memory and comprising instructions that, when executed by the programmable processor, direct the programmable processor to at least:
- 26 [e.i]** in response to receiving a storage request comprising content, retrieve a storage device policy from the device memory;
- 26 [e.ii]** process the content for storage based on the storage device policy;
- 26 [e.iii]** transfer the content to the device controller;
- 26 [e.iv]** subsequent to storing the content on the solid-state memory and in response to receiving a content request, direct the device controller to read the requested content from the solid-state memory;
- 26 [e.v]** receive the requested content from the device controller;
- 26 [e.vi]** process the requested content for transfer based on the storage device policy; and
- 26 [e.vii]** transfer the requested content; and

- 26 [f] the device controller configured to:
- 26 [f.i] receive the content from the programmable processor and store the content on the solid-state memory;
- 26 [f.ii] read the requested content from the solid-state memory in response to the direction from the programmable processor; and
- 26 [f.iii] transfer the requested content to the programmable processor.

Claim 27

- 27 The apparatus of claim 26 further comprising an interface connector that communicatively couples the solid-state memory, the device controller, the programmable processor, and the device memory to a host computer.

Claim 28

- 28 The apparatus of claim 27 further comprising a printed circuit board communicatively coupled to the interface connector that mounts the solid-state memory, the device memory, the device controller, and the programmable processor.

Claim 29

- 29 The apparatus of claim 28 further comprising a case that supports the printed circuit board.

Claim 30

- 30 [pre] The apparatus of claim 26 wherein the instructions that, when executed, direct the programmable processor to retrieve a storage

device policy from the device memory, process the content for storage based on the storage device policy, transfer the content to the device controller; direct the device controller to read the requested content from the solid-state memory, receive the requested content from the device controller, process the requested content for transfer based on the storage device policy, and transfer the requested content comprise the instructions that, when executed, direct the programmable processor to:

- 30 [a] compress the content based on the storage device policy;
- 30 [b] transfer the compressed content to the device controller;
- 30 [c] subsequent to storing the compressed content on the solid-state memory and in response to receiving a content request, direct the device controller to read the compressed content from the solid-state memory;
- 30 [d] receive the compressed content from the device controller;
- 30 [e] decompress the compressed content based on the storage device policy; and
- 30 [f] transfer the decompressed content; and wherein:
- 30 [g] the device controller is configured to:
 - 30 [g.i] receive the compressed content from the programmable processor and store the compressed content on the solid-state memory;
 - 30 [g.ii] read the compressed content from the solid-state memory in response to the direction from the programmable processor; and
 - 30 [g.iii] transfer the compressed content to the programmable processor.

Claim 31

- 31 [pre]** The apparatus of claim 26 wherein the instructions that, when executed, direct the programmable processor to retrieve a storage device policy from the device memory, process the content for storage based on the storage device policy, transfer the content to the device controller; direct the device controller to read the requested content from the solid-state memory, receive the requested content from the device controller, process the requested content for transfer based on the storage device policy, and transfer the requested content comprise the instructions that, when executed, direct the programmable processor to:
- 31 [a]** encrypt the content based on the storage device policy;
- 31 [b]** transfer the encrypted content to the device controller;
- 31 [c]** subsequent to storing the encrypted content on the solid-state memory and in response to receiving a content request, direct the device controller to read the encrypted content from the solid-state memory;
- 31 [d]** receive the encrypted content from the device controller;
- 31 [e]** decrypt the encrypted content based on the storage device policy; and
- 31 [f]** transfer the decrypted content; and wherein:
- 31 [g]** the device controller is configured to:
- 31 [g.i]** receive the encrypted content from the programmable processor and store the encrypted content on the solid-state memory;
- 31 [g.ii]** read the encrypted content from the solid-state memory in response to the direction from the programmable processor; and
- 31 [g.iii]** transfer the encrypted content to the programmable processor.

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that foregoing
**PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO.
11,907,553** exclusive of the parts exempted as provided in 37 C.F.R. §42.24(a),
contains 13,990 words and therefore complies with the type-volume limitations of
37 C.F.R. §42.24(a).

Dated: August 5, 2026

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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the foregoing **Petition for *Inter Partes* Review of U.S. Patent No. 11,907,553 and Exhibits** are being served on August 5, 2026 via Federal Express overnight mail on counsel of record for U.S. Patent No. 11,907,553 as addressed below:

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