IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF TEXAS
FORT WORTH DIVISION

GAEA, LLC,	)	Case No. 4:26-cv-00348-P
Plaintiff,	)	**JURY TRIAL DEMANDED**
v.	)	
META PLATFORMS, INC.,	)	
Defendant.	)	

META PLATFORMS, INC.'S INVALIDITY CONTENTIONS

Pursuant to the Court's Scheduling Order (Dkt. No. 34), Meta Platforms, Inc. ("Meta") hereby serves its Invalidity Contentions and Subject-Matter Eligibility Contentions for United States Patent Nos. 10,776,023 (the "'023 Patent"); 11,907,553 (the "'553 Patent"); and 12,265,715 (the "'715 Patent") (collectively, "the Asserted Patents"), and accompanying document production on Gaea, LLC ("Gaea").

Meta's Invalidity Contentions are based on information reasonably known and available to Meta at this time. Meta has not yet completed its investigation of the facts and documents relating to this action and has not completed its preparation for trial. Because Meta's investigation, prior art search, analysis, discovery, and trial preparation are still ongoing, Meta may identify additional prior art or arguments that will add meaning to already known prior art or arguments, lead to additions or changes to these Invalidity Contentions, and/or provide additional prior art and arguments. Meta reserves the right to amend, supplement, and/or otherwise modify these Invalidity Contentions. Meta further reserves the right to rely on any facts, documents, or other evidence that are (i) subsequently discovered; (ii) subsequently determined to be relevant for any purpose; or

(iii) subsequently determined to have been omitted from these Invalidity Contentions or from a production of documents or things in discovery, including third-party discovery. Meta further reserves the right to rely on reports and/or testimony from experts and from fact witnesses such as prior artists. Documents relating to expert testimony, if any, will be produced when expert discovery is exchanged in accordance with the Scheduling Order.

Gaea asserts that Meta infringes claims 1, 9, and 14 of the ’023 Patent; claims 1-4 and 9-12 of the ’553 Patent; and claims 1 and 9 of the ’715 Patent (collectively, “Asserted Claims”) under 35 U.S.C. § 271. *See* Plaintiff’s Disclosure of Asserted Claims. Gaea no longer asserts U.S. Patent No. 11,327,669 (the “’669 Patent”). *Id.* Gaea should not be permitted to assert any other claims of the Asserted Patents or the ’669 Patent. If Gaea is permitted to do so over Meta’s objections, Meta reserves the right to provide and rely on Invalidity Contentions for any other claim(s) that Gaea asserts, including, but not limited to, relying on prior art references not otherwise disclosed in these Invalidity Contentions.

Meta expressly denies that any accused product or any of Meta’s other products infringes the Asserted Claims, and nothing in these Invalidity Contentions should be interpreted as contradicting that express denial of infringement.

The Asserted Claims are invalid under the claim constructions Gaea has implied or assumed in its Infringement Contentions; the claim constructions Meta has implied or assumed in these Invalidity Contentions; and any other constructions the Court may adopt that are in accordance with law. Meta therefore has based its Invalidity Contentions, at least in part, on the claim constructions or positions that Gaea appears to have adopted (explicitly or implicitly) in its Complaint and in its Infringement Contentions, which include deficiencies and ambiguities that necessarily limit Meta’s ability to understand how Gaea is interpreting the Asserted Claims.

Nothing in these Invalidity Contentions should be construed as an admission that Meta agrees with any of Gaea's explicit or implicit claim constructions. To be clear, Meta expressly reserves the right to challenge the sufficiency of Gaea's Infringement Contentions and the construction of any claims or claim terms, phrases, or clauses that Gaea purports to have explicitly or implicitly construed, that Gaea identifies, or that Gaea may construe in the future. If Gaea proposes new constructions, purports to clarify its existing constructions, or otherwise identifies any constructions in its forthcoming proposed claim terms for construction, preliminary constructions, or throughout the claim construction process, Meta reserves its right to amend, supplement, and/or otherwise modify these Invalidity Contentions. Meta further reserves its right to amend, supplement, and/or otherwise modify these Invalidity Contentions following any constructions adopted by the Court. Prior art not included in this disclosure, whether or not now known to Meta, also may become relevant depending on the claim constructions ultimately adopted by the Court. Under a correct reading of the Asserted Claims in light of the specifications and prosecution histories, the Asserted Claims are invalid for anticipation and/or obviousness based on the prior art cited in these Invalidity Contentions; and for lack of written description and/or enablement under 35 U.S.C. § 112(a).

The obviousness combinations of references provided below under 35 U.S.C. § 103 are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified below or references yet to be identified are possible, and Meta reserves the right to use any such combination(s) in this litigation. In particular, Meta is currently unaware of the extent, if any, to which Gaea will contend that limitations of the Asserted Claims are not disclosed in the art Meta has identified. If an issue arises with respect to any such limitation, Meta reserves the right to identify other references that would have made obvious the addition of the

allegedly missing limitation to the disclosed product or method.

Meta further reserves the right to amend its Invalidity Contentions to substitute or add alternative invalidating references if Gaea attempts to demonstrate entitlement to an earlier effective filing date for the Asserted Patents.

The accompanying invalidity claim charts identify specific examples of where a prior art reference discloses—either expressly, implicitly in the larger context of the passage, or inherently—each limitation of the Asserted Claims and/or examples of disclosures in view of which a person of ordinary skill in the art would have considered each limitation anticipated and/or obvious. Where Meta cites to a particular figure in any prior art reference, the citation should be understood to encompass the caption and description of the figure and the text relating to and/or describing the figure. Where Meta cites to particular text that refers to a figure, the citation should be understood to include the figure and related figures as well. In addition, the accompanying invalidity claim charts include examples of where the prior art discloses the subject matter recited in the preambles of the Asserted Claims without regard to whether the preambles are properly considered to be limitations of these claims.

In the accompanying invalidity claim charts, Meta has endeavored to identify the most relevant portions of the references. But the references may contain additional support for particular claim limitations, including additional invalidity support for ambiguous terms, phrases, or clauses for which it is unclear how Gaea purports to construe the term/phrase/clause or how it should be properly construed. Meta reserves the right to rely on uncited portions of prior art references, other documents and/or instrumentalities, and fact and/or expert testimony to provide context or to aid in understanding the references and/or cited portions thereof. Moreover, Meta may rely on admissions concerning the scope of the prior art relevant to the Asserted Patents found in, *inter*

alia, (1) the patents' prosecution history and the prosecution history of related patents and/or patent applications; (2) any testimony or declarations of named inventors or other fact or expert witnesses concerning the prior art, the Asserted Patents, and/or related patents and/or patent applications; or (3) any papers filed or evidence Gaea submits in connection with this litigation or in any other pending or future proceeding involving Gaea or any of its predecessors-in-interest or one or more of the Asserted Patents or any related patents.

These disclosures are made without waiver of or prejudice to any objections that Meta may have regarding the subject matter of these disclosures or any documents or individuals identified herein. Meta expressly reserves all objections, including but not limited to: (a) relevance; (b) attorney-client privilege; (c) common interest privilege; (d) work-product privilege and protection; (e) any other applicable privilege or protection under federal or state law; (f) undue burden; (g) overbreadth; (h) the admissibility in evidence of these disclosures or the subject matter thereof; (i) production of proprietary and confidential business information, financial data, trade secrets, or secrets that belong to Meta; and (j) any other proper ground. All objections are expressly reserved.

I. *Sotera*-Plus Stipulation

The Asserted Patents are subject to pending IPR petitions: IPR2026-00425, IPR2026-00426, and IPR2026-00427. If one or more of the IPRs are instituted, Meta will amend its asserted prior art in compliance with IPR estoppel and any applicable stipulations. Specifically, Meta entered into a stipulation by letter served on September 9, 2026, stating as follows:

> We write to state stipulations hereby provided by Meta Platforms, Inc. as defendant in the above-captioned litigation and Petitioner in the below-identified *inter partes* review ("IPR") proceedings before the Patent Trial and Appeal Board ("PTAB").
>
> **IPR2026-00425**
> Petitioners hereby stipulate that if the PTAB institutes an inter partes review on IPR2026-00425, then Petitioner (i) will not pursue in the pending district court litigations the specific

grounds of invalidity that were raised or grounds that reasonably could have been raised under 35 U.S.C. §§ 102 or 103 on the basis of prior art patents or printed publications in IPR2026-00425, and (ii) will not pursue in the pending district court litigations grounds of invalidity under 35 U.S.C. §§ 102 or 103 that cite to any of the prior art references listed in the grounds for IPR2026-00425 with respect to any challenged claim (*see* Grounds 1-4 of the Petition), including in combination with any other prior art that could not have been raised in IPR2026-00425 (e.g., system art) for grounds of invalidity under 35 U.S.C. § 103. To avoid any doubt, if the PTAB declines institution or rescinds institution of IPR2026-00425, then Petitioners reserve the right to pursue any grounds of invalidity, including but not limited to the grounds in (i) and (ii), in the pending district court litigations.

IPR2026-00426
Petitioners hereby stipulate that if the PTAB institutes an inter partes review on IPR2026-00426, then Petitioner (i) will not pursue in the pending district court litigations the specific grounds of invalidity that were raised or grounds that reasonably could have been raised under 35 U.S.C. §§ 102 or 103 on the basis of prior art patents or printed publications in IPR2026-00426, and (ii) will not pursue in the pending district court litigations grounds of invalidity under 35 U.S.C. §§ 102 or 103 that cite to any of the prior art references listed in the grounds for IPR2026-00426 with respect to any challenged claim (*see* Grounds 1-4 of the Petition), including in combination with any other prior art that could not have been raised in IPR2026-00426 (e.g., system art) for grounds of invalidity under 35 U.S.C. § 103. To avoid any doubt, if the PTAB declines institution or rescinds institution of IPR2026-00426, then Petitioners reserve the right to pursue any grounds of invalidity, including but not limited to the grounds in (i) and (ii), in the pending district court litigations.

IPR2026-00427
Petitioners hereby stipulate that if the PTAB institutes an inter partes review on IPR2026-00427, then Petitioner (i) will not pursue in the pending district court litigations the specific grounds of invalidity that were raised or grounds that reasonably could have been raised under 35 U.S.C. §§ 102 or 103 on the basis of prior art patents or printed publications in IPR2026-00427, and (ii) will not pursue in the pending district court litigations grounds of invalidity under 35 U.S.C. §§ 102 or 103 that cite to any of the prior art references listed in the grounds for IPR2026-00427 with respect to any challenged claim (*see* Grounds 1-3 of the Petition), including in combination with any other prior art that could not have been raised in IPR2026-00427 (e.g., system art) for grounds of invalidity under 35 U.S.C. § 103. To avoid any doubt, if the PTAB declines institution or rescinds institution of IPR2026-00427, then Petitioners reserve the right to pursue any grounds of invalidity, including but not limited to the grounds in (i) and (ii), in the pending district court litigations.

For the avoidance of doubt, for any IPR that is instituted, the above stipulation will go into effect and Meta hereby disclaims from these Invalidity Contentions any prior art grounds identified in the respective stipulation.

II. Invalidity Contentions

A. Prior Art

Meta identifies the following prior art as anticipating the Asserted Claims and/or rendering them obvious under 35 U.S.C. § 103, combined with other references and/or the background knowledge of a person of ordinary skill in the art at the time of the alleged invention of the Asserted Patents:

1. U.S. Patent Publication No. 2012/0166749 ("Eleftheriou")
2. UK Patent Application Publication No. GB 2,448,353 A ("Broadbent")
3. U.S. Patent No. 9,256,542 ("Flower")
4. U.S. Patent No. 7,549,016 ("Fujibayashi")
5. U.S. Patent Publication No. 2015/0381727 ("Muhlestein")
6. U.S. Patent No. 9,052,823 ("Yamamoto")
7. U.S. Patent Publication No. 2017/0249080 ("Bonnet")
8. Willow System
9. Seagate Kinetic System
10. Samsung PM953S System
11. Micron M600 System
12. U.S. Patent Publication No. 2016/0313943 ("Hashimoto")
13. U.S. Patent No. 8,874,835 ("Davis")
14. U.S. Patent Publication No. 2015/0032938 ("Salessi")
15. U.S. Patent Publication No. 2014/0089278 ("Lovinger")
16. U.S. Patent Publication No. 2015/0146364 ("Chou")
17. U.S. Patent Publication No. 2012/0246435 ("Meir")
18. U.S. Patent Publication No. 2015/0052167 ("Olster")

19. International Publication No. WO 2014/136263 ("Kubota")

20. U.S. Patent No. 7,853,759 ("Sadovsky")

21. U.S. Patent No. 9,760,502 ("Raam")

22. Samsung PM1633a System

23. Samsung 840 Pro System

The above-referenced patents and publications constitute prior art to the Asserted Patents regardless of whether the Asserted Patents can claim priority to the provisional application. Specifically, the patents and publications are prior art under §§ 102(a)(1)-(2) because they are issued patents or patent applications that name another inventor and were effectively filed before November 7, 2016, or printed publications published before November 7, 2016.

The above-referenced prior art systems constitute prior art to the Asserted Patents regardless of whether the Asserted Patents can claim priority to the provisional application. Specifically, the systems are prior art under § 102(a)(1) because they were in public use, on sale, or otherwise available to the public before November 7, 2016.

- **Willow System**

The Willow System is a solid-state drive developed by Sudharsan Seshadri, Mark Gahagan, Sundaram Bhaskaran, Trevor Bunker, Arup De, Yanqin Jin, Yang Liu, and Steven Swanson of the University of California, San Diego. They presented their findings at the 11th USENIX Symposium on Operating Systems Design and Implementation on October 6-8, 2014. (https://www.usenix.org/system/files/conference/osdi14/osdi14-paper-seshadri.pdf.)

The Willow System was in public use, on sale, or otherwise available to the public by at least October 2014. (*See, e.g.*, https://www.usenix.org/system/files/conference/osdi14/osdi14-paper-seshadri.pdf.)

- **Seagate Kinetic System**

The Seagate Kinetic System is a hard disk drive and solid-state drive system manufactured by Seagate. It was in public use, on sale, or otherwise available to the public by at least October 2013. (*See, e.g.*, https://investors.seagate.com/news/news-details/2013/New-Seagate-Breakthrough-Fundamentally-Alters-Cloud-Economics/default.aspx.)

- **Micron M600 System**

The Micron M600 System is a solid-state drive manufactured by Micron and was in public use, on sale, or otherwise available to the public by at least September 2014. (*See, e.g.*, https://www.tweaktown.com/news/40189/micron-announces-m600-2-5-sata-msata-and-m-2-ssds-for-oems/index.html.)

- **Samsung PM953S System**

The Samsung PM953S is a PCIe NVMe enterprise solid-state drive in the M.2 form factor that implements Samsung's multi-stream technology. The PM953S uses host-directed stream control to allow the host to indicate which data writes share a similar lifetime, so that the device can place related data together in the same erase blocks.

The Samsung PM953S System was in public use, on sale, or otherwise available to the public by at least July 2015. (*See, e.g.*, https://download.semiconductor.samsung.com/resources/brochure/Multi-Stream%20SSD%20Technology.pdf.) In addition, Meta incorporates by reference pages 28-33 from the invalidity contentions cover pleading served by Samsung in the *Gaea, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:26-cv-264-JRG-RSP (E.D. Tex.) litigation on August 31, 2026.

- **Samsung PM1633a System**

The Samsung PM1633a is an enterprise solid-state drive in a 2.5-inch form factor that uses a dual-port SAS 12 Gb/s (SAS 3.0) interface and implements multi-stream, stream-directed data placement, including the SAS/SCSI stream commands necessary for multi-stream operation.

The Samsung PM1633a System was in public use, on sale, or otherwise available to the public before November 2016. Meta incorporates by reference pages 33-35 from the invalidity contentions cover pleading served by Samsung in the *Gaea, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:26-cv-264-JRG-RSP (E.D. Tex.) litigation on August 31, 2026.

- **Samsung 840 Pro System**

The Samsung 840 Pro is a 2.5-inch solid-state drive that uses a SATA 6 Gb/s interface. Samsung engineers developed and implemented a multi-stream interface on the 840 Pro that allowed the host system to inform the SSD of the expected lifetime of data being written, enabling the SSD to place data with similar lifetimes together and reduce garbage-collection overhead. The implementation supported four explicit streams plus a default stream, communicated stream IDs at the SATA command level, and included host-side Linux kernel modifications to pass stream IDs from applications through the file system to the SSD.

The Samsung 840 Pro System was in public use, on sale, or otherwise available to the public by at least June 17, 2014. In addition, Meta incorporates by reference pages 25-28 from the invalidity contentions cover pleading served by Samsung in the *Gaea, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:26-cv-264-JRG-RSP (E.D. Tex.) litigation on August 31, 2026.

B. Additional Prior Art Systems

Meta's prior art investigation has also identified the following prior art systems, which were known, used, offered for sale, and/or sold in the United States prior to the earliest alleged

priority date of the Asserted Patents:

1. Pure Storage FlashArray System
2. Toshiba NVMe PCIe System
3. Toshiba Opal SED System
4. Veritas SmartIO System

Meta is pursuing third-party discovery concerning these systems. Meta reserves the right to amend or supplement these Invalidity Contentions to chart and rely upon these systems, alone or in combination with any other prior art identified herein or hereafter, upon obtaining discovery concerning them, and will seek leave to do so to the extent required. Meta further reserves the right to rely on these systems as evidence of the state of the art and of the knowledge and motivations of a person of ordinary skill in the art.

C. Disclosures Regarding Anticipation and Obviousness

Meta identifies whether each of the above prior art references anticipates and/or renders obvious the Asserted Claims and produces exemplary invalidity claim charts as Exhibits 1-21. Exhibits 1-21 are invalidity claim charts for prior art items 1-21 in the list found above in Section II.A. With respect to the Samsung PM953S System, Samsung PM1633a System, and the Samsung 840 Pro System, Meta incorporates by reference the invalidity claim charts for those systems disclosed by Samsung in the *Gaea, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:26-cv-264-JRG-RSP (E.D. Tex.) litigation on August 31, 2026, including Ex. Nos. 023-05, 023-06, 553-05, 553-06, 715-05, 715-06. Meta also identifies examples of combinations of the above prior art references that make the Asserted Claims invalid under 35 U.S.C. § 103 for obviousness. A person of ordinary skill in the art would have been motivated to combine prior art references in the manner identified, including in combination with the person of ordinary skill in the art's own knowledge.

The exemplary invalidity claim charts identify where each element of the Asserted Claims can be found in each prior art reference. For many prior art references and claim elements, the prior art reference discloses the claim element in multiple places (including any of the supporting documents used to describe each prior art instrumentality) or there are multiple descriptions of where and how the prior art reference discloses the claim element. Thus, Meta has provided exemplary citations to descriptions of where each element of the Asserted Claims is found within each prior art reference. Meta may rely on other descriptions of where each element of the Asserted Claims is found within each prior art reference. In instances where Meta cites a particular figure or table in a prior art reference, the citation should be understood to encompass the caption and description of the figure or table and any text relating to that figure or table. Similarly, where a cited portion of text refers to a figure or table, the citation should be understood to include the figure or table as well.

Where Meta identifies a prior art reference as anticipating the Asserted Claims, any element of the Asserted Claims that is not expressly disclosed by the prior art reference is implicitly and/or inherently disclosed by the prior art reference—based on, for example, how the prior art reference and claim element would be understood by a person of ordinary skill in the art at the time of the alleged invention. If any of the prior art references are found not to anticipate the Asserted Claims, Meta contends that these references nevertheless render the Asserted Claims obvious, individually or at least in combination with each other or other references, as explained herein and in the accompanying charts. If prior art identified by Meta as anticipating is found not to anticipate the Asserted Claims, the Asserted Claims do not go beyond combining known elements to achieve predictable results or do more than choose between clear alternatives known to those of skill in the art. If prior art Meta has identified as anticipating is found not to anticipate

the Asserted Claims, the Asserted Claims are nevertheless invalid because the Asserted Claims contain nothing that goes beyond "ordinary innovation."

As explained herein and/or in the accompanying charts, it would have been obvious to a person of ordinary skill in the art at the time of the alleged inventions claimed in the Asserted Patents to combine the various references cited herein to arrive at the Asserted Claims. Where Meta has identified a combination of prior art references that make the Asserted Claims obvious, the Exhibits identify where each element of each Asserted Claim is found within each item of prior art used in such combination. If a specific combination is not referenced herein, Meta contends that it would have been obvious to a person of ordinary skill in the art to combine the various references cited herein so as to practice the Asserted Claims. If Gaea contends that a particular claim limitation is allegedly missing in a particular reference, a person of ordinary skill in the art would have found it obvious to combine that reference with any of the other references cited herein or in the accompanying charts to arrive at the allegedly missing claim limitation.

With regard to motivation to combine and other obviousness factors, a person of ordinary skill in the art at the time of the alleged inventions of the Asserted Patents would have been motivated to combine each of the prior art references identified in the accompanying charts. The motivation and/or incentive to combine these references comes from many sources, including, but not limited to, the known published prior art references and products themselves, the background knowledge of those of ordinary skill in the art, the common field of technology of the references, and the teachings in the references directed to solving the problem that the Asserted Patents were allegedly directed to solving. These references identify and address many of the same technical issues and suggest similar solutions to those issues.

Accordingly, the teachings of the individual prior art references, combined with the

background knowledge of a person of ordinary skill in the art at the time of the alleged invention of the Asserted Patents, would have rendered obvious the Asserted Claims for at least the reasons described below and in the accompanying charts.

Meta reserves the right to amend, supplement, and/or otherwise modify these Invalidity Contentions. Among other things, Meta's investigation and discovery, including third-party discovery, in connection with this lawsuit is ongoing, and these contentions are based on information obtained to date. The Court has not yet construed any terms or phrases of the Asserted Claims, and Gaea has not provided any validity contentions in response to any of Meta's Invalidity Contentions. In particular, Gaea has not identified any way in which it disputes that the Asserted Claims are invalid based on the prior art Meta has identified, including any way in which Gaea disputes that these prior art references disclose each and every element of each Asserted Claim either by anticipation or through obviousness. Accordingly, Meta reserves the right to amend, supplement, and/or otherwise modify these Invalidity Contentions. If, for example, Gaea disputes that a prior art reference discloses a claim element, Meta may identify other aspects or disclosures of the prior art reference and any other prior art reference that would have made obvious the addition of the allegedly missing limitation(s) to the disclosed reference.

* * *

Accompanying exhibits include exemplary charts that identify prior art references that anticipate the Asserted Claims. In addition to the anticipatory references described below and/or in the accompanying charts, the Asserted Claims are invalid for obviousness.

The ultimate determination of whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including "(1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior

art; and (4) objective evidence of nonobviousness." *Miles Labs., Inc. v. Shandon, Inc.*, 997 F.2d 870, 877 (Fed. Cir. 1993); *see also Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966). The U.S. Supreme Court's decision in *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415–16 (2007), reaffirmed *Graham* and further held that a claimed invention can be obvious even if there is no teaching, suggestion, or motivation for combining the prior art to produce that invention. In summary, *KSR* holds that patents based on new combinations of elements or components already known in a technical field may be found to be obvious. *See generally KSR*, 550 U.S. 398. Specifically, the Court in *KSR* rejected a rigid application of the "teaching, suggestion, or motivation [to combine]" test. *Id*. at 418. "In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose of the patentee controls. What matters is the objective reach of the claim." *Id*. at 419. "Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *Id*. at 420. In particular, in *KSR*, the Supreme Court emphasized the principle that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id*. at 416. A key inquiry is whether the "improvement is more than the predictable use of prior art elements according to their established functions." *Id*. at 417.

Meta generally contends that the Asserted Claims of the Asserted Patents would have been obvious because they, at most, only slightly modify a known solution to a common issue at the time or merely arrange old elements, with each performing the same function that it had previously been known to perform, and yield no more than what one of ordinary skill would expect from such an arrangement.

In addition to the above obviousness factors, various additional exemplary combinations,

modifications, and reasons or motivations to implement such combinations and modifications are provided below. In addition to the prior art identified herein and in the accompanying charts, prior art not included in this disclosure, whether or not now known to Meta, may become relevant depending on the claim constructions the Court ultimately adopts.

In addition to the prior art references identified below and in the accompanying charts, Meta also relies on relevant portions of the Asserted Patents, the file histories of the Asserted Patents, the Asserted Patents themselves (including the cited references), and other evidence, including fact and expert testimony, to prove that the Asserted Claims are anticipated and/or rendered obvious under 35 U.S.C. §§ 102 and/or 103.

If Gaea challenges a combination of prior art Meta has identified, Meta reserves the right to supplement these Invalidity Contentions to further specify the reason or motivation to combine the prior art in the manner suggested.

D. Exemplary Combinations, Motivations to Combine, and Expectations of Success

For the reasons discussed above, a POSITA would have been motivated to combine any charted reference with any of the other charted references and/or POSITA knowledge. In addition, a POSITA would have been motivated to implement one or more of the following exemplary combinations:

1. Printed Circuit Board and Case

A POSITA would have been motivated to combine any reference with the teachings of one or more of the Micron M600, Samsung PM953S, and Chou references regarding mounting the components of a solid-state storage device on a printed circuit board and enclosing the printed circuit board and components within a case or housing as reflected in the attached charts for claims 3-4 and 11-12 of the ’553 Patent and claim 9 of the ’715 Patent. Those references reflect

conventional physical implementations of solid-state storage devices in which the device electronics are mounted on a printed circuit board and the resulting assembly is contained within a housing.

Implementing the components disclosed by any reference on a printed circuit board would have been a routine and predictable way to mechanically support and electrically interconnect those components in a compact storage device. Likewise, enclosing the resulting printed-circuit-board assembly within a case or housing would have been a routine and predictable way to protect the device components and provide a physically integrated storage device suitable for installation and use with a host system. These modifications concern the conventional physical packaging and interconnection of the disclosed components and would not have altered the operation or function of the underlying storage architecture.

A POSITA therefore would have had reason to implement the teachings of any reference using the conventional printed-circuit-board and housing arrangements taught by the Micron M600, Samsung PM953S, and/or Chou references, with a reasonable expectation of success. The combination would have amounted to the use of known physical packaging techniques for their known purposes and would have yielded the predictable result of the disclosed storage components mounted and interconnected on a printed circuit board within a protective case or housing.

2. **Interface Connector**

A POSITA would have been motivated to combine any reference with the teachings of one or more of the Micron M600, Samsung PM953S, Muhlestein, Seagate Kinetic, Sadovsky, Hashimoto, Chou, Meir, and Salessi references regarding use of an interface connector or communication interface to communicatively couple a storage device and its components to a host computer as reflected in the attached charts for claims 2 and 10 of the ’553 Patent and claim 9 of the ’715 Patent. Those references reflect conventional implementations in which storage devices

communicate with host systems through standardized or otherwise suitable physical interfaces, including SATA, SAS, PCIe, NVMe, Ethernet, USB, SCSI, and other host interfaces.

Implementing the storage architecture disclosed by any reference with such an interface connector or physical host interface would have been a routine and predictable way to provide the mechanical, electrical, and signaling connection necessary for communication between the storage device and a host computer. A POSITA would have understood that the particular physical interface could be selected from known interfaces appropriate for the storage device and host without changing the underlying storage functions performed by the device.

A POSITA therefore would have had reason to implement the teachings of any reference using the interface connector or physical host-interface arrangements taught by the Micron M600, Samsung PM953S, Muhlestein, Seagate Kinetic, Sadovsky, Hashimoto, Chou, Meir, and/or Salessi references, with a reasonable expectation of success. The combination would have amounted to use of known host-interface technology for its known purpose and would have yielded the predictable result of communicatively coupling the disclosed storage components to a host computer.

3. **Programmable Processor**

To the extent required by the language of the Asserted Claims of the ’553 and ’715 Patents, a POSITA would have been motivated to combine any reference with the teachings of one or more of the Willow, Fujibayashi, Muhlestein, Hashimoto, and Meir references regarding use of a separate programmable processor in conjunction with a device controller. Those references reflect known storage architectures in which programmable processing circuitry is used together with control circuitry responsible for managing storage-device operations.

Implementing the functions disclosed by any reference using a programmable processor operatively coupled to a separate device controller would have been a routine and predictable way

to divide functions between programmable processing circuitry and specialized storage-control circuitry. Such an arrangement would permit software or firmware to be executed by the programmable processor while storage-interface, memory-management, data-transfer, or other device-control functions are performed by separate controller circuitry. A POSITA would have understood that allocating the disclosed functions between these known components was an ordinary implementation choice that would not require changing the underlying storage functionality.

A POSITA therefore would have had reason to implement the teachings of any reference using the separate programmable-processor and device-controller architectures taught by the Willow, Fujibayashi, Muhlestein, Hashimoto, and/or Meir references, with a reasonable expectation of success. The combination would have amounted to arranging known processing and control components according to known storage-device architectures and would have yielded the predictable result of a storage system employing both a programmable processor and a separate device controller.

4. **Device Memory**

A POSITA would have been motivated to combine any reference with the teachings of one or more of the Bonnet, Eleftheriou, Flower, Fujibayashi, Yamamoto, Willow, Broadbent, Muhlestein, Micron M600, Samsung PM953S, Hashimoto, Meir, and Salessi references regarding use of device memory associated with a controller or programmable processor as reflected in the attached charts for the Asserted Claims. Those references reflect conventional storage architectures in which local memory, such as RAM, DRAM, SRAM, cache memory, buffer memory, or other working memory, is available to storage-control or processing circuitry of a storage device.

Implementing the storage architecture disclosed by any reference with such device memory

would have been a routine and predictable way to provide temporary or working storage for information used by the controller or processor in performing storage operations. Such memory could be used for instructions, metadata, mapping information, buffers, queues, cached information, intermediate results, or other information used in the course of controlling storage and retrieval operations. Adding such local memory would not have changed the underlying storage functions disclosed by the reference, but instead would have provided a conventional memory resource for carrying out those functions.

A POSITA therefore would have had reason to implement the teachings of any reference using the device-memory arrangements taught by the Bonnet, Eleftheriou, Flower, Fujibayashi, Yamamoto, Willow, Broadbent, Muhlestein, Micron M600, Samsung PM953S, Hashimoto, Meir, and/or Salessi references, with a reasonable expectation of success. The combination would have amounted to use of known local memory for its known purpose in connection with storage-control or processing circuitry and would have yielded the predictable result of a controller or programmable processor having access to device memory while performing the disclosed storage functions.

5. **Policy Availability**

To the extent a reference discloses a storage device policy but not the particular manner in which that policy is made available when a storage request is processed, a POSITA would have had reason to use known techniques for communicating, storing, and accessing such policy information. One conventional approach was to provide the policy, or information identifying the applicable policy, with or in association with the write request. References including Eleftheriou, Sadovsky, Samsung PM953S, Hashimoto, Lovinger, and Olster reflect such techniques. Another conventional approach was to store the policy in device memory and retrieve or access it when processing a subsequent storage request. References including Bonnet, Muhlestein, Micron M600,

and Meir reflect such techniques. A POSITA would have understood that either approach provided a straightforward way to make an already-defined policy available when needed.

Accordingly, a POSITA would have been motivated to implement any disclosed storage device policy using either request-associated policy information or locally stored policy information retrieved or accessed when processing the request, with a reasonable expectation of success. It would have been obvious to do so, either based on POSITA knowledge or through combination with the references identified above.

6. **Recording Method**

A POSITA would have been motivated to combine any reference with the teachings of one or more of Sadovsky, Kubota, Eleftheriou, Flower, Broadbent, Micron M600, Hashimoto, and Davis regarding use or selection of different recording methods for writing content to storage media. Those references reflect known approaches in which content could be written using different storage media, technologies, or write modes, including, for example, SSD versus HDD or tape and SLC, MLC, TLC, or QLC recording.

A POSITA would have understood that these different recording methods involved known tradeoffs in performance, density, endurance, retention, reliability, and cost, and that selecting among them based on the desired treatment of the data was a routine and predictable storage-design choice. Accordingly, to the extent any reference does not expressly disclose the claimed recording method, selecting or implementing an appropriate recording method as part of the storage device policy would have been within the knowledge of a POSITA and, alternatively, would have been obvious based on the teachings of the references discussed above.

7. **Storage Information and Retrieval**

A POSITA would have been motivated to combine any reference with the teachings of one or more of the Bonnet, Eleftheriou, Flower, Yamamoto, Broadbent, Sadovsky, Seagate Kinetic,

Davis, Hashimoto, Meir, and Olster references regarding maintaining information that associates a logical address, object identifier, file identifier, key, or other content identifier with a physical storage location as reflected in the attached charts for the asserted claims of the ’023 Patent. Those references reflect known storage architectures that use mapping tables, translation information, indexes, metadata, lookup structures, or other stored information to determine where identified content is physically stored.

Maintaining such identifier-to-location information would have been a routine and predictable way to permit a storage system to locate data whose physical storage location is different from, or not inherent in, the identifier used by a host or application. A POSITA would have understood that such mapping or location information could be created or updated when content is stored or moved and then maintained in memory or other metadata storage for subsequent use.

A POSITA likewise would have been motivated to use the maintained mapping or location information when processing a request to retrieve previously stored content. The Bonnet, Eleftheriou, Flower, Broadbent, Yamamoto, Seagate Kinetic, Davis, Hashimoto, Meir, and Olster references reflect the known and predictable use of stored mapping, translation, index, or location information to determine the physical location of requested content and retrieve that content from the identified storage location as reflected in the attached charts for the asserted claims of the ’023 Patent. Using the same information that associates an identifier with a physical location to locate the corresponding content in response to a retrieval request would have been a natural and predictable use of that information.

A POSITA therefore would have had reason to implement the teachings of any reference using the mapping and retrieval techniques taught by the Bonnet, Eleftheriou, Flower, Yamamoto,

Broadbent, Sadovsky, Seagate Kinetic, Davis, Hashimoto, Meir, and/or Olster references, with a reasonable expectation of success. The combination would have amounted to using known mapping and lookup techniques for their known purposes and would have yielded the predictable result of maintaining information associating content identifiers with physical storage locations and using that information to locate and retrieve previously stored content.

8. **Solid State Device**

A POSITA would have been motivated to combine any reference with the teachings of one or more of the Bonnet, Eleftheriou, Micron M600, Willow, Samsung PM953S, Hashimoto, Meir, and Salessi references regarding implementation of storage functionality in an SSD or other solid-state storage device having its own internal controller or control circuitry. Those references reflect known self-contained solid-state storage architectures in which solid-state memory and circuitry responsible for controlling operation of that memory are included within the storage device.

Implementing the storage functions disclosed by any reference within such an SSD or solid-state storage device would have been a routine and predictable way to provide those functions using nonvolatile solid-state memory and local device-control circuitry. A POSITA would have understood that storage-management functions can be implemented by controller or processing circuitry located within the solid-state storage device and that incorporating such circuitry with the solid-state memory would permit the device to receive requests or commands and perform the corresponding storage operations internally.

A POSITA therefore would have had reason to implement the teachings of any reference using the self-contained SSD or solid-state-storage-device architectures taught by the Bonnet, Eleftheriou, Micron M600, Willow, Samsung PM953S, Hashimoto, Meir, and/or Salessi references, with a reasonable expectation of success. The combination would have amounted to implementing known storage functionality in a known solid-state storage-device architecture and

would have yielded the predictable result of an SSD or other solid-state storage device containing both solid-state memory and internal controller or control circuitry.

9. SSD Implementations

A POSITA would have been motivated to combine any of Eleftheriou, Broadbent, Flower, Fujibayashi, Muhlestein, Yamamoto, Bonnet, Kubota, or Sadovsky with any of the Willow, Seagate Kinetic, Samsung PM953S, or Micron M600 systems. The patent references principally disclose functional storage architectures and techniques, while the system references provide concrete, known implementations of storage devices and systems on which such functionality could be implemented. A POSITA seeking to implement the teachings of a patent reference would naturally have looked to known storage systems for conventional implementation details, including, as applicable, the arrangement of storage media, controllers, programmable processors, device memory, host interfaces, printed circuit boards, housings, and other hardware and firmware used to carry out storage operations.

The combination would use a known storage-device or storage-system architecture as a practical implementation platform for the functions taught by the patent reference. The particular system architecture could be selected based on ordinary design considerations, including the desired storage medium, interface, form factor, processing architecture, performance, capacity, and deployment environment. Because the system references disclose working implementations of known storage architectures and components performing their established functions, a POSITA would have had a reasonable expectation of successfully implementing the patent reference's teachings using any of those known systems.

The particular teaching supplied by a selected system reference would depend on that system's disclosure; this rationale does not assume that every system reference discloses every implementation feature. Rather, where a system reference supplies a particular feature or

implementation detail missing from or left unspecified by a patent reference, a POSITA would have had reason to use that known feature in implementing the patent reference for the reasons described above and as further detailed below.

Eleftheriou expressly concerns the placement and retrieval of data in a storage architecture that includes solid-state storage and other storage media. A POSITA implementing Eleftheriou would have had reason to combine its teachings with any of the Willow, Seagate Kinetic, Samsung PM953S, or Micron M600 systems because those systems provide known storage-management techniques and storage-device or storage-system architectures suitable for carrying out or supplementing Eleftheriou's teachings. For example, a POSITA would have had reason to employ teachings from those systems concerning controllers, programmable processors, device memory, host interfaces, physical device implementation, data mapping, placement, or retrieval. Such a combination would use known storage techniques and components for their established purposes while preserving Eleftheriou's underlying storage-management functionality.

Broadbent principally concerns management of stored content, including maintaining information identifying stored content and its storage location and using that information in connection with subsequent access to the content. A POSITA implementing Broadbent would have had reason to combine its teachings with any of the Willow, Seagate Kinetic, Samsung PM953S, or Micron M600 systems because those systems provide known architectures and techniques for storing, identifying, managing, and retrieving data. For example, a POSITA would have had reason to employ teachings concerning content identification, mapping, lookup, retrieval, processing, device control, memory, interfaces, or physical implementation. Such a combination would retain Broadbent's content-management and retrieval teachings while using known storage-system techniques and components for their established purposes.

Flower discloses a storage architecture in which a storage controller manages data stored among different storage resources, including solid-state storage. A POSITA implementing Flower would have had reason to combine its teachings with any of the Willow, Seagate Kinetic, Samsung PM953S, or Micron M600 systems because those systems provide known storage-device and storage-system techniques suitable for implementing or supplementing Flower's disclosed architecture. For example, a POSITA would have had reason to use teachings concerning device-level controllers, programmable processing, memory, interfaces, data placement or retrieval, or physical storage-device implementation. Such a combination would provide known techniques and components for carrying out Flower's storage-management functions and would have yielded predictable results.

Fujibayashi discloses an architecture in which processing and control circuitry manage access to solid-state memory. A POSITA would have had reason to combine Fujibayashi with any of the Willow, Seagate Kinetic, Samsung PM953S, or Micron M600 systems because those systems provide known implementations and techniques concerning programmable processing, storage control, memory, host interfaces, data management, and physical storage-device architecture. For example, a POSITA would have had reason to employ teachings from those systems concerning processors, controllers, memory, interfaces, mapping, retrieval, or physical implementation in carrying out Fujibayashi's disclosed storage operations. Such a combination would use known storage-system components and techniques according to their established functions and would have produced predictable results.

Muhlestein discloses a storage system employing processing, memory, storage-control, and host-communication functionality. A POSITA implementing Muhlestein would have had reason to combine its teachings with any of the Willow, Seagate Kinetic, Samsung PM953S, or

Micron M600 systems because those systems provide known storage-management techniques and concrete implementations of storage devices, processing circuitry, memory, interfaces, firmware, and related components. For example, a POSITA would have had reason to employ teachings concerning programmable processing, device control, local memory, host interfaces, storage-device architecture, or physical implementation. Incorporating such known teachings would supplement Muhlestein's storage-system functionality using conventional storage technologies with a reasonable expectation of success.

Yamamoto discloses a storage apparatus that manages data among storage resources, including solid-state storage devices. A POSITA implementing Yamamoto would have had reason to combine its teachings with any of the Willow, Seagate Kinetic, Samsung PM953S, or Micron M600 systems because those systems provide known techniques and architectures for implementing storage devices and managing stored data. For example, a POSITA would have had reason to employ teachings concerning storage placement, mapping, retrieval, device control, programmable processing, memory, host interfaces, or physical storage-device implementation. Such a combination would use known storage technologies for their established purposes while preserving Yamamoto's underlying storage-management functionality.

Bonnet expressly concerns a solid-state storage device and the control of storage operations within that device. A POSITA implementing Bonnet would have had reason to combine its teachings with any of the Willow, Seagate Kinetic, Samsung PM953S, or Micron M600 systems because those systems provide known storage-management techniques and storage architectures suitable for implementing or supplementing Bonnet's solid-state storage functionality. For example, a POSITA would have had reason to employ teachings concerning programmable processing, device control, memory, host interfaces, data placement or retrieval, firmware, or

physical device implementation. Such a combination would implement or supplement Bonnet's disclosed storage functions using known storage-system techniques and components and would have yielded predictable results.

Kubota discloses a storage architecture in which a controller manages the placement of data among different storage resources, including solid-state and other storage. A POSITA implementing Kubota would have had reason to combine its teachings with any of the Willow, Seagate Kinetic, Samsung PM953S, or Micron M600 systems because those systems provide known techniques and architectures for implementing storage resources and managing data within them. For example, a POSITA would have had reason to employ teachings concerning data placement, storage-device control, programmable processing, memory, interfaces, solid-state storage, or physical device implementation. Such a combination would provide conventional techniques and components for implementing or supplementing Kubota's storage-management teachings and would have had a reasonable expectation of success.

Sadovsky discloses storage-management functionality in which information associated with data is used to influence how data is handled and stored within a storage subsystem, including implementations involving solid-state storage. A POSITA implementing Sadovsky would have had reason to combine its teachings with any of the Willow, Seagate Kinetic, Samsung PM953S, or Micron M600 systems because those systems provide known storage-management techniques and storage architectures suitable for implementing or supplementing Sadovsky's teachings. For example, a POSITA would have had reason to employ teachings concerning data placement, mapping, retrieval, processing, device control, memory, host interfaces, firmware, or physical implementation. Such a combination would use known storage technology for its established purposes, would not require changing Sadovsky's principle of operation, and would have yielded

predictable results with a reasonable expectation of success.

10. Miscellaneous Combinations

Olster and Davis. A POSITA would have been motivated to combine Olster and Davis because both concern policy-based data storage systems using solid-state memory, and Davis provides more detailed data-placement policies for implementing and improving the type of replication and placement policy contemplated by Olster. For example, a POSITA could incorporate Davis's teachings regarding selection among different types of flash memory based on the characteristics or type of the data into Olster's configurable storage policy. Doing so would allow the system to better exploit known tradeoffs among storage density, cost, error rates, reliability, retention, and wear, thereby improving reliability and permitting different types of data to be prioritized appropriately. Because both references use controllers and software to apply storage policies to flash memory, the combination would have involved a routine modification of the applicable policy or programming, rather than a fundamental change to the storage architecture, and a POSITA would have had a reasonable expectation of success.

Meir and Salessi. A POSITA would have been motivated to combine Meir and Salessi because both concern SSDs and complementary techniques for processing and storing data. Meir already teaches a configurable storage policy, including policies implementing redundancy schemes such as RAID, while Salessi teaches processing algorithms including compression, decompression, encryption, and decryption and expressly contemplates using such processing in connection with RAID. For example, a POSITA could incorporate Salessi's processing algorithms into Meir's configurable policy and software so that selected content is compressed or encrypted before storage and decompressed or decrypted upon retrieval. The combination would improve performance and security, increase effective storage capacity and conserve resources through compression, reduce NAND wear by reducing the amount of data written, and facilitate protection

of sensitive information through encryption. Because the systems employ similar SSD architectures and Meir expressly contemplates configurable policy rules, implementing Salessi's algorithms would have amounted to a straightforward programming modification with a reasonable expectation of success.

Meir + Salessi + Chou. A POSITA would have been motivated to further combine the Meir-Salessi system with Chou's teachings concerning the physical implementation of an SSD on a printed circuit board within a case. For example, the relevant solid-state memory, processor, memory, controller, interface, and associated connections could be mounted on a printed circuit board supported by a case as taught by Chou. This conventional physical arrangement would improve system performance by reducing interference from nearby signals and thus reducing errors and retransmissions, while the case would protect the internal components from environmental conditions, improve resiliency, and extend component life. Meir and Chou both concern SSDs having controllers and solid-state memory, and the use of PCBs and cases was a common design option for providing hardware stability and protection; Salessi's data-processing teachings do not conflict with that physical implementation.

Meir, Salessi, and Lovinger. A POSITA would have been motivated to further combine Meir-Salessi with Lovinger by permitting the host to provide a storage policy together with the content in a storage request. This approach is a natural extension of Meir's goal of making storage policies configurable and would allow the host to select or configure the applicable policy as part of the particular request, without reprogramming device firmware or, for example, requiring a separate prior policy-setting operation. It would also provide greater flexibility in selecting the compression, encryption, or other processing to be applied to particular content under Salessi's processing teachings. Including policy information in a write request was also a known design

option by the relevant time. Because Meir, Salessi, and Lovinger employ similar storage-system structures, the modification would principally change the information conveyed and the storage-request flow rather than require a new storage architecture, and a POSITA would have had a reasonable expectation of success.

Meir, Salessi, Lovinger, and Chou. A POSITA would have been motivated to combine all four references for the same complementary reasons supporting the foregoing combinations. For example, Meir could provide the configurable SSD architecture and policy framework, Salessi could provide additional policy-based data-processing techniques such as compression and encryption, Lovinger could provide a storage-request mechanism in which policy information accompanies the content, and Chou could provide the conventional PCB-and-case implementation for the SSD hardware. Lovinger's modification to the software and storage-request flow would not affect the PCB-and-case hardware implementation taught by Chou, and a storage system incorporating Lovinger's request-flow teachings would likewise benefit from the stability and protection provided by Chou's physical arrangement. The references therefore could be combined without requiring incompatible changes to the system architecture and with a reasonable expectation of success.

E. Secondary Considerations

Subject to the reservation of rights stated above, Gaea has not established the existence of any secondary considerations. Meta reserves the right to supplement these Invalidity Contentions with respect to secondary considerations should Gaea adequately identify such secondary considerations and/or their alleged nexus to the Asserted Claims.

"The fact of near-simultaneous invention, though not determinative of statutory obviousness, is strong evidence of what constitutes the level of ordinary skill in the art." *Ecolochem, Inc. v. S. Cal. Edison Co.*, 227 F.3d 1361, 1379 (Fed. Cir. 2000) (quoting *Int'l Glass*

Co. v. United States, 408 F.2d 395, 405 (Ct. Cl. 1969)). "[T]he possibility of near simultaneous invention by two or more equally talented inventors working independently, . . . may . . . be an indication of obviousness when considered in light of all the circumstances." *Id.* (quoting *Lindemann Maschinenfabrik GmbH v. Am. Hoist & Derrick Co.*, 730 F.2d 1452, 1460 (Fed. Cir. 1984)); *see also Geo. M. Martin Co. v. All. Mach. Sys. Int'l LLC*, 618 F.3d 1294, 1305 (Fed. Cir. 2010) ("Independently made, simultaneous inventions, made 'within a comparatively short space of time,' are persuasive evidence that the claimed apparatus 'was the product only of ordinary mechanical or engineering skill.'" (citation omitted)). If any of the references in these Invalidity Contentions is found not to be prior art to the Asserted Patents, these references may be relied upon as evidence of near-simultaneous invention favoring obviousness.

Regardless, Meta is not aware of any evidence that: (1) Gaea developed a product embodying the claimed subject matter of the Asserted Claims that has enjoyed commercial success; (2) the Asserted Claims are directed to any long felt but unresolved need; (3) the Asserted Claims address any failure of others; (4) there is teaching away from the claimed subject matter by the prior art; (5) the claimed subject matter of the Asserted Claims has been copied or acclaimed by others; or (6) experts would have been skeptical of the claimed approach or idea set forth in the Asserted Claims. Nor is Meta aware of any evidence that there is a nexus between any such secondary consideration and the Asserted Claims.

F. Grounds of Invalidity Other Than Anticipation or Obviousness

The Asserted Claims are also invalid for failure to meet one or more of the requirements of 35 U.S.C. § 112.

Meta reserves the right to amend, supplement, and/or otherwise modify these Invalidity Contentions with respect to grounds of invalidity other than anticipation or obviousness. Due in part to Gaea's failure to sufficiently identify (a) the full scope of the accused instrumentalities and

(b) where Gaea contends that each element of the Asserted Claims is found within each accused instrumentality, Meta lacks a complete understanding of Gaea's alleged infringement and/or claim construction positions. If and when Gaea develops an infringement and/or claim construction theory that implicates infringement by Meta, Meta reserves the right to argue that the specification does not enable and/or provide a written description for such an interpretation. The Court has not yet construed any terms, phrases, or clauses of the Asserted Claims, and Gaea has not yet provided any validity contentions in response to Meta's Invalidity Contentions. In particular, Gaea has not identified any way in which it disputes that the Asserted Claims are invalid under 35 U.S.C. § 112. Moreover, Meta's discovery and investigation in connection with this lawsuit is ongoing, and these grounds are based on information obtained to date. Accordingly, Meta reserves the right to amend, supplement, and/or otherwise modify these Invalidity Contentions. Meta further reserves the right to rely on expert reports or testimony and any third-party discovery.

Meta lists below exemplary grounds upon which Meta presently contends the Asserted Claims are invalid for failure to meet one or more of the requirements of 35 U.S.C. § 112. These grounds are identified based on knowledge currently in Meta's possession. A more detailed basis will be set forth in Meta's claim construction briefs and expert reports on invalidity, to be served in accordance with the Scheduling Order. Further investigation may uncover additional grounds for invalidity, and Meta reserves the right to supplement these disclosures to include all additional grounds.

1. **Invalidity Under 35 U.S.C. § 112 (Written Description/Enablement)**

Pursuant to 35 U.S.C. § 112(a), a patent specification:

> "shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly

connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention."

The Federal Circuit has held that this language creates two closely related, yet separate requirements for a specification: (i) a written description of the invention ("written description"), and (ii) a written description of the manner and process of making and using the invention ("enablement"). *See Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1344 (Fed. Cir. 2010) (*en banc*).

The test for sufficiency of a patent's written description requires:

"an objective inquiry into the four corners of the specification from the person of ordinary skill in the art. Based on that inquiry, the specification must describe an invention understandable to that skilled artisan and show that the inventor actually invented the invention claimed."

Ariad, 598 F.3d at 1351. A patent is invalid for inadequate written description unless "the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Id*.

The enablement requirement mandates that the disclosure in the specification describe "the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the [invention]." 35 U.S.C. § 112(a). For a patent's specification to be enabling, it "must teach those skilled in the art how to make and use the full scope of the claimed invention without 'undue experimentation.'" *ALZA Corp. v. Andrx Pharms., LLC*, 603 F.3d 935, 940 (Fed. Cir. 2010) (quoting *Genentech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361, 1365 (Fed. Cir. 1997)).

Below is an exemplary list of claim elements[1] for which there is inadequate written description and/or lack of enablement under 35 U.S.C. § 112(a). For example, certain claim limitations fail to describe an invention understandable to a skilled artisan at the time of the invention and/or fail to show that the inventor actually possessed the invention claimed. *See Ariad*, 598 F.3d at 1351. As a further example, certain claims are invalid because the specification fails to teach those skilled in the art at the time of the alleged invention how to make and use the full scope of the claimed invention without undue experimentation. *See ALZA*, 603 F.3d at 940. As an additional example, certain claim limitations encompass any and all structures or acts for performing a recited function, including those beyond what the applicant(s) invented, such that the specification fails to provide a scope of enablement commensurate with the scope of the claim as asserted. *See Halliburton Oil Well Cementing Co. v. Walker*, 329 U.S. 1, 12–13 (1946). As yet another example, certain claims are invalid for failing to enable the full scope of the invention as defined by the claims. *See Amgen Inc. v. Sanofi,* 598 U.S. 594, 610 (2023*)* ("If a patent claims an entire class of processes, machines, manufactures, or compositions of matter, the patent's specification must enable a person skilled in the art to make and use the entire class.").

In addition, and without limitation, the Asserted Claims taken as a whole (rather than only as the sum of their individual limitations) are invalid for lack of written description and enablement. *See*, *e.g.*, *Novozymes A/S v. DuPont Nutrition Biosciences APS*, 723 F.3d 1336, 1346–51 (Fed. Cir. 2013). As described below, by way of example, a person of ordinary skill in the art

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[1] Any discrepancy between the language included in the bullets of this paragraph and the language of the corresponding claim element is inadvertent, and it is Meta's contention that the claim element is not adequately described and/or enabled under 35 U.S.C. § 112(a).

at the time of the alleged invention would not understand that the named inventors of the Asserted Patents were in possession of the claimed subject matter as of the effective filing date, nor would the patent's disclosure have enabled one skilled in the art at the time of the alleged invention to practice the Asserted Claims without undue experimentation.

Any deficiencies that render claims invalid for written description and/or enablement under 35 U.S.C. § 112 also infect and thereby invalidate any and all claims depending therefrom.

In addition to the claim as a whole, at least the following claim elements, or portions thereof, of the claims in the Asserted Patents are not supported by the written description and/or are not enabled under 35 U.S.C. § 112(a).

- Claims 1 and 9 of the '023 Patent, and any claims dependent therefrom are invalid for failure to satisfy the requirements of 35 U.S.C. § 112(a) because the specification as filed does not contain an adequate written description of a host, wherein a device controller is configured to "receive, from a host, at least one storage device policy." A POSITA would not have understood the inventors to possess the full scope of the claim because the as-filed specification does not describe a host as recited.
- Claims 1 and 9 of the '553 Patent, claim 1 of the '715 Patent, and any claims dependent therefrom are invalid for failure to satisfy the requirements of 35 U.S.C. § 112(a) because the specification as filed does not contain an adequate written description of a device memory directed to, "a programmable processor operatively coupled to the device memory." A POSITA would not have understood the inventors to possess the full scope of the claim because the as-filed specification does not describe a device memory as recited.

- Claims 1 and 9 of the ’553 Patent, claim 1 of the ’715 Patent, and any claims dependent therefrom are invalid for failure to satisfy the requirements of 35 U.S.C. § 112(a) because the specification as filed does not contain an adequate written description of a programmable processor directed to, “process the content for storage based on the storage device policy” nor “transfer the content to the device controller.” A POSITA would not have understood the inventors to possess the full scope of the claim because the as-filed specification does not describe a programmable processor as recited.
- Claims 1 and 9 of the ’553 Patent, claim 1 of the ’715 Patent, and any claims dependent therefrom are invalid for failure to satisfy the requirements of 35 U.S.C. § 112(a) because the specification as filed does not contain an adequate written description of a device controller directed to “receive the content from the programmable processor.” A POSITA would not have understood the inventors to possess the full scope of the claim because the as-filed specification does not describe a device controller directed to perform that task.
- Claim 1 of the ’553 Patent and any claims dependent therefrom are invalid for failure to satisfy the requirements of 35 U.S.C. § 112(a) because the specification as filed does not contain an adequate written description of a programmable processor directed to, “in response to receiving a storage request comprising content, retrieve a storage device policy from the device memory.” A POSITA would not have understood the inventors to possess the full scope of the claim because the as-filed specification does not describe a processor directed to perform that task.

- Claims 2 and 10 of the ’553 Patent and any claims dependent therefrom are invalid for failure to satisfy the requirements of 35 U.S.C. § 112(a) because the specification as filed does not contain an adequate written description of an interface connector which “communicatively couples the solid-state memory, the device controller, the programmable processor, and the device memory to a host computer.” A POSITA would not have understood the inventors to possess the full scope of the claim because the as-filed specification does not describe an interface connector directed to perform that task.
- Claim 9 of the ’553 Patent and any claims dependent therefrom are invalid for failure to satisfy the requirements of 35 U.S.C. § 112(a) because the specification as filed does not contain an adequate written description of a programmable processor directed to, “receive a storage request comprising content and a storage device policy.” A POSITA would not have understood the inventors to possess the full scope of the claim because the as-filed specification does not describe a programmable processor directed to perform that task.
- Claim 9 of the ’715 Patent and any claims dependent therefrom are invalid for failure to satisfy the requirements of 35 U.S.C. § 112(a) because the specification as filed does not contain an adequate written description of “a data link to communicatively couple the programmable processor and the device controller” that is mounted on a printed circuit board. The as-filed specification does not disclose a physical data link between a programmable processor and the device controller.
- Claims 1 and 9 of the ’553 Patent, claim 1 of the ’715 Patent, and any claims

dependent therefrom are invalid for failure to satisfy the requirements of 35 U.S.C. § 112(a) because the specification as filed does not contain an adequate written description of "a programmable processor" operatively coupled to both the device memory and a device controller, and "an application stored on the device memory and comprising instructions that, when executed by the programmable processor, direct the programmable processor" to perform the recited operations. This configuration is not described, such that a POSITA would not have understood the inventors to possess the full scope of the claims.

- To the extent Gaea contends that FDP is a storage policy and/or recording method, Claims 1 and 9 of the '023 Patent and any claims dependent therefrom are invalid for failure to satisfy the requirements of 35 U.S.C. § 112(a) because the specification as filed does not contain an adequate written description of a "storage policy" or "recording method for writing content to the storage media" that includes data placement.

These elements fail to meet the written description requirement and/or are not enabled. The Asserted Patents would not convey to one of skill in the art that, as of the filing dates, the inventors had possession of the claimed subject matter. Nor would the Asserted Patents teach one of ordinary skill in the art how to practice these claim elements without undue experimentation. To the contrary, the Asserted Patents recite only generic components in the embodiments disclosed. Additionally, the claims containing these limitations are invalid for failing to enable the full scope of the invention as defined by the claim.

III. Subject Matter Eligibility Contentions

Pursuant to Third Amended Miscellaneous Order No. 62 (N.D. Tex. Apr. 23, 2026), Meta provides the following identification of asserted claims that are directed to ineligible subject matter

under 35 U.S.C. § 101.

- Claims 1, 9, and 14 of the ’023 Patent;
- Claims 1-4 and 9-12 of the ’553 Patent;
- Claims 1 and 9 of the ’715 Patent.

In sum, these claims are directed to the abstract idea of storing content according to a policy. The claims recite that function largely in results-oriented terms—e.g., processing content “based on” a storage device policy or storing content using a “recording method” indicated by the storage device policy—without requiring any particular algorithm, data structure, storage-management technique, or other specific technological mechanism for accomplishing those results.

The additional limitations do not supply an inventive concept. Rather, they recite implementing the storage device policy and subsequent data retrieval using conventional computer and storage components performing their ordinary functions, including solid-state memory, device memory, device controllers, programmable processors, interface connectors, printed circuit boards, and cases. The recitation of such generic physical components does not transform an otherwise abstract, functionally-claimed process into patent-eligible subject matter.

IV. Accompanying Document Production

A. Production Pursuant to Paragraph 3-4(a)

Pursuant to Paragraph 3-4(a) of Miscellaneous Order No. 62, Meta hereby produces for inspection (in the case of source code) and review (in the case of non-source code documents), pursuant to the procedures of the Stipulated Protective Order (Dkt. No. 56), source code and other documentation sufficient to show the operation of the aspects and elements of the accused instrumentalities identified in Gaea’s Paragraph 3-1 charts. Such source code has been designated HIGHLY CONFIDENTIAL – SOURCE CODE and will be made available for

inspection on a secured computer at the offices of Morrison & Foerster LLP, 425 Market Street, San Francisco, California 94105, upon no less than five business days' advance notice.

B. Production Pursuant to Paragraph 3-4(b)

Pursuant to Paragraph 3-4(b) of Miscellaneous Order No. 62, Meta is producing, alongside its Invalidity Contentions, the known invalidating references referred to herein and in the accompanying claim charts. For any such item that is not in English, an English translation of the portion(s) relied upon has been or will be produced.

Dated: September 11, 2026

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that on September 11, 2026, a true and correct copy of the foregoing was served via email on all counsel of record.

/s/ Hannah Jiam
Hannah Jiam