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UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

GAEA, LLC, Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD. and SAMSUNG ELECTRONICS AMERICA, INC. Defendants.	Civil Action No. 2:26-cv-00264-JRG-RSP **DEMAND FOR JURY TRIAL**

DEFENDANTS' P.R. 3-3 AND 3-4 DISCLOSURES

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I. INTRODUCTION

Pursuant to P.R. 3-3 and 3-4 and the Docket Control Order (Dkt. No. 24), Defendants Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. ("Defendants") hereby disclose their P.R. 3-3 and 3-4 disclosures ("Invalidity Contentions") in view of Plaintiff Gaea, LLC's ("Gaea") Disclosure of Asserted Claims and Infringement Contentions ("Infringement Contentions"). In the event Gaea amends its Infringement Contentions, these Invalidity Contentions may change and Defendants reserve the right to amend or supplement these Invalidity Contentions. Defendants contend that each of Gaea's Asserted Claims (as defined below) is invalid under at least 35 U.S.C. §§ 101, 102, 103, and/or 112(a).

A. Asserted Claims

In its Infringement Contentions, Gaea asserts infringement of the following patents and claims (collectively, the "Asserted Patents" and "Asserted Claims"):

- Claims 1, 9, and 14 of U.S. Patent No. 10,776,023 ("the '023 patent")
- Claims 1-4 and 9-12 of U.S. Patent No. 11,907,553 ("the '553 patent");
- Claims 1 and 9 of U.S. Patent No. 12,265,715 ("the '715 patent");

These Invalidity Contentions address the Asserted Claims specifically set forth in Gaea's Infringement Contentions against Defendants. To the extent Gaea attempts to assert infringement of any other patents or claims, and if the Court grants Gaea leave to do so, Defendants reserve the right to revise, amend, correct, supplement, modify, or clarify these Invalidity Contentions.

B. Ongoing Discovery and Disclosures

Defendants base these Invalidity Contentions on their current knowledge and understanding of the Asserted Claims and review of prior art items as of the date of these Invalidity Contentions. These Invalidity Contentions are made without the benefit of discovery

regarding the parties' claim construction contentions, any expert discovery, any third-party discovery, and any claim construction opinion or order by the Court. Accordingly, these Invalidity Contentions are provided without prejudice to Defendants' right to revise, amend, correct, supplement, modify, or clarify these Invalidity Contentions. Defendants reserve the right to complete their investigation and discovery of the facts, to produce subsequently discovered information, and to introduce such subsequently discovered information at the time of any hearing or trial in this action.

Defendants incorporate by reference all other bases for invalidity identified in their Answers, Initial Disclosures, and interrogatory responses in this matter, and during the prosecution of the Asserted Patents and all related patents and/or patent applications. Defendants further incorporate by reference all admissions regarding the Asserted Patents including, but not limited to, admissions in the specifications of the Asserted Patents, and the prosecution of the Asserted Patents and related patents and/or patent applications.

C. Related Actions

On August 5, 2026, Samsung Electronics Co., Ltd. and Meta Platforms, Inc. jointly filed petitions for *inter partes* review (IPR) challenging the following claims of the Asserted Patents:

- **IPR2026-00425:** Claims 1, 2, 7, 9, 14-20, 32, 34, and 36 of the '023 patent;
- **IPR2026-00426:** Claims 1-7, 9-20, and 26-31 of the '553 patent; and
- **IPR2026-00427:** Claims 1, 2, 5-11, and 14-20 of the '715 patent.

In the event the Patent Trial and Appeal Board (PTAB) institutes review in any of the foregoing proceedings, Defendants expressly disclaim for purposes of this district-court litigation reliance on the prior art references asserted in that proceeding with respect to the Asserted Patent challenged therein.

Defendants specifically stipulate as follows with respect to each of the foregoing IPR proceedings: if the PTAB institutes IPR in that proceeding, then Defendants (i) will not pursue in this litigation the specific grounds of invalidity that were raised or grounds that reasonably could have been raised under 35 U.S.C. §§ 102 or 103 on the basis of prior art patents or printed publications in that proceeding, and (ii) will not pursue in this litigation grounds of invalidity with respect to the Asserted Patent challenged in that proceeding under 35 U.S.C. §§ 102 or 103 that cite to any of the prior art references listed in the grounds for that proceeding, including in combination with any other prior art that could not have been raised in the IPR (*e.g.*, system art) for grounds of invalidity under 35 U.S.C. § 103. To avoid any doubt, if the PTAB declines institution or rescinds institution in any of the foregoing proceedings, then Defendants reserve the right to pursue any grounds of invalidity with respect to that proceeding's Asserted Patent, including but not limited to the grounds in (i) and (ii), in this litigation.

D. Claim Construction

The Court has not construed the Asserted Claims. Defendants reserve the right to amend these Invalidity Contentions after the Asserted Claims are construed by the Court. Depending on positions that Gaea or its expert witness(es) may take concerning infringement and/or invalidity issues, the asserted prior art references may be of greater or lesser relevance. Given this uncertainty, the charts may reflect alternative applications of the prior art against the Asserted Claims. Thus, no chart or position taken by Defendants should be construed as an admission or suggestion that any Accused Instrumentality satisfies the limitations of the Asserted Claims or waiver of any kind.

E. Effective Date

Gaea asserts the following under P.R. 3-1(e):

Asserted Patent	Claimed Priority Date
The '023 Patent	November 7, 2016
The '553 Patent	November 7, 2016
The '715 Patent	November 7, 2016

Defendants do not concede that any of the Asserted Claims of the Asserted Patents are entitled to Gaea's purported priority dates. Defendants have relied on Gaea's disclosures in making these Invalidity Contentions. To the extent Gaea seeks and is granted leave to amend its disclosures in an attempt to establish any earlier effective date(s), Defendants reserve the right to amend these Invalidity Contentions in response, including by disclosing additional prior art or earlier versions or evidence of the prior art disclosed herein.

F. Prior Art Identification and Citation

The accompanying invalidity claim charts cite to particular teachings and disclosures of the prior art references as applied to features of the Asserted Claims. However, a person of ordinary skill in the art ("POSITA") may view an item of prior art generally in the context of other publications, literature, products, and understanding. Accordingly, the cited portions are only exemplary and are intended to put Gaea on notice of the basis for Defendants' contentions. Defendants have attempted to identify the most relevant portions of the references, but the references may contain additional support for particular claim limitations. Defendants reserve the right to rely on uncited portions of the prior art references, other documents, and/or prior art products, as well as fact and expert testimony, to provide context or to aid in understanding the cited portions of the references and interpreting the teachings of the prior art and to establish

bases for combinations of certain cited references that render the Asserted Claims obvious. Defendants reserve the right to rely on any prior art product referenced, embodied, or described in any of the prior art references identified herein, or which embodies any of the prior art references identified herein. Moreover, Defendants reserve the right to rely on inventor admissions concerning the scope of the prior art relevant to the Asserted Patents found in, *inter alia*, the prosecution histories of the Asserted Patents and related patents and/or patent applications, any testimony or declarations of the named inventors concerning the Asserted Patents or related patents, and any papers or evidence submitted by Gaea in connection with this litigation or any other pending or future litigation brought by Gaea involving the Asserted Patents or related patents. Defendants also may establish what was known to a POSITA through treatises, published industry standards, other publications, products, and/or testimony.

Where the invalidity claim charts cite to a particular figure or table in a reference, the citation should be understood to encompass the caption of the figure or table and other text relating to and/or describing the figure or table. Similarly, where the invalidity claim charts cite to particular text referring to a figure or table, the citation should be understood to include the figure and related figures or tables as well.

The prior art references listed herein and in the accompanying claim charts may disclose the elements of the Asserted Claims explicitly and/or inherently. The prior art references are also relevant for their showing of the state of the art and reasons and motivations for making improvements, additions, and combinations. The suggested obviousness combinations are provided in the alternative to Defendants' anticipation contentions and are not to be construed to suggest that any reference is not itself anticipatory.

Further, the combinations of prior art references contained herein demonstrating the obviousness of the Asserted Patents under 35 U.S.C. § 103 are merely exemplary and are not intended to be exhaustive. All such combinations are intended to include and be in view of the knowledge of a POSITA. Additional obviousness combinations of the identified prior art references are possible, and Defendants reserve the right to use any such combination(s) in this Action. In particular, Defendants are currently unaware of the extent, if any, to which Gaea will contend that limitations of any particular claim(s) are not disclosed in the art that Defendants have identified as anticipatory. To the extent that Gaea does so, Defendants reserve the right to identify other evidence or references that anticipate or render obvious the particular claim(s).

Nothing in these Invalidity Contentions should be treated as an admission that any of the Accused Instrumentalities meet any limitation of the Asserted Claims. Defendants deny infringing the Asserted Claims.

G. Additional Reservation of Rights

Defendants reserve all rights to further supplement or modify these Invalidity Contentions, including the prior art disclosed and stated grounds of invalidity. In addition, Defendants reserve the right to prove invalidity of the Asserted Claims on bases other than those required to be disclosed in these disclosures and contentions pursuant to P.R. 3-3.

Defendants' identification in the prior art of claim elements recited in the preamble of any claims is not intended to indicate that any such preamble is limiting. All such disclosures are made only to the extent the preamble is determined to be limiting.

As described above, Defendants also intend to diligently seek discovery from third parties to demonstrate the inventions were in public use, on sale, or otherwise available to the public under 35 U.S.C. § 102(a). Defendants may therefore modify, amend, and/or supplement these Invalidity Contentions if and when further information becomes available.

II. BACKGROUND AND STATE OF THE ART

Set forth below is a summary of the state of the art as understood as of the asserted priority date of the Asserted Patents for the general subject matter of each of the Asserted Patents. The information discussed in this section would have formed the background knowledge of a POSITA at the time the Asserted Patents were filed and would have been used in determining whether and how to combine references to achieve the claimed inventions. *See Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013) (stating that "the knowledge [of a person of ordinary skill in the art] is part of the store of public knowledge that must be consulted when considering whether a claimed invention would have been obvious"). Defendants expressly reserve the right to rely on each of the prior art references, systems, concepts, and technologies discussed in this section with respect to each of the Asserted Patents.

A. The Asserted Patents

The Asserted Patents are members of the same patent family and share a common specification. The '023 patent, the earliest-filed patent of the family, was filed on November 6, 2017. The '553 and '715 patents are continuations of the '023 patent, filed on April 8, 2022 and January 10, 2024, respectively. All three patents claim priority to provisional applications filed on November 7, 2016. Gaea contends that the asserted claims of each of the Asserted Patents are entitled to a priority date of "at least November 7, 2016." Infringement Contentions at 3-4.

The '553 and '715 patents claim apparatuses comprising conventional components (solid-state memory, device memory, a programmable processor, and a device controller) in which an application directs a programmable processor to "process content for storage based on [a] storage device policy" and transfer the content to the device controller for storage on solid-state memory. *See* '553 patent at cls. 1, 9; '715 patent at cl. 1. The claims do not set forth any particular type of processing, algorithm, or data-transformation method. The claims also do not set forth any

particular "storage device policy" or any particular technological mechanism for accomplishing the processing. The '553 and '715 patents thus describe a functional processing-then-storing objective performed by conventional solid-state drive (SSD) hardware, without claiming a particular storage technique or technological improvement.

The '023 patent is directed to a related but distinct concept: receiving a "storage device policy" from a host that indicates a "recording method for writing content to the storage media," storing content using that method, recording "storage information" including a content identifier, and later using that information to retrieve the content. *See* '023 patent at cls. 1, 9. The '023 patent does not set forth any particular "storage device policy," "recording method," "content identifier," or manner of retrieving content. Its independent claims use the broader term "storage media" rather than requiring solid-state memory.

Gaea's Infringement Contentions seek to cover Flexible Data Placement (FDP) functionality (*see, e.g.*, Dkt. No. 36 at 8; Infringement Contentions at 2), which is a mechanism in use for addressing the write amplification problem, a fundamental challenge inherent to NAND flash memory such as that used in the accused SSD products. As described below, however, the prior art's extensive body of work addressing this problem long predated the Asserted Patents' purported November 7, 2016 priority date.

B. Write Amplification Was a Known Problem

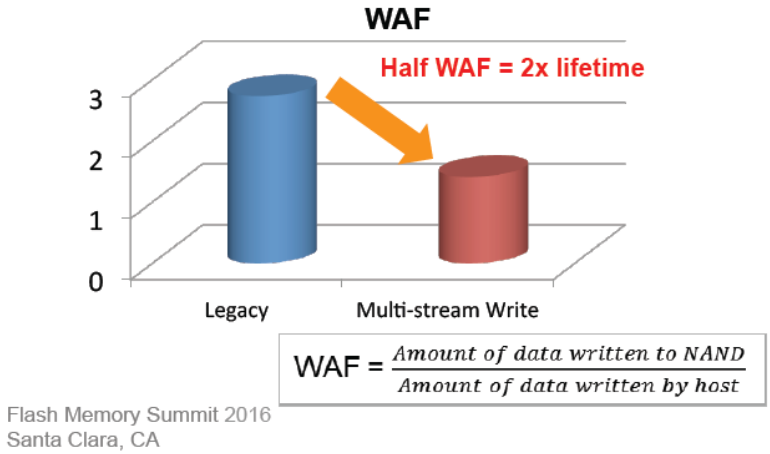
NAND flash memory cannot overwrite data in place. *See*, *e.g.*, U.S. Patent App. Pub. No. 2012/0166749 (Eleftheriou), ¶[0005]. When data is updated, the new version must be written to a free page while the previously occupied page is marked invalid. *Id.* To reclaim space consumed by invalidated pages, the device's internal garbage-collection process selects an occupied block, copies all still-valid pages to another location, and erases the original block. *Id.* These internal operations cause the total volume of data physically written to the NAND medium to exceed the

volume of data written by the host, which is a phenomenon known as write amplification. *Id.* ¶[0008]. The write amplification factor ("WAF") is defined as the ratio of total data written to the SSD to the total data written by the host:

> The write amplification (WA) is defined as follows:
>
> WA=(Total amount of data written to SSD)/(Total amount of data written to SSD from host)

U.S. Patent No. 9,830,079 (Kanno) (SAMSUNG-GAEA_00003324), 6:22-29.

The storage industry uniformly recognized write amplification as a critical limitation. For example, IBM characterized it as "one of the most critical issues limiting the random write performance and write endurance lifespan in Solid-state storage devices." Eleftheriou, ¶[0008]. Toshiba noted that, because higher WAF increases program/erase cycles per physical block, it directly accelerates endurance degradation. Kanno, 6:30-36. Samsung itself documented the problem: "[W]rite amplification decreases SSD lifetime because each NAND chip can endure a certain number of writes before it begins to fail." Samsung, "Multi-Stream SSD Technology" (2015) (SAMSUNG-GAEA_00004625). Samsung's Changho Choi confirmed the relationship quantitatively ("Half WAF = 2x lifetime"):



Choi, "Multi-Stream Write SSD," Flash Memory Summit 2016 (SAMSUNG-GAEA_00004394).

The academic community likewise documented this problem. For example, Lu et al. identified file-system mechanisms that exacerbate flash write amplification, including journaling, synchronous metadata writes, and page-aligned updates. Lu et al., "Extending the Lifetime of Flash-based Storage through Reducing Write Amplification from File Systems," FAST '13, § 1 (SAMSUNG-GAEA_00004609). Likewise, Lee et al. empirically demonstrated that "higher file system utilization leads to larger WAF and reduced performance." Lee et al., "F2FS: A New File System for Flash Storage," FAST '15, § 3.2.4 (SAMSUNG-GAEA_00004577). Specifically, "[a]s [the authors] raised utilization level from 80% to 97.5%, the amount of GC increased and the performance degradation became more visible." *Id.* Examining the problem from the perspective of SSD firmware, Zhang et al. confirmed that garbage-collection cost increases with larger random-write working sets: "[W]hen random writes are performed over a large working set, garbage collection has a higher cost since blocks contain more live data, which must be rewritten before erasing a block." Zhang et al., "De-indirection for flash-based SSDs with Nameless Writes," FAST '12, §§ 3, 6.4 (SAMSUNG-GAEA_5702).

C. Continued Scaling Made the Write Amplification Problem Worse

As flash storage scaled to meet growing capacity demands, the very techniques that increased density also made write amplification a more acute problem. Each successive generation of flash required new device physics, firmware, and storage-management algorithms, *see* Eleftheriou ¶¶[0004]-[0008] (discussing flash controllers, garbage collection, wear leveling, and write amplification); Lu § 1 (discussing FTL design and file-system mechanisms), and the resulting architectural constraints compounded the consequences of internal write overhead.

To increase bit density, manufacturers progressed from single-level cell ("SLC") to multi-level cell ("MLC"), triple-level cell ("TLC"), and quad-level cell ("QLC") flash. *See*, *e.g.*, Agrawal et al., "Design Tradeoffs for SSD Performance," p. 2; Colgrove et al., "Purity: Building Fast, Highly-Available Enterprise Flash Storage from Commodity Components," p. 2 ("Modern SSDs can store from 1-4 bits per cell… QLC store … 4 bits per cell"); Chen, Koufaty & Zhang, "Understanding Intrinsic Characteristics and System Implications of Flash Memory Based Solid State Drives," § 2.1 (2009). The industry also moved from planar NAND devices to three-dimensional architectures. *See*, *e.g.*, U.S. Patent Pub. No. 2009/0121271 (Son), ¶¶[0008], [0063]-[0064].

These advances increased capacity and lowered cost per bit, Agrawal, p. 7, but each successive density increase drastically reduced program/erase ("P/E") endurance. SLC flash is rated for approximately 100,000 P/E cycles, whereas MLC supports only 3,000 to 5,000 cycles, and TLC and QLC support still fewer. Colgrove, p. 2. Lu et al. confirmed that the endurance problem "is getting worse as storage density increases with the adoption of multi-level cells (MLC)" (Lu, Abstract) because finer voltage steps inside each cell are "less tolerant to leakage and noise interference," causing "the reliability and lifetime of flash memory [to] decline[] dramatically" (Lu, § 1). At the same time, process-geometry scaling increased susceptibility to read disturb errors, cell-to-cell interference, and retention loss, requiring heavier error correction and more frequent internal data-refresh operations. Cai et al., "Read Disturb Errors in MLC NAND Flash Memory," §§ 1-3 (SAMSUNG-GAEA_00041470). The result was that any given level of write amplification consumed the device's shrinking P/E budget far more quickly: a WAF of 2 that was easily absorbed over 100,000 SLC cycles could exhaust an MLC device rated for 3,000 cycles in a fraction of the time.

The industry responded to these scaling-driven constraints by implementing controllers with management techniques such as wear leveling, garbage collection, and bad-block management. *See*, *e.g.*, Agrawal et al., pp. 1-2, 10-11. Another technique, over-provisioning (*i.e.*, reserving physical flash capacity beyond what is advertised to the host) could reduce WAF by maintaining a larger pool of free blocks for garbage collection. *Id.* at pp. 5, 10; Kanno ('079), 13:1-22 (explaining that a larger over-provisioned area delays garbage collection and allows invalidated blocks to be reused without copying valid data). But over-provisioning came at a direct cost to user-visible capacity, *id.*, creating an inherent tension: the more capacity a manufacturer devoted to mitigating WAF, the less capacity was available to the customer. At the same time, the trend toward larger flash pages meant that even small host writes triggered full-page operations, further amplifying write volume at the device level. Lu § 1 (observing that "the trend of increasing page size of the flash memory makes this problem more serious," because partial-page updates nearly always require read-modify-write operations).

In sum, write amplification was one of many well-documented consequences of the storage industry's drive toward increased density.

D. Segregating Data by Expected Lifetime Was the Known Solution

The solution to write amplification was equally well known: grouping data with similar expected lifetimes into the same erase block, thus permitting erasure of the entire block without the need to copy remaining valid pages. Multi-stream, discussed further below, is a known mechanism in use for segregating data by its expected lifetime. Data segregation was explored academically beginning in 2008. For example, Chang described classifying data by write frequency and separately managing hot and cold data across SLC and MLC flash, explaining that "[t]he SLC flash better handles small and frequently arriving data, while MLC flash is suitable to store bulk and cold data." L.-P. Chang, "Hybrid Solid-State Disks," ASP-DAC (2008), § III

(SAMSUNG-GAEA_00004373). Building on that concept, Lee et al. implemented hot/cold queue detection in FlexFS, whereby "[h]ot data with a high update frequency generates more outdated versions of itself than cold data, which is updated infrequently." S. Lee et al., "FlexFS: A Flexible Flash File System for MLC NAND Flash Memory," USENIX ATC '09, § 4.1.3 (SAMSUNG-GAEA_00004792).

Patent publications likewise taught the concept. For example, Huang et al. disclosed dividing SSD storage blocks by data class reflecting expected lifespan, storing like-classified data in the same erase block, and expressly identified the resulting WAF reduction: "[T]he write amplification factor is reduced and performance is improved." U.S. Patent App. Pub. No. 2013/0024599 (Huang) (SAMSUNG-GAEA_00000984), ¶¶[0006]-[0007], [0103]-[0105], [0115], Cls. 17-19. Extending this approach to firmware-level categorization, Seo classified data by update frequency and life cycle into categories mapped to distinct physical areas, disclosing that the system "may reduce a garbage collection operation by physically classifying a space in which data is stored according to the locality of data." U.S. Patent App. Pub. No. 2014/0281172 (Seo) (SAMSUNG-GAEA_00001265), ¶¶[0044], [0068]-[0070], [0119]-[0122]. Applying the same principle at the interface level, Hashimoto disclosed stream-ID-based physical block placement with dedicated input-block pools for each stream, such that "the type of data (or lifetime of data) stored in the physical block 36 can be uniform." U.S. Patent App. Pub. No. 2016/0321010 (Hashimoto) (SAMSUNG-GAEA_00001713) (published Nov. 3, 2016), ¶¶[0116]-[0124], [0148].

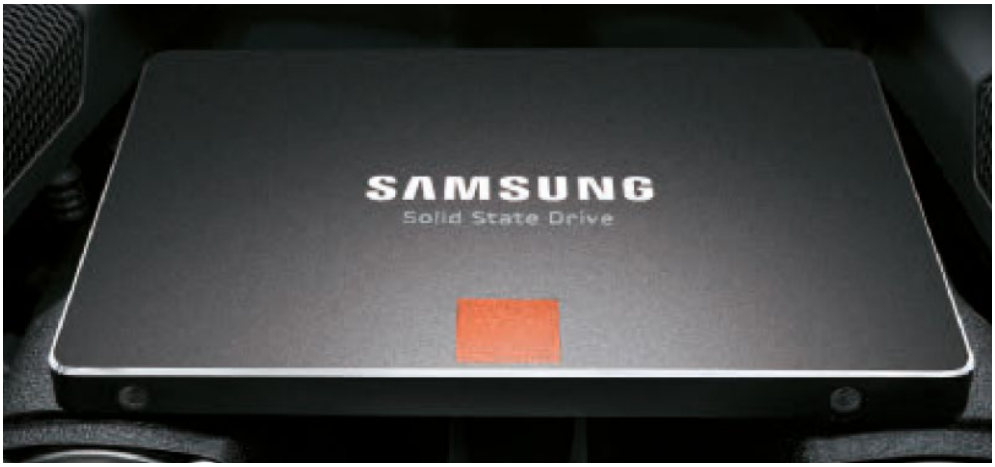
The concept was also formally standardized. In November 2014, Samsung, Toshiba, Micron, NetApp, and OCZ jointly submitted a Storage Intelligence Proposal to the T10 Technical Committee defining streams as same-lifetime data whose co-location eliminates

unnecessary data copying. SCSI T10, Working Draft 14-275r0 (Nov. 3, 2014) (SAMSUNG-GAEA_00025438), p. 2. That standard was completed in May 2015. WD Blue 1TB SSD Reviewed, Fudzilla.com (Oct. 12, 2016) (SAMSUNG-GAEA_00029210), p. 5 ("A more advanced yet recent feature included in [the WD Blue 1TB SSD] is multi-stream, which was introduced in the T10 standard in May 2015 and is featured in Samsung's PM953S NVMe SSDs.").

NVMe Technical Proposal 008a, which provided a host mechanism to indicate logical blocks as part of one stream for device media-allocation optimization, was ratified on November 2, 2016, before Gaea's purported November 7, 2016 priority date; Samsung's Choi was a listed contributor. NVM Express, "NVMe Technical Proposal 008a" (ratified November 2, 2016; revised November 9, 2016) (SAMSUNG-GAEA_00024918).

E. Samsung Was First to Build and Commercialize Multi-Stream

In June 2014, Samsung engineers published "The Multi-Streamed Solid-State Drive" at HotStorage '14, defining a stream as "an abstraction of SSD capacity allocation that stores a set of data with the same lifetime expectancy." Kang et al., HotStorage '14 (SAMSUNG-GAEA_00004556), p. 2. Samsung implemented and tested a working multi-stream prototype on the Samsung 840 Pro SSD, as described in Section III.A.1.b.i below. Kang et al., HotStorage '14, §§ 3-4.



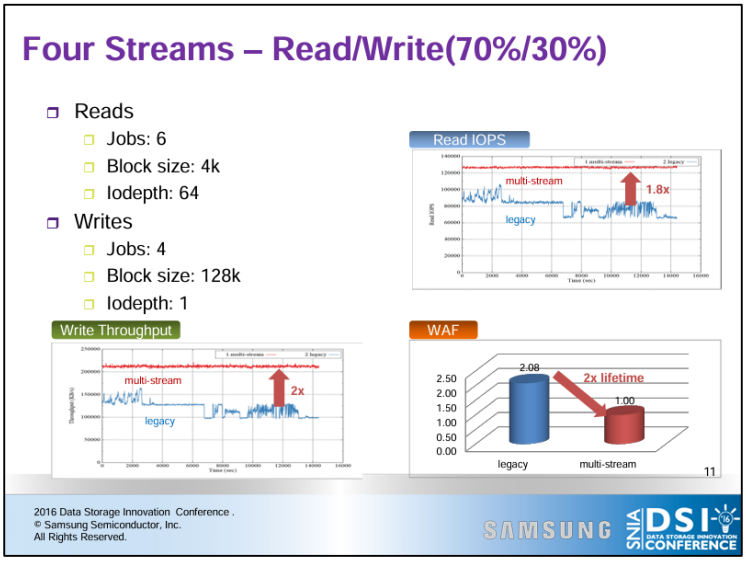
840 Pro Brochure (SAMSUNG-GAEA_00025478) at 1; Samsung 840 Pro SSD – CNET (SAMSING-GAEA_00029063) at 3-4.

Samsung advanced multi-stream to production with the PM953S NVMe SSD and later to the PM1633a SSD. Samsung sold the PM953S NVMe SSD to ZT Group International at least as early as the week of May 18, 2015. Samsung sold the PM1633a SSD to NetApp, Inc. at least as early as June 21, 2016. *See* Sections III.A.1.b.ii and III.A.1.b.iii below.

PM953S 2015 Multi-Stream SSD Technology (SAMSUNG-GAEA_00026542) at 1.

PM1633a Product Brief (SAMSUNG-GAEA_00029563) at 1.

In June 2016, Samsung's Choi presented measured write-amplification data under controlled benchmark conditions, finding that Multi-Stream reduced WAF from 2.08 (legacy) to 1.00, with approximately 2× write throughput and approximately 2× lifetime improvement:



Choi, "Increasing SSD Performance and Lifetime with Multi-stream Technology," SNIA DSI Conference, June 2016, (SAMSUNG-GAEA_00025880) p. 11.

Moreover, as listed below in the disclosure of prior art, Samsung has numerous patents directed to multi-stream technology in solid-state drives that are prior-art to the Asserted Patents.

F. Hyperscalers Drove the Industry's Shift to Policy-Based SSD Control

Multi-Stream did not emerge in isolation: it was contemporaneous with a broader movement in the storage industry away from opaque device abstractions and toward software-programmable, policy-based control of storage media. Historically, device manufacturers concealed the complexity of NAND flash management behind a Flash Translation Layer ("FTL") and a simple logical block interface, preserving backward compatibility but preventing the host from exploiting knowledge of device behavior. *See*, *e.g.*, Chen, Koufaty & Zhang, "Understanding Intrinsic Characteristics and System Implications of Flash Memory Based Solid State Drives," §§ 2.1-2.2 (2009).

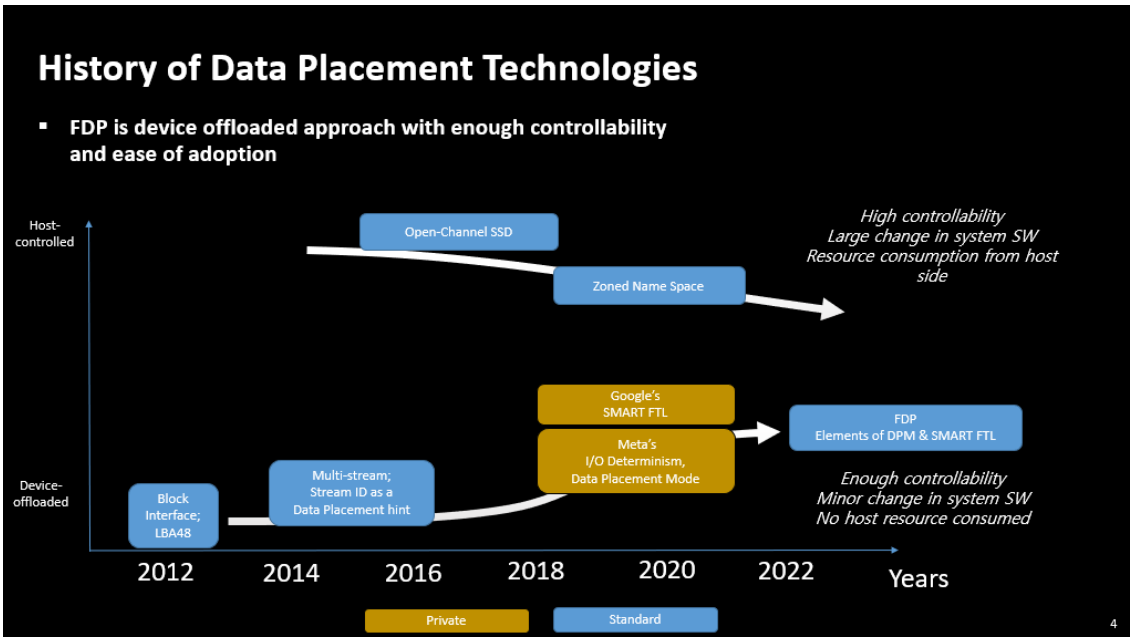
The rise of hyperscale operators changed this calculus. Because operators such as Google and Meta control much of the computing stack (*e.g.*, from applications through distributed storage software to hardware procurement), hardware/software co-optimization at the storage layer became practical. The Google File System ("GFS"), first published in 2003, exemplified this approach. GFS was "driven by observations of [Google's] application workloads and technological environment, both current and anticipated, that reflect a marked departure from some earlier file system assumptions." Ghemawat, Gobioff & Leung, "The Google File System," Abstract (2003). Google recognized that "co-designing the applications and the file system API benefits the overall system by increasing our flexibility." *Id.* § 1.

Ceph, developed at the University of California, Santa Cruz and published in 2006, replaced traditional allocation tables entirely with CRUSH ("Controlled Replication Under Scalable Hashing"), a pseudo-random data distribution function in which any party (*e.g.*, client, storage device, or metadata server) "can independently calculate the location of any object" using only a hierarchical cluster map and configurable placement rules. Weil et al., "Ceph: A Scalable, High-Performance Distributed File System," § 5.1 (2006). Thus, by at least 2006 (a full

decade before Gaea's purported November 7, 2016 priority date) distributed storage systems had demonstrated the practice of exposing storage characteristics to host-level software and implementing policy-based data-placement decisions at the software layer.

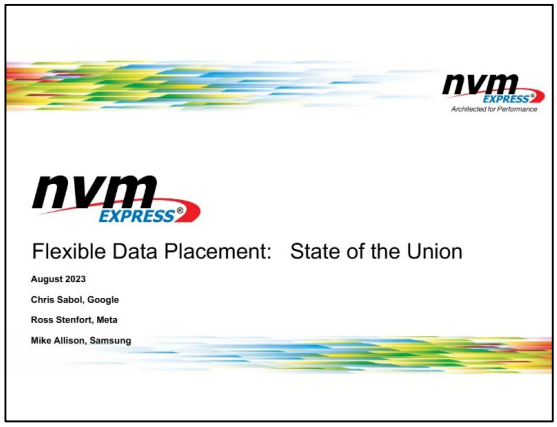
G. FDP Was a Direct, Incremental Evolution of Multi-Stream

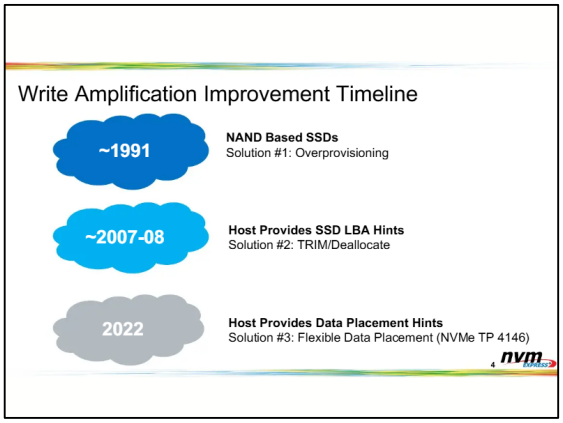
Flexible Data Placement ("FDP"), the technology at the center of Gaea's infringement allegations, was developed as an evolution of Samsung's Multi-Stream architecture. Samsung's internal technology presentations trace a lineage: "2014 Multi-stream; Stream ID as a Data Placement hint … 2020 FDP Elements of DPM & SMART FTL":



FDP_202310_Techday.pptx (SAMSUNG-GAEA_00027353), slide 4.

An August 2023 "Flexible Data Placement: State of the Union" presentation from nonprofit industry consortium NVM Express, Inc. identified FDP as "Solution #3" in a numbered sequence spanning decades of write-amplification improvement:



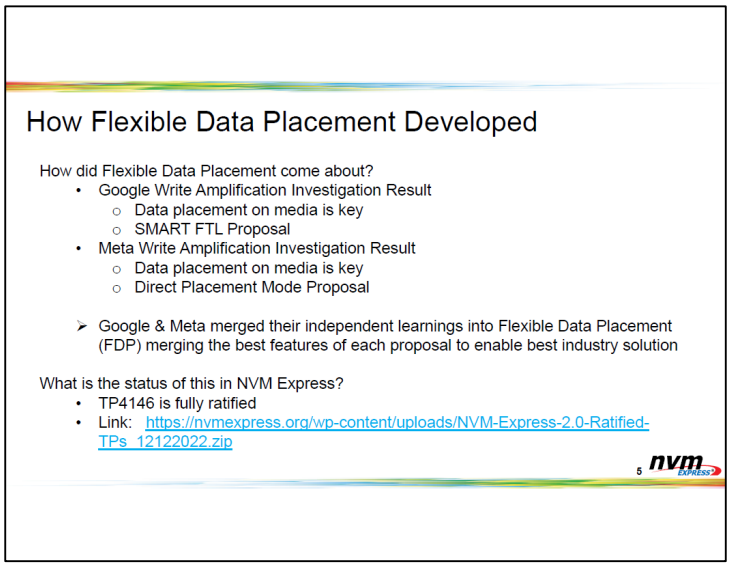


Slides 1, 4. NVM Express maintains the open NVMe standard governing how computers communicate with solid-state storage. Its members include competing hyperscalers, OEMs, and flash manufacturers, including Samsung, Meta, and Google. New features enter the standard through numbered Technical Proposals co-drafted by engineers from multiple member companies. The "State of the Union" presentation was authored by Chris Sabol (Google), Ross Stenfort (Meta), and Mike Allison (Samsung), all of whom played key roles in the development of FDP.

An NVM Express white paper co-authored by Samsung engineers states that FDP's "set of Reclaim Unit Handles is analogous to an SSD supporting multiple streams where write commands may specify the Stream Directive to indicate the write resources to use for writing the logical blocks." Introduction to Flexible Data Placement: A New Era of Optimized Data Management (SAMSUNG-GAEA_00050405), p. 8. According to the white paper, FDP's improvement over Streams was not the concept of host-directed data placement but rather the addition of an alignment-feedback mechanism. *Id.*, pp. 8, 10. For example, the white paper explained that "[t]he NVMe Streams capability has no mechanism for the host to determine the current alignment." *Id.* p. 8. The white paper characterizes FDP as "a more flexible interface that enables the host software stack to introduce incremental benefits." *Id.*, p. 10. The ratified NVMe

Technical Proposal 4146 likewise describes FDP as "an enhancement of the NVM Command Set." TP4146 Flexible Data Placement 2022.11.30 Ratified (SAMSUNG-GAEA_00024964), p. 2.

FDP was specifically designed to "retrofit[] existing applications that follow software data placement policies." Introduction to Flexible Data Placement: A New Era of Optimized Data Management, p. 10. FDP resulted from the merger of independently developed proposals by Google (SMART FTL) and Meta (Direct Placement Mode), each of which was premised on the concept that host-directed media data placement reduces write amplification.



Flexible Data Placement: State of the Union, slide 5. Samsung contributed seven named co-authors to TP4146, the largest contingent of any contributor. TP4146 Flexible Data Placement 2022.11.30 Ratified, p. 2.

H. Host-Programmable SSD Policies and Content Processing Were Known Before November 2016

As such, FDP and its predecessor, Multi-Stream, center around the concept of host-communicated storage policies, which actually extends back decades. For example, IBM's Data

Facility Storage Management Subsystem ("DFSMS"), introduced in the 1980s, defined policy types through which an administrator specified how the system should handle data; IBM's GPFS and Spectrum Scale later extended these concepts with configurable policy-driven tiered storage management. Ashton et al., "Two Decades of Policy-Based Storage Management for the IBM Mainframe Computer" (2003), pp. 5-6; GPFS: Advanced Administration Guide (2014), pp. 13-16; IBM Spectrum Scale (IBM Redbooks, May 2015), pp. 272-274.

At the SSD interface level, NVMe 1.2 (November 3, 2014) expanded host-configurable features including workload hints and a Dataset Management command carrying context attributes for access frequency, sequential write/read range, write-prepare indication, and access latency. NVM Express Revision 1.2 (Nov. 3, 2014), pp. 119-120, 145-148. The Open-Channel SSD specification (April 2016), dated seven months before Gaea's purported November 7, 2016 priority date, went further, exposing physical media geometry and placing data placement, garbage collection, and wear leveling under host control. Open-Channel Solid State Drives, NVMe Specification Revision 1.2 (Apr. 2016), pp. 3-6. SBC-3 (October 2010) provided WRITE SAME and UNMAP commands through which the host directed pattern writing, deallocation, and thin-provisioning operations on the storage device. SCSI Block Commands - 3 (SBC-3), Working Draft Revision 25 (Oct. 27, 2010), pp. 146-148, 177-181.

Policy-driven content processing was equally well established. For example, RAID controllers processed content for storage by applying mirroring, striping, and parity calculations, and all such processing was governed by controller-software policies. Patterson, Gibson & Katz, "A Case for Redundant Arrays of Inexpensive Disks (RAID)," pp. 2-6; Chen et al., "RAID: High-Performance, Reliable Secondary Storage," pp. 11-16, 53-54. Pure Storage's Purity software implemented software-designed mechanisms for Reed-Solomon encoding, parity

layout, rebuild behavior, and flash-endurance management. Colgrove et al., "Purity: Building Fast, Highly-Available Enterprise Flash Storage from Commodity Components," pp. 1, 4-6. EMC's XtremIO XDP placed data based on content fingerprints rather than logical addresses and was "completely implemented in software … allowing tremendous flexibility." EMC Corporation, "XtremIO Data Protection (XDP)," pp. 11-12, 22. Pre-priority patent publications, including Armitano (US 2004/0230795), Devarakonda (US 2007/0244939; US 2007/0244940), and DeJana (US 2014/0297695), disclosed storage systems in which requests carried policy-like attributes dictating replication, routing, and placement.

III. P.R. 3-3 DISCLOSURES AND CONTENTIONS

The following Appendices 023, 553, and 715 (collectively, the "Appendices") include claim charts (as exhibits to each Appendix) of prior art references and products that, alone and/or in combination with other references, render the Asserted Claims of the Asserted Patents invalid under §§ 102 or 103, and further include secondary references that would have been obvious to combine with the charted prior art references and motivations for making such combinations.

Appendix 023	U.S. Patent No. 10,776,023
Appendix 553	U.S. Patent No. 11,907,553
Appendix 715	U.S. Patent No. 12,265,715

A. P.R. 3-3(a) Disclosures: Identification of Items of Prior Art That Anticipate or Render Obvious Asserted Claims

Subject to Defendants' reservation of rights, the following prior art patents, printed publications, and products, alone and/or in combination, anticipate and/or render obvious the Asserted Claims of the Asserted Patents.

1. The '023 Patent

a. Prior Art Patents and Published Patent Applications

Patent No. / Patent Application Publication No.	Country of Origin	Issue/Publication Date	Short Title
2015/0052167	United States	February 19, 2015	Olster
8,874,835	United States	October 28, 2014	Davis
2016/0313943	United States	October 27, 2016	Hashimoto
10,552,058	United States	February 4, 2020	Jadon
2008/0215800	United States	September 4, 2008	Lee
9,400,749	United States	July 26, 2016	Kuzmin
7,925,807	United States	April 12, 2011	Panabaker
9,075,851	United States	July 7, 2015	Kilian
5,875,158	United States	February 23, 1999	Schell
9,021,189	United States	April 28, 2015	Salessi
8,095,508	United States	January 10, 2012	Chamberlain
8,880,836	United States	November 4, 2014	Owa
6,134,631	United States	October 17, 2000	Jennings
2015/0046636	United States	February 12, 2015	Seo
2015/0347291	United States	December 3, 2015	Choi
10,095,613	United States	October 9, 2018	Jo
10,282,324	United States	May 7, 2019	Bhimana '324
10,824,576	United States	November 3, 2020	Bhimana '576
10,509,770	United States	December 17, 2019	Huo '770
9,880,780	United States	January 30, 2018	Martineau '780
9,898,202	United States	February 20, 2018	Martineau '202
9,959,046	United States	May 1, 2018	Huo '046
10,296,264	United States	May 21, 2019	Hassani '264
10,732,905	United States	August 4, 2020	Hassani '905
12,073,125	United States	August 27, 2024	Huen '125
11,586,392	United States	February 21, 2023	Huen '392

Patent No. / Patent Application Publication No.	Country of Origin	Issue/Publication Date	Short Title
10,592,171	United States	March 17, 2020	Huen '171
10,866,905	United States	December 15, 2020	Pandurangan
10,324,832	United States	June 18, 2019	Yang
10,120,606	United States	November 6, 2018	Kim
10,216,417	United States	February 26, 2019	Huen '417
11,048,411	United States	June 29, 2021	Huen '411
10,739,995	United States	August 11, 2020	Huen '995
2012/0166749	United States	June 28, 2012	Eleftheriou
2,448,353A	Great Britain	February 29, 2012	Broadbent
9,256,542	United States	February 9, 2016	Flower
7,549,016	United States	June 6, 2009	Fujibayashi
2015/0381727	United States	December 31, 2015	Muhlestein
9,052,823	United States	June 9, 2015	Yamamoto
2017/0249080	United States	August 31, 2017	Bonnet
2014/136263	Japan	October 22, 2014	Kubota
7,853,759	United States	December 14, 2010	Sadovsky

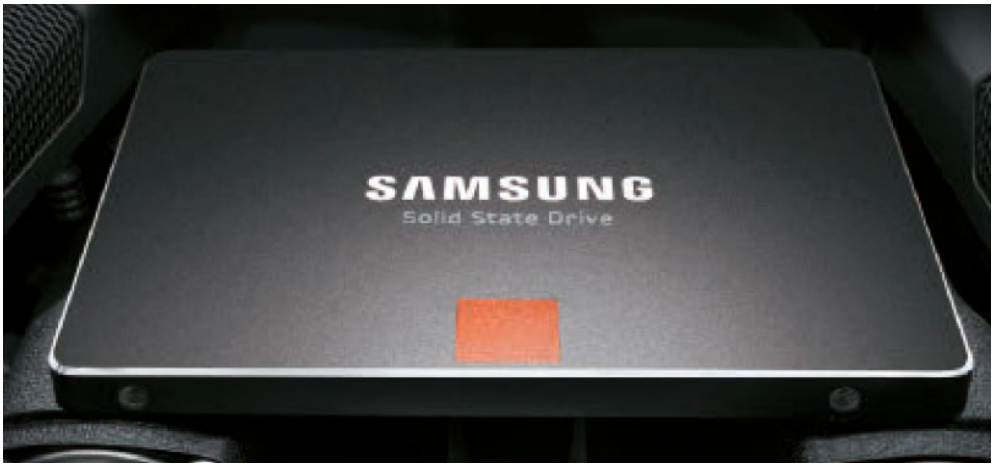
b. Prior Art Products

Product	Entities Involved in Use, Sale, Offer for Sale, or Publication	First Date Used, Sold, Offered, or Made Public	Short Title
Samsung PM953S Solid-State Drive	Samsung, Microsoft, HPQ, Dell, ZT Group International, Lenovo	May 19, 2015	PM953S
Samsung PM1633a Solid-State Drive	Samsung, NetApp, Inc., Smart Modular Technologies, WPG Americas, Inc.	June 21, 2016	PM1633a

Product	Entities Involved in Use, Sale, Offer for Sale, or Publication	First Date Used, Sold, Offered, or Made Public	Short Title
Samsung 840 Pro Solid-State Drive	Samsung, Jeong-Uk Kang, Jeeseok Hyun, Hyunjoo Maeng, Sangyeun Cho	June 17, 2014	840 Pro
Radian Memory Systems RMS-250	Radian Memory Systems, upon information and belief OEMs, such as EMC, NetApp, Dell, Isilon, and Data Domain	August 4, 2015	RMS-250
Seagate Kinetic	Seagate	October 2013	Seagate Kinetic
Micron M600	Micron	September 2014	Micron M600
UC San Diego Willow SSD	Sudharsan Seshadri, Mark Gahagan, Sundaram Bhaskaran, Trevor Bunker, Arup De, Yanqin Jin, Yang Liu, and Steven Swanson of the University of California, San Diego	October 2014	Willow SSD

(i) Samsung 840 Pro (Kang Paper Implementation)

The Samsung 840 Pro is a 2.5-inch solid-state drive that uses a SATA 6Gb/s interface.



840 Pro Brochure at 1; Samsung 840 Pro SSD – CNET at 3-4.

Design and features

Drive type	7mm-thick, 2.5-inch standard internal drive
Connector options	SATA 3 (6Gbps), SATA 2, SATA
Available capacities	64GB, 128GB, 256GB, 512GB
Product dimensions	7mm-thick, 2.5-inch standard
Capacity of test unit	512GB
Controller	3-core MDX controller

Samsung 840 Pro SSD – CNET at 3.

Samsung engineers developed and implemented a multi-stream interface on the 840 Pro that allowed the host system to inform the SSD about the expected lifetime of data being written, enabling the SSD to place data with similar lifetimes together and reduce garbage-collection overhead. Kang – The Multi-Streamed Solid-State Drive at 3-4. The Samsung 840 Pro (Kang paper) system was first publicly available no later than June 17, 2014, when Dr. Jeong-Uk Kang

published the paper "The Multi-Streamed Solid-State Drive," disclosing Samsung's implementation of the multi-stream interface on the 840 Pro, including the stream-based data placement mechanism, the SATA-command-level stream-ID communication, and the host-side Linux kernel modifications. *Id.* Samsung's implementation supported four explicit streams (Streams 1-4) plus a default stream (Stream 0). *Id.* On the host side, the implementation modified the Linux kernel to pass stream IDs from applications down through the file system to the SSD. *Id.*

The following documents teach aspects of the Samsung 840 Pro (Kang Paper) system:

- Kang – The Multi-Streamed Solid-State Drive (published June 17, 2014): SAMSUNG-GAEA_00004556
- 840 Pro Brochure: SAMSUNG-GAEA_00025478
- Samsung SSD Pro 840 Pro Series Data Sheet Rev. 1.3: SAMSUNG-GAEA_00028070
- Samsung 840 Pro SSD – CNET: SAMSING-GAEA_00029063
- Samsung SSD 840 Pro Storage Review: SAMSING-GAEA_0029089
- Samsung 840 Pro SSD: More Speed, Less Power, And Toggle-Mode 2.0: SAMSUNG-GAEA_00029080
- Samsung SSD White Paper: SAMSUNG-GAEA_00026563
- Samsung Power Loss Protection in SSDs White Paper: SAMSUNG-GAEA_00025195
- Multi-Stream SSD Technology: SAMSUNG-GAEA_00004625
- ADS50974-014: SAMSUNG-GAEA_00028065
- MDX User's Manual: SAMSUNG-GAEA_00051003

- ATA&ATAPI Command Set-3 (ACS-3) Specification: SAMSUNG-GAEA_00050426

(ii) Samsung PM953S (Multi-Stream SSD)

The Samsung PM953S is a PCIe NVMe enterprise solid-state drive in the M.2 form factor that implements Samsung's multi-stream technology. Samsung PM953S M.2 Datasheet v1.0 (SAMSUNG-GAEA_00026488) at 1.

PM953S 2015 Multi-Stream SSD Technology (SAMSUNG-GAEA_00026542) at 1.

PM953S Image at 1.

The PM953S uses host-directed stream control to allow the host to indicate which data writes share a similar lifetime, so that the SSD can place related data together in the same erase blocks. PM953S 2015 Multi-Stream SSD Technology at 1-2; PM953S M.2 Datasheet at 4.

> With multi-stream technology, an innovative new technology standardized in T10, implemented in Samsung PM953S NVMe SSD, garbage collection can be eliminated or reduced by storing associated or similar lifetime data in the same erase block. This helps avoid NAND erase block fragmentation for data with the same lifetime. As a result of the decreased write amplification, storage systems exhibit improved read/write performance and a longer SSD device lifetime.

PM953S 2015 Multi-Stream SSD Technology at 2.

> **What is a stream?**
> Streams are host hints that indicate when data writes are associated with one another or have a similar lifetime. That is, a group of individual data writes are a collective stream and each stream is given a stream ID. For example, "hot" data can be assigned a unique stream ID and the data for that stream ID would go to the same erase block (Figure 1).

Id.

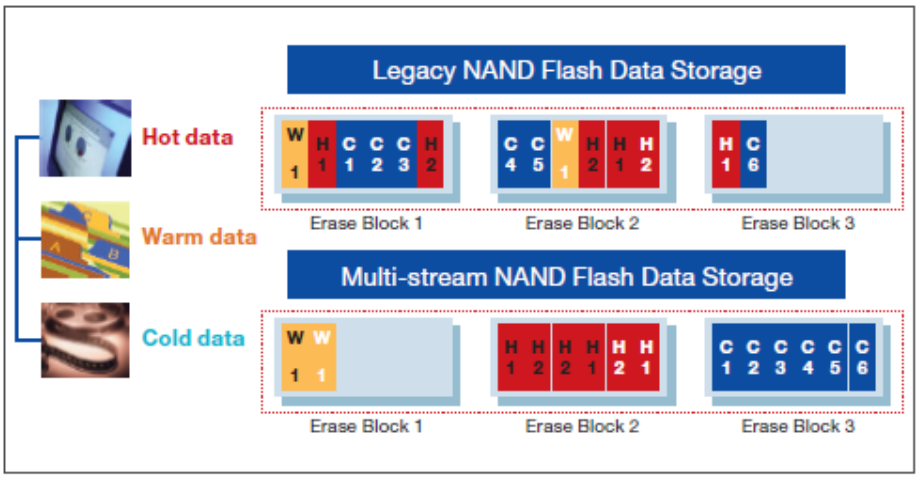


Figure 1. Legacy vs Multi-Stream Storage

Id.

The PM953S is compliant with NVM Express Specification Rev. 1.1a and supports the "Set Feature" command for enabling multi-stream technology, "Stream Control" commands

from the host, and namespace organization. Samsung PM953S M.2 Datasheet v1.0 at 4, 35, 39, 42.

FEATURES

- 128Gb NAND Flash Memory
- LPDDR3 DRAM Buffer Memory
- PCI Express Gen3
  - Single port X4 lanes
- Compliant with PCI Express Base Specification Rev. 3.0
- Compliant with NVM Express Specification Rev.1.1a
- Enhanced Power-Loss Data Protection
- End-to-End Data Protection
- Support SSD Enhanced S.M.A.R.T. Feature Set
- Hardware based AES-XTS 256-bit Encryption Engine
- Static and Dynamic Wear Leveling
- RoHS / Halogen-Free Compliant

PM953S M.2 Datasheet at 4.

[Table 117] Opcode for Admin Commands

Opcode (Hex)	Command Name
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Feature
0Ah	Get Feature
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download
80h – BFh	I/O Command Set Specific
C0h – FFh	Vendor Specific

Samsung PM953S M.2 Datasheet v1.0 at 35.

[Table 120] Identify Namespace Data Structure

Bytes	O/M	Default Value		Description
7:0	M	480GB 960GB	37E436B0h (512B) 6FC81AB0h (512B)	Namespace Size
15:88	M	480GB 960GB	37E436B0h (512B) 6FC81AB0h (512B)	Namespace Capacity
23:16	M	-		Namespace Utilization A device may report Namespace Utilization equal to Namespace Capacity at all times if the product is not targeted for thin provisioning environments
24	M	0h		Namespace Features Bits 7:1 Reserved Bit 0: Thin provisioning not supported
25	M	0h		Number of LBA Formats
26	M	0h		Formatted LBA Size Bits 7:5 – Reserved Bit 4: Metadata interleaved or separate (based on LBA format) Bit 3:0 – Indicates LBA format
27	M	0h		Metadata Capabilities Bits 7:2 – Reserved Bit 1 – Supports Metadata as separate buffer Bit 0 – Supports Metadata as extended LBA
28	M	0h		End-to-end Data Protection Capabilities Bits 7:5 – Reserved Bit 4 – Supports protection information as last 8 bytes of Metadata Bit 3 – Supports protection information as first 8 bytes of metadata Bit 2 – Supports Type 3 protection information Bit 1 – Supports Type 2 protection information Bit 0 – Supports Type 1 protection information
				End-to-End Data Protection Type Settings

Id. at 39.

[Table 125] Storage Intelligence NVM command set – Execution commands

Opcode (07)	Opcode (06:02)	Opcode (01:00)	Opcode2	O/M1	Command3
Standard Command	Function	Data Transfer			
0b	000 00b	00b	00h	M	Flush
0b	000 00b	01b	01h	M	Write
0b	000 00b	10b	02h	M	Read
0b	000 01b	00b	04h	O	Write Uncorrectable
0b	000 01b	01b	05h	O	Compare
0b	000 10b	00b	08h	O	Write Zeroes
0b	000 10b	01b	09h	O	Dataset Management
0b	000 11b	01b	0Dh	O4	Reservation Register
0b	000 11b	10b	0Eh	O4	Reservation Report
0b	001 00b	01b	11h	O4	Reservation Acquire
0b	001 01b	01b	15h	O4	Reservation Release
0b	00110b	00b	18h	O	Stream Control
0b	00111b	00b	1Ch	O	Garbage Collection
Vendor Specific					
1b	na	na	80h – FFh	O	Vendor specific

Id. at 42.

The Samsung PM953S uses "host hints that indicate when data writes are associated with one another or have a similar lifetime." PM953S 2015 Multi-Stream SSD Technology at 2. A group of individual data writes forms a collective stream; each stream receives a stream ID, and

data for a given stream ID is directed to the same erase block. *Id.* The PM953S processes content based on the multi-stream stream ID and is further configured to execute algorithms such as wear-leveling, error correcting code, bad block management, and garbage collection. PM953S 2015 Multi-Stream SSD Technology at 2.

> The three most crucial components of any SSD are the NAND flash memory, the controller, and the firmware. The first does the critical task of storing your precious data; the second two work together to accomplish the complex and equally essential tasks of managing data storage and maintaining the performance and lifespan of the SSD. Using the control program contained in the drive firmware, the controller (an embedded microchip) executes automated signal processing, wear-leveling, Error Correcting Code (ECC), bad block management, and garbage collection algorithms, communicates with the host device (e.g. a PC), and facilitates data encryption, among other tasks. Redundantly stored in NAND flash, the firmware may be updated manually to improve or extend functionality when the SSD manufacturer releases an update.

Samsung SSD White Paper at 30.

> **How does multi-stream eliminate or reduce garbage collection?**
> Because the data within an erase block has a similar lifetime or is associated with one another, there is a greater chance that an entire erase block is freed when data is deleted by a host system. The FIO benchmark tool is used for the performance measurements on Samsung PM953S M.2 NVMe SSDs.
> This SSD implements the NVMe interface of the multi-stream technology as standardized in T10 on May 2015. Figure 2 shows the performance measurement system and SIO configuration.

PM953S 2015 Multi-Stream SSD Technology at 2.

The Samsung PM953S was sold by Samsung at least as early as the week of May 18, 2015, to ZT Group International, Inc. *See* PM953S_000MU_2015~2016_20260806. Samsung also sold the PM953S to Microsoft, HPQ, Dell, and Lenovo. *Id.* A PM953S device and corresponding source code are available for inspection at Jones Day's Dallas Office. The following documents teach aspects of the Samsung PM953S system:

- Multi-Stream SSD Technology: SAMSUNG-GAEA_00004625

- Samsung PM953S M.2 Datasheet v1.0: SAMSUNG-GAEA_00005400
- PM953S Image: SAMSUNG-GAEA_00050423
- PM953S(2) Image: SAMSUNG-GAEA_00050423
- PM953S BOM: SAMSUNG-GAEA_00026560
- Samsung SSD White Paper: SAMSUNG-GAEA_00026563
- Samsung Power Loss Protection in SSDs White Paper: SAMSUNG-GAEA_00025195
- NVM-Express 1_1a SAMSUNG-GAEA_00004641
- PM953S_000MU_2015~2016_20260806 SAMSUNG-GAEA_00026559
- UBX Users Manual VOL2 v0.0: SAMSUNG-GAEA_00028086
- MZ1LV480HCHP_v0.1_사본: SAMSUNG-GAEA_00028076
- MZ1LV960HCJH_v0.1_사본: SAMSUNG-GAEA_00028081
- ads64438-000 pm953 m2 outline rev00 150318: SAMSUNG-GAEA_00028074

(iii) Samsung PM1633a (Multi-Stream SSD)

The Samsung PM1633a is an enterprise solid-state drive in a 2.5-inch form factor that uses a dual-port SAS 12 Gb/s (SAS 3.0) interface and implements multi-stream, stream-directed data placement. PM1633a Product Brief at 1; PM1633a 2.5 Spec v1.1 at 3.

PM1633a Product Brief at 1.

Physical

Form Factor:	2.5"
Interface:	SAS 12 Gbps
Protocol:	SCSI (SSP)
Power Draw:	Unknown (Idle) 9.0 W (Avg) Unknown (Max)

Samsung PM1633a 3.8 TB Specs at 2. The PM1633a supports the SAS/SCSI stream commands necessary for multi-stream operation. PM1633a Product Brief at 1; PM1633a 2.5 Spec v1.1 at 3.

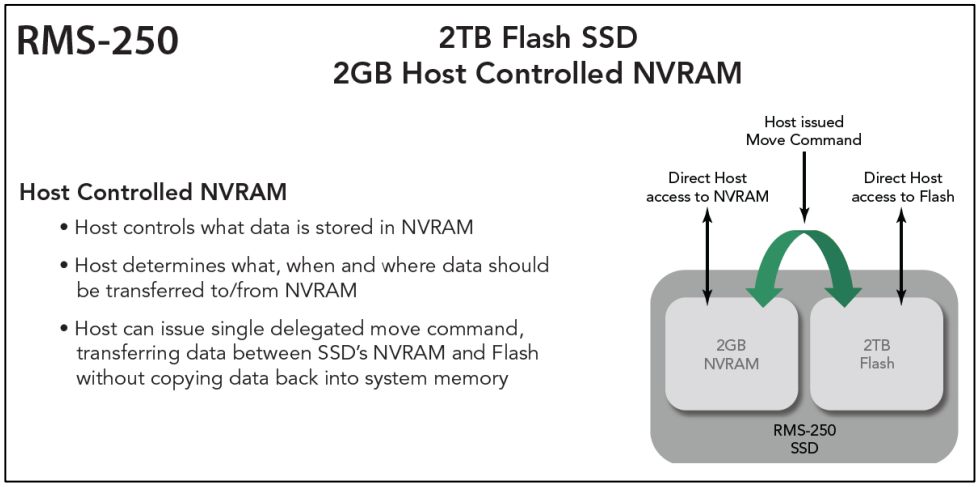
The Samsung PM1633a was sold by Samsung at least as early as June 21, 2016, to NetApp, Inc. *See* PM953S_000G3_2015~2016_20260806. Samsung also sold the PM1633a to Smart Modular Technologies, Smart Modular Tech (Europe), and WPG Americas, Inc. *Id.* A PM1633a device and corresponding source code are available for inspection at Jones Day's Dallas Office. The following documents teach aspects of the Samsung PM1633a system:

- PM1633a Product Brief: SAMSUNG-GAEA_00025963
- PM1633a 2.5 Spec v1.1: SAMSUNG-GAEA_00025945
- Samsung PM1633a 3.8 TB Specs: SAMSUNG-GAEA_00029156
- PM1633a SAS SSD: SAMSUNG-GAEA_00025963
- PM1633a MZILS3T8HMLH-000G3 BOM: SAMSUNG-GAEA_00025962
- Maximizing Data Center and Enterprise Storage Efficiency: SAMSUNG-GAEA_00025921
- Samsung SSD White Paper: SAMSUNG-GAEA_00026563

- Samsung Power Loss Protection in SSDs White Paper: SAMSUNG-GAEA_00025195
- Seagate SCSI Command Reference, Rev. D: SAMSUNG-GAEA_0025966
- PM953S_000MU_2015~2016_20260806: SAMSUNG-GAEA_0025965
- ADS70145-000_PM1633a(4TB)_OUTLINE_20160523_v0.0_사본: SAMSUNG-GAEA_00028576
- MZILS3T8HMLH_ADS69389-010_v0.0_사본: SAMSUNG-GAEA_00028760
- Rex_Flash_Channel_Users_Manual_ver0.91_v0.0_사본_v0.0_사본: SAMSUNG-GAEA_00028765
- T-REX_SAS12G_SSD_Controller_Overall_Architecture_v0.0_사본: SAMSUNG-GAEA_00048636
- ML31_HIL_Typhoon_Micro_Arch_Spec_EDM_v0.0_사본: SAMSUNG-GAEA_00028577

(iv) Radian RMS-250

The Radian RMS-250 is a 2.5-inch NVMe solid-state drive designed for data-center applications, offering up to 2 TB of enterprise eMLC NAND Flash storage with a PCIe Gen3 x4 NVMe interface. RMS-250 Spec Sheet at 1.



Id.

Id.

Unlike conventional SSDs that rely on an internal Flash Translation Layer to manage data placement opaquely, the RMS-250 replaces the FTL with Radian's "Symphonic" Cooperative Flash Management firmware. *Id.* This firmware enables the host system and SSD to cooperatively manage flash storage (*e.g.*, including data placement, garbage collection scheduling, and lifecycle management). *Id.*

> Supporting the Symphonic Cooperative Flash Management (CFM) firmware, the RMS-250 is a 2TB eMLC SSD that uniquely provides up to 2GB of host controlled local NVRAM.

Id.

> **Supports:**
> - Symphonic™ Cooperative Flash Management firmware
> - Up to 2GB host controlled NVRAM
> - Up to 2TB eMLC Flash
> - Over 300K IOPS in 66% Read/33% Write mix
> - 2.5″ Form Factor with SFF-8639 connector
> - NVMe PCIe x4 Gen3 interface
> - DiaLog™ OEM Diagnostic Lifecycle Monitoring
> - Fault Tolerant Flush-to-Flash™ Backup System
> - DuraLife™ Ultra-Capacitor Power Management System

Id. The Radian RMS-250 supports multi-stream writes and intelligent placement of data on the storage device, allowing the host to insert hot/cold data intelligence into the garbage-collection process. *Id*.

The Radian RMS-250 was sold and in public use at least as early as 2015. *See* Exhibit 553-07. The following documents teach aspects of the Radian RMS-250 system:

- RMS-250 Spec Sheet: SAMSUNG-GAEA_00025874

(v) Seagate Kinetic

The Seagate Kinetic is a hard disk drive and solid-state drive system manufactured by Seagate and was sold and in public use at least as early as October 2013. New Seagate Breakthrough Fundamentally Alters Cloud Economics, https://investors.seagate.com/news/news-

details/2013/New-Seagate-Breakthrough-Fundamentally-Alters-Cloud-Economics/default.aspx. The following documents teach aspects of the Seagate Kinetic:

- Seagate Kinetic Product Manual: SAMSUNG-GAEA_00005540
- Kinetic GitHub: https://github.com/Kinetic

(vi) Micron M600

The Micron M600 is a solid state drive manufactured by Micron and was sold and in public use at least as early as September 2014. Micron Announces M600 2.5 SATA, mSATA and m.2 SSDs for OEMs, https://www.tweaktown.com/news/40189/micron-announces-m600-2-5-sata-msata-and-m-2-ssds-for-oems/index.html. The following documents teach aspects of the Micron M600:

- M600 Datasheet: https://www.micron-electronic.com/pdf-dd/mtfddak1t0mbf-1an12abyy.pdf
- TCG Opal 2.01 Specification: https://trustedcomputinggroup.org/wp-content/uploads/TCG_Storage-Opal_SSC_v2.01_rev1.00.pdf

(vii) UC San Diego Willow SSD

The UC San Diego Willow SSD is a solid state drive made by Sudharsan Seshadri, Mark Gahagan, Sundaram Bhaskaran, Trevor Bunker, Arup De, Yanqin Jin, Yang Liu, and Steven Swanson of the University of California, San Diego. They presented their findings at the 11th USENIX Symposium on Operating Systems Design and Implementation on October 6-8, 2014. https://www.usenix.org/system/files/conference/osdi14/osdi14-paper-seshadri.pdf. The following documents teach aspects of the UC San Diego Willow SSD:

- Willow Paper: https://www.usenix.org/system/files/conference/osdi14/osdi14-paper-seshadri.pdf

- Willow Slides: https://www.usenix.org/sites/default/files/conference/protected-files/osdi14_slides_seshadri.pdf
- Willow Conference Presentation: https://www.youtube.com/watch?v=zpCN8GipdnM&t=1071s

2. The '553 Patent

a. Prior Art Patents and Published Patent Applications

Patent No. / Patent Application Publication No.	Country of Origin	Issue or Publication Date	Short Title
2012/0246435	United States	September 27, 2012	Meir
9,021,189	United States	April 28, 2015	Salessi
2015/0146364	United States	May 28, 2015	Chou
2014/0089278	United States	March 27, 2014	Lovinger
7,768,789	United States	August 3, 2010	Ni
10,846,231	United States	November 24, 2020	Kusuno
9,075,851	United States	July 7, 2015	Kilian
10,552,058	United States	February 4, 2020	Jadon
9,400,749	United States	July 26, 2016	Kuzmin
6,134,631	United States	October 17, 2000	Jennings
9,069,703	United States	June 30, 2015	Raam
7,925,807	United States	April 12, 2011	Panabaker
8,095,508	United States	January 10, 2012	Chamberlain
2015/0347291	United States	December 3, 2015	Choi
10,095,613	United States	October 9, 2018	Jo
10,282,324	United States	May 7, 2019	Bhimana '324
10,824,576	United States	November 3, 2020	Bhimana '576
10,509,770	United States	December 17, 2019	Huo '770
9,880,780	United States	January 30, 2018	Martineau '780
9,898,202	United States	February 20, 2018	Martineau '202
9,959,046	United States	May 1, 2018	Huo '046

Patent No. / Patent Application Publication No.	Country of Origin	Issue or Publication Date	Short Title
10,296,264	United States	May 21, 2019	Hassani '264
10,732,905	United States	August 4, 2020	Hassani '905
12,073,125	United States	August 27, 2024	Huen '125
11,586,392	United States	February 21, 2023	Huen '392
10,592,171	United States	March 17, 2020	Huen '171
10,866,905	United States	December 15, 2020	Pandurangan
10,324,832	United States	June 18, 2019	Yang
10,120,606	United States	November 6, 2018	Kim
10,216,417	United States	February 26, 2019	Huen '417
11,048,411	United States	June 29, 2021	Huen '411
10,739,995	United States	August 11, 2020	Huen '995
2012/0166749	United States	June 28, 2012	Eleftheriou
2,448,353A	Great Britain	February 29, 2012	Broadbent
9,256,542	United States	February 9, 2016	Flower
7,549,016	United States	June 6, 2009	Fujibayashi
2015/0381727	United States	December 31, 2015	Muhlestein
9,052,823	United States	June 9, 2015	Yamamoto
2017/0249080	United States	August 31, 2017	Bonnet
2014/136263	Japan	October 22, 2014	Kubota
7,853,759	United States	December 14, 2010	Sadovsky

b. Prior Art Products

Product	Entities Involved in Use, Sale, Offer for Sale, or Publication	First Date Used, Sold, Offered, or Made Public	Short Title
Samsung PM953S Solid-State Drive	Samsung, Microsoft, HPQ, Dell, ZT Group International, Lenovo	May 19, 2015	PM953S

Product	Entities Involved in Use, Sale, Offer for Sale, or Publication	First Date Used, Sold, Offered, or Made Public	Short Title
Samsung PM1633a Solid-State Drive	Samsung, NetApp, Inc., Smart Modular Technologies, WPG Americas, Inc.	June 21, 2016	PM1633a
Samsung 840 Pro Solid-State Drive	Samsung, Jeong-Uk Kang, Jeeseok Hyun, Hyunjoo Maeng, Sangyeun Cho	June 17, 2014	840 Pro
Radian Memory Systems RMS-250	Radian Memory Systems, upon information and belief OEMs, such as EMC, NetApp, Dell, Isilon, and Data Domain	August 4, 2015	RMS-250
Seagate Kinetic	Seagate	October 2013	Seagate Kinetic
Micron M600	Micron	September 2014	Micron M600
UC San Diego Willow SSD	Sudharsan Seshadri, Mark Gahagan, Sundaram Bhaskaran, Trevor Bunker, Arup De, Yanqin Jin, Yang Liu, and Steven Swanson of the University of California, San Diego	October 2014	Willow SSD

3. The '715 Patent

a. Prior Art Patents and Published Patent Applications

Patent No. / Patent Application Publication No.	Country of Origin	Issue/Publication Date	Short Title
2012/0246435	United States	September 27, 2012	Meir
9,021,189	United States	April 28, 2015	Salessi
2015/0146364	United States	May 28, 2015	Chou
2014/0089278	United States	March 27, 2014	Lovinger
7,768,789	United States	August 3, 2010	Ni
10,846,231	United States	November 24, 2020	Kusuno
9,075,851	United States	July 7, 2015	Kilian
10,552,058	United States	February 4, 2020	Jadon
9,400,749	United States	July 26, 2016	Kuzmin
6,134,631	United States	October 17, 2000	Jennings
9,069,703	United States	June 30, 2015	Raam
7,925,807	United States	April 12, 2011	Panabaker
8,095,508	United States	January 10, 2012	Chamberlain
2015/0347291	United States	December 3, 2015	Choi
10,095,613	United States	October 9, 2018	Jo
10,282,324	United States	May 7, 2019	Bhimana '324
10,824,576	United States	November 3, 2020	Bhimana '576
10,509,770	United States	December 17, 2019	Huo '770
9,880,780	United States	January 30, 2018	Martineau '780
9,898,202	United States	February 20, 2018	Martineau '202
9,959,046	United States	May 1, 2018	Huo '046
10,296,264	United States	May 21, 2019	Hassani '264
10,732,905	United States	August 4, 2020	Hassani '905
12,073,125	United States	August 27, 2024	Huen '125
11,586,392	United States	February 21, 2023	Huen '392
10,592,171	United States	March 17, 2020	Huen '171

Patent No. / Patent Application Publication No.	Country of Origin	Issue/Publication Date	Short Title
10,866,905	United States	December 15, 2020	Pandurangan
10,324,832	United States	June 18, 2019	Yang
10,120,606	United States	November 6, 2018	Kim
10,216,417	United States	February 26, 2019	Huen '417
11,048,411	United States	June 29, 2021	Huen '411
10,739,995	United States	August 11, 2020	Huen '995
2012/0166749	United States	June 28, 2012	Eleftheriou
2,448,353A	Great Britain	February 29, 2012	Broadbent
9,256,542	United States	February 9, 2016	Flower
7,549,016	United States	June 6, 2009	Fujibayashi
2015/0381727	United States	December 31, 2015	Muhlestein
9,052,823	United States	June 9, 2015	Yamamoto
2017/0249080	United States	August 31, 2017	Bonnet
2014/136263	Japan	October 22, 2014	Kubota
7,853,759	United States	December 14, 2010	Sadovsky

b. Prior Art Products

Product	Entities Involved in Use, Sale, Offer for Sale, or Publication	First Date Used, Sold, Offered, or Made Public	Short Title
Samsung PM953S Solid-State Drive	Samsung, Microsoft, HPQ, Dell, ZT Group International, Lenovo	May 19, 2015	PM953S
Samsung PM1633a Solid-State Drive	Samsung, NetApp, Inc., Smart Modular Technologies,	June 21, 2016	PM1633a

Product	Entities Involved in Use, Sale, Offer for Sale, or Publication	First Date Used, Sold, Offered, or Made Public	Short Title
	WPG Americas, Inc.		
Samsung 840 Pro Solid-State Drive	Samsung, Jeong-Uk Kang, Jeeseok Hyun, Hyunjoo Maeng, Sangyeun Cho	June 17, 2014	840 Pro
Radian Memory Systems RMS-250	Radian Memory Systems, upon information and belief OEMs, such as EMC, NetApp, Dell, Isilon, and Data Domain	August 4, 2015	RMS-250
Seagate Kinetic	Seagate	October 2013	Seagate Kinetic
Micron M600	Micron	September 2014	Micron M600
UC San Diego Willow SSD	Sudharsan Seshadri, Mark Gahagan, Sundaram Bhaskaran, Trevor Bunker, Arup De, Yanqin Jin, Yang Liu, and Steven Swanson of the University of California, San Diego	October 2014	Willow SSD

B. P.R. 3-3(b) Disclosures: Each Item of Prior Art that Anticipates and/or Renders Obvious the Asserted Claim, and Obviousness Combinations and Motivations

Based on presently known information, the Appendices to these Invalidity Contentions identify for each item of prior art whether it anticipates the Asserted Claims and/or renders the Asserted Claims obvious. Where all claim elements of the Asserted Claims are identified, either explicitly or inherently as understood by a POSITA, in a single charted item of prior art, the Asserted Claims are anticipated by that item of prior art.

To the extent Gaea asserts that any of the prior art references charted in the Appendices fail to explicitly or inherently disclose any element of the Asserted Claims, it would have been obvious to modify such reference to include the allegedly missing element, in view of the knowledge of a POSITA and/or in combination (as provided in the chart below) with any of the other prior art references identified in this section, in the Appendices, and/or admitted prior art of the Asserted Patents.

1. Prior Art Grounds

a. The '023 Patent (Appendix 023)

Ex. No.	Grounds
023-01	Olster, Davis
023-02	Hashimoto
023-03	Jadon, Lee
023-04	Samsung PM953S
023-05	Samsung PM1633a
023-06	Samsung 840 Pro
023-07	Radian RMS-250 Radian RMS-250 and Jadon
023-8	Panabaker
023-9	Kim

Ex. No.	Grounds
023-10	Seagate Kinetic
023-11	Micron M600
023-12	UC San Diego Willow SSD

b. The '553 Patent (Appendix 553)

Ex. No.	Grounds
553-01	Meir and Salessi Meir, Salessi, and Ni Meir, Salessi, and Chou Meir, Salessi, and Lovinger Meir, Salessi, Lovinger, and Ni Meir, Salessi, Lovinger, and Chou Meir and Ni Meir and Chou Meir and Lovinger Meir, Lovinger, and Ni Meir, Lovinger, and Chou
553-02	Jadon Jadon and Ni Jadon and Chou Jadon and Kilian Jadon, Kilian, and Ni Jadon, Kilian, and Chou
553-03	Kusuno Kusuno and Ni Kusuno and Chou Kusuno and Kilian Kusuno, Kilian, and Ni Kusuno, Kilian, and Chou
553-04	Samsung PM953S Samsung PM953S and Ni Samsung PM953S and Chou Samsung PM953S and Hiew Samsung PM953S and the knowledge of the person with ordinary skill in the art

Ex. No.	Grounds
553-05	Samsung PM1633a
553-06	Samsung 840 Pro
553-07	Radian RMS-250 Radian RMS-250 and Jadon
553-08	Jennings Jennings and Ni Jennings and Chou Jennings and Kilian Jennings, Kilian, and Ni Jennings, Kilian, and Chou
553-09	Raam Raam and Ni Raam and Chou Raam and Kilian Raam, Kilian, and Ni Raam, Kilian, and Chou
553-10	Seagate Kinetic
553-11	Micron M600
553-12	UC San Diego Willow SSD
553-13	Kim Kim and Ni Kim and Chou

c. The '715 Patent (Appendix 715)

Ex. No.	Grounds
715-01	Meir and Salessi Meir, Salessi, and Chou Meir, Salessi, and Ni Meir Meir and Chou Meir and Ni
715-02	Jadon Jadon and Ni Jadon and Chou

Ex. No.	Grounds
715-03	Kusuno Kusuno and Ni Kusuno and Chou
715-04	Samsung PM953S Samsung PM953S and Ni Samsung PM953S and Chou Samsung PM953S and Hiew Samsung PM953S and the knowledge of a POSITA
715-05	Samsung PM1633a
715-06	Samsung 840 Pro
715-07	Radian RMS-250 Radian RMS-250 and Jadon
715-08	Jennings Jennings and Ni Jennings and Chou
715-09	Raam Raam and Ni Raam and Chou
715-10	Seagate Kinetic
715-11	Micron M600
715-12	UC San Diego Willow SSD
715-13	Kim Kim and Ni Kim and Chou

2. Motivations to Combine

It would have been obvious to a POSITA to combine one or more of the prior art references listed above with each of the other references and/or nothing more than his or her own knowledge, education, experience and/or common sense to arrive at the claimed invention. As the Supreme Court emphasized in *KSR Int'l Co. v. Teleflex, Inc.,* inventions arising from ordinary innovation, ordinary skill, or common sense are not patentable. 550 U.S. 398, 406, 420-

422 (2007). In addition, "the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id*. at 416. Because the Asserted Claims simply arrange familiar elements known in the field of the Asserted Patents, with each performing the same function it had been known to perform, and yield no more than what one would expect from such an arrangement, the combinations are obvious as will be explained in more detail in the attached Appendices.

The identified prior art references also use those familiar elements for their primary or well-known purposes in a manner well within the ordinary level of skill in the art. In addition, the identified prior art addresses the same or similar technical issues relating to the Asserted Patents and suggests the same or similar solutions to those issues. Moreover, because there were a finite number of predictable solutions for the problems purportedly solved by the Asserted Patents, a POSITA would have had good reason to pursue and/or combine known options and related applications. *Id.* Accordingly, common sense and the knowledge of the prior art render the claims invalid under either Section 102 or Section 103.

The Supreme Court has held that, "[w]hen a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a POSITA can implement a predictable variation, Section 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill . . . ." *Id*. at 417. Here, a POSITA would have been motivated by market forces to combine or modify references using known methods that a POSITA would have recognized as offering improvements to solutions of that time. The references identified describe methods that were known to offer

improvements, and, accordingly, a POSITA would have been motivated to combine or modify combined references to include such improvements as will be discussed in more detail in the attached Appendices.

Finally, as further described in the attached Appendices, the motivation to combine the teachings of the prior art references disclosed herein is also found in the references themselves and in: (1) the nature of the problem being solved, (2) the express, implied, and inherent teachings of the prior art, including the admitted prior art of the Asserted Patents, (3) the knowledge of persons of ordinary skill in the art, (4) the fact that the prior art is generally directed towards methods and systems described in the Asserted Patents and/or (5) the predictable results obtained in combining the different elements of the prior art, particularly in light of the well published and known evolution of technologies related to the Asserted Patents.

3. Additional Motivations to Combine

No showing of a specific motivation to combine the identified prior art references described herein and in the attached charts is required, as each combination of art would have had no unexpected results and at most would have simply represented a known alternative to a POSITA. *See id.* at 414-18 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a POSITA is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id*. at 421. Nevertheless, in addition to the information contained in this section and elsewhere in these Invalidity Contentions, Defendants identify additional exemplary motivations and reasons to combine the cited art for each Asserted Patent in the attached P.R. 3-3(c) claim charts.

4. Additional References

In addition to the prior art listed herein, additional prior art references may be referenced to show the state and evolution of technology at the time of the alleged invention and may be relevant to the validity of the Asserted Claims depending on, e.g., infringement and other positions taken by Gaea.

C. P.R. 3-3(c) Disclosures: Charts Identifying Where in Each Item of Prior Art Each Element of the Asserted Claim Is Found

Based on presently known information, the Appendices comprise claim charts that identify where specifically in each alleged item of prior art each limitation of each asserted claim is found.

D. P.R. 3-3(d) Disclosures: Invalidity Under 35 U.S.C. § 112(a)

The Asserted Claims are invalid for failure to satisfy the written description and enablement requirements of 35 U.S.C. § 112(a). The below examples are merely exemplary and are not intended to be limiting. Defendants reserve all rights to amend these Invalidity Contentions under 35 U.S.C. § 112(a), including after the Asserted Claims are ultimately construed by the Court and/or to account for any changes in the law concerning written description or enablement under 35 U.S.C. § 112(a). Defendants additionally reserve the right to provide additional explanation and/or argument for these Invalidity Contentions under Section 112(a), including, for example, based on expert testimony.

1. The '023 Patent

The following claim terms fail the requirements of 35 U.S.C. § 112(a) and therefore render the Asserted Claims invalid. For example:

Claim Element	Section 112(a) Requirement
Claims 1, 9, and 14: "wherein the at least one storage device policy	There is lack of written description and enablement for this claim term because the specification discloses "recording method[s]" only in the context of magnetic disk drives. The specification does

Claim Element	Section 112(a) Requirement
indicates at least a recording method for writing content to the storage media;"	not disclose "recording method[s]" in the context of SSDs, as accused of infringement. The specification describes recording methods through discussions of recording paths, recording patterns (255, 260, 265), recording path density, track spacing, bits per inch, actuator arm positioning, and read/write transducer placement, all of which are specific to magnetic disk technology. '023 patent, 5:26-7:5. Although the specification briefly mentions that "[w]hile the recording process differs for different types of storage media, the concept applies to all types of storage media" (6:59-61), the specification never describes or enables any recording method for solid-state drives or any other type of storage media. The specification admits that "the recording paths discussed may be inapplicable" to solid state memory (6:62-63). A POSITA would not be able to make and use the full scope of these claims without undue experimentation, and the specification does not reasonably convey possession of this claim term across its full scope. Claims 1, 9, and 14 accordingly lack written description and enablement under 35 U.S.C. § 112(a).
Claims 1, 9, and 14: "storage device policy"	There is a lack of written description and enablement for this claim term because the claims cover a genus of "storage device policies," and the minimal species disclosed in the specification are described in results-oriented, functional language (*e.g.*, controlling "margin of error" or making "trade-offs between reliability of storage and volume of storage," '023 patent, 3:10-12) without explaining how to achieve these results. This term encompasses essentially any algorithm, rule, library, or function as a storage device policy, but the patent does not disclose representative species across the full claimed genus. The breadth of this term sweeps in policies that no skilled artisan would consider useful or operable, let alone inventive. For example, the claims as written would cover storage device policies that affirmatively increase the risk of data loss. *See*, *e.g.*, '023 patent, 6:9-25 (implying that cloud storage providers have a higher tolerance for data "corruption"); 8:4-8 (stating that "content corruption" in video data may be of "little concern"). No host would purposefully implement such policies, but such destructive implementations fall squarely within the scope of "storage device policy" as claimed. The claim scope is inconsistent with the specification's generic, high-level disclosure, which consists of little more than black-box diagrams and generic flowcharts that describe policy operation only by its intended results, not by any particular structure or algorithm. Moreover, claim 14 recites "wherein the storage media comprises a solid-state memory device." The patent does not describe or enable a storage device policy as applied to a solid-state memory device. Instead it merely asserts that "the applicability to the concepts presented herein" as it relates to magnetic disks could also apply to solid-state storage media, without explaining how such concepts

Claim Element	Section 112(a) Requirement
	would translate to solid-state media even though the patent acknowledges that some magnetic disk features such as "the recording paths discussed may be inapplicable" to solid state memory (6:62-63). A POSITA would not be able to make and use the full scope of these claims without undue experimentation, and the specification does not reasonably convey possession of this claim term across its full scope. Claims 1, 9, and 14 accordingly lack written description and enablement under 35 U.S.C. § 112(a).

Accordingly, all of the above claims and their dependent claims of the '023 patent fail to comply with 35 U.S.C. § 112(a) for lack of enablement and lack of written description and are invalid. Further, all of the above claims and their dependent claims *as a whole* fail to meet the enablement and written description requirements of 35 U.S.C. § 112(a). Each Asserted Claim combines multiple limitations, including "storage device policy," "recording method," and (for claim 14) application to "solid-state memory devices," without any disclosure of how these elements function together. The specification provides only generic, results-oriented descriptions of individual concepts in isolation; it nowhere discloses or enables the combination of all claimed elements operating as an integrated system. A POSITA seeking to implement the full scope of any Asserted Claim would face undue experimentation because the specification provides no guidance on how to: (1) implement a "storage device policy" with sufficient particularity to practice the claims; (2) apply the claimed "recording method" limitations (which are described only in the context of magnetic disk technology) to solid-state memory devices; (3) integrate these concepts into a functioning storage system that performs all claimed functions; or (4) implement the claimed "policy" genus without unlimited trial-and-error testing. The specification's failure to disclose any working example, algorithm, or structure for the claimed combination, combined with the unpredictable nature of implementing "policies" across fundamentally different storage technologies demonstrates that a POSITA would require undue

experimentation to make and use the claimed invention. Moreover, the specification does not reasonably convey that the inventors possessed the full scope of the claimed invention at the time of filing. The specification describes "storage device policies" only through their intended results (e.g., making "trade-offs between reliability of storage and volume of storage"), not through any particular algorithm, data structure, or implementation. The inventors thus failed to describe the claimed genus with sufficient detail to demonstrate possession of the full scope of claimed subject matter. This includes that each and every Asserted Claim of the '023 patent is invalid for failure to comply with § 112(a).

2. The '553 Patent

The following claim terms fail the requirements of 35 U.S.C. § 112(a) and therefore render the Asserted Claims invalid. For example:

Claim Element	Section 112(a) Requirement
Claims 1-4, 9-12: "storage device policy"	There is a lack of written description and enablement for this claim term for the same reasons explained above for the '023 patent, including that the specification does not describe or enable a storage device policy as applied to a solid-state memory device. Instead it merely asserts that "the applicability to the concepts presented herein" as it relates to magnetic disks could also apply to solid-state storage media, without explaining how such concepts would translate to solid-state media even though the patent acknowledges that some magnetic disk features such as "the recording paths discussed may be inapplicable" to solid state memory
Claims 9-12: "receive a storage request comprising content and a storage device policy;"	There is a lack of written description and enablement for this claim term because the '553 patent's specification never describes an embodiment in which a storage request contains a storage device policy. Rather, every disclosed write sequence treats a previously received or updated policy as distinct from the subsequent request containing the content. *See generally* '553 patent, Figs. 8B-E, 9A-D, 10A-D, 11A-D. While the '553 patent describes that a storage request may include information in addition to the content (*e.g.*, "an identification code, encoding information, [or] data protection information," *id.*, 23:35-37), the '553 patent repeatedly distinguishes such request-specific information from the "storage device policy." *See id.*, 15:22-28; 18:60-19:1; 22:27-32; 23:31-49 (distinguishing a "specific instruction of write protection"

Claim Element	Section 112(a) Requirement
	delivered with content from an "overarching policy"). A POSITA would not be able to make and use claims 9-12 without undue experimentation, and the specification does not reasonably convey possession of this claim term. Claims 9-12 accordingly lack written description and enablement under 35 U.S.C. § 112(a).
Claims 1-4, 9-12: "a programmable processor operatively coupled to the device memory;"	There is lack of written description and enablement for this claim term because the specification does not disclose a "programmable processor operatively coupled to the device memory." Figure 6 depicts a "programmable logic device 605," but a programmable logic device is a hardware component (such as an FPGA), not a "processor" that executes software instructions. The specification describes the programmable logic device 605 as performing hardware functions such as "custom encryption through hardware" or serving as "a regular expression engine" (11:24-27), confirming its nature as a fixed-function hardware device. Moreover, Figure 6 shows device memory 135 as part of device controller 130, not as coupled to programmable logic device 605. The specification states that the programmable logic device 605 is "inserted directly into the data and/or control path" between the interface connector and device controller (11:20-21), not coupled to device memory for instruction retrieval and execution. A POSITA would not be able to make and use claims 1-4 and 9-12 without undue experimentation, and the specification does not reasonably convey possession of this claim term. Claims 1-4 and 9-12 accordingly lack written description and enablement under 35 U.S.C. § 112(a).
Claims 1-4, 9-12: "an application stored on the device memory and comprising instructions that, when executed by the programmable processor, direct the programmable processor to at least:"	There is lack of written description and enablement for this claim term because the specification does not disclose "an application stored on the device memory and comprising instructions … executed by the programmable processor." The programmable logic device 605 in Figure 6 is a hardware logic component, not a processor that retrieves and executes application instructions from device memory. The specification describes that the programmable logic device 605 is used for hardware-level processing such as encryption or pattern recognition, performed through hardware logic rather than through execution of software instructions stored in memory. Figure 6 shows device memory 135 integrated within device controller 130, not accessible to or coupled with programmable logic device 605 for instruction storage and execution. The specification's disclosure of software applications and instructions stored in memory relates to operation of the device controller 130 itself, not to a separate programmable processor executing instructions from device memory as claimed. A POSITA would not be able to make and use claims 1-4 and 9-12 without undue experimentation, and the specification does not reasonably convey possession of this claim term. Claims 1-4 and 9-12

Claim Element	Section 112(a) Requirement
	accordingly lack written description and enablement under 35 U.S.C. § 112(a).

Accordingly, all of the above claims and their dependent claims of the '553 patent fail to comply with 35 U.S.C. § 112(a) for lack of enablement and lack of written description and are invalid. Further, all of the above claims and their dependent claims *as a whole* fail to meet the enablement and written description requirements of 35 U.S.C. § 112(a). Each Asserted Claim of the '553 patent recites a combination of limitations including a "programmable processor operatively coupled to the device memory," "an application stored on the device memory comprising instructions ... executed by the programmable processor," a "storage device policy," and (for claims 9-12) "a storage request comprising content and a storage device policy." The specification, however, nowhere discloses or enables as an integrated system. The specification's only disclosure of a "programmable" element is the "programmable logic device 605" shown in Figure 6, which is a hardware logic component (such as an FPGA), not a software-executing processor coupled to device memory. The specification provides no disclosure of how an application stored in device memory would interact with a programmable processor to implement any storage device policy, let alone the full scope of policies claimed. A POSITA seeking to implement the claims would face undue experimentation because the specification provides no guidance on: (1) the specification discloses no "programmable processor" that executes stored application instructions—only a programmable logic device 605 that performs hardware-level functions through logic gates rather than software execution; (2) how an "application" stored in "device memory" could be "executed by" a programmable processor when the specification shows device memory 135 integrated within device controller 130, separate from programmable logic device 605; (3) how to receive a "storage request comprising

... a storage device policy" when every disclosed embodiment treats policy receipt as a separate operation from content storage requests; or (4) how to implement the genus of "storage device policies" across different storage media types. The breadth of the claims, combined with the absence of any enabling disclosure for the claimed combination of elements, renders the full scope of the claims unpredictable and would require undue experimentation to practice. Moreover, the specification does not reasonably convey that the inventors possessed the full scope of the claimed combination at the time of filing. The specification fails to describe any embodiment with a programmable processor executing application instructions from device memory, fails to describe any embodiment in which a storage request contains a storage device policy, and fails to describe representative species of the claimed "storage device policy" genus. The inventors' failure to describe how the claimed elements would function together or even to disclose a single embodiment containing all claimed elements, demonstrates that they did not possess the claimed invention. This includes that each and every Asserted Claim of the '553 patent is invalid for failure to comply with § 112(a).

3. The '715 Patent

The following claim terms fail the requirements of 35 U.S.C. § 112(a) and therefore render the Asserted Claims invalid. For example:

Claim Element	Section 112(a) Requirement
Claims 1 and 9: "storage policy"	There is a lack of written description and enablement for this claim term for the same reasons explained above for the term "storage device policy" of the '023 and '553 patents. The specification of the Asserted Patents draws no substantive distinction between the terms "storage policy" and "storage *device* policy," mentioning the former term only a single time and otherwise referring to the latter. '715 patent at 28:30-32 ("The storage device policy may be defined such that each object that is stored on storage media 110 may be handled independently, *i.e.* with its own distinct storage policy.").
Claims 1 and 9: "a programmable processor	There is a lack of written description and enablement for this claim term for the same reasons explained above for the '553 patent.

Claim Element	Section 112(a) Requirement
operatively coupled to the device memory;"	
Claims 1 and 9: "an application stored on the device memory comprising instructions that, when executed by the programmable processor, direct the programmable processor to:"	There is a lack of written description and enablement for this claim term for the same reasons explained above for the '553 patent.
Claim 9: "a data link to communicatively couple the programmable processor and the device controller"	There is a lack of written description and enablement for this claim term because the '715 specification fails to describe "a data link to communicatively couple the programmable processor and the device controller" that is mounted on a printed circuit board.

Accordingly, all of the above claims and their dependent claims of the '715 patent fail to comply with 35 U.S.C. § 112(a) for lack of enablement and lack of written description and are invalid. Further, all of the above claims and their dependent claims *as a whole* fail to meet the enablement and written description requirements of 35 U.S.C. § 112(a). Like the '553 patent, each Asserted Claim of the '715 patent recites a combination of limitations including a "programmable processor operatively coupled to the device memory," "an application stored on the device memory comprising instructions ... executed by the programmable processor," and a "storage policy." The specification, however, nowhere discloses or enables as an integrated system. A POSITA seeking to implement the claims would face undue experimentation because: (1) the specification discloses no "programmable processor" that executes stored application instructions—only a programmable logic device 605 that performs hardware-level functions through logic gates rather than software execution; (2) the specification discloses no embodiment in which device memory stores an application that is executed by a programmable processor; (3) the specification provides no guidance on implementing the full genus of possible policies; and (4) the specification fails to explain how all claimed elements would function together as a

system. The specification's disclosure amounts to nothing more than a wish or plan for implementing the claimed combination, not an enabling description that would allow a POSITA to make and use the invention without undue experimentation. Moreover, the specification does not reasonably convey that the inventors possessed the full scope of the claimed invention at the time of filing. The inventors described isolated components through generic functional language but failed to demonstrate possession of the claimed combination of a programmable processor, device memory storing application instructions executed by that processor, and a genus of storage policies. The absence of any working example, algorithm, or structural detail for the claimed system confirms that the inventors did not possess the claimed invention. This includes that each and every Asserted Claim of the '715 patent is invalid for failure to comply with § 112(a).

E. Invalidity for Unpatentable Subject Matter Under 35 U.S.C. § 101

The Asserted Claims of the Asserted Patents are also invalid under 35 U.S.C. § 101. Defendants set forth their subject matter eligibility contentions in the served Eligibility Contentions, pursuant to the Court's Standing Order Regarding Subject Matter Eligibility Contentions and the Docket Control Order.

IV. P.R. 3-4 DISCLOSURES AND CONTENTIONS

A. P.R. 3-4(a) Disclosures

Pursuant to P.R. 3-4(a), based on its investigation to date, Defendants have already produced and/or is producing documentation within its possession, custody, or control "sufficient to show the operation of any aspects or elements" of the Accused Instrumentalities identified by Gaea in its Infringement Contentions to the extent any such documentation is in the possession, custody, or control of Defendants. *See generally* production VOL 001. To be clear, defendant

Samsung Electronics America, Inc. is not aware of any responsive documents in its possession, custody, or control under P.R. 3-4(a); all such documents are solely those of defendant Samsung Electronics Co., Ltd.

Defendants reserve the right to supplement these disclosures with additional documentation.

B. P.R. 3-4(b) Disclosures

In accordance with P.R. 3-4(b), Defendants are producing a set of all prior art references identified in these Invalidity Contentions. *See* production Volume 002. Defendants are also producing prior art references concerning each item of prior art systems and methods. Any prior art references not in English are produced with an English translation of at least the portion(s) relied upon. These prior art references are cited herein and support the contentions presented. In addition, physical exhibits of prior art systems and methods will be made available for inspection at a mutually-agreeable time and location. Defendants reserve the right to produce a certified translation of any prior art references at a later time.

Defendants' search for prior art references, additional documentation, and/or corroborating evidence concerning prior art apparatuses and methods is ongoing. Accordingly, Defendants reserve the right to supplement its production, as provided by the local rules, as additional prior art references, additional documentation, and/or corroborating evidence concerning prior art documents/apparatuses, and methods are obtained during the course of discovery.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via email on August 31, 2026.

/s/ Stuart W. Yothers
Stuart W. Yothers