

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD.,
Petitioner

v.

WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY
TECHNOLOGY CO., LTD.
Patent Owner.

Case No. IPR2026-00485
U.S. Patent No. 11,257,891

**DECLARATION OF DR. MICHAEL LEBBY
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,257,891**

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I. INTRODUCTION

1. I have been retained by Samsung Display Co., Ltd. (“Samsung” or “Petitioner”), as an independent expert in this proceeding before the Patent Trial and Appeal Board (“PTAB” or “Board”). I understand that Samsung is requesting that the Board institute an *inter partes* review (“IPR”) proceeding of U.S. Patent No. 11,257,891 (“the ’891 Patent”) (Ex-1001), currently assigned to Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd. (“Patent Owner” or “PO”).

2. I am not and have never been an employee of Samsung. I am being compensated at my usual and customary rate of \$650 per hour. No part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding.

3. I have been asked to provide my independent analysis of the ’891 Patent in light of the prior art publications cited below. I have also been asked to consider the state of the art and prior art available as of June 7, 2018. Based on the prior art discussed in this declaration, it is my opinion that Claims 1-18 of the ’891 Patent are unpatentable for the reasons provided below.

A. Qualifications

4. I have summarized in this section my educational background, career, publications, and other relevant qualifications. My full curriculum vitae is attached as Ex-1003 to this Declaration.

5. I received a Bachelor of Engineering degree in Electrical and Electronic Engineering in 1984 from the University of Bradford, UK. I then took an MBA in 1985. I also received a Ph.D. in Semiconductor Physics in 1987 from the University of Bradford, UK. I was awarded a Doctor of Engineering degree with a focus in optoelectronics in 2004 from the University of Bradford, UK.

6. As described in this Section, and further detailed in my curriculum vitae (Ex-1003), over the course of my 40-year career in electronics and optoelectronics, I have worked in nearly every aspect of the electronic and optoelectronics business, ranging from epitaxial wafer growth (compound semiconductors), electrical and optoelectronic device and circuit design, using modeling and simulation, electrical and optoelectronic device and component fabrication, testing, and qualification, to the implementation of devices into packages and panels, both hermetic and non-hermetic, as well as analysis of package/panel materials such as plastics (including plastic housings such as resin-packaged lead frame housings), optical plastics, metallic-based packages, semiconductor-based packages, and ceramic-based packages. I have also designed device and display packages (through-pin, surface

mount, flip-chip, and various combinations thereof) for printed circuit board mounting. Many of the designed packages were implemented into electronic and optoelectronic modules/panels and sub-system/luminaire applications that included various electronics designs. The modules/panels have been at least fiber-optic-, display-, lighting-, imaging-, sensing-, power-, and RF-based. I have also worked in commercially based industrial research-and-development laboratories to bring new electronic, optoelectronic-, display-, and photonic- based technologies from the research proof-of-concept phase through prototyping and qualified manufacturing for volume release. This has included both transfer as well as injection molding techniques for packaging.

7. I have been both an entrepreneur (e.g., Ignis Optics Inc, One Chip Photonics, Lightwave Logic Inc.), as well as an intrapreneur (e.g., Motorola, Intel, TE Connectivity (previously Tyco Electronics), AT&T Bell Labs), creating innovative new programs, both as venture backed start-ups as well as corporate funded divisions. I have built these entities to develop electronic, optoelectronics, and photonics technology from the laboratory and fabrication clean room to production factories.

8. I received a Bachelor of Electrical Engineering degree in 1984, a Master of Business Administration in 1985, and a Doctorate degree in 1987, all from University of Bradford in the United Kingdom. My Ph.D. thesis involved the design

and fabrication of both optoelectronic and electronic compound semiconductor devices (such as GaAs, InP etc.), and their associated characterization. In 2004, I was awarded a Doctor of Engineering degree (a higher doctorate degree) from University of Bradford for my technical contributions to the field.

9. My career started in the late 1970s at the Ministry of Defense in the UK where I spent time at their R&D facility in Malvern (RSRE – Royal Signals and Radar Establishment). I worked on electronic and optoelectronic semiconductor device design, fabrication, and characterization, and especially materials using III-V compound semiconductors such as GaAs and InP. These devices included electronic transistors, optical waveguides, and optoelectronic device operation. My research work in semiconductor device design then took me to AT&T Bell Laboratories in 1985, where I pursued research in novel opto-device designs using III-V semiconductor material systems that included FETs, bipolar transistors, optical waveguides, optics, LEDs, laser diodes, and photodetectors. The devices researched became, in part, the subject of my PhD thesis that was granted in 1987.

10. I moved to Motorola in 1989 to further develop my electronic, optoelectronic, semiconductor and display engineering and development skills, and I became a Research and Development Manager in Motorola, until I left the company in 1998. During my time at Motorola, I worked on many photonic, electronic, display and optical technology projects that included optical lenses,

display, imaging, camera, fiber-optic optical interconnects, electronic circuits (both analog and digital), displays, LEDs, OLEDs, and laser devices, as well as the packaging and reliability of mobile product prototypes. At that time, I was particularly interested in miniature displays/panels and miniature optics using a number of technologies such as LEDs, lasers, LCDs, lenses, and organic LEDs which were aimed towards (at the time) pagers, mobile phones, micro-imagers/displays, holograms, and advanced prototypes of futuristic communications hardware. I was also particularly interested in miniature color displays in which LEDs/OLEDs could be utilized, and the associated drive and processing electronics for them. One interesting patent I was a co-inventor on is called an Electronic Book which was filed in 1994 (US. Patent Number 5.534,888). This invention relates, in general, to optical displays and, more particularly, to optical displays in electronic books and was an early patent in the field of electronic books.

11. In aiming for miniature full color displays and associated optics, the early 1990s, there was only red wavelength Phosphide (GaAsP and/or InGaAlP) and AlGaAs based LED technology that was advanced in technology and performance. Green wavelength Gallium Phosphide based LEDs had low emission output, and blue wavelength emission LEDs were only available using pure Silicon Carbide on Silicon Carbide substrate wafers, with very low emission output. I worked closely with Motorola's mobile divisions on new and novel display prototypes for mobile

phones etc., and optics to research and develop how best to innovate with full color red, green, and blue displays and associated electronics. A number of alternative technologies were evaluated, such as LCD (Liquid Crystal Displays), OLED (organic LEDs), and Gallium Nitride and Indium Gallium Nitride materials grown onto Sapphire. I also explored the electronic circuits that were needed to drive, operate, and signal these types of optoelectronic displays.

12. During my time at Motorola as a Research and Development Manager, I designed optical and electrical packages/panels for these displays and devices, which included standard TO- cans, over-molded plastic DIL solutions, and ceramic-based and semiconductor-based technology.

13. The compound semiconductors used in the early 1990s at Motorola corporate research, for which I was a Research and Development Manager, included the Group III-V materials system, Group IV material system, Group VI material system, and Group III-N material system. A number of these materials included: GaAs, InP, GaN, GaP, InGaAlP, and silicon, amongst other materials, all of which were intended to be designed into various light emitting sources, detectors, and electronics in their associated optical package platforms that included optics and lens design. The research work at Motorola also included work on displays and, in particular, miniature displays and optics for pagers, clam-shell phones, and head-mounted displays that included mounting onto eyeglasses (similar in concept to

Google glass™). The types of displays ranged from large arrays of visible LEDs (i.e., 10,000 LEDs on a chip) that required custom LED packaging to tiny color LCDs, where work was conducted into approaches to efficiently optically package the displays as well as OLEDs, even though the technology was not mature. At the time, I explored less corrosive metallization for OLED displays as well as approaches in the fabrication processing to improve brightness and lifetime of OLED materials. On-board integrated LED driver electronic circuits were implemented in some of the prototypes. Some of the research work at Motorola utilized phosphor technology, especially for display projects that were based on field emission (i.e., the field emission display (FED)), as well as arrays of visible LED/OLED displays and optics where a full color gamut was required by both internal and external customers. The phosphor technology performed down-conversion of light energy.

14. I also initiated Motorola's work in optical interconnect (Optobus™) technology, that incorporated both transfer and injection molded optical parts. This project involved the research and development of a multi-channel electronic IC chip for parallel optical interconnect.

15. I was one of Motorola's most prolific inventors, having over 150 issued utility patents as an inventor or a co-inventor by the late 1990s. Many of the photonics, electronics, and optical/display prototypes with which I was involved

were subject to reliability and stress testing that included humidity, temperature, optical, mechanical, and electrical evaluation. These consumer products all were driven using standard electronic ICs and electronic signaling where I had a role in design and simulation of these circuits.

16. I filed my first GaN patent, which taught techniques using GaN and InGaN LEDs, in 1996, shortly after the invention of high performance GaN/InGaN blue LEDs by Nichia in the early 1990s. My work at Motorola addressed, in part, the big issue at the time in the mid-1990s: full color display and display electronics composed of red, green and blue LEDs that could be utilized in mobile products as well as other applications. As part of this work, I was engaged in how to optically package these technologies that allowed for electrical, optical, and thermal high performance. Examples of patents on which I am a co-inventor, with respect to high heat conductivity surface emitting optical devices, include, for example, U.S. Patent No. 5,538,919, as well as U.S. Patent No. 5,818,404, U.S. Patent No. 5,739,800, and U.S. Patent No. 5,838,703, which three patents address LED packaging solutions.

17. Another of my inventions was directed to a new semiconductor laser that had the potential to be manufactured in high volume. This device was called a VCSEL (vertical cavity surface emitting laser), and the invention was to optimize the performance using an oxide process, and is now the basis for the highest volume semiconductor laser today (with its recent implementation as a structured light

sensor in facial recognition systems utilized in modern day smart mobile phones). The VCSEL is a surface emitting diode laser and operates in a similar fashion to most LED chips today. Some of the goals of the research work at Motorola was to be able to optically package VCSEL laser diodes and their associated optical lenses in a similar approach to LEDs as well as drive them using novel electronic circuits. Laser diodes require thermal issues to be addressed very carefully, as they develop significant levels of heat during operation. The optical package designs at the time (including for lasers and LED packages) took into account optical lensing, thermal heat sinking and thermal paths to take the heat away from the source. My additional patents, including during my time at Motorola, are listed in my curriculum vitae (Ex-1003).

18. Between 1998 and 1999, I worked as the Director of Technology/ BD (Fiber Optics) for Tyco Electronics (previously AMP). I joined Tyco Electronics as a member of the Global Optoelectronics Division's management team. I was responsible for growing the optoelectronics and optical business through external interactions that included mergers, acquisitions, strategic alliances, and technical strategic planning. Much of that work was laser-and LED-based, with associated optics, and included designing and characterizing laser- and LED-based optical packages and modules for customer qualification specifications.

19. In 1999, I left Tyco and started employment at Intel. At Intel, I was involved heavily in photonic technology, especially technology that supported silicon photonic device platforms. As a culmination of this work, I was one of Intel's founders of its silicon photonics division in the year 2000, and worked to set up a fabrication facility in South San Jose. The work involved integrating silicon FET electronics with optoelectronics and optics onto the same silicon semiconductor wafer. I was also part of Intel Capital's optical investment team, and participated in over 30 photonics investments into photonics, optics, and optoelectronics. Focus included optical devices, packaging and modules. Technologies investigated included lasers, LEDs, optics, and optical displays.

20. At the end of 2000, I left Intel and raised venture capital funding for a company called Ignis Optics Inc. The main goal of the company was to design and manufacture, in high volume, very high-performance fiber optic transceiver modules, and associated optics with data rates up to OC-192, or approximately 10 Gbps. The fiber optic transceiver modules have the capability of transmitting and receiving optical signals that are controlled using programmable electronics and packaged optoelectronics chips, such as laser diodes, optical lenses, and photodetectors.

21. In 2005, I took up employment for a trade association, based in Washington, D.C., called IEEE Optoelectronics Industry Development Association

(OIDA). As head of this trade association, and with photonics and optics manufacturers that included fiber optics, display, cameras, sensing, defense, aerospace, LED lighting, OLED displays (including flexible), and automotive vendors as members, I was responsible, in part, for industry-based technology roadmaps; and I implemented common industry roadmap methodologies with common features such as “Red Brick Walls” and transferred them into optoelectronics roadmaps for the industry in which displays as well as LEDs, OLEDs, fiber-optics, optics, fiber, cameras, optical sensors, projection techniques, and their associated packaging, were featured. OIDA roadmaps featured purple brick walls, to show differentiation from the semiconductor industry.

22. In 2010, I became the General Manager and CTO of Translucent, Inc., a high-tech start-up company which developed and manufactured silicon and rare earth oxide based epitaxial semiconductor wafers. One of the key drivers at Translucent was to develop a new and novel platform for the growth of GaN and InGaN onto silicon for low-cost LED, RF FET, and power FET manufacturing on larger format substrate wafers (e.g., 200mm), in order to achieve economies of scale and lower chip costs. Translucent pioneered the deposition of single crystal rare earth oxides such as Erbium Oxide (ErOx), Gadolinium Oxide (GdOx), Neodymium Oxide (NdOx), etc., that, when grown, single crystal layers of GaN/InGaN/AlN could be grown on top of them. This allows a lattice-matched, and monolithic-based,

wafer template to be manufactured for both FET and LED fabrication. While at Translucent, I researched various epitaxial semiconductor layer structures that utilized rare earth oxide technology in order to improve the performance of FETs and LEDs. Other material growth work at Translucent focused on the growth of Silicon Germanium (SiGe) compounds with rare earth oxides, and various crystal orientation wafer substrates. I patented a number of electronic FET device designs using rare earth oxides while employed at Translucent.

23. I am currently Chief Executive Officer (CEO) and Chief Technology Officer (CTO) of GenusTechnik Inc. GenusTechnik Inc. is my consulting company, through which I engage in my expert witness work.

24. I recently retired as Chairman and CEO of Lightwave Logic Inc. (NASDAQ:LWLG), where I served as a Director of the Board of Directors. Lightwave Logic is a company that is developing electro-optical polymer materials for a number of data-rich industries.

25. Throughout my career, I have also had an active role in a number of technical professional organizations, including, among others, IEEE Components, Packaging, and Manufacturing Technology (CPMT), IEEE Electronic Components and Technology Conferences (ECTC); IEEE TC-10 (Technical Committee on Optoelectronics), and IEEE Optoelectronics Industry Development Association (OIDA). Through these organizations, I have consistently been a part of committees,

events, and workshops relating to semiconductor, optoelectronics, electronics, and packaging technology. I am currently at the grade of Fellow of the IEEE, Optica and National Academy of Inventors (NAI).

26. I also serve as a Technical Expert/Consultant for the European Commission. In my work at the European Commission, I review and advise on general electronics, semiconductors, photonics, optoelectronics, imaging, sensing, display (LCD, LED, OLED, flexible displays etc.), and related ICT (Information and communications technology) technology.

27. My work has also led to over 225 USPTO utility patents in semiconductors, electronics, optics, displays, and optoelectronics, including a number of patents relating to display technology. I am the author of more than 60 publications and over 300 media events/talks etc.

B. Materials Considered

28. In forming my opinions, I reviewed the following documents, in addition to others I have cited in my declaration. I also relied on my own knowledge of and experience in electronics, photonics, semiconductors, displays, as well as materials and mechanical/back-end assembly/manufacturing of innovative products in the display sector. These include the design and/or development of display devices in consumer electronics and familiarity with OLED displays, flexible display panels, display module structures, adhesives, and/or packaging technologies:

Ex. No.	Description
Ex-1001	U.S. Patent No. 11,257,891 (“the ’891 Patent”)
Ex-1004	Prosecution History of U.S. Patent No. 11,257,891
Ex-1005	U.S. Patent No. 9,780,157 (“Kwon”)
Ex-1006	U.S. Patent No. 10,651,261 (“Kang’261”)
Ex-1007	U.S. Patent Publication No. 2017-0287937 (“Ka”)
Ex-1008	Korean Patent Publication No. 2017-0103740
Ex-1009	Certified translation of Korean Patent Publication No. 2017-0103740
Ex-1010	INTENTIONALLY LEFT BLANK
Ex-1011	INTENTIONALLY LEFT BLANK
Ex-1012	INTENTIONALLY LEFT BLANK
Ex-1013	INTENTIONALLY LEFT BLANK
Ex-1014	INTENTIONALLY LEFT BLANK
Ex-1015	INTENTIONALLY LEFT BLANK
Ex-1016	INTENTIONALLY LEFT BLANK
Ex-1017	INTENTIONALLY LEFT BLANK
Ex-1018	INTENTIONALLY LEFT BLANK
Ex-1019	INTENTIONALLY LEFT BLANK
Ex-1020	Claim mapping table for the ’891 Patent
Ex-1021	Chinese Patent No. 205140985U
Ex-1022	U.S. Patent No. 12,238,996 to Park (“Park’996”)

Ex. No.	Description
Ex-1023	U.S. Patent No. 9,627,463 to Kwon (“Kwon’463”)
Ex-1024	U.S. Patent No. 10,762,838 to Kang (“Kang’838”)
Ex-1025	U.S. Patent No. 10,424,631 to Kim (“Kim’631”)
Ex-1026	U.S. Patent No. 10,803,792 to Kim (“Kim’792”)
Ex-1027	U.S. Patent No. 9,349,758 to Ki (“Ki”)
Ex-1028	U.S. Patent No. 9,356,087 to Kee (“Lee’087”)
Ex-1029	U.S. Patent Publication No. 2015/0382446 to Kwon (“Kwon’446”)
Ex-1030	U.S. Patent Publication No. 2015/0187279 to Lee (“Lee’279”)
Ex-1031	U.S. Patent Publication No. 2017/0358641 to Park (“Park’641”)
Ex-1032	U.S. Patent Publication No. 2018/0337226 to Liu (“Liu’226”)
Ex-1033	WIPO Publication No. 2017/177127A1 to Shyu (“Shyu”)
Ex-1034	U.S. Patent Publication No. 2018/0204895 to Lin (“Lin’895”)
Ex-1035	Gregory P. Crawford, Flexible Flat Panel Displays, Wiley Series in Display Technology (2005) (“Crawford”)

II. LEGAL STANDARDS

29. In forming my opinions and considering the subject matter of the ’891 Patent and its claims in light of the prior art, I am relying on certain legal principles that counsel in this case explained to me. My understanding of these concepts is summarized below.

30. I understand that earlier publications and patents may act to render a patent unpatentable for one of two reasons: (1) anticipation, and (2) obviousness.

A. Anticipation

31. As explained to me by counsel, it is my understanding that the claims of a patent are anticipated by a prior art reference if each and every element of the claim is found either explicitly or inherently in the reference. I understand that inherency requires a showing that the missing descriptive matter in the claim is necessarily present in the allegedly anticipating reference, and that it would have been so recognized by a person of ordinary skill in the art (“POSITA”).

32. I understand that when a challenged claim covers several structures, either generically or as alternatives, the claim is deemed anticipated if any of the structures within the scope of the claim is found in the prior art reference.

33. Although anticipation typically involves the analysis of a single prior art reference, I understand that additional references may be used to show that the prior art reference has enabling disclosure (i.e., allows a POSITA to make the invention without undue experimentation), to explain the meaning of a term used in the prior art reference, and/or to show that a characteristic is inherent in the prior art reference.

B. Obviousness

34. As explained to me by counsel, I understand that a claim is invalid as obvious if it would have been obvious to a person of ordinary skill in the art at the time the alleged invention was made. This means that even if all of the elements of the claim cannot be found in a single prior art reference that would anticipate the claim, a person of ordinary skill in the art who was aware of the prior art would have been able to come up with the claimed invention. This may be the case, for example, where the missing element represents only an insubstantial difference over the prior art or a reconfiguration of a known system. I understand that in an obviousness determination, the person of ordinary skill in the art is presumed to have knowledge of all material prior art.

35. I understand that an obviousness analysis requires an understanding of the scope and content of the prior art, any differences between the alleged invention and the prior art, and the level of ordinary skill in evaluating the pertinent art.

36. I understand that when a product is available, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill in the art can implement a predictable variation, obviousness likely bars its patentability. For the same reason, if a technique has been used to improve one device and a person of ordinary skill in the art would recognize

that it would improve similar devices in the same way, using the technique would have been obvious.

37. I understand that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art at the time of the alleged invention. I have been told that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I have been told that the inferences and creative steps a person of ordinary skill in the art would employ are relevant to the determination of obviousness.

38. I understand that one may consider, e.g., whether (1) the change was merely the predictable result of using prior art elements according to their known functions, or whether it was the result of true inventiveness; (2) there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; (3) the claimed innovation applies a known technique that had been used to improve a similar device or method in a similar way; (4) the claimed invention would have been obvious to try, meaning that the claimed innovation was one of a relatively small number of possible approaches to the problem with a reasonable expectation of success by those skilled in the art; (5) the

invention merely substituted one known element for another known element in order to obtain predictable results; (6) the invention merely applies a known technique to a known device, method, or product to yield predictable results; or (7) known work in one field of endeavor may have prompted variations of it for use in either the same field or a different one based on design incentives or other market forces that would have been predictable to a person of ordinary skill in the art.

39. I further understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of the invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I understand that there must be a nexus—that is, a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

40. I am not aware of any allegations by the named inventors of the '891 Patent or any assignee of the '891 Patent that any secondary considerations tend to rebut the obviousness of the '891 Patent.

41. Additionally, I understand that in considering obviousness, it is important not to use the benefit of hindsight derived from the patent under consideration.

C. Level of Ordinary Skill in the Art

42. When interpreting a patent, I understand that it is important to identify the relevant art pertaining to that patent, as well as the level of ordinary skill in that art at the time of the claimed invention. The “art” is the field of technology to which the patent is related.

43. I am informed and understand that the POSITA is a hypothetical person who is presumed to know the relevant prior art. I understand that the actual inventor’s skill is not determinative of the level of ordinary skill. I further understand that factors that may be considered in determining level of skill include: (i) the types of problems encountered in the art; (ii) prior art solutions to those problems; (iii) the rapidity with which innovations are made; (iv) the sophistication of the technology; and (v) the educational level of active workers in the field. I understand that not all such factors may be present in every case, and one or more of them may predominate.

44. I understand that a POSITA is one who is presumed to be aware of all pertinent art, thinks along conventional wisdom in the art, and is a person of ordinary creativity.

45. A person of ordinary skill in the art at the relevant time (“POSITA”), which I have been told to consider as of May 20, 2021 would have had at least a bachelor’s degree in electrical engineering, materials science, mechanical engineering, or a related field, and two years of experience in the design and/or development of display devices in consumer electronics, including familiarity with OLED displays, flexible display panels, display module structures, adhesives, and/or packaging technologies. A higher level of education or skill might make up for less experience, and vice versa.

46. Based on my knowledge, skill, and experience, I have an understanding of the capabilities of a person of ordinary skill in the relevant art. For example, from my industry experience, I am familiar with what an engineer designing innovative flexible display and associated electronics, photonics, and materials technologies into a consumer product for high volume manufacturing would have known and found predictable in the art. From teaching and supervising my post-graduate students, I also have an understanding of the knowledge that a person with this academic experience possesses. Furthermore, I possessed the knowledge of a POSITA myself at least as of 1990.

D. Claim Construction

47. I understand that the United States Patent and Trademark Office interprets claim terms in an *inter partes* review proceeding under the same claim

construction standard that is used in a United States federal court. I understand that under this standard, the meaning of claim terms is considered from the viewpoint of a POSITA at the time of the alleged invention.

48. I have been informed that claim terms are generally given their ordinary and customary meaning as understood by one of ordinary skill in the art in light of the specification and the prosecution history pertaining to the patent. I understand, however, that claims terms are generally not limited by the embodiments described in the specification.

49. I understand that in addition to the claims, specification, and prosecution history, other evidence may be considered to ascertain the meaning of claim terms, including textbooks, encyclopedias, articles, and dictionaries. I have been informed that this other evidence is often less significant and less reliable than the claims, specification, and prosecution history.

III. SUMMARY OF GROUNDS

50. I understand that Petitioner challenges the validity of Claims 1-18 of the '891 Patent. It is my opinion that the following grounds demonstrate that the claims of the '891 Patent are invalid.

Ground	Summary
1	Claims 1, 7, and 10 are obvious over Kwon (Ex-1005)

Ground	Summary
2	Claims 3, 11, and 16 are obvious over Kwon and Kang'261 (Ex-1006)
3	Claims 2, 4-6, 8-9, 12-15, and 17-18 are obvious over Kwon, Kang'261, and Ka (Ex-1007)

IV. TECHNOLOGY BACKGROUND

A. Display Panels Having An Active Region and A Non-Display Region Disposed Around The Active Region and Extending to Form A Bending Region, A Fanout Routing Region, and A Component Disposing Region Were Known

51. Display panels having an active region and a non-display region disposed around the active region and extending to form a bending region, a fanout routing region, and a component disposing region were well known by 2018. This part of the technology background establishes that architectural layouts and interconnects for bendable display panels were already known to a POSITA by 2018 through many pieces of prior art. In particular, various parts of the display can be viewed from the perspective of: (1) panel layout, substrate zoning where a substrate in a bendable display can be divided into an active display areas and a surrounding inactive or peripheral area; (2) inactive areas that include (a) fan-out and routing area, (b) bending and bend allowing area, (c) component disposing and pad area; (3) mechanical and routing stress engineering, (4) packaging with pad level interconnections, and (5) active area signal routing layouts. For example, U.S. Patent No. 12,238,996 to Park (Ex-1022, "Park'996") teaches a display device, which

“includes a substrate including a display area and a peripheral area disposed around the display area,” wherein “[t]he peripheral area includes a bending region and a contact region adjacent to the bending region.” Ex-1022, Abstract. Specifically, Park’996 teaches that “display panel 100 includes a display area DA within which an image is displayed, and a peripheral area PA, in which an image is not displayed” that “surround[s] the display area DA” and includes “various elements and/or signal lines that are used to generate and/or transmit various signals applied to the display area DA.” Ex-1022 (Park’996), 3:20-28; *see also id.*, 4:19-26 (“bending region BA, for example, may be disposed at the peripheral area PA between the display area DA and the pad portion PP,” “extends across the display panel 100 in the first direction D1,” and “display panel 100 is bent in the bending region BA such that the pad portion PP is separated from the display area DA by the bending region BA”). Moreover, Park’996 teaches that “the first portion 61a of the first connection line 60a and the first portion 61b of the second connection line 60b are formed with the different layers, and they may be disposed to cross each other in the region (e.g., a fan-out region).” Ex-1022 (Park’996), 8:64-9:13, Fig. 1. This is also taught by U.S. Patent No. 9,627,463 to Kwon (Ex-1023, “Kwon’463”). Kwon’463 teaches that a flexible display that “includes a flexible base layer defined with a display area and a non-display area.” Ex-1023 (Kwon’463), 2:22-24. Kwon’463 further teaches that “the flexible display 100 includes at least one active area (i.e., display area), in which

an array of display pixels are formed therein,” “[o]ne or more inactive areas ... at the periphery of the active area” that “surrounds a rectangular shape active area.” Ex-1023 (Kwon’463), 4:10-27. Kwon’463 also teaches that “[i]n embodiments where a non-display area at the edge of the flexible display 100 is bent, the increase in the routing area for accommodating the wire traces can actually increase the size of the inactive area to be hidden under a masking.” Ex-1023, 23:29-35; *see also id.*, 26:57-64. “In addition to the bend allowance section, in some embodiments, the patterned insulation layer may also be provided in the routing area between the active area and the bend allowance section as well as the routing area between the COF bonding area and the bend allowance section.” Ex-1023 (Kwon’463), 25:67-26:5.

52. *See also, e.g.*, Ex-1024 (Kang’838), Abstract, 4:26-50 (“In the inactive area N/A, an image is not displayed and various wiring lines and circuits for driving a display element of the active area A/A are disposed. ... The inactive area N/A may be ... an area surrounding the active area A/A. The inactive area N/A includes a first inactive area NA1, a bending area BA, a second inactive area NA2, and a pad area PA. ... The bending area BA extends from the first inactive area NA1 and may be bent. The second inactive area NA2 extends from the bending area BA and the pad area PA extends from the second inactive area NA2. In the pad area PA, a pad to be connected to a driver IC 112 is disposed.”), 5:40-63 (“The plurality of bending patterns BP is disposed in a center portion of the bending area BA. ... Further, even

though the plurality of bending patterns BP is disposed in the bending area BA in FIG. 1, the plurality of bending patterns BP may be disposed to extend from the bending area BA into the first inactive area NA1 and/or the second inactive area NA2, but is not limited thereto”), Figs. 5B-5C; Ex-1025 (Kim’631), Abstract (“A display device includes a substrate including a bending area located between a first area and a second area. ... A first wiring unit including a plurality of first wirings is arranged on the substrate to sequentially extend over the first area, the bending area, and the second area.”), 2:25-30, 4:17-26, 17:8-23, Fig. 2; Ex-1026 (Kim’792), 1:66-2:9 (“a display device including a display panel that includes a display area including a plurality of pixels and a first peripheral area adjacent to the display area,” which “include[s] a bendable region extending across the display panel and a plurality of signal lines partially included in the bendable region”), 2:35-41, 2:64-3:10, 4:44-57, 7:28-40, 8:31-38, 8:44-49; Ex-1027 (Ki), 4:4-11, 24:57-61 (“the patterned insulation layer may also be applied in the routing area between the active area and the bend allowance section”), 27:1-12; Ex-1028 (Lee’087), 3:24-31, 4:66-5:6, 7:1-14 (“the matrix of pixels in the secondary active area of the bend portion may be continuously extended from the matrix of the pixels in the active area of the central portion” or “the secondary active area within the bend portion and the active area within the central portion of the flexible display 100 may be separated apart from each other by the bend allowance section of the flexible display 100” and “[s]ome components

in the central portion and the bend portion can be electrically connected via one or more conductive line 120 laid across the bend allowance section of the flexible display 100”), 28:55-63, Figs. 1, 15A; Ex-1029 (Kwon’446) ¶¶7, 14, 29; Ex-1030 (Lee’279), Abstract, ¶¶11, 32, 67, 69, 84-85, 88, 144, 159, Fig. 4; Ex-1031 (Park’641), Abstract, ¶¶7, 27, 33, 53, 62, Fig. 1; Ex-1032 (Liu’226) ¶¶7, 27, 30, 100, 125; Ex-1033 (Shyu) ¶¶28-29, 32-33, 36-37, Figs. 2, 7, 22-23; Ex-1034 (Lin’895) ¶¶44, 46-47, 69, 77, 82-84, 112, Figs, 10, 30; Ex-1035 (Crawford), 1 (“Flexible flat panel display technologies offer many potential advantages, such as very thin profiles, lightweight and robust display systems, the ability to flex, curve, conform, roll, and fold a display for extreme portability, high-throughput manufacturing, wearable displays integrated in garments and textiles, and ultimate engineering design freedom (e.g. odd-shaped displays).”).

53. It was also well known by 2018 that the component disposing region may have a plurality of component connecting pads. For example, Park’996 teaches that “[i]n the peripheral area PA of the display panel 100, a pad portion PP” is disposed, which receives “the signals from an external source” and is attached to “[a] printed circuit film,” and “bumps of the printed circuit film may be electrically connected to pads P of the pad portion PP.” Ex-1022 (Park’996), 3:44-48. Moreover, Kwon’463 teaches that “some of the components, such as data drive-IC, may be mounted on a separate printed circuit and coupled to a connection interface

(Pads/Bumps) disposed in the inactive area using a printed circuit film such as flexible printed circuit board (FPCB), chip-on-film (COF), tape-carrier-package (TCP) or any other suitable technologies” and “the inactive area with the connection interface can be bent away from the plane of the adjacent portion of the flexible display so that the printed circuit film (e.g., COF, FPCB and the like) is positioned at the rear side of the flexible display 100.” Ex-1023 (Kwon’463), 4:36-49. Kwon’463 further teaches that “[t]he wire trace, which is provided with the reinforced portion at the stepped areas, may extend across the bend allowance section and routed to pads for COF or other components of the flexible display 100.” Ex-1023 (Kwon’463), 28:14-26, Figs. 1, 13A.

54. *See also, e.g.*, Ex-1024 (Kang’838), 5:40-63 (“The first connection line CL1 is disposed in the center portions of the pad area PA and the second inactive area NA2. The first connection line CL1 is connected to a pad connected to the driver IC 112 and transmits power voltage to the plurality of bending patterns BP disposed in the bending area BA.”); Ex-1025 (Kim’631), 5:5-19 (“A pad unit 500 may overhang an edge of the substrate 100. A separate chip may be attached to the pad unit 500. The pad unit 500 may include a first pad unit 510 and a second pad unit 520. The first wiring unit 300 may be connected to the first pad unit 510, and the second wiring unit 400 may be connected to the second pad unit 520. A signal applied to the pad unit 500 may be provided to the display 200.”), Cl. 16; Ex-1026

(Kim'792), 16:32-46 ("the signal lines 10, 20, 30, 40, 50, and 60 disposed in the bending region (BDA) may extend downward from the bending region (BDA) to form a pad (PAD), or signal pad, corresponding to end portions of the signal lines" and "[t]he pad (PAD) may be connected to a printed circuit film on which driving circuit chips are mounted" and "to a plurality of electrical nodes in the display area (DA) by the plurality of signal lines (SL)"), 19:62-20:3, Fig. 5; Ex-1027 (Ki), 4:30-44 ("some of the components ... may be ... coupled to a connection interface (Pads/Bumps) disposed in the inactive area"), Figs. 1, 12A; Ex-1028 (Lee'087), 5:16-37, 19:33-48 ("a pad for receiving one or more signals may be provided on one end of the conductive lines"); Ex-1029 (Kwon'446) ¶31, Figs. 1A-1B; Ex-1031 (Park'641) ¶28; Ex-1032 (Liu'226) ¶¶104, 113, Fig. 1; Ex-1034 (Lin'895) ¶82; Ex-1035 (Crawford), 304 ("The row and column patterning was such that all the traces of each type are extended beyond the active area of the device and then merged into a single contact pad or shorting bar.").

B. Display Panels Wherein A First Section of A First Power Trace Is Disposed Within the Non-Display Region Around the Active Region and Connected to A Second Section of the First Power Trace Disposed Within the Component Disposing Region Were Known

55. Display panels wherein a first section of a first power trace is disposed within the non-display region around the active region and connected to a second section of the first power trace disposed within the component disposing region were

well known by 2018. This part of the technology background focuses on demonstrating that a segmented power trace interconnect from an active display area that reaches across a bending zone, and ends into a component and pad area was already known to a POSITA by 2018 through prior art. In particular, a bendable display can be viewed as: (1) architecture that segments power routing; (2) bridging a bending region, (3) the use of guard rings, perimeters and grid-like patterns for trace topology design, and (4) terminal interfacing with component pads. For example, Park'996 teaches that "[t]he signal line transmitting the common voltage ELVSS may extend to enclose the left side, the upper side, and the right side of the display area DA" functioning "as a guard ring"; "[t]he signal line transmitting the gate low voltage VGL is connected to the gate drivers 400a and 400b and may be used to generate a low voltage level of the gate signal in the gate drivers 400a and 400b"; and "[t]he signal line transmitting the initialization voltage Vint is connected to an initialization voltage transmitting line disposed in the display area DA to transmit the initialization voltage Vint" and "may be used to drive the pixel PX." Ex-1022 (Park'996), 5:42-53; *see also id.*, 6:34-46. Park'996 further teaches that "parts of the signal lines" are "disposed in the first and second contact regions CA1 and CA2 of the upper side and the lower side of the bending region BA" and the "part of the signal line disposed at the bending region BA and the contact regions CA1 and CA2 is referred to as a connection line," which "includes first connection

lines 60a and second connection lines 60b ... alternately arranged in the first direction.” Ex-1022 (Park’996), 6:66-7:10, Fig. 2. Moreover, Park’996 teaches that “first connection line 60a includes a first portion 61a,” which “extends from the first contact region CA1 to the upper side of the first contact region CA1 (in the direction D2) ... from the peripheral area PA of the display panel 100 and may connect with the element transmitting the above-described signals”; “a second portion 62a ... disposed throughout the first contact region CA, the bending region BA, and the second contact region CA”; and “a third portion 63a,” which “extends from the second contact region CA2 to the lower side of the second contact region CA2 (in the opposite direction to D2)” and “may be connected to a pad P of the pad portion PP.” Ex-1022 (Park’996), 7:11-27 (“In the first contact region CA1, one end of the second portion 62a is connected to the first portion 61a, and in the second contact region CA2, the other end of the second portion 62a is connected to the third portion 63a.”). This is also taught by Kwon’463. Kwon’463 teaches that “a VSS line and a VDD line in the flexible display 100 may have the grid-like trace design, especially if such lines are arranged to cross over a bend allowance section.” Ex-1023 (Kwon’463), 23:5-18, 29:31-45, 29:66-30:17, 32:28-47, 33:3-12.

56. *See also, e.g.,* Ex-1024 (Kang’838), 5:29-45 (“The power link line PLL includes a first power link line PLL1 and a second power link line PLL2. The first power link line PLL1 is disposed in the first inactive area NA1. The second power

link line PLL2 is disposed in the second inactive area NA2 and extends from the first inactive area NA1 to the pad area PA. For example, the second power link line PLL2 includes a first connection line CL1 disposed in the pad area PA and the second inactive area NA2, a plurality of bending patterns BP disposed in the bending area BA, and a second connection line CL2 disposed in the first inactive area NA1.”), 5:64-6:13 (“The second connection line CL2 is disposed in the first inactive area NA1 and is connected to the plurality of bending patterns BP and the first power link line PLL1. The second connection line CL2 extends from the plurality of bending patterns BP toward the first inactive area NA1 and is disposed in the center portion of the first inactive area NA1. The first power link line PLL1 transmits power voltage transmitted through the first connection line CL1 and the plurality of bending patterns BP to the plurality of power lines PL of the active area A/A. The first power link line PLL1 is disposed in the first inactive area NA1 and extends to both ends (e.g., opposite sides) of the first inactive area NA1. The first power link line PLL1 includes a first hole H1 disposed in the center portion of the first inactive area NA1. The first hole H1 will be described below with reference to FIG. 2.”), 6:24-34; Ex-1025 (Kim’631), 4:17-41 (“The first wiring unit 300 and the second wiring unit 400 may be positioned over the non-display area NDA outside the display area DA, and may be sequentially disposed over the first area 1A, the second area 2A, and the bending area BA. ... The first wiring unit 300 may be a wiring unit that transmits a

data signal to the display 200. ... The second wiring unit 400 may be spaced apart from the first wiring unit 300. The second wiring unit 400 may include a first power wiring unit 410 and a second power wiring unit 420 that supply driving power to the display 200, and a driving circuit wiring unit 430 applying a signal to a scan driving circuit 530. The first power wiring unit 410 and the second power wiring unit 420 may be referred to as a driver, and may drive the display. The scan driving circuit 530 may be a shift register. For example, the first power wiring unit 410 may be an ELVDD line, the second power wiring unit 420 may be an ELVSS line, and the driving circuit wiring unit 430 may be a scan line or a gate line.”), 5:49-60; Ex-1026 (Kim’792), 13:62-14:29, 14:45-50, 15:14-49, 20:38-48; Ex-1027 (Ki), 2:65-3:2, 27:1-6 (“The wire trace having the reinforced section may extend across the bend allowance section and routed to pads for COF or other components of the flexible display 100. In such instances, there may be additional stepped region (similar to EB1 and EB2) at or near the opposite end of the bend allowance section.”), Cl. 8; Ex-1028 (Lee’087), 17:29-37, 17:66-18:8, 26:1-13; Ex-1029 (Kwon’446) ¶¶17, 71-73, 105; Ex-1030 (Lee’279) ¶¶16, 76, 87, 91, 150, Cl. 1; Ex-1031 (Park’641) ¶¶8, 47, 99; Ex-1032 (Liu’226) ¶¶37-39, 45-50, 103; Ex-1033 (Shyu) ¶¶30, 48-49; Ex-1034 (Lin’895) ¶¶51, 60-62, 64-66, 94, Figs. 11, 34.

57. It was also well known by 2018 that the second section of the first power trace is connected to the plurality of component connecting pads. For

example, Park’889 teaches “third portion 63a,” which “may be connected to a pad P of the pad portion PP.” Ex-1022 (Park’996), 7:11-27; *see also id.*, 15:11-20 (“The signals input to the pad portion PP through the printed circuit film 700 are transmitted to the elements of the display panel 100 through the signal lines, which extend across the bending region BA.”), Fig. 9. This is also taught by Kwon’463. *See, e.g.*, Ex-1023 (Kwon’463) 23:5-18, Figs. 1, 13A-13B.

58. *See also, e.g.*, Ex-1024 (Kang’838), 12:24-36 (“For example, the first connection lines CL1A are connected at both ends (e.g., opposite sides) of the pad area PA at both ends (e.g., opposite sides) of the second inactive area NA2. Bending patterns BP connected to the first connection lines CL1A are also disposed at both ends of the bending area BA. Second connection lines CLA2 extending from the bending patterns BP toward the first inactive area NA1 are also at both ends (e.g., opposite sides) of the first inactive area NA1. Therefore, the second power link line PLL2A, which includes the first connection lines CL1A, the bending patterns BP, and the second connection lines CL2A, may be connected to both ends of the first power link line PLL1, which extends to both ends of the first inactive area NA1.”), 13:51-64, Figs. 5B-5C; Ex-1025 (Kim’631), 2:23-24 (“a pad unit located over the second area of the substrate”), 5:5-37, Cl. 16; Ex-1026 (Kim’792), 19:62-20:3; Ex-1027 (Ki), 4:30-44; Ex-1029 (Kwon’446) ¶31; Ex-1031 (Park’641) ¶107, Cl. 14; Ex-1032 (Liu’226) ¶104.

C. Display Panels Wherein A First Section of A Second Power Trace is Disposed Adjacent to the Active Region, Between the Active Region and the Bending Region, and Connected to a Second Section of the Second Power Trace Disposed Within the Component Disposing Region By At Least A Set of Second Connecting Sub-Traces Disposed Within the Bending Region Were Known

59. Display panels wherein a first section of a second power trace is disposed adjacent to the active region, between the active region and the bending region, and connected to a second section of the second power trace disposed within the component disposing region by at least a set of second connecting sub-traces disposed within the bending region were well known by 2018. This part of the technology background focuses that prior to 2018 it was well known to a POSITA that routing a secondary power trace such as ELVDD across a displays bend region using sub-traces and patterned bridges. In particular, a POSITA would see that bendable displays would contain: (1) dual power separation for secondary power traces; (2) power trace bridge connection using connecting sub-traces, (3) placement of power traces in the bendable display, and (4) connections to terminal component areas. For example, Park’996 teaches this for the same reasons described in the previous section. *See, e.g.*, Ex-1022 (Park’996), 5:42-43, 6:66-7:27. Additionally, Park’996 teaches that “[t]he first group 510a includes at least one first signal line 10, the second group 520a includes at least one second signal line 20, and the third group 530a includes at least one third signal line 30” and “[i]n the bending region BA, first

to fifth additional groups 510b, 520b, 530b, 540b, and 550b may be disposed at the right side of the data signal line group 560 ... symmetrically with the first to fifth groups 510a, 520a, 530a, 540a, and 550a with respect to the data signal line group 560” with “substantially the same as the characteristics” to one another. Ex-1022 (Park’996), 4:48-64. Park’996 further teaches that “[t]he fourth group 540a includes a fourth signal line 40,” which “may transmit the voltage of the constant polarity such as the common voltage ELVSS” and the “fifth group 550a includes a fifth signal line 50,” which “may transmit a signal that is different from that of the fourth signal line 40, for example, the voltage of the constant polarity such as a driving voltage ELVDD” and “may be connected to a driving voltage transmitting line 72 connected to the driving voltage line 172 of the display area DA.” Ex-1022 (Park’996), 6:34-46. This is also taught by Kwon’463 for the reasons described in the previous section Kwon’463 teaches that “a VSS line and a VDD line in the flexible display 100 may have the grid-like trace design, especially if such lines are arranged to cross over a bend allowance section.” Ex-1023 (Kwon’463), 23:5-18; *see also id.*, 29:31-45, 29:66-30:17, 32:28-47, 33:3-12.

60. *See also, e.g.*, Ex-1024 (Kang’838), 6:14-17 (“The first power link line PLL1 is connected to the plurality of bending patterns BP. For example, the first power link line PLL1 is connected to the plurality of bending patterns BP through the second connection line CL2.”), 12:5-36 (“FIG. 5A is a plan view of a display

device according to still another embodiment of the present disclosure, FIG. 5B is a plan view of a display device according to another embodiment of the present disclosure, and FIG. 5C is a plan view of a display device according to still another embodiment of the present disclosure. As compared with the display device 100 of FIG. 1, in display devices 500A, 500B, and 500C of FIGS. 5A, 5B, and 5C, the number of holes in the first power link line PLL1 is different, and the arrangement of the second power link lines PLL2A, PLL2B, and PLL2C are different from that of the display device 100 of FIG. 1. However, as the other configurations are substantially the same as the display device 100 of FIG. 1, redundant descriptions will be omitted or briefly described. Referring to FIG. 5A, the second power link lines PLL2A in the display device 500A are disposed at both ends (e.g., opposite sides) of the inactive area N/A to be connected to both ends of the first power link line PLL1. For example, the first connection lines CL1A are connected at both ends (e.g., opposite sides) of the pad area PA at both ends (e.g., opposite sides) of the second inactive area NA2. Bending patterns BP connected to the first connection lines CL1A are also disposed at both ends of the bending area BA. Second connection lines CLA2 extending from the bending patterns BP toward the first inactive area NA1 are also at both ends (e.g., opposite sides) of the first inactive area NA1. Therefore, the second power link line PLL2A, which includes the first connection lines CL1A, the bending patterns BP, and the second connection lines

CL2A, may be connected to both ends of the first power link line PLL1, which extends to both ends of the first inactive area NA1.”), 13:30-36 (“The second connection lines CL2B of the second power link lines PLL2B are connected to a point other than the center portion and both ends of the first power link line PLL1. For example, the second connection lines CL2B may be connected to points corresponding to the one quarter point and three quarters point of the first power link line PLL1, but is not limited thereto.”); Ex-1025 (Kim’631), 4:17-41 (“For example, the first power wiring unit 410 may be an ELVDD line, the second power wiring unit 420 may be an ELVSS line, and the driving circuit wiring unit 430 may be a scan line or a gate line.”), 5:61-6:7; Ex-1026 (Kim’792), 13:62-14:29, 14:45-50, 15:14-49, 20:38-48; Ex-1027 (Ki), 18:6-14, 19:16-30 (“a single conductive line trace 120 can include two or more sub-traces, which split and merge at every joint X. From a first joint X, one of the sub-traces extends in a first direction that is angled away from the tangent vector of the curvature for a predetermined distance, and then extends in a second direction towards a second joint X.”), 19:43-56, 31:38-56; Ex-1028 (Lee’087), 23:12-38; Ex-1029 (Kwon’446) ¶¶61, Figs. 2A, 8B; Ex-1030 (Lee’279) ¶¶70, 73, 94; Ex-1031 (Park’641) ¶97; Ex-1032 (Liu’226) ¶¶40, 51; Ex-1033 (Shyu) ¶¶30, 48-49; Ex-1034 (Lin’895) ¶¶51, 60-62, 64-66, 94, Figs. 11, 34.

61. It was also well known by 2018 that the second portion of the second power trace is connected to the plurality of component connecting pads. For

example, Park'996 teaches this for the same reasons described in the previous section. *See, e.g.*, Ex-1022 (Park'996), 6:66-7:27, 15:11-20. This is also taught by Kwon'463. *See, e.g.*, Ex-1023 (Kwon'463), 23:5-18, Figs. 1, 13A-13B.

62. *See also, e.g.*, Ex-1024 (Kang'838), 13:51-64 (“Second connection lines CL2 and CL2A which extend from the bending patterns BP toward the first inactive area NA1 are also disposed at the center portion and both ends of the first inactive area NA1. Therefore, the first connection lines CL1 and CL1A, the bending patterns BP, and the second connection lines CL2 and CL2A may be respectively connected to the center portion and both ends of the first power link line PLL1, which extends to both edges of the first inactive area NA1.”); Ex-1025 (Kim'631), 2:23-24, 5:5-37, Cl. 16; Ex-1026 (Kim'792), 19:62-20:3; Ex-1027 (Ki), 27:1-6; Ex-1029 (Kwon'446), Fig. 8B; Ex-1031 (Park'641), Cl. 14; Ex-1032 (Liu'226) ¶104.

D. Display Panels Wherein the First Section of the Second Power Trace is Separately Connected to the Second Section of the Second Power Trace Disposed Within the Component Disposing Region By Two Sets of the Second Connecting Sub-Traces Passing Through Two Sections of the Bending Region Were Known

63. Display panels wherein the first section of the second power trace is separately connected to the second section of the second power trace disposed within the component disposing region by two sets of the second connecting sub-traces passing through two sections of the bending region were well known by 2018. This part of the technology background focuses that prior to 2018 it was well known to a

POSITA that routing a secondary power trace across a bendable OLED display using two separate sets of sub-traces that reach across two sections of a bending region. In particular, a POSITA would see that for bendable displays, there would be: (1) a dual path and sectional routing, (2) separation via channels and split grids, (3) continuous sub-trace bridging, and (4) distributed non-central sub-trace tap points. For example, Park'996 teaches that "parts of the signal lines" are "disposed in the first and second contact regions CA1 and CA2 of the upper side and the lower side of the bending region BA" and the "part of the signal line disposed at the bending region BA and the contact regions CA1 and CA2 is referred to as a connection line," which "includes first connection lines 60a and second connection lines 60b ... alternately arranged in the first direction." Ex-1022 (Park'996), 6:66-7:10, Fig. 2. Moreover, Park'996 teaches that "first connection line 60a includes a first portion 61a," which "extends from the first contact region CA1 to the upper side of the first contact region CA1 (in the direction D2) ... from the peripheral area PA of the display panel 100 and may connect with the element transmitting the above-described signals"; "a second portion 62a ... disposed throughout the first contact region CA, the bending region BA, and the second contact region CA"; and "a third portion 63a," which "extends from the second contact region CA2 to the lower side of the second contact region CA2 (in the opposite direction to D2)" and "may be connected to a pad P of the pad portion PP." Ex-1022 (Park'996), 7:11-27 ("In the

first contact region CA1, one end of the second portion 62a is connected to the first portion 61a, and in the second contact region CA2, the other end of the second portion 62a is connected to the third portion 63a.”), Figs. 1-2. This is also taught by Kwon’463. Kwon’463 teaches that “[s]everal conductive lines are included in the flexible display 100 for electrical interconnections between various components therein” and “[t]he circuits fabricated in the active area and inactive area may transmit various signals via one or more conductive lines to provide a number of functionalities in the flexible display 100.” Ex-1023 (Kwon’463), 16:64-17:5 (“[S]ome conductive lines may be used to provide interconnections between the circuits and/or other components in the central portion and the bend portion of the flexible display 100.”). Kwon’463 further teaches that “[t]he wire trace may split into additional number of sub-traces, resulting series of links arranged in a grid-like configuration” and “[n]either the number of sub-traces nor the shapes of the sub-traces of the grid-like trace design are particularly limited.” Ex-1023 (Kwon’463), 23:5-18; *see also id.*, 32:28-47. Moreover, Kwon’463 teaches that “one or more of power signal wires of the flexible display 100, such as the VDD and/or the VSS, has the grid-like wire trace formed of multiple diamond-chain traces adjoined side-by-side,” which “includes one or more elongated channels in its grid-like wire trace,” each “provided between two divided grid parts ... on the opposite sides of the

elongated channel” that “are connected at one or both ends of the power signal wire.”

Ex-1023 (Kwon’463), 33:3-20.

64. *See also, e.g.*, Ex-1024 (Kang’838), 5:29-39 (“The power link line PLL includes a first power link line PLL1 and a second power link line PLL2. The first power link line PLL1 is disposed in the first inactive area NA1. The second power link line PLL2 is disposed in the second inactive area NA2 and extends from the first inactive area NA1 to the pad area PA. For example, the second power link line PLL2 includes a first connection line CL1 disposed in the pad area PA and the second inactive area NA2, a plurality of bending patterns BP disposed in the bending area BA, and a second connection line CL2 disposed in the first inactive area NA1.”), 13:30-36 (“The second connection lines CL2B of the second power link lines PLL2B are connected to a point other than the center portion and both ends of the first power link line PLL1. For example, the second connection lines CL2B may be connected to points corresponding to the one quarter point and three quarters point of the first power link line PLL1, but is not limited thereto.”); Ex-1025 (Kim’631), 5:12-19 (“the first wiring unit 300 may include a plurality of first wirings 300-1, 300-2, . . . that may be disposed over the substrate 100 to sequentially extend over the first area 1A, the bending area BA, and the second area 2A of the substrate 100” and “may be spaced apart from each other by a predetermined space.”), 5:61-6:7, Fig. 1; Ex-1026 (Kim’792), 15:35-43; Ex-1027 (Ki), 19:16-30, 19:43-56, 31:38-56; Ex-1028

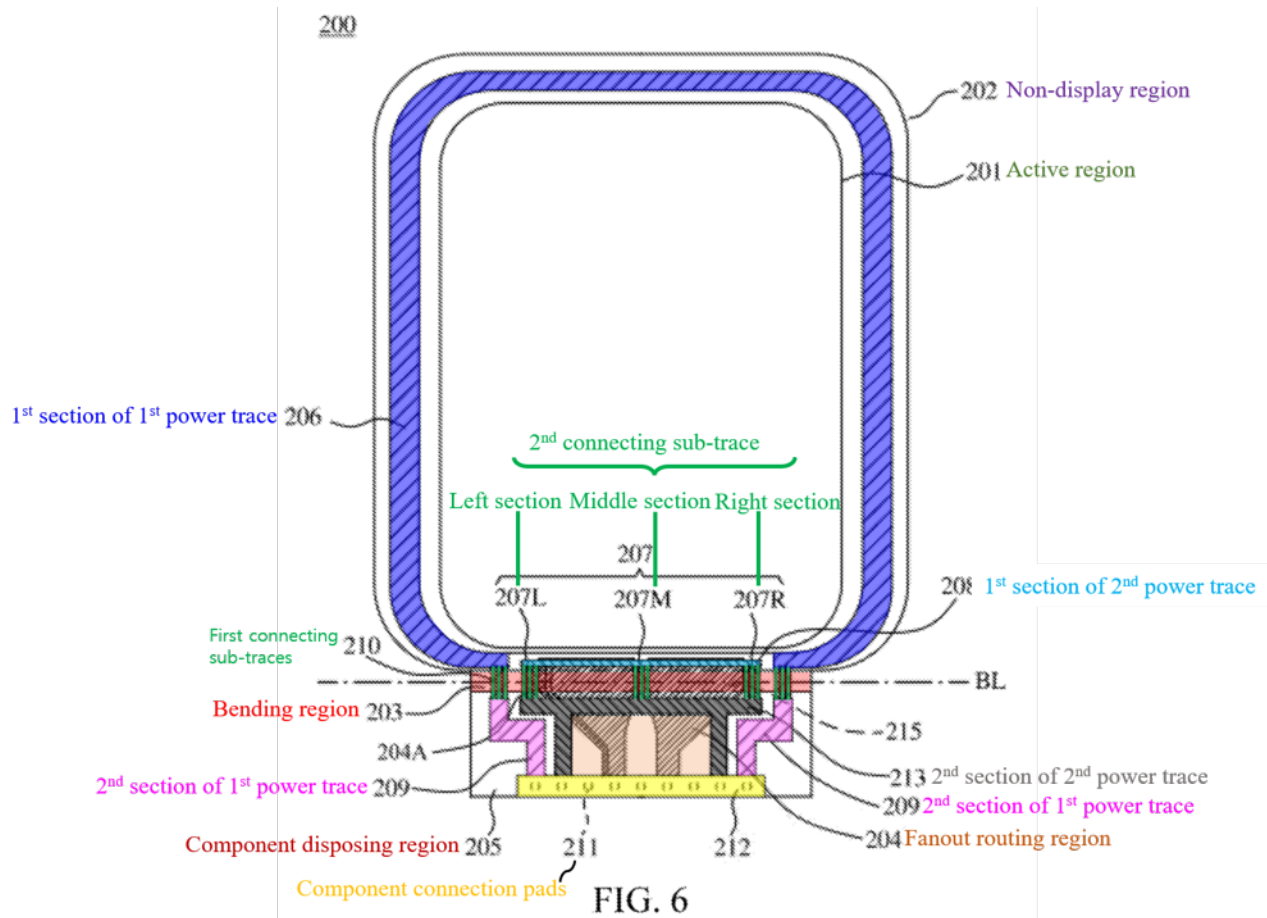
(Lee'087), 23:12-38, 26:1-13; Ex-1029 (Kwon'446) ¶¶61, 105; Ex-1030 (Lee'279) ¶¶32, 70, 73, 94; Ex-1031 (Park'641) ¶¶8, 53, 97, Cl. 1; Ex-1032 (Liu'226) ¶¶37-40, 45-51, 103-104; Ex-1033 (Shyu) ¶¶30, 48-49, Figs. 24, 26.

V. THE '891 PATENT

A. Overview of the '891 Patent

65. The '891 Patent teaches a display device that purportedly “solve[s] the problems existing in the conventional art, to allow that the bottom border of the display panel can realize a true narrow border design, and to avoid the narrow border design that may cause product reliability problems or product failure due to trace breakage.” Ex-1001, 2:32-36. As shown in annotated Figure 6 below,¹ the '891 Patent teaches a display device, which includes an active region 201 (light green) and non-display region 202 (dark purple) that includes a bending region 203 (red), a fanout routing region 204 (orange), and a component disposing region 205 (maroon) containing component connecting pads 211 (yellow). Ex-1001, 5:29-37.

¹ Throughout, emphasis and annotations are added unless otherwise specified.

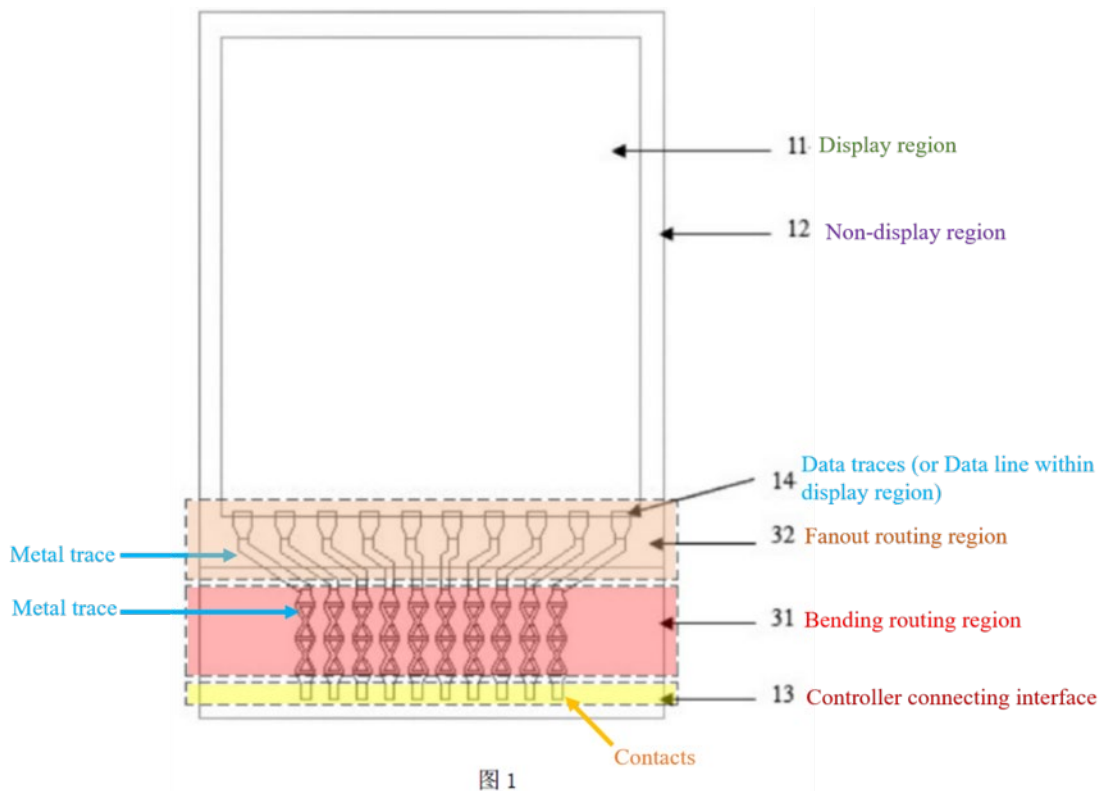


66. Independent Claim 1 of the '891 Patent recites a specific arrangement of the components of the display device including a first section of a first power trace 206 (blue) disposed within the non-display region 202 around the active region 201, and connected to a second section of the first power trace 209 (pink) disposed within the component disposing region 205, and connected to the plurality of component connecting pads 211. Ex-1001, Cl. 1, 9:26-32. A first section of the second power trace 208 (light blue) is disposed adjacent to the active region 201 and disposed between the active region 201 and the bending region 203, and connected to a second section of the second power trace 213 (grey) disposed within the component

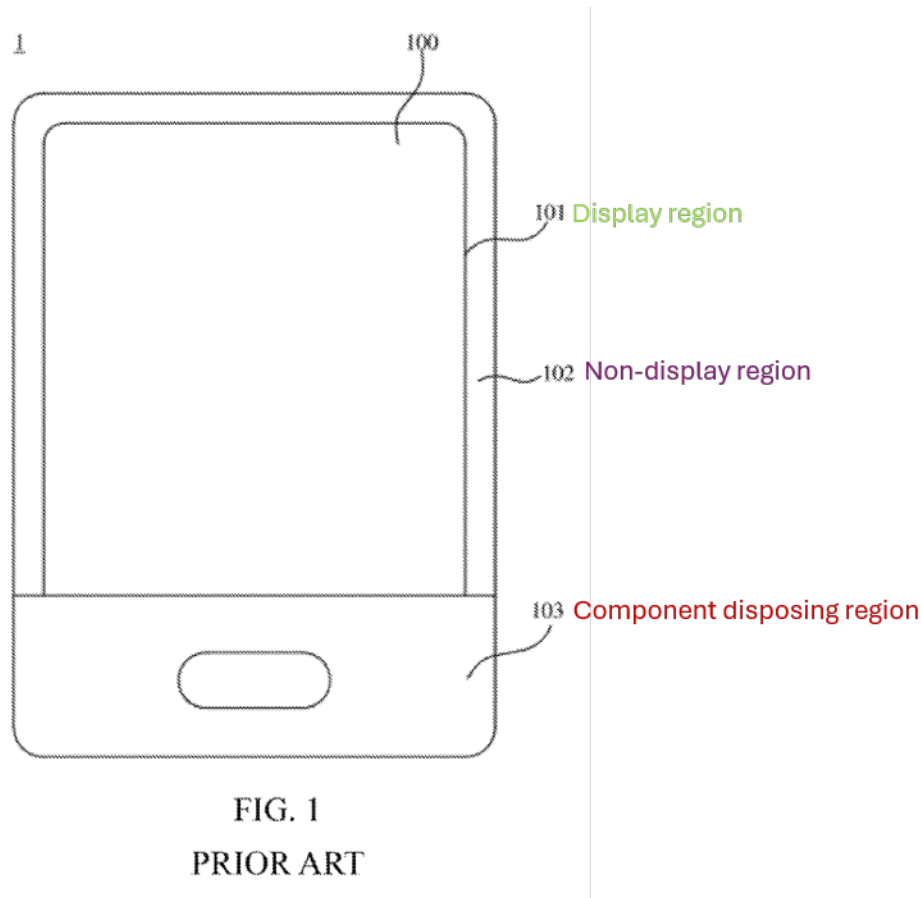
disposing region 205 by at least a set of second connecting sub-traces 207 (green) passing through two sections of the bending region 207L, 207R disposed within the bending region 203 and connected to the plurality of component connecting pads 211. Ex-1001, Cl. 1. Independent Claims 11 and 16 of the '891 Patent include three sets of connecting sub-traces passing through a left section 207L, a middle section 207M, and a right section 207R of the bending region. Ex-1001, Cls. 11, 16, 10:31-51, 11:1-17.

67. The '891 Patent discusses at least an “active region/display region,” “non-display region,” “bending routing region/bending line,” “data trace/metal trace”, “fanout routing region,” “component controlling interface/component disposing region,” “contacts,” “high-potential power trace,” “low-potential power trace,” and two sections of “bending line” through which the “high-potential power trace” passes as prior art in its prior art section. Specifically, the '891 Patent states that “China utility model patent No. 205140985U discloses a flexible AMOLED display panel structure comprising a first substrate and a second substrate, the second substrate being a protective cover plate, and the first substrate comprising *a display region* [light green] and *a non-display region* [dark purple], wherein the non-display region is disposed around the display region and is bilaterally symmetric”; “[e]ach of contacts [yellow] of a controller connecting interface [maroon] disposed on the non-display region is connected to each of *data traces* [blue] within the display

region by a metal routing structure, and the metal routing structure includes *a bending routing region* [red] and *a fanout routing region* [orange], each *metal trace* in a bending routing region and each *metal trace* in the fanout routing region is connected to each other one by one”; and “[b]y changing the metal routing structure of the flexible AMOLED display panel, resistance of the metal traces in the bending routing region and resistance of the metal traces in the fanout routing region are more uniform, and the display region in the entire display panel is proportionally increased, therefore increasing area of the display region.” Ex-1001, 1:22-40. *See also* Ex-1021 (CN205140985U), Fig. 1 (annotated).



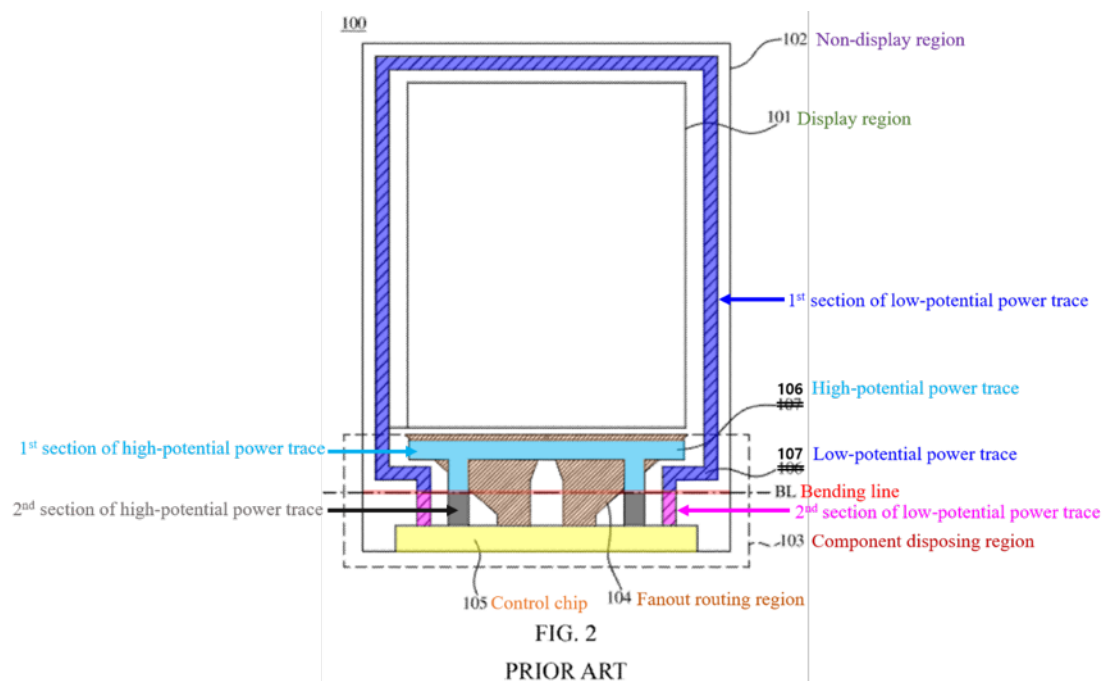
68. Referring to Figure 1 (prior art) below, the '891 Patent shows “a display panel 100 for a conventional smartphone 1,” which “includes a display region 101 [light green] and a non-display region 102 [dark purple] ... distributed around the display region 101”; “[a] component disposing region 103 [maroon] ... disposed under the display region 101 and configured for disposing a plurality of traces (not shown) and at least one control chip 105.” Ex-1001, 1:41-49, Fig. 1 (annotated).



69. Next, referring to Figure 2 (prior art) below, the '891 Patent states that “a fanout routing region 104 [orange] is disposed within the component disposing region 103 [maroon], and the fanout routing region 104 has a plurality of traces

configured for connecting the display region 101 [light green] and the control chip 105 [yellow], thereby controlling the display region 101 by the control chip 105.” Ex-1001, 1:49-54, Fig. 2 (annotated). The ’891 Patent further states that “high-potential power trace 106² is disposed within the component disposing region 103 and under the display region 101 to provide a high-potential voltage to the display region 101”; “low-potential power trace 107 surrounds the display region 101 and extends downwardly outside the high-potential power trace 106 and is retracted below the high-potential power trace 106”; and “low-potential power trace 107 is parallel to the high-potential power trace 106, and extends downwardly to connect the control chip 105.” Ex-1001, 1:53-62. Figure 2 also shows that conventional high-potential power trace 106 has a first section (blue) over the bending line (red) and a second section (grey) under the bending line; and conventional low-potential power trace 107 has a first section (blue) over the bending line (red) and a second section (pink) under the bending line. Ex-1001, Fig. 2.

² A POSITA would have understood that there is a typographical error in Figure 2 such that reference numerals 106 and 107 should be swapped to 107 and 106, respectively.



B. Prosecution History of the '891 Patent

70. I have reviewed the prosecution history of the '891 Patent. The '891 Patent was filed December 12, 2018 as the U.S. national stage entry of PCT Application No. PCT/CN2018/108168, filed September 28, 2018. It claims priority to Chinese Application No. 201810581903.1, filed June 7, 2018.

71. The '891 Patent was allowed after one office action. On June 22, 2021, the Examiner rejected then-pending Claims 1–2, 11, and 17–18 as anticipated over U.S. Patent Publication No. 2017/0288008 to Kim (“Kim”), Claims 5–6 as obvious over Kim, and Claim 8 as obvious over Kim in view of U.S. Patent Publication No. 2014/0042406 to Degner (“Degner”). Ex-1004, 247–58. In a September 21, 2021 response, the Applicant amended independent Claim 1 to recite “wherein the first section of the second power trace is separately connected to the second section of

the second power trace disposed within the component disposing region by two sets of the second connecting sub-traces passing through two sections at the bending region” and independent Claim 17 (issued as Claim 16) to recite “wherein the first section of the power trace is separately connected to the second section of the power trace disposed within the component disposing region by three sets of connecting sub-traces passing through a left section, a middle section and a right section of the bending region.” Ex-1004, 283-289. The Applicant argued that these limitations were not taught by the prior art of record. *Id.* The Examiner issued a Notice of Allowance on November 5, 2021. Ex-1004, 290-94.

72. This Declaration presents new prior-art grounds and arguments that I understand were not considered during prosecution. In my opinion, the challenged claims are invalid as obvious for the reasons explained below.

VI. CLAIM CONSTRUCTION

73. I do not believe that any term requires express construction to resolve the issues presented in my Declaration. That said, the '891 specification explains that certain structures fall within the scope of certain claim terms. As noted below, the associated claims terms would have been understood by a POSITA to include at least such recited structures

an active region: a display area that includes, at least pixels, such as “a plurality of thin-film transistors to control the emitting of the display panel.” Ex-1001, 6:5-8.

a non-display region: an area that does not display an image and instead includes non-display components, such as “the plurality of traces and the control chip.” Ex-1001, 1:66-2:6.

a second power trace: a second trace (different than the first trace) that transmits power, such as a VDD trace. Ex-1001, 7:34-36 (“the second power trace is a high-potential power trace (VDD)”).

component connecting pads: pads for connecting an electronic component, such as “a controller chip,” “a rigid board,” a “rigid-flex board” or the like, using, for example, “a plurality of bumps.” Ex-1001, 6:26-34.

VII. DESCRIPTION OF THE APPLIED PRIOR ART

A. Kwon (Ex-1005)

74. Kwon (U.S. Patent No. 9,780,157) issued October 3, 2017. I understand that Kwon is prior art to the '891 Patent under 35 U.S.C. §102(a)(1).

75. Kwon teaches “a flexible display having a plurality of innovations configured to allow bending of a portion or portions to reduce apparent border size and/or utilize the side surface of an assembled flexible display.” Ex-1005, Abstract. As shown in annotated Figures 1 and 16A below, Kwon teaches a “flexible display

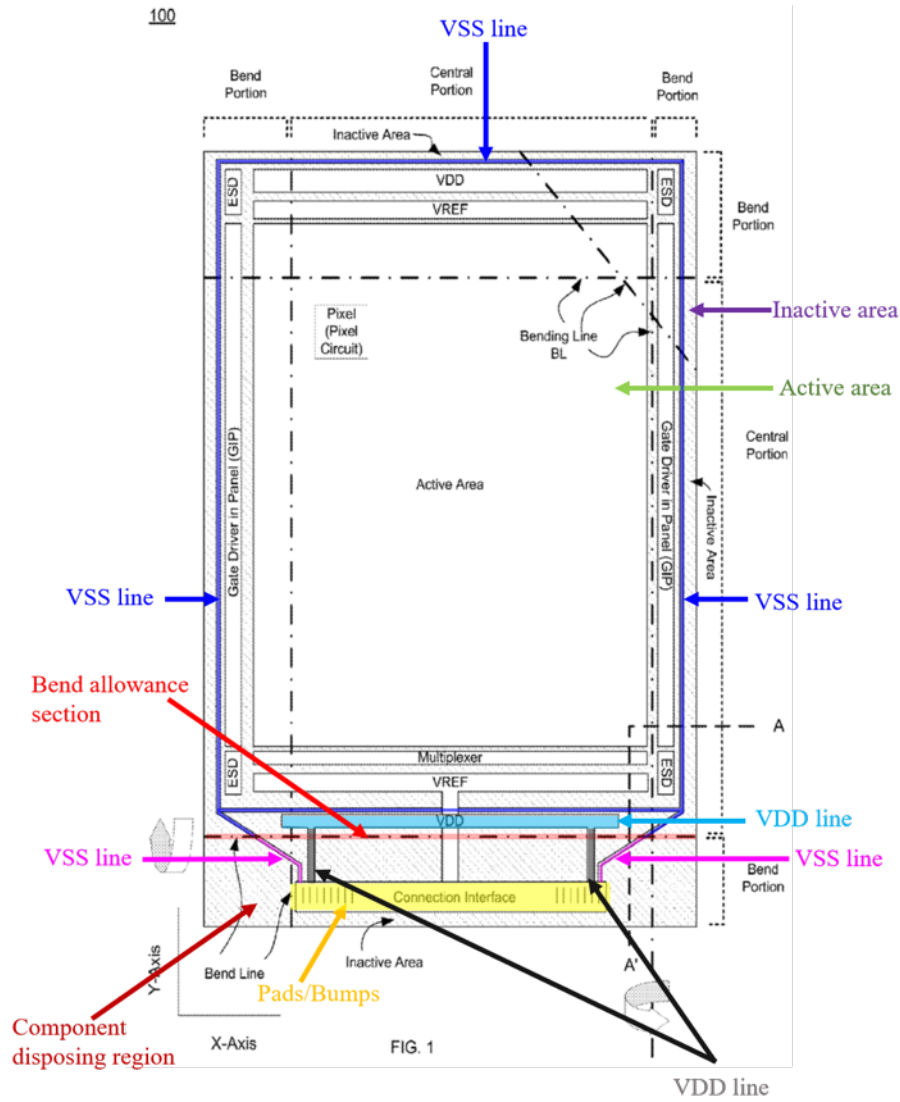
100.” Ex-1005, Figs. 1, 16A. That flexible display includes an active area (light green) surrounded by an inactive area (dark purple). The inactive area further includes a “bend allowance section” (red), “routing area” (orange), and “connection interface” (maroon) with “Pads/Bumps” (yellow).

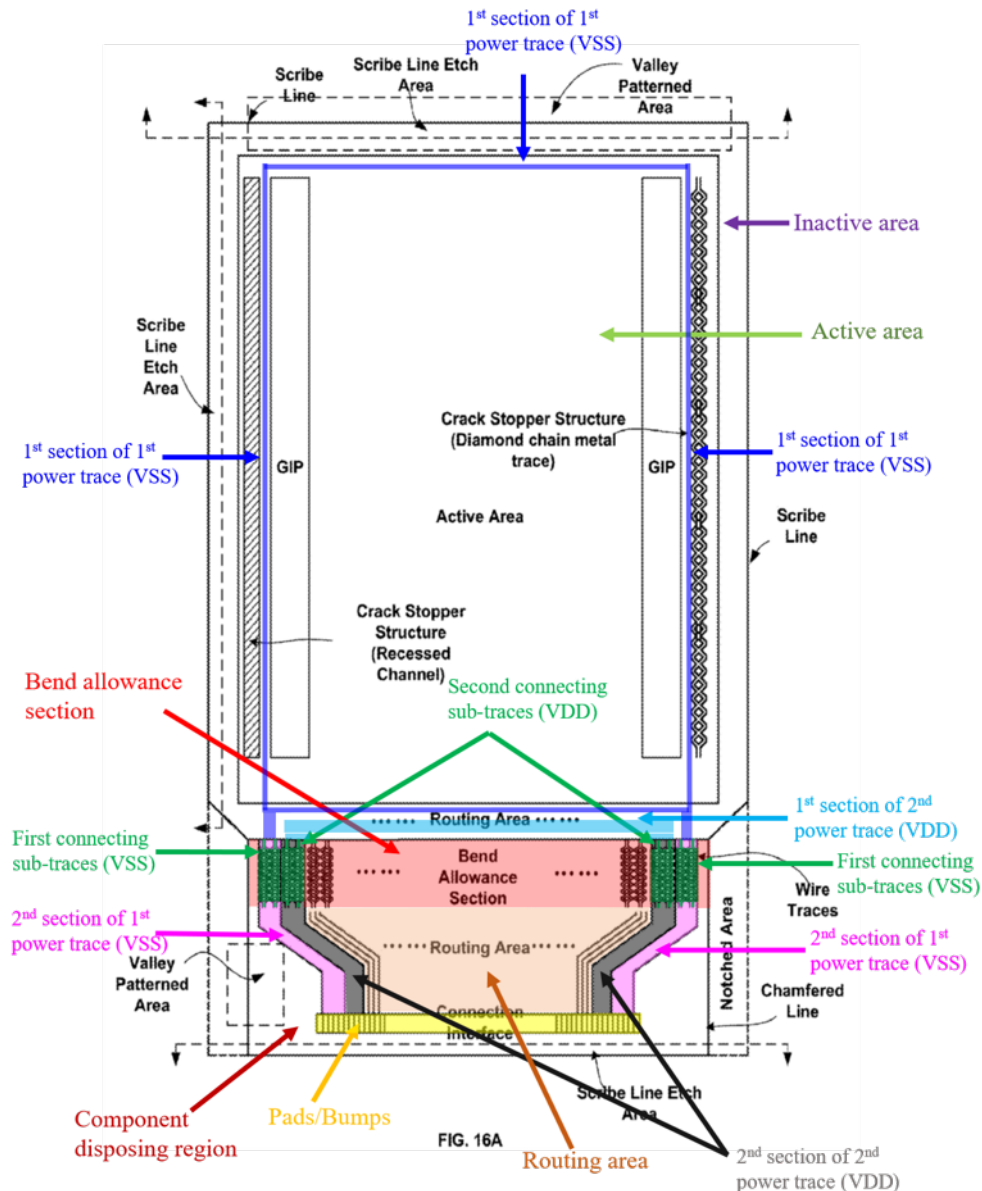
76. The bend portion includes a bend allowance section, which can be actively curved in a certain bend radius.” Ex-1005, 6:33-35. “The bend allowance section” is “between the active area and the inactive area where the external printed circuit is attached thereto.” Ex-1005, 34:7-9. “The bend allowance section” has “only the conductive line 120 rather than active display components or peripheral circuits.” Ex-1005, 46:30-32.

77. The “routing area” is ““between the active area and the bend allowance section” as well as “between the COF bonding area and the bend allowance section” and has a patterned insulation layer containing wire traces. Ex-1005, 31:23-31. The COF bonding area is “coupled to a connection interface (Pads/Bumps, Pins) disposed in the inactive area.” Ex-1005, 5:46-47.

78. Kwon also teaches VSS lines (blue and pink) and VDD lines (light blue and grey), as shown in annotated Figures 1 and 16A below. Ex-1005, 2:31-33, Figs. 1, 16A. Kwon teaches that “the area positioned even further out toward the scribe line of the base layer 106” may include VSS lines (blue) and surround the “top edge and the bottom edge” and “side edges of the flexible display 100.” Ex-1005, 35:51-

63, 36:32-37. Kwon further teaches a “plurality of wire traces extending between the first area and the second area” (green) that connects the first and second sections of the power traces. Ex-1005, 2:31-33. Kwon also teaches that these wire traces “may split into additional number of sub-traces” to connect the first and second sections of the corresponding traces. Ex-1005, 28:32-34. “For example, a VSS line and a VDD line in the flexible display 100 may ... are arranged to cross over a bend allowance section.” Ex-1005, 28:38-41. Moreover, Kwon teaches that the above “wire trace[s] . . . may extend across the bend allowance section” so that the second section of the first power trace (VSS line) (pink) and second power trace (VDD line) (grey) are “routed to pads for COF or other components of the flexible display 100.” Ex-1005, 33:40-43.





B. Kang'261 (Ex-1006)

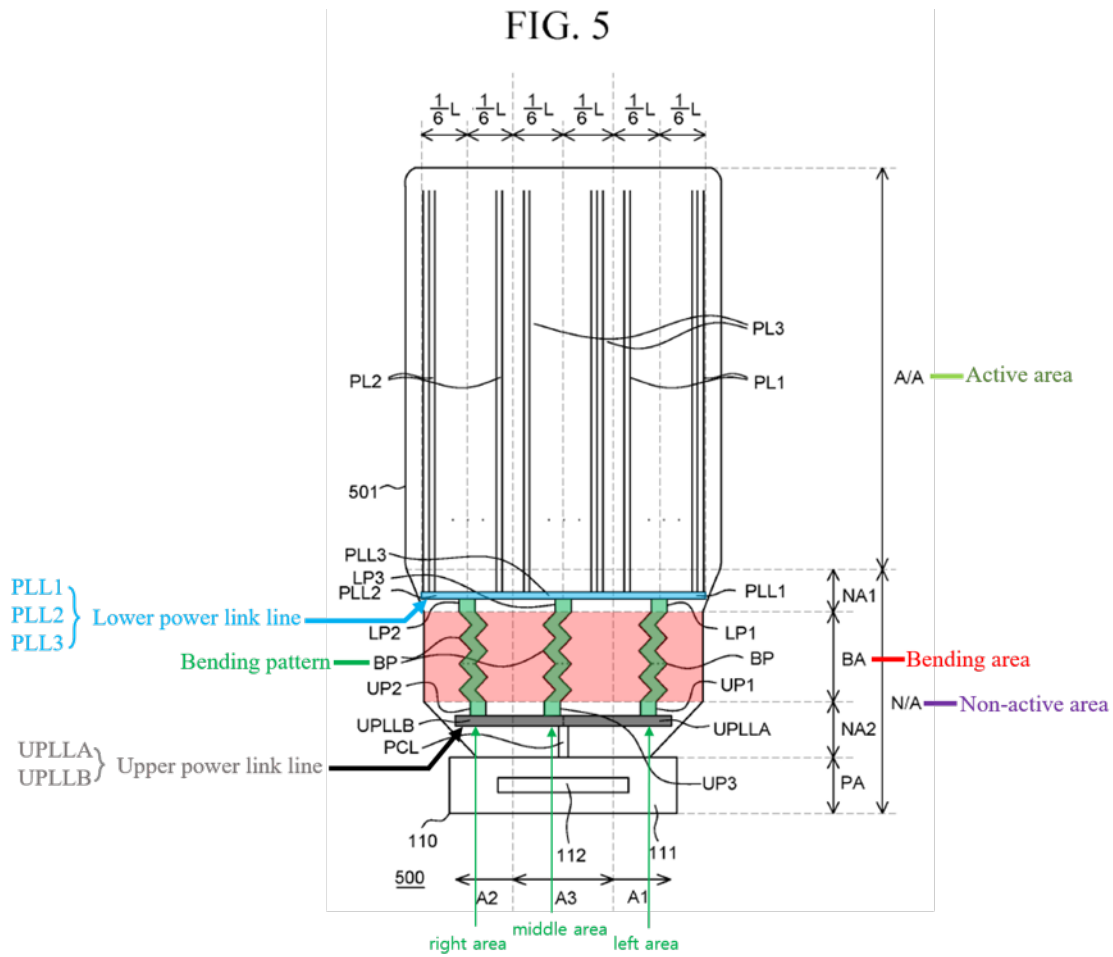
79. Kang'261 (U.S. Patent No. 10,651,261) was filed August 16, 2018, and claims priority to a Korean Patent Application filed August 16, 2017. I understand that Kang'261 is prior art to the '891 Patent under at least AIA 35 U.S.C. § 102(a)(2).

80. Kang'261's Korean counterpart is essentially identical to the U.S. filing. *See generally* Ex-1006 (U.S. published application), Ex-1008 (Korean application), Ex-1009 (certified translation of Korean application). The figures are identical, and the specification is equivalent. *Id.* Because the described subject matter is identical, Kang'261's Korean counterpart provides support for Kang'261's disclosures, and I understand that Kang'261 is thus available as a patent prior art reference under AIA 35 U.S.C. §102(a)(2) as of its Korean priority date of August 16, 2017.

81. Kang'261 teaches a "Display Device" with a plurality of power lines and power link lines disposed in the active (light green) and non-active (dark purple) areas, respectively, that are configured to transmit power voltage across a bending area (red) via bending patterns connecting an upper power link line (light blue) to a lower power link (grey) line using sub-traces (green) divided across right, middle, and left areas. Ex-1006, 13:20-14:46, 15:18-20. As shown in the annotated version of Figure 5³ below, Kang'261 teaches a "first area A1, second area A2, and third area A3 . . . defined by dividing the length of the substrate 501 along a longitudinal direction" with A1 corresponding to the "the left area of the substrate 501," A2 corresponding to "the right area," and A3 corresponding to the "the central area."

³ For clarity, Figure 5 has been flipped vertically without changing its content.

Ex-1006, 13:20-33, Fig. 5. Kang'261 further teaches that "the power link lines," one of which corresponds to the second power trace (VDD), "are disposed to transmit power voltage to pixels in their respective areas." Ex-1006, 15:18-20. These power link lines are further divided by "upper power link lines" UPLLs and "lower power link lines," PLLs. *See* Ex-1006, 13:42-14:46. These two sections are connected by a "plurality of bending patterns BP in the bending area BA" and Kang'261 teaches that "some are disposed in the first area A1, some are disposed in the second area A2, and others are disposed in the third area A3." Ex-1006, 14:1-4.



C. Ka (Ex-1007)

82. Ka (U.S. Patent Publication No. 2017/0287937) was filed November 23, 2016 and published October 5, 2017. I understand that Ka is prior art to the '891 Patent under 35 U.S.C. §102(a)(1) and (2).

83. Ka is directed to a “Display Device Capable of Reducing Resistance of Driving Voltage Supply Wires,” and teaches specific, quantified width relationships among its first driving voltage transmission line 11 (light blue), second driving voltage transmission line 12 (grey), and driving voltage connection lines (green). Ex-1007, Cover. As shown in annotated Figure 1⁴ below, Ka teaches that “first driving voltage transmission line 11 and the second driving voltage transmission line 12 may each have a width of about 50 to about 200 micrometers, and the driving voltage connection line 15⁵ may have a width of about 3 micrometers.” Ex-1007 ¶74, Fig. 1. Ka teaches that “the display panel 300 may be bent with a predetermined curvature in the bending area BA [red].” Ex-1007 ¶68. Ka further teaches that transmission-line / trace-section widths are deliberately set wider than the connecting sub-trace or connection-line widths that cross the bend region because “[w]hen the length or width of the wires is increased or decreased, current density

⁴ For clarity, Figure 1 has been flipped vertically without changing its actual content.

⁵ A POSITA would have understood that “17” in the quotation is a typographical error because Ka’s driving voltage connection line corresponds to component “15.” See, e.g., Ex-1007 ¶¶62, 65, 74-76, 84-88.

VIII. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS

A. Ground 1: Claims 1, 7, and 10 are obvious over Kwon

1. Independent Claim 1

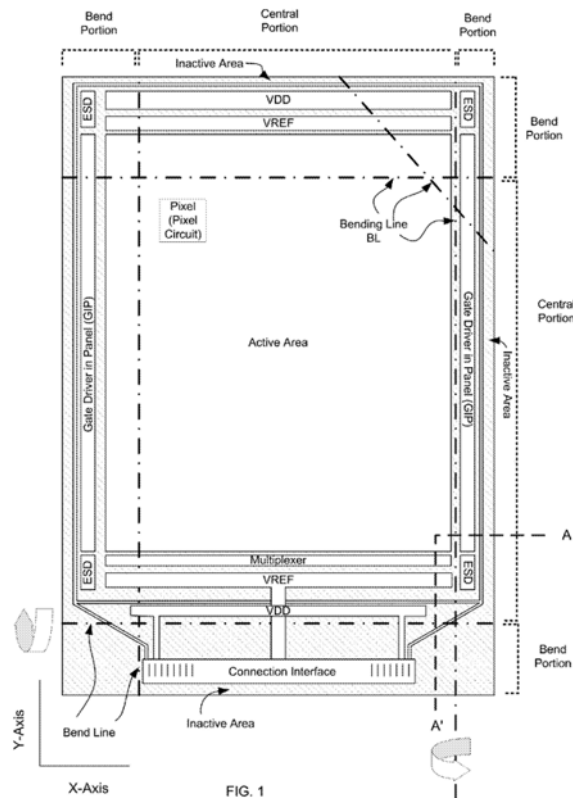
a. 1[pre]: A display panel, comprising:

84. In my opinion, Kwon teaches⁶ the preamble of Claim 1, to the extent that it is limiting.

85. As shown in Figure 1 below, Kwon teaches a “flexible display 100.” Ex-1005, Fig. 1. Kwon further teaches that flexible display 100 “may be incorporated in electronic devices.” Ex-1005, 5:15-16. Moreover, Kwon teaches that its “assembled display may include *a display panel*.” Ex-1005, 1:15.

⁶ I use the term “teaches” to include both express teachings and those that, in my opinion, are fairly suggested to a person of ordinary skill in the art. I have been informed by counsel that this approach is consistent with the test for obviousness under patent law.

100



- b. 1[a]: an active region and a non-display region, the non-display region disposed around the active region and extending to form a bending region, a fanout routing region, and a component disposing region; the component disposing region having a plurality of component connecting pads;

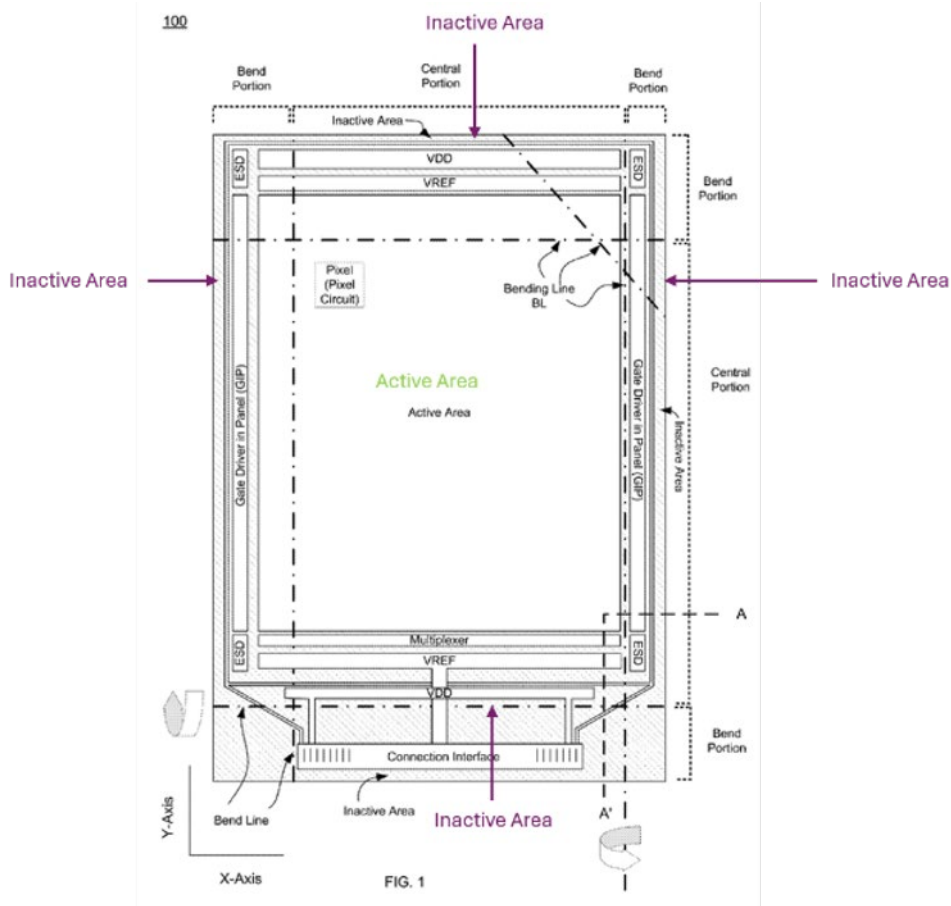
86. In my opinion, Kwon teaches Element 1[a].

87. Although the recited “active region,” “non-display region,” “bending region,” “fanout routing region,” “component disposing region,” and “connecting pads” are admittedly prior art components (*see* Section V), Kwon also teaches that its display panel comprises an “active region,” “non-display region,” “bending

region,” “fanout routing region,” “component disposing region,” and “plurality of component connecting pads.”

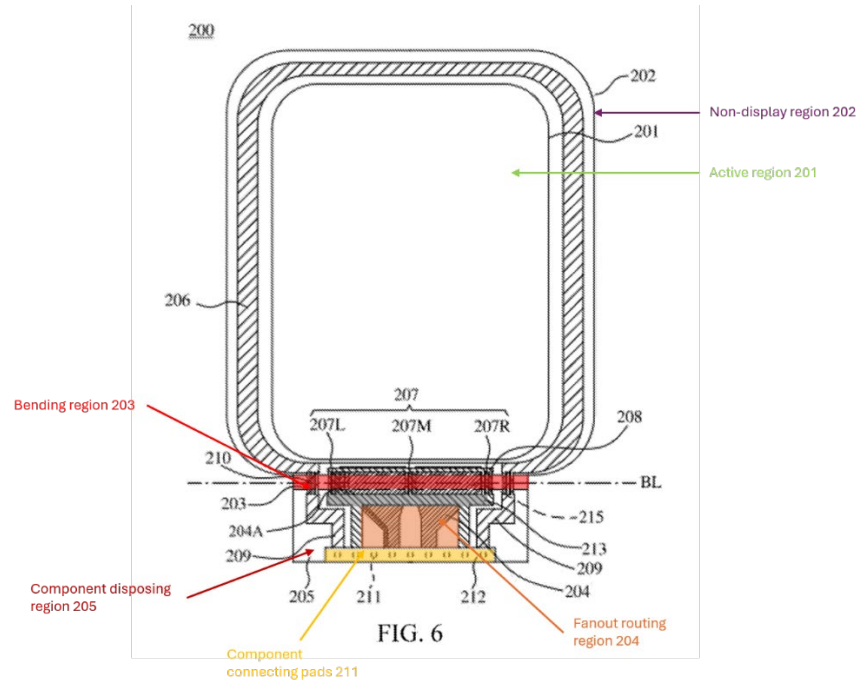
88. Specifically, Kwon’s display panel 100 includes an active region and a non-display region disposed around the active region. Kwon teaches that “flexible display 100 includes at least one active area (i.e., display area), in which an array of display pixels are formed therein” and “[o]ne or more inactive areas ... provided at the periphery of the active area.” Ex-1005, 5:17-20. Kwon also teaches that “the inactive area may be adjacent to one or more sides of the active area.” Ex-1005, 5:20-21. Kwon’s active area corresponds to the recited “active region” and Kwon’s inactive area corresponds to the recited “non-display region.”

89. As shown in annotated Figure 1 below, Kwon’s display panel 100 has a non-display region, which Kwon calls an inactive area, that surrounds the active region. Ex-1001, Fig. 6; Ex-1005, Fig. 1. In Figure 1, the inactive area is shaded in grey and houses a number of non-pixel, non-display-active components. Indeed, Kwon expressly teaches that “the *inactive area surrounds a* rectangular shape *active area*.” Ex-1005, 5:21-23.

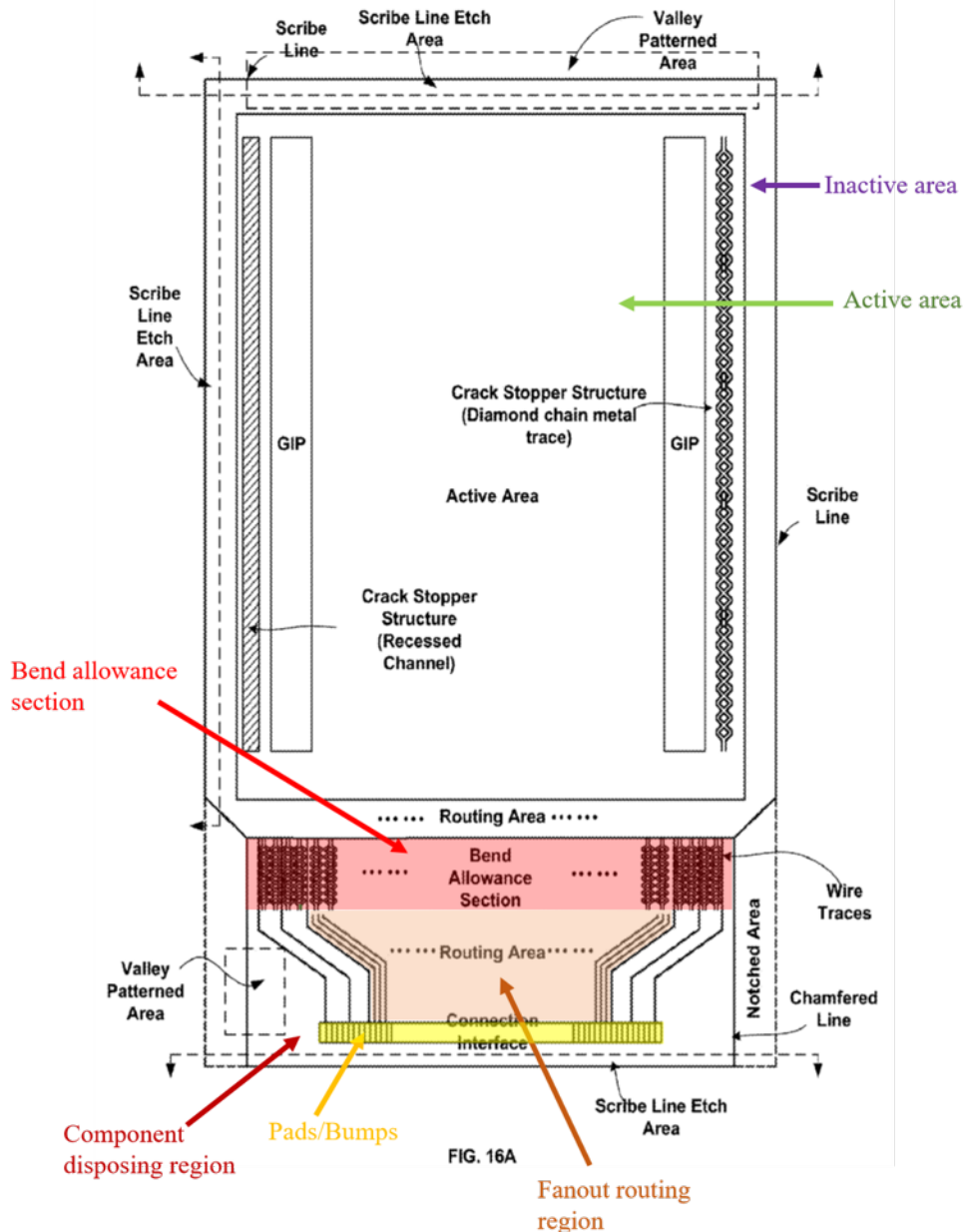


90. Kwon also teaches that the non-display region extends to form a bending region, a fanout routing region, and a component disposing region, which has a plurality of component connecting pads at its end. The “component disposing region” of the ’891 Patent “is disposed under the display region” and “configured for disposing a plurality of traces (not shown) and at least one control chip.” Ex-1001, 1:46-49, Fig. 6 (annotated below (maroon)). The “fanout routing region” of the ’891 Patent “is disposed within the component disposing region” and “has a plurality of traces configured for connecting the display region” and the control chip,

“thereby controlling the display region [] by the control chip.” Ex-1001, 1:49-54,
Fig. 6 (orange).



91. As shown in annotated Figure 16A below, like the '891 Patent, Kwon's non-display region (i.e., inactive area (dark purple)) extends to form a bending region (red), which Kwon calls a “Bend Allowance Section,” a fanout routing area (orange), which Kwon calls a “Routing Area,” and a component disposing region (maroon) that includes at its end what Kwon calls a “connection interface” (yellow). Ex-1005, Fig. 16A.



92. Specifically, Kwon teaches a component disposing region that includes an “inactive area with the connection interface [that] can be bent away from the plane of the adjacent portion of the flexible display so that the printed circuit (e.g., COF, PCB and the like) is positioned at the rear side of the flexible display 100.” Ex-1005, 5:50-54. Kwon teaches that “bending the inactive area allows to minimize or to

eliminate the inactive area to be seen from the front side of the assembled flexible display 100.” Ex-1005, 6:65-67. Kwon teaches that “the bend allowance section” is “between the active area and the inactive area where the external printed circuit is attached thereto.” Ex-1005, 34:7-9. Kwon’s bend allowance section corresponds to the recited “bending region,” which is formed by an extension of the inactive area, as shown in Figure 16A above.

93. Notably, Kwon teaches several bend regions in the inactive areas around multiple edges of the flexible display 100. But the specific “bending region” corresponding to this claim element is the bottom bend region in Kwon’s Figure 1 (also referred to specifically as the “bend allowance section” in Kwon’s Figure 16A). Ex-1005, Figs. 1, 16A.

94. Kwon’s “connection interface” is part of the recited “component disposing region” because, like the ’891 Patent, Kwon’s connection interface is bent, by way of the bend area, to be disposed under the display region and configured to dispose a plurality of traces and at least one control chip. Ex-1001, 1:46-49. As Kwon explains “some of the components, such as data drive-IC, may be mounted on a separate printed circuit and coupled to a connection interface (Pads/Bumps, Pins) disposed in the inactive area using a printed circuit such as flexible printed circuit board (PCB), chip-on-film (COF), tape-carrier-package (TCP) or any other suitable technologies.” Ex-1005, 5:44-50. With respect to the ’891 Patent, the component

disposing region is a zone on a flexible substrate that is configured for electronic chips and components. Kwon teaches this concept with similar function and relative position. Kwon's region is under the display panel where the control chip and connection traces are disposed.

95. Moreover, Kwon's routing area corresponds to the recited "fanout routing region" because, like the '891 Patent, it is disposed in the component disposing region, and includes a plurality of traces that connect to the pads on the "connection region" with an attached, e.g., COF device. Ex-1005, 22:4-9, 31:23-31.

96. Additionally, as I explained in the Technology Background section (see Section IV.A.), display panels having an active region and a non-display region disposed around the active region and extending to form a bending region, a fanout routing region, and a component disposing region having a plurality of component connecting pads were well known by 2018.

- c. **1[b]: wherein a first section of a first power trace is disposed within the non-display region around the active region, the first section of the first power trace is connected to a second section of the first power trace disposed within the component disposing region, and the second section of the first power trace is connected to the plurality of component connecting pads; and**

97. In my opinion, Kwon teaches Element 1[b].

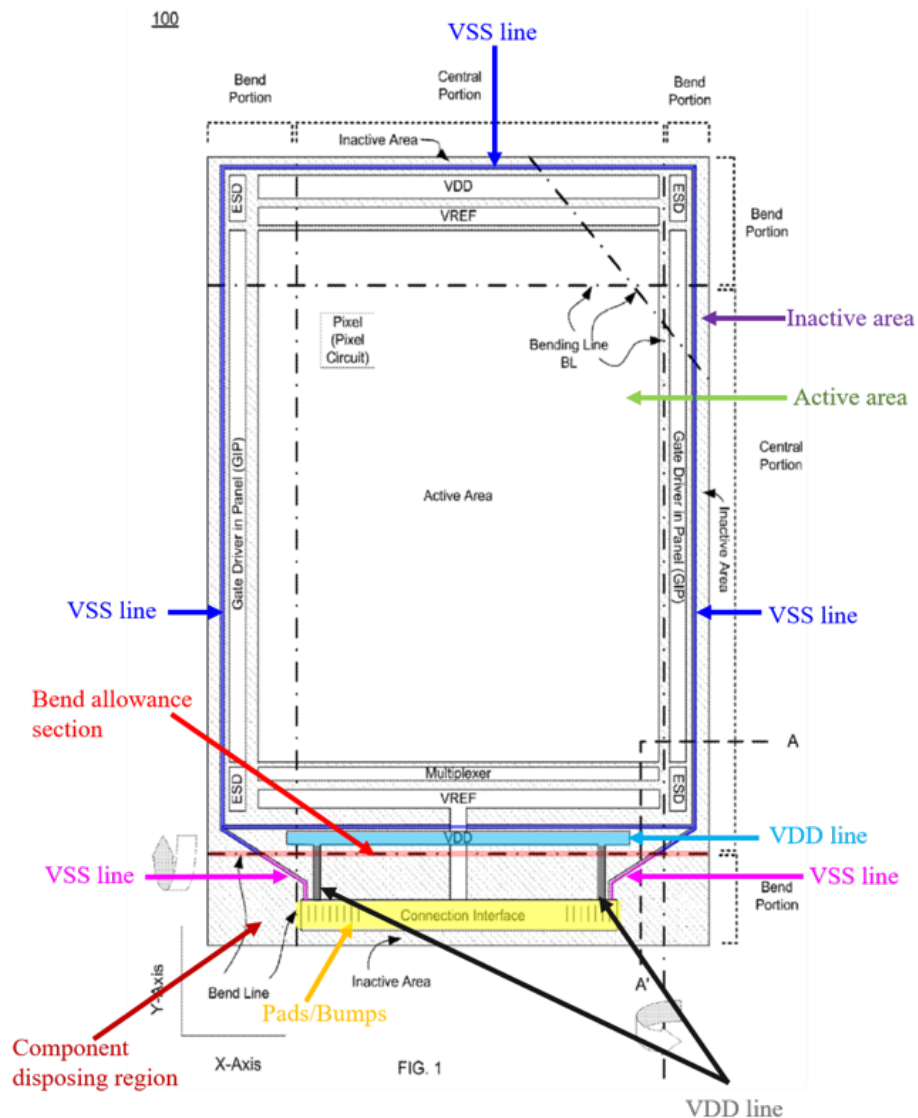
98. Although the recited "first section of a first power trace" and "second section of the first power trace" are admittedly prior art components (*see* Section V),

Kwon also teaches that its display panel comprises a “first section of a first power trace” and “second section of the first power trace.”

99. Kwon teaches that a first section of a first power trace is disposed within the non-display region around the active region. Kwon teaches “*a VSS line* and a VDD line in the flexible display 100.”⁷ Ex-1005, 28:38-41. Specifically, Kwon’s VSS located around the active area corresponds to the recited “first section of a first power trace.” Kwon teaches that “[v]arious signal lines, including but not limited to, the data signal lines from the display D-IC and *the VDD/VSS lines ... may be routed in the GIP input signal line area.*” Ex-1005, 35:55-61. This is shown in Kwon’s Figure 1, annotated below (VSS line in dark blue). All of these features are located in a non-display area, which Kwon identifies as the “inactive area” with grey shading in its Figure 1. Moreover, Kwon’s main power supply bus line running along the periphery of the active area is structurally positioned between the active pixel matrix and the bending region. In Kwon, power signals originate from the driver IC control chip located on the pad area (the component disposing region). A power line section exists in this IC pad area to distribute or receive power to and from the IC control

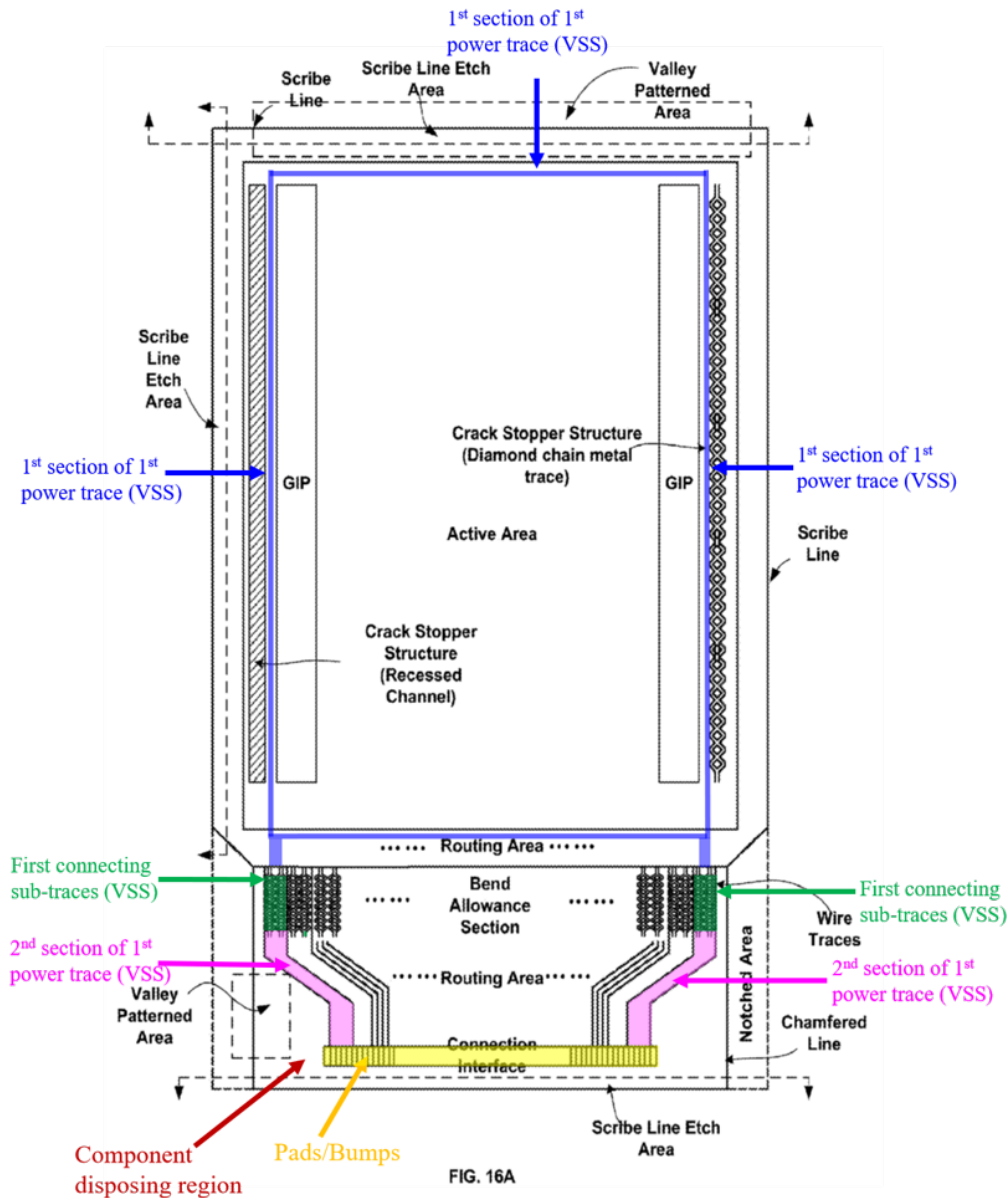
⁷ “VDD” stands for “Voltage Drain Drain” which is high, and the VDD line is the path through which current flows from outside the panel into the OLED (specifically, into the anode of the OLED). “VSS” stands for “Voltage Source Source” which is low, and the VSS line is the path through which current flows out of the OLED (specifically, from the cathode of the OLED) to the outside of the panel. Therefore, the VDD line and the VSS line must always exist together.

chip. In Kwon, across the flexible bending area, power is routed in addition to signal lines as multiple parallel, narrow, bend-resilient conductive traces to minimize mechanical stress and prevent wire breaking during bending. The power line connects to the input and output bonding pads which are configured to receive the display driver IC or COF output terminals.



100. Kwon's VSS lines routed in the GIP input signal area correspond to recited first section of a first power trace. *See, e.g.*, Ex-1001, 6:48-49 ("the first section 206 of the first power trace is a low-potential power trace (VSS)"). As shown in annotated Figure 16A below, (with Kwon's VSS lines (blue) from Figure 1 overlayed), the VSS lines are disposed within the inactive region around the active region of the display panel, because the GIP (Gate Driver in Panel) where they are routed surrounds the active area in Kwon's inactive area. Ex-1005, 36:32-37, Fig. 16A.⁸

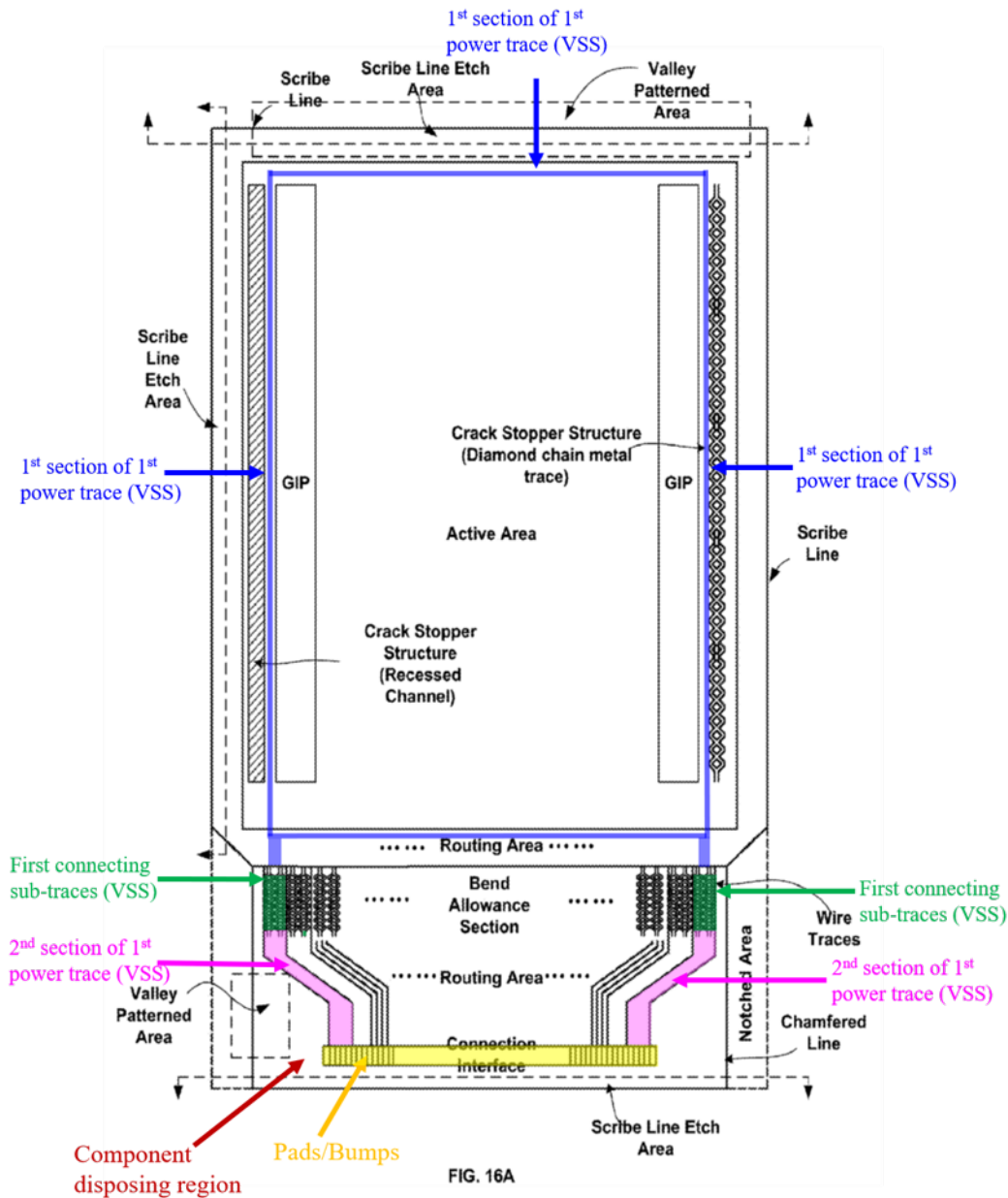
⁸ Generally, unlike the anode, which consists of multiple individual electrodes, the cathode connected to the low-potential power trace 107 is formed as a single, large-area common electrode. Consequently, electrical contact between the cathode and the low-potential power trace 107 is established along the edges of this common electrode. Therefore, it is well-known in the art for a low-potential power trace to substantially surround the display region. This is illustrated in annotated Fig. 2 (Prior Art) of the '891 Patent (see Section V), where the low-potential power trace 107 is shown substantially surrounding the display region.



101. Kwon teaches that the first section of the first power trace (VSS) is connected to a second section of the first power trace disposed within the component disposing region. Kwon teaches that “[s]ome conductive lines may be routed from the substantially flat portion to the bend portion of the flexible display 100.” Ex-1005, 20:8-10. Specifically, Kwon teaches that “[t]he wire trace ... may extend

across the bend allowance section and routed to pads for COF or other components of the flexible display 100.” Ex-1005, 33:40-43. Kwon’s wire traces (pink) in the routing area that connect to the component disposing region (maroon) and its included connection interface (yellow) correspond to the recited “second section of the first power trace disposed within the component disposing region.”

102. As shown in annotated Figure 16A below, the first section of the first power trace (i.e., VSS lines (blue)) is connected by sub-traces (green) through the bend allowance section to a second section of the first power trace disposed within the component disposing region (i.e., pink), as recited. Ex-1005, Fig. 16A, 25:42-44 (“a wire trace includes at least two sub-traces arranged to form a trace design resembling a chain with a series of connected links”), 28:32-34 (“wire trace may split into additional number of subtraces, resulting series of links arranged in a grid-like configuration”).



103. As shown in annotated Figure 16A above, Kwon further teaches that the second section of the first power trace (pink) is connected to the plurality of component connecting pads (yellow) within the component disposing region (maroon), as recited. Ex-1005, Fig. 16A, 33:40-43 (“The wire trace, ... may extend across the bend allowance section and *routed to pads for COF* or other components

of the flexible display 100.”); *see also id.*, 21:54-55 (“a pad for receiving one or more signals may be provided on one end of the conductive lines”), 44:7-8 (“part of the conductive lines can serve as a connector (e.g., pads or pins)”).

104. In annotated Figure 16A of Kwon above, features such as Crack Stopper Structure⁹, Notched area¹⁰, Scribe Line etch area¹¹ and Valley patterned Area¹²—which can be applied to the basic structure shown in annotated Figure 1—are described. However, since these features do not necessitate changes to the basic VDD and VSS structure shown in annotated Figure 1, the VDD and VSS structure in annotated Figure 16A remain substantially identical to those in annotated Figure 1.

105. Additionally, as I explained in the Technology Background section (see Section IV.B.), display panels wherein a first section of a first power trace is disposed within the non-display region around the active region and connected to a second section of the first power trace disposed within the component disposing

⁹ It prevents cracks originating from the edge during the scribing process from propagating to the Active Area.

¹⁰ It trims both sides of the bending allowance section to reduce its size, facilitating easier bending.

¹¹ An area where the buffer layer, which facilitates crack propagation from the edge during the scribing process, is intentionally removed from a specific region near the panel edge.

¹² An area having a narrow line connected to the connector. The narrow line is to be cut by the edge scribing process.

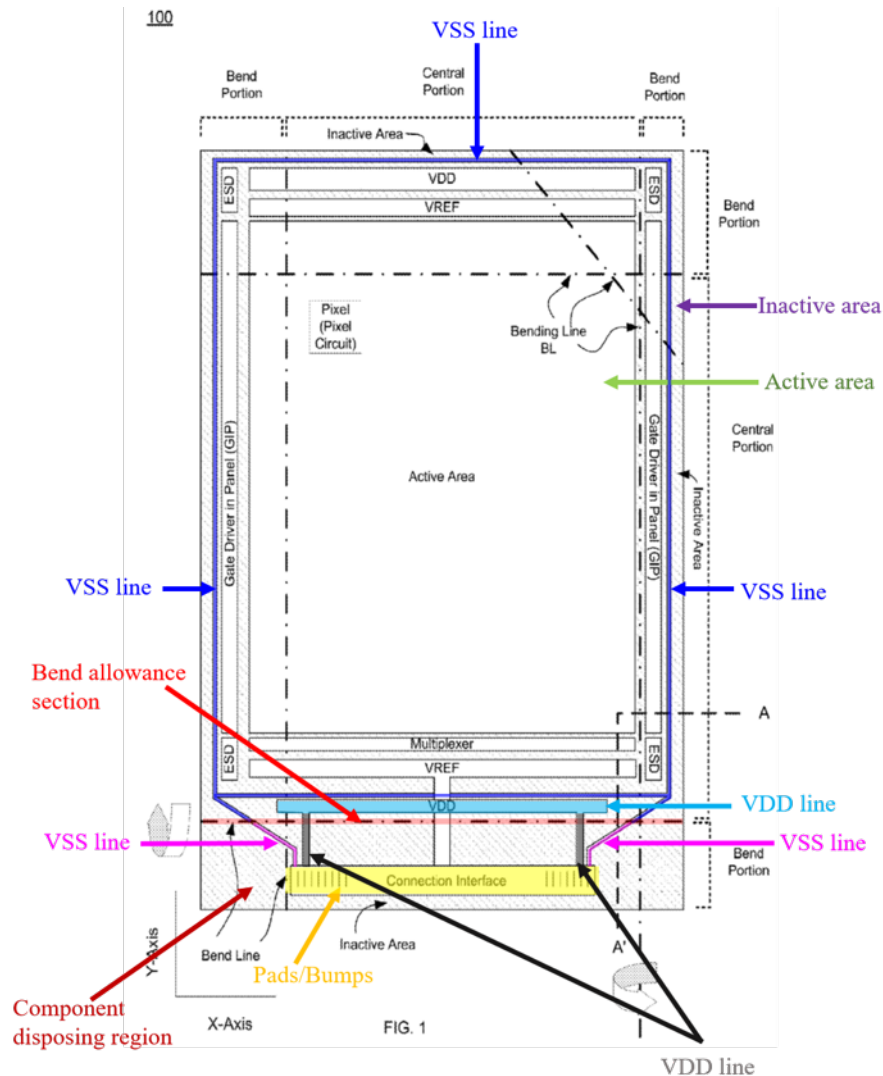
region and the second section of the first power trace is connected to the plurality of component connecting pads were well known by 2018.

- d. **1[c]: a first section of a second power trace is disposed adjacent to the active region and disposed between the active region and the bending region, the first section of the second power trace is connected to a second section of the second power trace disposed within the component disposing region by at least a set of second connecting sub-traces disposed within the bending region, and the second portion of the second power trace is connected to the plurality of component connecting pads,**

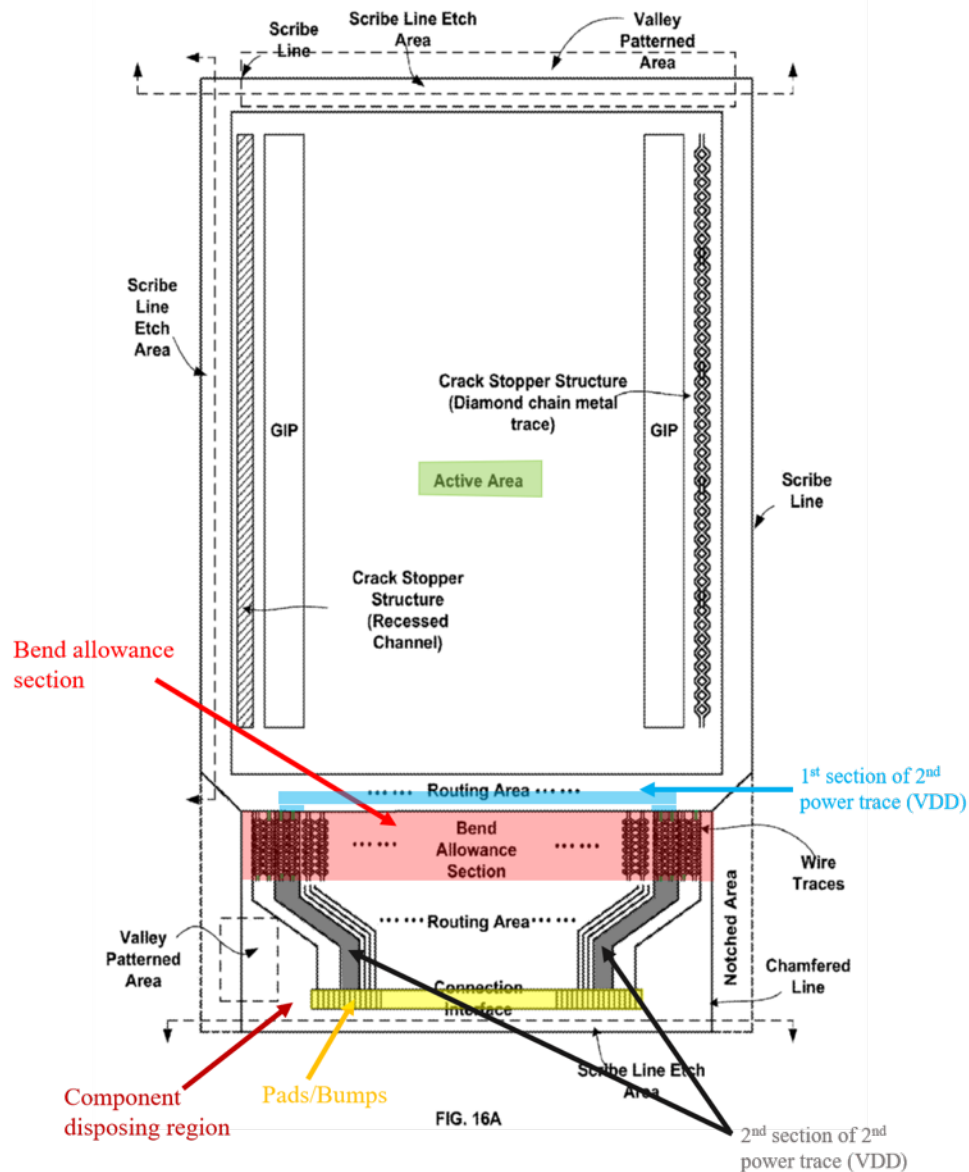
106. In my opinion, Kwon teaches Element 1[c].

107. Although the recited “first section of a second power trace” and “second section of the second power trace” are admittedly prior art components (*see* Section V), Kwon also teaches that its display panel comprises “a first section of a second power trace ... connected to a second section of the second power trace.”

108. Specifically, Kwon teaches that a first section of a second power trace is disposed adjacent to the active region, between the active region and the bending region. Specifically, Kwon’s VDD line (light blue) is a second power trace disposed between the active region and the bend allowances section, as shown in annotated Figure 1. *See, e.g.*, Ex-1001, 7:34-36 (“the first section 208 of the second power trace is a high-potential power trace (VDD)”).



109. As shown in annotated Figure 16A below, (with Kwon's VDD lines (light blue) from Figure 1 overlaid), the VDD line is disposed adjacent to the active region (immediately below it) and disposed between the active region and the bend allowance section. Ex-1005, Fig. 16A. To be clear, the "second power trace" corresponds to Kwon's VDD line, and the "first section" of the section power trace corresponds to the portion of the VDD line that sits between the active area and the bend allowance section.



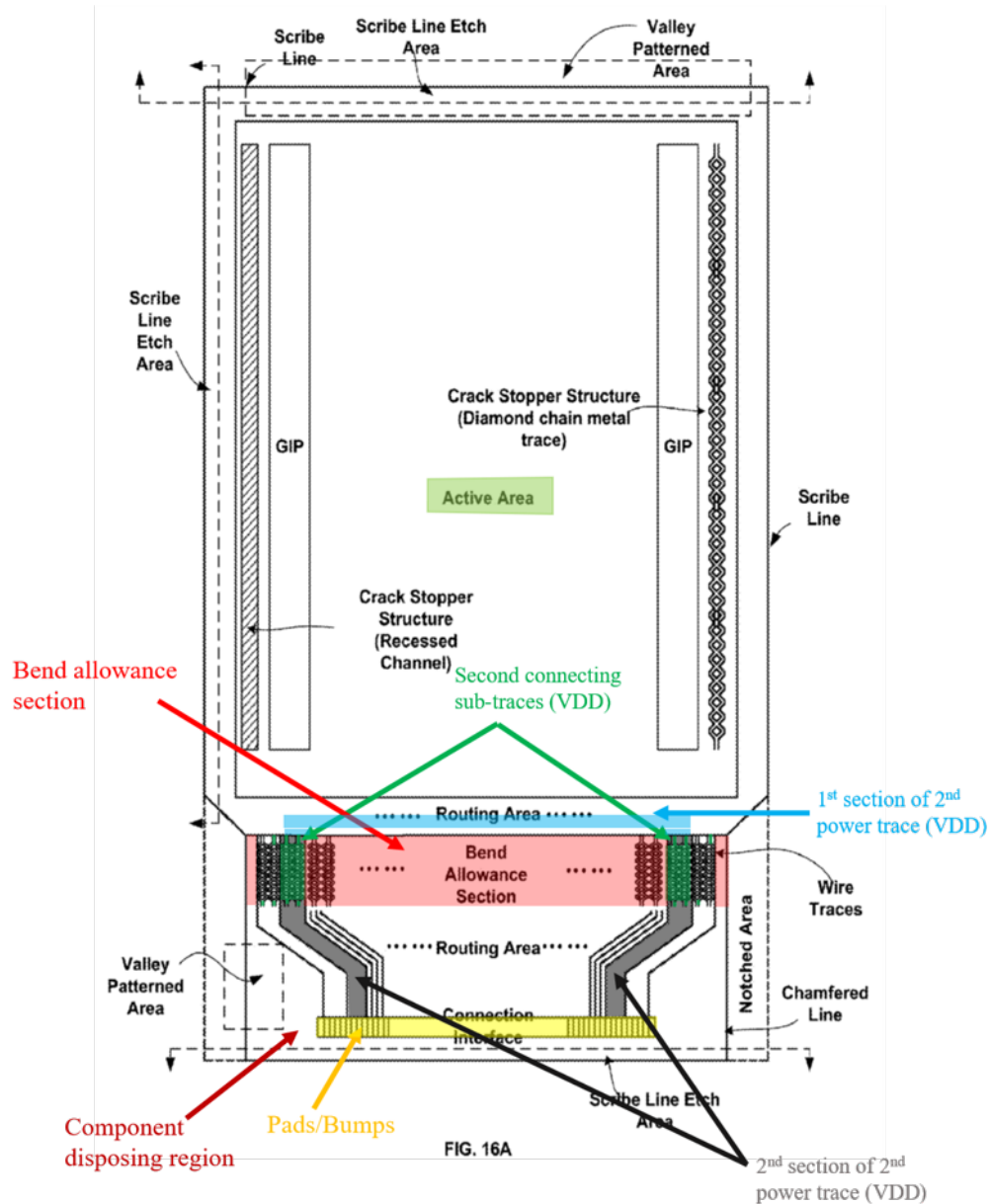
110. Just like for the VSS line discussed above, a VDD “wire trace may split into additional number of sub-traces, resulting series of links arranged in a grid-like configuration” such that it is configured, for example, “as a web of diamond trace shapes.” Ex-1005, 28:32-35. Kwon further explains that the “**VDD line** in the flexible display 100 may have the grid-like trace design, especially if such lines are *arranged to cross over a bend allowance section*.” Ex-1005, 28:38-41.

111. Kwon thus teaches that the first section of the second power trace is connected to a second section of the second power trace disposed within the component disposing region by at least a set of second connecting sub-traces disposed within the bending region as shown in Figure 16A.

112. Specifically, Kwon teaches that “[s]ome conductive lines may be routed from the substantially flat portion to the bend portion of the flexible display 100.” Ex-1005, 20:8-10. Indeed, “[t]he wire trace ... may extend across the bend allowance section and routed to pads for COF or other components of the flexible display 100.” Ex-1005, 33:40-43. To be clear, Kwon’s wire traces (grey) in the routing area after the bend allowance section, which connect to the connection interface (yellow) within the component disposing region (maroon) correspond to the recited “second section of the second power trace disposed within the component disposing region.”

113. As shown in annotated Figure 16A below, the first section of the second power trace (i.e., VDD line (light blue)) is connected by at least a set of second connecting sub-traces (green) disposed within the bending region (red) to a second section of the second power trace disposed within the component disposing region (grey), as recited. Ex-1005, Fig. 16A, 25:42-44 (“a wire trace includes at least two sub-traces arranged to form a trace design resembling a chain with a series of

connected links”), 28:32-34 (“wire trace may split into additional number of subtraces, resulting series of links arranged in a grid-like configuration”).



114. As shown in annotated Figure 16A above, the second section of the second power trace (grey) is connected to the plurality of component connecting pads (yellow) within the component disposing region (maroon). Ex-1005, Fig. 16A,

33:40-43 (“The wire trace ... may extend across the bend allowance section and *routed to pads for COF* or other components of the flexible display 100.”).

115. Kwon also includes Figure 16B, providing a blow up and further explanation of the use of its subtraces crossing the bending region. Specifically, “FIG. 16B is an enlarged view of lower left corner of the flexible display near the notched area.” Ex-1005, 37:17-18. As shown in annotated Figure 16B below, the upper-most portion of the VDD line (light blue, “first section of second power trace”) is connected the lower portion (grey, “second section of the second power trace”) via a mesh/grid subtrace (green, “second connecting subtrace”) that passes through the bend allowance section. Ex-1005, Fig. 16B.

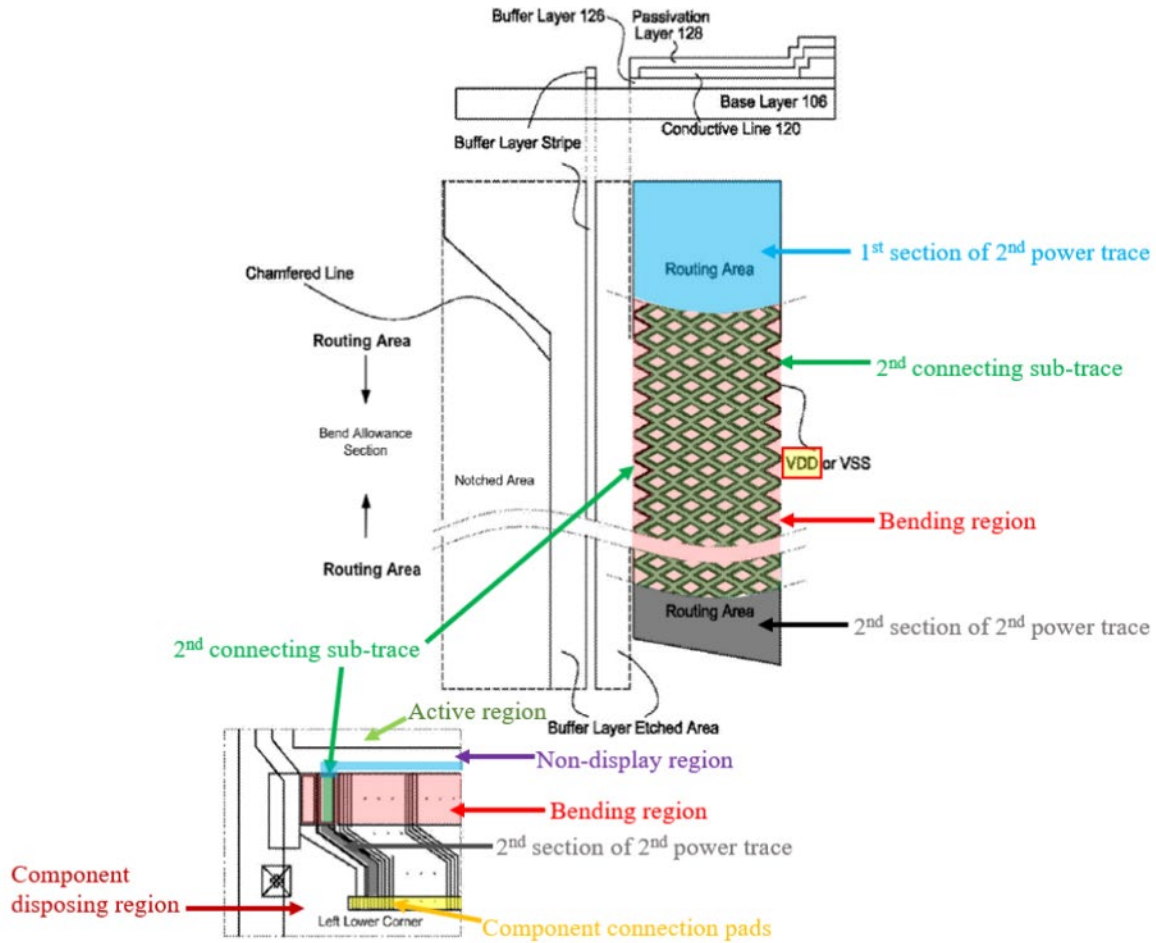
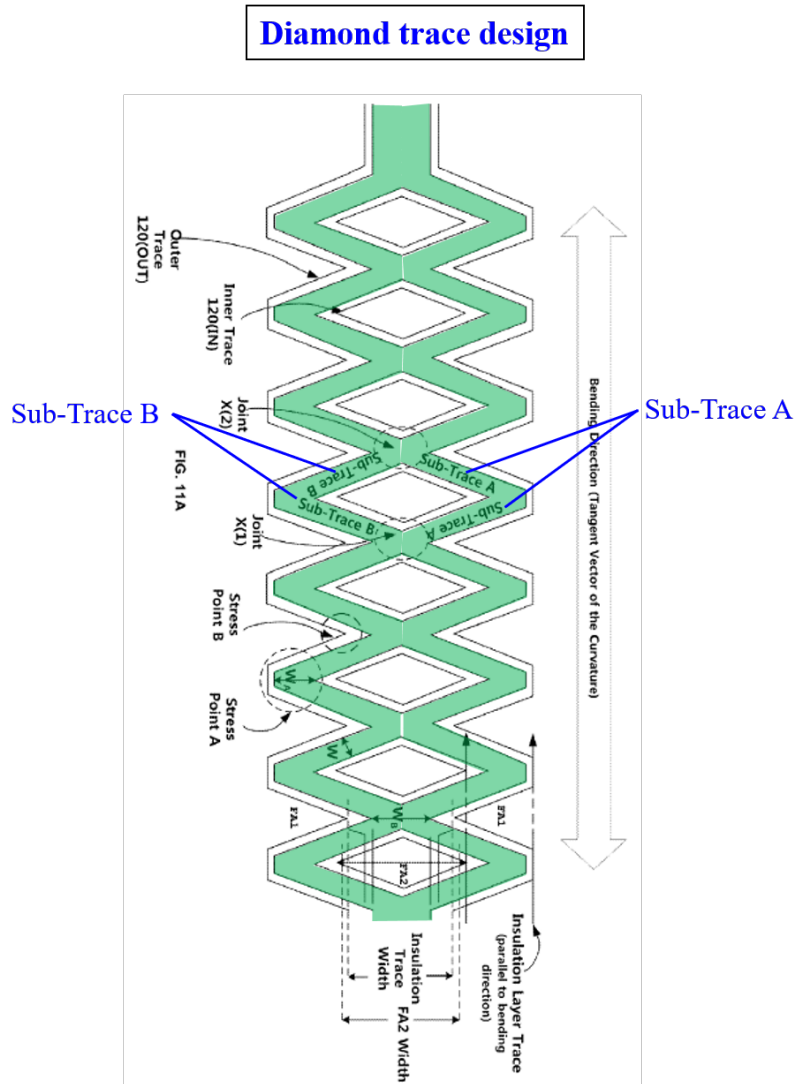


FIG. 16B

116. Kwon teaches that “a wire trace can be configured as a web of diamond trace shapes as illustrated in FIG. 11B,” “such a trace design is particularly useful for receiving a wire trace that transmit a common signal to multiple points or for a wire trace that require a very low electrical resistance,” “for example, a VSS line and a VDD line in the flexible display 100 may have the grid-like trace design, especially if such lines are arranged to cross over a bend allowance section.” Ex-1005, 28:34-41. Kwon also teaches that “the grid-like wire trace shown in FIG. 11B can converge back to form the diamond trace shown in FIG. 11A.” Ex-1005, 28:47-

50. Kwon also teaches that “one or more of power signal wires of the flexible display 100, such as the VDD and/or the VSS, has the grid-like wire trace formed of multiple diamond-chain traces adjoined side-by-side as depicted in FIG. 21.” Ex-1005, 43:28-32. Based on the above teachings of Kwon, the VDD and/or VSS in the bend allowance section can have the strain-reducing trace design shown in annotated Fig. 11A, 11B and 21. Ex-1005, Figs. 11A-11B, 21.

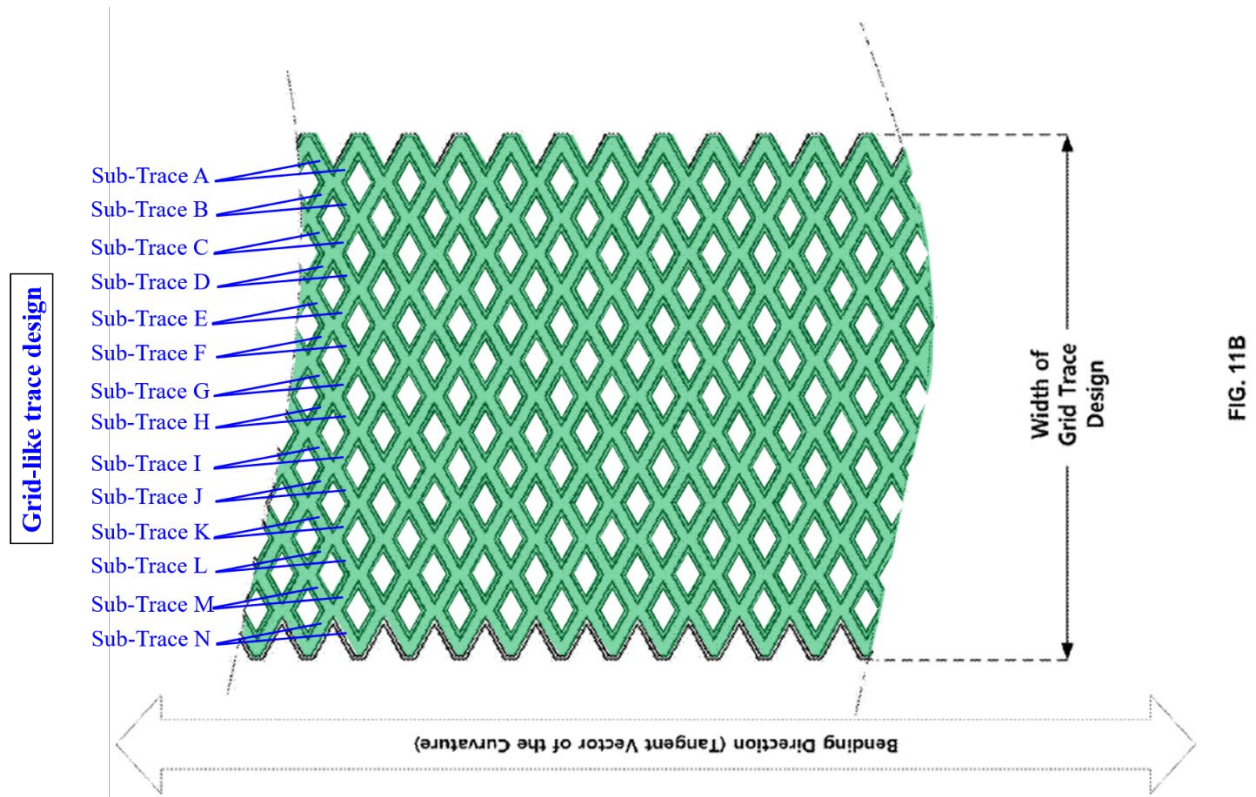
117. Kwon teaches that “[r]eferring to FIG. 11A, the conductive line 120 includes sub-trace A and sub-trace B, which are split away from each other and merge back at each joint X,” “in this example, the shape of the conductive lines” and “[t]he other end of line 120 between the joint X(1) and X(2) (i.e., link) has a diamond shape with an open area surrounded by the sub-trace A and the sub-trace B,” “with additional joints X, the conductive line may 120 forms a chain of diamond shaped links, and thus the trace design may be referred to as the diamond trace design.” Ex-1005, 25:48-67. Referring to annotated Figure 11A below, one wire trace of the diamond trace design has two sub-traces consisting of Sub-Trace A and Sub-Trace B.



118. Referring again to annotated Figure 16A above, in either the right or left portion of the bending allowance section, the first and second sections of the second power trace are connected by two second connecting sub-traces (green) each having the diamond trace design. Since one second connecting sub-trace possesses the two sub-traces as described in annotated Figure 11A, the first and second sections of the second power trace in either the right or left portion of the bending allowance section are connected by a set of four sub-traces.

119. Alternatively, unlike the configuration shown in annotated Figure 16A, even in cases where the first and second sections of the second power trace are connected by a single second connecting sub-trace, that single second connecting sub-trace still comprises two sub-traces as illustrated in annotated Figure 11A. Consequently, the first and second sections of the second power trace in either the right or left portion of the bending allowance section are connected by a set of two sub-traces.

120. Alternatively, annotated Figure 11B shows a grid-like trace design. The grid-like trace design below has 14 Sub-traces from Sub-Traces A to N counted in the same manner as shown in annotated Fig. 11A. Consequently, the first and second sections of the second power trace in either the right or left portion of the bending allowance section are connected by a set of 14 Sub-traces from Sub-Traces A to N.



121. Alternatively, annotated Figure 21 shows another grid-like trace design. The grid-like trace design below has 24 Sub-traces from Sub-Traces A to X counted in the same manner as shown in annotated Fig. 11A. Consequently, the first and second sections of the second power trace in either the right or left portion of the bending allowance section are connected by a set of 24 Sub-traces from Sub-Traces A to X.

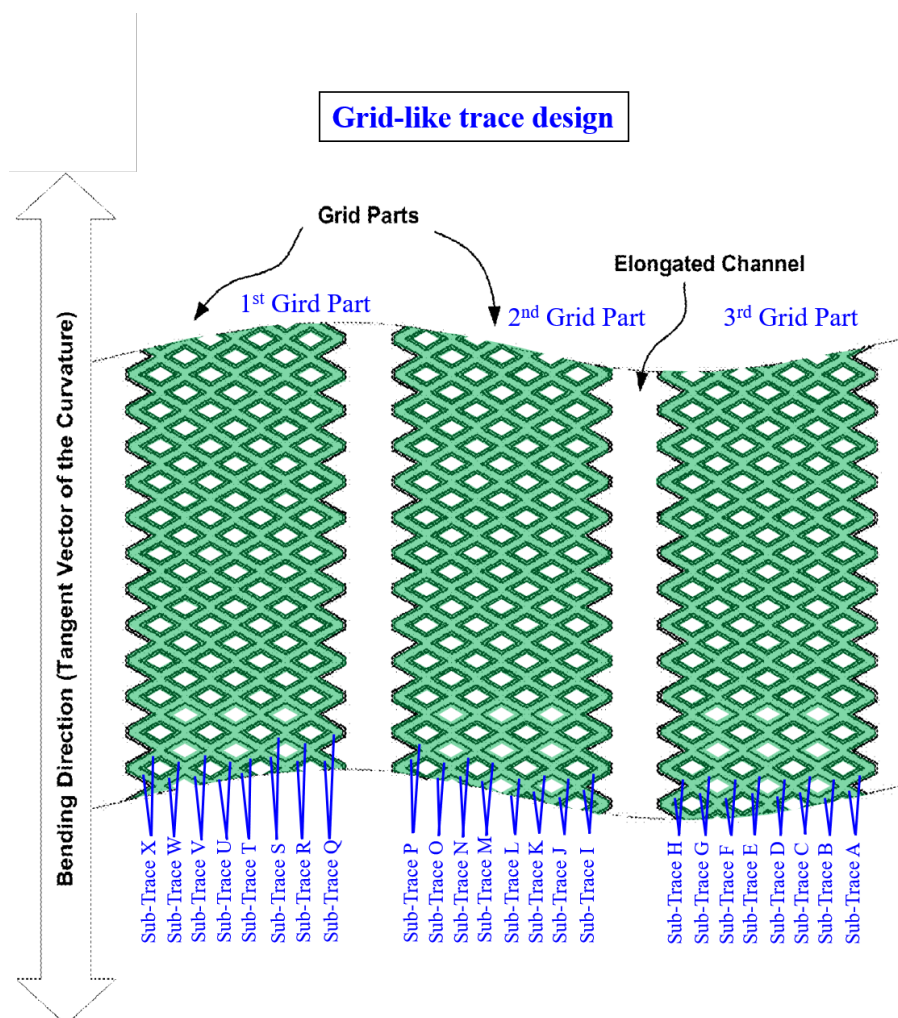


FIG. 21

122. Alternatively, regarding annotated Figure 21, Kwon teaches that “a wire trace with a grid-like trace strain-reducing trace design is provided with an elongated channel between divided grid-parts of the wire trace.” Ex-1005, 42:53-55. “It should be noted that the separated parts of the wire trace on one side of the elongated channel is connected to the part of the wire trace on the opposite side of the elongated channel, and thus both parts of the wire trace transmit the identical signal. The connection between the divided parts of the wire trace may be achieved

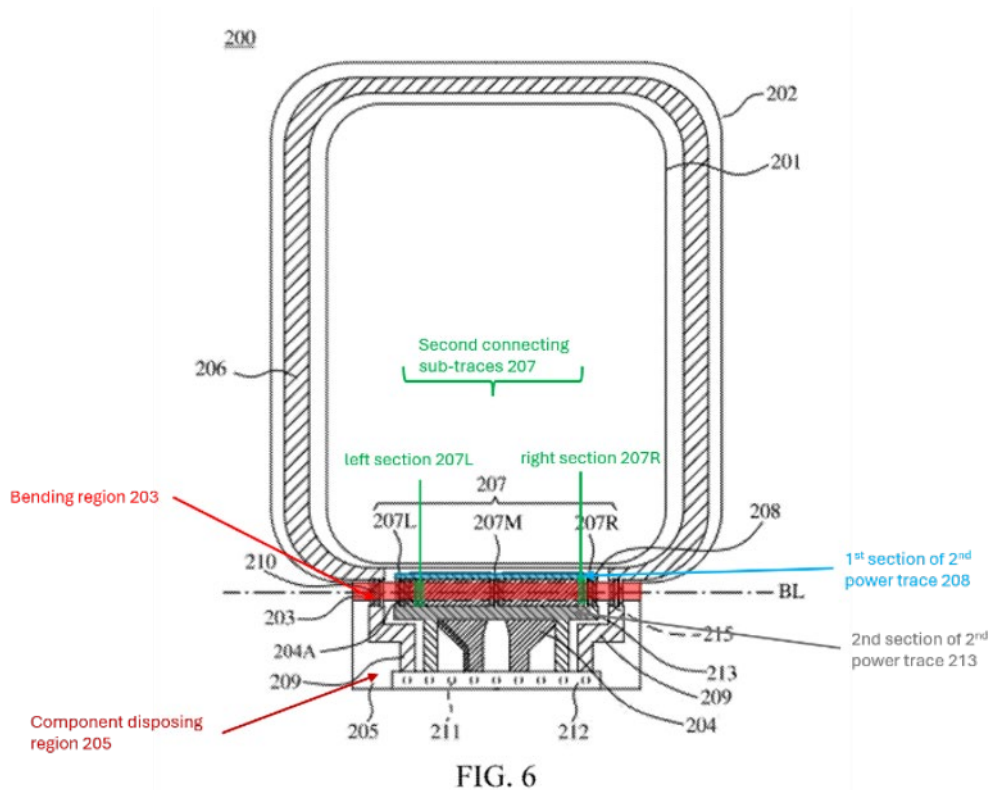
at one or both ends of the wire trace by a conductive path, which may be a part of the wire trace. The connection of the divided parts of the wire trace may be achieved within the bend allowance section or outside the bend allowance section.” Ex-1005, 42:63-43:5. Here, 1st Grid Part, 2nd Grid Part and 3rd Grid part which extend along the elongated channel correspond to the claimed second connecting sub-traces. Consequently, the first and second sections of the second power trace in either the right or left portion of the bending allowance section are connected by a set of three second connecting sub-trace which are the 1st to 3rd Grid parts.

123. Additionally, as I explained in the Technology Background section (see Section IV.C.), display panels wherein a first section of a second power trace is disposed adjacent to the active region between the active region and the bending region and connected to a second section of the second power trace disposed within the component disposing region by at least a set of second connecting sub-traces disposed within the bending region and connected to the plurality of component connecting pads were well known by 2018.

- e. **1[d]: wherein the first section of the second power trace is separately connected to the second section of the second power trace disposed within the component disposing region by two sets of the second connecting sub-traces passing through two sections of the bending region.**

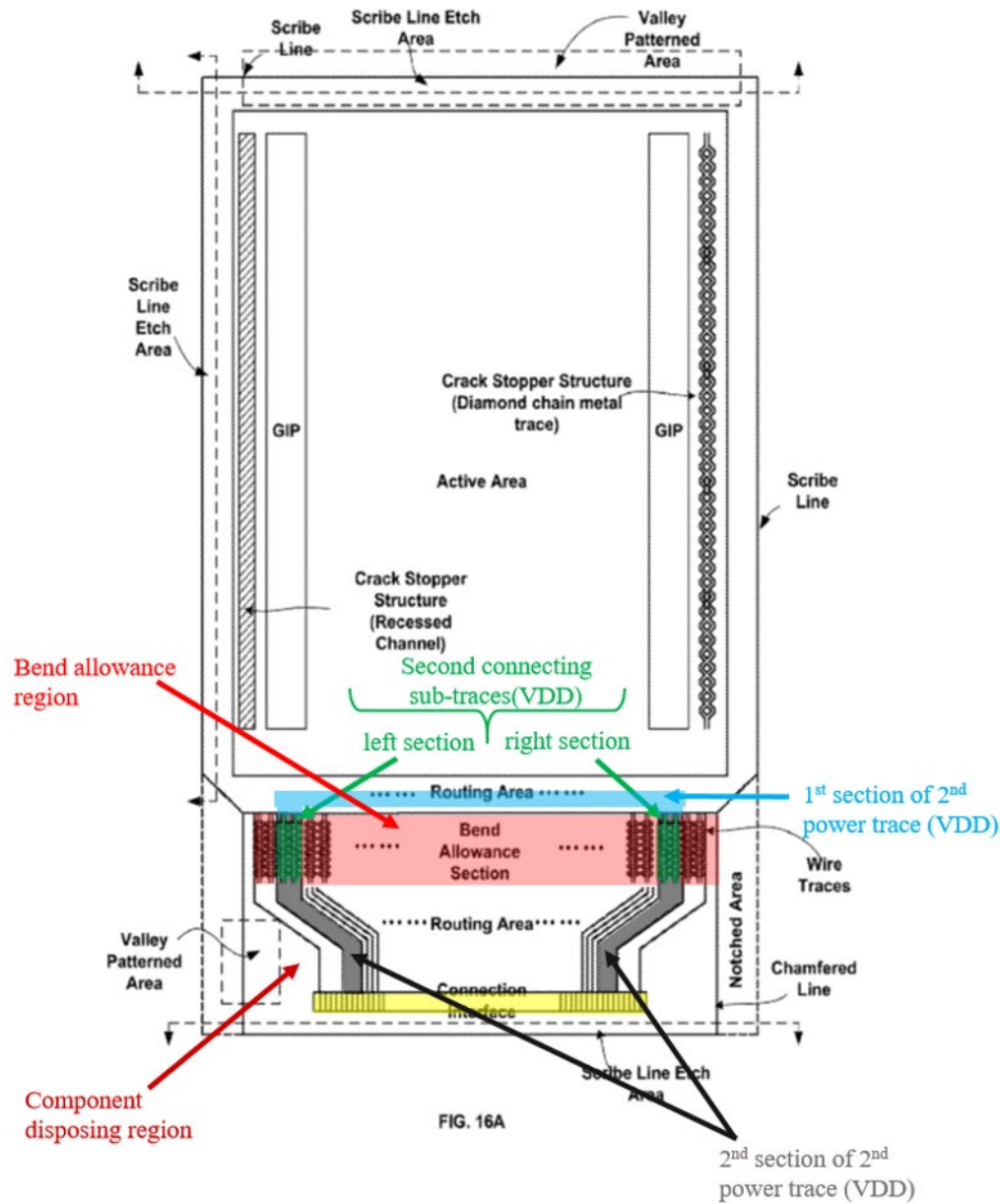
124. In my opinion, Kwon teaches Element 1[d].

125. Although the recited “two sections of the bending region” are admittedly prior art components (*see* Section V), Kwon also teaches that its display panel comprises two sections of the bending region. For example, as shown in Kwon’s figures and further explained below, the bend allowance section includes, at least, a symmetric left and right side the same way that ’891 patent does. *See, e.g.*, Ex-1001, 1:40-45 (“The display panel 100 includes a display region 101 and a non-display region 102, the non-display region 102 is distributed around the display region 101 and is *bilaterally symmetric*.”).



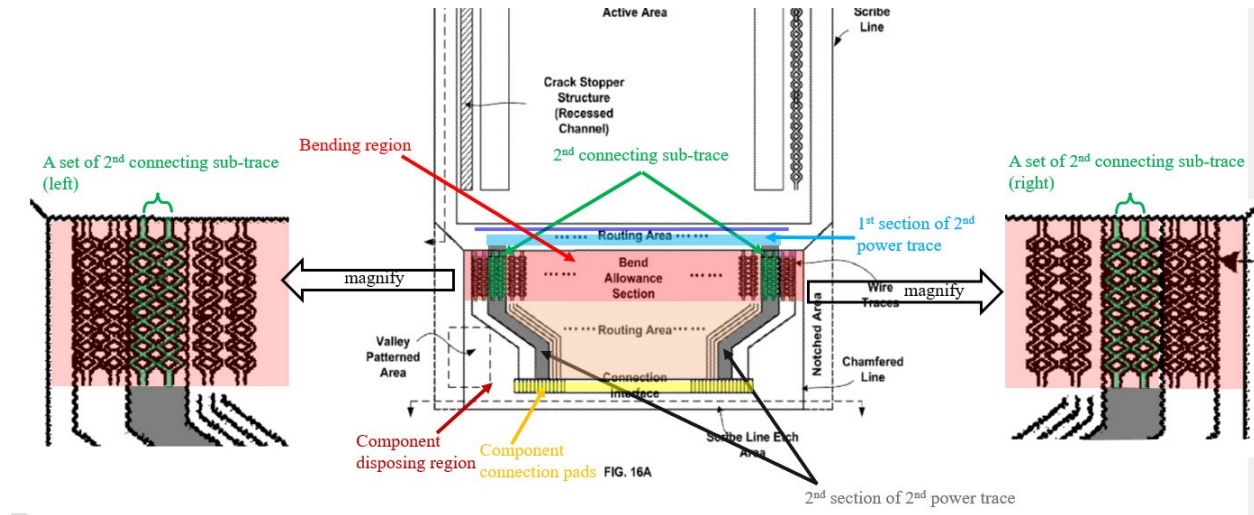
126. As explained above in connection with Element 1[c], Kwon’s VDD line corresponds to the recited second power trace. The first section (light blue), disposed

between the active area and the bend allowance section, is connected to the second section (grey) via a number of sets of subtraces (green). As shown in annotated Figure 16 below, there is a set of subtraces on the left side of the VDD line, and a set on the right side. The left-side and right-side correspond to the recited “two sections of the bending region” in the same way as the described by the ’891 Patent, because they are located on both opposing, symmetric ends of the VDD line. *See, e.g., Ex-1001, 8:7-14 (“the second connecting sub-traces 207 are **separately disposed at two ends** of the first section 208 of the second power trace and the second section 213 of the second power trace”).*



127. Both of these separate left and right sections are shown in the below cropped and annotated Figure 16A' below. Ex-1005, Fig. 16A'. As previously described, just like the '891 Patent, Kwon teaches a symmetric set of traces positioned in, at least, the left and right sides of the bend allowance section. And

these traces separately connect the first and second sections because they are distinct from each other, and positioned on opposing ends of the VDD line.



128. As I described in detail in Element 1[c], the second connecting sub-traces (green) can form sets of 2, 3, 4, 14, or 24 sub-traces in either the right or the left portion of the bending region (red). Here, since the second connecting sub-traces (green) form a set in either the right or the left portion of the bending region (red), this results in two sets.

129. Additionally, as I explained in the Technology Background section (see Section IV.D.), display panels wherein the first section of the second power trace is separately connected to the second section of the second power trace disposed within the component disposing region by two sets of the second connecting sub-traces passing through two sections of the bending region were well known by 2018.

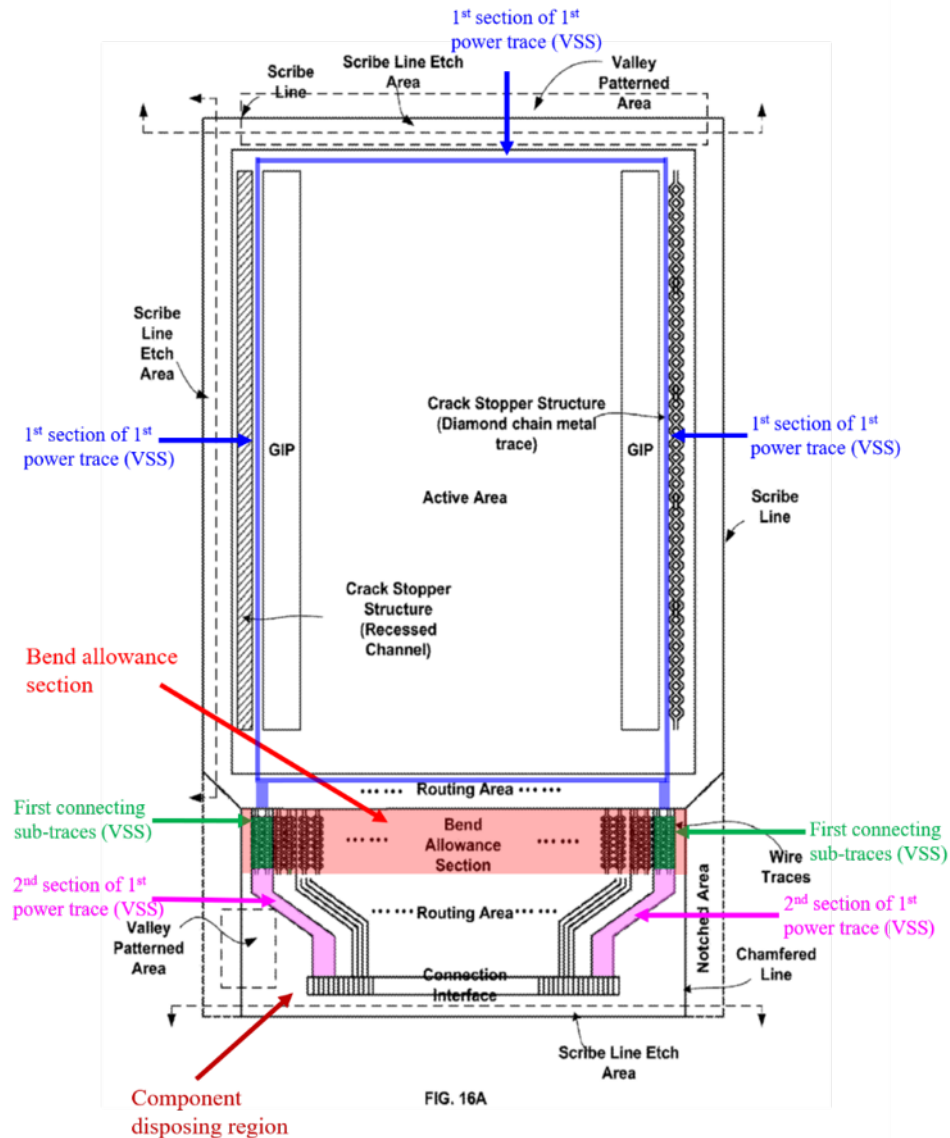
- 2. Claim 7: The display panel according to claim 1, wherein the first section of the first power trace is separately connected to the second section of the first power trace disposed within the component disposing region by a plurality of first connecting sub-traces disposed within the bending region.**

130. In my opinion, Kwon teaches Claim 7.

131. Notably, Claim 7 is very similar to claim Elements 1[c] and 1[d], just applied to the “first power trace” (VSS) as opposed to the “second power trace” (VDD). That is to say that Claim 1 does not specifically recite either “first connecting subtraces” or the “separately connected” requirements recited in Claim 7. Regardless, each of these additional features are taught in connection with Kwon’s VSS line.

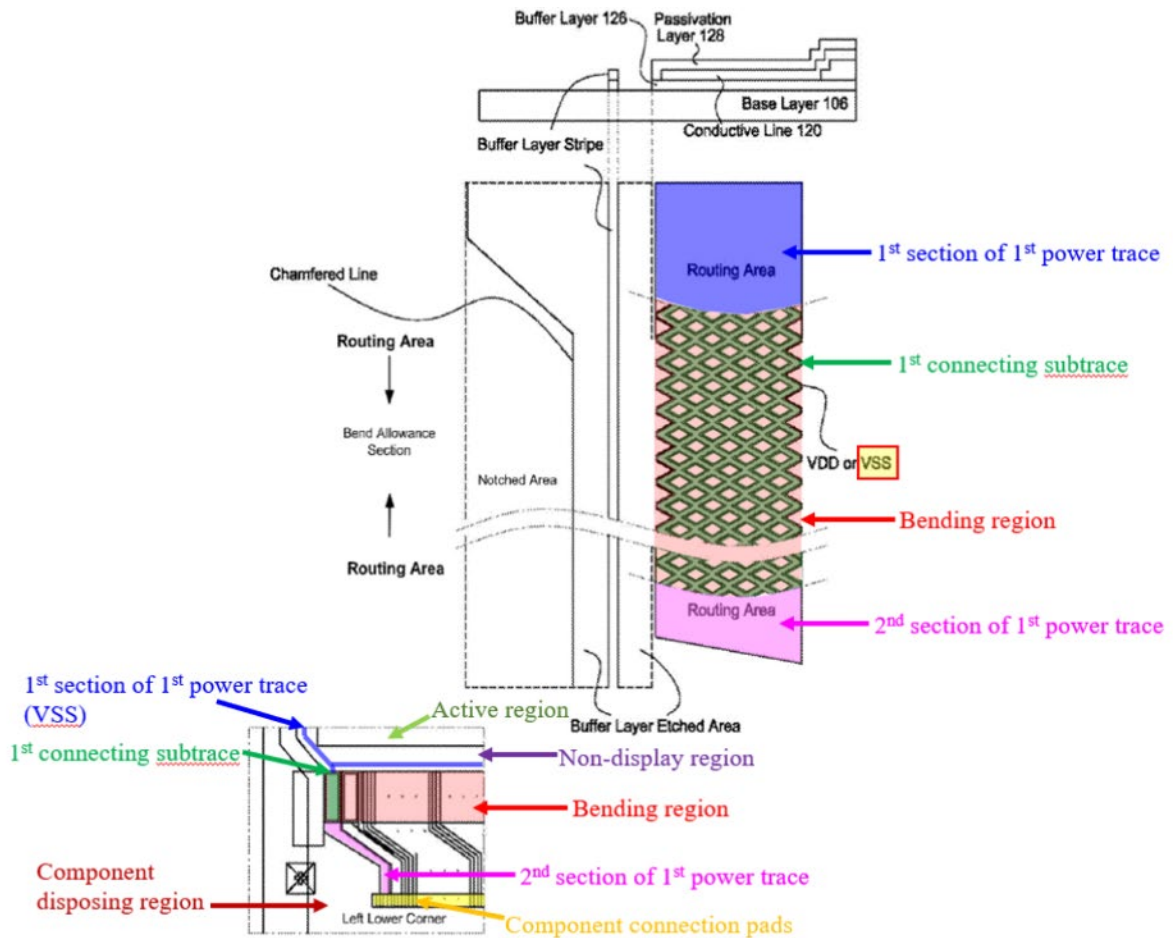
132. As explained above in connection with Element 1[b], Kwon’s VSS line corresponds to the recited first power trace. The portion of the VSS line that surrounds the active area corresponds to the recited first section of the first power trace (blue). The portion of the VSS line in the routing area below the bend allowance section (pink) corresponds to the recited second section of the first power trace. Each of these two sections are separately connected by a number of subtraces (green) that pass through the bend allowance section (red). As explained above in connection with Element 1[d], these sections are separately connected in the same was as described by the ’891 Patent because they are a symmetric set of traces

positioned in, at least, the left and right sides of the bend allowance section, and they are distinct from each other, positioned on opposing ends of the VSS line.



133. Moreover, similar to discussed above in Figure 16A for Element 1[c] and the VDD line, Kwon's Figure 16B provides a blow up and further explanation of the use of its subtraces crossing the bending region, including the VSS line.

Specifically, “FIG. 16B is an enlarged view of lower left corner of the flexible display near the notched area.” Ex-1005, 37:17-18. As shown in annotated Figure 16B below, the upper-most portion of the VSS line (blue, “first section of first power trace”) is connected the lower portion (pink, “second section of the first power trace”) via a mesh/grid subtrace (green, “first connecting subtrace”) that passes through the bend allowance section. Ex-1005, Fig. 16B.

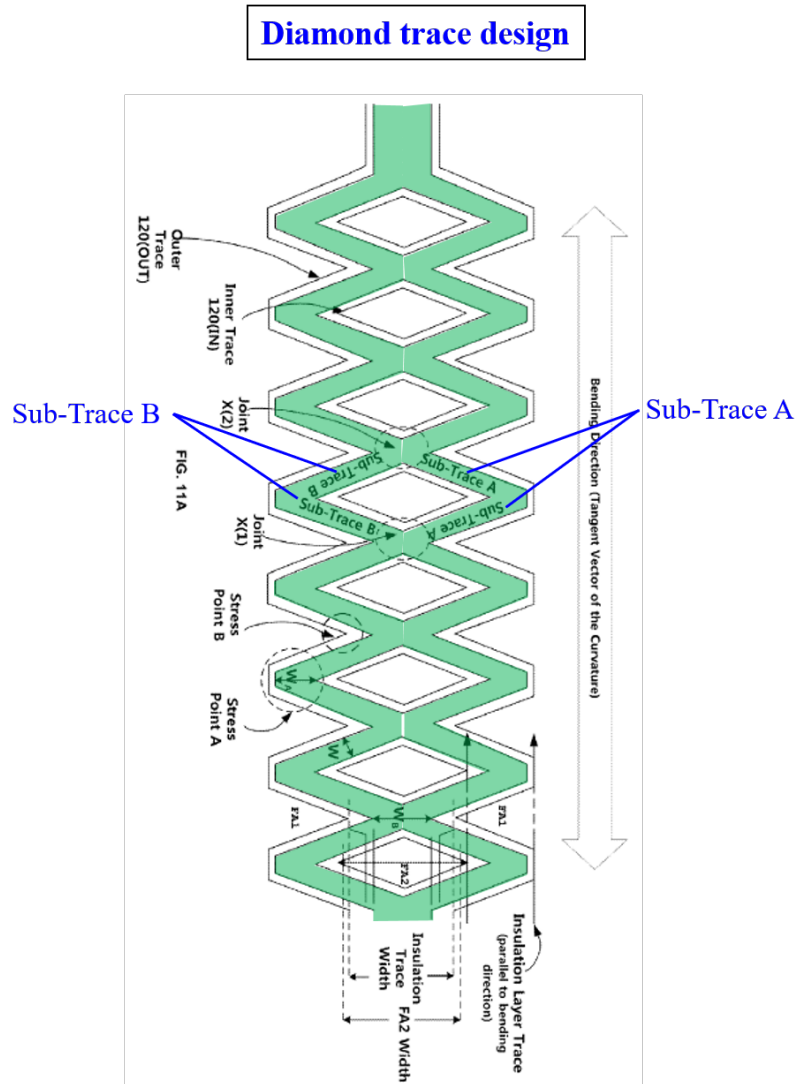


134. Referring again to annotated Figure 16A above, the number of second connecting sub-traces (green) connected between the first section of the first power

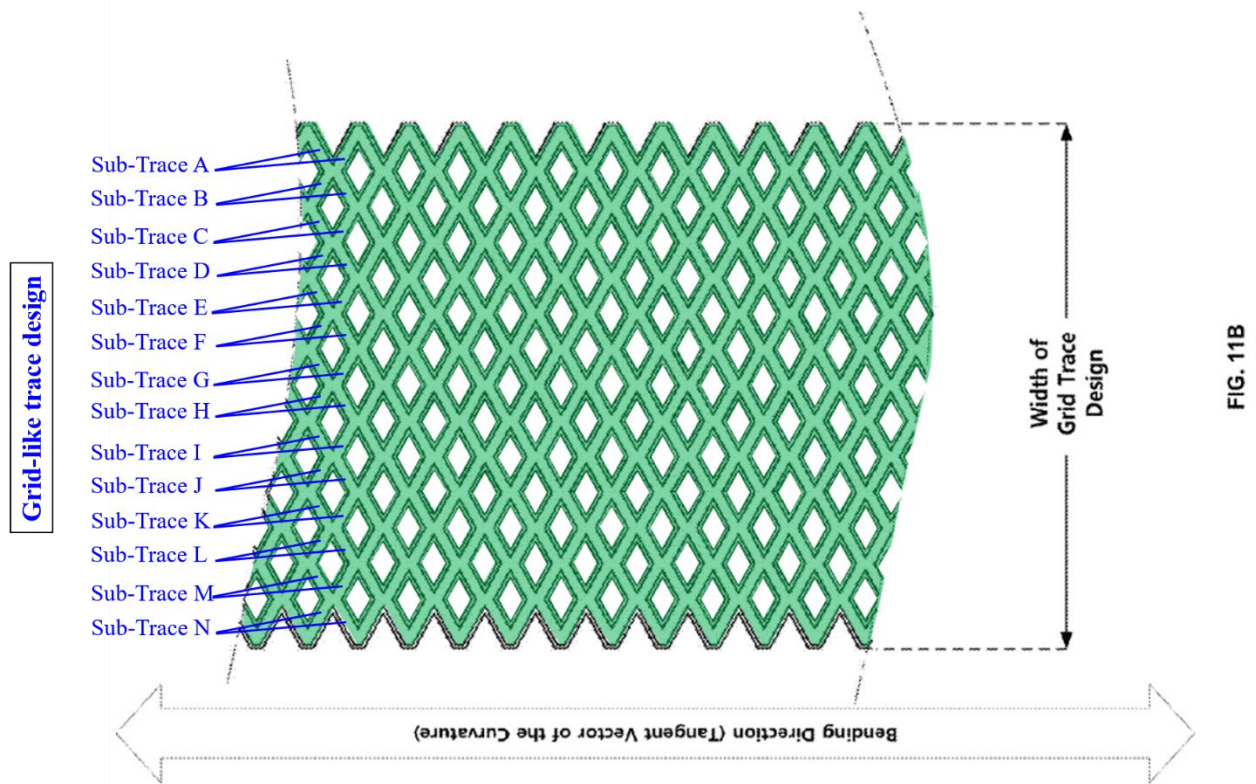
trace (i.e., VSS lines (blue)) and the second section of the first power trace (pink) through either the right or the left portion of the bending region (red) is 2. Here, the number of 2 shows the claimed “a plurality of second connecting sub-traces.”

135. As explained for Element 1[c], the VDD and/or VSS in the bend allowance section can have the strain-reducing trace design shown in annotated Figures 11A, 11B and 21.

136. Referring again to annotated Figure 16A above, in either the right or left portion of the bending allowance section, the first and second sections of the second power trace are connected by two second connecting sub-traces (green) each having the diamond trace design. Since one second connecting sub-trace possesses the two sub-traces as described in annotated Figure 11A, the first and second sections of the second power trace in either the right or left portion of the bending allowance section are connected by four sub-traces. Here, the number of 4 shows the claimed “a plurality of second connecting sub-traces.”



137. Alternatively, annotated Figure 11B below shows a grid-like trace design. The grid-like trace design below has 14 Sub-traces from Sub-Traces A to N counted in the same manner as shown in annotated Figure 11A. Consequently, the first and second sections of the second power trace in either the right or left portion of the bending allowance section are connected by 14 Sub-traces from Sub-Traces A to N. Here, the number of 14 shows the claimed “a plurality of second connecting sub-traces.”



138. Alternatively, annotated Figure 21 shows another grid-like trace design. The grid-like trace design below has 24 Sub-traces from Sub-Traces A to X counted in the same manner as shown in annotated Figure 11A. Consequently, the first and second sections of the second power trace in either the right or left portion of the bending allowance section are connected by 24 Sub-traces from Sub-Traces A to X. Here, the number of 24 shows the claimed “a plurality of second connecting sub-traces.”.

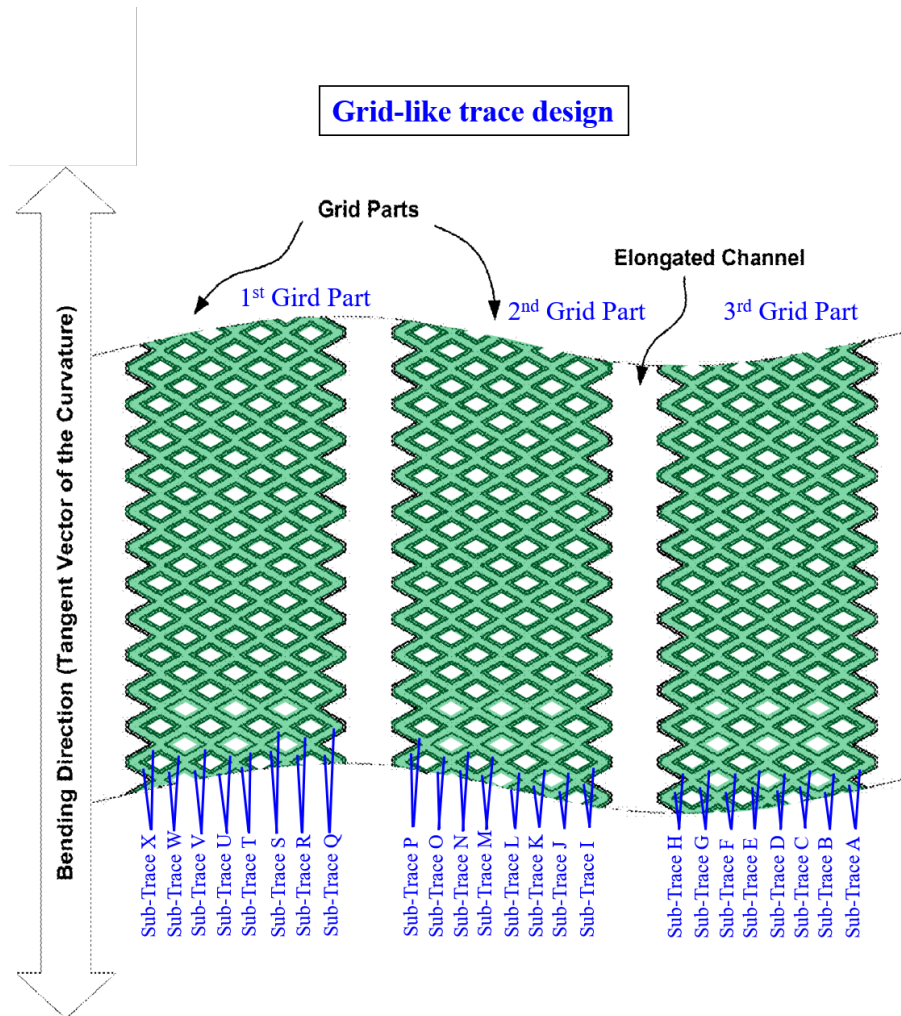


FIG. 21

139. Alternatively, as explained for Element 1[c], 1st Grid Part, 2nd Grid Part and 3rd Grid part shown in annotated Figure 21 which extend along the elongated channel can correspond the claimed second connecting sub-traces. This is because Kwon teaches that “the separated parts of the wire trace on one side of the elongated channel is connected to the part of the wire trace on the opposite side of the elongated channel, and thus both parts of the wire trace transmit the identical signal,” and “the connection between the divided parts of the wire trace may be

achieved at” “both ends of the wire trace by a conductive path,” and “the connection of the divided parts of the wire trace may be achieved” “outside the bend allowance section.” Ex-1005, 42:63-43:5. Consequently, the first and second sections of the second power trace in either the right or left portion of the bending allowance section are connected by three second connecting sub-trace which are the 1st to 3rd Grid parts. Here, the number of 3 shows the claimed “a plurality of second connecting sub-traces.”

3. **Claim 10: The display panel according to claim 1, wherein the fanout routing region further comprises a plurality of data traces, and wherein a material of the first connecting sub-traces and the second connecting sub-traces located within the bending region and a material of the plurality of data traces is selected from a group consisting of titanium-aluminum-titanium, molybdenum, copper, and silver nanowire.**

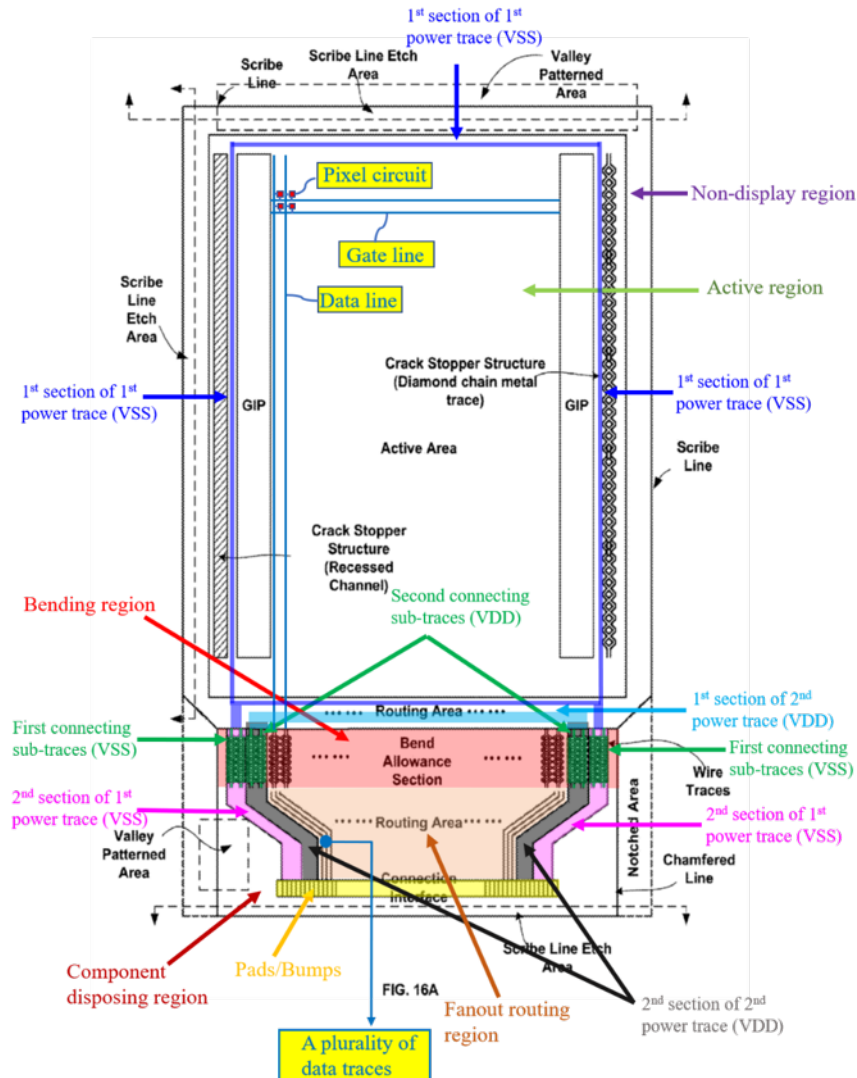
140. In my opinion, Kwon teaches Claim 10.

141. Although the recited “plurality of data traces” are admittedly prior art components (*see* Section V), Kwon also teaches that its fanout routing region further comprises a plurality of data traces.

142. As shown in annotated Figure 16A below and explained for Element 1[a], Kwon’s “Routing Area” (orange) corresponds to the recited “fanout routing region.” Ex-1005, Fig. 16A. Kwon clearly teaches routing fan-out using data lines and traces where signal or data lines are fanned out or gathered together to bridge

the spacing difference between the display pixel pitch and display driver IC chip pad pitch. Kwon teaches conductive lines including, for example, data lines that “communicate with one or more driving circuits,” which corresponds to the recited “plurality of data traces.” Specifically, Kwon teaches that “[e]ach pixel in the active area may be associated with a pixel circuit,” which, in turn, is “electrically connected to a gate line and a data line to communicate with one or more driving circuits, such as a gate driver¹³ and a data driver positioned in the inactive area of the flexible display 100.” Ex-1005, 5:33-40. Additionally, Kwon teaches that “a pad for receiving one or more signals may be provided on one end of the conductive lines” and “[t]he other end of the conductive line may be connected to the *data lines* of the pixels[.]” Ex-1005, 21:54-57. Accordingly, as shown in annotated Figure 16A below, the conductive lines (navy blue) connected between the pads (yellow) and the data lines are the plurality of data traces (navy blue). Ex-1005, Fig. 16A (modified to include pixel circuit, gate line, and data line as taught by Kwon).

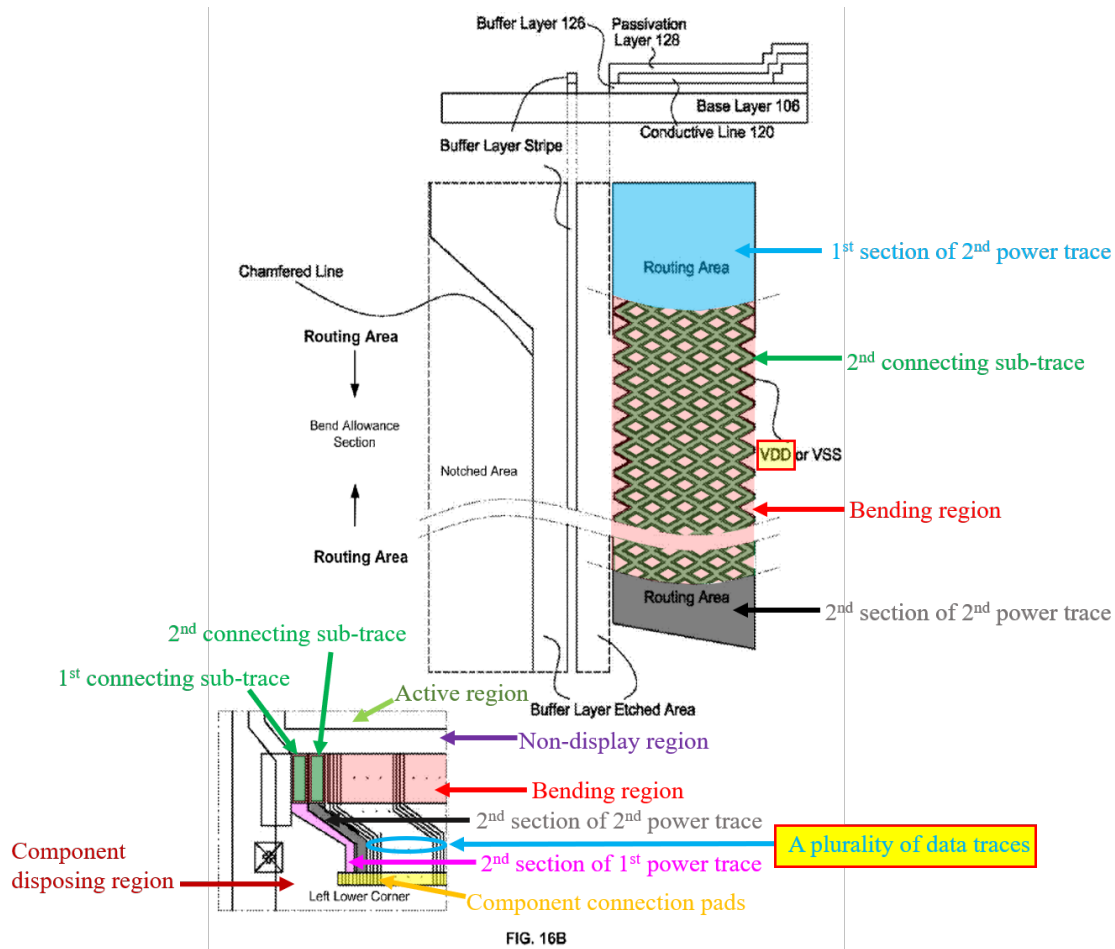
¹³ The gate driver here is a GIP (gate in panel). Ex-1005, 5:43-44.



143. Moreover, Kwon further teaches that the material of the first connecting sub-traces, the second connecting sub-traces, and the data traces may consist of titanium-aluminum-titanium, molybdenum, or copper. Specifically, Kwon explains that “at least some of the conductive lines 120 of the flexible display 100 may be formed with *two or more of layers selected from aluminum (Al), titanium (Ti), molybdenum (Mo), Copper (Cu)* layers.” Ex-1005, 20:39-42. Kwon further

teaches that “[e]xamples of such combination include *an aluminum layer sandwiched between titanium layers (Ti/Al/Ti)[.]*” Ex-1005, 20:43-44.

144. Further, annotated Figure 16B below shows the lower left corner of the flexible display, the conductive lines (light blue), which are the claimed data trace, are routed on the right side of the second section of the second power trace (grey) to the pads.



145. Kwon teaches that “the term conductive lines broadly refers to a trace of conductive path for transmitting any type of electrical signals (fn: this is a data

signal transmitted through the data trace), power and/or voltages (fn: this is a power voltage transmitted through VDD or VSS) from one point to another point in the flexible display 100.” Ex-1005, 19:52-55. This section means that the conductive lines can be data traces or power lines, such as VDD or VSS.

B. Ground 2: Claims 3, 11, and 16 are rendered obvious by the combination of Kwon and Kang’261

1. A POSITA would have been motivated to combine Kwon’s teachings with Kang’261’s teachings and would have had a reasonable expectation of success.

146. A POSITA would have been motivated to combine the teachings of Kwon and Kang’261 and would have had a reasonable expectation of success in doing so because both references are directed to flexible display devices that route power-supply conductive lines across a non-active, bendable region of the substrate in order to reduce the size of the non-active area while preserving the electrical and mechanical integrity of those power lines during bending. Ex-1005, Abstract, Figs. 1, 16A; Ex-1006, Abstract, Figs. 1, 5. For example, Kwon and Kang’261 teach flexible displays where there are well-established design principles in flexible OLED display engineering. Both patents are in the same field of flexible, bendable, or foldable OLED display panels. Both are aimed at the challenges of minimizing non-display margins by bending and folding edge substrates behind the active display panel as well as maintaining metal trace integrity i.e. avoiding cracking, fatigue, delamination from repetitive bending. Kwon teaches a bendable OLED display

panel with multi-layer metal wiring and Gate-In-Panel (GIP) line integration to reduce bezel width while Kang'261 teaches a wiring topology or architecture that improves trace integrity for the power lines also for foldable OLED display panels. And each reference is directed to similar methods of solving similar problems. First, they each focus on mitigating crack propagation over a bending region. Second, they each address potential issues that may arise when the bending regions and corresponding routing regions are notched, chamfered, or otherwise narrower than the active display region.

147. Specifically, Kwon is directed to a “Flexible Display Device With Gate-In-Panel Circuit,” and teaches VSS/VDD power lines and other conductive lines routed through a bend allowance section of the inactive area of the display panel. Ex-1005, 2:22-28. Kwon further teaches a strain-reducing trace design in which a conductive line, including specifically a “VSS line and a VDD line,” is divided into “at least two sub-traces” that “split away from each other and merge back at each joint,” forming a chain of diamond-shaped (or grid-like) links, in order to reduce crack initiation and propagation in the bend region while preserving the low electrical resistance required for power transmission. *See* Ex-1005, 25:48-50, 28:32-44. Moreover, Kwon teaches a “notch may be provided in the bend allowance section between the first area and the second area to reduce the size of bend allowance section” and “the notch provided in the bend allowance section would

also facilitate easier bending of the flexible base layer.” Ex-1005, 3:32-37. By removing this notch, the routing area after Kwon’s bend allowance section is narrower than the display area, causing the wires to be packed more tightly in the routing area. This narrowing constrains the degrees of freedom in placement and design for VDD and VSS routing within the non-display area. This may also cause an increase in resistance and may affect the uniformity of power distribution for the VDD and VSS lines in the non-display area.

148. Similarly, Kang’261 teaches a “Display Device” including plurality of power lines and power link lines disposed in the active and non-active areas of the display device, respectively. Further, as shown in Figure 5, Kang’261 also teaches a notched area on either side of the bend/routing area that serves to make the bended region narrower than the active display area. Ex-1006, Fig. 5. This causes the same issues noted above with respect to Kwon (increased resistance and potentially uneven power distribution). Kang’261 teaches to solve these similar problems by using multiple vertical subtraces, which are then connected to a horizontal line in the bent region. These multiple vertical subtraces are configured to transmit power voltage across a bending area via bending patterns connecting an upper power link line to a lower power link line using sub-traces divided across a right, middle, and left area. Ex-1006, 13:20-14:46, 15:18-20. Kang’261 teaches that its sub-traces “may employ repeated patterns having at least one of a diamond, rhombic, zigzag, or

circular shape” and that “[t]he bending patterns BP may employ a variety of shapes to reduce stress and cracks on the bending patterns BP.” Ex-1006, 7:17-21.

149. Accordingly, a POSITA attempting to address issues similar to those in Kwon would have looked to the solutions provided by Kang’261, which provides additional implementation details for the sub-trace geometry of power lines crossing Kwon’s bend area. Specifically, a POSITA would have been motivated to implement Kang’261 teachings into Kwon’s system because Kwon expressly directs a POSITA to apply Kwon’s sub-trace geometry to power lines that “cross over a bend allowance section” (Ex-1005, 28:38-41) and Kang’261 teaches additional examples of bending patterns employing “a variety of shapes” that may be used to reduce stress and cracks (Ex-1006, 7:19-21), which is a goal of Kwon’s system. *See, e.g.*, Ex-1005, 8:52-55 (discussing the need to “suppress generation of cracks” in the system), 23:11-12 (discussing patterning the conductive lines “to suppress crack propagation in the wire traces”). Further, to solve problems related to increased resistance and potentially uneven power distribution, Kang’261 employs an upper power link line, extending horizontally, that distributes power within itself and supplies it to multiple points on a lower power link line, also extending horizontally, via a bending pattern of at least 3 vertical traces. As a result, supplying power at multiple points along the lower power link line resolves resistance issues and ensures a uniform power supply to the active region. Indeed, Kwon acknowledges that “[b]end stress management of

the insulation layers near the conductive line is just as important as the managing the strain of the conductive line itself.” Ex-1005, 24:21-23. A POSITA would have understood that implementing Kang’261’s bend-durable sub-trace geometries with Kwon’s diamond-chain/grid design would have been a suitable design choice to solve these similar problems in both references.

150. Additional motivations to combine are as follows. Kwon teaches “for example, cellular telephones and portable computers include displays for presenting information to a user” and “an array of organic-light emitting diode (OLED) elements is disposed in the first area of the flexible base layer.” Ex-1005, 1:10-12, Cl. 1. Kang’261 teaches that “display devices are being utilized in a variety of applications, such as in monitors, TVs, smartphones, and watches” and “examples of display devices include organic light emitting diode (OLED) displays.” Ex-1006, 10:42-44. Both Kwon and Kang’261 thus relate to the OLED technology for the smartphone sized panels.

151. Further, Kwon teaches that “a high ratio of the active area size compared to that of inactive area, which is sometimes referred to as the screen to bezel ratio, is one of the most desired feature.” Ex-1005, 1:32-35. In Kwon, to maximize the screen to bezel ratio, the inactive area was bent to the rear of the active area. Particularly, Kwon discloses that “bending the inactive area allows to minimize or to eliminate the inactive area to be seen from the front side of the assembled

flexible display 100” (Ex-1005, 6:65-67) and teaches that “the inactive area with the connection interface can be bent away from the plane of the adjacent portion of the flexible display so that the printed circuit (e.g., COF, PCB and the like) is positioned at the rear side of the flexible display 100.” Ex-1005, 50-54. In Kwon, to prevent cracks caused by bending, the wiring passing through the bending area is designed with a bend stress-reducing structure. Particularly, Kwon teaches that “[s]ince the bend allowance section is most heavily affected by the bend stress, various bend stress-reducing features are applied to the components on the base layer 106 of the bend allowance section,” “a wire trace having the diamond trace design is bent in the bending direction,” and “a VSS line and a VDD line in the flexible display 100 may have the grid-like trace design, especially if such lines are arranged to cross over a bend allowance section.” Ex-1005, 14:11-14, 27:38-39, 28:38-41.

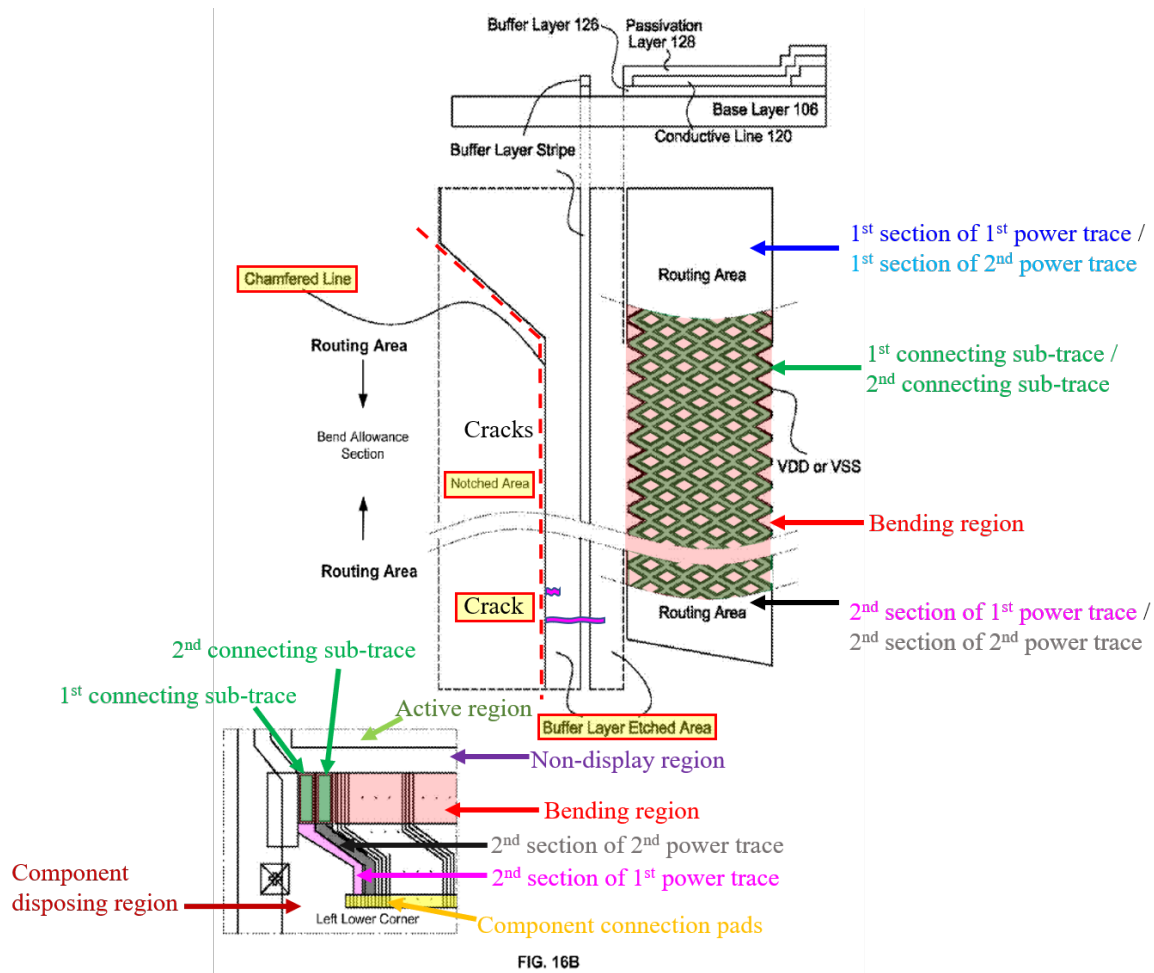
152. Like Kwon, Kang’261 teaches that “studies on creating a display device having a wide display area and a reduced volume and weight are being conducted” and “the study of reducing bezel sizes in display devices is one of them.” Ex-1006, 10:44-47. Like Kwon, in Kang’261, to reduce bezel size, the inactive area was bent to the rear of the active area. Particularly, Kang’261 teaches that “the bending area BA is bent in a bending direction in the final product (e.g., to allow circuitry to be placed behind and overlapping with the display panel).” Ex-1006, 7:11-13. Like Kwon, in Kang’261, to prevent cracks caused by bending, the wiring passing

through the bending area is designed with a bend stress-reducing structure. Particularly, Kang'261 teaches that "the bending patterns BP of the power link line may be formed into a pattern of a specific shape to minimize stress and cracks on the plurality of link lines in the bending area BA" and "for example, the bending patterns BP may employ repeated patterns having at least one of a diamond, rhombic, zigzag, or circular shape, but is not limited thereto." Ex-1006, 7:14-21.

153. Both Kwon and Kang'261 focus on specific areas of OLED fields. They share the common goal of achieving a narrow bezel through panel bending. To accomplish this, both methods involve bending the panel's inactive area to be positioned beneath the active area. Furthermore, they both address the issue of cracking during the bending process by designing the wires passing through the bending region with a bend stress-reducing structure. Thus, a POSITA would have found it readily apparent to combine Kwon and Kang'261 within the specific domain of panel bending for smartphone sized OLED panels.

154. Annotated Figure 16B below of Kwon shows a lower left corner of the flexible display 100. Referring to Figure 16B below of Kwon, as mentioned above, the portion located outside the chamfered line is removed by the chamfering process and is referred to as the notched area. The notch provided in the bend allowance section reduces the size of bend allowance section to facilitate easier bending of the flexible base layer. Kwon teaches that "in order to reduce crack initiation and

propagation from the inorganic layers near the chamfered line, the insulation layer is etched in the area between the wire trace (e.g., VSS/VDD line) to the chamfered line,” “the buffer layer 126 disposed on the base layer 106 in the area between the chamfered line and the conductive line 120 in the bend allowance section, which is closest to the chamfering line (e.g., VSS/VDD line) can be removed” and “crack initiation and propagation from the chamfered line can be hindered by the buffer layer etched area.” Ex-1005, 37:18-31.



155. Referring again to annotated Figure 16B above, cracks¹⁴ (pink) originating from the cutting process at the chamfered line have their propagation halted by the buffer layer etched area. The buffer layer etched area extends from the chamfered line to the non-display region with a predetermined width. Given the potential for crack-induced damage over this etched area, VDD and VSS lines must be routed inward of the buffer layer etched area. The notched area and the buffer layer etched area restrict the regions where VDD and VSS lines can be placed within the non-display area. These constraints reduce the degree of freedom in design for VDD and VSS routing within the non-display area. Consequently, this may cause an increase in resistance (or IR drop¹⁵) for VDD and VSS lines in the non-display area. This can also prevent power from being uniformly distributed from the non-display region to the active region in a horizontal direction¹⁶.

156. Kang'261 teaches that “the inventors of the present disclosure reduced the size of the non-active area by removing some portions from the non-active area” and “the inventors of the present disclosure also recognized that it is necessary to realign various lines and components disposed in the non-active area in order to

¹⁴ The cracks are added to annotated Figure 16A for illustrative purposes, in accordance with Kwon's description.

¹⁵ IR drop stands for voltage drop caused by electrical resistance.

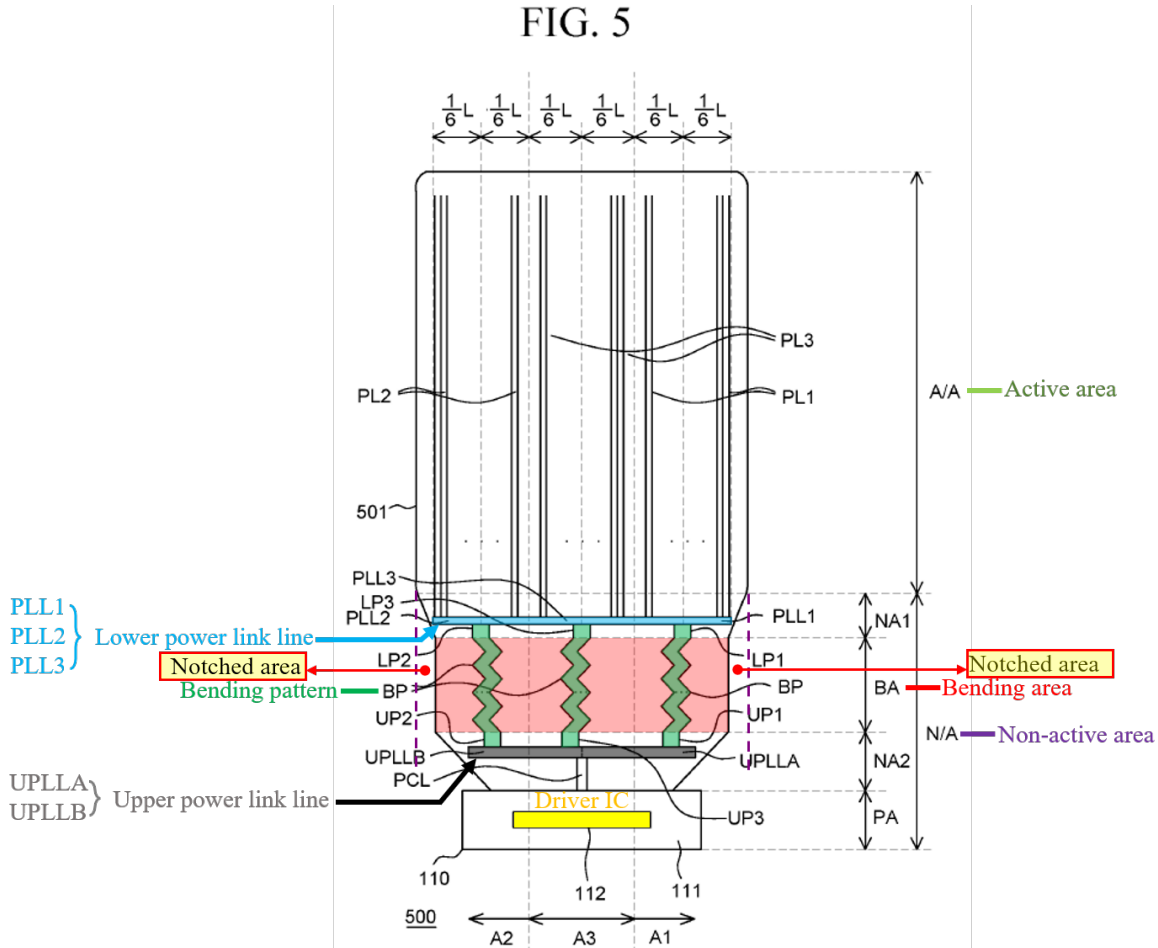
¹⁶ The horizontal direction here is the same as the longitudinal direction of Kang'261.

maximize the removable portion therein.” Ex-1006, 1:41-54. Kang’261 teaches that “when power voltage is supplied to a plurality of pixels from a driver IC, power voltage drop may occur due to resistance in the power lines, causing non-uniformity in brightness among the plurality of pixels.” Ex-1006, 1:54-58. Kang’261 teaches that “an object to be achieved by the present disclosure is a reduction in power voltage drop by adding points from which power voltage can be supplied, in order to improve brightness uniformity in a display device.” Ex-1006, 2:1-6.

157. Referring to annotated Figure 5 below, similar to Kwon, the panel of Kang’261 also features notched areas formed on both sides of the non-active area (purple) where the bending area (red) is located. While these notched areas reduce the size of the bending area (red) to facilitate easier bending, they simultaneously can act as a limiting factor in power distribution design that can cause the power voltage drop. To solve the power voltage drop issue, Kang’261 employs the upper power link line (grey). The upper power link line (grey), extending horizontally, distributes power within itself and supplies it to multiple points on the lower power link line (blue) via a bending pattern (green)¹⁷. As a result, supplying power at multiple points along the lower power link line (blue) resolves high resistance issues (IR drop) and ensures a uniform power supply to the active region (light green). As

¹⁷ The bending pattern (green) may extend perpendicular to the bending area (red) to minimize the impact of bending stress.

shown in Figure 5 below, the number of multiple points along the lower power link line (blue) can be three.



158. As explained above, Kang’261 proposes a method to resolve issues such as voltage drop caused by removing the inactive region in Kwon. Therefore, it would have been obvious to a POSITA to combine Kwon and Kang’261. Kang’261 teaches that “the power voltage output point of the driver IC 112 of the display device 600 may be changed in various ways depending on the model and design of the driver IC 112,” and “when the power voltage output point of the driver IC 112 is

changed, the layout or disposition of pad connecting lines may be changed accordingly.” Ex-1006, 17:49-54. That is, referring again to Figure 5 above, regarding the relationship between the upper power link line (grey) and the driver IC (yellow), the upper power link line’s (grey) horizontal extension allows for easy connection even if the power input point varies depending on the driver IC model or design. Therefore, regardless of the driver IC model or design, the degree of freedom in designing the power wiring in the non-active area can be increased. Kang’261 teaches that “[d]isplay devices are being utilized in a variety of applications, such as in monitors, TVs, smartphones, and watches” (Ex-1006, 10:42-44) and Kwon teaches that “some of the components, such as data drive-IC, may be mounted on a separate printed circuit and coupled to a connection interface (Pads/Bumps, Pins) disposed in the inactive area using a printed circuit such as flexible printed circuit board (PCB), chip-on-film (COF), tape-carrier-package (TCP) or any other suitable technologies.” Ex-1005, 5:44-50.

159. Kwon cites various OLED products as examples and explains that components such as data drive ICs can be attached to the connection interface in diverse ways. This suggests that the model and design of the Driver IC can vary significantly. Therefore, the need to secure design freedom for power wiring, regardless of the Driver IC model or design, could serve as another reason indicating that it would be obvious for a POSITA to combine Kwon and Kang’261.

160. A POSITA would have had a reasonable expectation of success in combining the teachings of Kwon and Kang’261. Both references address the identical structural context—power-line routing across the bend region of a flexible display to minimize the inactive area—rendering their teachings directly interchangeable and combinable. Ex-1005, Abstract, Figs. 1, 16A; Ex-1006, Abstract, Figs. 1, 5. A POSITA would thus have understood that these references disclose interrelated teachings based on well-understood technologies that would have been amenable to various well-understood and predictable combinations.

2. Dependent Claim 3: The display panel according to claim 1, wherein the first section of the second power trace is separately connected to the second section of the second power trace disposed within the component disposing region by three sets of the second connecting sub-traces passing through a left section, a middle section, and a right section of the bending region.

161. In my opinion, Kwon in view of Kang’261 (“Kwon-Kang’261”) teaches Claim 3.

162. Kwon teaches that the first section of the second power trace is separately connected to the second section of the second power trace disposed within the component disposing region for the reasons described for Element 1[d].¹⁸ While

¹⁸ Dependent Claim 3 has a “set” limitation, which was already explained in detail in the description of Element 1[c]. Kwon satisfies the “a set of” limitation by using a wire trace having the diamond trace design or the grid-like trace design arranged to cross over a bend allowance section.

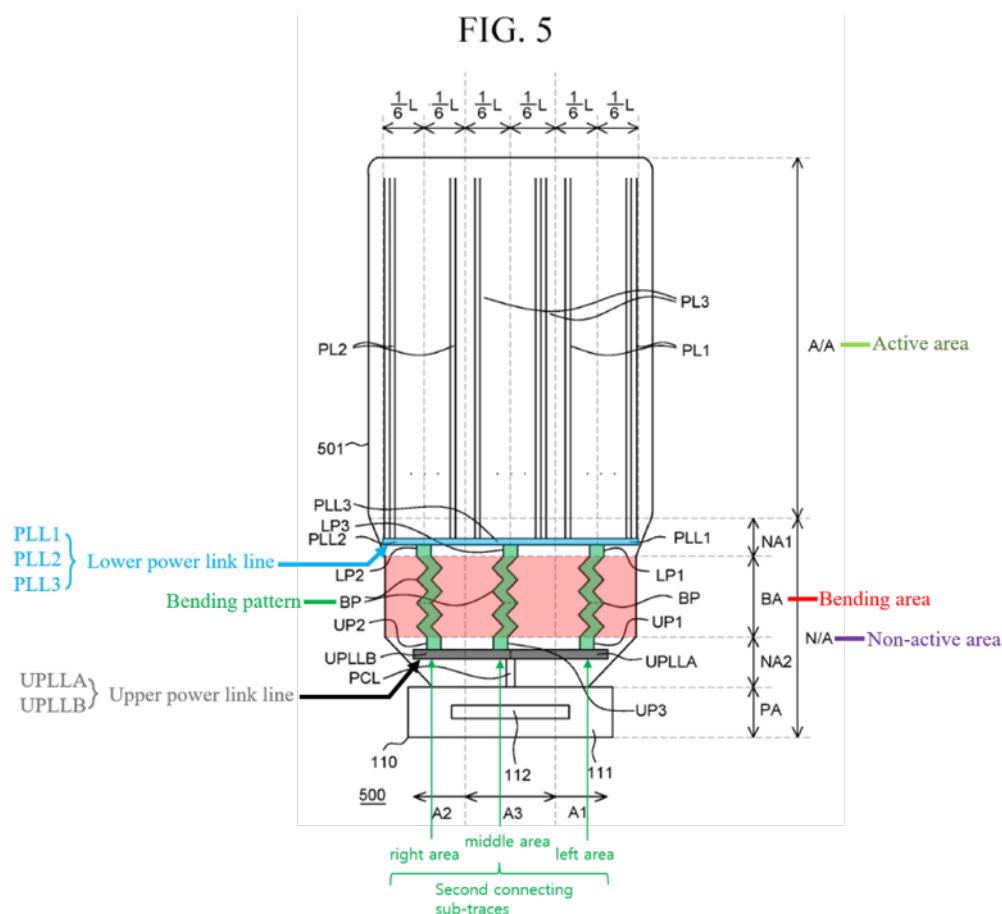
Kwon teaches that the two components are connected by at least two sets of the second connecting sub-traces passing through two sections of the bending region (*see* Element 1[d]), it would have been obvious to implement Kwon's system to include three sets of the second connecting sub-traces passing through a left section, a middle section, and a right section of the bending region. For example, a POSITA dividing a bend region into three logical sections would have been able to implement three sets of second connecting sub-traces passing the 3 sections using standard design techniques. This is taught by Kang'261.

163. As shown in the annotated Figure 5 below, Kang'261 teaches a "first area A1, second area A2, and third area A3 . . . defined by dividing the length of the substrate 501 along a longitudinal direction" with A1 corresponding to the "the left area of the substrate 501," A2 corresponding to "the right area," and A3 corresponding to the "the central area." Ex-1006, 13:20-33. Kang'261 further teaches that "the power link lines and power lines corresponding to the respective areas are disposed to transmit power voltage to pixels in their respective areas." Ex-1006, 15:18-20. Kang'261 teaches that the power link lines are further divided by "upper power link lines" UPLLs and "lower power link lines," PLLs, which correspond to the two sections of the recited second power trace. Ex-1006, 13:42-14:46. Specifically, Kang'261 teaches that "[t]he upper power link line includes a first portion UPLLA, extending from the center of the third area A3 through the first

area A1, and a second portion UPLLB, extending from the center of the third area A3 through the second area A2.” Ex-1006, 13:34-41. Kang’261 teaches that “in the first non-active area NA1, the first lower power link line PLL1 is disposed in the first area A1, the second lower power link line PLL2 is disposed in the second area A2, and the third lower power link line PLL3 is disposed in the third area A3[,]” “the first lower power link line PLL1, the second lower power link line PLL2, and the third lower power link line PLL3 may extend throughout the length of the first area A1, second area A2, and third area A3, respectively” and “PLL1, PLL2, and PLL3 can form a single power line[.]” Ex-1005, 14:29-46.

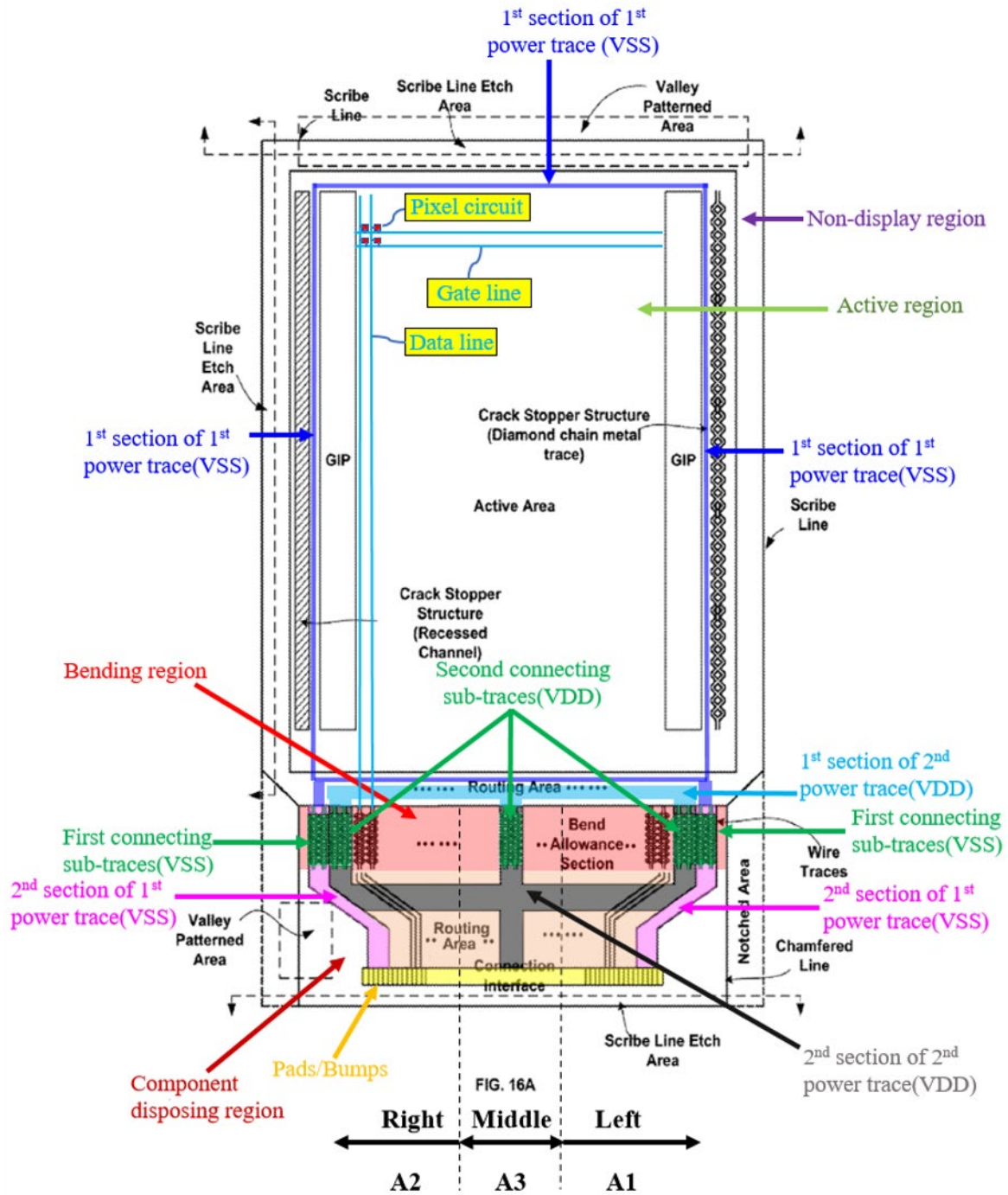
164. Kang’261 further teaches that its UPLL and PLL sections are connected to each other by a “plurality of bending patterns BP in the bending area BA,” wherein “some are disposed in the first area A1, some are disposed in the second area A2, and others are disposed in the third area A3.” Ex-1006, 14:1-4. Specifically, Kang’261 teaches that “the plurality of bending patterns may extend to the first lower connecting line from an end of the first portion of the upper power link line” and the “other bending patterns among the plurality of bending patterns may extend to the second lower connecting line from an end of the second portion of the upper power link line.” Ex-1006, 22:9-14. For example, “[t]he lower power link line transmits power voltage received through the upper power link line and the plurality of bending patterns BP to each of the first power lines PL1 and second power lines

PL2[.]” Ex-1006, 7:22-25. Kang’261’s bending patterns BP correspond to the recited “second connecting sub-traces.” As shown in Figure 5, Kang’261 teaches that three sets of bending patterns BP (green) pass through a left section (A2), a middle section (A3), and a right section (A1) of the bending region (red). Ex-1006, Fig. 5.



165. A POSITA would have been motivated to combine Kwon with Kang'261 and had a reasonable expectation in doing so for the reasons described in Section VIII.B.1. Specifically, Kwon's subtraces (green) would have been used to connect an upper portion of the VDD line (light blue), extending through the middle

of the bend allowance section, to a lower portion of the VDD line (grey) that connects to the pads on Kwon's connection interface, as in the modified Figure below (middle traces added). Moreover, like Kwon, Kang'261 teaches that "the bending patterns BP of the power link line may be formed into a pattern of a specific shape to minimize stress and cracks on the plurality of link lines in the bending area BA" and "for example, the bending patterns BP may employ repeated patterns having at least one of a diamond, rhombic, zigzag, or circular shape, but is not limited thereto." Ex-1006, 7:17-21. Therefore, it would have been obvious to a POSITA that the portion of the bending patterns BP in Kang'261 passing through the bending area may be configured as a set of sub-traces, as taught in Kwon.



3. Independent Claim 11

a. 11[pre]: A display panel comprising:

166. In my opinion, Kwon-Kang'261 teaches Element 11[pre] for the reasons described in Section VIII.A.1.a.

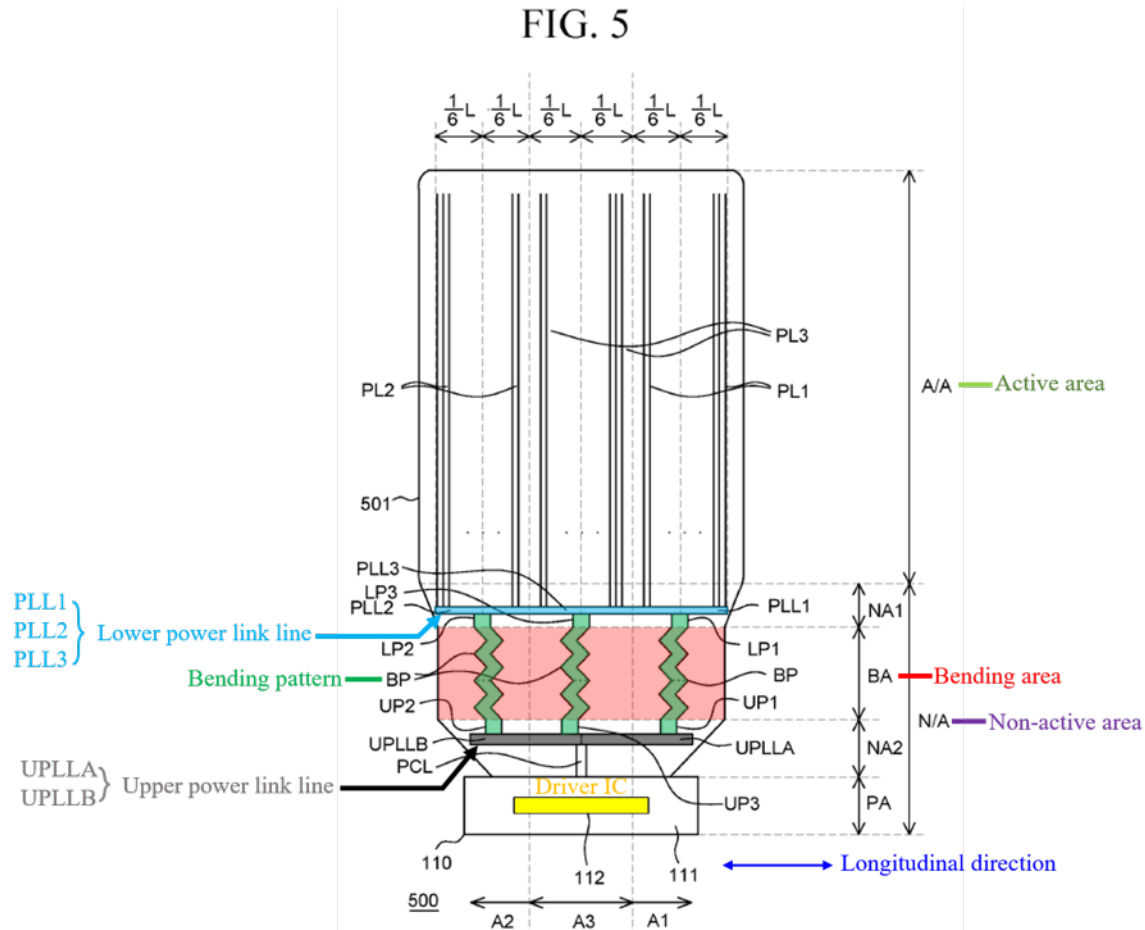
b. 11[a]: an active region and a non-display region, the non-display region disposed around the active region and extending to form a bending region and a component disposing region, wherein the bending region defines a left section, a middle section, and a right section, the component disposing region having a plurality of component connecting pads; and

167. In my opinion, Kwon-Kang'261 teaches Element 11[a].

168. Kwon teaches an active region and a non-display region, the non-display region disposed around the active region and extending to form a bending region and a component disposing region, the component disposing region having a plurality of component connecting pads for the reasons described in Section VIII.A.1.b. Kwon further teaches a left and right section, as described above in connection with Claim 7.

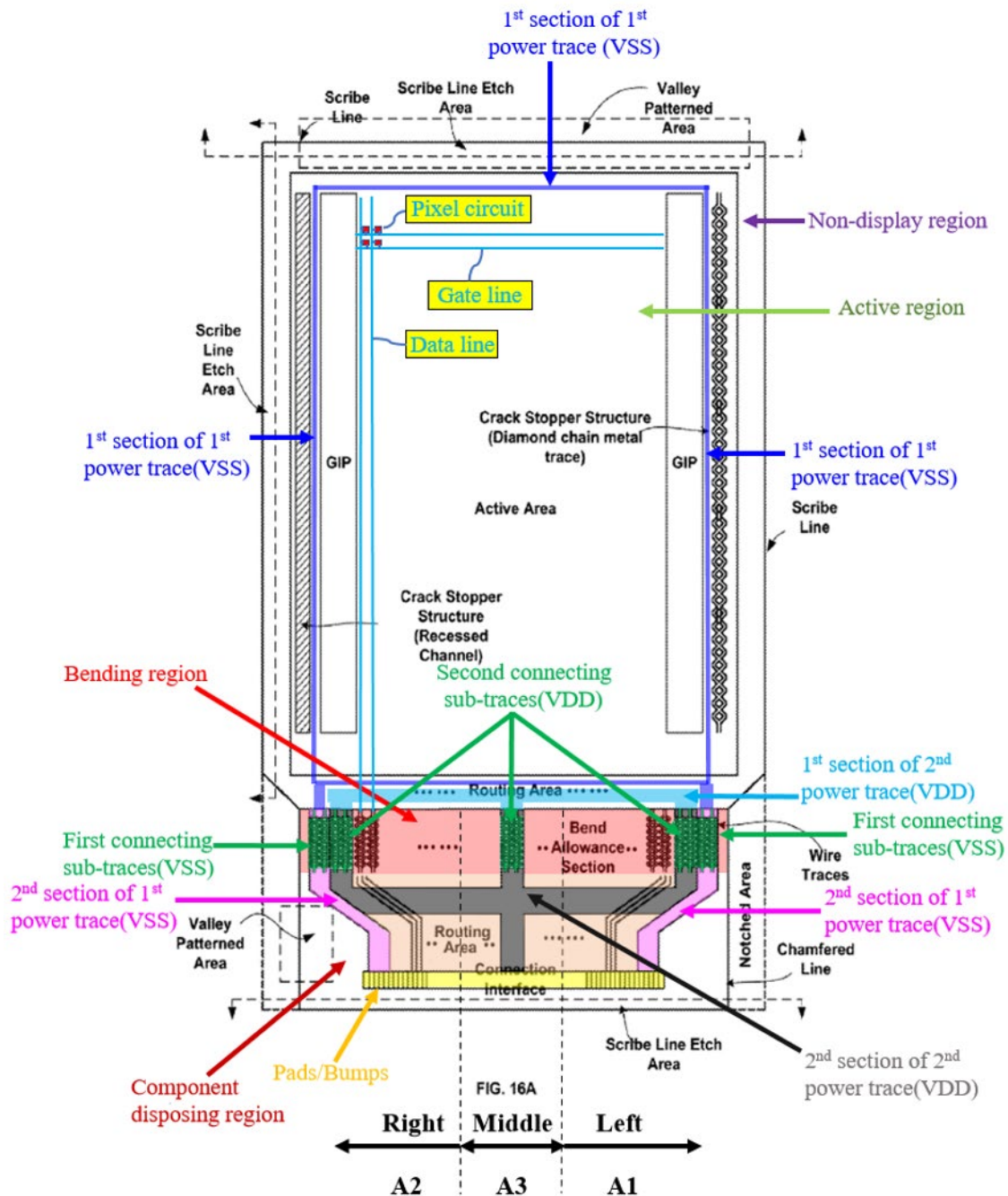
169. Kang'261 further teaches that the bending region defines a left section, a middle section, and a right section. Specifically, as shown in annotated Figure 5 below, Kang'261 teaches that “substrate 501 of the display device 500 includes a first area A1, second area A2, and third area A3[,]” which “may be defined by dividing the length of the substrate 501 along a longitudinal direction.” Ex-1006,

13:20-24, Fig. 5. Kang'261's first area A1, second area A2, and third area A3 correspond to the recited left section, a middle section, and a right section of the bending region, as explained above in connection with Claim 3.



170. A POSITA would have been motivated to implement Kang'261's left-right-middle teaching in Kwon. As previously explained, Kwon specifically teaches left and right edges of the bend allowance area, as discussed above in connection with Claim 7. Kwon further teaches that data traces pass over the bend allowance section internal to the VDD and VSS traces on the left and right edges, as explained in connection with Claim 10. A POSITA implementing Kwon and Kang'261

together would have identified the portions of Kwon's bend allowance section A1, A2, and A3, corresponding to a left, right, and middle sections, to more efficiently organize and identify the particular subraces. Doing so would be nothing more than routine and ordinary naming, and would not otherwise affect the structure and operation of Kwon's device. This is shown in the figure below combining Kwon's Figure 16A and Kang'261's Figure 5.

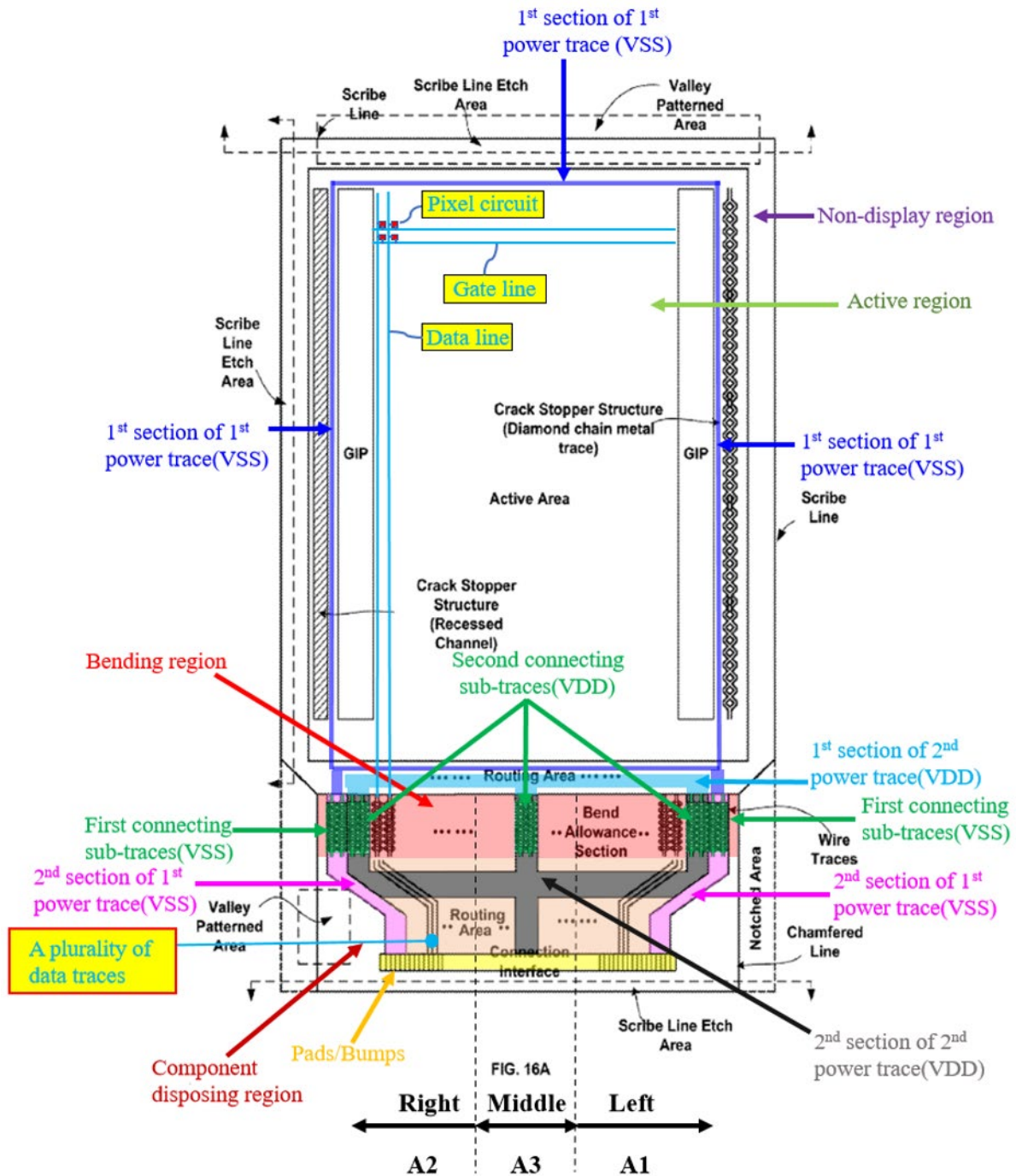


- c. 11[b]: a plurality of data traces passing through the bending region and connected with the active region and the plurality of component connecting pads;

171. In my opinion, Kwon-Kang'261 teaches Element 11[b].

172. Kwon teaches a plurality of data traces passing through the bending region for the reasons described in Section VIII.A.3. *See, e.g.*, Ex-1005, 5:33-50, 21:54-57, 46:29-32. Kwon's conductive lines including, for example, data lines "to communicate with one or more driving circuits" correspond to the recited "plurality of data traces" passing through the bending region.

173. Moreover, as explained in the prior section, the data traces pass through the middle section of the bend allowance region, corresponding to Kang'261's A3. Thus, both Kwon and Kang'261 teach a plurality of data traces that pass through a bending region and that are connected with an active region and component connecting pads.



- d. 11[c]: wherein a first section of a power trace is disposed adjacent to the active region, the first section of the power trace is connected to a second section of the power trace disposed within the component disposing region by three sets of connecting sub-traces passing through the left section, the middle section and the right section, and the second section of the power trace is connected to the plurality of component connecting pads.**

174. In my opinion, Kwon-Kang'261 teaches Element 11[c].

175. Kwon teaches that a first section of a power trace is disposed adjacent to the active region, the first section of the power trace is connected to a second section of the power trace disposed within the component disposing region, and the second section of the power trace is connected to the plurality of component connecting pads for the reasons described in Section VIII.A.1.d.

176. Kang'261 teaches that the first section of the power trace is connected to a second section of the power trace disposed by three sets of connecting sub-traces passing through the left section, the middle section and the right section for the reasons described in Section VIII.B.2.

4. Independent Claim 16

- a. 16[pre]: A display panel comprising:**

177. In my opinion, Kwon-Kang'261 teaches Element 16[pre] for the reasons described in Section VIII.A.1.a.

- b. 16[a]: an active region and a non-display region, the non-display region disposed around the active region and extending to form a bending region and a component disposing region;**

178. In my opinion, Kwon-Kang'261 teaches Element 16[a] for the reasons described in Section VIII.A.1.b.

- c. 16[b]: wherein a first section of a power trace is disposed adjacent to the active region, the first section of the power trace is separately connected to a second section of the power trace disposed within the component disposing region by at least one set of connecting sub-traces passing through the bending region,**

179. In my opinion, Kwon-Kang'261 teaches Element 16[b] for the reasons described in Section VIII.A.1.c (first section of a power trace is disposed within the non-display region around (and adjacent to) the active region) and VIII.A.2 (first section of the power trace is separately connected to a second section of the power trace disposed within the component disposing region by at least one set of connecting sub-traces passing through the bending region).

- d. 16[c]: wherein the first section of the power trace is separately connected to the second section of the power trace disposed within the component disposing region by three sets of connecting sub-traces passing through a left section, a middle section and a right section of the bending region.**

180. In my opinion, Kwon-Kang'261 teaches Element 16[c].

181. Kwon teaches that the first section of the power trace is separately connected to the second section of the power trace disposed within the component disposing region for the reasons described in the previous section.

182. Kang'261 teaches that the first section of the power trace is separately connected to the second section of the power trace by three sets of connecting sub-traces passing through a left section, a middle section and a right section of the bending region for the reasons described in in Section VIII.B.2.

C. Ground 3: Claims 2, 4-6, 8-9, 12-15, and 18-19 are rendered obvious by the combination of Kwon, Kang'261, and Ka

1. A POSITA would have been motivated to combine Kwon's teachings with Kang'261's teachings and Ka's teachings and would have had a reasonable expectation of success.

183. A POSITA would have been motivated to combine the teachings of Kwon, Kang'261, and Ka and had a reasonable expectation of success in doing so because all three references relate to flexible, foldable display devices including bending region and sub-traces to minimize the bottom border using similar components. Ex-1005, Abstract, Figs. 1, 16A; Ex-1006, Abstract, Figs. 1, 5; Ex-1007 ¶¶4-5, Fig. 1. *See also* Section VIII.B.1.

184. As explained in Section VIII.B.1, Kwon and Kang'261 would have been combined because they each include similar teachings and address similar problems related to cracking in a bend area, and voltage and power distribution issues for wires passing through a bending area. Moreover, Kwon and Kang'261

each include some teachings relating the design and width of its various traces, but leaves some of those routine implementation details to a POSITA.

185. A POSITA seeking such implementation details relating to the width of traces would have turned to a reference such as Ka, which teaches substantially the same architecture of wires crossing a bending region.

186. Kwon and Ka both address the complete system-level architecture and micro-structural trace wiring that a POSITA would have used for standard design criteria (without any significant research or experimentation) in the field of flexible and foldable displays. A POSITA would have also understood that both Kwon and Ka teach the use and design of a bendable and flexible display that incorporates a narrow bezel architecture where the power traces and sub-traces are designed to cope with repetitive movement or bending

187. For example, Ka teaches a display device in which a plurality of driving voltage transmission lines are connected by sub-trace driving voltage connection lines. Ka further teaches specific, quantified width relationships among its driving voltage transmission lines and driving voltage connection lines to solve the same problems as those discussed by Kwon. Ex-1007 ¶74. In particular, Ka teaches that the sub-traces may have a width of about 3 micrometers while the power traces can “each have a width of about 50 to about 200 micrometers[.]” Ex-1007 ¶74. Ka further teaches that transmission-line / trace-section widths are deliberately set wider

than the connecting sub-trace or connection-line widths that cross the bend region because “[w]hen the length or width of the wires is increased or decreased, current density and voltage drop may also increase or decrease, causing deterioration in luminance uniformity of the image displayed in the display area.” Ex-1007 ¶4. Ka also notes that “in wire design, there is a limit to how much a line width of the driving voltage supply lines 10a and 10b may be increased” and provides solutions accordingly. Ex-1007 ¶65.

188. A POSITA would have been motivated to implement Ka’s teachings with the Kwon-Kang’261 combination because, for example, one of Kwon’s goals is to “achieve more stable level of luminance” in the display. Ex-1005, 11:38-41. Ka further addresses similar problems to those in both Kwon and Kang’261. *See, e.g.*, Section VIII.B.1; Ex-1005, 8:52-55, 23:8-12, 24:21-23, 26:8-11, 27:11-13; Ex-1006, 7:19-21.

189. Additional motivations to combine are as follows. As explained in the “motivation to combine” section of Kwon and Kang’261, Kwon and Kang’261 relate to the OLED technology for the smartphone sized panels. Ka teaches that “the width of a bezel that covers the peripheral area PA in the display device, such as a smart phone, can be reduced” and “[t]he light emitting element LD, which may be an organic light emitting diode OLED.” Ex-1007 ¶¶69, 102. Therefore, Kwon, Kang’261, and Ka relate to the OLED technology for the smartphone sized panels.

190. As also explained in the “motivation to combine” section of Kwon and Kang’261, Kwon and Kang’261 have a goal of achieving a narrow bezel through panel bending. To accomplish this, Kwon teaches a method involving bending the panel’s inactive area so that it is positioned beneath the active area. Furthermore, Kwon addresses the issue of cracking during the bending process by designing the wires passing through the bending region with a structure that reduces bend stress. Like Kwon and Kang’261, Ka teaches “when the display panel 300 is bent, the width of the peripheral area PA when being viewed from the front (e.g., the top plan view) can be reduced so that the width of a bezel that covers the peripheral area PA in the display device, such as a smart phone, can be reduced.” Ex-1007 ¶69. Like Kwon and Kang’261, Ka teaches that “a layer made of an inorganic material is susceptible to cracks when being bent, and wires may be damaged due to the cracks” and “[b]ecause of their material, the second portion 17b of the data connection lines 17 in the bending area BA and the driving voltage connection line 15 have low stress caused by strain such that the risk of a short-circuit or degradation due to bending can be reduced.” Ex-1007 ¶¶79, 109. Further, referring to annotated Figure 3 of Ka below, the driving voltage connection lines (green) are uniformly spaced part from each other, so they are arranged to be less affected by stress caused by bending in the bending area (red).

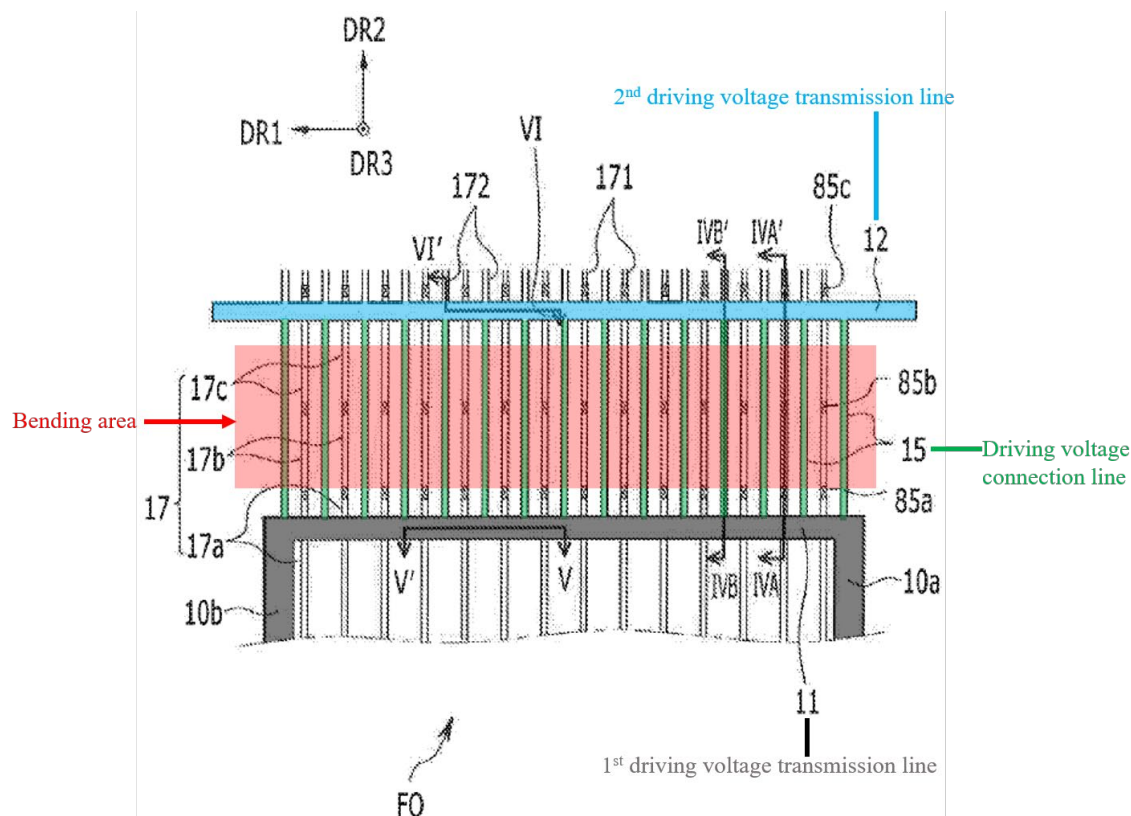


FIG. 3

191. Kwon, Kang'261, and Ka share the common goal of achieving a narrow bezel through panel bending. To accomplish this, both Kwon and Ka's methods, for example involve bending the panel's inactive area to be positioned beneath the active area. Furthermore, they each address the issue of cracking during the bending process by modifying the wires passing through the bending region. Thus, a POSITA would have found it readily apparent to combine Kwon, Kang'261, and Ka within the specific domain of panel bending for smartphone sized OLED panels.

192. Further, as detailed in the description of Claim 2 below, Kwon's panel may have an IR drop issue. Particularly, in the non-display region on Kwon's panel,

the notched area and the buffer layer etched area (designed to stop cracks from the chamfered line) restrict where VDD and VSS power lines can be routed. These constraints force the lines inward, reducing design flexibility. Consequently, this layout can lead to increased resistance (IR drop) and hinder the uniform horizontal distribution of power from the non-display region to the active region. Ka teaches that “in wire design, there is a limit to how much a line width of the driving voltage supply lines 10a and 10b may be increased.” Ex-1007 ¶65. That is, Ka points out that there is a limit to widening a line width of the driving voltage supply lines 10a and 10b which correspond to the second section of the second power trace in Kwon. Ka teaches that “the plurality of driving voltage connection lines 15 connects to the first driving voltage transmission line 11 and the second driving voltage transmission lines 12 at many points.” Ex-1007 ¶65. That is, to address the IR drop issue that may occur in a panel similar to Kwon’s, Ka proposes adopting a horizontally extending “first driving voltage transmission line 11” and configuring the plurality of driving voltage connection lines to be connected at multiple points between the first driving voltage transmission line 11 and the second driving voltage transmission line 11.

193. In the Kwon-Kang’261-Ka combination, a conductive line extending horizontally between the bending area and the driver IC (referred to as the “first driving voltage transmission line 11” in Ka) is positioned. From this horizontally extending conductive line, power is supplied to the active area at many points

(described as “at multiple points” in Ka). Thus, a POSITA would have had a reasonable expectation of success in combining the teachings of Kwon, Kang’261, and Ka. All three references relate to flexible, foldable display devices including bending region and sub-traces to minimize the bottom border using similar components, rendering their teachings interchangeable and combinable. Ex-1005, Abstract, Figs. 1, 16A; Ex-1007 ¶¶4–5, Fig. 1. A POSITA would thus have understood that these references disclose interrelated teachings based on well-understood technologies that would have been amenable to various well-understood and predictable combinations. A POSITA would also have understood that the combination of Kwon-Kang’261 with Ka would have allowed the design of Kwon’s bendable, flexible display to have a narrow bezel layout with high integrity split power sub-trace architectures that can be folded while Ka and Kang’261 creates an architecture of power and data routing with sub-trace dimensions.

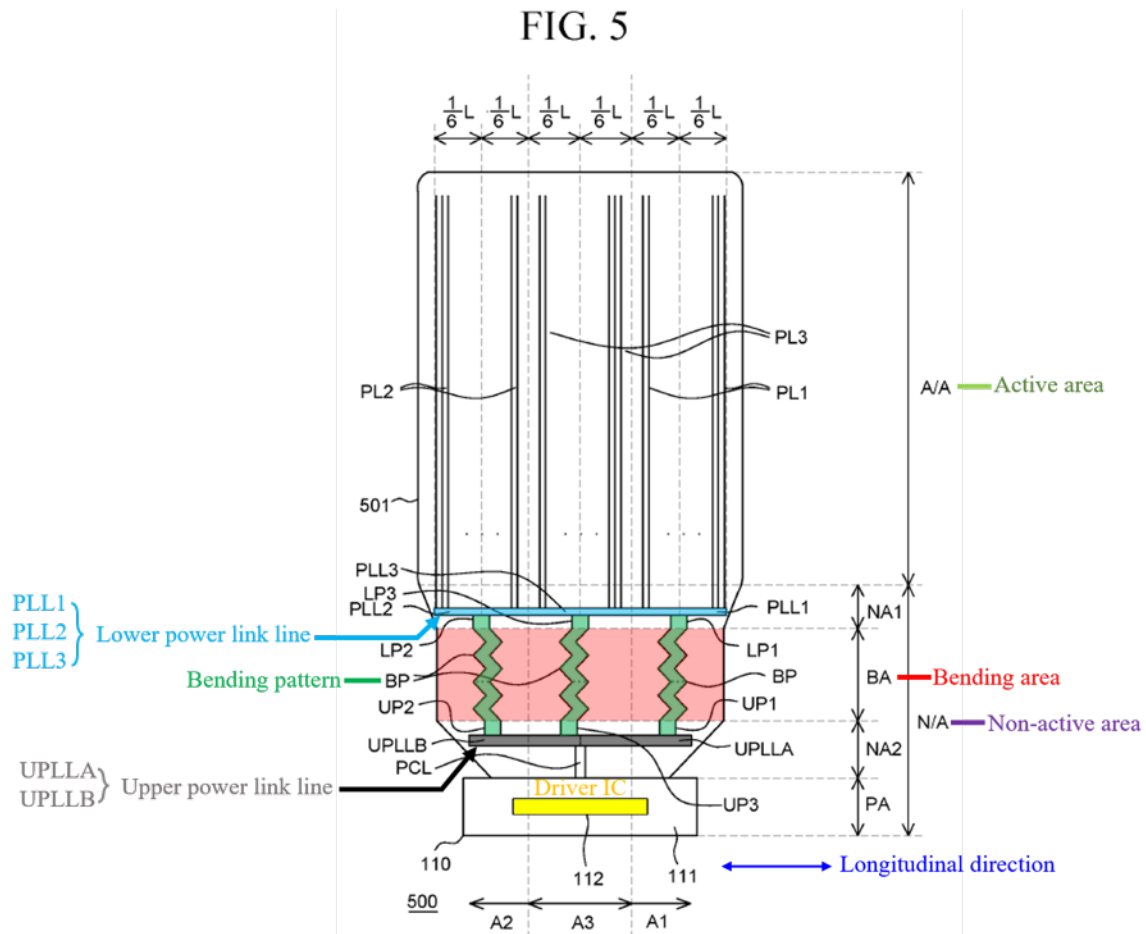
- 2. Dependent Claim 2: The display panel according to claim 1, wherein the first section of the second power trace and the second section of the second power trace are parallel to each other, and a width of the first section of the second power trace is less than a width of the second section of the second power trace, and is greater than a width of the second connecting sub-trace.**

194. Kwon in view of Kang’261, and Ka (“Kwon-Kang’261-Ka”) teaches Claim 2.

195. The Kwon-Kang'261-Ka combination teaches that the first section of the second power trace and the second section of the second power trace are parallel to each other. As discussed in connection with claim Element 1[c], Kwon teaches that the first second power trace (the VDD line) sits between the active display area and the bend allowance section, stretching from left to right. Kwon teaches that power supply bus lines positioned in the non-display area adjacent to the active pixel matrix (first section) actually extend horizontally across the panel width (parallel to the bending axis). Kwon also teaches that for the second section on the pad and COF side that beyond the bending region and in the pad area or component disposing region, the power line conductors and bonding pad connections also extend horizontally across the width of the flexible film. Together the architecture for the two sections are parallel to each other in the unfolded planar layout. To the extent PO argues that Kwon does not expressly teach to use a parallel second section of the VDD line, nothing in Kwon would have precluded a POSITA from implementing such an obvious approach as a matter of routine design choice. A POSITA would have been motivated to do so for the reasons explained above in Section VIII.B.1. Indeed, such a configuration is taught by both Kwon and Kang'261. It would have been obvious to a POSITA to implement Kwon and Kang'261's teaching together such that that a first section of the VDD line above the bend allowance section would be parallel to a second section of the VDD line below it.

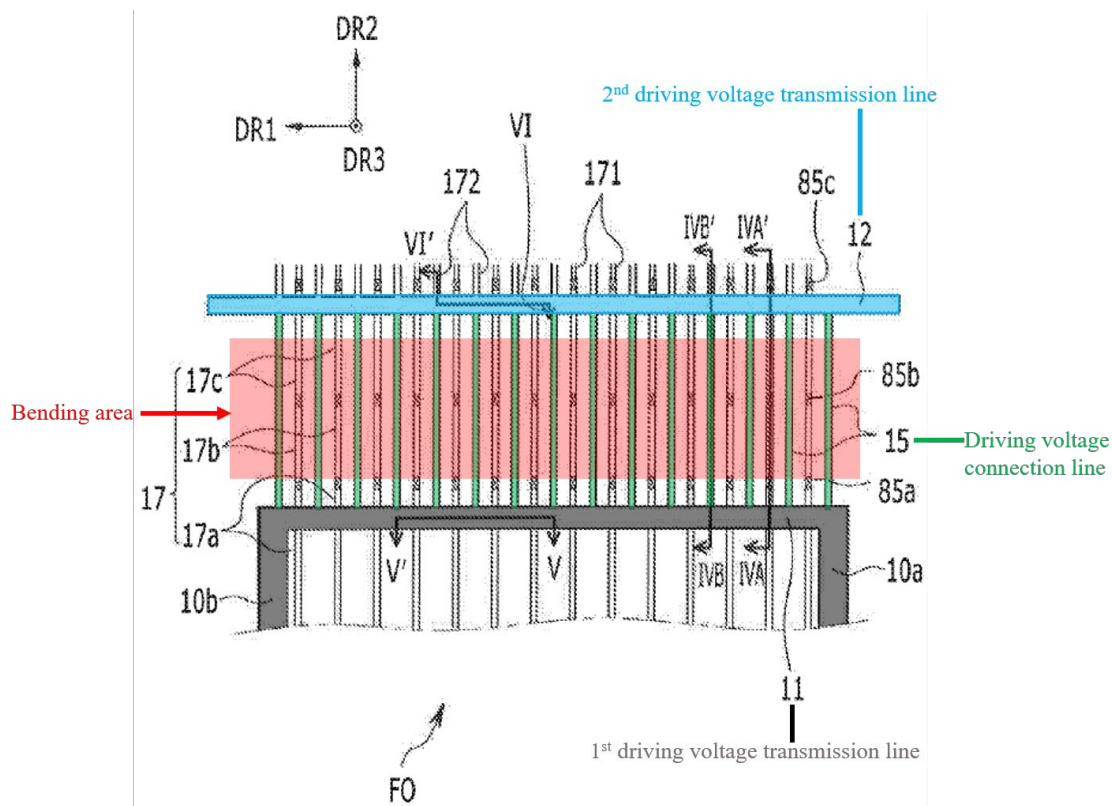
196. As explained in Section VIII.B.2 and shown in annotated Figure 5 below, Kang'261's first lower power link line PLL1 (blue) having the lower power link lines PLL1, PLL2 and PLL3 corresponds to the recited "first section of the second power trace" and Kang'261's first portion UPLLA of the upper power link line (grey) having the first and second portions UPLLA and UPLLB corresponds to the recited "second section of the second power trace." To address the voltage drop caused by the notched area in Kwon, Kang'261 teaches the upper power link line (grey) that is located under the bending area (red) and extends parallel to the lower power link line (blue). Ex-1006, Fig. 5. This configuration enables the bending patterns (green) to connect to the lower power link line at multiple points, thereby supplying power uniformly to the active area (green). Kang'261 further teaches that "substrate 501 of the display device 500 includes a first area A1, second area A2, and third area A3[,]" which "may be defined by dividing the length of the substrate 501 along a longitudinal direction." Ex-1006, 13:20-24. Moreover, Kang'261 teaches that "power voltage from the driver IC 112 [yellow] may be sequentially transmitted to the pad connecting line PCL, the first portion UPLLA of the upper power link line, the first upper connecting line UP1, a bending pattern BP, the first lower connecting line LP1, the first lower power link line PLL1, and the first power lines PL1 in sequence, to transmit power voltage to pixels disposed in the first area A1." Ex-1006, 14:59-66; *see also id.*, 14:66-15:6 (describing the same for the power

transmitted UPPLB through second lower power link line PLL2). Kang'261's lower and upper power link lines (blue and grey) corresponding to the claimed first and second sections of the second power trace, respectively, extend the longitudinal direction and, thus, Kang'261's first section of the second power trace and the second section of the second power trace are parallel to each other. *Id.*; Ex-1006, Fig. 5.



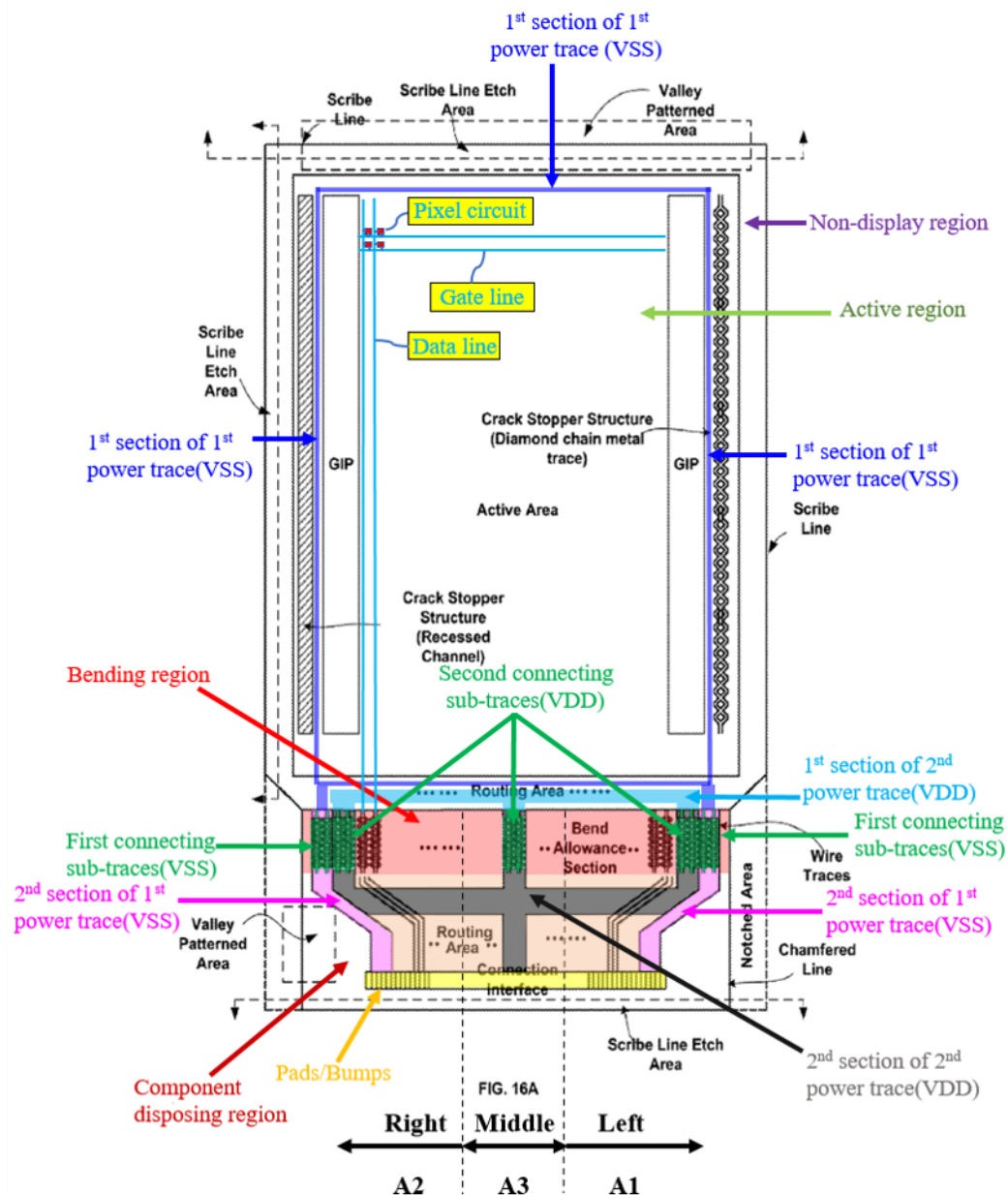
197. Indeed, this parallel relationship is additionally taught by Ka. For example, as shown below in Ka's annotated Figure 3, an upper voltage driving line (blue) and a lower voltage driving line (gray) are parallel extending horizontally,

connected by a number of smaller vertical lines (green). Similar to Kang'261, to resolve the voltage drop resulting from the notched area in Kwon, Ka teaches the 1st driving voltage transmission line (grey) that is located under the bending area (red) and extends parallel to the 2nd driving voltage transmission line (blue). Ex-1007, Fig. 3. This structure allows the driving voltage connection lines (green) to connect to the 2nd driving voltage transmission line (blue) at multiple points, facilitating a uniform power supply to the active region.



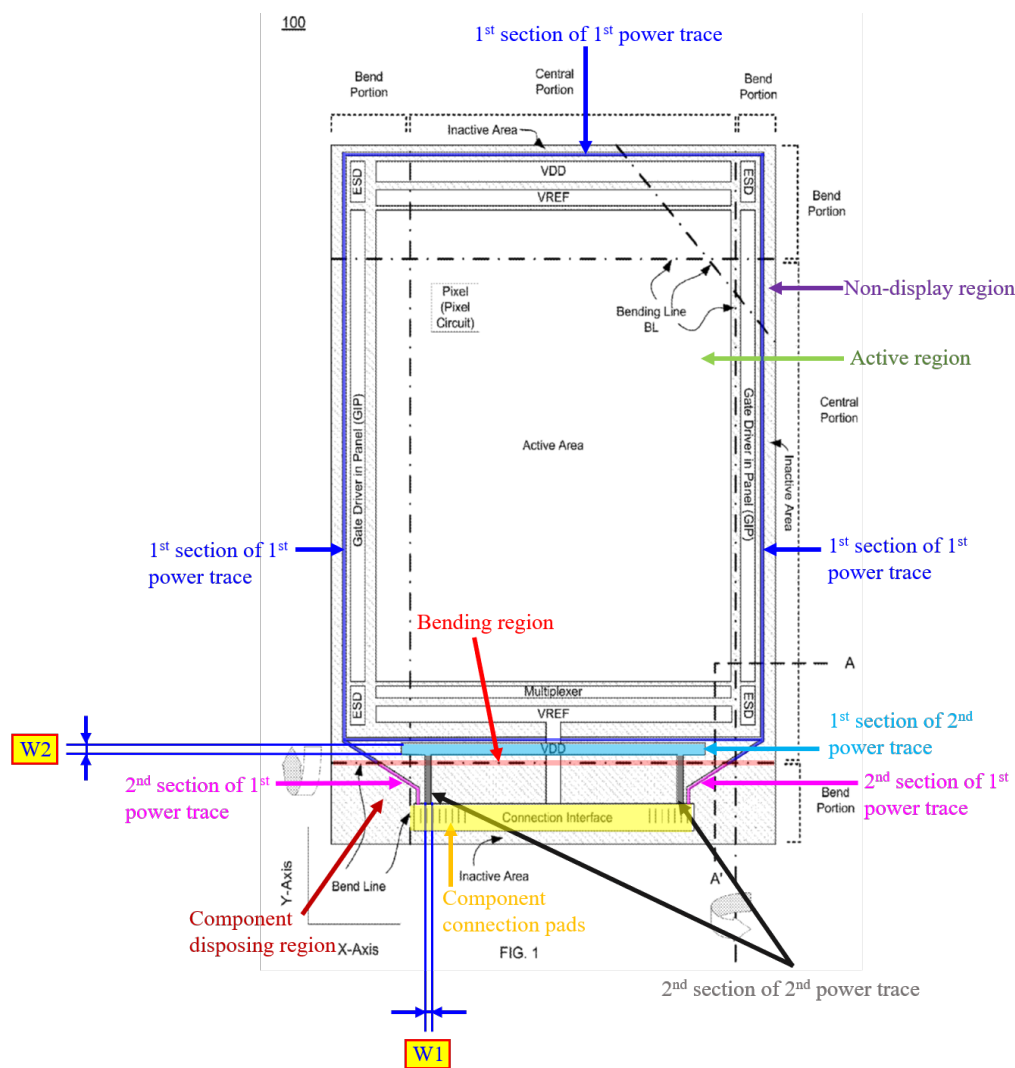
198. Thus, the combined system would have included the respective teachings from Kwon's Figure 16A, Kang'261's Figure 5, and Ka's Figure 3, as in

the modified figure below. As depicted in the figure, both the first section (light blue) and second section (gray) of the VDD lines are parallel to each other. Ex-1005, Fig. 16A.



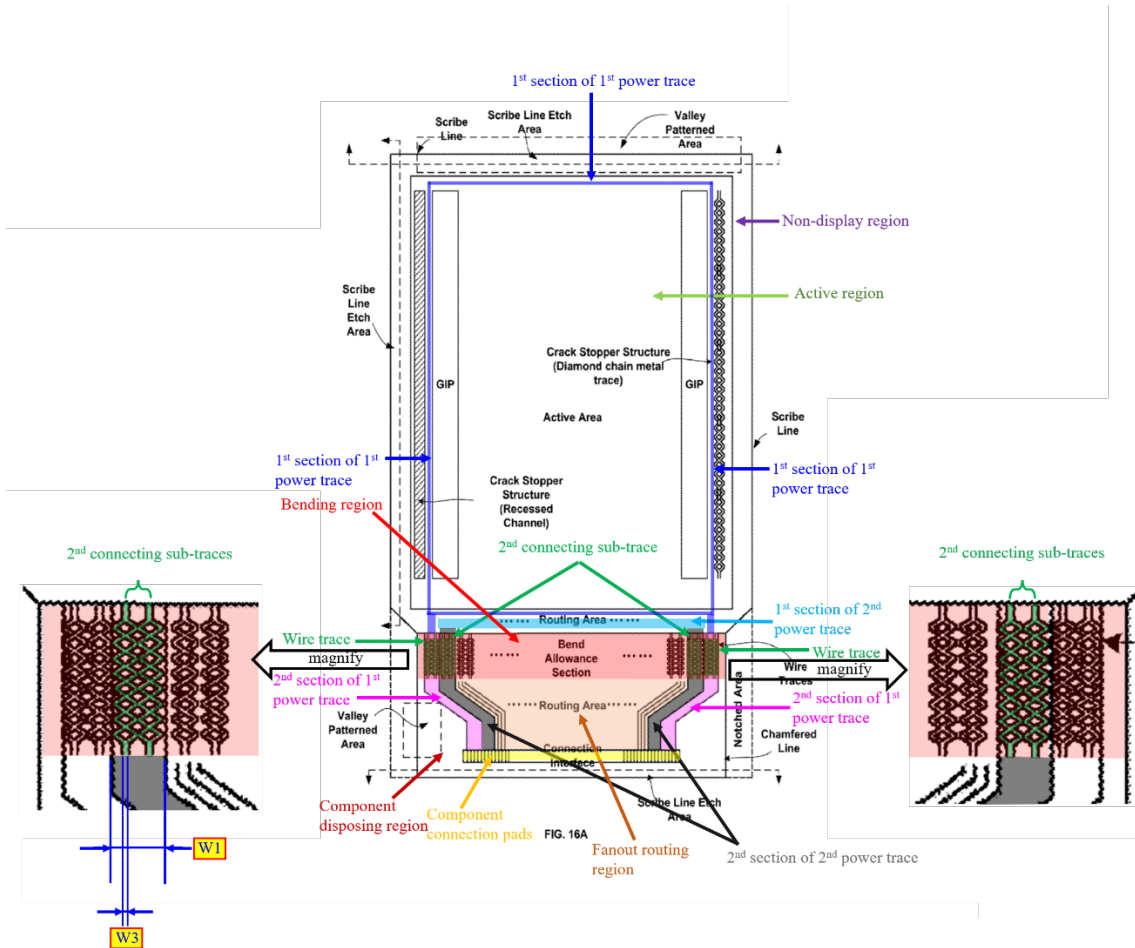
199. Kwon also teaches that a width of the first section of the second power trace is less than a width of the second section of the second power trace, and is

greater than a width of the second connecting sub-trace. As shown in Figure 1 of Kwon below, the second section of the second power trace (grey) has a first width W1, the first section of the second power trace (blue) has a second width W2 which is relatively greater than the first width W1.



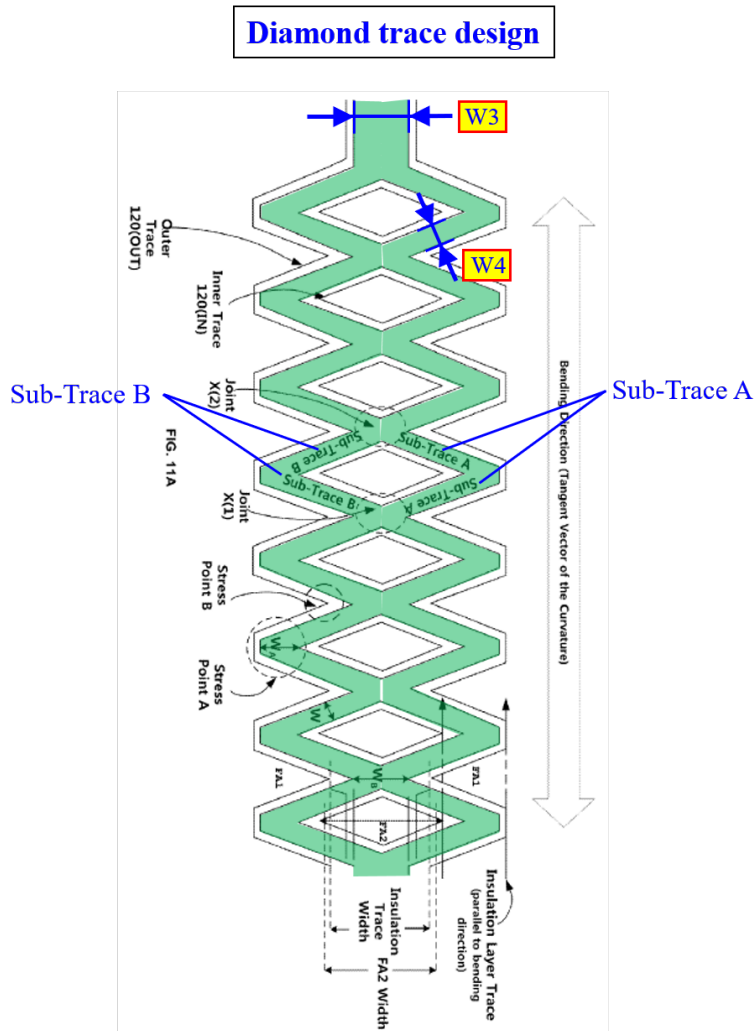
200. As shown in annotated Figure 16A of Kwon below, the second connecting sub-trace (green) has a third width W3. The third width W3 is relatively

greater than the first width W1 of the second section of the second power trace (grey) which is also shown in annotated Figure 1 above.



201. As shown in annotated Figure 11A of Kwon below, Sub-Trace A has a fourth width W4. The fourth width W4 is relatively smaller than the third width W3 of the second connecting sub-trace (green) which is also shown in annotated Figure 16A above. Kwon teaches that “the width of the conductive line 120 measured in the direction perpendicular to the tangent vector of the curvature at the stress points A [and B] ranges from about 2.5 μm to about 8 μm , more preferably, from about 3.5

um to about 6 um, more preferably from about 4.5 um to about 8.5 um, and more preferably at about 4.0 um.” Ex-1005, 28:1-7.



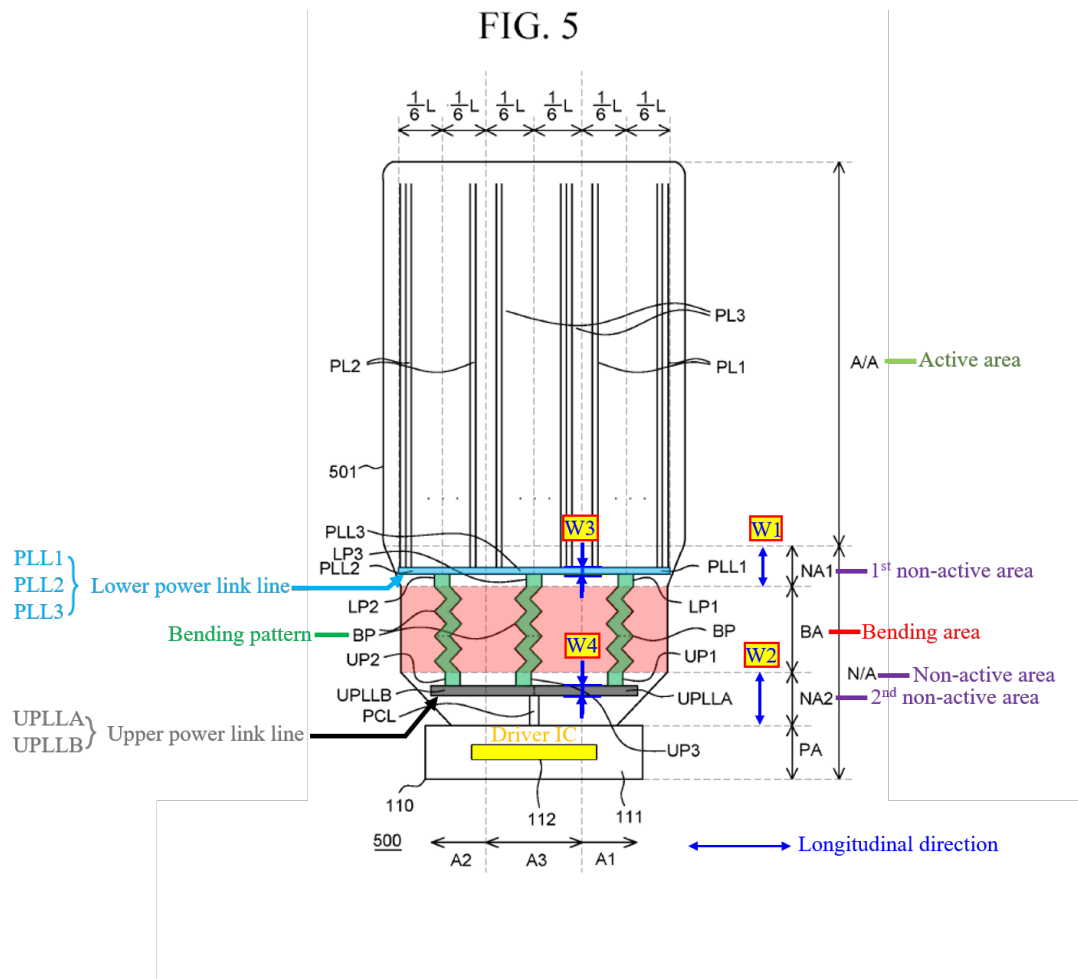
202. Thus, Kwon teaches some specific widths for its subtraces, with widths selected to minimize stress along the bend allowance area. Ex-1005, 28:1-7. As shown in Figures 1, 16A and 11A of Kwon above, the second width W2 of the first section of the second power trace is greater than the third width W3 and/or the fourth width W4 of the second connecting sub-trace. Further, since the third width W3

and/or the fourth width W4 of the second connecting sub-trace are implemented with a smaller width to minimize the impact of bending stress, it would have been obvious to a POSITA that the second width W2 of the first section of the second power trace, which is unaffected by bending stress, is greater than the third width W3 or the fourth width W4 of the second connecting sub-trace.

203. The Kwon-Kang'261 combination or the Kwon-Kang'261-Ka combination also teach that a width of the first section of the second power trace is less than a width of the second section of the second power trace. As shown in Kang'261's annotated Figure 5 below, the first non-active area (purple) has a first width W1. The second non-active area (purple) has a second width W2 relatively greater than the first width W1. Kang'261 discloses that "the bending area BA is bent in a bending direction in the final product (e.g., to allow circuitry to be placed behind and overlapping with the display panel)." Ex-1006, 7:11-13. That is, in Kang'261, to reduce bezel size, the inactive area was bent to the rear of the active area. The first non-active area (purple) remains in front side and needs to be covered by the bezel. When the first width W1 of the first non-active area (purple) increases, an area of the active area (light green) decreases. Therefore, it would have been understood by a POSITA that the first non-active area (purple) should be minimized as much as possible. Kang'261 also explains this understanding of those skilled in the art through the following teachings. Kang teaches that "the study of reducing

bezel sizes in display devices is one of them” and “two approaches to reducing the size of a bezel are: bending a non-active area of a substrate and reducing the size of the non-active area itself.” Ex-1006, 10:46-49. In contrast, the second non-active area (purple) is a region disposed on the rear side of the panel due to the bending of the bending region (red). Since the rear side of the panel is an area where light is not emitted, the second non-active area (purple) can be designed to have a larger size compared to the first non-active area (purple). Due to the reasons in the art described above, it is reflected in annotated Figure 5 of Kang’261 that the first non-active area (purple) has the first width W1 which is relatively narrow and the second non-active area (purple) has the second width W2 which is relatively wide. Kang’261 teaches that “the inventors realized that when power voltage is supplied to a plurality of pixels from a driver IC, power voltage drop may occur due to resistance in the power lines, causing non-uniformity in brightness among the plurality of pixels,” and “to compensate for the power voltage drop, a higher voltage was typically supplied.” Ex-1006, 1:54-59. As understood in the art, the resistance of a power line decreases as the power line becomes thicker. Therefore, a thicker power line results in less power voltage drop, reducing the need for a higher voltage. As described above and illustrated in annotated Figure 5 below, the second width W2 of the second non-active area (purple) is greater than the first width W1 of the first non-active area (purple). Therefore, a POSITA would have reduced resistance by widening the upper

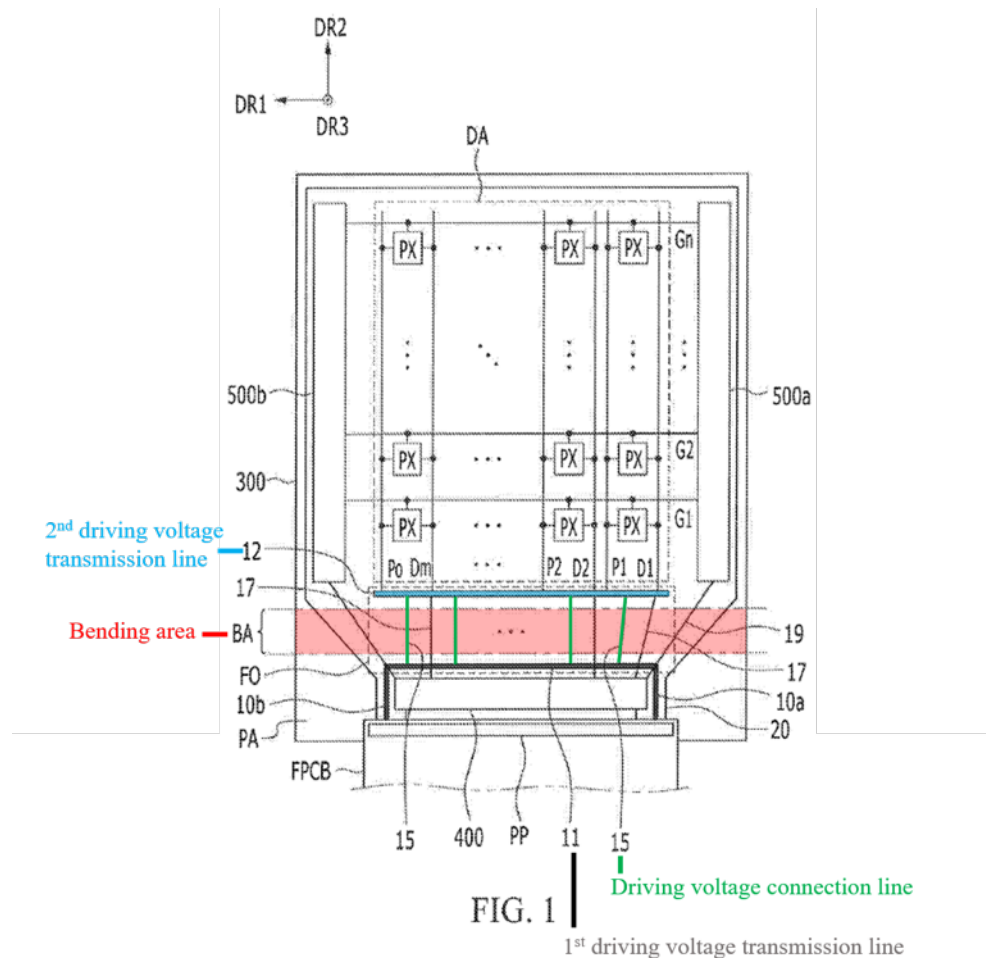
power link line (grey) under the condition that W2 is wider. This understanding by a POSITA is reflected in annotated Figure 5, where the lower power link line (blue) has a third width W3, and the upper power link line (grey) is depicted as having a fourth width W4 relatively greater than the third width W3. Accordingly, the Kwon-Kang'261 combination teaches that “a width of the first section of the second power trace (blue) is less than a width of the second section of the second power trace (grey).”



204. As explained above in the motivation to combine section, Kwon also teaches some specific widths for its subtraces, with widths selected to minimize stress along the bend allowance area. Ex-1005, 28:1-7. Thus, Kwon or the Kwon-Kang'261 combination teach specific widths for their subtraces and other components. Kwon and Kang'261, however, leave some implementation details for other common traces and specific widths of the same to a POSITA. To the extent that a POSITA would have been interested in such routine details, they are taught by Ka.

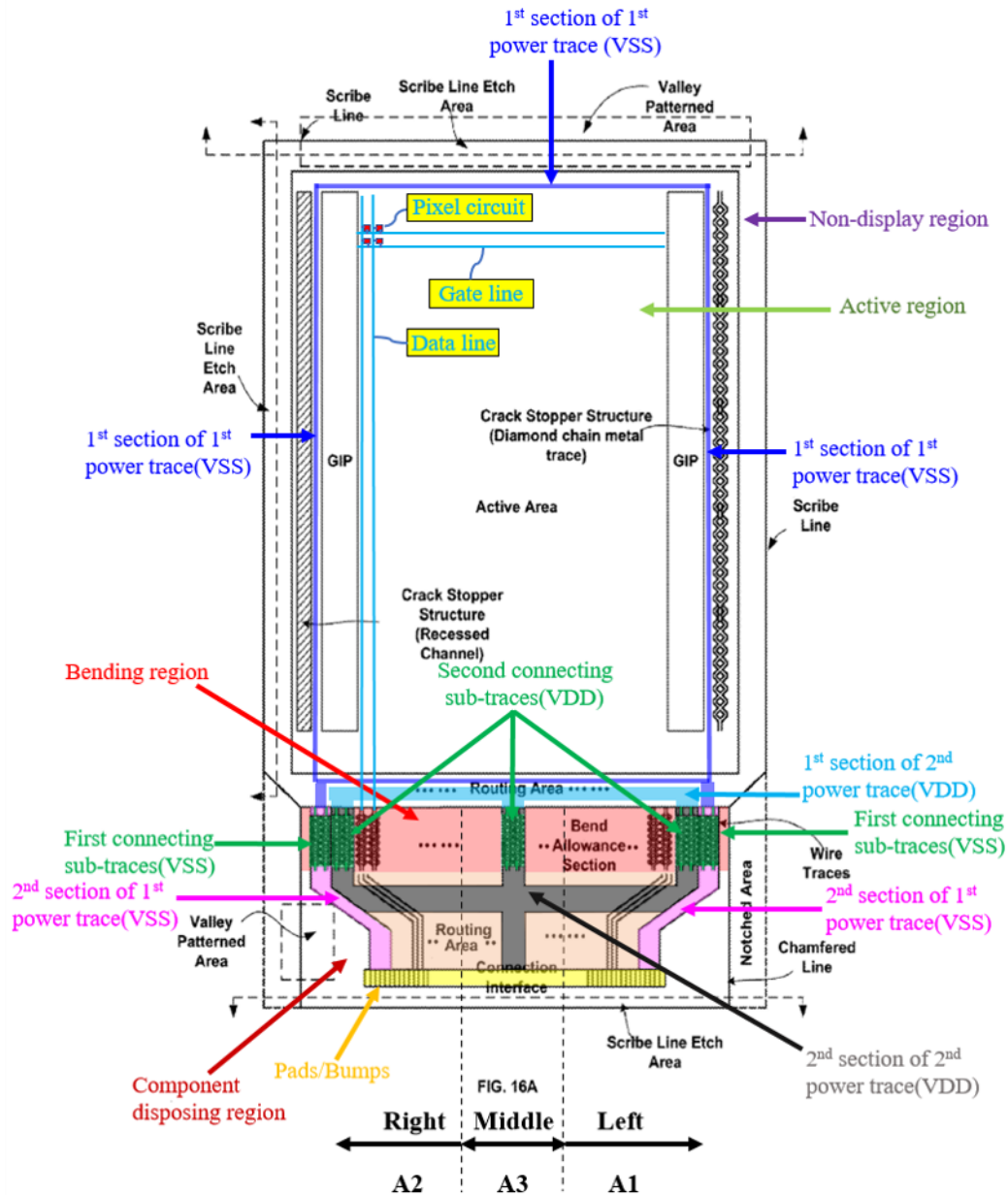
205. For example, Ka teaches that a width of the first section of the second power trace is less than a width of the second section of the second power trace, and is greater than a width of the second connecting sub-trace. Ka teaches “a display device[,]” which “includes a display panel including a display area and a peripheral area, a plurality of data lines and a plurality of driving voltage lines provided in the display area, a plurality of data connection lines provided in the peripheral area and connected to the plurality of data lines, *a first driving voltage transmission line* provided in the peripheral area and overlapping the plurality of data connection lines, *a second driving voltage transmission line* provided in the peripheral area and disposed between the first driving voltage transmission line and the display area, and *a plurality of driving voltage connection lines.*” Ex-1007 ¶5. Ka further teaches that “the first driving voltage transmission line 11 ... is connected to the second driving

voltage transmission line 12 through the plurality of driving voltage connection lines 15.” Ex-1007 ¶65. As shown in annotated Figure 1 below, Ka’s second driving voltage transmission line 12 (blue) corresponds to the recited “first section of the second power trace,” first driving voltage transmission line 11 (grey) corresponds to the recited “second section of the second power trace),” and driving voltage connection line 15 corresponds to the recited “second connecting sub-trace.” Ex-1007, Fig. 1.



206. Referring to Ka's objectives of achieving a narrow bezel and preventing voltage drop, a POSITA would have recognized from Figure. 3 above that the width of the first driving voltage transmission line (blue) is less than that of the first driving voltage transmission line (grey) and the width of the first driving voltage transmission line (blue) is greater than that of the driving voltage connection line (green). Ka teaches that "the first driving voltage transmission line 11 and the second driving voltage transmission line 12 may each have a width of about 50 to about 200 micrometers, and the driving voltage connection line 17 may have a width of about 3 micrometers[,]" and "the inventive concept is not limited thereto." Ex-1007 ¶74. As applied in the Kwon-Kang-Ka combination, this teaching would practice the claim. Specifically, a POSITA would have implemented the upper section of the VDD line (blue) at the lower end of the width range suggested by Ka, e.g. 50-100 microns, since it is placed in the relatively narrow section between the display active area and the bend allowance section. This would additionally keep the non-display area around the phone's bezel as small as possible, which is a stated goal of both Kwon and Ka. And the subraces (green) would have been implemented with a width of about 3 microns as suggested by Ka (and similar in width to what is taught by Kwon itself). The lower section of the VDD line (the horizontal grey line added from Kang'261) would have been implemented at the higher end of the width range suggested by Ka, e.g. 100-200 microns, since it connects to a number of subraces in

the routing area the additional line (Kang'261's PCL) coming out of the bottom and then connecting with the connection interface.



207. Like Ka, the wiring thickness in the bending area in Kwon is thinner than in the non-bending area to resolve the crack issue occurring in the bending region. Particularly, Kwon teaches that “the width of the conductive line 120 . . . at

the stress points A ranges from about 2.5 um to about 8 um, more preferably, from about 3.5 um to about 6 um, more preferably from about 4.5 um to about 8.5 um, and more preferably at about 4.0 um” and the “width of the conductive line 120 at the stress points B should also be maintained in the similar manner as the width of the conductive line 120 at the stress points A.” Ex-1005, 28:10-17. Likewise, the wiring thickness in the bending area in Kang’261 is thinner than in the non-bending area to resolve the crack issue occurring in the bending region. Particularly, Kang’261 teaches that that “the bending patterns BP of the power link line may be formed into a pattern of a specific shape to minimize stress and cracks on the plurality of link lines in the bending area BA” and “for example, the bending patterns BP may employ repeated patterns having at least one of a diamond, rhombic, zigzag, or circular shape, but is not limited thereto.” Ex-1006, 7:14-21. It would have been understood by a POSITA that to resolve crack issues in the bending area, the wiring outside the bending region should be configured with thinner traces when passing through the bending area.

208. Accordingly, in the Kwon-Kang’261-Ka combination, a width (50-100 microns) of the first section of Kwon’s second power trace (blue) is less than a width (100-200 microns) of the second section of Kwon’s second power trace (gray), and a width of the first section of Kwon’s second power trace is greater than a width (~3 microns) of Kwon’s second connecting sub-trace (green). A POSITA would have

been motivated to combine Kwon-Kang'261 with Ka and had a reasonable expectation of success in doing so, for the reasons described in Section VIII.C.1.

3. Dependent Claim 4: The display panel according to claim 2, wherein a width of the first section of the second power trace is not greater than [150] microns.

209. In my opinion, Kwon-Kang'261-Ka teaches Claim 4.

210. Ka teaches that the width of the first section of the second power trace is not greater than 150¹⁹ microns. Specifically, Ka teaches that, as an example, “the first driving voltage transmission line 11 and the second driving voltage transmission line 12 may each have a width of about 50 to about 200 micrometers” and “the inventive concept is not limited thereto.” Ex-1007 ¶74. As shown in annotated Figure 1 below and explained above for Claim 2, Ka's second driving voltage transmission line 12 (blue) corresponds to the recited “first section of the second power trace.” Ex-1007, Fig. 1. Additionally, as explained above in connection with Claim 2, the width would be on the lower end of the range, e.g., 50-100 microns, to minimize the bezel area around the display. Indeed, While a portion of the range taught by Ka is greater than 150 microns, a POSITA would have been motivated to implement Ka's teachings in Kwon's system such that the width of Kwon's first section of the second power trace is not greater than 150 microns, as recited, because

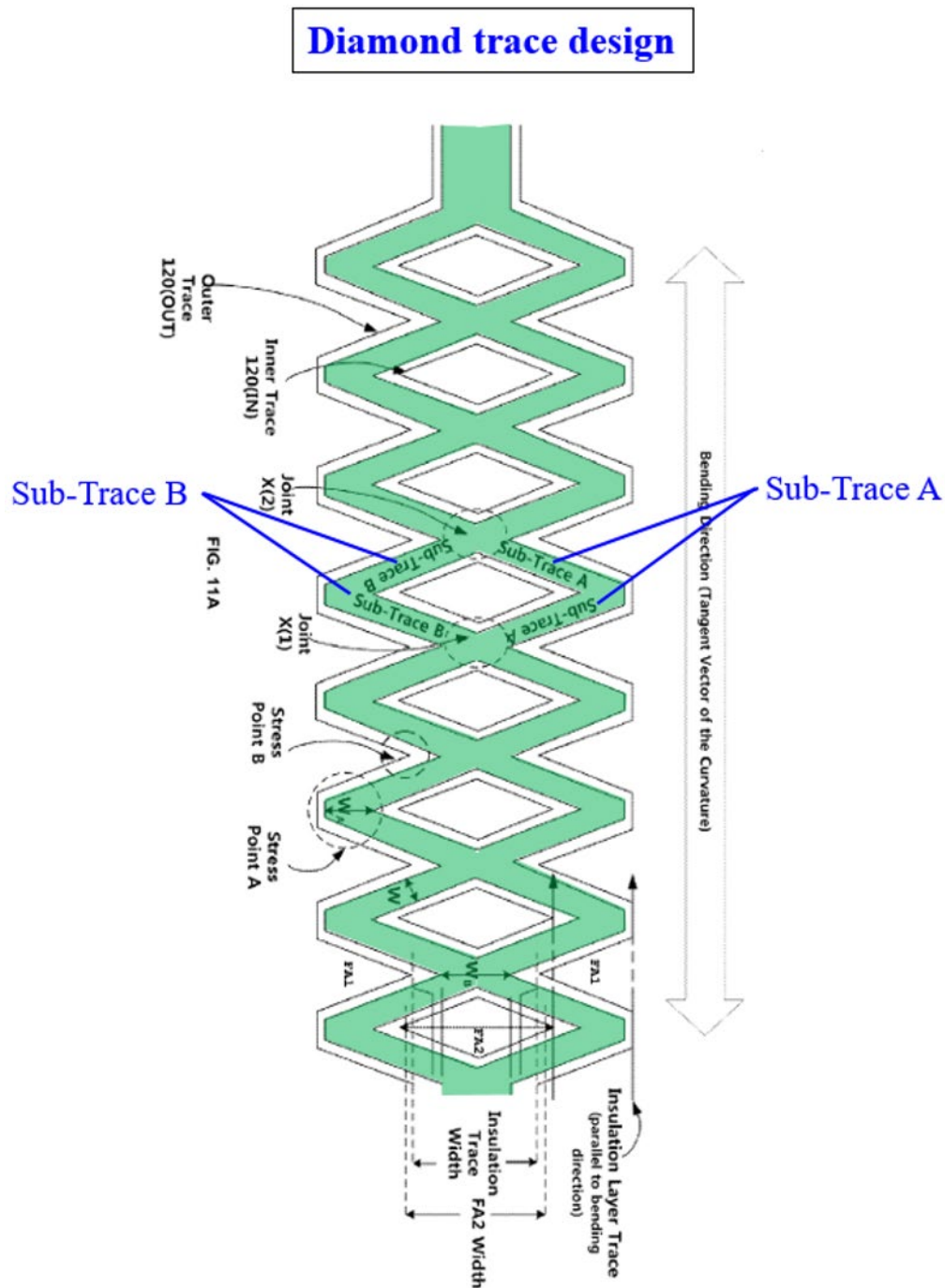
¹⁹ Applicant filed a certificate of correction that “ISO” should read as “150.” Ex 1004, 325-27.

covers the peripheral area PA in the display device, such as a smart phone, can be reduced.” Ex-1007 ¶69; *see also* Ex-1001, 4:49-53 (the display panel of the present invention not only greatly shortens “a length of a bottom border of the display panel, but also realize[s] the full-screen display design, and can also have a smaller smartphone size under the same display size”). It would thus have been obvious based on the combined teachings of Kwon and Ka to implement width of Kwon’s first section of the second power trace such that it is on the lower end of Ka’s range, and not greater than 150 microns, because Kwon, Kang’261, and Ka all relate to flexible display devices having display panels, which a POSITA would have understood should be designed and/or modified to be a suitable size for a smartphone. Moreover, a POSITA would have understood that a trace width limitation of less than 150 μm represents a normal and routine engineering design choice and optimization within an established numerical range in the display industry. Further, a POSITA would have understood that the 150 μm limitation is a linear dimension constraint that would have been viewed as a routine outcome of Ka’s trace-splitting teachings and standard industry bezel-narrowing practices.

4. Dependent Claim 5: The display panel according to claim 2, wherein a width of the second connecting sub-trace is not greater than 20 microns.

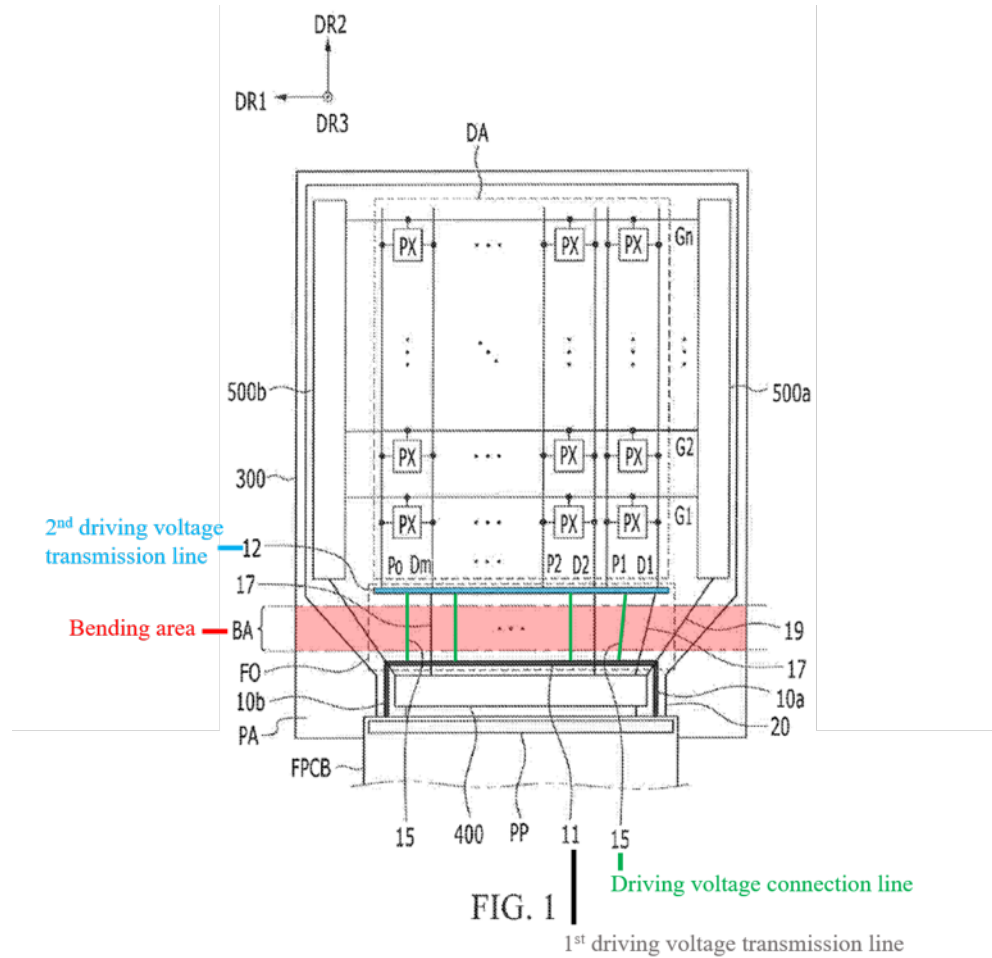
212. In my opinion, Kwon-Kang’261-Ka teaches Claim 5.

213. Kwon teaches that a width of the second connecting sub-trace is not greater than 20 microns. Specifically, “the width of the conductive line 120 . . . at the stress points A ranges from about 2.5 um to about 8 um, more preferably, from about 3.5 um to about 6 um, more preferably from about 4.5 um to about 8.5 um, and more preferably at about 4.0 um” and the “width of the conductive line 120 at the stress points B should also be maintained in the similar manner as the width of the conductive line 120 at the stress points A.” Ex-1005, 28:1-9. This is further depicted, for example, in annotated Figure 11A, below. Ex-1005, Fig. 11A. Kwon teaches that “[r]eferring to FIG. 11A, the conductive line 120 includes sub-trace A and sub-trace B, which are split away from each other and merge back at each joint X.” Ex-1005, 25:48-50. “In this example, the shape of the conductive line 120 between the joint X(1) and X(2) (i.e., link) has a diamond shape with an open area surrounded by the sub-trace A and the sub-trace B. With additional joints X, the conductive line 120 forms a chain of diamond shaped links, and thus the trace design may be referred to as the diamond trace design.” Ex-1005, 25:61-67. A POSITA would thus have understood that Kwon teaches that the width of the second connecting sub-trace is less than 8.5 microns.



214. This is also taught by Ka. Ka teaches that there are a “plurality of driving voltage connection lines 15 connecting the first driving voltage transmission line 11 and the second driving voltage transmission line 12[.]” Ex-1007 ¶74. As

shown in annotated Figure 1 below and explained above for Claim 2, Ka's driving voltage connection line 15 (green) corresponds to the recited "second connecting sub-trace." Ex-1007, Fig. 1. Ka further teaches that "the driving voltage connection line ... may have a width of about 3 micrometers." Ex-1007 ¶74. Ka thus teaches that a width of the second connecting sub-trace is not greater than 20 microns. Moreover, a POSITA would have understood that the fine-line dimensions are the predictable result of mechanical strain optimization and routine micro-lithographic design choices. A POSITA would have also understood that to create a reliable bendable or foldable display without breaking internal wiring, engineers must manage the mechanical stress concentrated at the bending axis.



5. **Dependent Claim 6: The display panel according to claim 3, wherein a width of the second section of the second power trace is not greater than 250 microns.**

215. In my opinion, Kwon-Kang'261-Ka teaches Claim 6.

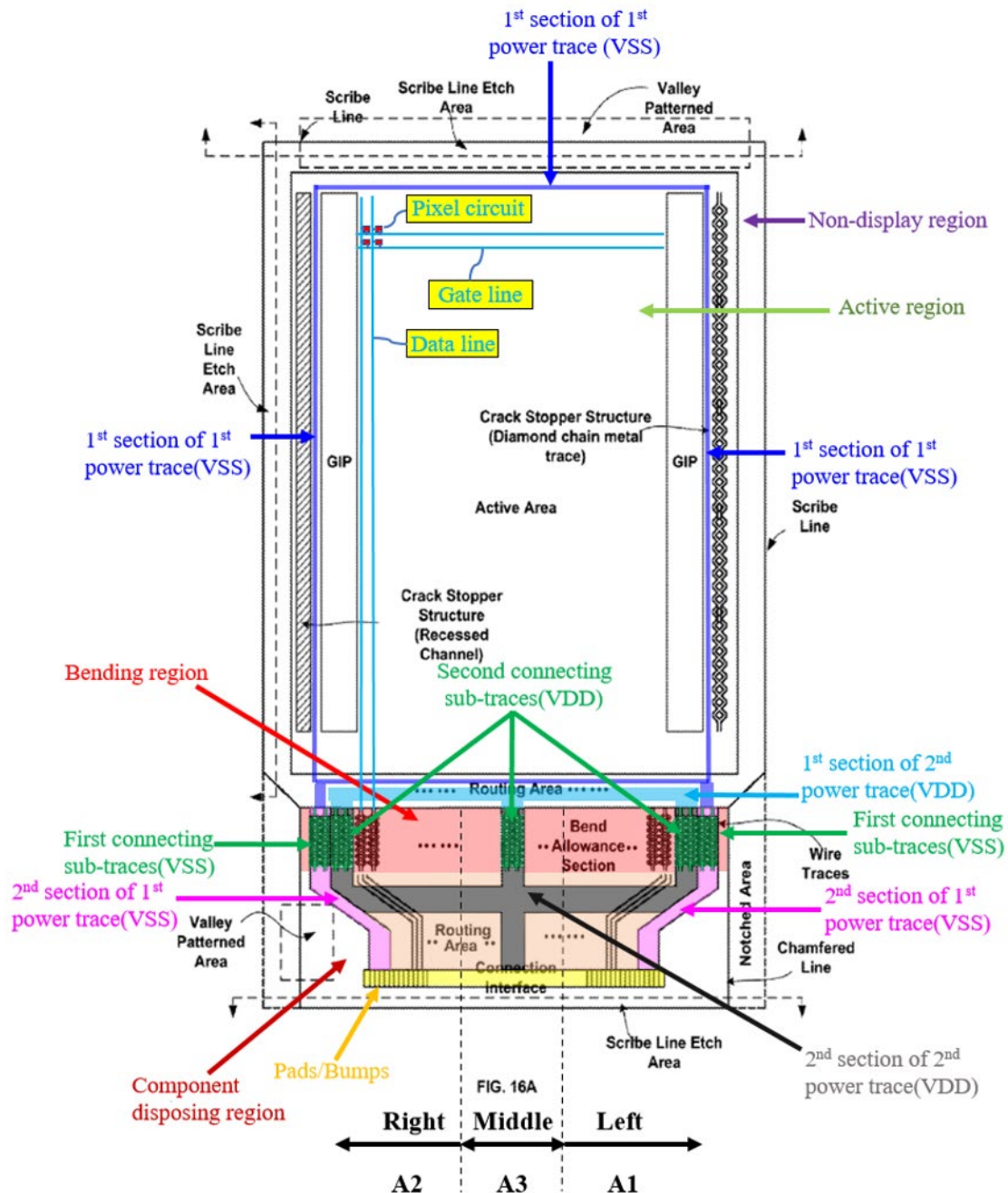
216. The Kwon-Kang'261 combination teaches the recited "second section of the second power trace" for the reasons described in Section VIII.B.2.

217. Ka teaches that a width of the second section of the second power trace is not greater than 250 microns for the reasons described for Claim 2. Indeed, the high end of Ka's range is 200 microns, which is less than 250 microns. Ex-1007 ¶74.

- 6. Dependent Claim 8: The display panel according to claim 6, wherein a width of the first section of the first power trace and a width of the second section of the first power trace are greater than a width of the first connecting sub-trace.**

218. In my opinion, Kwon-Kang'261-Ka teaches Claim 8.

219. Ka teaches this limitation for the reasons described for Claims 2 above. Specifically, in the Kwon-Kang'261-Ka combination, a width (50-100 microns) of the first section of Kwon's second power trace (blue) is less than a width (100-200 microns) of the second section of Kwon's second power trace (gray), and a width of the first section of Kwon's second power trace is greater than a width (~3 microns) of Kwon's second connecting sub-trace (green). Moreover, a POSITA would have understood that in a bendable, flexible display design, making the main power trace sections wider than the individual bending sub-traces would have been a standard textbook engineering requirement in flexible circuit design and a routine design choice.



7. **Dependent Claim 9:** The display panel according to claim 6, wherein a width of the first connecting sub-trace is not greater than 20 microns.

220. In my opinion, Kwon-Ka teaches Claim 9 for Claim 5.

8. **Claim 12: The display panel according to claim 11, wherein the first section of the power trace and the second section of the power trace are parallel to each other, and a width of the first section of the power trace is less than a width of the second section of the power trace, and is greater than a width of the connecting sub-trace.**

221. Kwon-Kang'261-Ka teaches Claim 12 for the reasons described for Claim 2.

9. **Dependent Claim 13: The display panel according to claim 12, wherein a width of the first section of the power trace is not greater than 150 microns.**

222. In my opinion, Kwon-Kang'261-Ka teaches Claim 13 for the reasons described for Claim 4.

10. **Dependent Claim 14: The display panel according to claim 12, wherein a width of the connecting sub-trace is not greater than 20 microns.**

223. In my opinion, Kwon-Kang'261-Ka teaches Claim 14 for the reasons described for Claim 5.

11. **Dependent Claim 15: The display panel according to claim 12, wherein a width of the second section of the power trace is not greater than 250 microns.**

224. In my opinion, Kwon-Kang'261-Ka teaches Claim 15 for the reasons described for Claim 6.

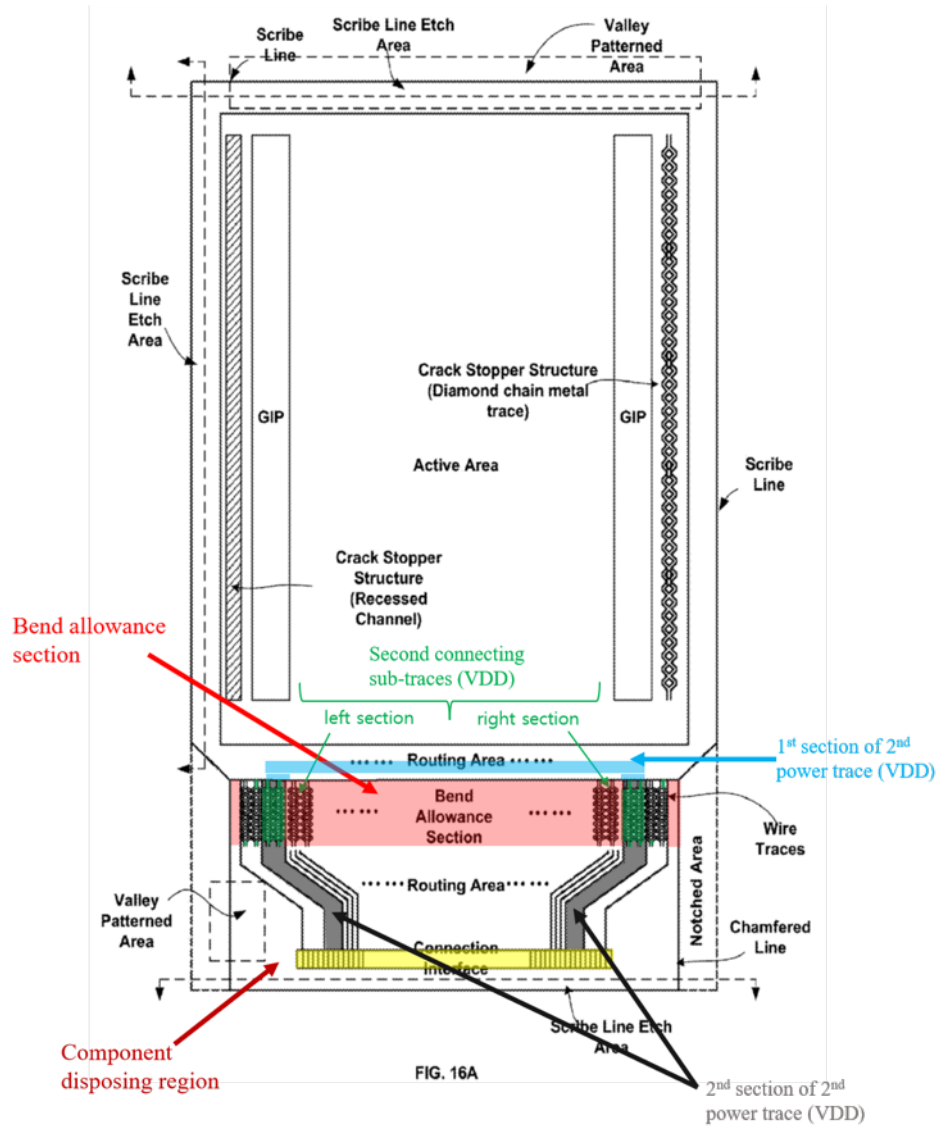
- 12. Dependent Claim 17: The display panel according to claim 16, wherein the first section of the power trace and the second section of the power trace are parallel to each other, and a width of the first section of the power trace is less than a width of the second section of the power trace, and is greater than a width of the connecting sub-trace.**

225. Kwon-Kang'261-Ka teaches Claim 17 for the reasons described for Claim 2.

- 13. Dependent Claim 18: The display panel according to claim 16, wherein the first section of the power trace is separately connected to the second section of the power trace disposed within the component disposing region by two sets of the connecting sub-traces passing through two sections of the bending region.**

226. Kwon-Kang'261-Ka teaches Claim 18.

227. Specifically, Kwon teaches that two sets of the connecting sub-traces of the power trace pass through two sections of the bending region for the reasons described in Sections VIII.A.1.e, VIII.B.2, and VIII.B.4.d. Ex-1005, Fig. 16A (annotated).



IX. CONCLUSION

228. For at least the reasons cited above, I believe that Claims 1-18 of the '891 Patent are unpatentable in view of the prior art.

229. I declare under the penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

U.S. Patent No. 11,257,891
Declaration of Michael Lebby, Ph.D.

Dated: September 11, 2026

Respectfully Submitted,

A handwritten signature in green ink, appearing to read 'Michael Lebby', is written over a horizontal line.

Michael Lebby, Ph.D.