

### **CERTIFICATE OF TRANSLATION ACCURACY**

I am a professional translator, reviewer, and/or project coordinator specializing in translating Korean, Japanese, and Chinese into English, and vice versa.

I served as Chief Examiner for the State of California's certified court interpreter exam and as a contract translator for various federal agencies through the U.S. Department of State for more than a decade. I taught at the University of California, Berkeley, and the Middlebury Institute of International Studies at Monterey Graduate Program in Translation.

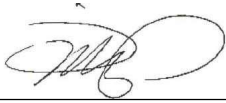
I have over 35 years of project coordination experience, routinely handling technical, legal, and business documents translated between English and Korean. These documents were submitted to entities including Korean judicial authorities, U.S. federal courts, the U.S. International Trade Commission (ITC), the U.S. Patent and Trademark Office (USPTO), and the USPTO Patent Trial and Appeal Board (PTAB).

I certify that I translated the following document from Korean into English. I further certify that it is a true, correct, and complete translation to the best of my knowledge and ability.

**KR 2017-0103740**

I certify under penalty of perjury that the foregoing is true and correct.

Executed this 31st day of May 2026 in Contra Costa County, State of California.

By: 

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Member, ATA



## Patent Application

|                                                            |                                                            |
|------------------------------------------------------------|------------------------------------------------------------|
| <b>[Application Category]</b>                              | Patent Application                                         |
| <b>[Applicant]</b>                                         |                                                            |
| <b>[Name]</b>                                              | LG Display Co., Ltd.                                       |
| <b>[Patent Client No.]</b>                                 | 1-1998-101865-5                                            |
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| <b>[Name]</b>                                              | INVENTUS Intellectual Property Group                       |
| <b>[Agent No.]</b>                                         | 9-2016-100001-1                                            |
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| <b>[General Power of Attorney Reg. No.]</b>                | 2014-036557-3                                              |
| <b>[Title of the Invention (Utility Model) in Korean]</b>  | DISPLAY DEVICE                                             |
| <b>[Title of the Invention (Utility Model) in English]</b> | DISPLAY DEVICE                                             |
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|                               |        |
|-------------------------------|--------|
| <b>[Application Language]</b> | Korean |
|-------------------------------|--------|

**[Purpose]**

This application is hereby submitted to the Commissioner of the Korean Intellectual Property Office (KIPO) as stated above.

Agent, Attorney, or Firm

INVENTUS Intellectual Property Group (signature or seal)

**[Fees]**



|                                          |                      |
|------------------------------------------|----------------------|
| <b>[(Basic) Application Fee]</b>         | 0 page(s) 46,000 KRW |
| <b>[Additional Fee]</b>                  | 65 pages 0 KRW       |
| <b>[Priority Claim Fee]</b>              | 0 case(s) 0 KRW      |
| <b>[Fee for Request for Examination]</b> | 0 claim(s) 0 KRW     |
| <b>[Total]</b>                           | 46,000 KRW           |



## **[Description of the Invention]**

### **[Title of the Invention]**

DISPLAY DEVICE {DISPLAY DEVICE [*in English*]}

### **[Technical Field]**

[0001] This specification relates to a display device, more particularly, to a display device capable of reducing power supply voltage drop and improving luminance uniformity through a new power supply voltage input method.

### **[Background Technology of the Invention]**

[0002] Flat-panel display devices, such as liquid crystal display devices (LCDs), organic light-emitting diode display devices (OLEDs), and quantum dot display devices (QDIs), are gaining attention in the spot light as next-generation display devices due to their thin profiles and low power consumption.

[0003] A display device includes a driver integrated circuit (Driver IC) that provides a power supply voltage for driving a plurality of pixels. The driver IC supplies the power supply voltage to each pixel via wired power lines arrayed in the display device.

[0004] However, the power supply voltage provided by the drive IC experiences a voltage drop as it travels through the lines; consequently, the power supply voltage supplied to each pixel is not constant, which may result in poor luminance uniformity in the display device. Therefore, there is a need for a method to supply a constant power supply voltage to a plurality of pixels in the display device.

### **[Summary of the Invention]**

### **[Problem to Be Solved]**

[0005] The inventors of this specification recognized the growing demand for flexible display devices, specifically the need to bend the non-display area to reduce the area footprint it occupies in a display device. To reduce the area of the non-display area, they removed a portion of it. Furthermore, they recognized that, in order to increase the area that can be removed, it is necessary to reposition various lines and components arranged in the non-display area. Accordingly, the inventors of this specification recognized that a design is

required to reduce the area occupied by power lines placed in the non-display area in order to minimize the area of the non-display area. Furthermore, while the power supply voltage is supplied from the drive IC to a plurality of pixels, a voltage drop occurs due to the resistance of the lines, resulting in uneven luminance across the pixels and requiring the application of a higher voltage to compensate for the voltage drop.

[0006] Accordingly, the inventors of the present specification have invented a display device capable of reducing the size of the non-display area and providing a constant power supply voltage by reducing the power supply voltage drop.

[0007] Accordingly, the object of this specification is to provide a display device that reduces power supply voltage drop and improves luminance uniformity by dividing the power supply voltage supply points.

[0008] Another problem that this specification seeks to solve is to provide a display device with improved luminance uniformity by disposing the power line, which supplies the power supply voltage, and the data line, which delivers the data voltage, so that they are both superimposed, thereby improving the delay deviations in the data voltage caused by parasitic capacitance.

[0009] The problems addressed in this specification are not limited to those mentioned above, and other problems not mentioned herein will be clearly understood by those skilled in the art from the following description.

#### **[Means to Solve the Problem]**

[0010] To solve the problems described above, a display device according to an embodiment of the present specification comprises a substrate comprising a display area provided with a plurality of pixels and a non-display area adjacent to the display area, a plurality of power lines provided in the display area to supply power to a plurality of pixels, comprising a plurality of first power lines and a plurality of second power lines; a lower power link line provided in the non-display area and connected to the plurality of power lines; a power link line comprising a first lower connection line and a second lower connection line extending from the lower power link line; wherein the plurality of first power lines includes at least two first power lines equidistant from the first lower connection line, and the plurality of second power lines includes at least two second power lines equidistant from the second lower connection line. Therefore, by dividing the points where the power supply voltage is supplied, the voltage drop of the power supply voltage can be reduced, and luminance uniformity can be improved.

[0011] To address the challenges described above, a display device according to another embodiment of the present specification comprises a substrate including a display area equipped with a plurality of pixels and a non-display area adjacent to the display area, a power link line comprising a plurality of power lines—including a plurality of first power lines and a plurality of second power lines—provided in the display area to supply power to the plurality of pixels, and a first lower power link line connected to the plurality of first power lines and a second lower power link line connected to the plurality of second power lines, both disposed in the non-display area. Furthermore, the first lower power link line and the second lower power link line are each disposed within the left and right areas of the substrate, respectively, thereby minimizing the amount of power supply voltage drop in the plurality of power supply lines and the power link line.

[0012] Further details regarding other embodiments are included in the detailed description and drawings.

#### **[Effect of the Invention]**

[0013] This specification can reduce the drop in power supply voltage by dividing the points where the power supply voltage is supplied and reducing the length of the lines to which the power supply voltage is applied, as well as the resulting resistance.

[0014] This specification can improve signal delay deviations caused by parasitic capacitance and line resistance by disposing the power line and the data line so that they are both superimposed.

[0015] The effects described in this specification are not limited to those illustrated above; a wider range of effects is included in this specification.

#### **[Brief Description of the Drawings]**

[0016] FIG. 1 is a plan view of a display device according to an embodiment of the present specification.

FIG. 2 is a cross-sectional view taken along line II-II' in FIG. 1.

FIG. 3 is a plan view of a display device according to another embodiment of the present specification.

FIG. 4 is a cross-sectional view taken along line IV-IV' in FIG. 3.

FIGS. 5 through 9 are plan views of a display device according to various embodiments of the present invention.

#### **[Detailed Description of Embodiments]**

[0017] The advantages and features of the present invention, as well as the methods for achieving them, will become clear upon reference to the embodiments described in detail below, together with the accompanying drawings. However, the present invention is not limited to the embodiments disclosed herein but may be implemented in various different forms; these embodiments are provided merely to ensure a complete

disclosure of the invention and to fully inform those skilled in the art of the scope of the invention, and the scope of the invention is defined solely by the claims.

[0018] The shapes, sizes, proportions, angles, and numbers disclosed in the drawings illustrating embodiments of the present invention are merely illustrative, and the present invention is not limited to the matters depicted therein. Throughout the specification, the same reference numerals denote the same components. Furthermore, in describing the present invention, detailed descriptions of related prior art are omitted if it is determined that such descriptions would unnecessarily obscure the essence of the present invention. When terms such as "includes/comprises," "has," or "consists of" are used in this specification, they imply that other elements may be added unless the term "only" is used. Unless otherwise explicitly stated, the use of a singular form of a component includes the plural form.

[0019] In interpreting the components, they shall be construed as including a margin of error even if not explicitly stated.

[0020] In the case of descriptions of positional relationships—for example, when the positional relationship between two parts is described using terms such as "on," "on the upper," "on the lower," or "adjacent to"—unless the terms "immediately" or "directly" are used, one or more other parts may be located between the two parts.

[0021] The term "on" a device or layer refers to a position immediately above another device or layer, or a position with another layer or device interposed between them.

[0022] Furthermore, terms such as "first" and "second" are used to describe various components, but these components are not limited by such terms. These terms are used merely to distinguish one component from another. Therefore, a "first" component mentioned hereinafter may also be a "second" component within the technical concept of the present invention.

[0023] Throughout the specification, the same reference numeral denotes the same component.

[0024] The dimensions and thicknesses of the various components shown in the drawings are provided for the convenience of description, and the present invention is not necessarily limited to the dimensions and thicknesses of the illustrated configurations.

[0025] The features of the various embodiments of the present invention may be partially or fully combined or integrated with one another; various technical interlockings and operations are possible; and each embodiment may be implemented independently of the others or in conjunction with them in an interrelated manner.

[0026] The display device according to an embodiment of this specification will be described in detail below with reference to the accompanying drawings.

[0027] FIG. 1 is a plan view of a display device according to an embodiment of this specification. For the sake of clarity, FIG. 1 shows only the substrate (101), power link line, power line, and drive IC (112) among the various components of the display device (100).

[0028] The substrate (101) serves as a base member for supporting various components of the display device (100) and may be made of an insulating material. For example, the substrate (101) may be made of plastic material such as glass or polyimide.

[0029] Referring to FIG. 1, the substrate (101) includes a display area (A/A) and a non-display area (N/A).

[0030] The display area (A/A) is an area in which a plurality of pixels are arranged to display an image. The display area (A/A) may include a display section for displaying an image and a circuit section for driving the display section. For example, if the display device (100) is an organic light-emitting display device, the display unit may include organic light-emitting elements. That is, the display unit may include an anode, an organic layer on the anode, and a cathode on the organic layer. The organic layer may, for example, consist of a hole transport layer, a hole injection layer, an organic light-emitting layer, an electron injection layer, and an electron transport layer. Furthermore, the circuit section may comprise various components such as a power line, thin-film transistors, storage capacitors, gate lines, and data lines, but is not limited thereto. Hereinafter, for the sake of convenience of description, it is assumed that the display device (100) is an organic light-emitting display device; however, the display device (100) is not limited to being an organic light-emitting display device.

[0031] Referring to FIG. 1, the display area (A/A) may have a rounded shape. As design aspects have recently gained prominence, there is a demand for display areas (A/A) with shapes other than the conventional rectangular form. Accordingly, the substrate (101) of the display device (100) according to one embodiment of this specification has a rounded shape. However, the shape of the display area (A/A) is not limited to this, and depending on the embodiment, the corners may be formed with a squared shape.

[0032] The non-display area (N/A) is an area where no image is displayed; it is an area where various lines and circuits for driving the display unit disposed in the display area (A/A) are located. In addition, the non-display area (N/A) may also contain a driver IC (112) that supplies signals for driving the display unit, as well as power link lines and data link lines.

[0033] The non-display area (N/A) can be defined as the area extending from the display area (A/A), as shown in FIG. 1. However, without being limited thereto, the non-display area (N/A) may also be defined as the area surrounding the display area (A/A).

[0034] Referring to FIG. 1, the non-display area (N/A) includes a first non-display area (NA1), a bending area (BA), a second non-display area (NA2), and a pad area (PA). The first non-display area (NA1) is an area extending from the display area (A/A), and the bending area (BA) is an area extending from the first non-display area (NA1) that is capable of bending. The second non-display area (NA2) is an area extending from the bending area (BA), and the pad area (PA) is an area extending from the second non-display area (NA2) where pads are disposed.

[0035] Meanwhile, the substrate (101) is defined as a display area (A/A) and a non-display area (N/A), and may also be defined as a first area (A1) and a second area (A2). The display area (A/A) and the non-display area (N/A) are defined by dividing the substrate (101) horizontally, while the first area (A1) and the second area (A2) may be defined by dividing the substrate (101) vertically. The first area (A1) is the left area of the substrate (101) and may be defined to include portions of the display area (A/A), the first non-display area (NA1), the bending area (BA), the second non-display area (NA2), and the pad area (PA), respectively. The second area (A2) is the right-hand area of the substrate (101) and may include other portions of the display area (A/A), the first non-display area (NA1), the bending area (BA), the second non-display area (NA2), and the pad area (PA), respectively. In this case, the first area (A1) and the second area (A2) may be symmetrical left and right.

[0036] The flexible film (110) is a film on which various components are disposed on a flexible base film (111), and serves as a component for supplying signals to the pixels in the display area (A/A). The flexible film (110) is disposed in the pad area (PA) of the non-display area (N/A) and supplies power supply voltage, data voltage, and other signals to the pixels in the display area (A/A) through the pads disposed in the pad area (PA). The flexible film (110) includes a base film (111) and a drive IC (112), and various other components may also be disposed thereon. In FIG. 1, the printed circuit board connected to the flexible film (110) has been omitted for the sake of simplicity.

[0037] The base film (111) is a layer that supports the flexible film (110). The base film (111) may be made of an insulating material; for example, it may be made of an insulating material that possesses flexibility.

[0038] The drive IC (112) is a component that processes data for displaying images and the drive signals

required to process that data. Depending on the method of mounting on the substrate (101) of the display device (100), the drive IC (112) may be disposed using methods such as Chip On Glass (COG), Chip On Film (COF), or Tape Carrier Package (TCP). In FIG. 1, for the sake of clarity, the drive IC (112) is shown mounted on a flexible film (110) using the Chip On Film method; however, the invention is not limited thereto.

[0039] A plurality of power lines are disposed in the display area (A/A), and a power link line is disposed in the non-display area (N/A). The plurality of power lines are lines for delivering a power supply voltage to the plurality of pixels disposed in the display area (A/A). The plurality of power lines receive the power supply voltage from the power link line and deliver it to the plurality of pixels.

[0040] The power link line is disposed in the non-display area (N/A) and serves to deliver the power supply voltage from the drive IC (112) to the power line. Specifically, the power link line is disposed in a first non-display area (NA1), a bending area (BA), and a second non-display area (NA2), connecting the drive IC (112) to a plurality of power lines, respectively. Thus, the power link line can deliver the power supply voltage to the plurality of power lines.

[0041] A plurality of power lines and power link lines may be formed from a conductive material. For example, the plurality of power lines and power link lines may be formed from one of various materials used in the fabrication of the gate electrodes, source electrodes, and drain electrodes of the organic light-emitting devices and thin-film transistors in the display area (A/A), and may be configured as a single layer or a multilayer. Specifically, the plurality of power lines and power link lines may be formed from molybdenum (Mo), chromium (Cr), titanium (Ti), nickel (Ni), neodymium (Nd), copper (Cu), and alloys of silver (Ag) and magnesium (Mg), among others.

[0042] Meanwhile, although FIG. 1 shows only a power link line and a plurality of power lines disposed on the substrate (101), various other lines—such as data lines, data link lines, and gate lines—that deliver data voltages to a plurality of pixels in the display area (A/A) may also be disposed. The data lines and data link lines will be described in detail later with reference to FIG. 2.

[0043] The power link line comprises a lower power link line disposed in a first non-display area (NA1), a plurality of bending patterns (BP) disposed in a bending area (BA), an upper power link line disposed in a second non-display area (NA2), and a pad connection line (PCL). Furthermore, the power link line may

further include a first lower connection line (LP1) and a second lower connection line (LP2) disposed in the first non-display area (NA1) to connect the lower power link line and the bending patterns (BP). Furthermore, the power link line may further include a first upper connection line (UP1) and a second upper connection line (UP2) disposed in the second non-display area (NA2) to connect the upper power link line to the bending pattern (BP).

[0044] The pad connection line (PCL) is connected to a pad disposed in the pad area (PA) and delivers the power supply voltage to the upper power link line disposed in the second non-display area (NA2).

[0045] The upper power link line is disposed in the central portion of the second non-display area (NA2) and includes a first portion (UPLLA) extending to the first area (A1) and a second portion (UPLLB) extending to the second area (A2). The upper power link line is connected to the pad connection line (PCL) at the center of the substrate (101). The first portion (UPLLA) and the second portion (UPLLB) of the upper power link line each extend from the second non-display area (NA2) to the central portions of the first area (A1) and the second area (A2), respectively.

[0046] The upper power link line is connected to a plurality of bending patterns (BP). Specifically, a first portion (UPLLA) of the upper power link line is connected to the bending patterns (BP) via a first upper connection line (UP1), and a second portion (UPLLB) is connected to the bending patterns (BP) via a second upper connection line (UP2). In this case, some of the plurality of bending patterns (BP) are connected to the first portion (UPLLA) of the upper power link line via the first upper connection line (UP1), and other ones of the plurality of bending patterns (BP) are connected to the second portion (UPLLB) of the upper power link line via the second upper connection line (UP2).

[0047] The first upper connection line (UP1) and the second upper connection line (UP2) are lines extending from a plurality of bending patterns (BP) toward the second non-display area (NA2) and are disposed in the second non-display area (NA2). The first upper connection line (UP1) is connected to a portion of the plurality of bending patterns (BP) and to a first portion (UPLLA) of the upper power link line. The second upper connection line (UP2) is connected to another portion of the plurality of bending patterns (BP) and to a second portion (UPLLB) of the upper power link line. Specifically, the first upper connection line (UP1) is connected to the end of the first portion (UPLLA), and the second upper connection line (UP2) is connected to the end of the second portion (UPLLB). However, the first upper connection line (UP1) and the second upper connection line (UP2) may be connected to other locations of the upper power link line depending on the line design, and are not limited thereto.

[0048] A plurality of bending patterns (BP) on the power link line are disposed in the bending area (BA). As described above, the bending area (BA) is an area extending from the first non-display area (NA1) to the second non-display area (NA2), and it is the area that is bent in the bending direction in the final product.

Therefore, the bending pattern (BP) of the power link line may consist of a specific geometric pattern in the bending area (BA) to minimize stress and cracks concentrated on a plurality of link lines. For example, the bending pattern (BP) may be a pattern in which a conductive pattern having at least one of a diamond shape, a rhombus shape, a zigzag shape, or a circular shape is repetitively disposed. However, this is not limited to these examples, and the shape of the bending pattern (BP) may take various forms to minimize the stress and cracks concentrated in the bending pattern (BP).

[0049] The lower power link line delivers the power supply voltage, which has been conveyed via the upper power link line and a plurality of bending patterns (BP), to the first power line (PL1) and the second power line (PL2) of the display area (A/A), respectively.

[0050] The lower power link lines are disposed in the first non-display area (NA1) and include a first lower power link line (PLL1) and a second lower power link line (PLL2). The first lower power link line (PLL1) is disposed in the first non-display area (NA1) and extends to both ends of the first area (A1). The second lower power link line (PLL2) is disposed in the first non-display area (NA1) and extends to the second area (A2), reaching both ends of the second area (A2). Furthermore, the first lower power link line (PLL1) and the second lower power link line (PLL2) are connected at the boundary between the first area (A1) and the second area (A2). In other words, the first lower power link line (PLL1) and the second lower power link line (PLL2) may be a single line.

[0051] Meanwhile, the lower power link lines are connected to a plurality of bending patterns (BP).

Specifically, the first lower power link line (PLL1) and the second lower power link line (PLL2) of the lower power link lines are connected to a plurality of bending patterns (BP). For example, the first lower power link line (PLL1) is connected to the bending patterns (BP) via a first lower connection line (LP1), and the second lower power link line (PLL2) is connected to the bending patterns (BP) via a second lower connection line (LP2). In this case, some of the plurality of bending patterns (BP) are connected to the first lower power link line (PLL1) via the first lower connection line (LP1), and other ones of the plurality of bending patterns (BP) are connected to the second lower power link line (PLL2) via the second lower connection line (LP2).

[0052] The first lower connection line (LP1) and the second lower connection line (LP2) are lines extending from a plurality of bending patterns (BP) toward the first non-display area (NA1) and are disposed in the first non-display area (NA1). The first lower connection line (LP1) is connected to a portion of the plurality of bending patterns (BP) and to the first lower power link line (PLL1). The second lower connection line (LP2) is connected to another portion of the plurality of bending patterns (BP) and to the second lower power link line (PLL2).

[0053] A plurality of first power lines (PL1) are disposed in a first area (A1) of the display area (A/A), and a plurality of second power lines (PL2) are disposed in a second area (A2) of the display area (A/A). Furthermore, the respective ends of the plurality of first power lines (PL1) and second power lines (PL2) extend into the first non-display area (NA1) and are connected to the first lower power link line (PLL1) and the second lower power link line (PLL2). Therefore, a plurality of first power lines (PL1) are connected to a single first lower power link line (PLL1), and a plurality of second power lines (PL2) are connected to a single second lower power link line (PLL2).

[0054] In accordance with the configuration of the power link line described above, the power supply voltage delivered from the drive IC (112) is delivered in the order of the pad connection line (PCL), the first portion of the upper power link line (UPLLA), the first upper connection line (UP1), the bending pattern (BP), the first lower connection line (LP1), the first lower power link line (PLL1), and the first power line (PL1), and supplied to the pixels disposed in the first area (A1). Furthermore, the power supply voltage delivered from the drive IC (112) is delivered in the order of the pad connection line (PCL), the second portion of the upper power link line (UPLLB), the second upper connection line (UP2), the bending pattern (BP), the second lower connection line (LP2), the second lower power link line (PLL2), and the second power line (PL2), and supplied to the pixels disposed in the second area (A2).

[0055] Referring to FIG. 1, the first lower connection line (LP1) may be connected to the midpoint of the first lower power link line (PLL1), and the second lower connection line (LP2) may be connected to the midpoint of the second lower power link line (PLL2). In other words, the first lower connection line (LP1) and the second lower connection line (LP2) may each be connected to the central portion of the first lower power link line (PLL1) and the second lower power link line (PLL2), respectively, rather than to their ends.

[0056] As described above, the first lower power link line (PLL1) extends to both ends of the first area (A1), and the first portion (UPLLA) of the upper power link line may extend to the central portion of the first area (A1). Furthermore, the bending pattern (BP) is connected to the end of the first portion (UPLLA) of the upper power link line, which extends to the central portion of the first area (A1) via the first upper connection line (UP1). Similarly, the second lower power link line (PLL2) extends to both ends of the second area (A2), and the second portion (UPLLB) of the upper power link line may extend to the central portion of the second area (A2). Furthermore, the bending pattern (BP) is connected to the end of the second portion (UPLLB) of the upper power link line, which extends to the central portion of the second area (A2) via the second upper connection line (UP2).

That is, some of the plurality of bending patterns (BP) may be disposed in the central portion of the first area (A1), while other ones of the plurality of bending patterns (BP) may be disposed in the central portion of the second area (A2). Therefore, some of the plurality of bending patterns (BP) may be connected to the central portion of the first lower power link line (PLL1), and other ones of the plurality of bending patterns (BP) may be connected to the central portion of the second lower power link line (PLL2).

[0057] Therefore, a plurality of first power lines (PL1) may include at least two first power lines (PL1) that are equidistant from the first lower connection line (LP1). That is, the first lower connection line (LP1), which is connected to a plurality of bending patterns (BP), is disposed in the central portion of the first area (A1), and since the first lower connection line (LP1) can be connected to the central portion of the first power supply link line (PLL1), a plurality of first power lines (PL1) may include at least two first power lines (PL1) that are equidistant from the first lower connection line (LP1). Furthermore, since the second lower connection line (LP2) can be connected to the central portion of the second power supply link line (PLL2), the plurality of second power lines (PL2) may include at least two second power lines (PL2) that are equidistant from the second lower connection line (LP2). That is, since the second lower connection line (LP2), which is connected to a plurality of bending patterns (BP), is disposed in the central portion of the second area (A2), at least two of the plurality of power lines may be equidistant from the second lower connection line (LP2).

[0058] Here, the fact that the first lower connection line (LP1) and the second lower connection line (LP2) are each connected to the center of the first lower power link line (PLL1) and the center of the second lower power link line (PLL2), respectively, means that the first lower connection line (LP1) and the second lower connection line (LP2) are connected to the exact center of the first lower power link line (PLL1) and the exact center of the second lower power link line (PLL2), respectively. Alternatively, the fact that the first lower connection line (LP1) and the second lower connection line (LP2) are each connected to the center of the first lower power link line (PLL1) and the center of the second lower power link line (PLL2), respectively, means that there are at least two first power lines (PL1) and second power lines (PL2) that are equidistant from the first lower connection line (LP1) and the second lower connection line (LP2) are connected to positions on the first lower power link line (PLL1) and the second lower power link line (PLL2) that are not their ends, such that there are at least two first power lines (PL1) and second power lines (PL2) located at equal distances from the first lower connection line (LP1) and the second lower connection line (LP2), respectively.

[0059] Meanwhile, assuming that the sum of the widths of the first area (A1) and the second area (A2) in the first non-display area (NA1) is L, the first lower-power link line (PLL1) and the second lower-power link line (PLL2)



may each have a length of  $1/2 * L$ . Furthermore, since some of the bending patterns (BP) are connected to the central portion of the first lower power link line (PLL1), the power supply voltage delivered through some of the bending patterns (BP) reaches the midpoint of the first lower power link line (PLL1), that is, a point  $1/4 * L$  from the boundary between the first area (A1) and the second area (A2), or in other words, a point  $1/4 * L$  from the entire first area (A1) and second area (A2), and is delivered to both ends of the first area (A1).

Furthermore, since some of the plurality of bending patterns (BP) are connected to the central portion of the second lower power link line (PLL2), the power supply voltage delivered through some of the plurality of bending patterns (BP) is introduced at the midpoint of the second lower power link line (PLL2), that is, the  $1/4 * L$  point from the boundary between the first area (A1) and the second area (A2), or in other words, the  $3/4 * L$  point from the entire first area (A1) and second area (A2), and is delivered to both ends of the second area (A2).

[0060] Hereinafter, FIG. 2 is referred to in conjunction with the following description to explain the relationship between the data link line and the upper power link line in the second non-display area (NA2).

[0061] FIG. 2 is a cross-sectional view taken along line II-II' in FIG. 1. FIG. 2 is a cross-sectional view of the second non-display area (NA2); more specifically, it is a cross-sectional view of the area containing the first portion (UPLLA) of the upper power link line disposed in the second non-display area (NA2).

[0062] Referring to FIG. 2, the display device (100) includes a substrate (101), a buffer layer (102), a power link line, an insulating layer (103), a data link line (DLL), and a protective layer (104).

[0063] A buffer layer (102) is disposed on the substrate (101). The buffer layer (102) can prevent the penetration of moisture or impurities through the substrate (101). However, the buffer layer (102) is not an essential component and may be selectively provided depending on the type of substrate (101) and the type of thin-film transistors disposed in the display area (A/A).

[0064] A first portion (UPLLA) of the upper power link line of the power link line is disposed on the buffer layer (102). As described above, the first portion (UPLLA) of the upper power link line may be formed from one of various materials used in the fabrication of the gate electrodes, source electrodes, and drain electrodes of the organic light-emitting devices and thin-film transistors in the display area (A/A).

[0065] The insulating layer (103) is an insulating layer for protecting the upper power link line. For example, the insulating layer (103) may be an insulating layer such as a gate insulating layer or an interlayer insulating layer, and may be composed of a single layer or a multilayer of silicon oxide (SiOx) or silicon nitride (SiNx), but is not limited thereto.

[0066] A plurality of data link lines (DLL) are disposed on the insulating layer (103). In this case, only a portion of the plurality of data link lines (DLL) may superimpose with the first portion (UPLLA) of the upper power link line. The data link lines (DLL) are lines for delivering data voltage from the drive IC (112) to a plurality of data lines in the display area (A/A). The data link lines (DLL) are disposed in the non-display area (N/A), while the data lines are disposed in the display area (A/A). Furthermore, the plurality of data link lines (DLL) are connected to the drive IC (112) and the plurality of data lines, respectively. The plurality of data link lines (DLL) and data lines may be formed from one of various materials used in the fabrication of the source electrodes, drain electrodes, and gate electrodes of the organic light-emitting diodes and thin-film transistors in the display area (A/A), and may be configured as a single layer or a multi-layer structure. In FIG. 2, the data link lines (DLL) are shown as being disposed on a first portion (UPLLA) of the upper power link line; however, the data link lines (DLL) may also be disposed beneath the first portion (UPLLA) of the upper power link line.

[0067] A protective layer (104) is disposed on a plurality of data link lines (DLLs). The protective layer (104) is an insulating layer for protecting the data link lines (DLLs). For example, the protective layer (104) may consist of a single or multiple layers of silicon oxide (SiO<sub>x</sub>) or silicon nitride (SiN<sub>x</sub>), but is not limited thereto.

[0068] Although FIG. 2 shows only the protective layer (104) disposed on the data link line (DLL), other structures, such as an organic layer or a planarization layer, may also be disposed thereon.

[0069] The range of applications for display devices is expanding to include monitors, TVs, smartphones, and watches, and research is underway to develop display devices that feature a large display area while reducing their volume and weight. One area of research focuses on reducing the size of the display device's bezel. To achieve this, techniques such as bending the substrate's non-display area and reducing the size of the substrate's non-display area are being employed. Consequently, research is underway on designs aimed at reducing the input area for the power supply voltage and minimizing the number of lines used to deliver the power supply voltage.

[0070] However, there is a problem in which a drop in the power supply voltage occurs due to the resistance of the power link lines when reducing the input area of the power supply voltage and the number of lines delivering the power supply voltage. Specifically, the drop in the power supply voltage causes an uneven power supply voltage to be delivered to a plurality of pixels in the display area. For example, if a power link

line that supplies power in the non-display area is located in the center of the non-display area, and if the power link line extends from the center of the non-display area to both ends in the non-display area adjacent to the display area, the non-display area, the power supply voltage applied through the power line located at the end of the display area may be lower than that applied through the power line located at the center of the display area. In other words, while the power line located at the center of the display area receives the power supply voltage directly from the power link line located at the center of the non-display area, the power line located at the end of the display area receives the power supply voltage via the power link line extending from the center of the non-display area to both ends, which is a longer path; therefore, the power supply voltage applied through the power line located at the end of the display area may be lower than that applied through the power line located at the center of the display area. Consequently, if an uneven power supply voltage is delivered to a plurality of pixels within the display area, luminance imbalance may occur, potentially reducing the reliability of the display device.

[0071] Accordingly, the display device (100) according to an embodiment of the present specification includes power link lines that supply the power supply voltage to a first area (A1) and a second area (A2) of the substrate (101), and can minimize the drop in the power supply voltage by reducing differences in line resistance caused by differences in the lengths of the lines through which the power supply voltage is supplied. Specifically, the power supply voltage from the drive IC (112) disposed in the pad area (PA) is introduced into the center of the second non-display area (NA2). Then, the power supply voltage is supplied to the centers of the first area (A1) and the second area (A2), respectively, via the first portion (UPLLA) and the second portion (UPLLB) of the upper power link line. Consequently, the power supply voltage introduced into the center of the non-display area (N/A) is delivered via a plurality of power lines not to the center of the display area (A/A), but rather, for example, the 1/4 and 3/4 points, rather than the center of the display area (A/A). Consequently, the voltage drop of the power supply voltage can be reduced compared to when it is delivered from the center of the substrate (101) to both ends of the substrate (101). Therefore, in the display device (100) according to an embodiment of this specification, before the power supply voltage introduced from the drive IC (112) to the center of the substrate (101) is delivered to the display area (A/A), by distributing the power supply voltage to multiple points and reducing the path the power supply voltage must travel to reach each power line, thereby minimizing the voltage drop, and thus has the effect of displaying an image with uniform luminance.

[0072] FIG. 3 is a plan view of a display device according to another embodiment of the present specification. FIG. 4 is a cross-sectional view along the IV-IV' line in FIG. 3. FIG. 4 is a cross-sectional view of the second

non-display area (NA2), showing the area containing the first portion (UPLLA) of the upper power supply link disposed in the second non-display area (NA2). The display device (300) shown in FIG. 3 and FIG. 4 differs from the display device (100) shown in FIG. 1 and FIG. 2 in that the first portion (UPLLA) and second portion (UPLLB) of the upper power link line are different; since the other configurations are substantially the same, a detailed description is omitted.

[0073] Referring to FIG. 3, the upper power link line includes a first portion (UPLLA) extending to the first area (A1) and a second portion (UPLLB) extending to the second area (A2). Furthermore, the first portion (UPLLA) and the second portion (UPLLB) of the upper power link line each extend from the center of the second non-display area (NA2) to the ends of the first area (A1) and the second area (A2), respectively. Accordingly, the first upper connection line (UP1) and the second upper connection line (UP2) may each extend from the central portion, rather than the ends, of the first portion (UPLLA) and the second portion (UPLLB) of the upper power link line.

[0074] Furthermore, similar to the first portion (UPLLA) of the upper power link line, the first lower power link line (PLL1) also extends to both ends of the first area (A1), and similar to the second portion (UPLLB) of the upper power link line, the second lower power link line (PLL2) also extends to both ends of the second area (A2).

[0075] Referring to FIG. 4, a first portion (UPLLA) of the upper power link line is disposed on the buffer layer (102). In this case, the first portion (UPLLA) of the upper power link line extends to the end of the first area (A1), and the first portion (UPLLA) of the upper power link line is disposed throughout the entire first area (A1). Furthermore, the second portion (UPLLB) of the upper power link line and the second lower power link line (PLL2) are disposed throughout the second area (A2), while the first lower power link line (PLL1) is disposed throughout the first area (A1).

[0076] An insulating layer (103) and a data link line (DLL) are disposed on the first portion (UPLLA) of the upper power link line. Furthermore, the first portion (UPLLA) of the upper power link line is disposed so as to superimpose with all of the data link lines (DLL).

[0077] In a display device (300) according to another embodiment of this specification, the first portion (UPLLA) and the second portion (UPLLB) of the upper power link line each extend from the center of the second non-display area (NA2) to the ends of the first area (A1) and the second area (A2), respectively, thereby minimizing deviations caused by the RC load on the data voltage. Furthermore, in the first non-display area (NA1), the first lower power link line (PLL1) and the second lower power link line (PLL2) each

extend from both ends of the first area (A1) to both ends of the second area (A2), thereby minimizing deviations caused by the RC load on the data voltage. As described above, when the data link line (DLL) superimposes with the upper power link line and the lower power link line, parasitic capacitance may occur between the data link line (DLL) and the upper and lower power link lines, which may result in an RC load on the data voltage delivered through the data link line (DLL). However, if the upper power link line and the lower power link line superimpose with only some of a plurality of data link lines (DLLs), different RC loads may occur for the respective data voltages delivered to the data link lines (DLLs) that superimpose with the upper power link line and the lower power link line, and to those that do not superimpose, resulting in RC load deviations depending on the data link lines (DLL). Accordingly, in the display device (300) according to another embodiment of this specification, the first portion (UPLLA) and the second portion (UPLLB) of the upper power link line each extend from the center of the second non-display area (NA2) to the end of the first area (A1) and the end of the second area (A2), such that the first portion (UPLLA) of the upper power link line superimposes with all data link lines (DLLs) disposed in the first area (A1), and the second portion (UPLLB) of the upper power link line superimposes with all data link lines (DLLs) disposed in the second area (A2). Furthermore, the first lower power link line (PLL1) and the second lower power link line (PLL2) of the lower power link lines each extend from the first non-display area (NA1) to both ends of the first area (A1) and the second area (A2), such that the first lower power link line (PLL1) superimposes with all data link lines (DLL) disposed in the first area (A1), and the second lower power link line (PLL2) may superimpose with all data link lines (DLLs) disposed in the second area (A2). Therefore, in the display device (300) according to another embodiment of this specification, deviations in the RC load delivered through the data link lines (DLLs) can be reduced, ensuring that the delay in the data voltage occurs identically across all data link lines (DLLs), thereby minimizing deviations caused by the delay in the data voltage.

[0078] FIG. 5 is a plan view of a display device according to another embodiment of the present specification. The display device (500) shown in FIG. 5 differs from the display device (300) shown in FIG. 3 and FIG. 4 in that it further includes a third area (A3), a third upper connection line (UP3), a third lower connection line (LP3), a third lower power link line (PLL3), and a third power line (PL3), whereas other configurations are substantially the same; therefore, a detailed description of those components is omitted.

[0079] Referring to FIG. 5, the substrate (501) of the display device (500) includes a first area (A1), a second area (A2), and a third area (A3). The first area (A1), the second area (A2), and the third area (A3) can be defined by dividing the substrate (501) in the vertical direction. For example, when the substrate (501) is divided into three equal parts in the vertical direction, the first area (A1) is the left area of the substrate (501) and includes the display area (A/A) and a portion of the non-display area (N/A). The second area (A2) is the right area of the substrate (501) and includes another portion of the display area (A/A) and the non-display area (N/A). The third area (A3) is the central area of the substrate (501) and includes yet another portion of the display area (A/A) and the non-display area (N/A).

[0080] The upper power link line comprises a first portion (UPLLA) extending from a portion of the third area (A3) to the first area (A1), and a second portion (UPLLB) extending from another portion of the third area (A3) to the second area (A2). Furthermore, the first portion (UPLLA) and the second portion (UPLLB) each extend from the central portion of the third area (A3) to the end of the first area (A1) and the end of the second area (A2), respectively.

[0081] A plurality of upper connection lines are disposed in the second non-display area (NA2) and connect the first portion (UPLLA) and the second portion (UPLLB) of the upper power link line to a plurality of bending patterns (BP) disposed in the bending area (BA). The plurality of upper connection lines includes a first upper connection line (UP1), a second upper connection line (UP2), and a third upper connection line (UP3). The first upper connection line (UP1) is a line extending from the first portion (UPLLA) disposed in the first area (A1) toward the bending area (BA). The second upper connection line (UP2) is a line extending from a second portion (UPLLB) disposed in a second area (A2) toward the bending area (BA). The third upper connection line (UP3) is a line extending from the first portion (UPLLA) and the second portion (UPLLB) disposed in a third area (A3) toward the bending area (BA).

[0082] Each of a plurality of bending patterns (BP) is connected to a plurality of upper connection lines and is disposed in a bending area (BA). Specifically, some of the plurality of bending patterns (BP) are connected to a first upper connection line (UP1) extending from a first portion (UPLLA) of a first area (A1), while other ones of the plurality of bending patterns (BP) are connected to a second upper connection line (UP2) extending from a second portion (UPLLB) of a second area (A2), and yet another portion of the plurality of bending patterns (BP) is connected to a third upper connection line (UP3) extending from a first portion (UPLLA) and a second portion (UPLLB) of a third area (A3). In other words, within the bending area (BA), some of the plurality of bending patterns (BP) are disposed in the first area (A1), others are disposed in the second area (A2), and still others are disposed in the third area (A3).

[0083] A plurality of lower connection lines are connected to each of a plurality of bending patterns (BP) and are disposed in a first non-display area (NA1). Specifically, the plurality of lower connection lines includes a first lower connection line (LP1), a second lower connection line (LP2), and a third lower connection line (LP3). In the first non-display area (NA1), the first lower connection line (LP1) is disposed in the first area (A1), the second lower connection line (LP2) is disposed in the second area (A2), and the third lower connection line (LP3) is disposed in the third area (A3). Accordingly, the first lower connection line (LP1) is connected to a plurality of bending patterns (BP) disposed in the first area (A1), the second lower connection line (LP2) is connected to a plurality of bending patterns (BP) disposed in the second area (A2), and the third lower connection line (LP3) is connected to a plurality of bending patterns (BP) disposed in the third area (A3).

[0084] The first lower power link line (PLL1), the second lower power link line (PLL2), and the third lower power link line (PLL3) are each connected to the first lower connection line (LP1), the second lower connection line (LP2), and the third lower connection line (LP3), respectively. Specifically, the first lower power link line (PLL1) is connected to the first lower connection line (LP1), the second lower power link line (PLL2) is connected to the second lower connection line (LP2), and the third lower power link line (PLL3) is connected to the third lower connection line (LP3). That is, in the first non-display area (NA1), the first lower power link line (PLL1) is disposed in the first area (A1), the second lower power link line (PLL2) is disposed in the second area (A2), and the third lower power link line (PLL3) is disposed in the third area (A3). In this case, the first lower power link line (PLL1), the second lower power link line (PLL2), and the third lower power link line (PLL3) may each extend to both ends of the first area (A1), the second area (A2), and the third area (A3), respectively. Furthermore, the first lower power link line (PLL1), the second lower power link line (PLL2), and the third lower power link line (PLL3), which extend to both ends of the first area (A1), the second area (A2), and the third area (A3), respectively, may be connected to each other at the boundaries of each area. In other words, the first lower power link line (PLL1), the second lower power link line (PLL2), and the third lower power link line (PLL3) may be connected as a single line.

[0085] A plurality of power lines are disposed in the display area (A/A) and are connected to a first lower power link line (PLL1), a second lower power link line (PLL2), and a third lower power link line (PLL3). A plurality of power lines includes a first power line (PL1), a second power line (PL2), and a third power line (PL3). A plurality of first power lines (PL1) are disposed in a first area (A1) and connected to a first lower power supply link line (PLL1), a plurality of second power lines (PL2) are disposed in a second area (A2) and connected to a second lower power supply link line (PLL2), and a plurality of third power lines (PL3) are disposed in a third area (A3), and connected to a third lower power link line (PLL3).

[0086] In accordance with the configuration of the power link line described above, the power supply voltage delivered from the drive IC (112) is delivered in the order of the pad connection line (PCL), the first portion of the upper power link line (UPLLA), the first upper connection line (UP1), the bending pattern (BP), the first lower connection line (LP1), the first lower power link line (PLL1), and the first power line (PL1), and supplied to the pixels disposed in the first area (A1). Furthermore, the power supply voltage delivered from the drive IC (112) is delivered in the order of the pad connection line (PCL), the second portion of the upper power link line (UPLLB), the second upper connection line (UP2), the bending pattern (BP), the second lower connection line (LP2), the second lower power link line (PLL2), and the second power line (PL2), and supplied to the pixels disposed in the second area (A2). Finally, the power supply voltage delivered from the drive IC (112) is delivered in the order of the pad connection line (PCL), the first portion (UPLLA) and the second portion (UPLLB) of the upper power link line, the third upper connection line (UP3), the bending pattern (BP), the third lower connection line (LP3), the third lower power link line (PLL3), and the third power line (PL3), and supplied to the pixels disposed in the third area (A3).

[0087] A display device (500) according to another embodiment of the present specification divides a substrate (501) into a first area (A1), a second area (A2), and a third area (A3), and disposes corresponding power link lines and power lines to supply power supply voltage to the pixels in each area, but is not limited thereto. In this case, the substrate (501) may be divided into three or more areas to supply the power supply voltage. However, in the bending area (BA), the height of the neutral plane is designed to reduce the stress delivered to each line during bending. To facilitate the design of the neutral plane, a plurality of bending patterns (BP) and a plurality of data link lines may be disposed on the same layer. In this case, if the number of bending patterns (BP) disposed on the substrate (501) increases, the space available for disposing data link lines decreases. However, as the resolution of the display device increases, the number of data lines increases, and the number of data link lines connected to those data lines also increases. Therefore, in the case of a high-resolution display device, sufficient space is required for the data link lines, so the area on the bending area (BA) where bending patterns (BP) can be disposed may be limited. In this case, the number of areas on the substrate (501) and the corresponding design of the power link lines can be determined based on the resolution of the display device, the width of the bending area (BA), and the width of the data link lines. Accordingly, depending on the embodiment, the number of areas on the substrate (501) may be three or more.

[0088] Meanwhile, assuming that the sum of the widths of the first area (A1), the second area (A2), and the

third area (A3) in the first non-display area (NA1) is L, the first lower power link line (PLL1), the second lower power link line (PLL2), and the third lower power link line (PLL3) may each have a length of  $\frac{1}{3} * L$ . Furthermore, since some of the bending patterns (BP) are connected to the central portion of the first lower power link line (PLL1), the power supply voltage delivered through some of the bending patterns (BP) is delivered to the midpoint of the first lower power link line (PLL1), that is,  $\frac{1}{6} * L$  from the boundary between the first area (A1) and the third area (A3), and is delivered to both ends of the first area (A1). Furthermore, since another portion of the plurality of bending patterns (BP) is connected to the center of the second lower power link line (PLL2), the power supply voltage delivered through this portion enters at the midpoint of the second lower power link line (PLL2), that is, at the  $\frac{1}{6} * L$  point from the boundary between the second area (A2) and the third area (A3), and is delivered to both ends of the second area (A2). Finally, since another portion of the plurality of bending patterns (BP) is connected to the center of the third lower power link line (PLL3), the power supply voltage delivered through yet another portion of the plurality of bending patterns (BP) enters at the midpoint of the third lower power link line (PLL3), that is, at the  $\frac{1}{6} * L$  point from the boundary between the third area (A3) and the first area (A1), and is delivered to both ends of the third area (A3).

[0089] Accordingly, the display device (500) according to another embodiment of this specification includes a power link line that distributes the power supply voltage to a first area (A1), a second area (A2), and a third area (A3) of the substrate (501), and can minimize the drop in the power supply voltage by reducing differences in line resistance caused by differences in the length of the lines through which the power supply voltage is delivered. The power supply voltage introduced into the central portion of the second non-display area (NA2) is supplied via a plurality of power lines at points such as  $\frac{1}{6}$ ,  $\frac{1}{2}$ , and  $\frac{5}{6}$  points of the display area (A/A), thereby reducing the voltage drop compared to when the power supply voltage is delivered from the center of the substrate (501) to both ends of the substrate (501).

[0090] Therefore, in a display device (500) according to another embodiment of this specification, by distributing the power supply voltage input points to multiple locations, thereby shortening the path the power supply voltage must travel to reach each power line, which minimizes the voltage drop of the power supply voltage, resulting in the ability to display an image with uniform luminance.

[0091] FIG. 6 is a plan view of a display device according to another embodiment of the present specification. The display device (600) shown in FIG. 6 differs from the display device (100) shown in FIG. 1 and FIG. 2 in

the arrangement of the pad connection lines and the first portion (UPLLA) and second portion (UPLLB) of the upper power link line; since the other configurations are substantially the same, a detailed description is omitted.

[0092] Referring to FIG. 6, the drive IC (112) disposed on the flexible film (110) delivers a power supply voltage to the power link line via a first pad (P1) and a second pad (P2). The first pad (P1) and the second pad (P2) may be pads that output the power supply voltage. The flexible film (110) includes a plurality of pads that output a power supply voltage, data voltage, and the like, and among them, the first pad (P1) and the second pad (P2) may be pads disposed at the outermost positions among the plurality of pads disposed on the flexible film (110). However, in FIG. 6, for the sake of simplicity, only the first pad (P1) and the second pad (P2), from which the power supply voltage from the drive IC (112) is output, are shown among the plurality of pads.

[0093] The pad connection lines include a first pad connection line (PCL1) disposed in the first area (A1) within the second non-display area (NA2) and a second pad connection line (PCL2) disposed in the second area (A2). Furthermore, the first pad connection line (PCL1) extends from the first pad (P1) in the pad area (PA) to the second non-display area (NA2) from the end of the area corresponding to the first area (A1), and the second pad connection line (PCL2) extends from the second pad (P2) of the pad area (PA) to the second non-display area (NA2) via the end of the area corresponding to the second area (A2). That is, the first pad connection line (PCL1) and the second pad connection line (PCL2) are each connected to the first pad (P1) and the second pad (P2), which are disposed at the outermost positions among a plurality of pads on the flexible film (110), and are disposed at both ends of the pad area (PA).

[0094] Furthermore, although FIG. 6 shows two pad connection lines—a first pad connection line (PCL1) and a second pad connection line (PCL2)—the number of pad connection lines may be greater, or their positions may vary, depending on the arrangement of the pads from which the power supply voltage from the driver IC is output, and the present invention is not limited thereto.

[0095] The upper power link line includes a first portion (UPLLA) disposed in the first area (A1) and a second portion (UPLLB) disposed in the second non-display area (NA2). Specifically, the upper power link line includes a first portion (UPLLA) extending from one end of the second non-display area (NA2) to the first area (A1), and a second portion (UPLLB) extending from the other end of the second non-display area (NA2) to the second area (A2). In this case, the first portion (UPLLA) extends from one end of the second non-display area (NA2) to the central portion of the first area (A1), and the second portion (UPLLB) may extend from the other end of the second non-display area (NA2) to the central portion of the second area (A2).

[0096] The upper power link line is connected to the pad connection line. Specifically, at one end of the second non-display area (NA2), the first portion (UPLLA) of the upper power link line is connected to the first pad connection line (PCL1). At the other end of the second non-display area (NA2), the second portion (UPLLB) of the upper power link line is connected to the second pad connection line (PCL2).

[0097] The upper power link line is connected to a plurality of bending patterns (BP). Specifically, a first portion (UPLLA) of the upper power link line is connected to the bending patterns (BP) via a first upper connection line (UP1), and a second portion (UPLLB) of the upper power link line is connected to the bending patterns (BP) via a second upper connection line (UP2). That is, the end of the first portion (UPLLA) of the upper power link line is connected to the first upper connection line (UP1) at the center of the first area (A1), and the end of the second portion (UPLLB) of the upper power link line is connected to the second upper connection line (UP2) at the center of the second area (A2).

[0098] In the display device (600) according to another embodiment of this specification, the power supply voltage is supplied from the drive IC (112) disposed in the pad area (PA) to both ends of the non-display area (N/A), respectively. The power supply voltage output point of the drive IC (112) in the display device (600) may vary depending on the model and design of the drive IC (112). Even if the arrangement of the pad connection lines changes as the power supply voltage output point of the drive IC (112) changes, the first portion (UPLLA) and second portion (UPLLB) of the upper power link line connected to the first pad connection line (PCL1) and the second pad connection line (PCL2), respectively, can be extended to the central portions of the first area (A1) and the second area (A2). Therefore, the display device (600) according to another embodiment of this specification can distribute the power supply voltage to multiple points before it is delivered from the drive IC (112) to the display area (A/A), regardless of changes in the power supply voltage input points due to the model or design of the drive IC (112). Consequently, by reducing the path length that the power supply voltage must travel before being delivered to each power line, the voltage drop is minimized, resulting in the ability to display images with uniform brightness. Therefore, since the placement of the power link lines can be freely determined based on the type and design of the drive IC (112), design flexibility is enhanced.

[0099] Furthermore, by dividing the power supply voltage and supplying it to the first pad connection line (PCL1) and the second pad connection line (PCL2), which are disposed at both ends of the second non-display area (NA2), heat generation caused by excessive current and deformation of the display device (600) can be mitigated, thereby reducing performance degradation of the display device (600).

[0100] FIG. 7 is a plan view of a display device according to another embodiment of the present specification. The display device (700) shown in FIG. 7 differs from the display device (600) shown in FIG. 6 in that the first portion (UPLLA) and second portion (UPLLB) of the upper power link line are different; since the other configurations are substantially the same, a detailed description is omitted.

[0101] Referring to FIG. 7, a first portion (UPLLA) of the upper power link line is disposed in the first area (A1) within the second non-display area (NA2), and a second portion (UPLLB) of the upper power link line is disposed in the second area (A2). In this case, the first portion (UPLLA) of the upper power link line extends from one end of the second non-display area (NA2) to the boundary between the first area (A1) and the second area (A2), and the second portion (UPLLB) of the upper power link line extends from the other end of the second non-display area (NA2) to the boundary between the first area (A1) and the second area (A2), such that the first portion (UPLLA) and the second portion (UPLLB) of the upper power link line are connected to each other. Accordingly, the first upper connection line (UP1) and the second upper connection line (UP2) may extend from the central portions of the first portion (UPLLA) and the second portion (UPLLB) of the upper power link line. That is, the first portion (UPLLA) and the second portion (UPLLB) are disposed across the entire second non-display area (NA2).

[0102] Furthermore, in the first non-display area (NA1), the first lower power link line (PLL1) extends to both ends of the first area (A1), and the second lower power link line (PLL2) extends to both ends of the second area (A2). That is, just as with the first portion (UPLLA) and the second portion (UPLLB) in the second non-display area (NA2), the first lower power link line (PLL1) and the second lower power link line (PLL2) are also disposed throughout the first non-display area (NA1).

[0103] In a display device (700) according to another embodiment of this specification, the first portion (UPLLA) and the second portion (UPLLB) of the upper power link line each extend from both ends of the second non-display area (NA2) to the boundary between the first area (A1) and the second area (A2), thereby minimizing deviations caused by the RC load for the data voltage. Specifically, the first portion (UPLLA) of the upper power link line extends from one end of the second non-display area (NA2) to the boundary between the first area (A1) and the second area (A2), allowing it to superimpose with all data link lines disposed in the first area (A1). Furthermore, the second portion (UPLLB) of the upper power link line extends from the other end of the second non-display area (NA2) to the boundary between the first area (A1) and the second area (A2), allowing it to superimpose with all data link lines disposed in the second area (A2).

Furthermore, the first lower power link line (PLL1) and the second lower power link line (PLL2) are also disposed throughout the first non-display area (NA1), allowing them to superimpose with all data link lines disposed in the first non-display area (NA1). Therefore, in the display device (700) according to another embodiment of this specification, deviations in the RC load delivered through the data link lines can be reduced, ensuring that the delay in the data voltage occurs uniformly across all data link lines, thereby minimizing deviations caused by the delay in the data voltage.

[0104] FIG. 8 is a plan view of a display device according to another embodiment of the present specification. The display device (800) shown in FIG. 8 differs from the display device (600) shown in FIG. 6 in the arrangement of the first portion (UPLLA) and second portion (UPLLB) of the upper power link line and the bending pattern (BP); since the other configurations are substantially the same, a detailed description is omitted.

[0105] Referring to FIG. 8, a first pad connection line (PCL1) and a second pad connection line (PCL2) are disposed at both ends of the second non-display area (NA2), respectively. Furthermore, within the second non-display area (NA2), the first portion (UPLLA) of the upper power link line is disposed in the first area (A1), and the second portion (UPLLB) of the upper power link line is disposed in the second area (A2). In this case, the first portion (UPLLA) of the upper power link line is connected in the same line as the first pad connection line (PCL1), and the second portion (UPLLB) is connected in the same line as the second pad connection line (PCL2).

[0106] In other words, the first portion (UPLLA) and the second portion (UPLLB) may also be disposed at one end of the first area (A1)—which is one end of the second non-display area (NA2)—and at one end of the second area (A2), respectively, in the same manner as the first pad connection line (PCL1) and the second pad connection line (PCL2).

[0107] The upper power link line is connected to a plurality of bending patterns (BP). Specifically, a first portion (UPLLA) of the upper power link line is connected to the bending patterns (BP) via a first upper connection line (UP1), and a second portion (UPLLB) of the upper power link line is connected to the bending patterns (BP) via a second upper connection line (UP2). For example, a first pad connection line (PCL1) disposed at one end (A1) of a first area (A1), the bending pattern (BP) is connected to the first portion (UPLLA) and the first upper connection line (UP1), and the bending pattern (BP) is connected to the second pad connection line (PCL2), the second portion (UPLLB), and the second upper connection line (UP2) disposed at one end of the second area (A2). Therefore, a plurality of bending patterns (BP) connected to the first upper connection line (UP1) and the second upper connection line (UP2) can also be disposed at both ends of the non-display area (N/A), that is, at both ends of the bending area (BA).

[0108] In another embodiment of the present specification, the display device (800) supplies power supply

voltage from the drive IC (112) disposed in the pad area (PA) to both ends of the non-display area (N/A). Furthermore, the power link line, which delivers the power supply voltage, can be arranged in a straight line to minimize the length of the line. Specifically, the first pad connection line (PCL1) and the second pad connection line (PCL2) are each disposed at both ends of the second non-display area (NA2). Furthermore, the first portion (UPLLA) of the upper power link line, the first upper connection line (UP1), and the bending pattern (BP) are connected in a straight line to the first pad connection line (PCL1). Furthermore, the second portion (UPLLB) of the upper power link line, the second upper connection line (UP2), and the bending pattern (BP) are connected in a straight line to the second pad connection line (PCL2). Therefore, the display device (800) according to another embodiment of this specification has the effect of displaying an image with uniform brightness by minimizing the drop in the power supply voltage, as it reduces the path through which the power supply voltage travels before it is delivered from the drive IC (112) to the display area (A/A).

[0109] FIG. 9 is a plan view of a display device according to another embodiment of the present specification. The display device (900) shown in FIG. 9 differs from the display device (100) shown in FIG. 1 and FIG. 2 in that the first portion (UPLLA) and second portion (UPLLB) of the upper power link line are different; since the other configurations are substantially the same, a detailed description is omitted.

[0110] Referring to FIG. 9, the upper power link line includes a first portion (UPLLA) extending to a first area (A1) and a second portion (UPLLB) extending to a second area (A2). The first portion (UPLLA) and the second portion (UPLLB) of the upper power link line are connected to pad connection lines (PCL).

Furthermore, the first portion (UPLLA) and the second portion (UPLLB) of the upper power link line each extend from the second non-display area (NA2) to the central portions of the first area (A1) and the second area (A2), respectively.

[0111] The upper power link line is connected to a plurality of bending patterns (BP). Specifically, a first portion (UPLLA) of the upper power link line is connected to the bending patterns (BP) via a first upper connection line (UP1), and a second portion (UPLLB) is connected to the bending patterns (BP) via a second upper connection line (UP2). In this case, some of the plurality of bending patterns (BP) are connected to the first portion (UPLLA) of the upper power link line via the first upper connection line (UP1), and other ones of the plurality of bending patterns (BP) are connected to the second portion (UPLLB) of the upper power link line via the second upper connection line (UP2).

[0112] The first portion (UPLLA) and the second portion (UPLLB) may each be connected via the shortest path between the first upper connection line (UP1) and the second upper connection line (UP2) and the pad connection line (PCL). That is, the first portion (UPLLA) and the second portion (UPLLB) may each be disposed diagonally in the second non-display area.

[0113] In the display device (900) according to another embodiment of this specification, the power supply voltage is supplied from the drive IC (112) disposed in the pad area (PA) to both ends of the non-display area (N/A), respectively. The power supply voltage output point of the drive IC (112) in the display device (600) may vary depending on the model and design of the drive IC (112). Even if the arrangement of the pad connection lines changes as the power supply voltage output point of the drive IC (112) changes, the first portion (UPLLA) and second portion (UPLLB) of the upper power link line connected to the first pad connection line (PCL1) and the second pad connection line (PCL2), respectively, can be extended to the central portions of the first area (A1) and the second area (A2). A plurality of bending patterns (BP) disposed in the central portions of the first area (A1) and the second area (A2) are connected to the first portion (UPLLA) and the second portion (UPLLB), respectively, which have been extended to the central portions of the first area (A1) and the second area (A2). In this case, the first portion (UPLLA) and the second portion (UPLLB) can connect the pad connection line (PCL) disposed at the center of the non-display area (N/A)—that is, at the boundary between the first area (A1) and the second area (A2)—to the plurality of bending patterns (BP) via the shortest distance. Therefore, the length of the power link lines that deliver the power supply voltage delivered to the center of the non-display area (N/A) to the centers of the first area (A1) and the second area (A2), respectively, can be minimized. Consequently, as the length of the power link lines is reduced, the resistance of the power link lines can be decreased, and the voltage drop of the power supply voltage can also be reduced. Consequently, the display device (900) according to an embodiment of the present specification distributes the power supply voltage introduced from the drive IC (112) to the center of the substrate (101) to multiple points before it is delivered to the display area (A/A). At the same time, by minimizing the path through which the power supply voltage is delivered, the voltage drop of the power supply voltage is minimized, thereby enabling the display of an image with uniform luminance.

[0114] The display device according to various embodiments of this specification can be described as follows.

[0115] A display device according to an embodiment of the present specification comprises a substrate including a display area provided with a plurality of pixels and a non-display area adjacent to the display area; a plurality of power lines provided in the display area to supply power to the plurality of pixels, comprising a plurality of first power lines and a plurality of second power lines; a lower power link line provided in the non-display area and connected to the plurality of power lines, a power link line extending from the lower power link line and comprising a first lower connection line and a second lower connection line, wherein the plurality of first power lines includes at least two first power lines equidistant from the first lower connection line, and the plurality of second power lines includes at least two second power lines equidistant from the

second lower connection line.

[0116] According to another feature of the present specification, the non-display area comprises a first non-display area in which a lower power link line is disposed, a bending area adjacent to the first non-display area, a second non-display area adjacent to the bending area, and a pad area adjacent to the second non-display area; the substrate includes a first area in which a plurality of first power lines and a first lower connection line are disposed, and a second area in which a plurality of second power lines and a second lower connection line are disposed; the lower power link lines include a first lower power link line extending to the first area and a second lower power link line extending to the second area; and each of the first lower connection line and the second lower connection line may extend from the first lower power link line and the second lower power link line, respectively, toward the bending area.

[0117] According to another feature of the present specification, one of the first area and the second area may be the left area, and the other may be the right area.

[0118] According to another feature of the present specification, the first lower power link line extends to both ends of the first area, and the second lower power link line extends to both ends of the second area, and the first lower power link line and the second lower power link line may be connected at the boundary between the first area and the second area.

[0119] According to another feature of the present specification, the power link line may further include a plurality of bending patterns provided in the bending area and connected to the first lower connection line and the second lower connection line, an upper power link line provided in the second non-display area, and an upper connection line provided in the second non-display area to connect the bending patterns to the upper power link line.

[0120] According to another feature of the present specification, the upper power link line may include a first portion extending to the first area and a second portion extending to the second area.

[0121] According to another feature of the present specification, the first portion and the second portion of the upper power link line may each extend to the central portion of the first area and the central portion of the second area, respectively.

[0122] According to another feature of the present specification, some of the plurality of bending patterns may extend from the end of the first portion of the upper power link line to the first lower connection line, and other ones of the plurality of bending patterns may extend from the end of the second portion of the upper power link line to the second lower connection line.

[0123] According to another feature of the present specification, the first portion and the second portion of the upper power link line may each extend to the end of the first area and the end of the second area, respectively.

[0124] According to another feature of the present specification, the device comprises a display area, a plurality of data lines supplied to the display area to supply data signals to a plurality of pixels, and a non-display area and connected to the plurality of data lines, wherein a first portion of the upper power link line superimposes with all of the data link lines disposed in a first area among the plurality of data link lines, and a second portion of the upper power link line may superimpose with all of the data link lines disposed in a second area among the plurality of data link lines.

[0125] According to another feature of the present specification, the first lower-power link line may superimpose with all of the data link lines disposed in a first area among the plurality of data link lines, and the second lower-power link line may superimpose with all of the data link lines disposed in a second area among the plurality of data link lines.

[0126] According to another feature of the present specification, the plurality of power lines further includes a plurality of third power lines disposed in the display area to supply power to a plurality of pixels, and the power link lines further include third lower power link lines disposed in the non-display area and connected to the plurality of third power lines, the substrate may further include a third area in which a plurality of third power lines and third lower power link lines are disposed between the first area and the second area.

[0127] According to another feature of the present specification, the power link line may further include a pad connection line that connects the central portion of the upper power link line or both ends of the upper power link line to a pad in the pad area.

[0128] According to another feature of the present specification, the pad connection line may include a first pad connection line and a second pad connection line, each disposed at both ends of the second non-display area in the pad area.

[0129] According to another feature of the present specification, the upper power link line may include a first upper power link line, which is disposed at one end of the second non-display area and includes a first portion extending to the first area, and a second upper power link line, which is disposed at the other end of the second non-display area and includes a second portion extending to the second area.

[0130] According to another feature of the present specification, the bending pattern may be a pattern in which a conductive pattern having at least one of a diamond shape, a rhombus shape, a zigzag shape, or a circular shape is repetitively disposed.

[0131] A display device according to another embodiment of the present specification comprises a substrate including a display area provided with a plurality of pixels and a non-display area adjacent to the display area; a power line disposed in the display area to supply power to the plurality of pixels, comprising a plurality of first power lines and a plurality of second power lines; and a power link line comprising a first lower power link line connected to the plurality of first power lines and a second lower power link line connected to the plurality of second power lines, disposed in the non-display area and connected to the first lower power link lines and second lower power link lines, respectively; each of the first lower power link lines and the second lower power link lines is disposed within the left and right areas of the substrate, respectively, to minimize the voltage drop in the power lines and the power link lines.

[0132] According to another feature of the present specification, the non-display area extends from the display area and includes a first non-display area in which the first lower power link line and the second lower power link line are disposed, a bending area extending from the first non-display area, a second non-display area extending from the bending area, and a pad area extending from the second non-display area, the first lower power link line extends from the first non-display area to both ends of the left-side area, the second lower power link line extends from the first non-display area to both ends of the right-side area, and the first lower power link line and the second lower power link line may be connected at the boundary between the left-side area and the right-side area.

[0133] According to another feature of the present specification, the power link line further includes a first lower connection line extending from the first lower power link line to the bending area and a second lower connection line extending from the second lower power link line to the bending area, wherein a plurality of first power lines may be disposed symmetrically with respect to the first lower connection line, and a plurality of second power lines may be disposed symmetrically with respect to the second lower connection line.

[0134] According to another feature of the present specification, the display further comprises a plurality of data lines provided in the display area and supplying data signals to a plurality of pixels, and a plurality of data link lines provided in the non-display area and connected to the plurality of data lines; the power link lines are disposed in the bending area, a plurality of bending patterns connected to a first lower power link line and a second lower power link line, and provided in a second non-display area, and further includes an upper power link line comprising a first portion electrically connected to the first lower power link line and a second portion electrically connected to the second lower power link line, wherein the first and second portions may be superimposed on a plurality of data link lines to minimize deviations caused by the RC load of the data link lines.



[0135] According to another feature of the present specification, the first lower-power link line and the second lower-power link line may be superimposed on a plurality of data link lines to minimize deviations caused by the RC loads of the data link lines.

[0136] Although embodiments of the present invention have been described in greater detail with reference to the accompanying drawings, the present invention is not necessarily limited to these embodiments and may be variously modified within the scope of the technical concept of the present invention. Therefore, the embodiments disclosed in the present invention are intended to illustrate, not to limit, the technical concept of the present invention, and the scope of the technical concept of the present invention is not limited by these embodiments. Consequently, the embodiments described above must be understood as illustrative in all respects and not as limiting. The scope of protection of the present invention should be interpreted in accordance with the appended claims, and all technical concepts falling within the scope of the claims should be interpreted as falling within the scope of the present invention.

**[Description of Reference Numerals/Codes]**

[0137]

100: display device

101, 501: substrate

102: buffer layer

103: insulation layer

104: protective layer

110: flexible film

111: base film

112: drive IC

A/A: display area

N/A: non-display area

NA1: first non-display area

BA: bending area

NA2: second non-display area

PA: pad area

A1: First area



A2: second area

A3: third area

DLL: data link line

PL1: first power line

PL2: second power line

PL3: third power line

PLL1: first lower power link line

PLL2: second lower power link line

PLL3: third lower power link line

LP1: first lower connection line

LP2: second lower connection line

LP3: third lower connection line

BP: bending pattern

UP1: first upper connection line

UP2: second upper connection line

UP3: third upper connection line

UPLLA: first part of the upper power link line

UPLLB: second part of the upper power link line

PCL: pad connection line

PCL1: first pad connection line

PCL2: second pad connection line



**[What is claimed is]**

**[Claim 1]**

A display device comprising: a substrate comprising a display area equipped with a plurality of pixels and a non-display area adjacent to the display area; and a plurality of power lines provided in the display area to supply power to the plurality of pixels, comprising a plurality of first power lines and a plurality of second power lines; a power link line comprising a lower power link line provided in the non-display area and connected to the plurality of power lines, a first lower connection line extending from the lower power link line, and a second lower connection line; wherein the plurality of first power lines includes at least two first power lines equidistant from the first lower connection line; wherein the plurality of second power lines comprises at least two second power lines equidistant from the second lower connection line.

**[Claim 2]**

The display device of claim 1, wherein the non-display area comprises: a first non-display area in which the lower power link line is disposed; a bending area adjacent to the first non-display area; a second non-display area adjacent to the bending area; and a pad area adjacent to the second non-display area; wherein the substrate comprises a first area in which the plurality of first power lines and the first lower connection lines are disposed, and a second area in which the plurality of second power lines and the second lower connection lines are disposed; wherein the lower power link lines include a first lower power link line extending to the first area and a second lower power link line extending to the second area; wherein each of the first lower connection line and the second lower connection line extends from the first lower power link line and the second lower power link line, respectively, toward the bending area side.



**[Claim 3]**

The display device of claim 2, wherein one of the first area and the second area is a left area and the other is a right area.

**[Claim 4]**

The display device of claim 2, wherein the first lower power link line extends to both ends of the first area, the second lower power link line extends to both ends of the second area, and the first lower power link line and the second lower power link line are connected at the boundary between the first area and the second area.

**[Claim 5]**

The display device of claim 2, wherein the power link line comprises: a plurality of bending patterns provided in the bending area and connected to the first lower connection line and the second lower connection line; an upper power link line provided in the second non-display area; and an upper connection line provided in the second non-display area and connecting the bending patterns to the upper power link line.

**[Claim 6]**

The display device of claim 5, wherein the upper power link line comprises a first portion extending to the first area and a second portion extending to the second area.

**[Claim 7]**

The display device of claim 6, wherein the first portion and the second portion of the upper power link line each extend to the central portion of the first area and the central portion of the second area, respectively.



**[Claim 8]**

The display device of claim 7, wherein some of the plurality of bending patterns extend from the end of the first portion of the upper power link line to the first lower connection line, and others of the plurality of bending patterns extend from the end of the second portion of the upper power link line to the second lower connection line.

**[Claim 9]**

The display device of claim 6, wherein the first portion and the second portion of the upper power link line each extend to the end of the first area and the end of the second area, respectively.

**[Claim 10]**

a plurality of data lines provided in the display area and supplying data signals to the plurality of pixels; and a plurality of data link lines provided in the non-display area and connected to the plurality of data lines; wherein a first portion of the upper power link line superimposes with all of the data link wires among the plurality of data link wires disposed in the first area; and a second portion of the upper power link line superimposes with all of the data link wires among the plurality of data link wires disposed in the second area.

**[Claim 11]**

The display device of claim 10, wherein the first lower power link line superimposes with all of the data link lines among the plurality of data link lines disposed in the first area, and the second lower power link line superimposes with all of the data link lines among the plurality of data link lines disposed in the second area.



**[Claim 12]**

The display device of claim 5, wherein the plurality of power lines are disposed in the display area, further comprising a plurality of third power lines that supply power to the plurality of pixels, the power link lines are disposed in the non-display area, further comprises a third lower power link line connected to the plurality of third power lines, wherein the substrate further comprises a third area between the first area and the second area in which the plurality of third power lines and the third lower power link line are disposed.

**[Claim 13]**

The display device of claim 5, wherein the power link line further comprises a pad connection line connecting the central portion of the upper power link line or both ends of the upper power link line to pads in the pad area.

**[Claim 14]**

The display device of claim 13, wherein the pad connection line comprises a first pad connection line and a second pad connection line, each disposed at both ends of the second non-display area within the pad area.

**[Claim 15]**

The display device of claim 5, wherein the upper power link line comprises: a first upper power link line disposed at one end of the second non-display area and including a first portion extending into the first area; and a second upper power link line disposed at the other end of the second non-display area and including a second portion extending into the second area.



**[Claim 16]**

The display device of claim 5, wherein the bending pattern is a pattern in which a conductive pattern having at least one of a diamond shape, a rhombus shape, a zigzag shape, or a circular shape is repetitively arranged.

**[Claim 17]**

A display device comprising: a substrate including a display area provided with a plurality of pixels and a non-display area adjacent to the display area; a plurality of power lines provided in the display area to supply power to the plurality of pixels, comprising a plurality of first power lines and a plurality of second power lines; and a power link line disposed in the non-display area and connected to the plurality of first power lines and the plurality of second power lines; wherein the first lower power link line and the second lower power link line are arranged within the left and right areas of the substrate, respectively, to minimize the power voltage drop in the power lines and the power link line.

**[Claim 18]**

The display device of claim 17, wherein the non-display area comprises: a first non-display area extending from the display area and in which the first lower power link line and the second lower power link line are disposed; a bending area extending from the first non-display area; a second non-display area extending from the bending area; and a pad area extending from the second non-display area, wherein the first lower power link line extends from the first non-display area to both ends of the left area, the second lower power link line extends from the first non-display area to both ends of the right area, and the first lower power link line and the second lower power link line are connected at the boundary between the left area and the right area.



**[Claim 19]**

The display device of claim 18, wherein the power link line further comprises a first lower connection line extending from the first lower power link line to the bending area and a second lower connection line extending from the second lower power link line to the bending area, wherein the plurality of first power lines are disposed symmetrically with respect to the first lower connection line, and the plurality of second power lines are arranged symmetrically with respect to the second lower connection line.

**[Claim 20]**

The display device of claim 18 further comprising: a plurality of data lines provided in the display area and supplying data signals to the plurality of pixels; and a plurality of data link lines provided in the non-display area and connected to the plurality of data lines; wherein the power link lines further comprise a plurality of bending patterns disposed in the bending area and connected to the first lower power link line and the second lower power link line; and an upper power link line provided in the second non-display area and including a first portion electrically connected to the first lower power link line and a second portion electrically connected to the second lower power link line, wherein the first portion and the second portion are superimposed with the multiple data link lines so as to minimize deviation due to the RC load of the multiple data link lines.



**[Claim 21]**

The display device of claim 20, wherein the first lower-power link line and the second lower-power link line are arranged to superimpose with the plurality of data link lines so as to minimize deviations caused by the RC load of the plurality of data link lines.



### **[Summary]**

#### **[Abstract]**

This specification relates to a display device comprising a substrate having a display area equipped with a plurality of pixels and a non-display area adjacent to the display area; a plurality of power lines, including a first power line and a second power line, provided in the display area to supply power to the plurality of pixels; a lower power link line provided in the non-display area and connected to the plurality of power lines; and a power link line extending from the lower power link line and comprising a first lower connection line and a second lower connection line, wherein the plurality of first power lines includes at least two first power lines equidistant from the first lower connection line, and the plurality of second power lines includes at least two second power lines equidistant from the second lower connection line. Therefore, by distributing the points where power is supplied, voltage drop can be reduced, and luminance uniformity can be improved.

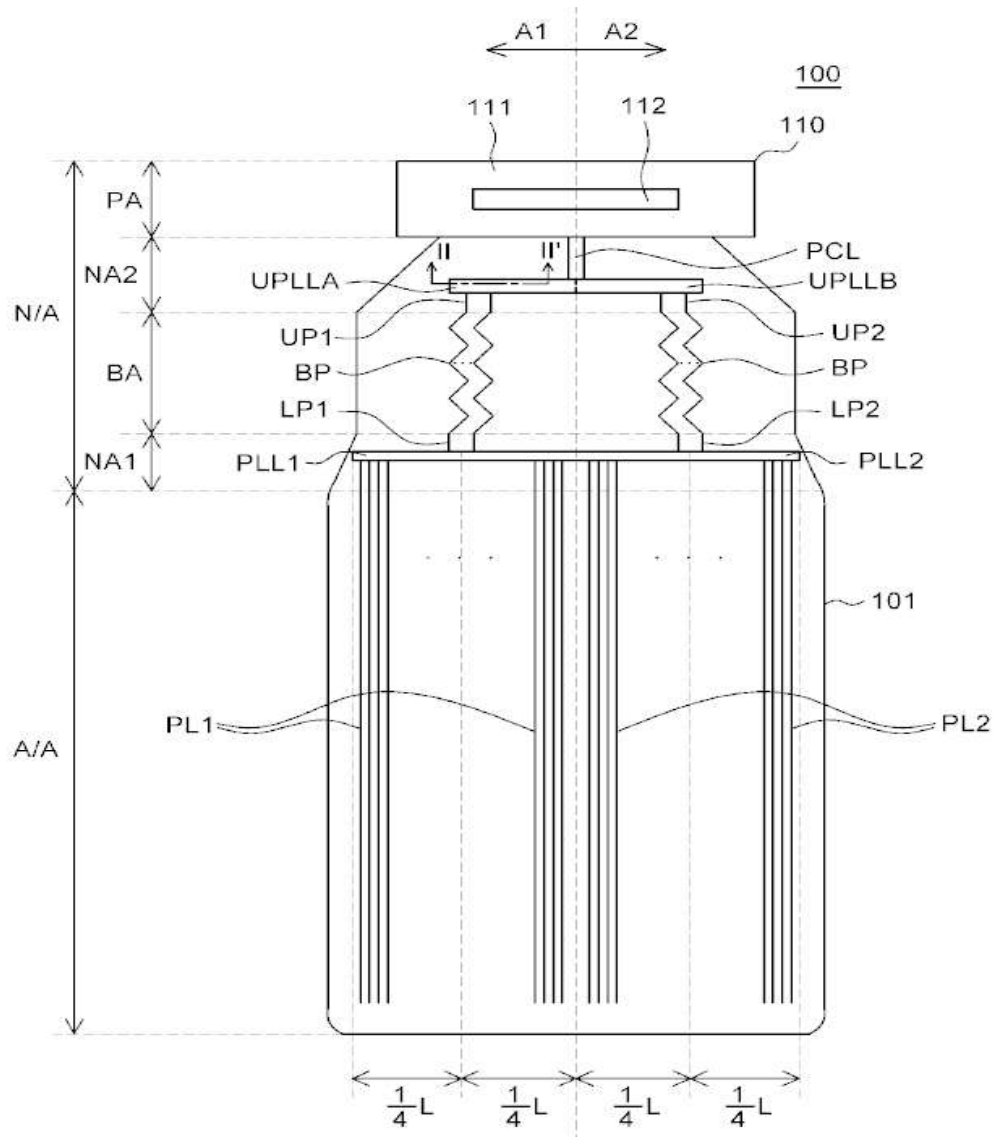
#### **[Representative Drawing]**

FIG. 1



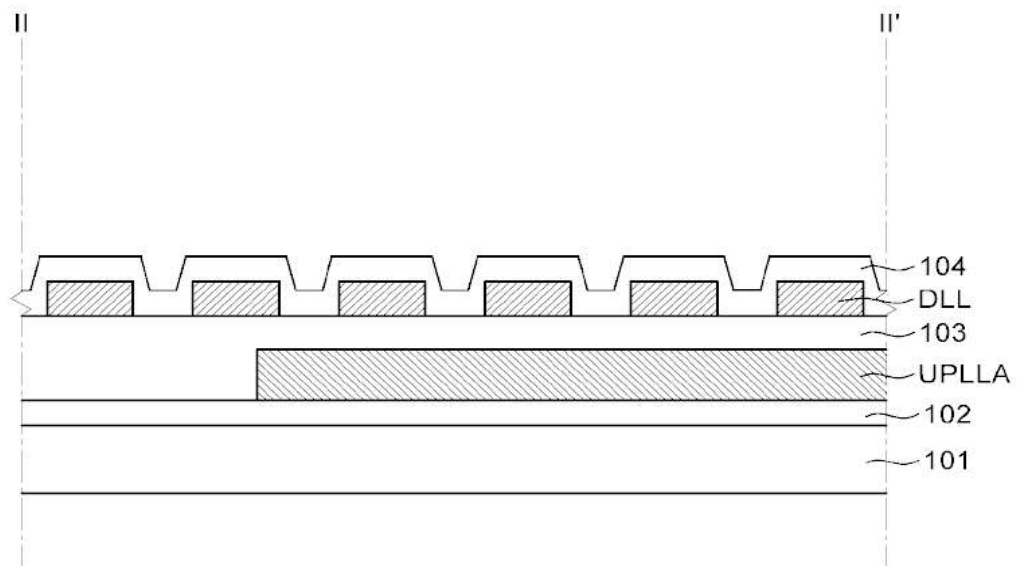
[Drawing]

[FIG. 1]





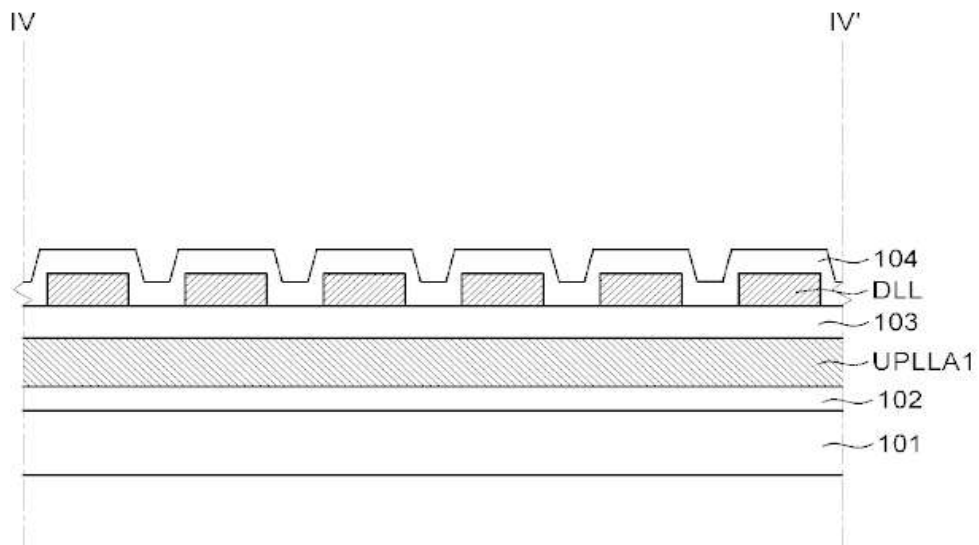
[FIG. 2]



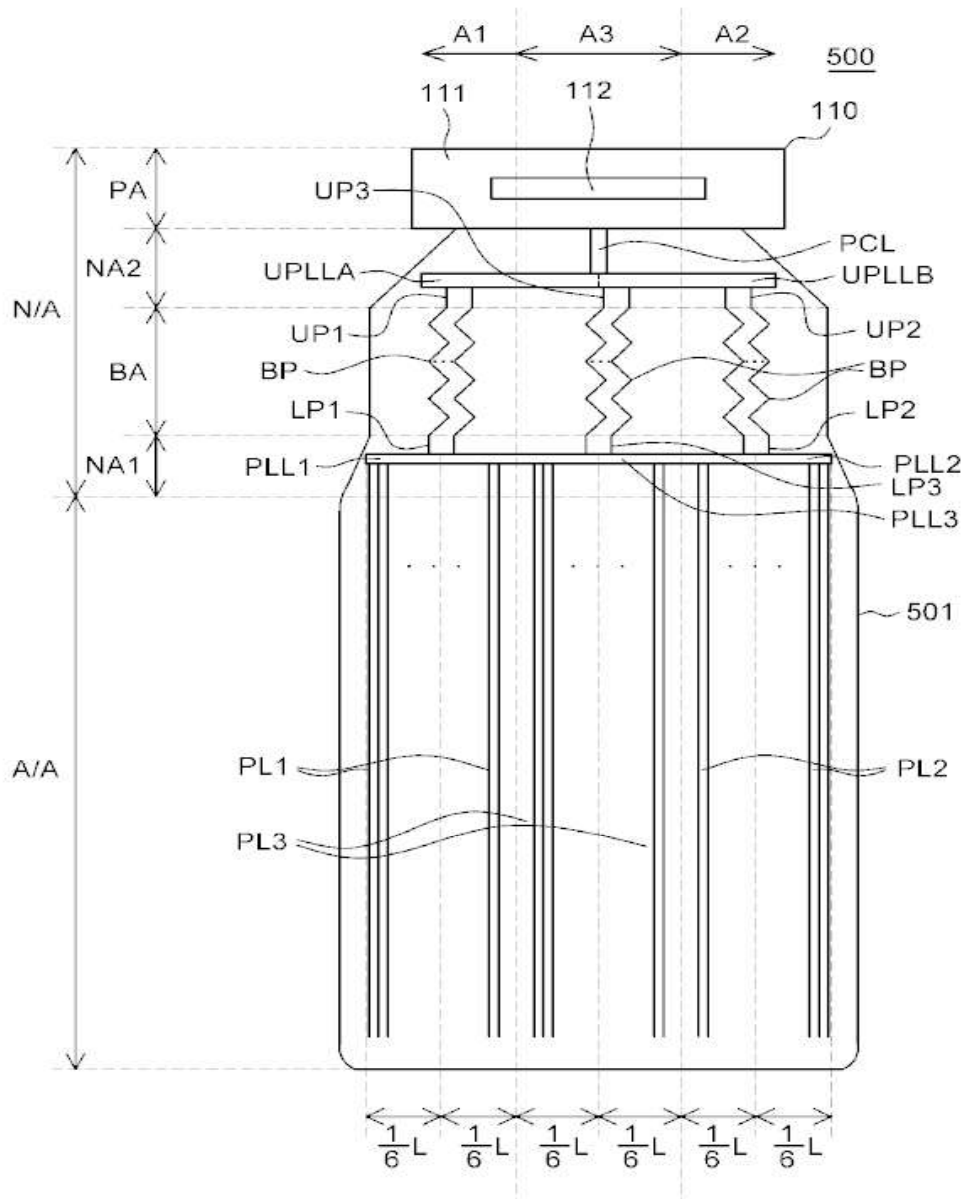




[FIG. 4]

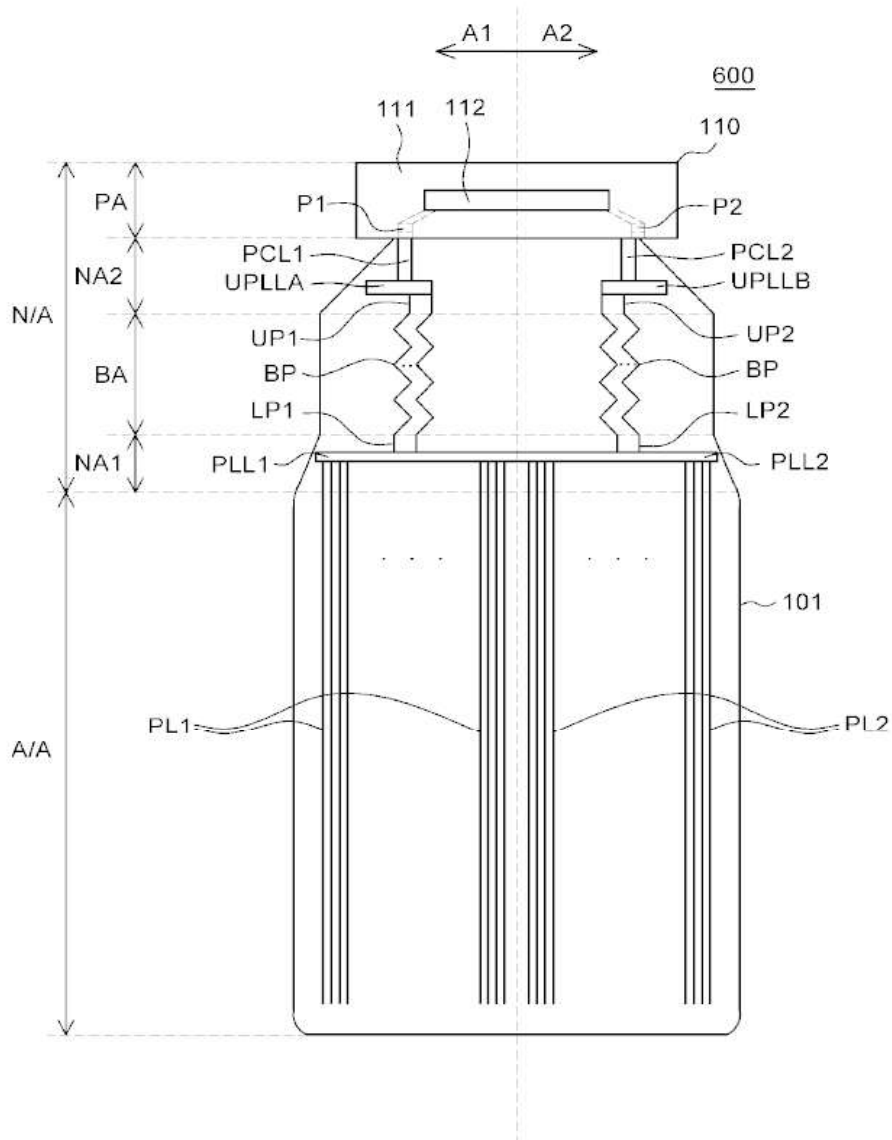


[FIG. 5]



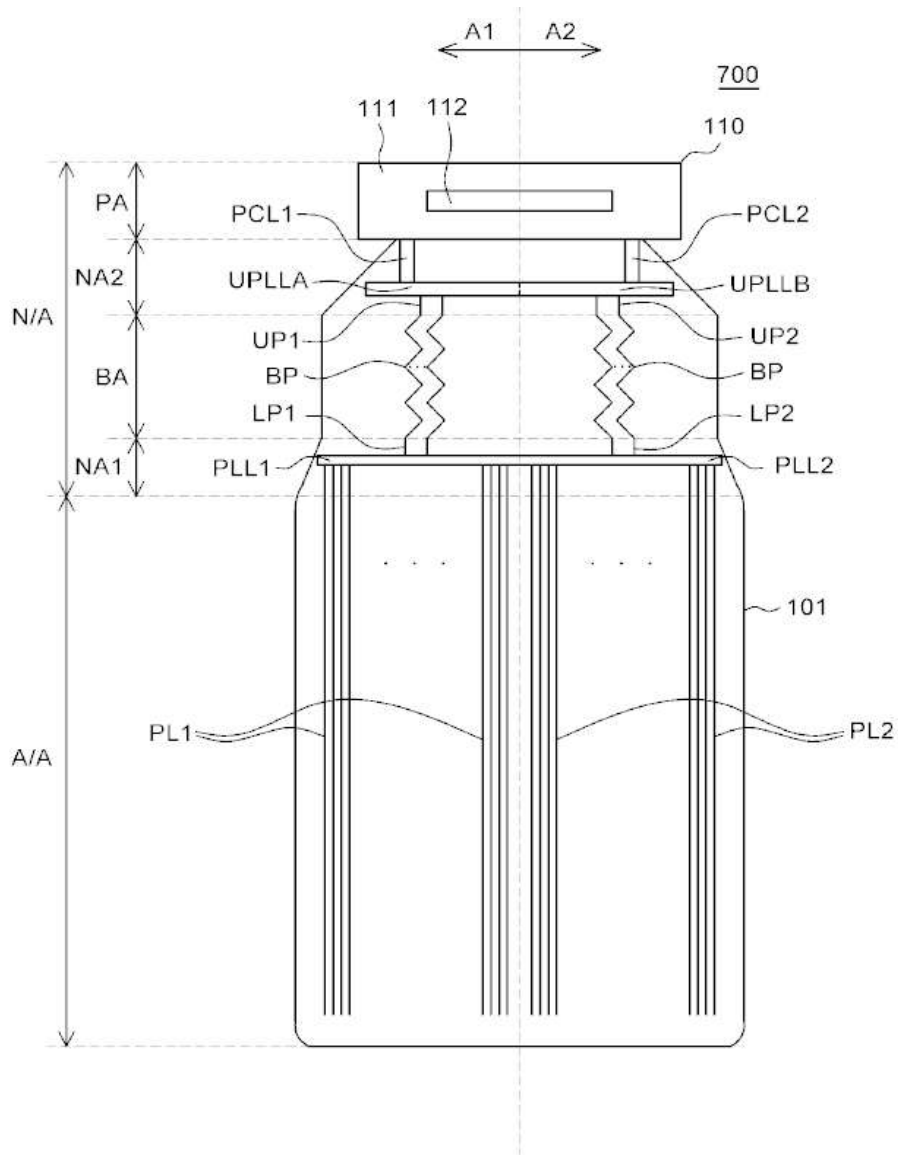


[FIG. 6]

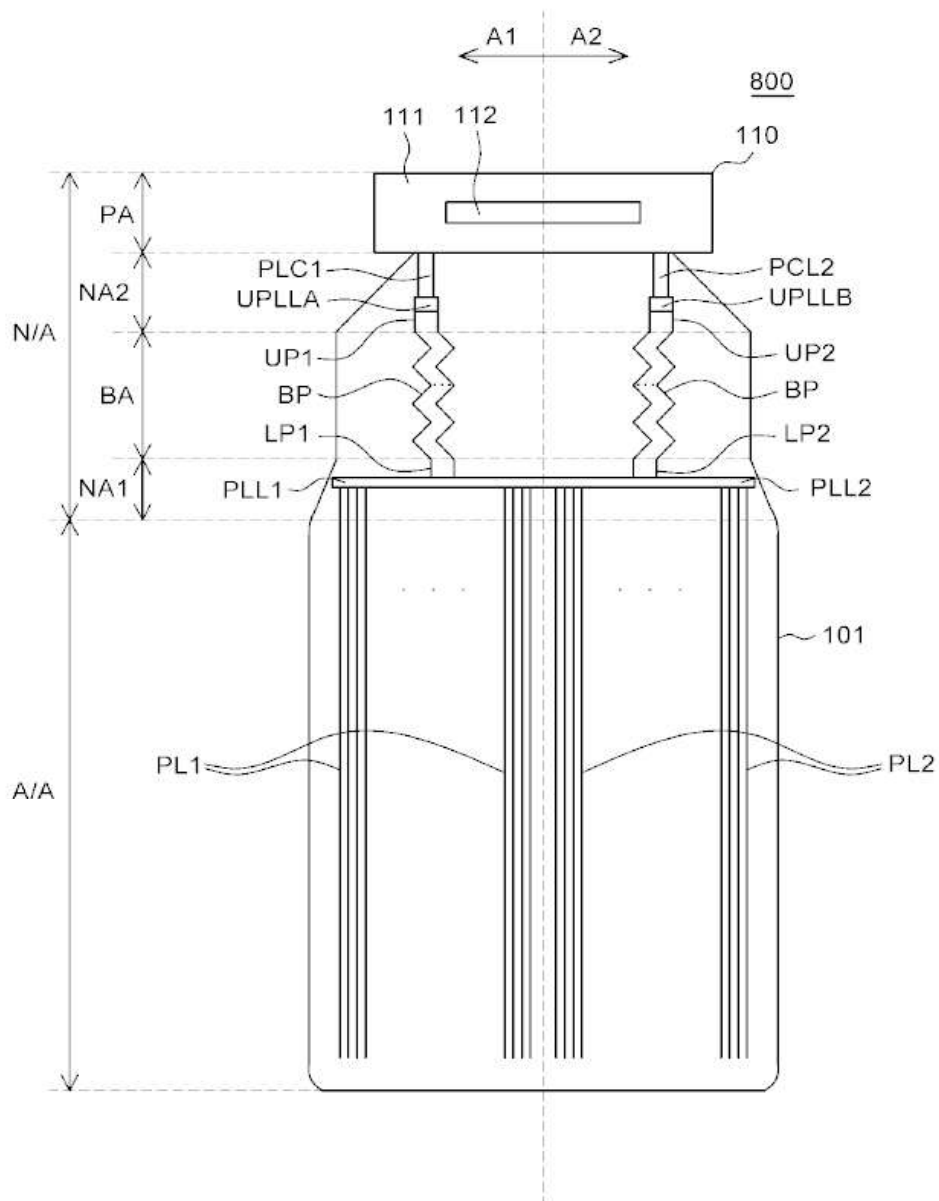




[FIG. 7]



[FIG. 8]





[FIG. 9]

