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I am a professional translator, reviewer, and/or project manager specializing in translating Korean, Japanese, and Chinese into English and vice versa.

I served as Chief Examiner for the State of California's certified court interpreter exam and as a contract translator and interpreter for various federal agencies through the U.S. Department of State for more than a decade. I taught at the University of California, Berkeley, and the Middlebury Institute of International Studies at Monterey (MIIS) Graduate Program in Translation.

I have more than 35 years of project coordination experience, routinely handling technical, legal, and business documents translated between English and Korean. These documents were submitted to entities including Korean judicial authorities, U.S. federal courts, the U.S. International Trade Commission (ITC), the U.S. Patent and Trademark Office (USPTO), and the USPTO Patent Trial and Appeal Board (PTAB).

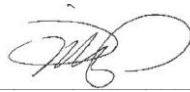
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Ex-1011, Lee '538 (Korean priority application)

I certify under penalty of perjury that the foregoing is true and correct.

Executed on the 25th day of June 2026 in Contra Costa County, State of California.

By: _____



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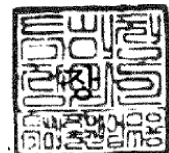
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[Bibliography]

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[Applicant]	
[Name]	Samsung Display Co., Ltd.
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[Title of the Invention in Korean]	DISPLAY APPARATUS
[Title of the Invention in English]	DISPLAY APPARATUS
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[Application Language]	Korean

[Purpose] This application is hereby submitted to the Commissioner of the Korean Intellectual Property Office (KIPO) as stated above.

Attorney, Agent or Firm Y.P. Lee, Mock & Partners (signature or seal)

[Fees]

[Application Filing Fee]	0 sheet(s)	46,000 KRW
[Additional Application Filing Fee]	80 sheets	0 KRW
[Priority Claim Fee]	0 case(s)	0 KRW
[Fee for Request for Examination]	0 claim(s)	0 KRW
[Total]		46,000 KRW

[Description of the Invention]

[Title of the Invention]

DISPLAY APPARATUS [*in Korean*] {DISPLAY APPARATUS [*in English*]}

[Technical Field]

[0001] The present invention relates to a display apparatus, and more particularly, to a display apparatus in which cracks in the wiring in the bending area have been improved.

[Background Art of the Invention]

[0002] Among display devices, organic light-emitting display devices are attracting attention as next-generation display devices due to their advantages of wide viewing angles, excellent contrast, and fast response times.

[0003] Generally, an organic light-emitting display apparatus comprises thin-film transistors and organic light-emitting diodes (OLEDs) formed on a substrate, and operates by the OLEDs emitting light on their own. Such organic light-emitting display apparatuses are used as display units in both small devices, such as mobile phones, and large devices, such as televisions.

[Summary of the Invention]

[Problem to Be Solved by the Invention]

[0004] The present invention aims to provide a display apparatus that improves wiring cracks in bending areas. However, these issues are merely exemplary, and the scope of the present invention is not limited thereto.

[Means to Solve the Problem]

[0005] According to one aspect of the present invention, a display apparatus is provided, comprising: a substrate including a display area, a peripheral area surrounding the display area and extending on one side thereof, and a bending area in which at least a portion of the peripheral area is bent; an inorganic insulating layer disposed on the substrate so as to overlap the display area and the peripheral area, and having an opening corresponding to the bending area; a display element disposed on the pixel circuit; contact metal that electrically connects the pixel circuit and the display element; an optical functional layer comprising a first layer disposed on the display element and having an opening corresponding to the display element, and a second layer disposed on the first layer, extending into the peripheral area, and covering the bending area; a pad section disposed at the end of the peripheral area; a first organic layer disposed on the bending area; and connecting wiring that extends from the display area through the bending area to the pad section, at least a portion of which comprises the same material as the contact metal; wherein the connecting wiring comprises a first metal pattern disposed beneath the first organic layer; and a second metal pattern disposed on top of the first organic layer and electrically connected to the first metal pattern through contact holes penetrating the first organic layer.

[0006] According to this embodiment, the opening has a sloped surface and a lower surface, and at least a portion of the connecting wiring may be disposed in contact with the sloped surface and the lower surface.

[0007] According to this embodiment, the display apparatus further comprises a planarized insulating layer disposed on the pixel circuit, wherein the planarized insulating layer comprises: a first planarized insulating layer; and a second planarized insulating layer disposed on the first planarized insulating layer; and the first organic layer may comprise the same material as the first planarized insulating layer.

[0008] According to this embodiment, the display apparatus may further comprise a buried organic layer disposed on the connection wiring corresponding to the opening and filling at least a portion of the opening.

[0009] According to this embodiment, the first height—from the lower surface of the opening to the upper surface of the buried organic layer—may be greater than the second height—from the lower surface of the opening to the upper surface of the inorganic insulating layer.

[0010] According to this embodiment, the buried organic layer may comprise the same material as the second planarized insulating layer.

[0011] According to this embodiment, a second organic layer disposed on the buried organic layer corresponding to the opening may further be comprised.

[0012] According to this embodiment, the third height—measured from the lower surface of the opening to the upper surface of the second organic layer—may be greater than the second height—measured from the lower surface of the opening to the upper surface of the inorganic insulating layer.

[0013] According to this embodiment, the device further includes a pixel-defining film disposed on the planarized insulating layer and defining a light-emitting area through the opening; the second organic layer may comprise the same material as the pixel-defining film.

[0014] According to this embodiment, a planarized insulating layer disposed on the pixel circuit; a pixel-defining film disposed on the planarized insulating layer and defining a light-emitting area through an opening; and a buried organic layer disposed beneath the connection wiring corresponding to the opening and filling at least a portion of the opening; wherein the first organic layer comprises the same material as the pixel-defining film, and the buried organic layer may comprise the same material as the planarized insulating layer.

[0015] According to this embodiment, the pixel circuit includes a thin-film transistor and a storage capacitor; the thin-film transistor includes a semiconductor layer, a gate electrode that at least partially overlaps the semiconductor layer, and an electrode layer on the gate electrode; the first metal pattern comprises the same material as the electrode layer; and the second metal pattern may comprise the same material as the contact metal.

[0016] According to this embodiment, the display element includes an input sensing layer disposed thereon, wherein the input sensing layer comprises a first insulating layer, a first conductive layer, a second conductive layer, and a second insulating layer disposed between the first conductive layer and the second conductive layer; the first metal pattern comprises the same material as the contact metal, and the second metal pattern may comprise the same material as the first conductive layer.

[0017] According to this embodiment, the first layer may be disposed so as to cover the bending area.

[0018] According to this embodiment, an input sensing layer is disposed on the display element; the input sensing layer comprises a first insulating layer, a first conductive layer, a second conductive layer, and a second insulating layer disposed between the first conductive layer and the second conductive layer; the second insulating layer comprises an organic insulating material and may be disposed so as to cover the bending area.

[0019] According to this embodiment, the first insulating layer comprises an organic insulating material and may be disposed so as to cover the bending area.

[0020] According to this embodiment, the device may further include a stress-relief layer disposed on the optical functional layer corresponding to the bending area.

[0021] According to this embodiment, the first metal pattern is disposed along a first direction, and the first organic layer may expose at least a portion of each of the first metal patterns through the contact holes.

[0022] According to this embodiment, the first organic layer may be disposed so as to cover the edges of each of the first metal patterns.

[0023] According to this embodiment, the second metal pattern may be disposed offset from the first metal pattern along the first direction.

[0024] According to this embodiment, the first metal pattern includes a plurality of mutually spaced metal islands, the second metal pattern includes a plurality of mutually spaced metal bridges, and the metal islands may be interconnected by the metal bridges.

[0025] According to this embodiment, one end of the metal bridge may be connected to a single metal island, and the other end may be connected to another metal island adjacent to the metal island.

[0026] According to this embodiment, the metal bridges may include first bridges and second bridges that are spaced apart and arranged side by side around the metal islands.

[Effect of the Invention]

[0027] According to one embodiment of the present invention described above, a display apparatus in which cracks in the wiring in the bending area have been improved can be implemented in detail. Of course, the scope of the present invention is not limited to these effects.

[Brief Description of the Drawings]

[0028] FIG. 1 is a plan view schematically illustrating a portion of a display apparatus according to one embodiment of the present invention.

FIG. 2a and FIG. 2b are cross-sectional views schematically illustrating cross-sections of the display apparatus of FIG. 1 taken along line A-A'.

FIG. 3 is a plan view schematically illustrating a portion of the display apparatus according to one embodiment of the present invention.

FIG. 4 is an equivalent circuit diagram of a pixel that may be included in a display apparatus according to one embodiment of the present invention.

FIG. 5 is a plan view schematically illustrating the display panel of the display apparatus shown in FIG. 1.

FIG. 6 is a cross-sectional view schematically illustrating a portion of the display apparatus according to one embodiment of the present invention.

FIG. 7 is a cross-sectional view showing a portion of FIG. 6 enlarged and schematically illustrated.

FIGS. 8a through 8c are cross-sectional views schematically showing an enlarged portion of the display apparatus according to one embodiment of the present invention.

FIG. 9 is a cross-sectional view schematically illustrating a portion of a display apparatus according to one embodiment of the present invention.

FIG. 10 is a cross-sectional view showing a portion of FIG. 9 magnified and schematically illustrated.

FIG. 11 is a cross-sectional view schematically showing an enlarged portion of a display apparatus according to one embodiment of the present invention.

FIGS. 12a through 12d are plan views showing a portion of FIG. 5 enlarged and schematically illustrated.

FIG. 13 is a cross-sectional view schematically showing a cross section taken along the H-H' line of the connection wiring in FIG. 12.

[Detailed Description of Embodiments]

[0029] Since the present invention is capable of various modifications and may have multiple embodiments, specific embodiments are illustrated in the drawings and described in detail in the description below.

The effects and features of the present invention, as well as the methods for achieving them, will become clear upon reference to the embodiments described in detail below, together with the drawings. However, the present invention is not limited to the embodiments disclosed below but may be implemented in various forms.

[0030] Hereinafter, the embodiments of the present invention will be described in detail with reference to the accompanying drawings; when describing with reference to the drawings, identical or corresponding components are assigned the same reference numerals, and redundant descriptions thereof are omitted.

[0031] In this specification, terms such as “first” and “second” are used not in a limiting sense, but for the purpose of distinguishing one component from another.

[0032] In this specification, expressions in the singular include the plural unless the context clearly indicates otherwise.

[0033] Terms such as “include/comprise” or “have” in this specification mean that the features or components described herein are present, and do not preclude the possibility of adding one or more other features or components.

[0034] In this specification, when it is stated that a film, area/region, component, or other element is located on top of or above another element, this includes not only cases where it is directly above the other element, but also cases where another film, area, component, or other element is interposed between them.

[0035] In this specification, when a film, area, component, etc., is described as being connected, this includes cases where the films, areas, or components are directly connected, and/or cases where they are indirectly connected with other films, areas, or components interposed between them.

For example, when this specification states that a film, area, component, etc., is electrically connected, this refers to cases where the film, area, component, etc., is directly electrically connected, and/or where another film, area, component, etc., is interposed between them, resulting in an indirect electrical connection.

[0036] In this specification, “A and/or B” refers to cases where it is A, B, or both A and B. Furthermore, “at least one of A and B” refers to cases where it is A, B, or both A and B.

[0037] In this specification, the x-axis, y-axis, and z-axis are not limited to the three axes of a Cartesian coordinate system but may be interpreted in a broader sense that includes them. For example, the x-axis, y-axis, and z-axis may be orthogonal to one another, but they may also refer to different directions that are not orthogonal to one another.

[0038] In this specification, if an embodiment can be implemented in other ways, a specific sequence of processes may be performed differently from the order in which they are described. For example, two processes described consecutively may be performed substantially simultaneously, or they may proceed in the reverse order of the description.

[0039] In the drawings, components may be shown enlarged or reduced in size for the sake of clarity. For example, the size and thickness of each component shown in the drawings are arbitrary representations for the sake of clarity; therefore, the present invention is not necessarily limited to what is shown.

[0040] FIG. 1 is a plan view schematically illustrating a portion of a display apparatus according to one embodiment of the present invention.

[0041] Referring to FIG. 1, the display apparatus (1) includes a display area (DA) and a peripheral area (NDA) outside the display area (DA). The display area (DA) contains a plurality of pixels (P) comprising display elements, and the display apparatus (1) can provide an image using light emitted from the plurality of pixels (P) disposed in the display area (DA). The peripheral area (NDA) is a type of non-display area where no display elements are arranged, and the display area (DA) may be entirely surrounded by the peripheral area (NDA).

[0042] Although FIG. 1 illustrates a display apparatus (1) having a flat display surface, the present invention is not limited thereto. In another embodiment, the display apparatus (1) may include a three-dimensional or curved display surface.

[0043] If the display apparatus (1) includes a three-dimensional display surface, the display apparatus (1) includes a plurality of display areas pointing in different directions and may, for example, include a polygonal prismatic display surface. In another embodiment, when the display apparatus (1) includes a curved display surface, the display apparatus (1) may, of course, be implemented in various forms, such as a flexible, foldable, or rollable display apparatus.

[0044] Furthermore, in one embodiment, FIG. 1 illustrates a display apparatus (1) that can be applied to a mobile phone terminal. Although not explicitly described, a mobile phone device can be configured by mounting the electronic modules, camera module, power supply module, and other

components mounted on the mainboard, together with the display apparatus (1), on a bracket or in a case. The display apparatus (1) according to the present invention can be applied to large electronic devices, such as televisions and monitors, as well as small and medium-sized electronic devices, such as tablets, in-car navigation systems, game consoles, and smartwatches.

[0045] FIG. 1 illustrates a case where the display area (DA) of the display apparatus (1) is a rectangle with rounded corners; however, in another embodiment, the shape of the display area (DA) may be circular, elliptical, or a polygon such as a triangle or pentagon.

[0046] Hereinafter, the display apparatus (1) according to one embodiment of the present invention will be described using an organic light-emitting display apparatus as an example; however, the display apparatus of the present invention is not limited thereto. As another embodiment, the display apparatus (1) of the present invention may be an inorganic light-emitting display apparatus (Inorganic Light Emitting Display or inorganic EL display apparatus) or a quantum dot light-emitting display apparatus (Quantum Dot Light Emitting Display). For example, the light-emitting layer of the display elements provided in the display apparatus (1) may include organic materials, inorganic materials, quantum dots, a combination of organic materials and quantum dots, or a combination of inorganic materials and quantum dots.

[0047] FIG. 2a and FIG. 2b are schematic cross-sectional views showing cross-sections taken along line A-A' of the display apparatus of FIG. 1, and FIG. 3 is a schematic plan view showing a portion of the display apparatus (1) according to one embodiment of the present invention.

[0048] Referring to FIG. 2a, the display apparatus (1) according to one embodiment of the present invention may include a display layer (DU), an input sensing layer (TU), an optical function

layer (OU), an anti-reflection layer (PU), and a window layer (WU). At least some of the components—including the display layer (DU), touch sensing layer (TU), optical function layer (OU), anti-reflective layer (PU), and window layer (WU)—may be formed through a continuous process, or at least some of the components may be bonded to one another via an adhesive member. FIG. 2a illustratively shows an optically clear adhesive (OCA) as the adhesive member. The adhesive member described below may include a conventional adhesive or tackifying agent. In one embodiment of the present invention, the anti-reflective layer (PU) and the window layer (WU) may be replaced by other structures or omitted.

[0049] In one embodiment, the input sensing layer (TU) is disposed directly on the display layer (DU). In this specification, the statement that “structure B is disposed directly on structure A” means that no separate adhesive layer or adhesive member is disposed between structure A and structure B. Structure B is formed via a continuous process on the base surface provided by structure A after structure A has been formed.

[0050] It can be defined as a display panel (DP) comprising a display layer (DU), an input sensing layer (TU) disposed directly on the display layer (DU), and an optical function layer (OU). In one embodiment, as shown in FIG. 2a, an optically clear adhesive (OCA) may be disposed between the display panel (DP) and the anti-reflective layer (PU), and between the anti-reflective layer (PU) and the window layer (WU), respectively.

[0051] In another embodiment, as shown in FIG. 2b, the display panel (DP) may include an anti-reflective layer (CU). The anti-reflection layer (CU) may be disposed between the touch sensing layer (TU) and the optical function layer (OU). The anti-reflection layer (CU) may include a color filter provided to correspond to the light-emitting area of each pixel (P) and a light-blocking layer provided to correspond to the non-light-emitting area between each pixel (P). In one embodiment, no optically clear adhesive (OCA) is interposed between the anti-reflection layer (CU) and the display panel (DP), and the anti-reflection layer (CU) may be disposed directly on the display panel (DP).

[0052] The display layer (DU) generates an image, and the input sensing layer (TU) acquires coordinate information of external inputs (e.g., touch events). Although not shown separately, the display panel (DP) according to one embodiment of the present invention may further include a protective member disposed on the underside of the display layer (DU). The protective member and the display layer (DU) may be bonded via an adhesive member.

[0053] The optical function layer (OU) can improve optical efficiency. The optical function layer (OU) can, for example, improve the front-view luminous efficiency and/or side visibility of light emitted from an organic light-emitting diode (OLED).

[0054] The anti-reflective layer (PU) reduces the reflectance of external light incident from the upper side of the window layer (WU). The anti-reflective layer (PU) according to one embodiment of the present invention may include a retarder and a polarizer. The retarder may be of the film type or the liquid crystal coating type, and may include a $\lambda/2$ retarder and/or a $\lambda/4$ retarder. The polarizer may also be of the film type or the liquid crystal coating type. The film type comprises a stretched synthetic resin film, and the liquid crystal coating type may comprise liquid crystals arranged in a predetermined array. The retarder and polarizer may further comprise a protective film. The retarder and polarizer themselves, or the protective film, may be defined as the base layer of the anti-reflective layer (PU).

[0055] The following describes in detail the structure of the display layer (DU), the touch-sensing layer (TU), and the optical function layer (OU) with reference to FIG. 3.

[0056] Referring to FIG. 3, the display panel (DP) includes a display layer (DU) and an input sensing layer (TU). The display layer (DU) is shown in a simplified manner to illustrate the stacking relationship of the input sensing layer (TU). Additionally, the polarization unit (PU, FIG. 2a) and the window unit (WU, FIG. 2a), which may be disposed on top of the input sensing layer (TU), are not shown.

[0057] The display layer (DU) may be formed on the substrate (100) with the circuit layer (CL), the organic light-emitting diode (OLED), and the thin film encapsulation layer (TFE) disposed sequentially thereon. The input sensing layer (TU) may be disposed directly on the thin film encapsulation layer (TFE). Since the thin film encapsulation layer (TFE) includes at least one organic encapsulation layer (320), as shown in FIG. 6 and others described below, it can provide a more planarized base surface. Therefore, even if the input sensing layer (TU) structures described below are formed through a continuous process, the fail rate can be reduced.

[0058] The input sensing layer (TU) may have a multilayer structure. The input sensing layer (TU) includes sensing electrodes, trace lines connected to the sensing electrodes, and at least one insulating layer. The input sensing layer (TU) may, for example, detect external inputs using a capacitive method. The operating method of the input sensing layer (TU) is not specifically limited in the present invention; in one embodiment of the present invention, the input sensing layer (TU) may also detect external inputs using an electromagnetic induction method or a pressure sensing method.

[0059] As shown in FIG. 3, the input sensing layer (TU) according to one embodiment of the present invention may include a first insulating layer (410), a first conductive layer (MTL1), a second insulating layer (420), and a second conductive layer (MTL2).

[0060] For example, the first conductive layer (MTL1) and the second conductive layer (MTL2)

may each have a single-layer structure or a stacked multilayer structure. The conductive layer in a monolithic structure may include a metal layer or a transparent conductive layer. The metal layer may include molybdenum, silver, titanium, copper, aluminum, and alloys thereof. The transparent conductive layer may include transparent conductive oxides such as ITO (indium tin oxide), IZO (indium zinc oxide), ZnO (zinc oxide), and ITZO (indium tin zinc oxide). In addition, the transparent conductive layer may include conductive polymers such as PEDOT, metal nanowires, and graphene.

[0061] A multilayer conductive layer may include multiple metal layers. The multiple metal layers may, for example, have a three-layer structure such as Ti/Al/Ti. A multilayer conductive layer may include at least one metal layer and at least one transparent conductive layer.

[0062] The first conductive layer (MTL1) and the second conductive layer (MTL2) each include a plurality of patterns. Hereinafter, the first conductive layer (MTL1) may be understood to include first conductive patterns, and the second conductive layer (MTL2) may be understood to include second conductive patterns. The first conductive patterns and the second conductive patterns may form the sensing electrodes shown in FIG. 6.

[0063] The first insulating layer (410) and the second insulating layer (420) may each have a single-layer or multi-layer structure. Each of the first insulating layer (410) and the second insulating layer (420) may include inorganic materials or composite materials. For example, at least one of the first insulating layer (410) and the second insulating layer (420) may include an inorganic film. The inorganic film may include at least one of aluminum oxide, titanium oxide, silicon oxide, silicon oxynitride, silicon nitride, zirconium oxide, and hafnium oxide. In another embodiment, the first insulating layer (410) and/or the second insulating layer (420) may be replaced with an organic insulating layer.

[0064] The optical functional layer (OU) may be disposed directly on the input sensing layer (TU). The optical functional layer (OU) may include a first layer (510) and a second layer (520) on top of the first layer (510). The first layer (510) and the second layer (520) may comprise organic insulating materials and may be configured to have different refractive indices. In one embodiment, the refractive index of the second layer (520) may be greater than that of the first layer (510).

[0065] FIG. 4 is a schematic diagram of a pixel (P) that may be included in a display apparatus (1) according to one embodiment of the present invention.

[0066] Referring to FIG. 4, each pixel (P) includes a pixel circuit (PC) connected to a scan line (SL) and a data line (DL), and an organic light-emitting diode (OLED) connected to the pixel circuit (PC).

[0067] The pixel circuit (PC) includes a drive thin-film transistor (Td), a switching thin-film transistor (Ts), and a storage capacitor (Cst). The switching thin-film transistor (Ts) is connected to the scan line (SL) and the data line (DL), and transmits the data signal (Dm) input via the data line (DL) to the driving thin-film transistor (Td) in response to the scan signal (Sn) input via the scan line (SL).

[0068] The storage capacitor (Cst) is connected to the switching thin-film transistor (Ts) and the drive voltage line (PL), and stores a voltage corresponding to the difference between the voltage received from the switching thin-film transistor (Ts) and the drive voltage (ELVDD) supplied to the drive voltage line (PL).

[0069] The drive thin-film transistor (Td) is connected to the drive power line (PL) and the storage capacitor (Cst), and can control the drive current flowing from the drive power line (PL) to the organic light-emitting diode (OLED) in accordance with the voltage value stored in the storage capacitor (Cst). The organic light-emitting diode (OLED) can emit light with a predetermined luminance based on the drive current (I_d).

[0070] Although FIG. 4 illustrates a case where the pixel circuit (PC) includes two thin-film transistors and one storage capacitor, the present invention is not limited thereto. In another embodiment, the pixel circuit (PC) may include seven thin-film transistors and one storage capacitor. In another embodiment, the pixel circuit (PC) may include two or more storage capacitors.

[0071] FIG. 5 is a plan view schematically illustrating the display panel (DP) of the display apparatus (1) shown in FIG. 1.

[0072] Referring to FIG. 5, the display panel (DP) includes a display unit (10), first and second scan drivers (20, 30), a terminal section (40), a data driver (50), a drive voltage supply line (60), and a common voltage supply line (70), all disposed on a substrate (100). Although not shown, a light-emission control driver (not shown) may be further disposed on one side of the first scan driver (20).

[0073] The substrate (100) may be formed from materials such as glass, metal, or organic materials. According to one embodiment, the substrate (100) may be formed from a flexible material. For example, the substrate (100) may be made of polyethersulfone, polyacrylate, polyetherimide,

polyethylene naphthalate, polyethylene terephthalate, polyphenylene sulfide, polyarylate, polyimide, polycarbonate, or cellulose acetate propionate.

[0074] Of course, various modifications are possible; for example, the substrate (100) may have a multilayer structure comprising two layers each containing such polymer resins and a barrier layer (comprising inorganic materials such as silicon oxide, silicon nitride, silicon oxynitride, or amorphous silicon) interposed between those layers.

[0075] The substrate (100) may include a display area (DA) and a peripheral area (NDA) surrounding the display area (DA). A portion of the peripheral area (NDA) may extend in one direction (e.g., the y-direction). The extended peripheral area (NDA) may accommodate a terminal section (40), a data driver (50), a drive voltage supply line (60), and fan-out wiring (FW), among other components. The substrate (100) may include a bending area (BA) corresponding to a portion of the peripheral area (NDA). For example, the bending area (BA) may be a portion of the extended peripheral area (NDA). By bending the bending area (BA) so that the extended peripheral area (NDA) partially overlaps with the display area (DA), the width of the peripheral area (NDA) visible to the user can be reduced.

[0076] The display unit (10) is located on the display area (DA) and includes pixels (P) connected to data lines (DL) and drive voltage lines (PL) extending in a first direction (e.g., the y-direction) and to scan lines (SL) extending in a second direction (e.g., the x-direction) that intersects the

first direction (e.g., the y-direction). Each pixel (P) emits light of, for example, red, green, blue, or white, and may include, for instance, an organic light-emitting diode (OLED).

[0077] The display unit (10) provides a predetermined image through light emitted from the pixels (P), and the display area (DA) is defined by the pixels (P). The display unit (10) has a generally rectangular shape, but in various embodiments, it may be configured as a polygon, a circle, an ellipse, or a shape corresponding to a portion thereof. In one embodiment, the display unit (10) has an overall rectangular shape but may have rounded corners where each corner is curved. The substrate (100) on which this display unit (10) is positioned may have curved edges in at least a portion of its outer perimeter.

[0078] The first and second scan drivers (20, 30) are disposed on the peripheral area (NDA) of the substrate (100) and generate and transmit scan signals to each pixel (P) via scan lines (SL). For example, the first scan driver (20) may be disposed on the left side of the display unit (10), and the second scan driver (30) may be disposed on the right side of the display unit (10). In this embodiment, a structure in which the first and second scan drivers (20, 30) are disposed on both sides of the display unit (10) is illustrated; however, in other embodiments, the scan driver may be disposed on only one side of the display unit (10).

[0079] The pad section (PD; see FIG. 6) may be located at the end extending from one side of the peripheral area (NDA). The pad section (PD) may be located on the peripheral area (NDA) of the substrate (100). The pad section (PD) may include pads for connecting to the terminal section (40) and the data driver (50).

[0080] The terminal section (40) is disposed at one end of the substrate (100) and includes a plurality of terminals (41, 42, 43, 44). The terminal section (40) is exposed and not covered by an insulating layer, allowing it to be electrically connected to a control unit, such as a flexible printed circuit board or an IC chip.

[0081] The data driver (50) is disposed on the peripheral region (NDA) of the substrate (100) and generates and transmits data signals to each pixel (P) via data lines (DL). The data driver (50) may be disposed on one side of the display unit (10) and, for example, may be disposed between the terminal portion (40) and the display unit (10). The data driver (50) can transmit data signals to the display panel (DP) by connecting to the pad section (PD). Although FIG. 5 illustrates the data driver (50) as being arranged on the substrate (100), in another embodiment, the data driver (50) may be provided on a flexible printed circuit board connected to the terminal portion (40).

[0082] The control unit converts multiple video signals received from an external source into multiple video data signals and transmits the converted signals to the data driver (50) via terminal (41). Furthermore, the data driver (50) generates data signals, and the generated data signals can be transmitted to the display area (DA) via fan-out wiring (FW). Furthermore, the control unit receives vertical sync signals, horizontal sync signals, and clock signals, generates control signals to drive the first and second scan drivers (20, 30), and transmits these signals to each driver via terminal (43). The control unit supplies the drive voltage (ELVDD) and the common voltage (ELVSS) to the drive voltage supply line (60) and the common voltage supply line (70), respectively, via terminals (42, 44).

[0083] The drive voltage supply line (60) is disposed on the peripheral area (NDA). For example, the drive voltage supply line (60) may be disposed between the data driver (50) and the display unit (10).

The drive voltage supply line (60) supplies a drive voltage (ELVDD) to the pixels (P). The drive voltage supply line (60) is disposed in a second direction (e.g., the x-direction) and may be connected to a plurality of drive voltage lines (PL) disposed in a first direction (e.g., the y-direction).

[0084] The common voltage supply line (70) is disposed on the peripheral area (NDA) and supplies a common voltage (ELVSS) to the counterelectrodes (230, FIG. 6) of the organic light-emitting diodes of the pixels (P). For example, the common voltage supply line (70) may be in the form of a loop open on one side and extend along the edge of the substrate (100), excluding the terminal section (40).

[0085] Meanwhile, an optical function layer (OU) may be disposed on top of the display area (DA). The optical function layer (OU) is formed across the entire front surface of the display area (DA) and may extend partially into the peripheral area (NDA). In practice, the optical function layer (OU) is disposed on top of the touch-sensing layer (TU) shown in FIG. 2a and FIG. 3 above, and it can serve to improve the light efficiency of pixels (P) and lateral visibility on the display area (DA).

[0086] The optical function layer (OU) is disposed on the front surface of the display area (DA), and a portion thereof may be disposed on the peripheral area (NDA). A second layer (520) of the optical function layer (OU) may extend toward the peripheral area (NDA). In one embodiment, the second layer (520) may extend toward the peripheral area (NDA) so as to overlap with the bending area (BA) of the substrate (100).

[0087] The second layer (520) covers the bending area (BA) and extends onto the peripheral area (NDA), but may not overlap with the data driver (50). The leading edge (520e) of the second layer (520) may be located between the bending area (BA) and the data driver (50). In this case, as the second layer (520) extends into the peripheral area (NDA), the end (520e) of the second layer (520) may be

configured to be as close as possible to the data driver (50) in order to sufficiently secure the width (L) extending from the bending area (BA). For example, the width (L) between the end of the bending area (BA) of the second layer (520) on the data driver (50) side and the end (520e) of the second layer (520) must be at least approximately 1 mm, and may, for example, be approximately 4 mm to 5 mm.

[0088] FIG. 6 is a cross-sectional view schematically illustrating a portion of a display apparatus according to one embodiment of the present invention. FIG. 6 corresponds to a cross section taken along line B-B' in FIG. 5.

[0089] First, with reference to FIG. 6, the structure on the display area (DA) will be described.

[0090] A barrier layer (110) may be disposed on the substrate (100). A buffer layer (111) may be disposed on the barrier layer (110). The buffer layer (111) may serve to prevent impurities from migrating through the substrate (100) into the various devices disposed on the substrate (100).

[0091] A pixel circuit (PC) comprising a thin-film transistor (TFT) and a storage capacitor (Cst) may be disposed on a buffer layer (111). The thin-film transistor (TFT) may include a semiconductor layer (A), a gate electrode (G) overlapping the channel region of the semiconductor layer (A), and an electrode layer (120) on the gate electrode (G). The electrode layer (120) may include a source electrode (S) and a drain electrode (D), connected to the source region and drain region of the semiconductor layer (A), respectively. A gate insulating layer (112) is interposed between the semiconductor layer (A) and the gate electrode (G), and a first interlayer insulation layer (113) and a second interlayer insulation layer (115) may be disposed between the gate electrode (G) and the electrode layer (120).

[0092] The storage capacitor (Cst) may be disposed in a stacked configuration with a thin-film transistor (TFT). The storage capacitor (Cst) may include a first electrode (CE1) and a second electrode (CE2) that are stacked on top of each other. In one embodiment, the gate electrode (G) of the thin-film transistor (TFT) may be integrally formed with the first electrode (CE1) of the storage capacitor (Cst). A first interlayer insulation layer (113) may be disposed between the first electrode (CE1) and the second electrode (CE2).

[0093] The semiconductor layer (A) may include a channel region and heavily doped source and drain regions. In one embodiment, the semiconductor layer (A) may include a silicon semiconductor material. In one embodiment, the semiconductor layer (A) may include polysilicon or amorphous silicon. In one embodiment, the semiconductor layer (A) may also include an oxide semiconductor material. In one embodiment, the pixel circuit (PC) includes a plurality of thin-film transistors (TFTs), and some of the TFTs may include a silicon semiconductor material, while other TFTs may include an oxide semiconductor material. When the semiconductor layer (A) includes an oxide semiconductor material, it may, for example, include an oxide of at least one material selected from the group consisting of indium (In), gallium (Ga), tin (Sn), zirconium (Zr), hafnium (Hf), titanium (Ti), and zinc (Zn).

[0094] The gate insulating layer (112) may comprise inorganic insulating materials such as silicon oxide, silicon oxynitride, or silicon nitride, and may be a single-layer or multilayer structure comprising the aforementioned materials.

[0095] The gate electrode (G) or first electrode (CE1) may comprise low-resistance conductive materials such as molybdenum (Mo), aluminum (Al), copper (Cu), and/or titanium (Ti), and may be a single layer or a multilayer structure composed of the aforementioned materials.

[0096] The first interlayer dielectric (113) may include inorganic insulating materials such as silicon oxide, silicon oxynitride, and silicon nitride, and may be a single layer or a multilayer structure comprising the materials above.

[0097] The second electrode (CE2) may include aluminum (Al), chromium (Cr), molybdenum (Mo), titanium (Ti), tungsten (W), and/or copper (Cu), and may be a single-layer or multilayer structure comprising the aforementioned materials.

[0098] The second interlayer insulation layer (115) may include inorganic insulating materials such as silicon oxide, silicon oxynitride, and silicon nitride, and may be a single-layer or multilayer structure comprising the aforementioned materials.

[0099] The electrode layer (120) may include aluminum (Al), molybdenum (Mo), titanium (Ti), tungsten (W), and/or copper (Cu), and may be a single-layer or multilayer structure comprising the aforementioned materials. For example, the electrode layer (120) may be a three-layer structure consisting of a titanium layer, an aluminum layer, and a titanium layer.

[0100] A planarized insulating layer (PIL) may be arranged on the pixel circuit (PC). The planarized insulating layer (PIL) may include at least one inorganic insulation layer (IOL), such as a barrier layer (110), a buffer layer (111), a gate insulation layer (112), a first interlayer insulation layer (113), and a second interlayer insulation layer (115), as well as other materials.

[0101] The planarized insulating layer (PIL) may include a first planarized insulating layer (116) and a second planarized insulating layer (117). The first planarized insulating layer (116) may include organic insulating materials such as acrylic, BCB (benzocyclobutene), polyimide, or HMDSO (hexamethyldisiloxane).

[0102] The second planarized insulating layer (117) may be arranged on top of the first planarized insulating layer (116). The second planarized insulating layer (117) may include organic insulating materials such as acrylic, BCB (benzocyclobutene), polyimide, or HMDSO (hexamethyldisiloxane). A contact metal (130) is disposed on the first planarized insulating layer (116), and the thin-film transistor (TFT) and the pixel electrode (210) can be electrically connected via the contact metal (130).

[0103] The pixel electrode (210) may be arranged on the second planarized insulating layer (117). The pixel electrode (210) may include a reflective layer containing silver (Ag), magnesium (Mg), aluminum (Al), platinum (Pt), palladium (Pd), gold (Au), nickel (Ni), neodymium (Nd), iridium (Ir), chromium (Cr), or compounds thereof. The pixel electrode (210) may include a reflective layer comprising the aforementioned materials, and a transparent conductive layer disposed above and/or below the reflective layer. The transparent conductive layer may include indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium oxide (In_2O_3), indium gallium oxide (IGO), or aluminum zinc oxide (AZO). In one embodiment, the pixel electrode (210) may have a three-layer structure consisting of an ITO layer, an Ag layer, and an ITO layer, stacked sequentially.

[0104] The pixel-defining film (119) covers the edges of the pixel electrode (210) and may include an opening that exposes the center of the pixel electrode (210). The pixel defining film (119) may include organic insulating materials such as BCB (benzocyclobutene), polyimide, or HMDSO (hexamethyldisiloxane). The light-emitting area (EA) can be defined through the opening in the pixel defining film (119), and red, green, or blue light can be emitted through the light-emitting area (EA). The area or width of the light-emitting area (EA) can define the area or width of the pixel.

[0105] The pixel defining film (119) may be formed in black. This pixel defining film (119) contains a light-blocking material and may be provided in black. The light-blocking material may include carbon black, carbon nanotubes, resins or pastes containing black dyes, metal particles such as nickel, aluminum, molybdenum, and their alloys, metal oxide particles (e.g., chromium oxide), or metal nitride particles (e.g., chromium nitride). If the pixel defining film (119) includes a light-blocking material, it can reduce edge reflections caused by the metal structures disposed beneath the pixel defining film (119).

[0106] The spacer (121) may be formed on the pixel-defining film (119). The spacer (121) can prevent damage to the layers beneath it caused by the mask during the formation process of the intermediate layer (220) and other layers to be described later. In one embodiment, the spacer (121) may comprise the same material as the pixel defining film (119), or it may comprise a different material. For example, if the spacer (121) comprises the same material as the pixel-defining film (119), the spacer (121) and the pixel-defining film (119) can be formed as a single unit through a halftone mask. If the pixel-defining film (119) is formed in black, the spacer (121) may also be formed in black.

[0107] The intermediate layer (220) includes a light-emitting layer that overlaps the pixel electrode (210). The light-emitting layer may contain organic materials. The light-emitting layer may contain polymeric organic materials or low-molecular-weight organic materials that emit light of a predetermined color. As described above, the light-emitting layer may be formed through a deposition process using a mask.

[0108] A first functional layer and a second functional layer may be disposed below and/or above the light-emitting layer, respectively. In one embodiment, unlike the light-emitting layer, which is patterned and disposed for each pixel, the first functional layer and the second functional layer may be provided integrally across the entire display area (DA).

[0109] The first functional layer may be a single layer or a multilayer. For example, when the first functional layer is formed from a polymeric material, it may be a single-layer structure known as a Hole Transport Layer (HTL), formed from polyethylene dihydroxythiophene (PEDOT: poly-(3,4)-ethylene-dihydroxythiophene) or polyaniline (PANI: polyaniline). If the first functional layer is formed from a low-molecular-weight material, it may include a hole injection layer (HIL) and a hole transport layer (HTL).

[0110] The second functional layer may be optional. For example, if the first functional layer and the light-emitting layer are formed from a polymer material, it may be desirable to form the second functional layer. The second functional layer may be a single layer or a multilayer. The second functional layer may include an Electron Transport Layer (ETL) and/or an Electron Injection Layer (EIL).

[0111] The counter electrode (230) may be composed of a conductive material with a relatively low work function. For example, the counter electrode (230) may include a (semi-)transparent layer comprising silver (Ag), magnesium (Mg), aluminum (Al), nickel (Ni), chromium (Cr), lithium (Li), calcium (Ca), or alloys thereof. Alternatively, the counter electrode (230) may further include a layer such as ITO, IZO, ZnO, or In_2O_3 on top of the (semi-)transparent layer comprising the aforementioned materials. In one embodiment, the counter electrode (230) may comprise silver (Ag) and magnesium (Mg).

[0112] A stacked structure comprising sequentially stacked pixel electrodes (210), an intermediate layer (220), and a counter electrode (230) can form a light-emitting diode, such as an organic light-emitting diode (OLED). The display layer (200), which includes a pixel circuit (PC), insulating layers, and an organic light-emitting diode (OLED), may be covered by a thin film encapsulation layer (TFE).

[0113] The thin film encapsulation layer (TFE) may include first and second inorganic encapsulation layers (310, 330) and an organic encapsulation layer (320) between them.

[0114] The first and second inorganic encapsulation layers (310, 330) may each include one or more inorganic insulators. Inorganic insulating materials may include aluminum oxide, titanium oxide, tantalum oxide, hafnium oxide, zinc oxide, silicon oxide, silicon nitride, and/or silicon oxynitride. The first and second inorganic encapsulation layers (310, 330) may be formed via chemical vapor deposition.

[0115] The organic encapsulation layer (320) may include a polymer-based material. Examples of polymer-based materials include acrylic resins, epoxy resins, polyimides, and polyethylene. For example, the organic encapsulation layer (320) may include acrylic resins, such as polymethyl methacrylate and polyacrylic acid. The organic encapsulation layer (320) may be formed by curing a monomer or by applying a polymer.

[0116] The thin film encapsulation layer (TFE) covers the entire display area (DA) and may be disposed so as to extend toward the peripheral area (NDA) to cover a portion of the peripheral area (NDA). The thin film encapsulation layer (TFE) may extend to the outer region of the drive voltage supply line (60).

[0117] The touch-sensing layer (TU) may include a first conductive layer (MTL1) and a second conductive layer (MTL2), which comprise sensing electrodes and/or trace lines, among other elements. A first insulating layer (410) is disposed between the thin film encapsulation layer (TFE) and the first conductive layer (MTL1), and a second insulating layer (420) may be disposed between the first conductive layer (MTL1) and the second conductive layer (MTL2).

[0118] The first conductive layer (MTL1) and the second conductive layer (MTL2) may include a conductive material. The conductive material may include molybdenum (Mo), aluminum (Al), copper (Cu), titanium (Ti), and the like, and may be formed as a multilayer or a single layer comprising the aforementioned materials. In some embodiments, the first conductive layer (MTL1) and the second conductive layer (MTL2) may have a structure in which a titanium layer, an aluminum layer, and a titanium layer are sequentially stacked (Ti/Al/Ti).

[0119] The first insulating layer (410) and the second insulating layer (420) may include inorganic insulators and/or organic insulators. Inorganic insulating materials may include silicon oxide,

silicon oxynitride, and silicon nitride. Organic insulating materials may include acrylic-based and imide-based organic compounds.

[0120] In FIG. 6, the second insulating layer (420) extends to the second partition wall (PW2); however, in other embodiments, the second insulating layer (420) may be disposed such that it extends past the bending area (BA) to cover a portion of the peripheral area (NDA).

[0121] The optical functional layer (OU) may be disposed on the input sensing layer (TU). The optical functional layer (OU) covers the second conductive layer (MTL2) and may include a first layer (510) disposed on the second insulating layer (420) and a second layer (520) disposed on the first layer (510).

[0122] An opening pattern (5100P) may be formed on the first layer (510) to correspond to the light-emitting area (EA). In one embodiment, the width of the opening pattern (5100P) may be larger than the width of the light-emitting area (EA) in the same direction. This opening pattern (5100P) is positioned in the light extraction direction of the pixel and can serve to improve light extraction efficiency by enhancing the straight-line propagation of light emitted from the light-emitting area (EA).

[0123] Meanwhile, to further improve the light extraction efficiency described above, a second layer (520) having a refractive index greater than that of the first layer (510) may be disposed on top of the first layer (510). The first layer (510) may comprise an insulating material having a first refractive index, and the second layer (520) may comprise an insulating material having a second refractive index.

[0124] The first refractive index of the first layer (510) may range from approximately 1.3 to approximately 1.6. In one embodiment, the first refractive index of the first layer (510) may range from

approximately 1.4 to approximately 1.55. The first layer (510) comprises, for example, ethylhexyl acrylate, pentafluoropropyl acrylate, poly(ethylene glycol) dimethacrylate, or ethylene glycol dimethacrylate. In one embodiment, the first layer (510) may include an acrylic-based organic material having a refractive index of approximately 1.5. In addition, the first layer (510) may be formed from a material that forms the organic encapsulation layer (320) of a thin film encapsulation (TFE) layer. In one embodiment, the first layer (510) may include an epoxy-based organic material and, in some cases, may also include a photopolymerizable material.

[0125] The second layer (520) may be a planarized insulating layer having a second refractive index. The second refractive index of the second layer (520) may range from approximately 1.65 to 1.85. The second layer (520) may include, for example, polydiarylsiloxane, methyltrimethoxysilane, or tetramethoxysilane. In one embodiment, the second layer (520) may comprise acrylic-based and/or siloxane-based organic materials having a refractive index of approximately 1.6. In another embodiment, the second layer (520) may include dispersed particles to increase the refractive index. For example, metal oxide particles such as zinc oxide (ZnO), titanium dioxide (TiO₂), zirconium dioxide (ZrO₂), and barium titanate (BaTiO₃) may be dispersed in the second layer (520).

[0126] The first layer (510) and the second layer (520) are arranged on the display area (DA) and may cover the entire display area (DA) while extending into the peripheral area (NDA). FIG. 6 illustrates the second layer (520) disposed so as to cover the bending area (BA); however, in other embodiments, the first layer (510) and the second layer (520) may be disposed so as to cover the bending area (BA).

As the second layer (520) extends past the bending area (BA) into the peripheral area (NDA), the upper surface (520_{us}) of the second layer (520) at the boundary between the display area (DA) and the peripheral area (NDA) can be configured to be generally flat.

[0127] By way of comparison, if the second layer (520) does not extend sufficiently into the peripheral area (NDA), a problem arises where spots are visible on the display panel due to the reflection of external light caused by variations in the thickness of the second layer (520) at the edges of the display area (DA). Therefore, in a display apparatus according to one embodiment of the present invention, the second layer (520) is extended sufficiently to the peripheral area (NDA) outside the display area (DA), so that the upper surface (520_{us}) at the boundary between the display area (DA) and the peripheral area (NDA) is generally flat, thereby minimizing thickness variations in the second layer (520); this effectively prevents the appearance of visible spots at the boundary between the display area (DA) and the peripheral area (NDA).

[0128] Meanwhile, referring to the peripheral area (NDA), a first partition wall (PW1) and a second partition wall (PW2) may be arranged on the peripheral area (NDA) adjacent to the display area (DA). The first partition wall (PW1) and the second partition wall (PW2) may be disposed so as to surround the display area (DA). Furthermore, the first partition wall (PW1) and the second partition wall (PW2) may be arranged at a distance from one another. A valley may be provided between the first partition wall (PW1) and the display area (DA), and another valley may be provided between the first partition wall (PW1) and the second partition wall (PW2). These first partition wall (PW1), second partition wall (PW2), and the valley structures formed thereby can serve to prevent the organic encapsulation layer (320) of the thin film encapsulation layer (TFE) from overflowing toward the edge

of the substrate (100). Therefore, the organic encapsulation layer (320) may be in contact with the inner surface of the first partition wall (PW1) facing the display area (DA). In this case, when it is stated that the organic encapsulation layer (320) is in contact with the inner surface of the first partition wall (PW1), it means that the first inorganic encapsulation layer (310) is positioned between the organic encapsulation layer (320) and the first partition wall (PW1), and the organic encapsulation layer (320) is understood to be in direct contact with this first inorganic encapsulation layer (310). The first inorganic encapsulation layer (310) and the second inorganic encapsulation layer (330) are disposed on the first partition wall (PW1) and the second partition wall (PW2), respectively, and may extend toward the edge of the substrate (100).

[0129] FIG. 6 illustrates a display apparatus equipped with a first partition wall (PW1) and a second partition wall (PW2); however, in other embodiments, the display apparatus may be configured to include only the first partition wall (PW1) or to include additional partition walls adjacent to the second partition wall (PW2). The first partition wall (PW1) includes a portion (117P1) of the second planarized insulating layer (117), a portion (119P1) of the pixel defining film (119), and a portion (121P1) of the spacer (121); and the second partition wall (PW2) includes a portion (116P2) of the first planarized insulating layer (116), a portion (117P2) of the second planarized insulating layer (117), a portion (119P2) of the pixel defining film (119), and a portion (121P) of the spacer (121). In another embodiment, the first partition wall (PW1) and the second partition wall (PW2) may further include portions of other layers, and some of these layers described above may be omitted.

[0130] A common voltage supply line (70) may be located on the outer side of the drive voltage supply line (60). The common voltage supply line (70) may extend from the lower portion of the first partition wall (PW1) to the second partition wall (PW2). The common voltage supply line (70) may be

electrically connected to the counter electrode (230) of the organic light-emitting diode (OLED) via a connecting electrode (72). In one embodiment, the common voltage supply line (70) is disposed on the same layer as the drive voltage supply line (60) and may include the same material as, for example, the electrode layer (120) of the thin-film transistor (TFT), and the connecting electrode (72) may include the same material as the pixel electrode (210) of the organic light-emitting diode (OLED).

[0131] The second layer (520) of the optical functional layer (OU) may extend into the peripheral area (NDA) and be disposed so as to overlap with the first partition wall (PW1) and the second partition wall (PW2).

[0132] As described above with reference to FIG. 5, the peripheral area (NDA) may include a bending area (BA) at least in part. The bending area (BA) may be disposed at a distance from the first partition wall (PW1) and the second partition wall (PW2).

[0133] The inorganic insulating layer (IOL) may include an opening (OP) corresponding to the bending area (BA). In other words, the inorganic insulating layer (IOL) disposed corresponding to the bending area (BA) may be removed from the bending area (BA). FIG. 6 illustrates that the inorganic insulating layer (IOL) corresponding to the bending area (BA) has been completely removed; however, in other embodiments, the barrier layer (110) or both the barrier layer (110) and the buffer layer (111) may remain partially or completely intact. Thus, by removing part or all of the inorganic insulating layer (IOL) located on the bending area (BA), crack propagation caused by the inorganic insulating layer (IOL) during bending of the substrate (100) can be prevented.

[0134] A first organic layer (710) may be arranged on the bending area (BA). The first organic layer (710) may comprise the same material as the planarized insulating layer (PIL). In one embodiment, the first organic layer (710) may comprise the same material as the first planarized insulating layer (116). Hereinafter, in this specification, when it is stated that “layer A” and “layer B” comprise the same material, this may mean that “layer A” and “layer B” are formed by the same process. Therefore, if the

first organic layer (710) comprises the same material as the first planarized insulating layer (116), the first organic layer (710) and the first planarized insulating layer (116) can be formed simultaneously. The first organic layer (710) may include a plurality of contact holes (FIG. 7, CH) penetrating the first organic layer (710).

[0135] Connection wiring (CW) may be arranged on the bending area (BA). The connection wiring (CW) may be electrically connected to the fan-out wiring (FW) shown in FIG. 5. The fan-out wiring (FW) may transmit data signals to each pixel via the connection wiring (CW) located on the bending area (BA).

[0136] In one embodiment, the fan-out wiring (FW) disposed in the peripheral area (NDA) other than the bending area (BA) may comprise the same material as the gate electrode (G) of the thin-film transistor (TFT) or the second electrode (CE2) of the storage capacitor (Cst). The connection wiring (CW) may be connected to the fan-out wiring (FW) through contact holes that penetrate a portion of the inorganic insulating layer (IOL).

[0137] The connection wiring (CW) may include a first metal pattern (MP1) disposed beneath the first organic layer (710), and a second metal pattern (MP2) disposed above the first organic layer (710) and electrically connected to the first metal pattern (MP1).

[0138] In one embodiment, the first metal pattern (MP1) may be disposed directly on the sloped surface (OP-S) and the lower surface (OP-B) of the opening (OP). When the first metal pattern (MP1) is disposed directly on the sloped surface (OP-S) and the lower surface (OP-B) of the opening (OP), the stress applied to the connection wiring (CW) can be reduced even if the neutral plane of the bending area (BA) is close to the surface of the substrate (100).

[0139] The first metal pattern (MP1) may comprise the same material as the electrode layer (120). When the first metal pattern (MP1) comprises the same material as the electrode layer (120), the first metal pattern (MP1) and the electrode layer (120) may be formed simultaneously.

[0140] In one embodiment, the second metal pattern (MP2) may be disposed offset from the first metal pattern (MP1) along a first direction (e.g., the y-direction). The second metal pattern (MP2) is disposed on the first organic layer (710) and is electrically connected to the first metal pattern (MP1) through a contact hole (FIG. 7, CH) penetrating the first organic layer (710). The second metal pattern (MP2) may comprise the same material as the contact metal (130). When the second metal pattern (MP2) comprises the same material as the contact metal (130), the second metal pattern (MP2) and the contact metal (130) may be formed simultaneously.

[0141] By disposing a first organic layer (710), which is an organic insulating material, between the first metal pattern (MP1) and the second metal pattern (MP2), the connection wiring (CW) can exhibit superior tensile strength compared to fan-out wiring (FW) disposed in the peripheral area (NDA) outside the bending area (BA).

[0142] The buried organic layer (720) is disposed on the connection wiring (CW) corresponding to the opening (OP) and may fill at least a portion of the opening (OP). The buried organic layer (720) can reduce the stress applied to the connection wiring (CW). Furthermore, by adjusting the thickness and modulus of the buried organic layer (720), it is possible to control the position of the stress-neutral plane in the multilayer structure—which includes the substrate (100), connection wiring (CW), and other components—within the bending area (BA).

[0143] The buried organic layer (720) may comprise the same material as the second planarized insulating layer (117). When the buried organic layer (720) comprises the same material as the second

planarized insulating layer (117), the buried organic layer (720) and the second planarized insulating layer (117) may be formed simultaneously.

[0144] A detailed description of section E—which includes the connection wiring (CW), the first organic layer (710), and the buried organic layer (720) within the bending area (BA)—is continued in the description of FIG. 7.

[0145] The ends of the first inorganic encapsulation layer (310) and the second inorganic encapsulation layer (330) of the thin film encapsulation layer (TFE), as well as the end of the first insulating layer (410) of the input sensing layer (TU), may extend to the buried organic layer (720). In one embodiment, the edges of the first inorganic encapsulation layer (310), the second inorganic encapsulation layer (330), and the first insulating layer (410) may be disposed across the buried organic layer (720) or located on top of the buried organic layer (720). A stress-relief layer (800) may be disposed on the second layer (520) of the optical functional layer (OU). The stress-relief layer (800) is disposed corresponding to the bending area (BA) and may include an organic insulating material. The stress-relief layer (800) can alleviate stress applied to the bending area (BA) by shifting the neutral plane of the bending area (BA) upward, thereby compensating for the modulus of the layers disposed corresponding to the bending area (BA).

[0146] The upper surface (520us') of the second layer (520) disposed beneath the stress-relief layer (800) may be configured to be sloped. The second layer (520) is formed of an organic insulating material and has a thickness that gradually decreases toward its ends; the upper surface (520us') of the second layer (520) corresponding to the bending area (BA) is a portion of the display panel (DP) that is not visible to the user, so even if the upper surface (520us') of the second layer (520) is configured at an angle, no stains are visible.

[0147] A pad section (PD) may be located at the edge of the peripheral area (NDA) of the substrate (100). The pad section (PD) may include pads for connecting to the terminal section (40) and

the data driver (50) shown in FIG. 5. In one embodiment, the pads may each be configured as a dual layer comprising a first pad metal (PM1) and a second pad metal (PM2). For example, the first pad metal (PM1) may comprise the same material as the gate electrode (G), and the second pad metal (PM2) may comprise the same material as the fan-out wiring (FW) or contact metal (130); however, the present invention is not necessarily limited thereto. In FIG. 6, the pad section (PD) is shown as being fully exposed on the inorganic insulating layer (IOL), but its edges may be covered by the insulating layer.

[0148] Meanwhile, the control dam (CD) may be disposed on the peripheral area (NDA) on the outer side of the bending area (BA). The second layer (520) may be controlled by the control dam (CD). The control dam (CD) may be disposed between the bending area (BA) and the pad section (PD) to prevent the second layer (520) from extending to the pad section (PD). Since the pad section (PD) must be connected to an integrated circuit and/or a printed circuit board, the second layer (520) may be disposed so as not to overlap with the pad section (PD).

[0149] In one embodiment, the control dam (CD) is arranged on the inorganic insulating layer (IOL) and may comprise the same material as the first layer (510) of the optical functional layer (OU). As described above, since the second layer (520) is controlled by the control dam (CD), the second layer (520) may be configured so as not to extend beyond the control dam (CD). The control dam (CD) may include a first dam (CD1) and a second dam (CD2) arranged at a mutual distance from each other. The width of the first dam (CD1) and the width of the second dam (CD2) may be the same or may differ from each other.

[0150] FIG. 7 is a plan view showing a magnified and schematic representation of a portion of FIG. 6, such as section E.

[0151] Referring to FIG. 7, as described above, the first metal pattern (MP1) may be arranged directly on the sloped surface (OP-S) and the lower surface (OP-B) of the opening (OP). The first metal

pattern (MP1) may include a plurality of metal islands (MI) disposed along a first direction (e.g., the y-direction). The plurality of metal islands (MI) may be spaced apart at a constant interval (d).

[0152] The first organic layer (710) is disposed on the first metal pattern (MP1). The first organic layer (710) may expose at least a portion of each metal island (MI) through contact holes (CH) penetrating the first organic layer (710). In one embodiment, the first organic layer (710) may be disposed to cover the edges (MI-E) of each metal island.

[0153] The upper surface of the first organic layer (710) may have convex and concave portions. In one embodiment, the first organic layer (710) may have a wavy upper surface that is at its lowest height at the contact holes (CH) and becomes higher as it moves away from the contact holes (CH).

[0154] The second metal pattern (MP2) may be disposed offset from the first metal pattern (MP1) along a first direction (e.g., the y-direction). The second metal pattern (MP2) may include a plurality of mutually spaced metal bridges (MB). The plurality of metal bridges (MB) may connect adjacent metal islands (MI) to one another along the first direction (e.g., the y-direction).

[0155] In one embodiment, the adjacent first metal island (MI1) and second metal island (MI2) may be connected by a first metal bridge (MB1). One end (EP1) of the first metal bridge (MB1) may abut the exposed surface of the first metal island (MI1), and the other end (EP2) may abut the exposed surface of the second metal island (MI2).

[0156] The second metal pattern (MP2) is disposed on the first organic layer (710) and may have a shape corresponding to the upper surface of the first organic layer (710). In one embodiment, when the first organic layer (710) has a wavy upper surface, the second metal pattern (MP2) takes on a wavy shape corresponding to the upper surface of the first organic layer (710), thereby increasing flexibility.

[0157] The buried organic layer (720) is disposed on the connection wiring (CW) corresponding to the opening (OP) and may fill at least a portion of the opening (OP). In one embodiment, a first height (h1) from the lower surface (OP-B) of the opening (OP) to the upper surface of the buried organic layer (720) may be greater than a second height (h2) from the lower surface (OP-B) of the opening (OP) to the upper surface of the inorganic insulating layer (IOU). By adjusting the thickness and modulus of the buried organic layer (720) in this manner, the neutral plane of the bending area (BA) can be controlled to be located near the connection wiring (CW).

[0158] A second layer (520) of the optical functional layer (OU) may be directly disposed on the buried organic layer (720). The second layer (520) extends to the peripheral area (NDA) so as to cover the bending area (BA), thereby preventing the appearance of visible spots at the boundary between the display area (DA) and the peripheral area (NDA). Furthermore, by being disposed on the bending area (BA), the position of the neutral plane of the bending area (BA) can be controlled, thereby alleviating the stress applied to the connection wiring (CW).

[0159] FIG. 8a through FIG. 8d are cross-sectional views that schematically show an enlarged portion of a display apparatus according to one embodiment of the present invention. FIG. 8a through FIG. 8d show an enlarged view of the region including the pad section (PD) along the C-C' line in FIG. 6, and some of them correspond to modified examples.

[0160] Referring to FIG. 8a, the first organic layer (710) may comprise the same material as the first planarized insulating layer (FIG. 6, 116), and the buried organic layer (720) may comprise the same material as the second planarized insulating layer (FIG. 6, 117).

[0161] Since the presence of an inorganic layer above the bending area (BA) may cause cracks, the ends of the first inorganic encapsulation layer (310), the second inorganic encapsulation layer (330), and the first insulating layer (410) may be disposed so as not to extend beyond the bending area (BA). In one embodiment, the first inorganic encapsulation layer (310), the second inorganic encapsulation layer (330), and the first insulating layer (410) may be disposed to cover a portion of the upper surface of the buried organic layer (720), but they do not extend to the upper surface of the buried organic layer (720) corresponding to the bending area (BA).

[0162] The first layer (510) of the optical functional layer (OU) may be disposed such that it extends past the bending area (BA) to cover a portion of the peripheral area (NDA). That is, the first layer (510) may be disposed to cover the buried organic layer (720). In this case, the end of the second insulating layer (420) of the input sensing layer (TU) may be disposed so as not to extend beyond the ends of the first inorganic encapsulation layer (310), the second inorganic encapsulation layer (330), and the first insulating layer (410). Therefore, the first layer (510) may be disposed directly on the buried organic layer (720), and the second layer (520) may be disposed on the first layer (510).

[0163] Referring to FIG. 8b, when the second insulating layer (420) comprises an organic insulating material, the second insulating layer (420) may be disposed such that it extends past the bending area (BA) to cover a portion of the peripheral area (NDA). That is, the second insulating layer (420) may be disposed directly on top of the buried organic layer (720) so as to cover it. The first layer (510) is disposed on top of the second insulating layer (420), and a second layer (520) may be disposed on top of the first layer (510).

[0164] Referring to FIG. 8c, a second organic layer (730) may be disposed on top of the buried organic layer (720). The second organic layer (730) may comprise the same material as the pixel-defining film (FIG. 6, 119). When the second organic layer (730) comprises the same material as the

pixel-defining film (FIG. 6, 119), the second organic layer (730) may be formed simultaneously with the pixel-defining film (FIG. 6, 119).

[0165] The third height (h3) from the lower surface (OP-B) of the opening (OP) to the upper surface of the second organic layer (730) may be greater than the second height (h2) from the lower surface (OP-B) of the opening (OP) to the upper surface of the inorganic insulating layer (IOU). By adjusting the thickness and modulus of each of the buried organic layer (720) and the second organic layer (730), the position of the neutral plane in the bending area (BA) can be easily controlled. The buried organic layer (720) and the second organic layer (730) may form a third partition wall (PW3).

[0166] The ends of the first inorganic encapsulation layer (310) and the second inorganic encapsulation layer (330) of the thin film encapsulation layer (TFE), as well as the end of the first insulating layer (410) of the input sensing layer (TU), may extend to the third partition wall (PW3). In one embodiment, the edges of the first inorganic encapsulation layer (310), the second inorganic encapsulation layer (330), and the first insulating layer (410) may be disposed across the third partition wall (PW3) or located on top of the third partition wall (PW3).

[0167] In one embodiment, the first layer (510) of the optical functional layer (OU) may be disposed so that it extends past the third partition wall (PW3) to cover a portion of the peripheral area (NDA). In another embodiment, the second insulating layer (420) of the input sensing layer (TU) may be disposed such that it extends past the third partition wall (PW) to cover a portion of the peripheral area (NDA). In yet another embodiment, the second insulating layer (420) and the first layer (510) may be disposed such that they extend past the third partition wall (PW3) to cover a portion of the peripheral area (NDA). In yet another embodiment, the second insulating layer (420) and the first layer (510) may be disposed so as not to extend beyond the bending area (BA), and thus may not cover the third partition wall (PW3).

[0168] Referring to FIG. 8d, a plurality of organic layers may be further disposed on the third

partition wall (PW3). For example, a third organic layer (740) may be further disposed on top of the second organic layer (730). In this case, the third organic layer (740) may include the same material as the spacer (21), but is not limited thereto.

[0169] When the second insulating layer (420) comprises an organic insulating material, the second insulating layer (420) may be disposed such that it extends past the bending area (BA) to cover a portion of the peripheral area (NDA). That is, the second insulating layer (420) may be disposed so as to cover the third organic layer (740). A first layer (510) may be disposed on top of the second insulating layer (420), and a second layer (520) may be disposed on top of the first layer (510).

[0170] Therefore, the buried organic layer (720), the second organic layer (730), the third organic layer (740), the first layer (510), or the second layer (520), which can be disposed on the bending area (BA), can be formed simultaneously during the process of forming the stacked structure of the display area (DA), without the need for any separate additional processes.

[0171] Referring to FIG. 8e, the first insulating layer (410) and the second insulating layer (420) may include an organic insulating material. When the first insulating layer (410) and the second insulating layer (420) include organic insulating material, the first insulating layer (410) may be disposed such that it extends past the bending area (BA) to cover a portion of the peripheral area (NDA). The second insulating layer (420) may be disposed on top of the first insulating layer (410). The first layer (510) may be disposed on top of the second insulating layer (420).

[0172] In FIG. 8e, a buried organic layer (720), a second organic layer (730), and a third organic layer (740) are shown stacked and disposed on the bending area (BA); however, the first insulating layer (410) and second insulating layer (420) described above, first layer (510), and second layer (520) described above can be applied equally even when only the buried organic layer (720) is disposed on

the bending area (BA), or when the buried organic layer (720) and the second organic layer (730) are stacked and disposed there.

[0173] Meanwhile, as shown in FIG. 8a through FIG. 8e, a stress-relief layer (800) may be disposed on the second layer (520) corresponding to the bending area (BA). the buried organic layer (720), the second organic layer (730), the third organic layer (740), the second insulating layer (420), the first layer (510), the second layer (520), and the stress-relief layer (800)—specifically by adjusting the thickness and modulus of the layers disposed over the bending area (BA)—the position of the stress-neutral plane in the multilayer structure, which includes the substrate (100) and connection wiring (CW) in the bending area (BA), can be easily controlled. By combining these layers to position the stress-neutral plane near the connection wiring (CW) in the bending area (BA), the stress applied to the connection wiring (CW) in the bending area (BA) can be minimized.

[0174] In one embodiment, the stress-relief layer (800) may include an organic insulating material, such as polyimide, epoxy resin, acrylic resin, polyester, photoresist, polyacrylic resins, polyimide resins, polyamide resins, siloxane resins, as well as elastic materials such as silicone, urethane, and thermoplastic polyurethane. Furthermore, the width of the stress-relief layer (800) may be formed to be generally equal to or greater than the width of the bending area (BA), taking the width of the bending area (BA) into account, and may, for example, be provided with a width of 40 mm to 60 mm. Furthermore, the thickness of the stress-relief layer (800) may be formed to be approximately 100 μm to 140 μm ; however, this may vary depending on the location of the stress-neutral plane of the laminates on the bending area (BA).

[0175] FIG. 9 is a cross-sectional view schematically illustrating a portion of a display apparatus according to one embodiment of the present invention.

[0176] FIG. 9 is similar to FIG. 6 but may further include a third flattening insulation layer (118). Additionally, it differs from FIG. 6 described above in terms of the relationship between the first organic layer (710), the buried organic layer (720), and the connection wiring (CW) in the bending area (BA). Since the other configurations are identical to the embodiment shown in FIG. 6, the following description will focus on the differences.

[0177] Referring to FIG. 9, in the display area (DA), a third planarized insulating layer (118) is disposed on top of the second planarized insulating layer (117). A first contact metal (120-1) may be disposed on the second planarized insulating layer (117), and a second contact metal (120-2) may be disposed on the third planarized insulating layer (118). The electrode layer (120) and the pixel electrode (210) may be electrically connected via the first contact metal (120-1) and the second contact metal (120-2).

[0178] The buried organic layer (720) may be disposed beneath the connection wiring (CW) corresponding to the opening (OP). The buried organic layer (720) may fill at least a portion of the opening (OP). In one embodiment, the upper surface of the buried organic layer (720) is disposed higher than the upper surface of the inorganic insulating layer (IOL), thereby controlling the position of the neutral plane of the bending area (BA) and the connection wiring (CW).

[0179] The buried organic layer (720) may comprise the same material as the planarized insulating layer (PIL). In one embodiment, the buried organic layer (720) may consist of a single layer. In this case, the buried organic layer (720) may comprise the same material as the first planarized insulating layer (116), the second planarized insulating layer (117), or the third planarized insulating layer (118).

[0180] In another embodiment, the buried organic layer (720) may comprise multiple layers. As shown in FIG. 9, the buried organic layer (720) may comprise a first buried layer (720-1) and a second buried layer (720-2) disposed on top of the first buried layer (720-1).

[0181] The first buried layer (720-1) may comprise the same material as the first planarized insulating layer (116); in this case, the second buried layer (720-2) may comprise the same material as the second planarized insulating layer (117) or the third planarized insulating layer (118). In another embodiment, the first buried layer (720-1) may comprise the same material as the second planarized insulating layer (117), and the second buried layer (720-2) may comprise the same material as the third planarized insulating layer (118).

[0182] In one embodiment, the upper surface of the second buried layer (720-2) is disposed higher than the upper surface of the inorganic insulating layer (IOL), thereby allowing control over the neutral plane of the bending area (BA) and the position of the connection wiring (CW).

[0183] The first metal pattern (MP1) of the connection wiring (CW) may be disposed on the buried organic layer (720). As shown in FIG. 8, if a second buried layer (720-2) is further included, the first metal pattern (MP1) may be disposed on the second buried layer (720-2).

[0184] In one embodiment, the first metal pattern (MP1) may comprise the same material as the first contact metal (130-1). When the first metal pattern (MP1) comprises the same material as the first contact metal (130-1), the first metal pattern (MP1) and the first contact metal (130-1) may be formed simultaneously. In another embodiment, the first metal pattern (MP1) may comprise the same material as the second contact metal (130-2). When the first metal pattern (MP1) comprises the same material as the second contact metal (130-2), the first metal pattern (MP1) and the second contact metal

(130-2) can be formed simultaneously.

[0185] A first organic layer (710) is formed on the first metal pattern (MP1). The first organic layer (710) may expose at least a portion of each of the first metal patterns (MP1) through contact holes (FIG. 10, CH). The first organic layer (710) may comprise the same material as the pixel defining film (119). When the first organic layer (710) comprises the same material as the pixel defining film (119), the first organic layer (710) may be formed simultaneously with the pixel defining film (119).

[0186] A second metal pattern (MP2) may be disposed on the first organic layer (710). The second metal pattern (MP2) may be electrically connected to the first metal pattern (MP1) through contact holes (FIG. 10, CH) that penetrate the first organic layer (710). The second metal pattern (MP2) may comprise the same material as the first conductive layer (MTL1) of the input sensing layer (TU). When the second metal pattern (MP2) comprises the same material as the first conductive layer (MTL1), the second metal pattern (MP2) may be formed simultaneously with the first conductive layer (MTL1).

[0187] FIG. 10 is a plan view schematically showing an enlarged portion of FIG. 9, for example, portion F.

[0188] Referring to FIG. 10, as described above, the first metal pattern (MP1) may be disposed on the second buried layer (720-2). In another embodiment, if the second buried layer (720-2) does not exist, the first metal pattern (MP1) may be disposed on the first buried layer (720-1).

[0189] The first metal pattern (MP1) may include a plurality of metal islands (MI) disposed along a first direction (e.g., the y-direction).

[0190] The first organic layer (710) is disposed on the first metal pattern (MP1). The first organic layer (710) covers the edges (MI-E) of the metal islands (MI) and may be in contact with the second buried layer (720-2). The upper surface of the first organic layer (710) may have convex and concave portions. In one embodiment, the first organic layer (710) may have a wavy upper surface that is lowest at the contact hole (CH) and becomes higher as it moves away from the contact hole (CH).

[0191] The second metal pattern (MP2) may be disposed offset from the first metal pattern (MP1) along a first direction (e.g., the y-direction). The second metal pattern (MP2) may include a plurality of mutually spaced metal bridges (MB). The plurality of metal bridges (MB) may connect adjacent metal islands (MI) to one another along the first direction (e.g., the y-direction).

[0192] The second metal pattern (MP2) is disposed on the first organic layer (710) and may have a shape corresponding to the upper surface of the first organic layer (710). In one embodiment, when the first organic layer (710) has a wavy upper surface, the second metal pattern (MP2) takes on a wavy shape corresponding to the upper surface of the first organic layer (710), thereby increasing flexibility.

[0193] In one embodiment, a second layer (520) of the optical functional layer (OU) may be directly disposed on the second metal pattern (MP2). The second layer (520) extends to the peripheral area (NDA) so as to cover the bending area (BA), thereby preventing the appearance of smudges at the boundary between the display area (DA) and the peripheral area (NDA). Furthermore, by being disposed on the bending area (BA), it can alleviate the stress applied to the bending area (BA).

[0194] FIG. 11 is a cross-sectional view schematically showing an enlarged portion of a display apparatus according to one embodiment of the present invention. FIG. 11 shows an enlarged view of the region containing the pad section (PD) along the C-C' line in FIG. 9.

[0195] Referring to FIG. 11, the second insulating layer (420) of the input sensing layer (TU) and the first layer (510) of the optical function layer (OU) may be disposed to extend through the bending area (BA) and cover a portion of the peripheral area (NDA). When the second insulating layer (420) comprises an organic insulating material, the second insulating layer (420) and the first layer (510) may be arranged to cover the connection wiring (CW) and the first organic layer (710). In another embodiment, when the first insulating layer (410) and the second insulating layer (420) comprise an organic insulating material, the first insulating layer (410), the second insulating layer (420), and the first layer (510) may be arranged to cover the connection wiring (CW) and the first organic layer (710). In yet another embodiment, the leading edge of the second insulating layer (420) may be positioned so as not to extend beyond the leading edges of the first inorganic encapsulation layer (310), the second inorganic encapsulation layer (330), and the first insulating layer (410), and the first layer (510) may be disposed to extend past the bending area (BA) and cover a portion of the peripheral area (NDA). A second layer (520) may be disposed on top of the first layer (510).

[0196] Meanwhile, as shown in FIGS. 10 and 11, a stress-relief layer (800) may be further disposed on top of the second layer (520) corresponding to the bending area (BA).

[0197] The first buried layer (720-1), the second buried layer (720-2), the second insulating layer (420), the first layer (510), the second layer (520), and the stress-relief layer (800)—specifically, the layers disposed over the bending area (BA)—it is possible to control the position of the stress-neutral plane in the multilayer structure, which includes the substrate (100), connection wiring (CW), and other components, within the bending area (BA).

[0198] FIG. 12a through FIG. 12d are schematic plan views showing enlarged portions of FIG. 5, such as section D, and FIG. 13 corresponds to a cross-section taken along line G-G' in FIG. 12a through FIG. 12d.

[0199] Referring to FIG. 12a and FIG. 13, the inorganic insulating layer (IOL) has an opening (OP) corresponding to the bending area (BA). The opening (OP) has a sloped surface (OP-S) and a lower surface (OP-B). Connection wiring (CW) is disposed on the opening (OP) along a first direction (e.g., the y-direction).

[0200] A first metal pattern (MP1) of the connection wiring (CW) is disposed on the opening (OP). In one embodiment, the first metal pattern (MP1) may be disposed directly on the sloped surface (OP-S) and the lower surface (OP-B) of the opening (OP). In another embodiment, the first metal pattern (MP1) may be disposed on an organic layer that fills at least a portion of the opening (OP).

[0201] A first metal pattern (MP1) may include a plurality of metal islands (MI) disposed at intervals along a first direction (e.g., the y-direction). The plurality of metal islands (MI) disposed along the first direction (e.g., the y-direction) may form discontinuous lines (L1), and the discontinuous lines may be disposed at intervals from one another along the second direction (e.g., the x-direction).

[0202] The first organic layer (710) exposes at least a portion of each of the first metal patterns (MP1) and may be disposed on the first metal patterns (MP1). The first organic layer (710) may include contact holes (CH) that penetrate the first organic layer (710) to expose at least a portion of each of the first metal patterns (MP1). In this case, the first organic layer (710) may be disposed so as to cover the edges of each of the first metal patterns (MP1).

[0203] The first organic layer (710) may form convex and concave portions. In one embodiment, the first organic layer (710) may have a wavy upper surface that is at its lowest height at the contact hole (CH) and becomes higher as it moves away from the contact hole (CH).

[0204] The second metal pattern (MP2) may be disposed on the first organic layer (710) along a first direction (e.g., the y-direction). The second metal pattern (MP2) may have a shape corresponding to the upper surface of the first organic layer (710). In one embodiment, when the first organic layer (710) has a wavy upper surface, the second metal pattern (MP2) takes on a wavy shape corresponding to the upper surface of the first organic layer (710), thereby increasing flexibility. The second metal pattern (MP2) may be disposed offset from the first metal pattern (MP1) along a first direction (e.g., the y-direction).

[0205] The second metal pattern (MP2) may include a plurality of mutually spaced metal bridges (MB). The multiple metal bridges (MB) may connect adjacent metal islands to one another along a first direction (e.g., the y-direction). In one embodiment, one end of a metal bridge (MB1) may be connected to a single metal island (MI1), and the other end may be connected to another metal island (MI2) adjacent to the metal island (MI1). Two metal bridges (MB1, MB2) that meet at a contact hole (CH1) exposing a single metal island (MI1) may be disposed at a distance from one another. In another embodiment, the ends of the two metal bridges (MB1, MB2) that meet at a contact hole (CH1) exposing a single metal island (MI1) may be disposed adjacent to one another.

[0206] Thus, since the connection wiring (CW) is configured to include a second metal pattern (MP2) that connects the first metal pattern (MP1) to the first metal pattern (MP1), stress applied to the connection wiring (CW) during bending of the substrate (100) can be reduced, thereby preventing cracks in the connection wiring (CW).

[0207] By way of comparison, if the connection wiring consists of a single continuous metal layer, stress applied across the entire length of the connection wiring during substrate bending may cause a crack to form at a single point along the connection wiring.

[0208] Referring to FIG. 12b, the second metal pattern (MP2) includes first bridges (MP2-1) and second bridges (MP2-2) that are spaced apart and arranged side by side around metal islands (MI). In one embodiment, the first bridges (MP2-1) and the second bridges (MP2-2) may be spaced apart and arranged parallel to a discontinuous line (L1) formed by the metal islands (MI). At a contact hole (CH1) exposing a single metal island (MI1), two bridges (MB1-1, MB2-1) that constitute the first bridges (MP2-1) and the two bridges (MB1-2, MB2-2) that constitute the second bridges (MP2-2) may meet the metal island (MI1) at multiple points.

[0209] Since the second metal pattern (MP2) forms multiple contacts with the first metal pattern (MP1), it can have at least two electrical paths. Therefore, even if cracks or breaks occur in the metal bridges (MB) that make up the second metal pattern (MP2), other electrical paths can be maintained.

[0210] Referring to FIG. 12c, the spacing between the first bridges (MP2-1) and the second bridges (MP2-2) may vary depending on their location. In one embodiment, the spacing (wl) between the first metal bridge (MB1-1) and the second metal bridge (MB1-2) at the contact hole (CH1) may be

smaller than the spacing (w_2) on the first organic layer (710). Since the metal bridges (MB) constituting the second metal pattern (MP2) have a curved shape, the tensile strength of the connection wiring (CW) can be further enhanced.

[0211] FIG. 12d differs from FIG. 12c described above in the shape of the contact holes (CH) in the first organic layer (710).

[0212] Referring to FIG. 12d, the first organic layer (710) may include contact holes (CH) that expose the center of each first metal pattern (MP1). As shown, the contact holes (CH) may be formed in various shapes, such as circular, square, or rhombic. In this case, the first organic layer (710) may form convex and concave portions. In one embodiment, the first organic layer (710) may have an upper surface with a wave-like shape, where the height is lowest at the contact holes (CH) and increases as the distance from the contact holes (CH) increases. As described above, the first organic layer (710) may be disposed so as to cover the edges of each of the first metal patterns (MP1).

[0213] The structure of the first organic layer (710) in this embodiment can be applied identically to all of the embodiments described above in FIG. 10a through FIG. 10c.

[0214] Although the present invention has been described with reference to the embodiments shown in the drawings, these are merely illustrative, and those skilled in the art will understand that various modifications and other equivalent embodiments are possible. Therefore, the true scope of protection of the present invention should be determined by the technical concepts set forth in the appended claims.

[Description of Symbols]

[0215] 100: substrate

DA: display area

NDA: peripheral area

BA: bending area

PD: pad section

DU: display layer

TU: input sensing layer

OU: optical functional layer

CU: anti-reflective layer

CD: control dam

510: first layer

520: second layer

710: first organic layer

720: buried organic layer

730: second organic layer

CW: connection wiring

MP1: first metal pattern

MP2: second metal pattern

800: stress-relief layer

[What is claimed is]

[Claim 1]

A display apparatus, comprising: a substrate including a display area, a peripheral area that surrounds the display area and extends on one side thereof, and a bending area in which at least a portion of the peripheral area is bent; an inorganic insulating layer disposed on the substrate so as to overlap the display area and the peripheral area, and having an opening corresponding to the bending region; a pixel circuit disposed on the display area; a display element disposed on the pixel circuit; contact metal electrically connecting the pixel circuit and the display element; an optical functional layer comprising a first layer disposed on the display element and having an opening corresponding to the display element, and a second layer disposed on the first layer, extending into the peripheral area, and covering the bending area; a pad section disposed at the end of the peripheral area; a first organic layer disposed on the bending area; and connection wiring extending from the display area through the bending area to the pad section, at least a portion of which comprises the same material as the contact metal; wherein the connection wiring comprises a first metal pattern disposed beneath the first organic layer; and a second metal pattern disposed on top of the first organic layer and electrically connected to the first metal pattern through contact holes penetrating the first organic layer.

[Claim 2]

The display apparatus of claim 1, wherein the opening has an inclined surface and a lower surface, and at least a portion of the connection wiring is arranged in contact with the inclined surface and the lower surface.

[Claim 3]

The display apparatus of claim 1, further comprising: a planarized insulating layer disposed on the pixel circuit, wherein the planarized insulating layer comprises a first planarized insulating layer and a second planarized insulating layer disposed on the first planarized insulating layer, and wherein the first organic layer comprises the same material as the first planarized insulating layer.

[Claim 4]

The display apparatus of claim 3, further comprising a buried organic layer disposed on the connection wiring corresponding to the opening and filling at least a portion of the opening.

[Claim 5]

The display apparatus of claim 1, wherein the first height—measured from the lower surface of the opening to the upper surface of the buried organic layer—is greater than the second height—measured from the lower surface of the opening to the upper surface of the inorganic insulating layer.

[Claim 6]

The display apparatus of claim 4, wherein the buried organic layer comprises the same material as the second planarized insulating layer.

[Claim 7]

The display apparatus of claim 3, further comprising: a second organic layer disposed on the buried organic layer corresponding to the opening.

[Claim 8]

The display apparatus of claim 7, wherein the third height—measured from the lower surface of the opening to the upper surface of the second organic layer—is greater than the second height—measured from the lower surface of the opening to the upper surface of the inorganic insulating layer.

[Claim 9]

The display apparatus of claim 7, further comprising: a pixel-defining film disposed on the flattening insulating layer and defining a light-emitting area through an opening; and wherein the second organic layer comprises the same material as the pixel-defining film.

[Claim 10]

The display apparatus of claim 1, further comprising: a planarized insulating layer disposed on the pixel circuit; a pixel-defining film disposed on the planarized insulating layer and defining a light-emitting area through an opening; and a buried organic layer disposed beneath the connection wiring corresponding to the opening and filling at least a portion of the opening; wherein the first organic layer comprises the same material as the pixel-defining film, and the buried organic layer comprises the same material as the planarized insulating layer.

[Claim 11]

The display apparatus of claim 1, wherein the pixel circuit comprises a thin-film transistor and a storage capacitor; the thin-film transistor comprises a semiconductor layer, a gate electrode that at least partially overlaps the semiconductor layer, and an electrode layer on the gate electrode; the first metal pattern comprises the same material as the electrode layer; and the second metal pattern comprises the same material as the contact metal.

[Claim 12]

The display apparatus of claim 1, comprising: an input sensing layer disposed on the display element, wherein the input sensing layer comprises a first insulating layer, a first conductive layer, a second conductive layer, and a second insulating layer disposed between the first conductive layer and the second conductive layer; wherein the first metal pattern comprises the same material as the contact metal, and the second metal pattern comprises the same material as the first conductive layer.

[Claim 13]

The display apparatus of claim 12, wherein the first layer is disposed so as to cover the bending area.

[Claim 14]

The display apparatus of claim 13, comprising: an input sensing layer disposed on the display element, wherein the input sensing layer comprises a first insulating layer, a first conductive layer, a second conductive layer, and a second insulating layer disposed between the first conductive layer and the second conductive layer, wherein the second insulating layer comprises an organic insulating material and is disposed so as to cover the bending area.

[Claim 15]

The display apparatus of claim 14, wherein the first insulating layer comprises an organic insulating material and is disposed so as to cover the bending area.

[Claim 16]

The display apparatus of claim 1, further comprising: a stress-relief layer disposed on the optical functional layer corresponding to the bending area.

[Claim 17]

The display apparatus of claim 1, wherein the first metal pattern is disposed along a first direction, and the first organic layer exposes at least a portion of each of the first metal patterns through the contact holes.

[Claim 18]

The display apparatus of claim 17, wherein the first organic layer is disposed so as to cover the edges of each of the first metal patterns.

[Claim 19]

The display apparatus of claim 17, wherein the second metal pattern is disposed offset from the first metal pattern along the first direction.

[Claim 20]

The display apparatus of claim 17, wherein the first metal pattern comprises a plurality of mutually spaced metal islands, the second metal pattern comprises a plurality of mutually spaced metal bridges, and the metal islands are connected to one another by the metal bridges.

[Claim 21]

The display apparatus of claim 17, wherein one end of the metal bridge is connected to a single metal island, and the other end is connected to another metal island adjacent to the metal island.

[Claim 22]

The display apparatus of claim 21, wherein the metal bridges include first bridges and second bridges that are spaced apart and arranged in a row around the metal islands.

[Summary]

[Abstract]

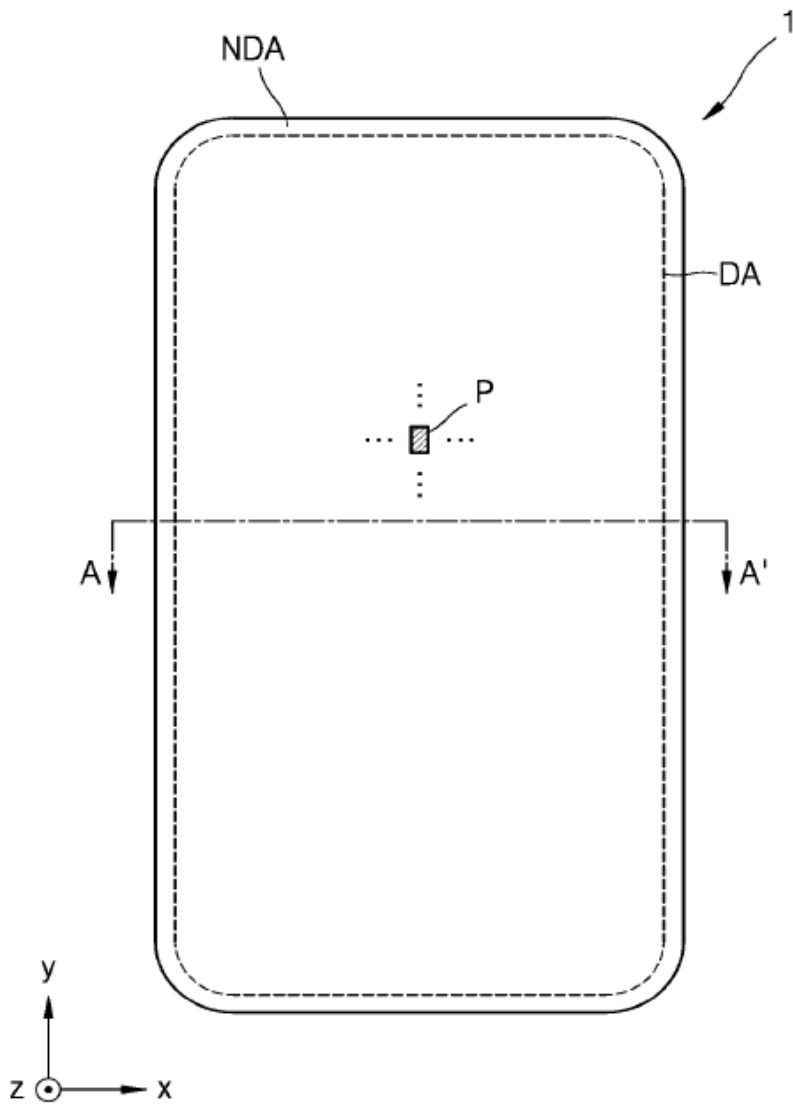
The present invention provides a display apparatus comprising: a substrate that includes a display area, a peripheral area surrounding the display area and extending on one side thereof, and a bending area in which at least a portion of the peripheral area is bent, in order to provide a display apparatus with improved wiring crack resistance in the bending area; an inorganic insulating layer disposed on the substrate so as to overlap the display area and the peripheral area, and having an opening corresponding to the bending area; a pixel circuit disposed on the display area; a planarized insulating layer disposed on the pixel circuit; a pad section disposed at the end of the peripheral area; and a first organic layer disposed on the bending area, the first organic layer comprising the same material as the planarized insulating layer; and connection wiring extending from the display area through the bending area to the pad section; wherein the connection wiring comprises a first metal pattern disposed beneath the first organic layer; and a second metal pattern disposed on top of the first organic layer and electrically connected to the first metal pattern through contact holes penetrating the first organic layer.

[Representative Drawings]

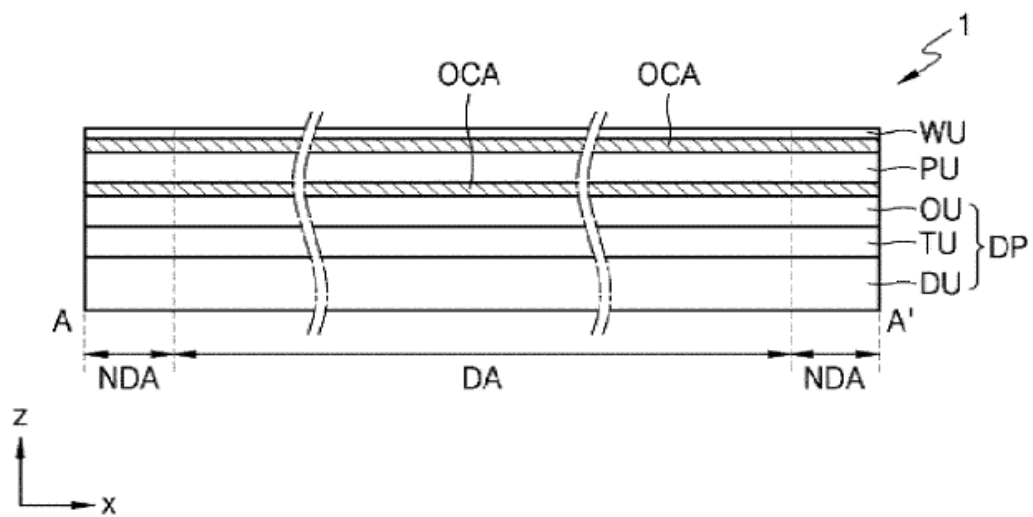
FIG. 6

[Drawings]

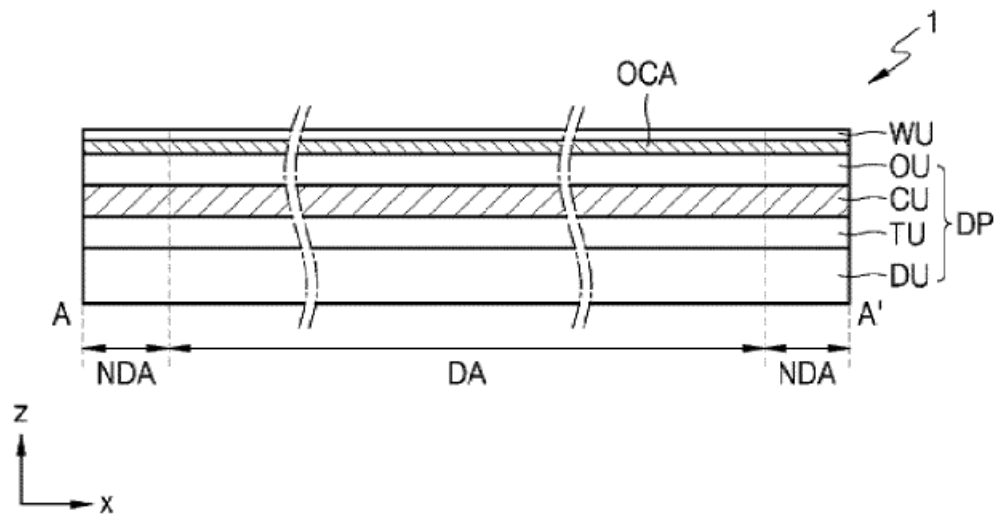
[FIG. 1]



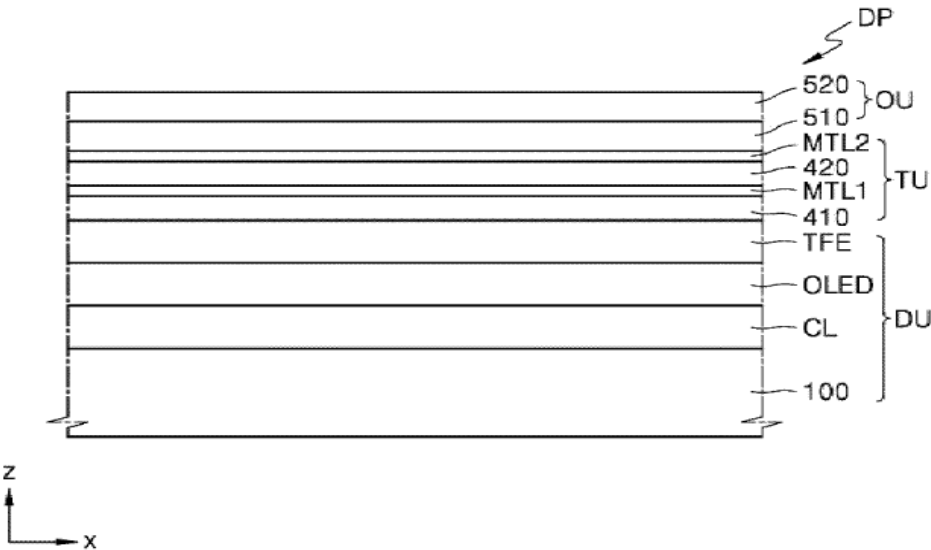
[FIG. 2]



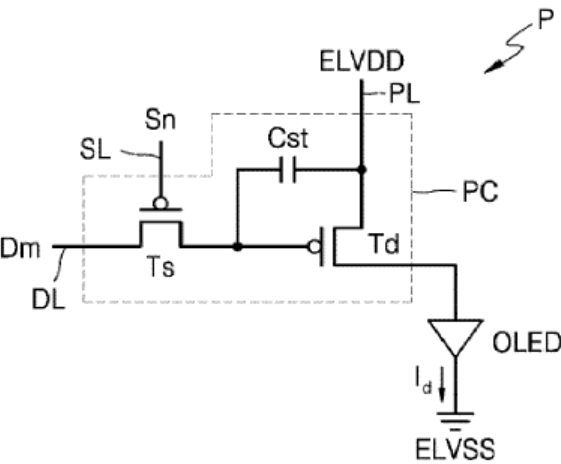
[FIG. 2b]



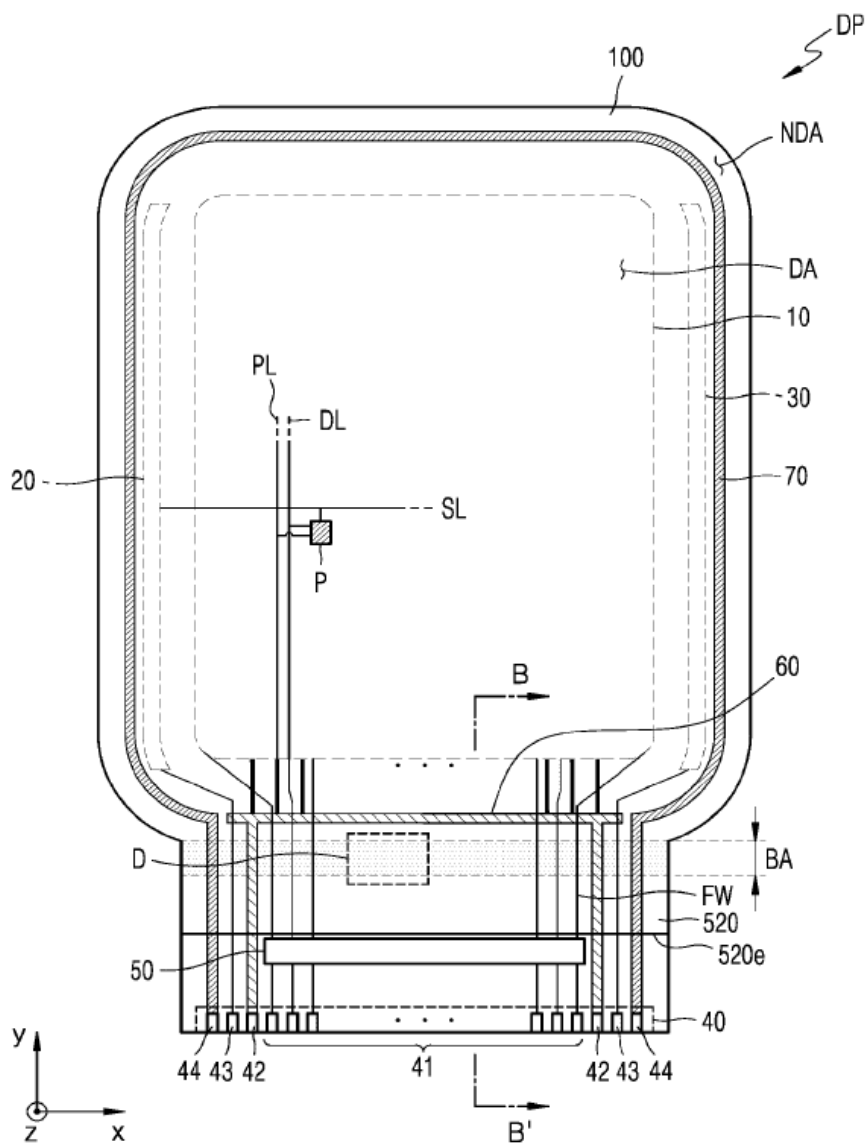
[FIG. 3]



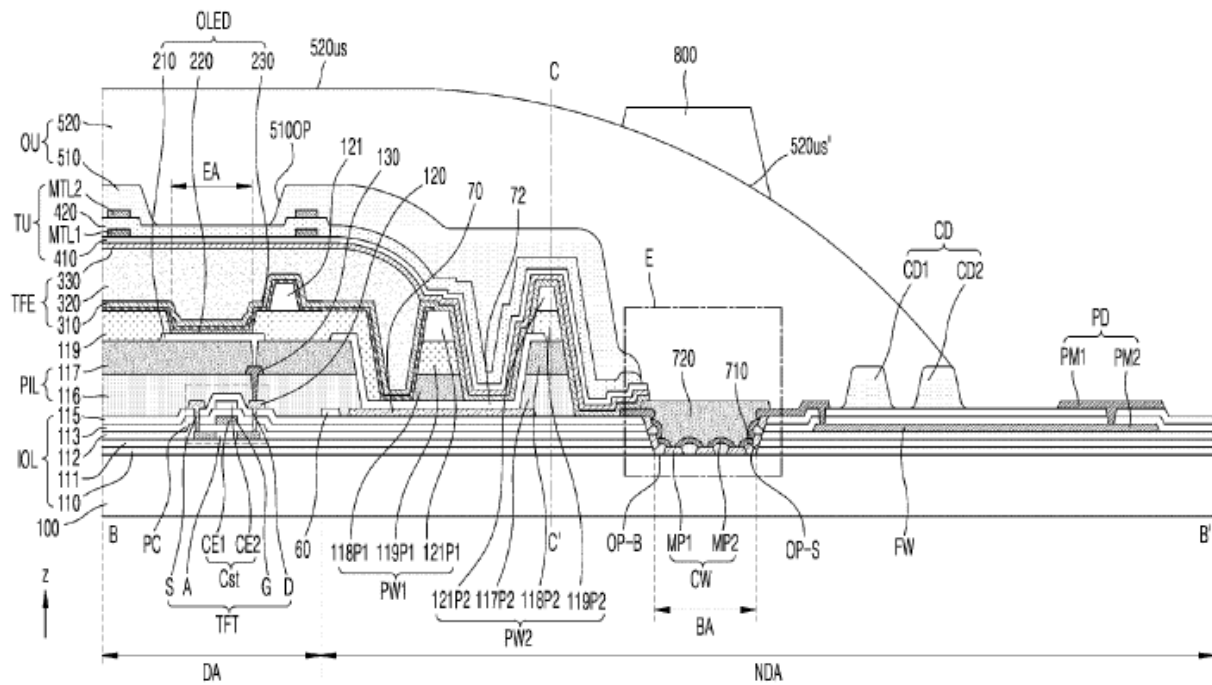
[FIG. 4]



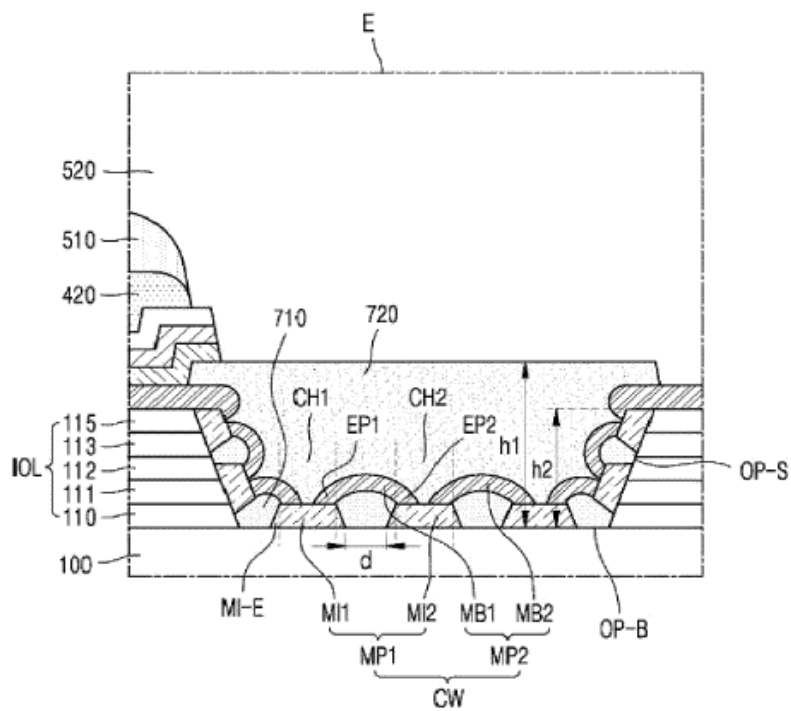
[FIG. 5]



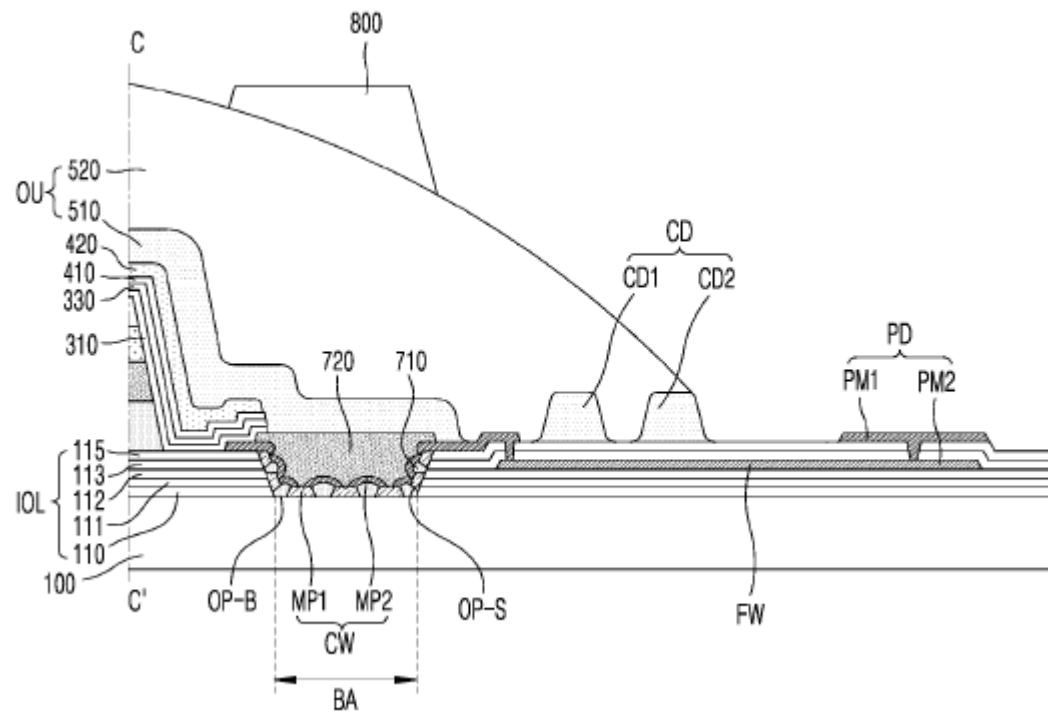
[FIG. 6]



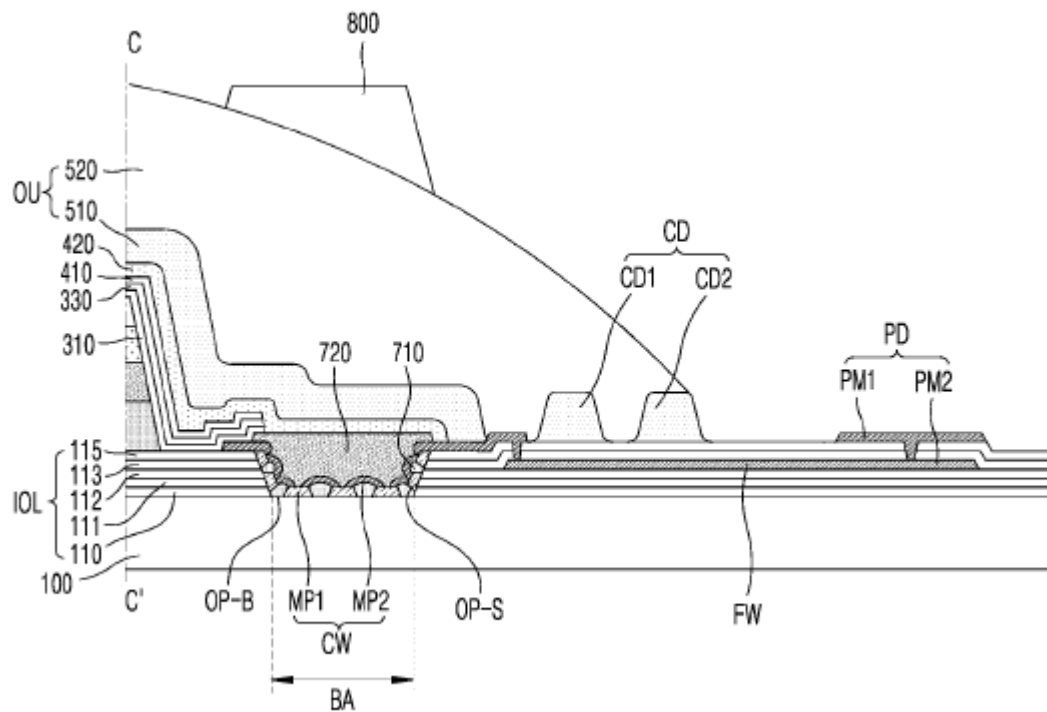
[FIG. 7]



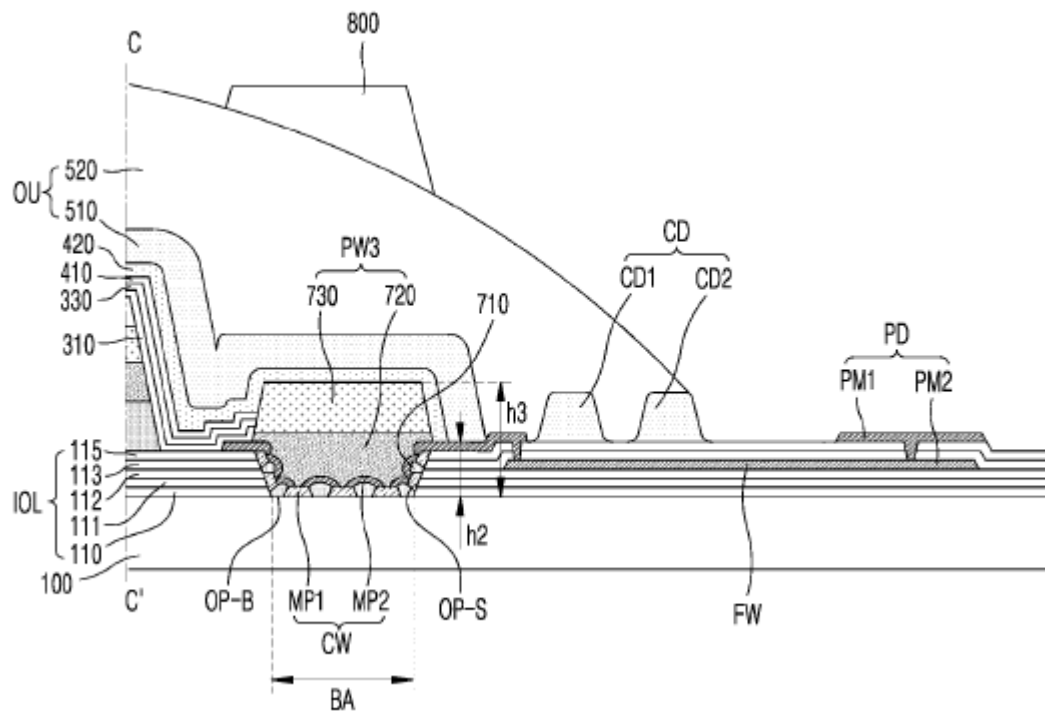
[FIG. 8a]



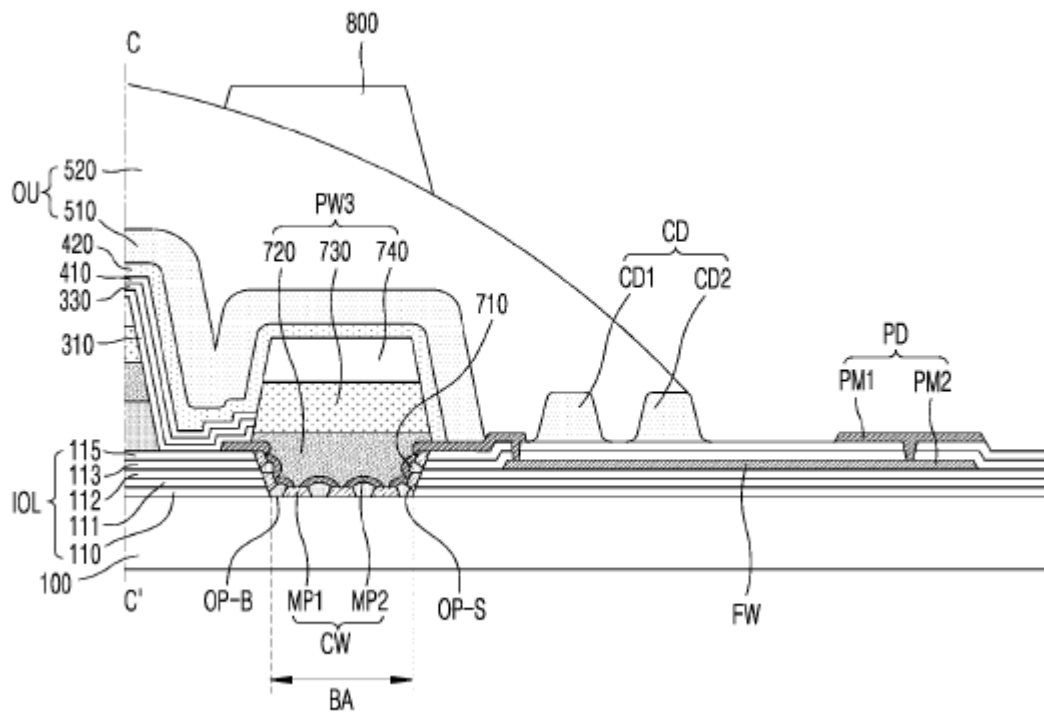
[FIG. 8b]



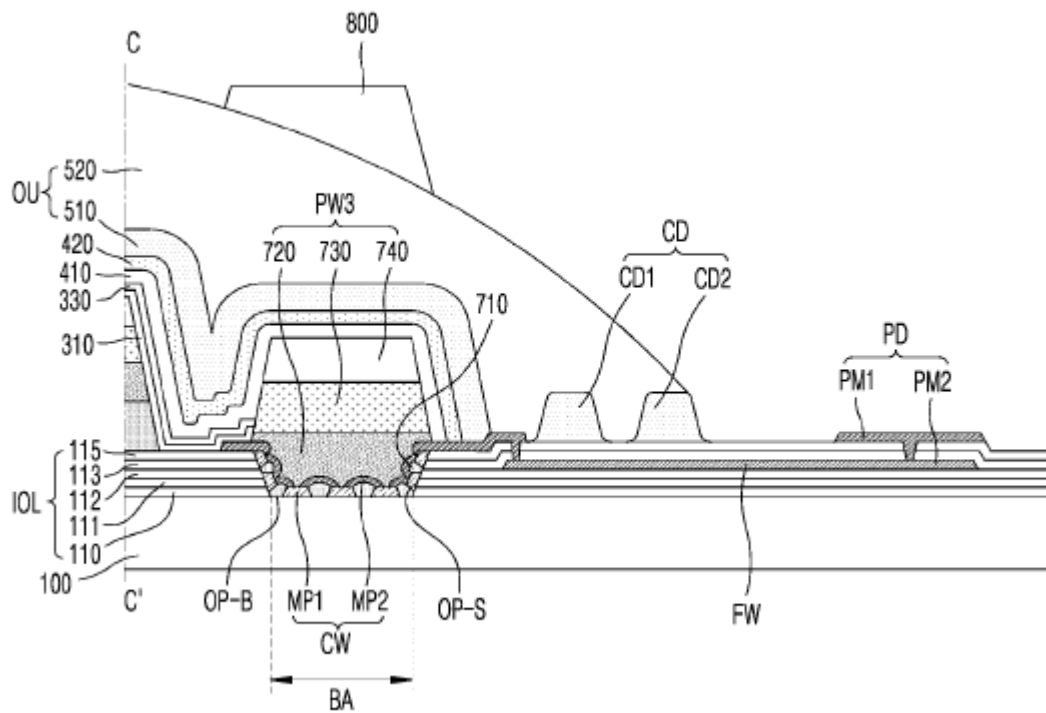
[FIG. 8c]



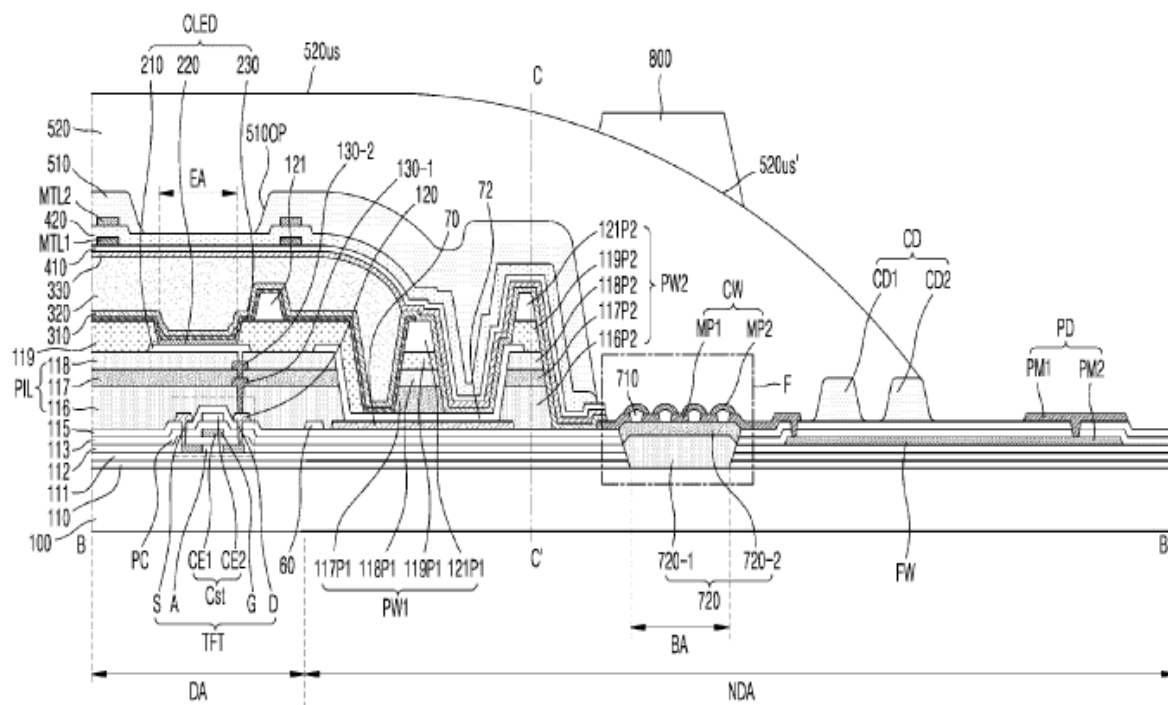
[FIG. 8d]



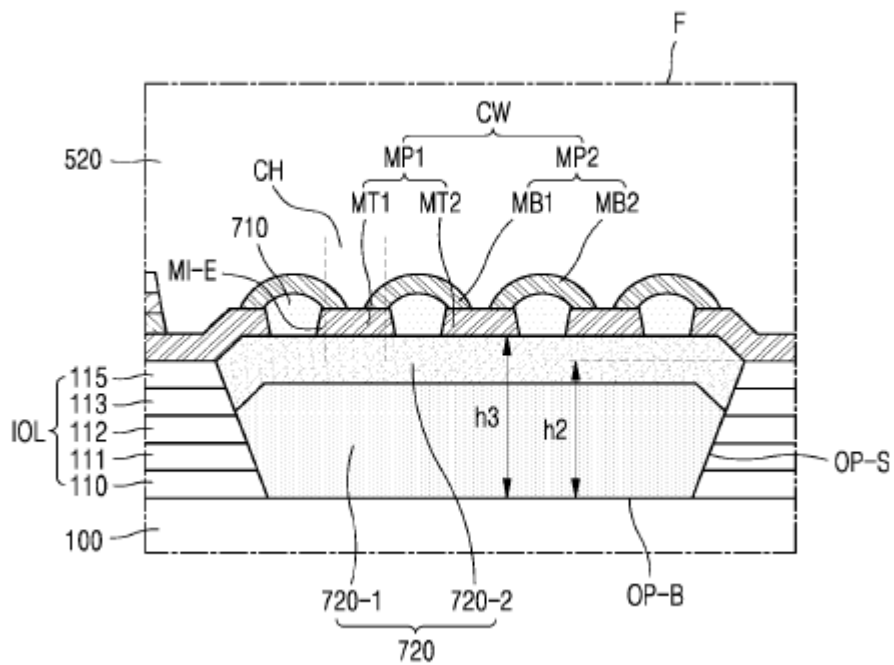
[FIG. 8e]



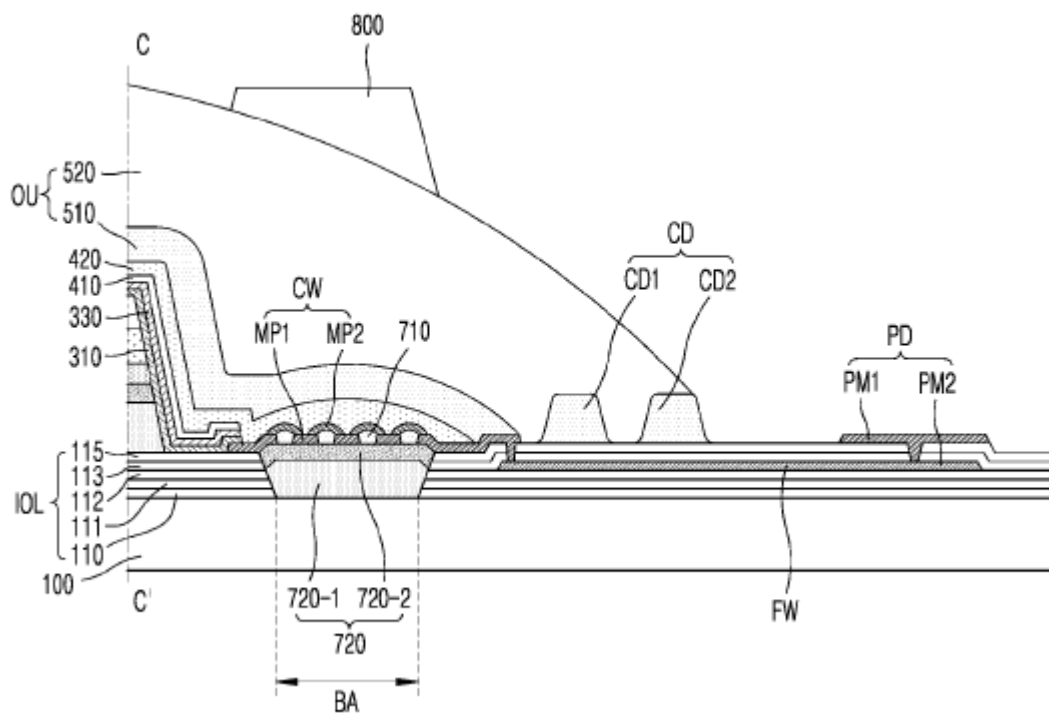
[FIG. 9]



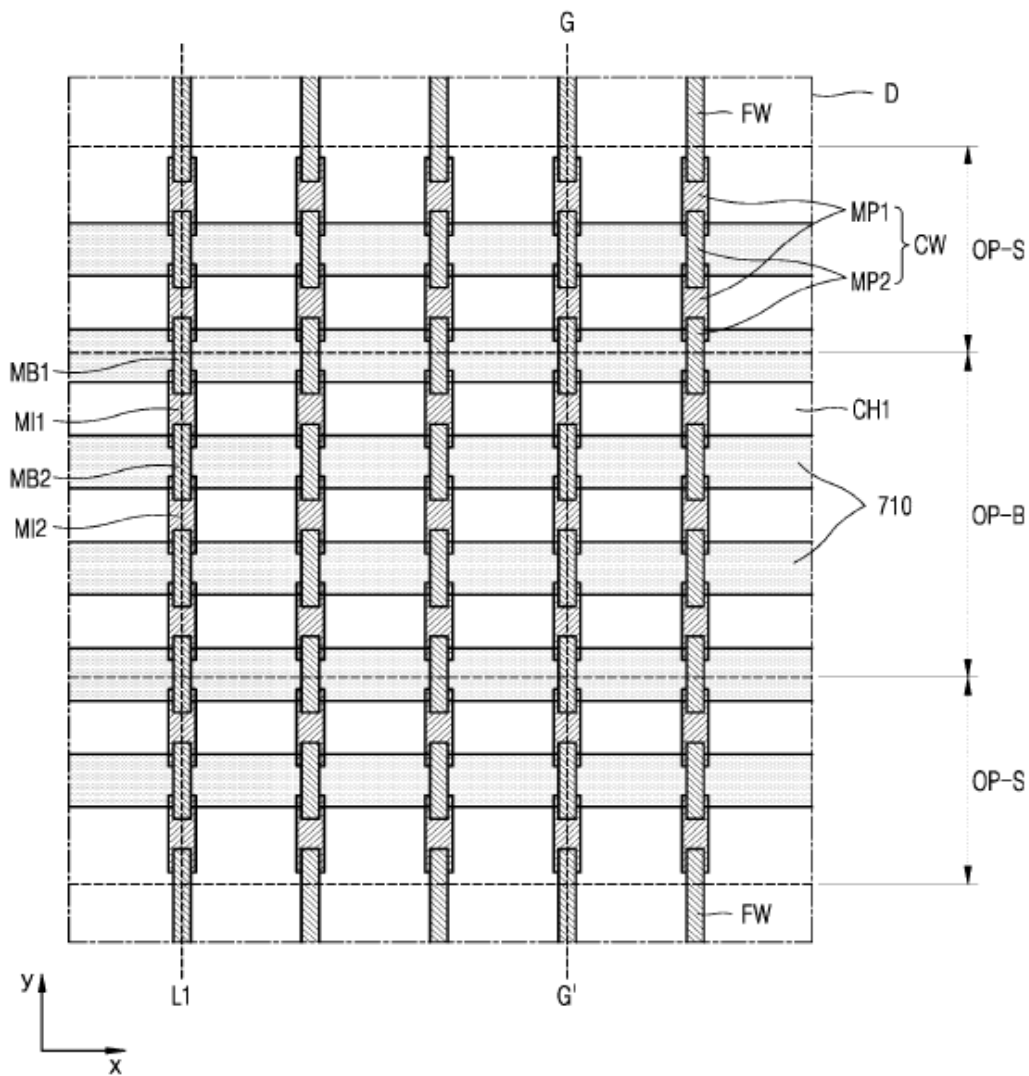
[FIG. 10]



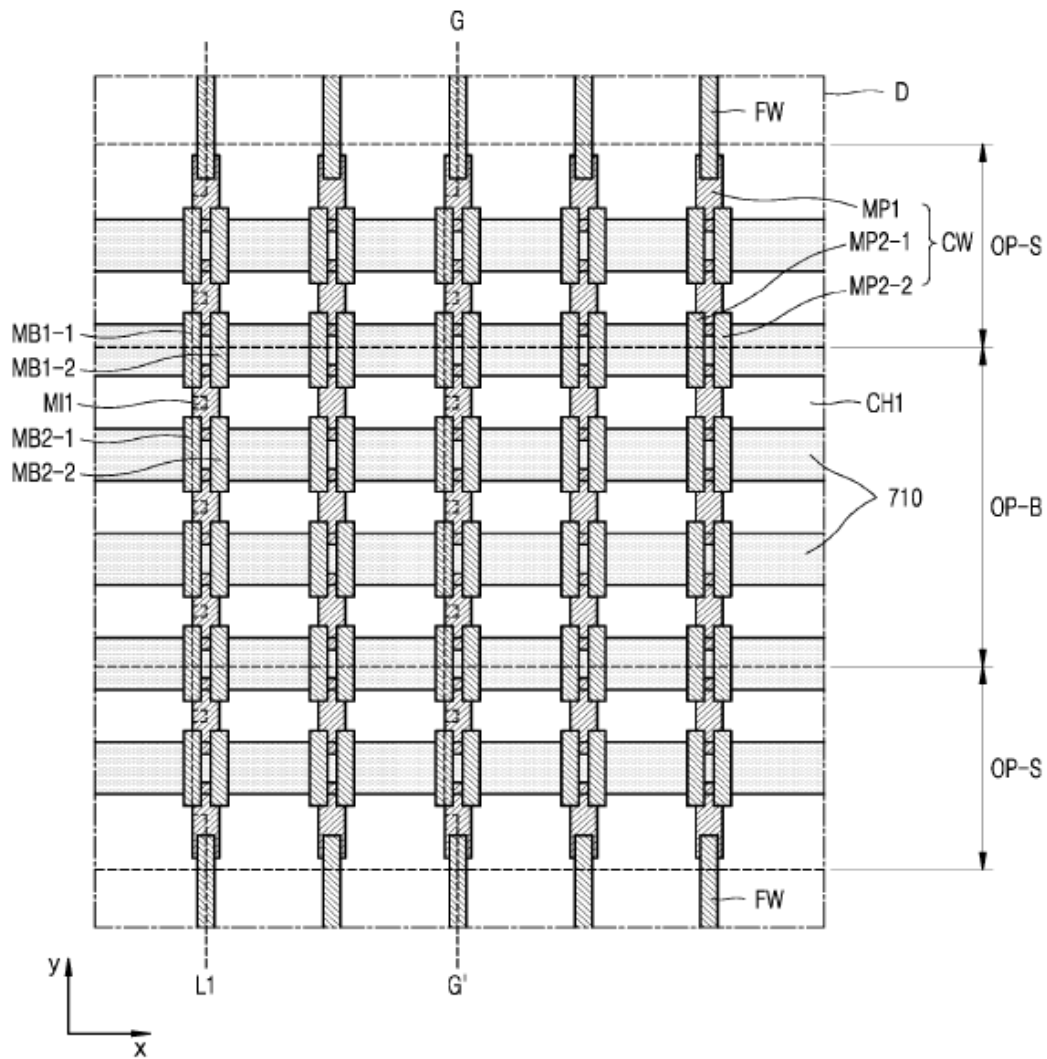
[FIG. 11]



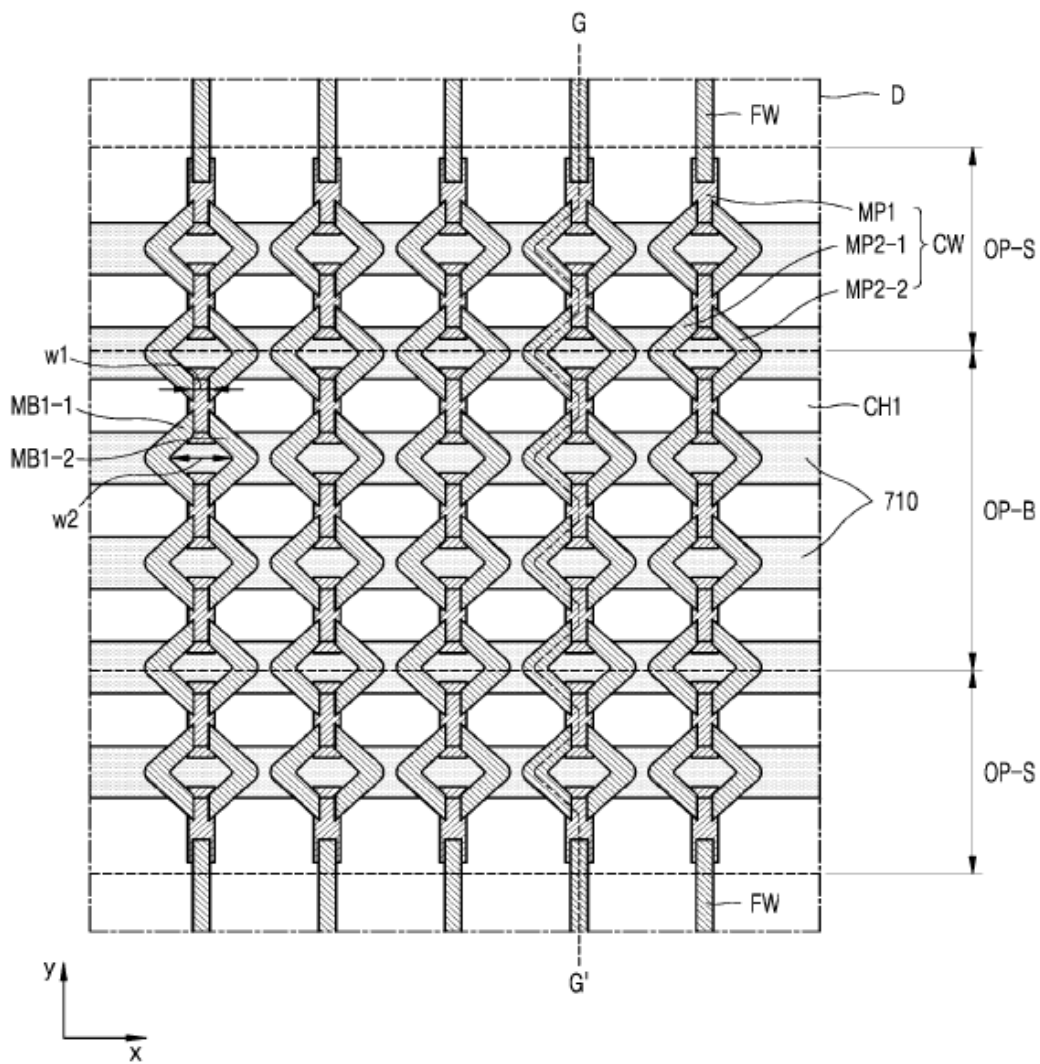
[FIG. 12a]



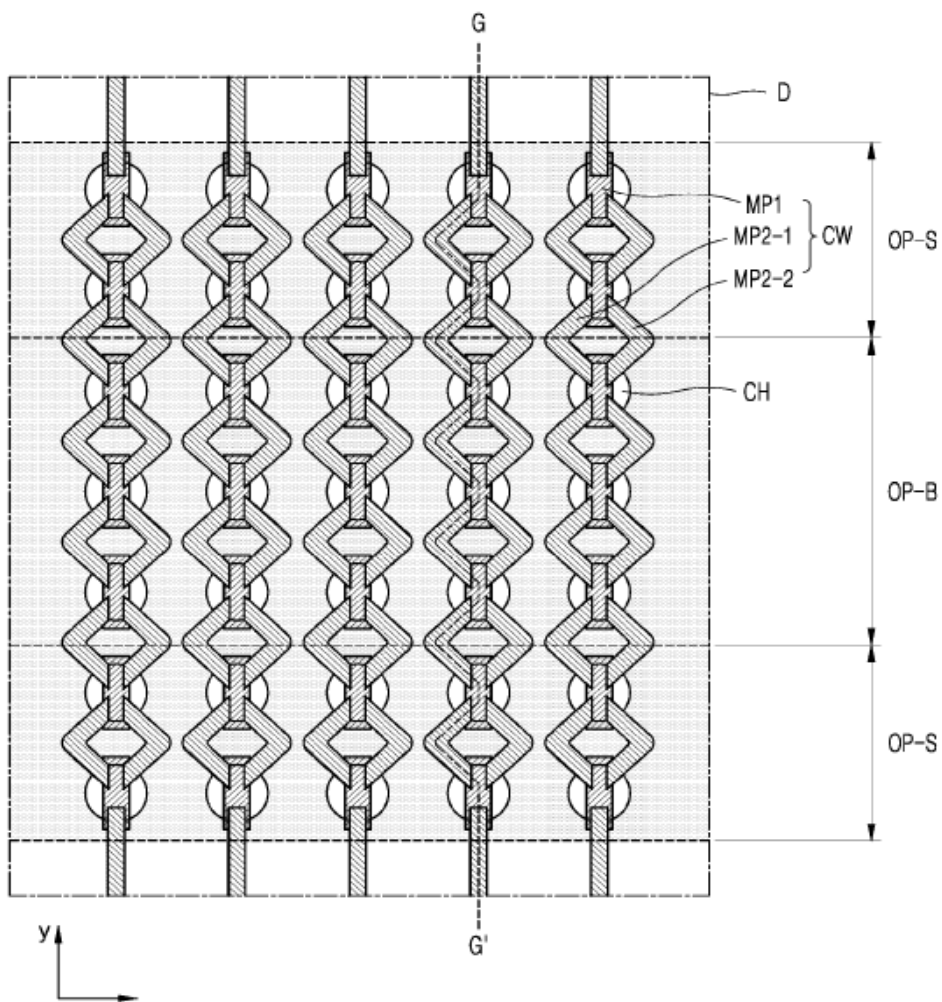
[FIG. 12b]



[FIG. 12c]



[FIG. 12d]



[FIG. 13]

