

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD.,
Petitioner

v.

WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY
TECHNOLOGY CO., LTD.
Patent Owner.

Case No. IPR2026-00487
U.S. Patent No. 12,133,429

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 12,133,429**

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LIST OF EXHIBITS¹

Ex. No.	Description
Ex-1001	U.S. Patent No. 12,133,429 (“the ’429 Patent”)
Ex-1002	Declaration of Dr. Michael Lebby
Ex-1003	Curriculum Vitae of Dr. Michael Lebby
Ex-1004	Prosecution History of U.S. Patent No. 12,133,429
Ex-1005	U.S. Patent No. 11,963,404 to Yi <i>et al.</i> (“Yi1”)
Ex-1006	U.S. Patent Application Publication No. 2022/0199741 to Yi <i>et al.</i> (“Yi2”)
Ex-1007	U.S. Patent No. 9,658,523 to Zhang <i>et al.</i> (“Zhang”)
Ex-1008	U.S. Patent No. 7,335,912 to Park <i>et al.</i> (“Park”)
Ex-1009	Takatoshi Tsujimura, <i>OLED Display Fundamentals and Applications</i> (2d ed., John Wiley & Sons, Inc. 2017).
Ex-1010	<i>Organic Light-Emitting Diodes (OLEDs): Materials, Devices and Applications</i> (Alastair Buckley ed., Woodhead Publishing Ltd. 2013).
Ex-1011	<i>Flexible Flat Panel Displays</i> (Gregory P. Crawford ed., John Wiley & Sons, Ltd. 2005).
Ex-1012	Stanley Wolf, <i>Silicon Processing for the VLSI Era, Volume 4: Deep-Submicron Process Technology</i> (Lattice Press 2002).
Ex-1013	Claim mapping table for the ’429 Patent

¹ Four-digit pin citations that begin with 0 are to the branded numbers added by Samsung in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

I. INTRODUCTION

Samsung Display Co., Ltd. (“Petitioner”) requests *inter partes* review (“IPR”) of Claims 1–20 of U.S. Patent No. 12,133,429 (“the ’429 Patent”) (Ex-1001), currently assigned to Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd. (“Patent Owner” or “PO”).

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Petitioner maintains that Petitioner Samsung Display Corporation is the only real party-in-interest in this proceeding. Specifically, petitioner maintains for example that its corporate parent, Samsung Electronics Ltd. does not fund or have the ability to control this proceeding. *See Sun Pharmaceutical Industries, Inc. v. Biofrontera*, PGR2026-00021, Paper 12 (PTAB May 26, 2026). However, out of an abundance of caution and based on the Board’s recent precedent, Petitioner identifies Samsung Electronics Ltd. as its corporate parent.

Related Matters: PO has asserted the ’429 Patent against Petitioner in *Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd. v. Samsung Display Co., Ltd. et al.*, 2:26-cv-228 (E.D. Tex.).

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III. FEE AUTHORIZATION

The United States Patent and Trademark Office is authorized to charge any fees due during this proceeding to Deposit Account No. LA500639.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '429 Patent is available for review, and Petitioner is not barred or estopped from requesting review.

V. PRECISE RELIEF REQUESTED

Petitioner requests review and cancellation of Claims 1–20 as unpatentable based on the following grounds, supported by a declaration from Dr. Michael Lebby. *See* Ex-1002 ¶¶1-177 (citing Ex-1001, Exs-1004–1013); Ex-1003.

Ground	Summary
1	Claims 1–5, 9, and 11–15 are rendered obvious by Yi1
2	Claims 7–8 and 17–18 are rendered obvious by Yi1 in view of Yi2
3	Claims 6 and 16 are rendered obvious by Yi1 in view of Zhang
4	Claims 10 and 20 are rendered obvious by Yi1 in view of Yi2 and Park

VI. THE CHALLENGED PATENT

U.S. Patent No. 12,133,429 (the “’429 Patent”) (Ex-1001) is titled “Display Panel and Display Device,” names Xing Wu as its sole inventor, and is assigned to Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd. Ex-1001, Cover. The ’429 Patent issued on October 29, 2024, from U.S. Application No. 17/764,557, which is the U.S. national stage of PCT Application No. PCT/CN2022/082256, filed March 22, 2022, and claims priority to Chinese Application No. 202210237733.1, filed March 11, 2022. Ex-1001, Cover, 1:5–11. The ’429 Patent contains 20 claims. Independent Claim 1 is directed to a display panel, and Claim 11 is directed to a display device comprising the display panel of Claim 1, “wherein the display panel is an organic light-emitting diode (OLED) panel.” Ex-1001, 8:62–9:20, 10:43–45. Dependent Claims 2–10 and 12–20 largely mirror one another, reciting parallel panel and device limitations. Ex-1002, ¶¶52–53.

The '429 Patent concedes that OLED panels and bottom shielding metals were already known in the art. It acknowledges that OLED screens “are currently widely used and have advantages of light weight and high color gamut value.” Ex-1001, 1:21–23; Ex-1002, ¶54. But the patent asserts that substrates “adopting organic flexible substrates[] are affected by interfaces between the substrates and inorganic layers,” such that OLED screens “are prone to have problems such as screen afterimages, initial drops, and poor service life.” Ex-1001, 1:23–27. To reduce that influence, the '429 Patent admits, “more and more of the OLED screens adopt bottom shielding metals to shield pixel driving circuits at the interfaces between the substrates and the inorganic layers.” Ex-1001, 1:28–31. The '429 Patent thus identifies only a narrow alleged problem with these known bottom shielding metals: in order to link to power supply lines, prior bottom shielding metals had “serrated edges,” and electro-static discharge (ESD) explosions were “likely to occur at tips of serrations, thereby affecting a display effect.” Ex-1001, 1:31–35; Ex-1002, ¶55.

The '429 Patent's purported solution is a display panel having a display region and a non-display region, comprising: a substrate; a shielding layer located on the substrate that includes a plurality of shielding blocks and a converging wire electrically connected to the shielding blocks and located on at least one side of them; a pixel driving circuit layer located on the shielding layer, whose pixel

driving circuits each at least partially overlap a corresponding one of the shielding blocks; and a plurality of power supply lines disposed on a side of the shielding layer away from the substrate and electrically connected to the converging wire through a plurality of through holes—wherein the converging wire between two adjacent through holes is disposed according to a shortest distance between the two adjacent through holes. Ex-1001, Abstract, 1:41–67. According to the ’429 Patent, this arrangement keeps the “expected current path” flowing through the converging wire within the boundary of the converging wire, conducted along the shortest distance between the adjacent through holes, so that “an accumulation of charges at a boundary of the shielding layer can be reduce[d], and an occurrence of an effect of ESD damage of the shielding layer can be reduced.” Ex-1001, 8:18–27; Ex-1002, ¶55.

Figures 1–3 illustrate the disclosed embodiment. Figure 1 is a cross-sectional view showing the panel’s layer stack: a substrate 1 (red), a shielding layer 2 (blue) located on the substrate 1, a bottom insulating layer 30 (green), a buffer layer 31, a pixel driving circuit layer 4 (purple), and a plurality of power supply lines 7 (yellow). Ex-1001, 4:8–16, Fig. 1.

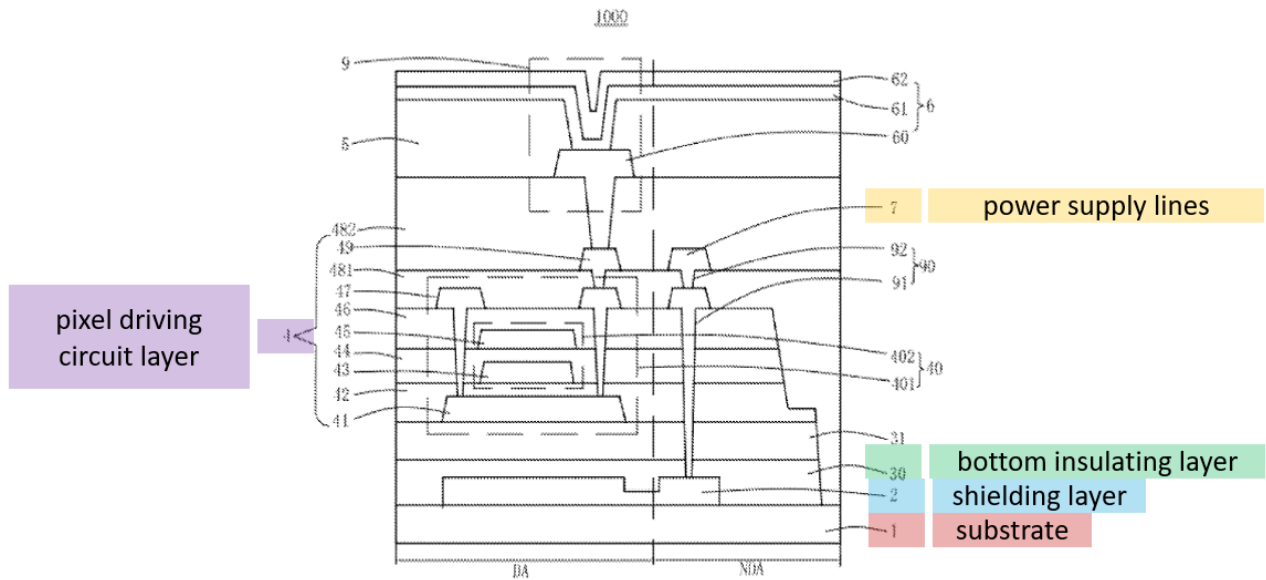
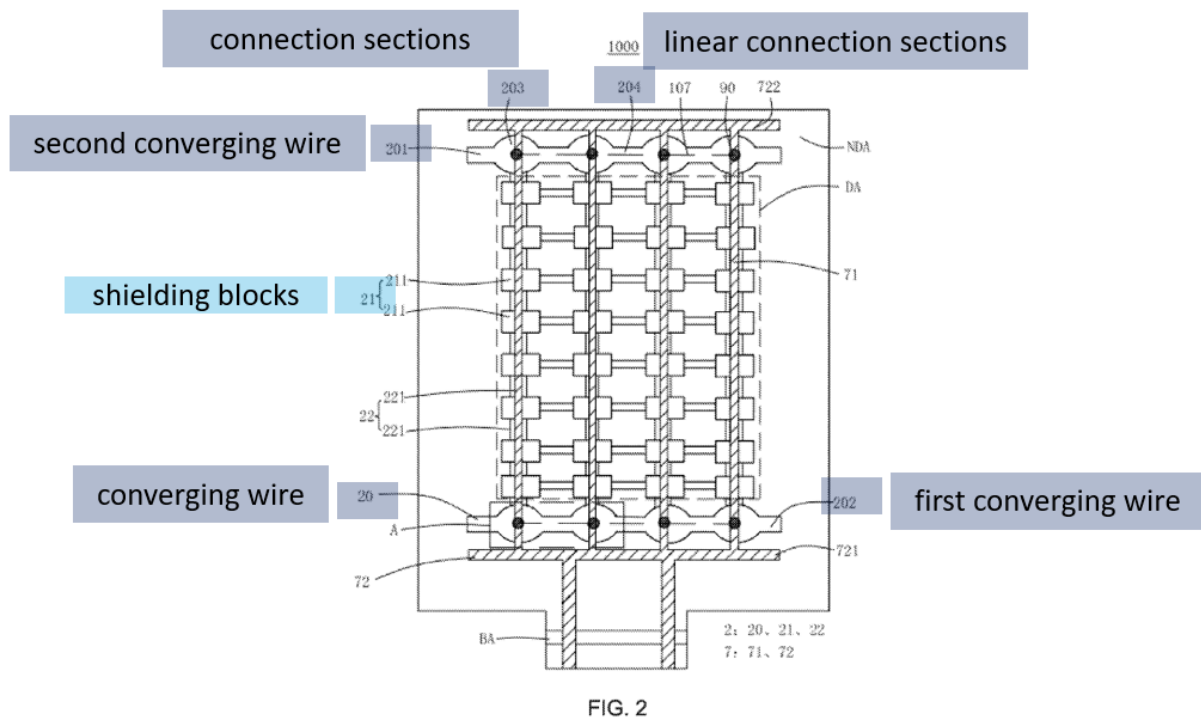


FIG. 1

Id. Fig. 1 (annotated).

Figure 2 is a top view of the display panel 1000. The shielding layer 2 includes a converging wire 20 located in the non-display region adjacent to the display region. Ex-1001, 4:36–42. The converging wire 20 (dark blue) includes a first converging wire 201 (dark blue) located in the first non-display region—which contains the bending sub-region BA at which the display panel bends—and a second converging wire 202 (dark blue) located in the second non-display region. Ex-1001, 4:3–7, 4:43–51. Each converging wire includes a plurality of first connection sections 203 (dark blue), the peripheries of which are arc shaped (e.g., “approximately oval or circular”), and a plurality of approximately linear second connection sections 204, each connected between a middle portion of two adjacent

first connection sections 203, with a maximum width of the first connection sections 203 greater than a width of the second connection sections 204. Ex-1001, 4:51–64. The shielding layer further includes a plurality of shielding blocks 211 arranged in an array, with each column of shielding blocks 211 (light blue) connected to a corresponding one of the first connection sections 203. Ex-1001, 5:1–13, Figs. 2, 3; Ex-1002, ¶¶56–57.



Ex-1001, Fig. 2 (annotated).

The pixel driving circuit layer 4 includes a semiconductor layer 41, a first insulating layer 42, a first gate metal layer 43, a second insulating layer 44, a second gate metal layer 45, an interlayer insulating layer 46 (i.e., a fourth

insulating layer), a third metal layer 47 (i.e., a second conductive metal layer), a first planarization layer 481 (i.e., a third insulating layer), a fourth metal layer 49 (i.e., a first conductive layer), and a second planarization layer 482. Ex-1001, 5:22–46. The plurality of power supply lines 7 are disposed in the fourth metal layer 49 and are electrically connected to the first connection sections 203 of the converging wire 20 through a plurality of through holes 90. Ex-1001, 6:47–51, 7:19–22. The through holes 90 include first through holes 91, which penetrate the first insulating layer 42, the second insulating layer 44, and the interlayer insulating layer 46, and second through holes 92, which penetrate the first planarization layer 481. The first through holes 91 “are communicated with the plurality of second through holes 92,” and the diameter of each first through hole 91 is smaller than the diameter of each second through hole 92. Ex-1001, 7:30–43; Ex-1002, ¶58.

As discussed in Sections XI and XII, each of the features that the ’429 Patent characterizes as its purported invention—a biased bottom shielding layer with mesh-connected shielding blocks, peripheral converging wires connected to the panel’s power supply lines through stacked through holes, and nested through holes of differing diameters—was well known to a person of ordinary skill in the art (“POSITA”) before the earliest alleged priority date of the ’429 Patent (March

11, 2022), as reflected in Yi1, Yi2, Zhang, and Park. *See infra* Sections XI, XII; Ex-1002, ¶¶44–45.

VII. PROSECUTION HISTORY OF THE '429 PATENT

The '429 Patent was filed March 22, 2022 as the U.S. national stage entry of PCT Application No. PCT/CN2022/082256, filed the same day, and claims priority to Chinese Application No. 202210237733.1, filed March 11, 2022.

The '429 Patent was allowed without any rejections. The prior art relied upon in this Petition was not considered by the Examiner during the prosecution of the '429 Patent. Therefore, the Grounds discussed in this Petition present new arguments that were not considered during prosecution. Ex-1002, ¶59.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA at the relevant time would have had at least a bachelor's degree in electrical engineering, materials science, mechanical engineering, or a related field, and two years of experience in the design and/or development of display devices or consumer electronics, including familiarity with OLED displays, flexible display panels, display module structures, adhesives, and/or packaging technologies, with additional education substituting for experience and vice versa. Ex-1002 ¶¶40–43.

IX. PRIORITY DATE

For purposes of this proceeding only, Petitioner applies the earliest alleged priority date of the '429 Patent: March 11, 2022.²

X. CLAIM CONSTRUCTION

Petitioner interprets the claims according to *Phillips*. 37 C.F.R. § 42.100(b). To resolve this Petition, Petitioner does not believe that any term requires express construction.³ CTPG, 44; Ex-1002 ¶61.

XI. BRIEF DESCRIPTION OF THE APPLIED PRIOR ART

A. Yi1 (Ex-1005)

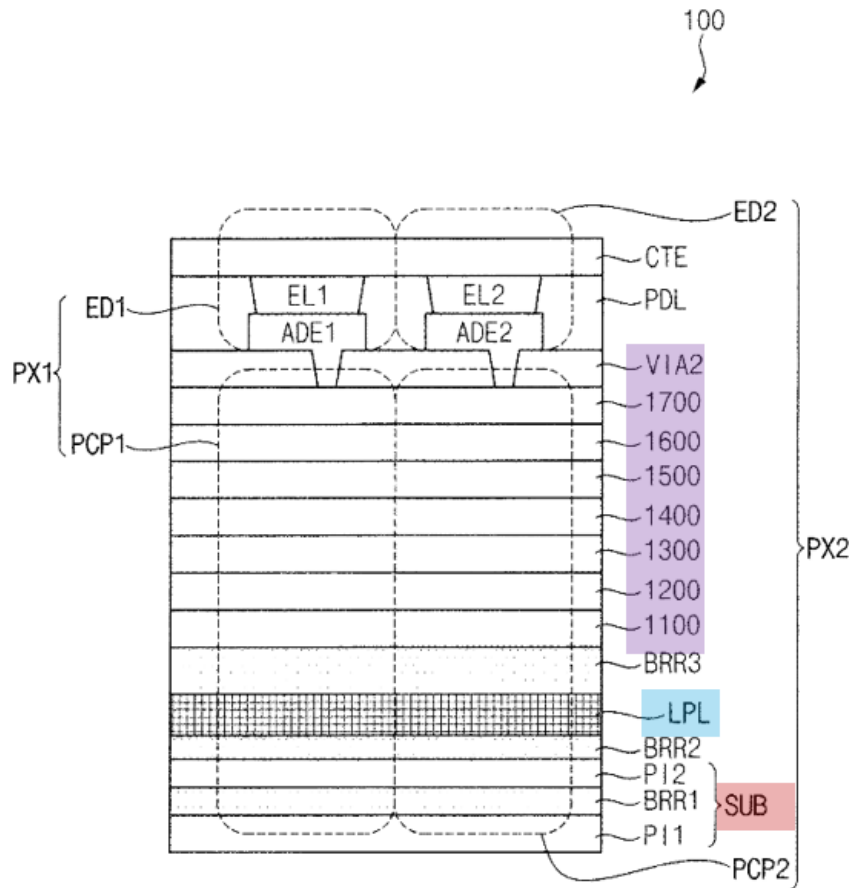
Yi1 (U.S. Patent No. 11,963,404) (Ex-1005) was filed on July 14, 2021, issued on April 16, 2024, and claims priority to a Korean application filed November 30, 2020. Ex-1005, Cover. Because Yi1 was filed before the earliest alleged priority date of the '429 Patent (March 11, 2022), Yi1 is prior art to the '429 Patent under at least 35 U.S.C. §102(a)(2). *Id.*; Ex-1002, ¶62.

² Petitioner respectfully reserves the right to challenge the priority date in other proceedings.

³ The Samsung litigation is in its infancy. Petitioner respectfully reserves all rights to raise claim construction and other arguments in district court and will request leave to submit the district court's claim construction as soon as it becomes available. Additionally, should PO raise express or implied claim construction arguments in its Preliminary Response, Petitioner will respectfully seek a Preliminary Reply to respond. Consolidated Trial Practice Guide ("CTPG"), 44–45.

Yi1 is directed to a display device that includes a lower pattern layer (LPL) (light blue) disposed between the substrate (red) and the active patterns (1100 and upward) of the pixel circuits (purple). Ex-1005, 10:51–11:25, Figs. 1, 4.

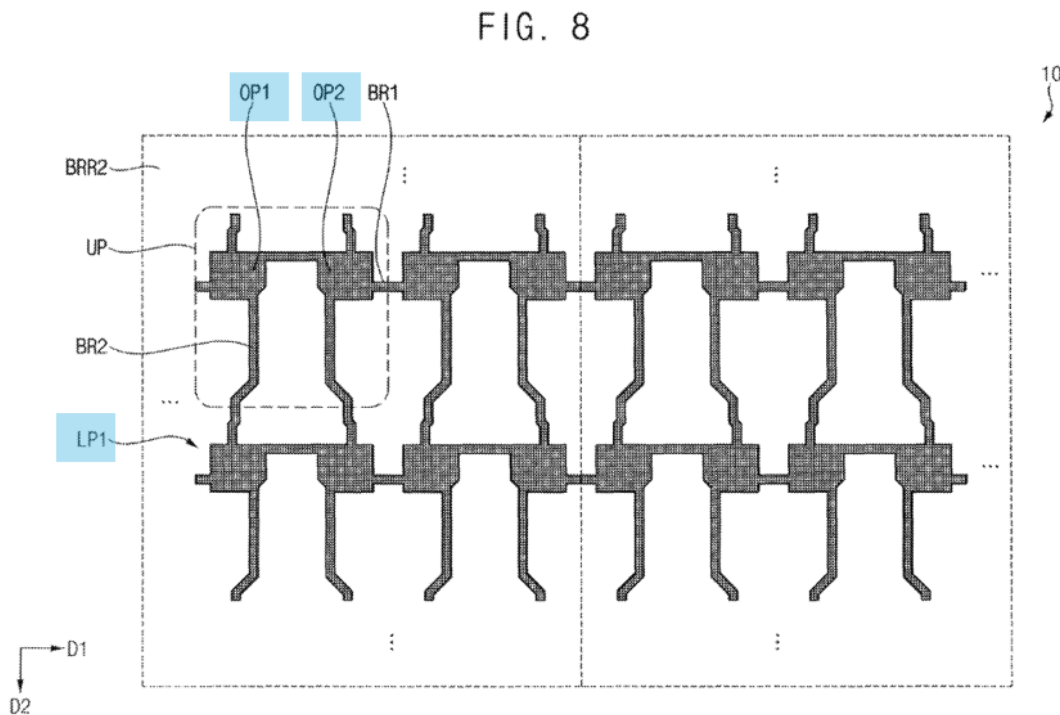
FIG. 4



Id. Fig. 4 (annotated).

The LPL includes a plurality of unit patterns UP—each composed of an overlap pattern OP (light blue) and connecting bridges—that are repeatedly arranged in a mesh shape. Ex-1005, 12:1–7, Fig. 8. The overlap patterns shield

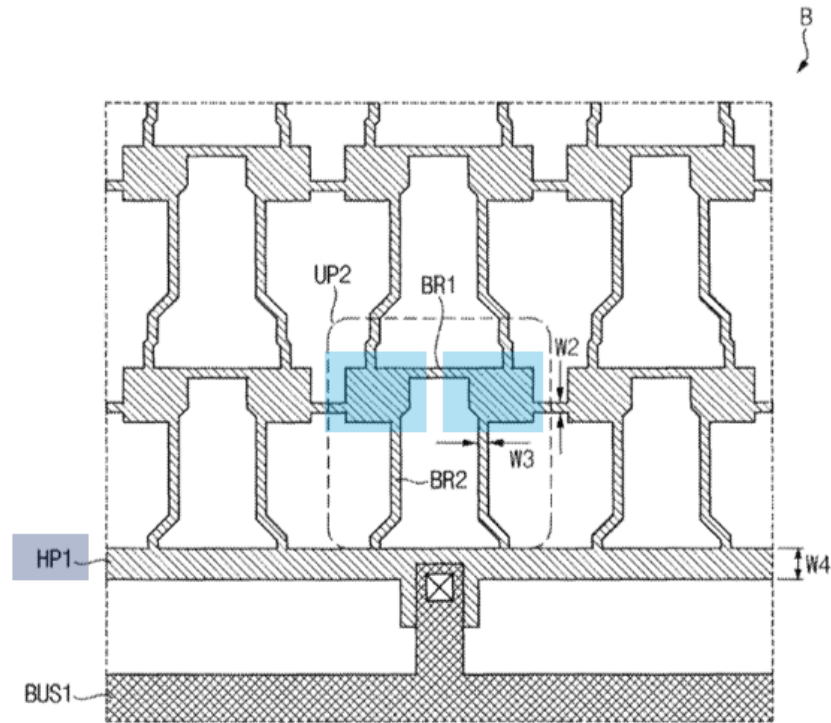
the first active pattern 1100 from polarization of the organic materials included in the organic film layers of the substrate, so that the electrical characteristics (e.g., threshold voltage, electron mobility) of the transistors are not changed and display quality is improved. Ex-1005, 11:20–25, 17:36–18:12; Ex-1002, ¶¶63–65.



Ex-1005, Fig. 8 (annotated).

The LPL is supplied with the power voltage ELVDD through horizontal patterns disposed along its edges. A first horizontal pattern HP1, disposed at the bottom of the mesh shape and extending in the first direction D1, is connected to a power voltage bus BUS1 (dark blue). Ex-1005, 19:30–32, 20:22–42, Figs. 19, 22.

FIG. 22

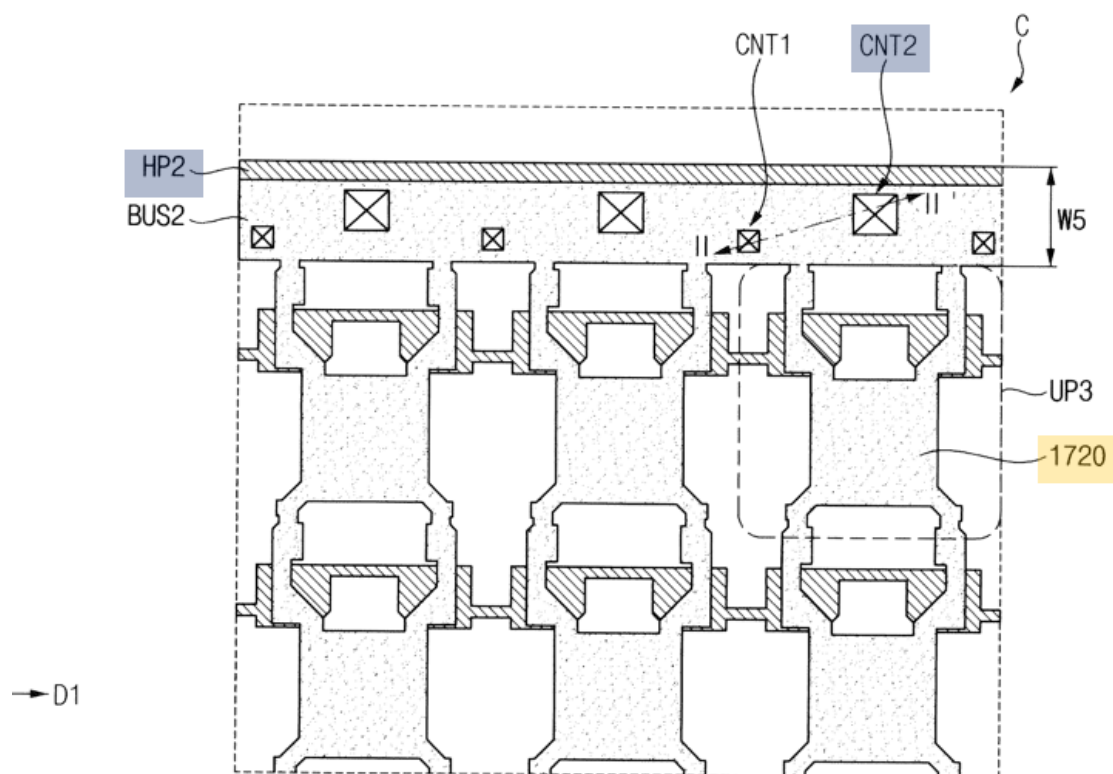


Id. Fig. 22 (annotated).

A second horizontal pattern HP2 (dark blue), disposed at the top of the mesh shape, contacts an intermediate connection pattern ICP through a second contact hole CNT2, and the ICP in turn contacts a power voltage pattern BUS2—provided together with the power voltage line 1720 (yellow)—through a first contact hole CNT1. Ex-1005, 20:55–21:9, Figs. 23, 24. The horizontal patterns thereby transmit the power voltage ELVDD to the unit patterns and “reduce a voltage drop

of the power voltage ELVDD applied to the unit patterns UP.” Ex-1005, 21:11–15; Ex-1002, ¶¶66–67.

FIG. 23



Ex-1005, Fig. 23 (annotated).

Yi1 is accordingly directed to the same alleged invention as the '429 Patent: a display panel with a biased shielding layer disposed beneath the pixel driving circuit layer, comprising a plurality of shielding blocks and a converging wire connected to the panel's power supply lines through stacked through holes. Yi1 is

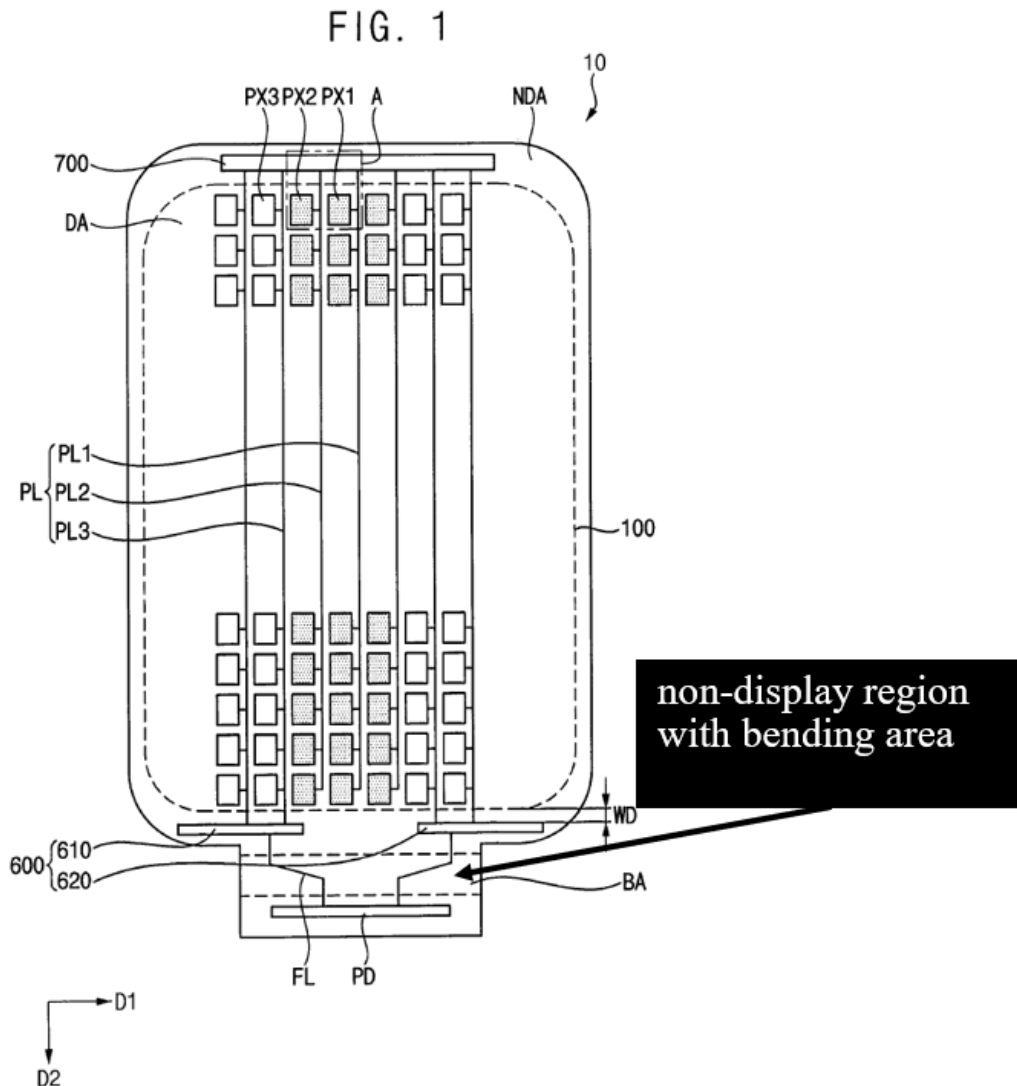
a Samsung Display patent naming inventor Changho Yi, and discloses a lower-pattern/shielding architecture closely analogous to that of Yi2, discussed next. Ex-1002, ¶67.

B. Yi2 (Ex-1006)

Yi2 (U.S. Patent Application Publication No. 2022/0199741) (Ex-1006) was filed on July 21, 2021, published on June 23, 2022, and claims priority to a Korean application filed December 18, 2020. Because Yi2 was filed before the earliest alleged priority date of the '429 Patent (March 11, 2022), Yi2 is prior art to the '429 Patent under at least 35 U.S.C. §102(a)(2). Ex-1002, ¶68.

Yi2 discloses a display device that is substantially similar in architecture to the display device of Yi1. Yi2's device includes a first lower pattern LP1 disposed on the substrate in the display area DA. Ex-1006, ¶¶100–101. The first lower pattern LP1 includes a plurality of unit patterns UP—each including an overlap pattern OP, first bridges BR1, and second bridges BR2—repeatedly arranged in a mesh shape. *Id.* ¶¶101–105, Figs. 8, 9. The overlap patterns OP overlap the gate electrodes and “may shield the first active pattern 1100 from polarization of organic materials included in the second organic film layer PI2,” *id.* ¶210, so that “the electrical characteristics of the first transistor T1 may not be changed.” *Id.* ¶177; *see id.* ¶¶93–94.

Yi2 further discloses a “bending area BA” included in the “non-display area NDA.” *Id.* ¶53. Figure 1 showcases the bending area in the non-display region:



Id. Fig. 1 (annotated).

Yi1 and Yi2 are commonly assigned Samsung Display patent documents sharing inventor Changho Yi, and disclose closely analogous lower-pattern/shielding architectures with nearly identical layer stacks. As discussed

below, Yi2 discloses each limitation of Claims 1–3, 7–9, 11–13, and 17–20. Ex-1002, ¶69.

C. Zhang (Ex-1007)

Zhang (U.S. Patent No. 9,658,523) (Ex-1007), assigned to STMicroelectronics, Inc. and International Business Machines Corporation, filed on March 31, 2014, and issued on May 23, 2017—before the earliest alleged priority date of the ’429 Patent—and is prior art to the ’429 Patent under at least 35 U.S.C. §102(a)(1). Ex-1002, ¶70.

Zhang discloses an interconnect structure having wavy metal lines that accommodates large self-aligned vias. Ex-1007, 1:20–26, 5:1–35, Figs. 1A, 1B, 7B. The metal line profile shape resembles a “bicycle chain” structure (Fig. 1B) in which wide portions 104 (via landing pads 106) (dark blue) are spaced periodically between narrow portions 105. Ex-1007, 5:7–20. The wide portions 104 accommodate via landing pads 106 that exceed the width of the narrow portions 105, and adjacent metal lines 102a and 102b can be staggered relative to one another so that via landing pads along one metal line are aligned with narrow portions of neighboring metal lines, maintaining a constant spacing 108. Ex-1007, 5:12–26.

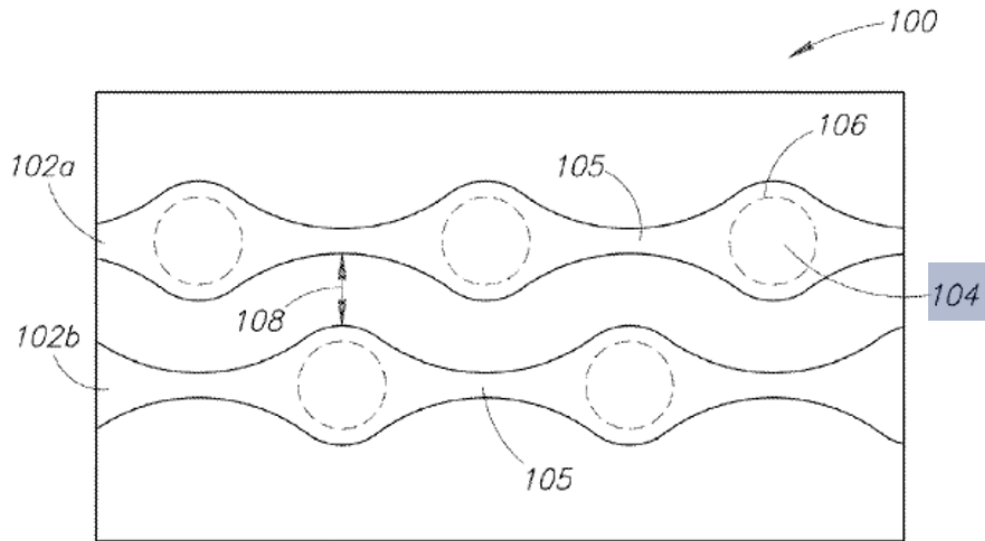


FIG.1B

Id. Fig. 1B (annotated).

Figure 7B shows the final wavy metal line structures 120 after metal fill, including narrow portions 122, intermediate width portions 123, and wide portions 124. Ex-1007, 5:44–57, Fig. 7B. The wide portions have rounded, arc-shaped peripheries resulting from the optical lithography process (OPC), creating a wavy undulating profile. Ex-1007, 6:5–30. The “rounded features forming the wavy metal line structures 120 are intentionally created by leveraging distortion that occurs in the lithography process”—corners of rectangular mask features “transfer to the photoresist and the metal trench as rounded features.” Ex-1007, 6:9–30; Ex-1002, ¶¶70–71. As Figure 7B illustrates, the wide portions (via landing pads) have arc-shaped (rounded) peripheries, while the narrow portions connecting them are

linearly shaped, and the maximum width of the wide portions (via landing pads) is greater than the width of the narrow connecting portions:

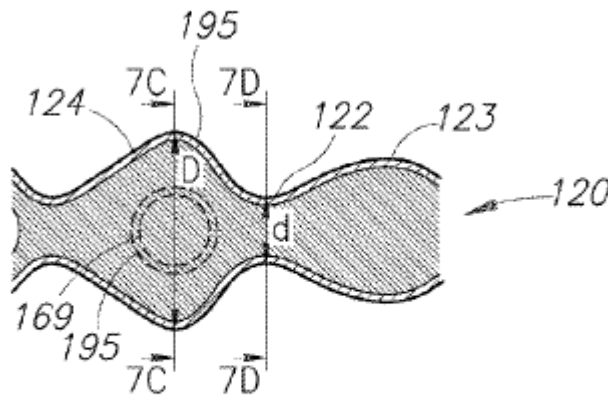


FIG. 7B

Zhang is accordingly directed to interconnect structures with wavy metal lines featuring arc-shaped wide portions (via landing pads) and linear narrow connecting portions, and supplies the rounded, arc-shaped feature geometry recited in dependent Claim 6. *See infra* Section XII.C; Ex-1002, ¶72.

D. Park (Ex-1008)

Park (U.S. Patent No. 7,335,912) (Ex-1008), assigned to Samsung SDI, issued on February 26, 2008, and is prior art to the '429 Patent under at least 35 U.S.C. §102(a)(1). Ex-1002, ¶73.

Park discloses an organic light emitting display having an “improved via hole.” Ex-1008, Abstract. Park explains that when the size of a via hole is reduced, “a pattern defect may be generated when patterning the lower electrode, thereby decreasing the device’s reliability.” Ex-1008, 1:30–32. Park solves this problem by “forming a via hole to be larger than a contact hole in a structure where the via hole is formed corresponding to the contact hole,” which “may prevent a patterning defect on a lower electrode, and improve processing stability and reliability of a device.” Ex-1008, 3:16–21. In Park’s structure, source and drain electrodes 241 and 245 are coupled to the semiconductor layer through contact holes 231 and 235 formed in an interlayer dielectric 230, and a via hole 267 formed above and corresponding to the contact hole 235 is larger than the underlying contact hole. Ex-1008, 4:52–5:11, Figs. 2, 3, 4A, 4B; Ex-1002, ¶73. These via holes are illustrated in Figures 4A and 4B:

FIG. 4A

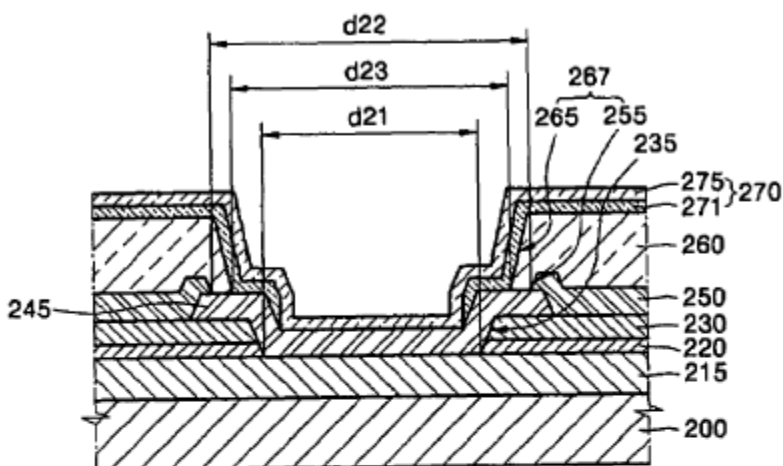
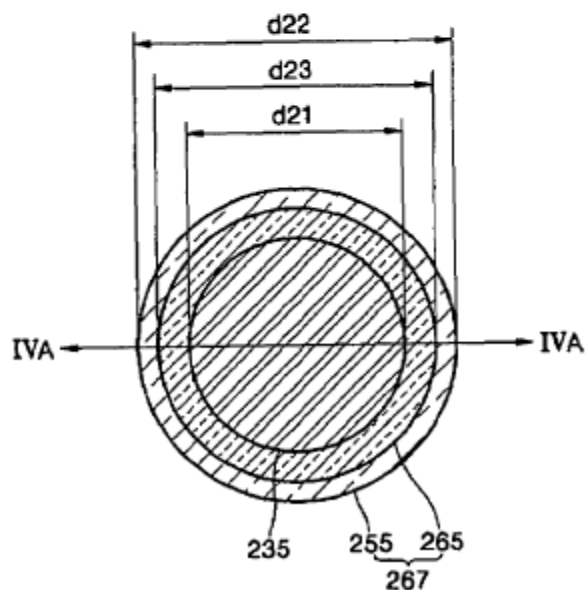


FIG. 4B



Park is accordingly directed to the same OLED display panel field as Yi1, Yi2, and the '429 Patent, and supplies an express motivation for dimensioning stacked, communicating through holes such that the upper hole is larger than the

lower hole, as recited in dependent Claim 10. *See infra* Section XII.D; Ex-1002, ¶73.

XII. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS

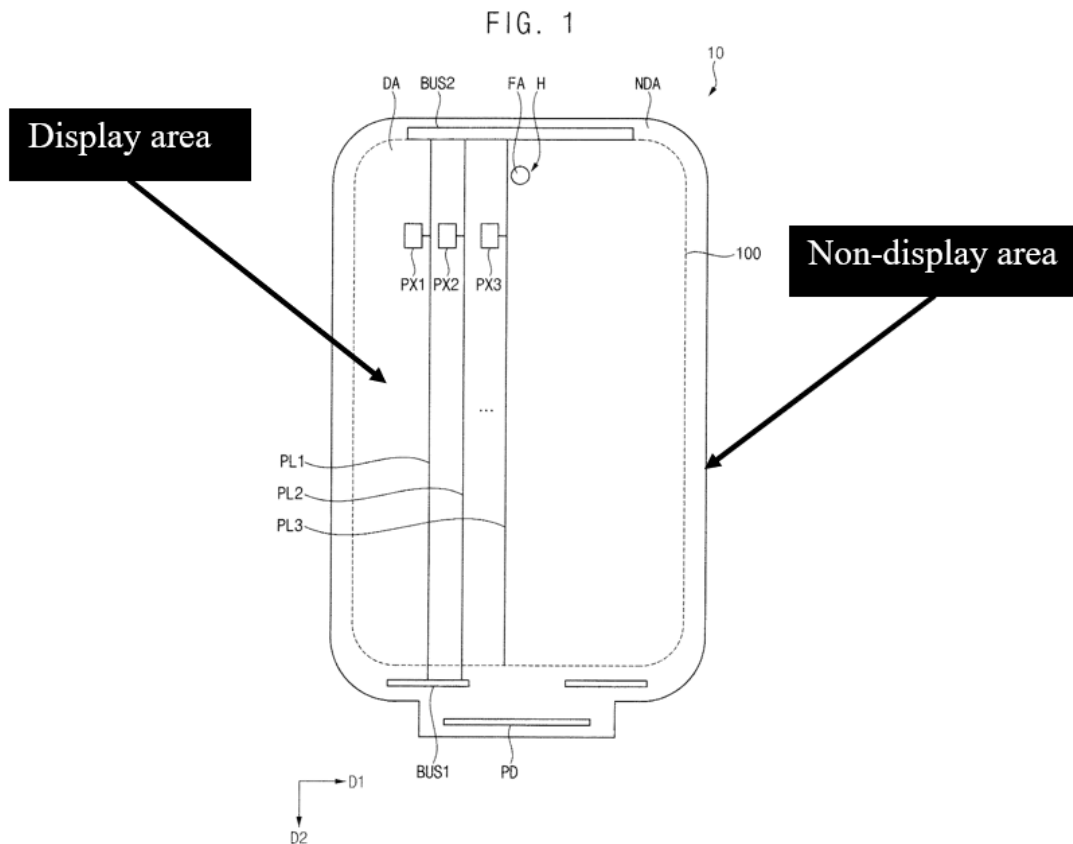
A. Ground 1: Claims 1–5, 9, and 11–15 Are Rendered Obvious by Yi1

1. Claim 1

- a. 1[pre]: A display panel, comprising a display region and a non-display region disposed on at least one side of the display region, wherein the display panel comprises:**

To the extent the preamble is limiting, Yi1 teaches a display panel, comprising a display region and a non-display region disposed on at least one side of the display region. Ex-1002, ¶74.

Yi1 teaches a display device which may be “divided into a hole area FA, a *display area DA*, and a *non-display area NDA*.” Ex-1005, 6:9–11. Figure 1 illustrates these areas:



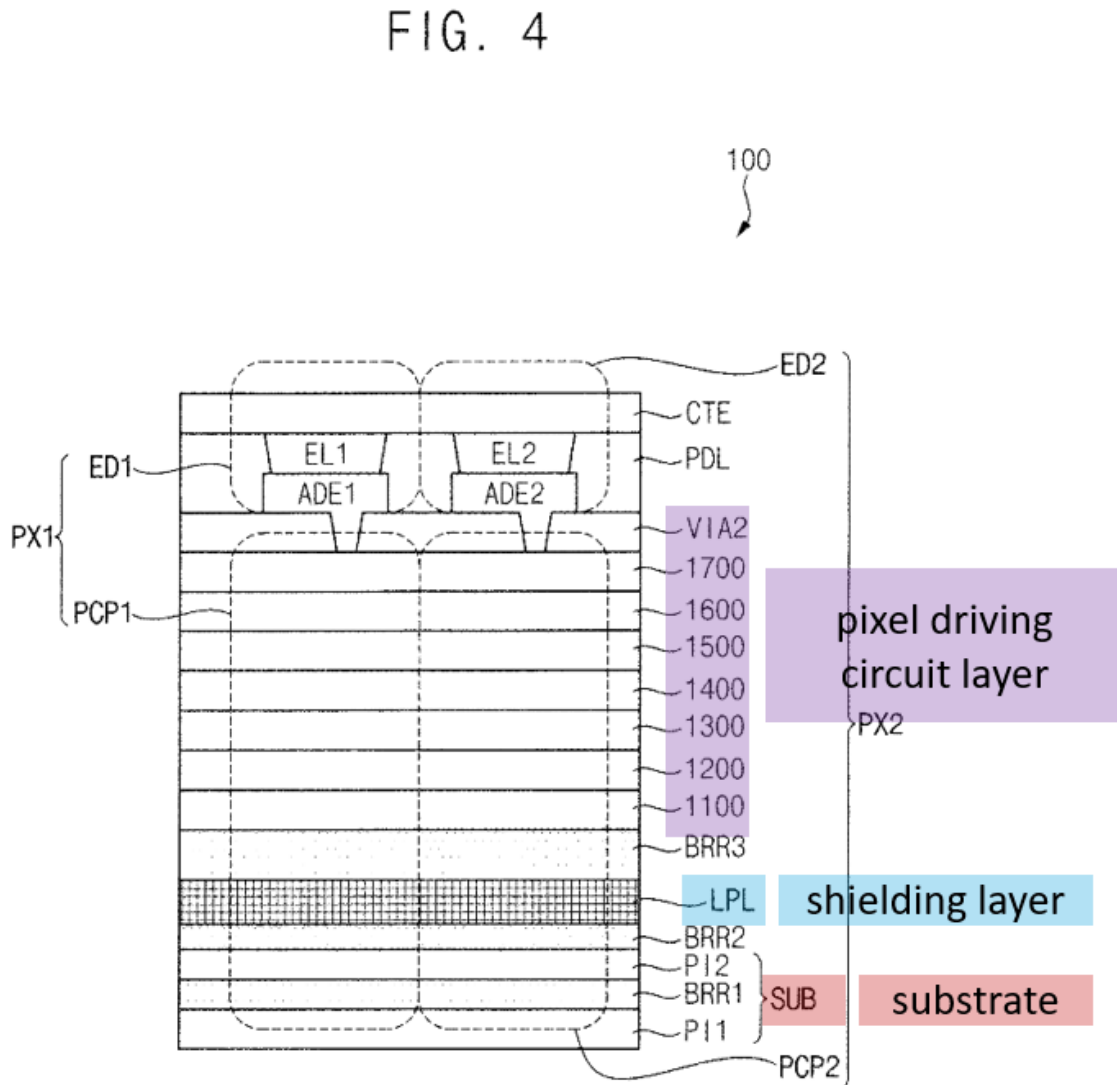
Id. Fig. 1 (annotated).

As is seen in the figure above, the non-display area “surround[s] the display area” and is on all four sides of the display area, so is on “at least one side” of the display area. Ex-1005, 6:16–18; Ex-1002, ¶74. From a technical standpoint, this arrangement is standard practice in OLED panel design, where the non-display region houses peripheral circuitry, power routing, and bending structures that cannot be placed within the active pixel array. *See* Ex-1009, 198; Ex-1011, 479.

b. 1[a]: a substrate;

Yi1 teaches element 1[a]. Ex-1002, ¶75.

Yi1 discloses a layer stack that makes up a display panel, illustrated in
Figure 4:



Ex-1005, Fig. 4 (annotated).

Figure 4 is a “cross-sectional view illustrating a display panel included in the display device of FIG. 1.” Ex-1005, 4:30–31. This stack includes a “first organic

film layer PI1, [a] first barrier layer BRR1, and [a] second organic film layer PI2,” and Yi1 teaches that these layers “***constitute a substrate SUB***” (red). Ex-1005, 10:51–11:5. This organic substrate structure is consistent with flexible OLED panel designs, in which alternating organic and inorganic barrier layers provide both mechanical flexibility and moisture/oxygen barrier properties essential for OLED longevity. See Ex-1009, 85, 240; Ex-1010, 524–525; Ex-1011, 60, 74.

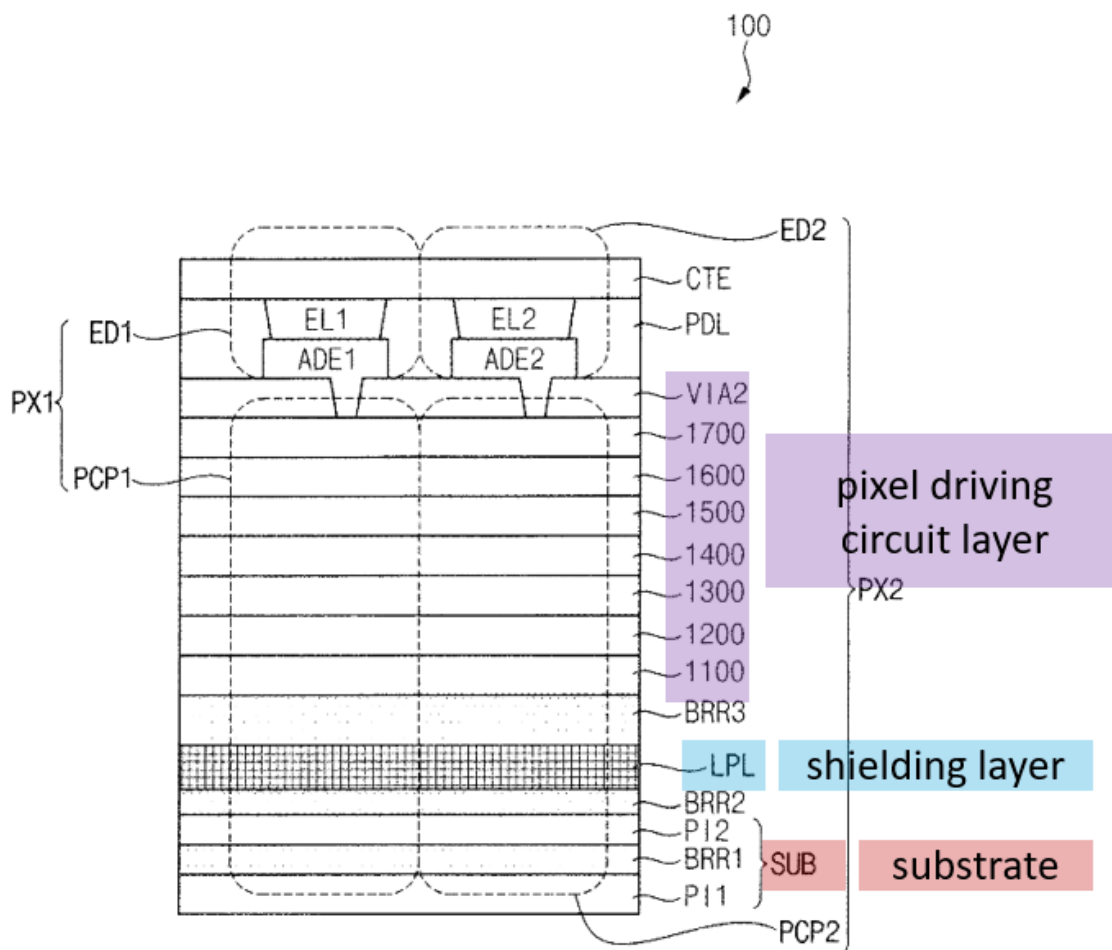
- c. **1[b]: a shielding layer located on the substrate, wherein the shielding layer comprises a plurality of shielding blocks and a converging wire electrically connected to the plurality of shielding blocks, and the converging wire is located on at least one side of the plurality of shielding blocks;**

Yi1 teaches element 1[b]. Ex-1002, ¶76.

First, Yi1 teaches a shielding layer located on the substrate. Yi1 teaches a lower pattern layer (LPL), which shields “the polarization phenomenon from electrically affecting the first and second active patterns.” Ex-1005, 11:20–25. As the ’429 Patent explains, the purpose of the shielding layer is to “shield the plurality of pixel driving circuits of the pixel driving circuit layer.” Ex-1001, 4:32–36. Yi1’s LPL (light blue), which “shield[s] the active pattern from polarization of organic materials included in the organic film layer” so that “the electrical characteristics of a transistor [are not] changed,” is accordingly a shielding layer. Ex-1005, 3:64–4:2; Ex-1002, ¶76. As Dr. Lebby explains, in

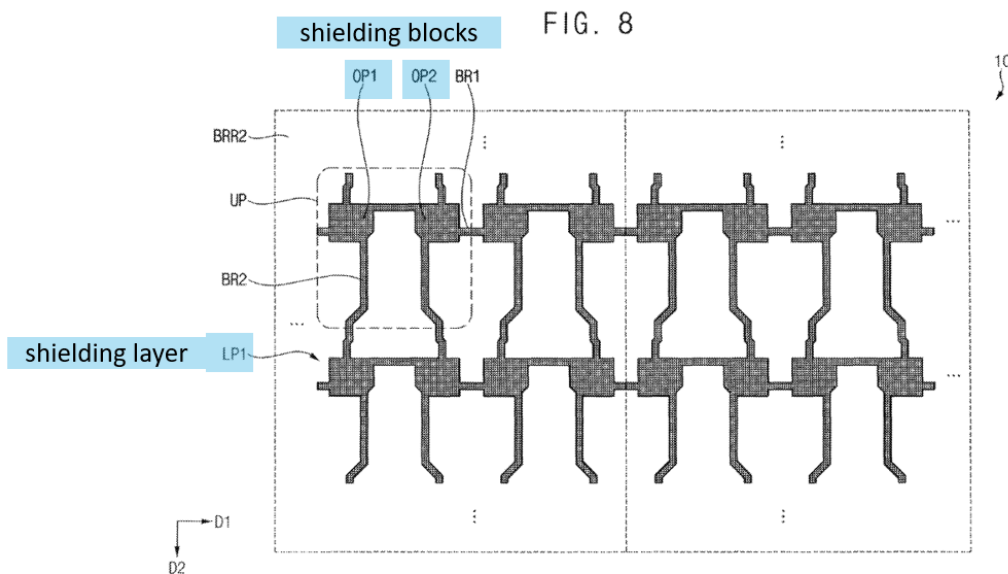
OLED display design, such shielding layers serve the critical function of preventing electrical instability in overlying TFTs caused by charge trapping at organic-inorganic interfaces. Ex-1002, ¶77.

FIG. 4



Ex-1005, Fig. 4 (annotated).

Second, Yil teaches that the shielding layer comprises a plurality of shielding blocks and a converging wire electrically connected to the plurality of shielding blocks. Figure 8 shows a diagram of the LPL, in which “a plurality of unit patterns UP are repeatedly arranged.” Ex-1005, 12:2–5. Each of this unit patterns is composed of two bridges and overlap pattern (OP) (light blue). Ex-1005, 12:5–7. The OP “shield the first active pattern from polarization of organic materials included in the second organic film layer,” and accordingly are the “shielding blocks” that make up the “shielding layer” (the LPL) (light blue). Ex-1002, ¶77.



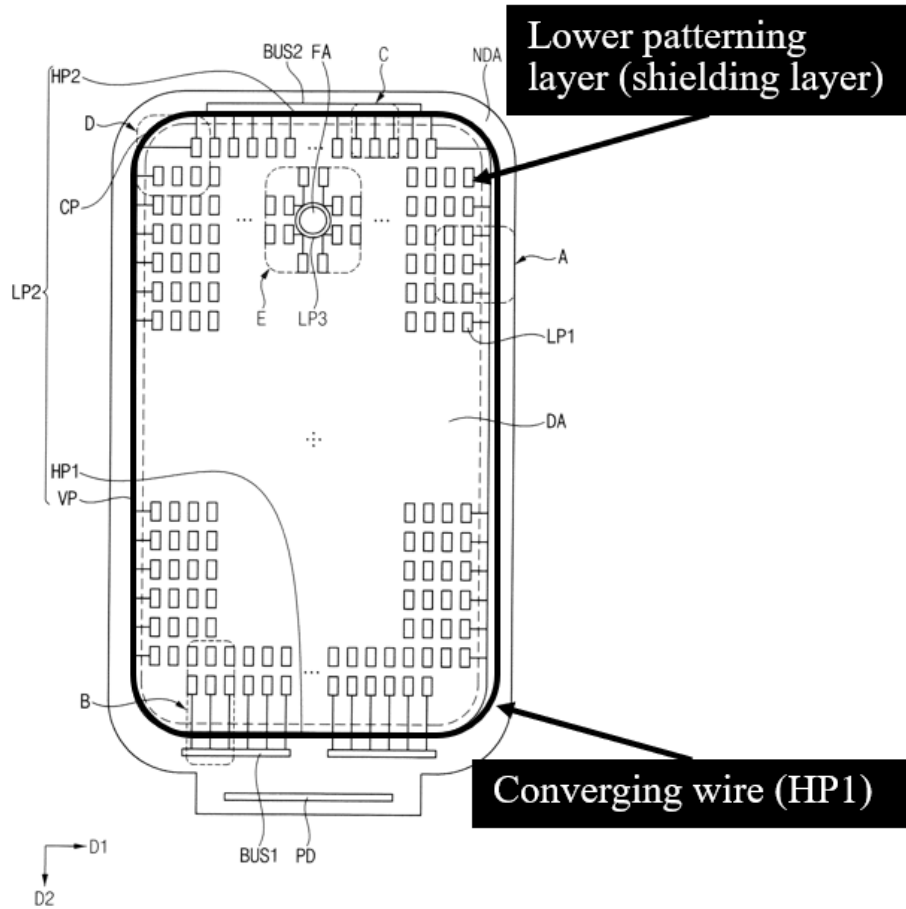
Ex-1005, Fig. 8 (annotated).

Third, Yi1 discloses a converging wire electrically connected to the plurality of the shielding blocks. As the '429 Patent explains, the “shielding layer includes a converging wire” alongside the shielding blocks. Ex-1001, 4:36–39.

A “plurality of power supply lines are electrically connected” to the converging wire, providing power to it. Ex-1001, 7:19–22. The converging wire reduces “an accumulation of charges at a boundary of the shielding layer,” and “an occurrence of an effect of electro-static discharge (ESD) damage of the shielding layer can be reduced.” Ex-1001, 8:24–27.

Yi1 discloses a “horizontal pattern,” (HP1) which is adjacent to the LPL. The arrangement of HP1 and the LPL is illustrated in Figure 19:

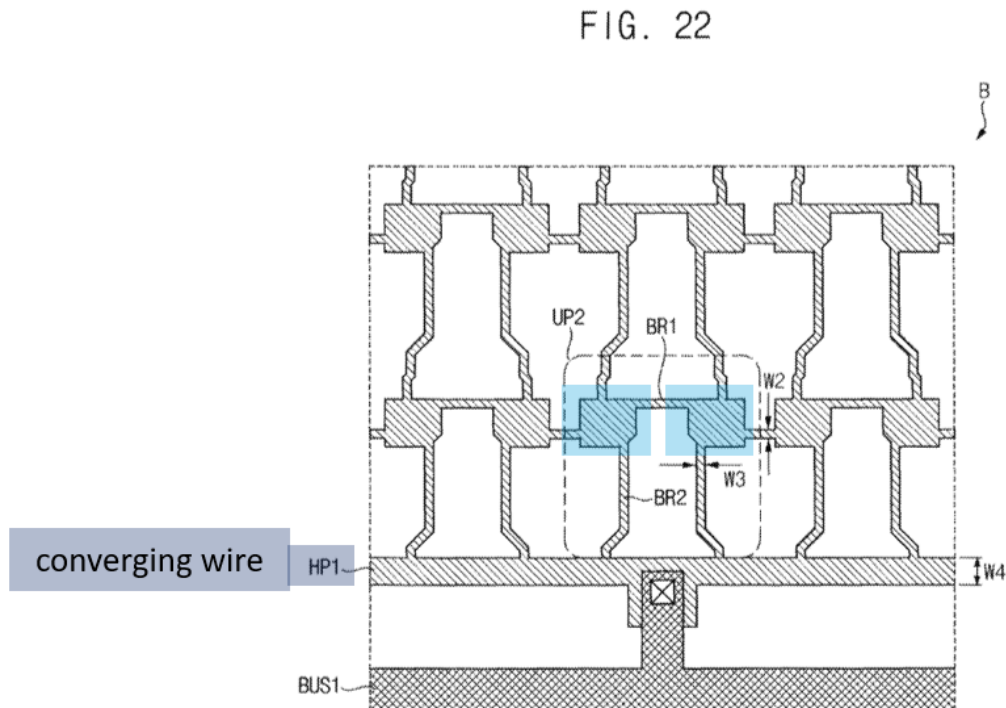
FIG. 19



Ex-1005, Fig. 19 (annotated).

HP1 is “connected to the power voltage bus BUS1,” permitting a “power voltage ELVDD” to be provided to the shielding layer. Ex-1005, 20:30–40. And the LPL, including the horizontal pattern, prevents “static electricity” from flowing to the “display panel,” so that “electrical breakdown [is] prevented.” Ex-1005,

23:25–29. Figure 22 provides a close up view of the relationship between the LPL (light blue), HP1 (dark blue), and the power voltage bus providing power:



Id. Fig. 22 (annotated).

HP1 (dark blue) is connected to the unit patterns above, and to the voltage bus (BUS1), which provides power to the shielding layer through HP1. Ex-1005, 20:20–37. Accordingly, HP1 is a converging wire electrically connected to the plurality of shielding blocks. Ex-1002, ¶¶77–79.

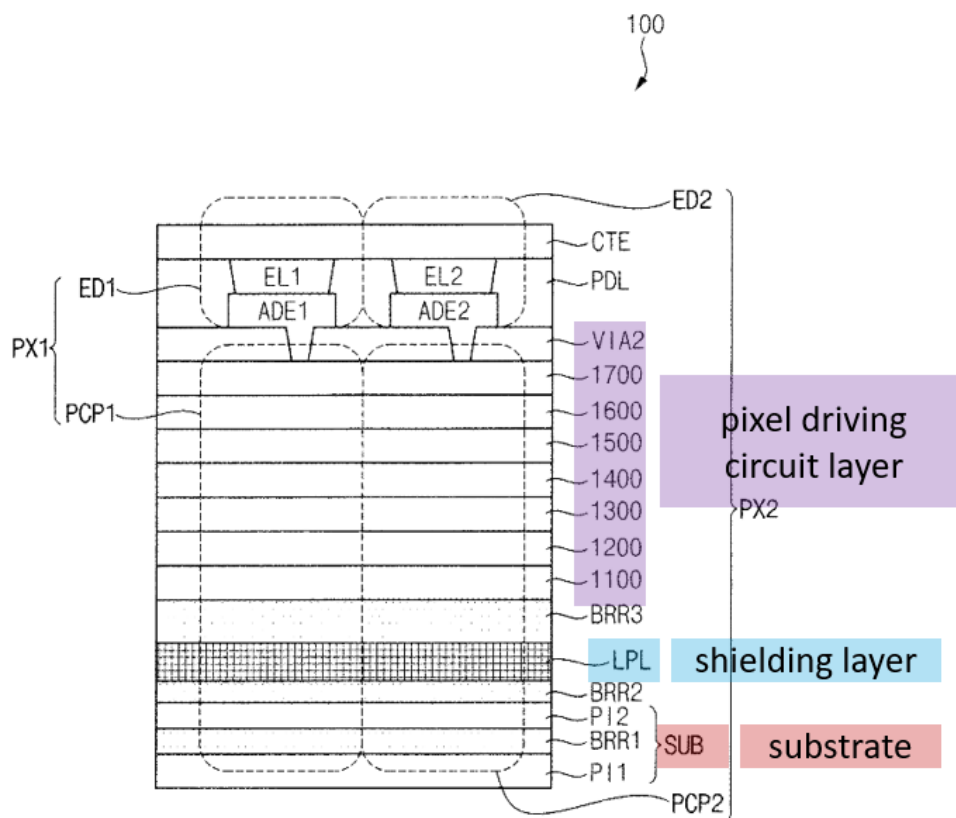
Third, Yi1 teaches that the converging wire is located on at least one side of the plurality of shielding blocks. As can be seen in Figures 19 and 22, the horizontal pattern HP1 is located on at least one side of the shielding blocks, surrounding them. *Id.*; Ex-1005, 20:20–37. This peripheral placement is an engineering choice that enables efficient power routing without consuming active display area—a fundamental design principle in OLED panel layout. *See* Ex-1009, 168, 186–189, 198; Ex-1011, 479; Ex-1002, ¶78.

- d. 1[c]: a pixel driving circuit layer located on the shielding layer, wherein the pixel driving circuit layer comprises a plurality of pixel driving circuits located in the display region, each of the plurality of pixel driving circuits at least partially overlaps a corresponding one of the shielding blocks; and**

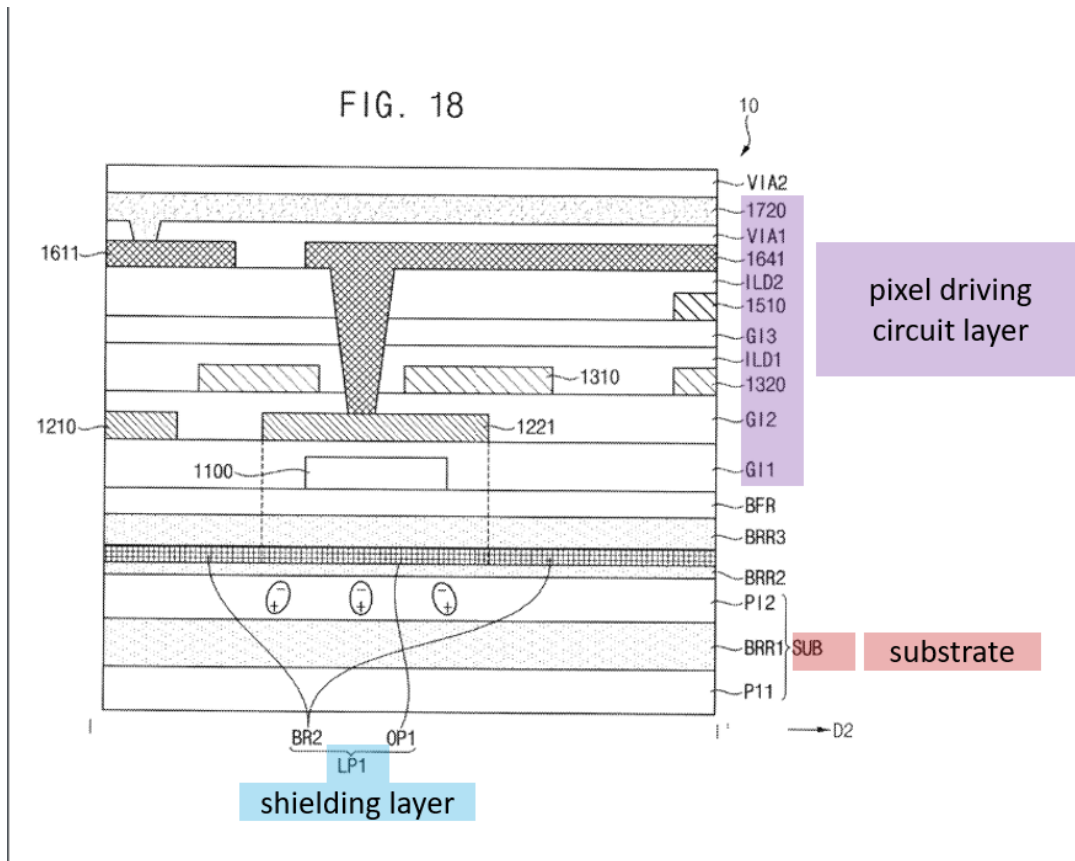
Yi1 teaches Element 1[c]. Ex-1002, ¶80.

First, Yi1 discloses the claimed pixel driving circuits. Yi1 teaches a “pixel circuit part,” (purple) which includes “a first organic film layer PI1, a first barrier layer BRR1, a second organic film layer PI2, a second barrier layer BRR2, a lower pattern layer LPL, a third barrier layer BRR3, a first active pattern 1100, a first conductive pattern 1200, a second conductive pattern 1300, a second active pattern 1400, a third conductive pattern 1500, a fourth conductive pattern 1600, and a fifth conductive pattern 1700.” Ex-1005, 10:51–60. These layers are depicted in Figures 4 and 18, which show two different side views of the pixel circuit parts:

FIG. 4



Id. Fig. 4 (annotated).



Id. Fig. 18 (annotated).

Yi1's PCP provides "the driving current to the first emitting diode" to form a pixel. Ex-1005, 10:33–36.

These structures and purpose are analogous to the makeup and purpose of the pixel driving circuit layer in the '429 Patent. As the Patent explains:

Referring further to FIG. 1, the pixel driving circuit layer 4 includes a semiconductor layer 41, a first insulating layer 42 located on the semiconductor layer 41, a first gate metal layer 43 located on the first insulating layer 42, a second insulating layer 44 located on the first gate metal layer 43, a second gate metal layer 45 located on the second insulating layer 44, an interlayer insulating layer 46 (i.e., a fourth insulating layer) located on the second gate metal layer 45, a third metal

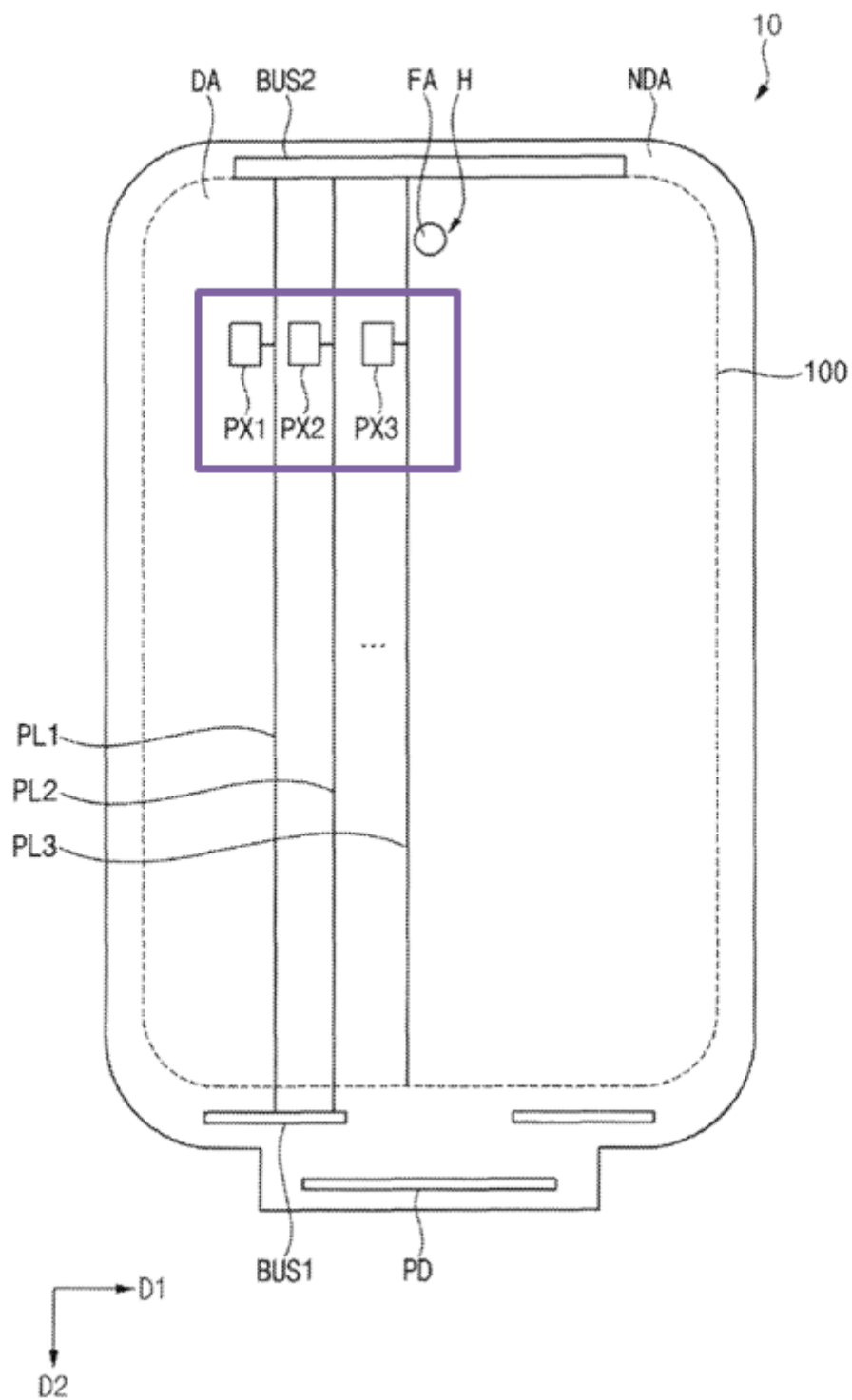
layer 47 (i.e., a second conductive metal layer) located on the interlayer insulating layer 46, a first planarization layer 481 (i.e., a third insulating layer) located on the third metal layer 47, a fourth metal layer 49 (i.e., a first conductive layer) located on the first planarization layer 481, and a second planarization layer 482 located on the fourth metal layer 49. The semiconductor layer 41, the first insulating layer 42, the first gate metal layer 43, the interlayer insulating layer 46, and the third metal layer 47 can jointly form the plurality of thin-film transistors 401. The first gate metal layer 43, the second insulating layer 44, and the second gate metal layer 45 can jointly form a plurality of capacitors 402. The plurality of pixel driving circuits 40 can include the plurality of capacitors 402 and the plurality of thin-film transistors 401 to drive the plurality of sub-pixels 9 to emit light.

Ex-1001, 5:22–46. Accordingly, the PCP is a pixel driving circuit. Ex-1002, ¶83.

As shown in Figure 1, these pixel driving circuits are located in the display region. Ex-1005, Fig. 1. Yil explains that a “pixel circuit part” and a corresponding “emitting diode” may constitute a “pixel.” Ex-1005, 10:28–29.

Figure 1 shows these pixels (PX1-30) (purple) in the display area of the device:

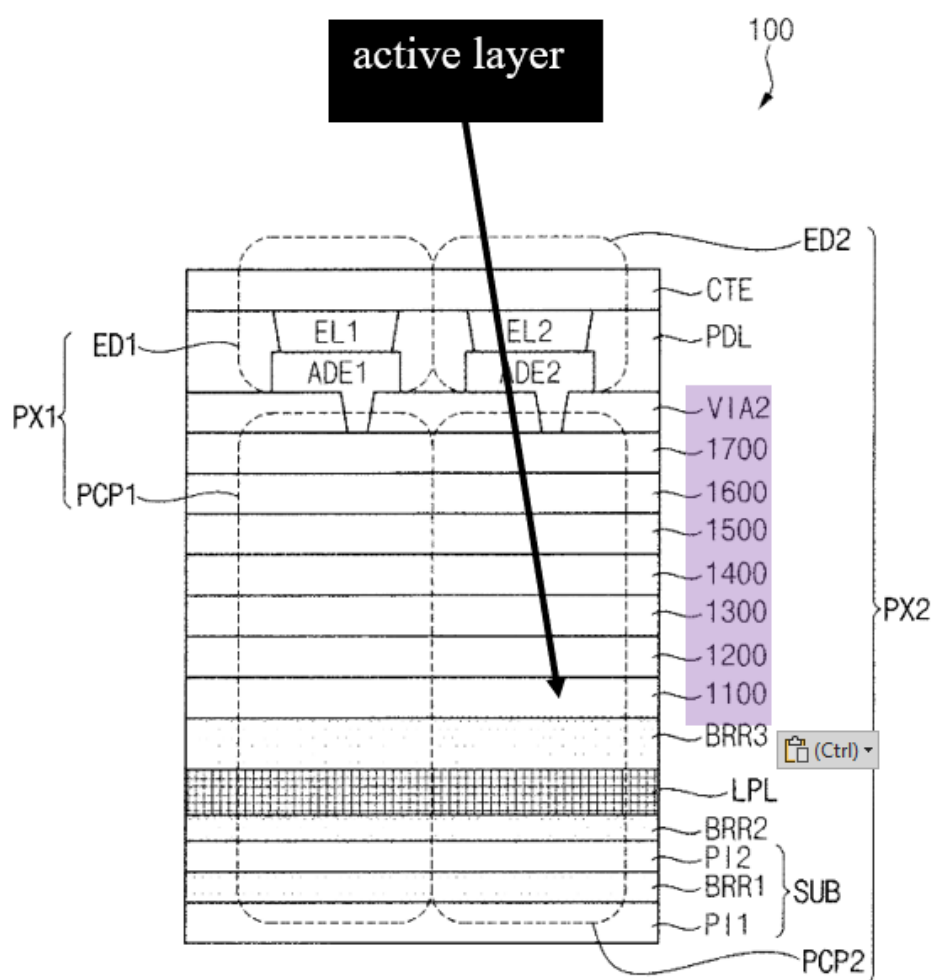
FIG. 1



Id. Fig. 1 (annotated).

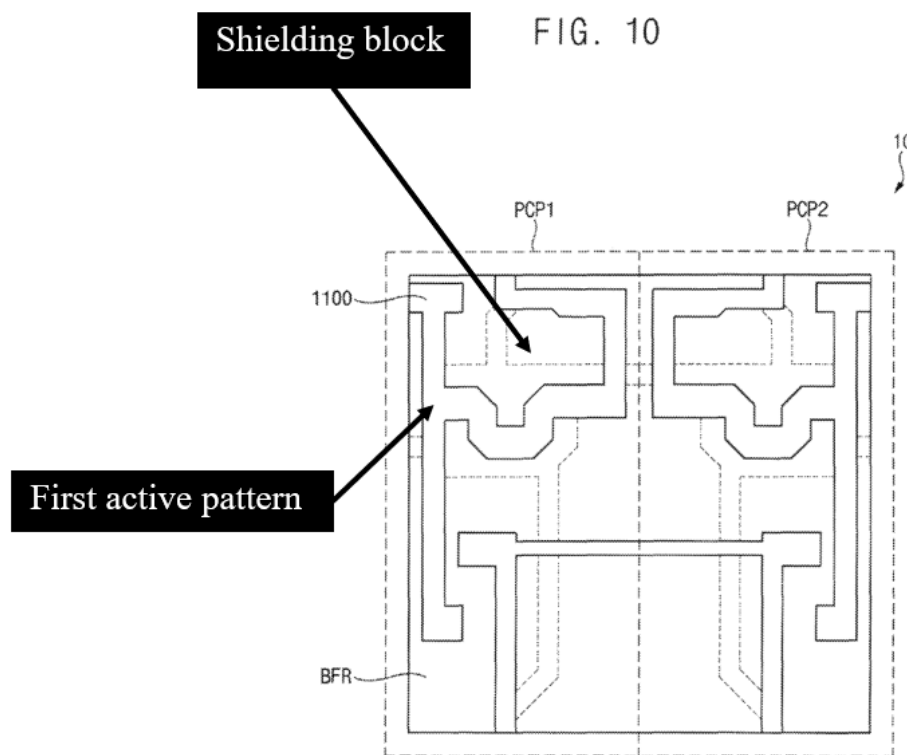
Furthermore, each of the pixel driving circuits at least partially overlaps a corresponding one of the shielding blocks. The first active pattern (1100) makes up one of the layers of the PCP, as shown in Figure 4:

FIG. 4



Id. Fig. 4 (annotated).

The first active pattern (1100) is disposed on the buffer layer that is placed over the lower pattern layer, and the “first active pattern 1100 may overlap the first lower pattern LP1.” Ex-1005, 12:65–13:7. Figure 10 provides a top-down view of this overlap:



Id. Fig. 10 (annotated).

Accordingly, Yi1 teaches this limitation. The overlap between the first active pattern and the first lower pattern ensures that the shielding blocks effectively shield each transistor from substrate polarization effects, confirming the

spatial correspondence between each pixel driving circuit and its corresponding shielding block. Ex-1002, ¶85.

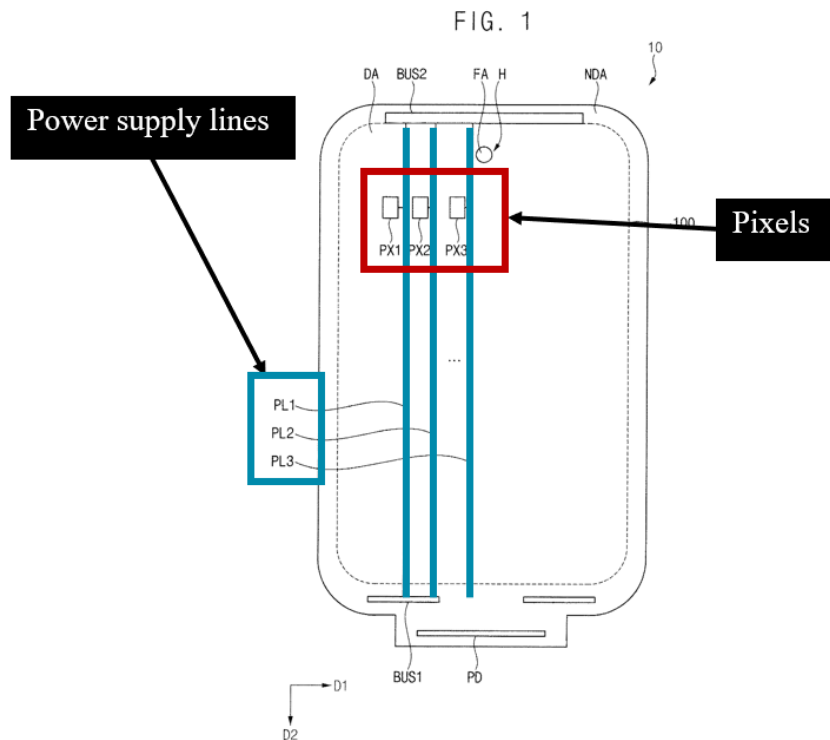
- e. **1[d]: a plurality of power supply lines disposed on a side of the shielding layer away from the substrate, wherein the plurality of power supply lines are electrically connected to the converging wire through a plurality of through holes;**

Yi1 teaches Element 1[d]. Ex-1002, ¶86.

First, Yi1 teaches a plurality of power supply lines disposed on a side of the shielding layer away from the substrate. As shown in Figure 1:

[t]he first and second pixels PX1 and PX2 may receive the power voltage ELVDD through the first and second power voltage lines PL1 and PL2, respectively. In addition, the power voltage pattern BUS2 may receive the power voltage ELVDD through the first and second power voltage lines PL1 and PL2. Accordingly, the third pixel PX3 may receive the power voltage ELVDD through the third power voltage line PL3.

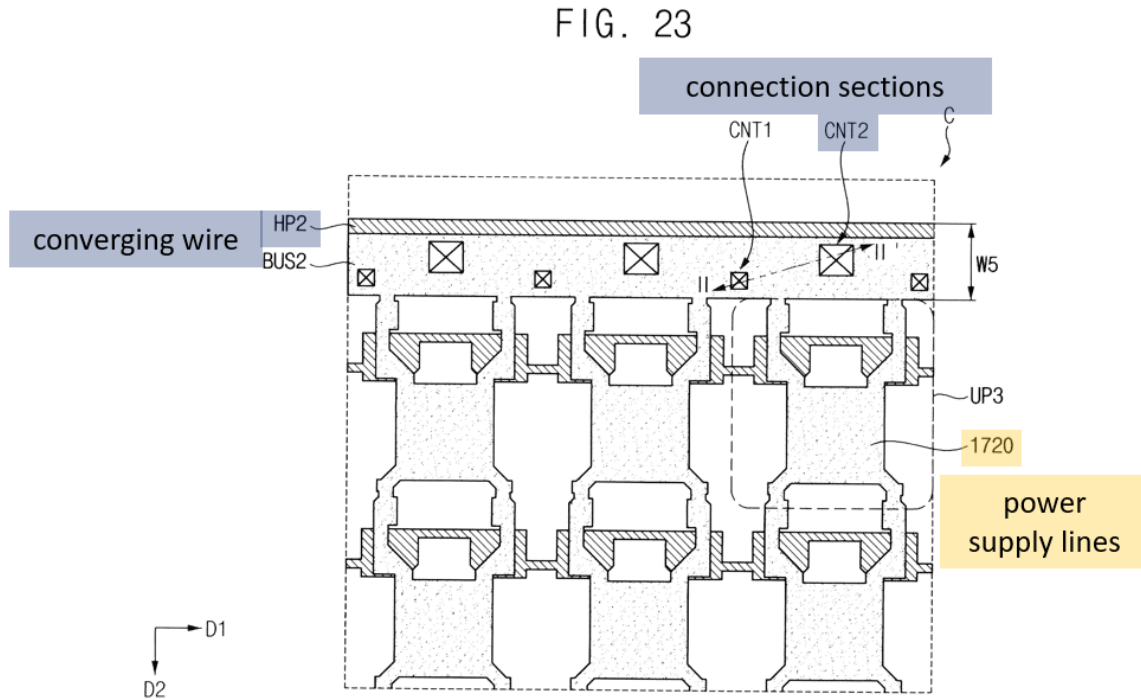
Ex-1005, 10:4–12. These power lines (blue) can be seen in the display device:



Id. Fig. 1 (annotated).

Second, Y11 teaches that the plurality of power supply lines are electrically connected to the converging wire through a plurality of through holes. Figure 23 illustrates HP2 (dark blue), a second horizontal pattern that is part of the converging wire. *See also id.* Fig. 19. A plurality of power supply lines (1720) are

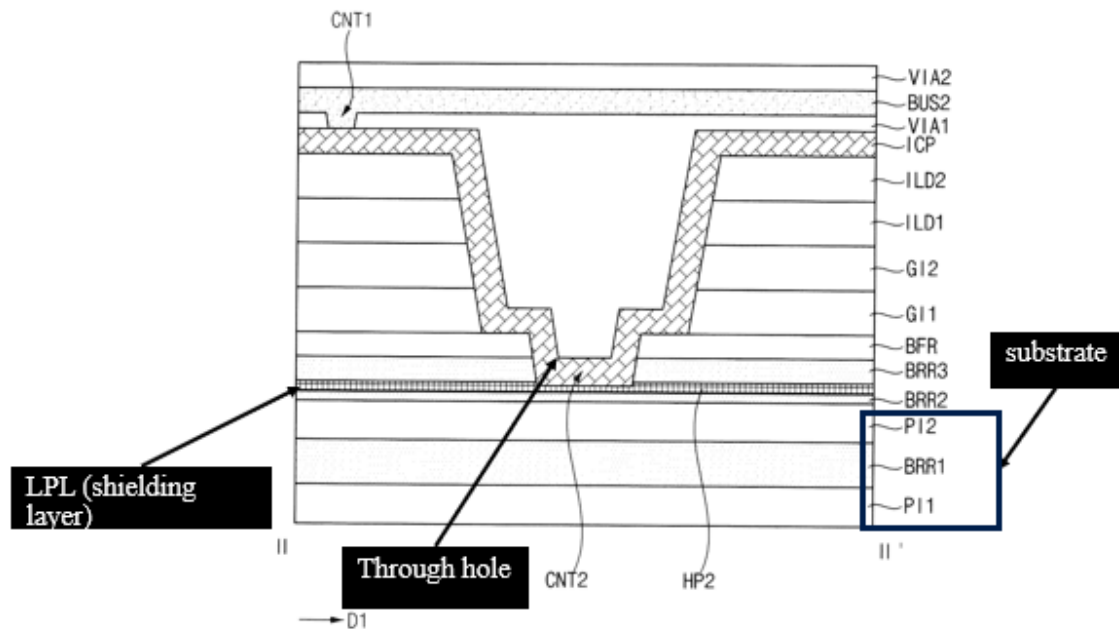
electrically connected to HP2 through a plurality of through holes (CNT2).



Id. Fig. 23 (annotated).

Figure 24 provides a cross sectional view along the line that is boxed in Figure 23, above:

FIG. 24



Id. Fig. 24 (annotated).

As Yi1 explains, “the second horizontal pattern HP2 may contact an intermediate connection pattern ICP *through a second contact hole CNT2*,” which in turn contacts BUS2 and the power lines. Ex-1005, 20:55–59; Ex-1002, ¶¶87–89. Figure 24 shows that the power lines are “disposed on a side of the shielding layer away from the substrate,” as they pass through CNT2 on the layers above the substrate. Ex-1002, ¶89.

Accordingly, Yi1 teaches a plurality of power supply lines (PL1-3; 1720) that are disposed on a side of the shielding layer away from the substrate (Ex-1005, Fig. 24), and the plurality of power supply lines are electrically connected to the

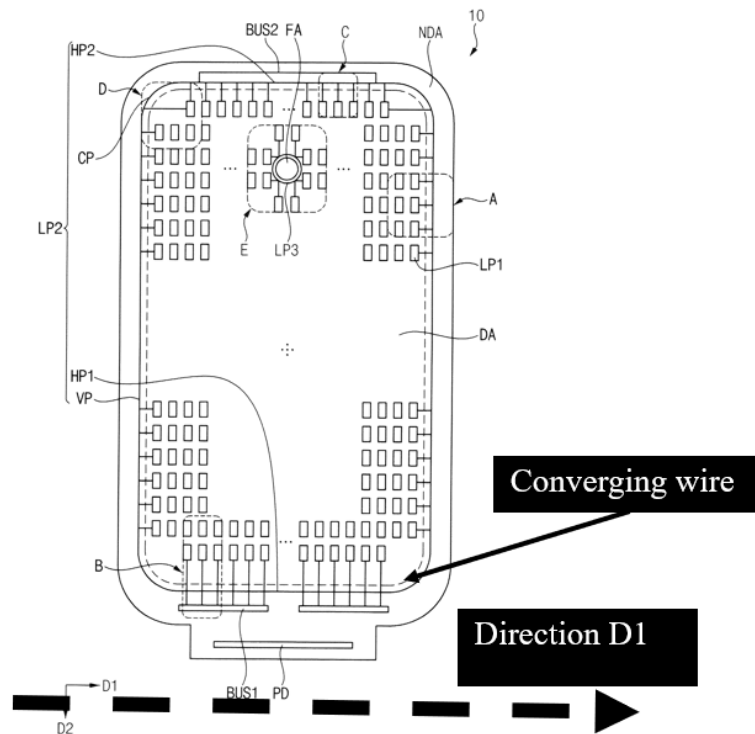
converging wire (HP2) through the plurality of through holes (CNT2). Ex-1002,
¶89.

- f. 1[e]: wherein the converging wire between two adjacent ones of the plurality of through holes is disposed according to a shortest distance between the two adjacent through holes.**

Yil teaches Element 1[e]. Ex-1002, ¶¶90–91.

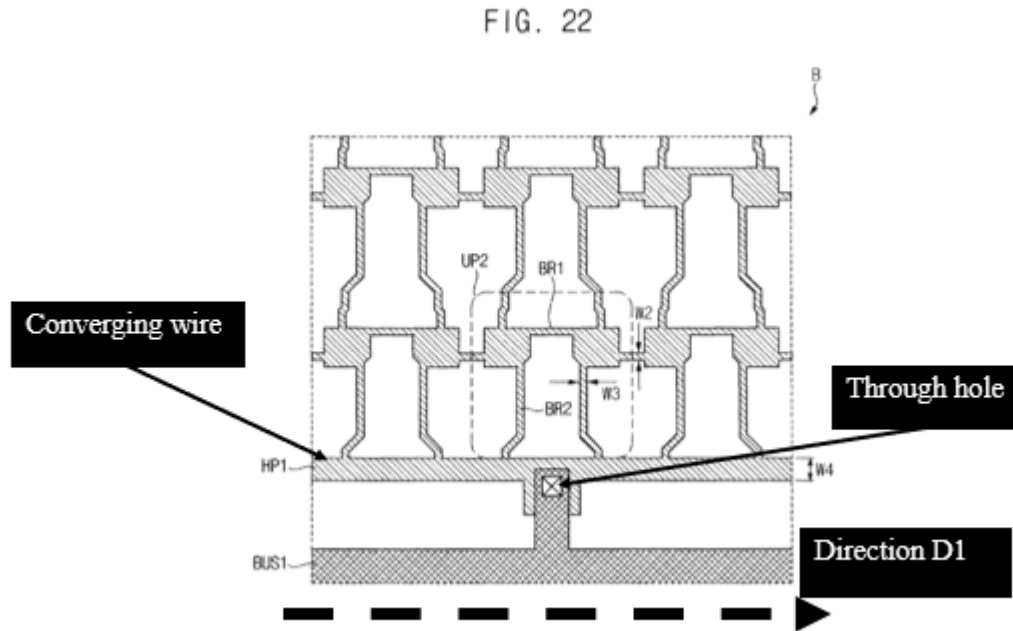
Figure 19 illustrates HP1, connected to the power voltage bus BUS1:

FIG. 19

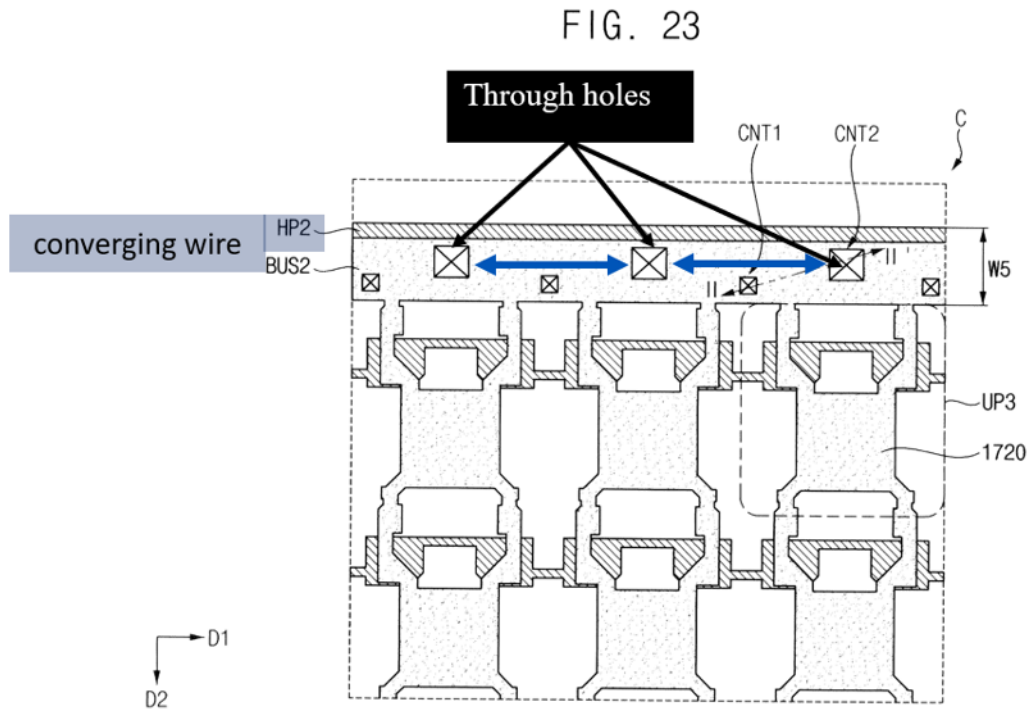


Ex-1005, Fig. 19 (annotated).

HP1 extends linearly in one linear direction (D1), and HP1 is connected with through holes. Figure 22 illustrates this connection:



Id. Fig. 22 (annotated).



Id. Fig. 23 (annotated).

Figure 22 is an enlarged view illustrating a portion of Figure 19. Ex-1005, 20:20–21. As Dr. Lebby explains, these patterns repeat as shown in Figure 19. Ex-1002, ¶91. Yi1 notes that HP1 is “disposed at the bottom of the mesh shape and may extend in the first direction D1.” Ex-1005, 19:30–32. As HP1 extends in one linear direction (D1), without any additional loops, kinks, or other geometric variations, it is disposed along a straight line according to the shortest distance between adjacent through holes. Ex-1002, ¶91. As Dr. Lebby further explains, this linear routing is the most obvious and predictable layout for a converging wire, as it minimizes wire resistance, reduces parasitic capacitance, and eliminates

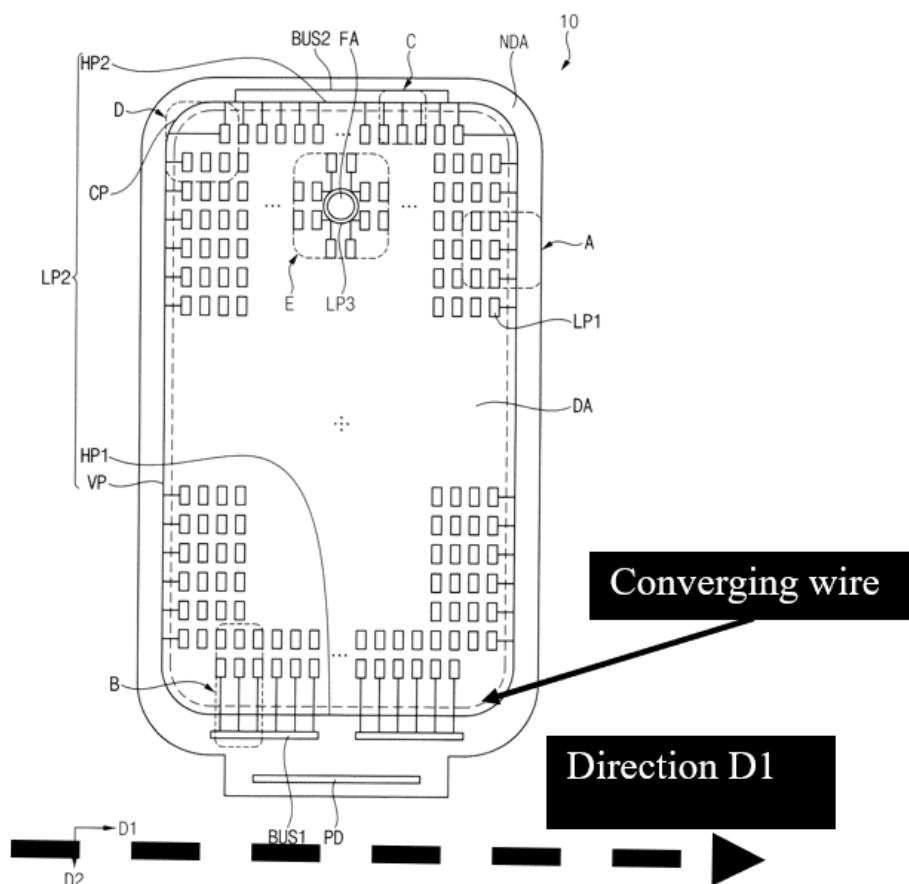
unnecessary current path deviations that could create charge accumulation points—precisely the ESD problem the '429 Patent purports to solve. Ex-1002, ¶91. That is to say that the shortest distance between two points is a straight line. Ex-1002, ¶91.

2. Claim 2: The display panel according to claim 1, wherein the converging wire between the two adjacent through holes is linear in arrangement.

Yi1 teaches the additional limitation in Claim 2. Ex-1002, ¶92.

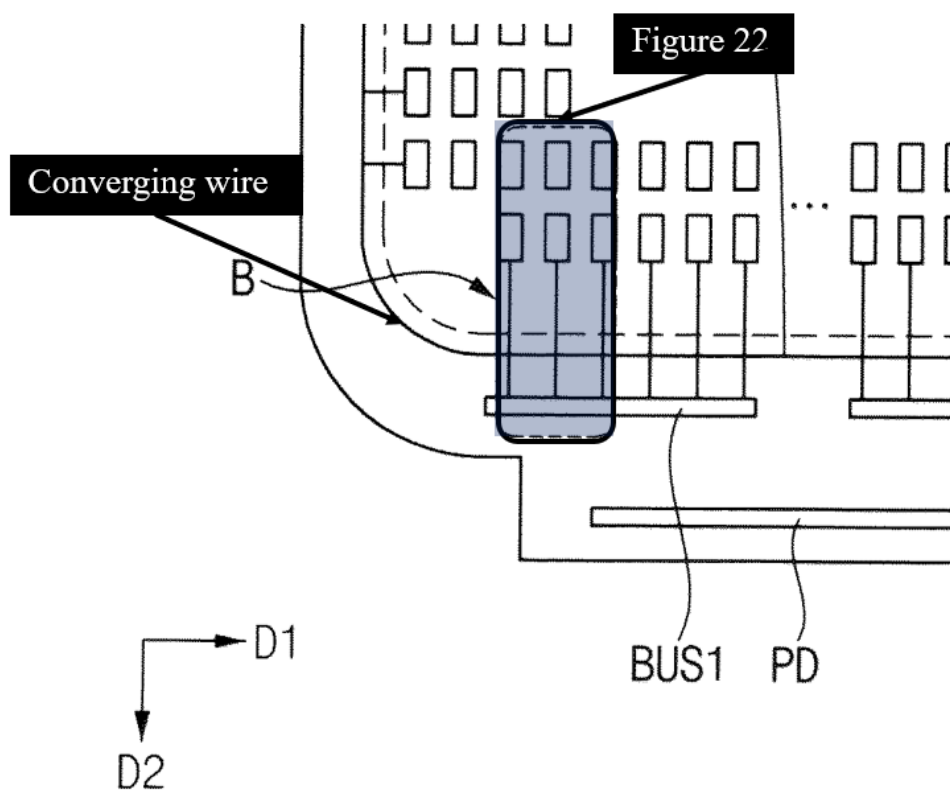
As described in Section XII.A.1.f, the horizontal pattern HP1 extends linearly in one direction. Figure 19 demonstrates that it extends linearly through adjacent through holes:

FIG. 19



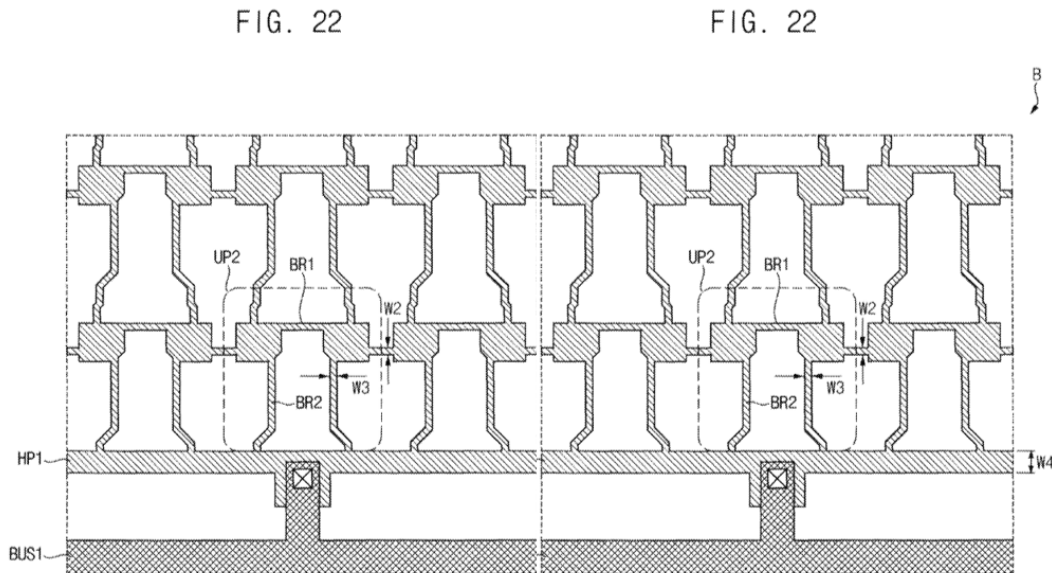
Ex-1005, Fig. 19 (annotated).

Figure 22 illustrates this linear relationship. Figure 22 is an enlarged view illustrating a portion of Figure 19, which is highlighted below. Ex-1005, 20:20–21.



Id. Fig. 19 (annotated; cropped).

Accordingly, multiple copies of Figure 22 can be aligned to showcase the linear relationship between through holes:



Id. Fig. 22 (modified).

As can be seen from the above, when aligned, HP1 is extending in one linear direction between the two adjacent through holes.

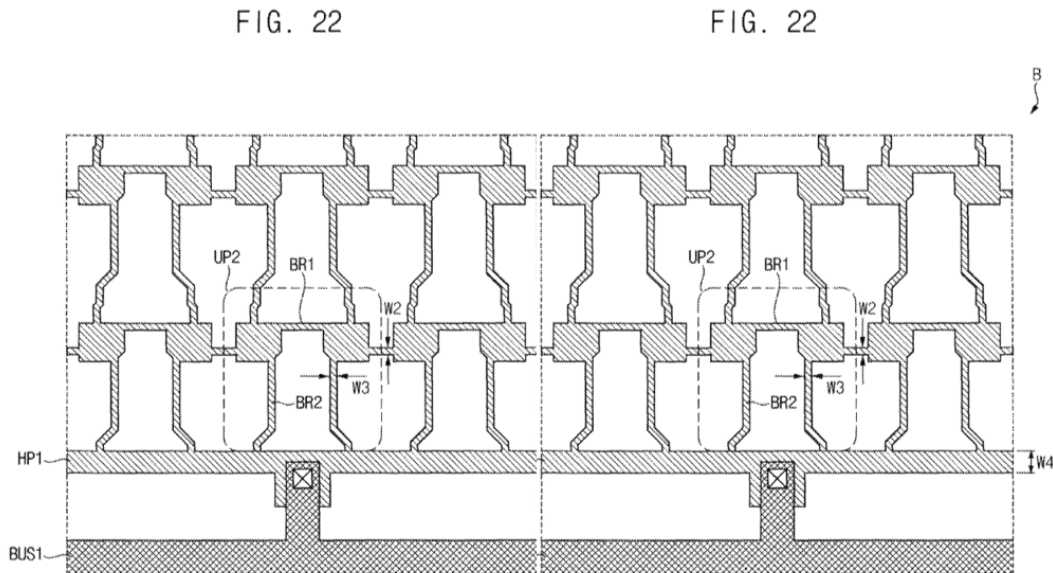
Accordingly, Yi1 renders Claim 2 obvious. Ex-1002, ¶¶93–94.

3. **Claim 3: The display panel according to claim 2, wherein the converging wire is linear in arrangement and the plurality of through holes overlappingly disposed on the converging wire are linear in arrangement.**

Yi1 teaches the additional limitations found in Claim 3. Ex-1002, ¶95.

As was shown in Section XII.A.2, when aligning multiple copies of Figure 22 to showcase a plurality of through holes disposed on converging wire HP1, the converging wire is linear and the through holes are disposed linearly. Similarly, Figure 24 shows HP2 disposed linearly, with a plurality of through holes

overlappingly disposed on the converging wire in a linear arrangement. A POSITA would have recognized that this arrangement would be similar around the display. Ex-1002, ¶95.



Ex-1005, Fig. 22 (duplicated).

Accordingly, Yi1 renders Claim 3 obvious. Ex-1002, ¶95.

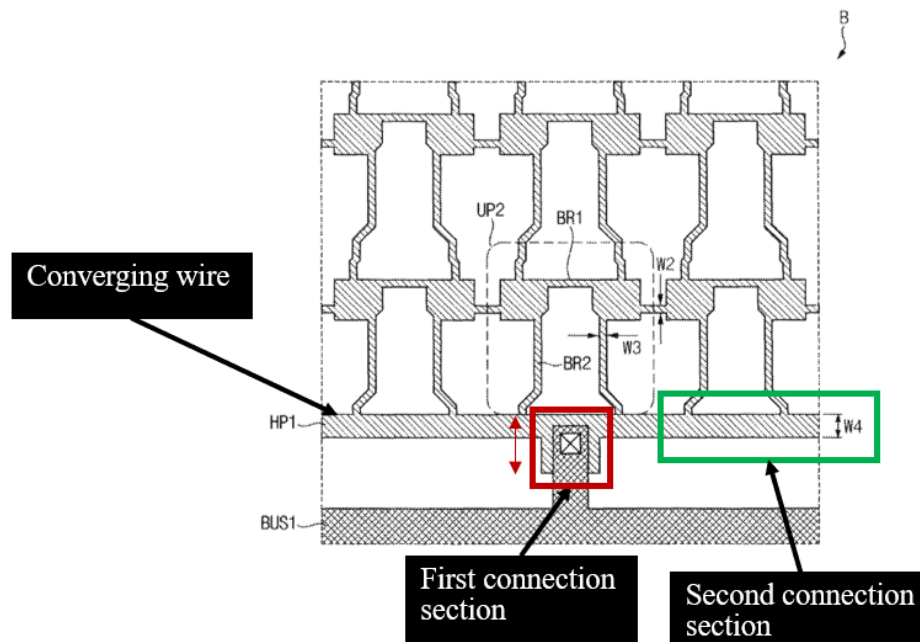
4. **Claim 4: The display panel according to claim 1, wherein the converging wire comprises a first converging wire, and the first converging wire comprises a plurality of first connection sections and a plurality of second connection sections; wherein each of the plurality of second connection sections is connected between a middle portion of two adjacent first plurality of connection sections, a width of each of the plurality of first connection sections is greater than a width of each of the plurality of second connection sections, and the plurality of power supply lines are electrically connected to the plurality of first connection sections through the plurality of through holes.**

Yi1 teaches the additional limitations found in Claim 4. Ex-1002, ¶96.

Claim 4 requires the converging wire to include a plurality of “first connection sections” which are wider than a plurality of “second connections.” *Id.* ¶96. Power supply lines connect to the converging wire through the first connection sections, and the second connection sections are disposed in between two adjacent first connection sections. *Id.*

First, Yi1 teaches that the converging wire comprises a first converging wire, comprising a plurality of first connection sections and a plurality of second connections sections. The first horizontal pattern (HP1) is a first converging wire, as detailed in Section XII.A.1.c. Figure 22 demonstrates that HP1 comprises a plurality of first connections sections (red box, which width noted by red arrow) and second connection sections (green box, which width noted by arrow labeled W4):

FIG. 22

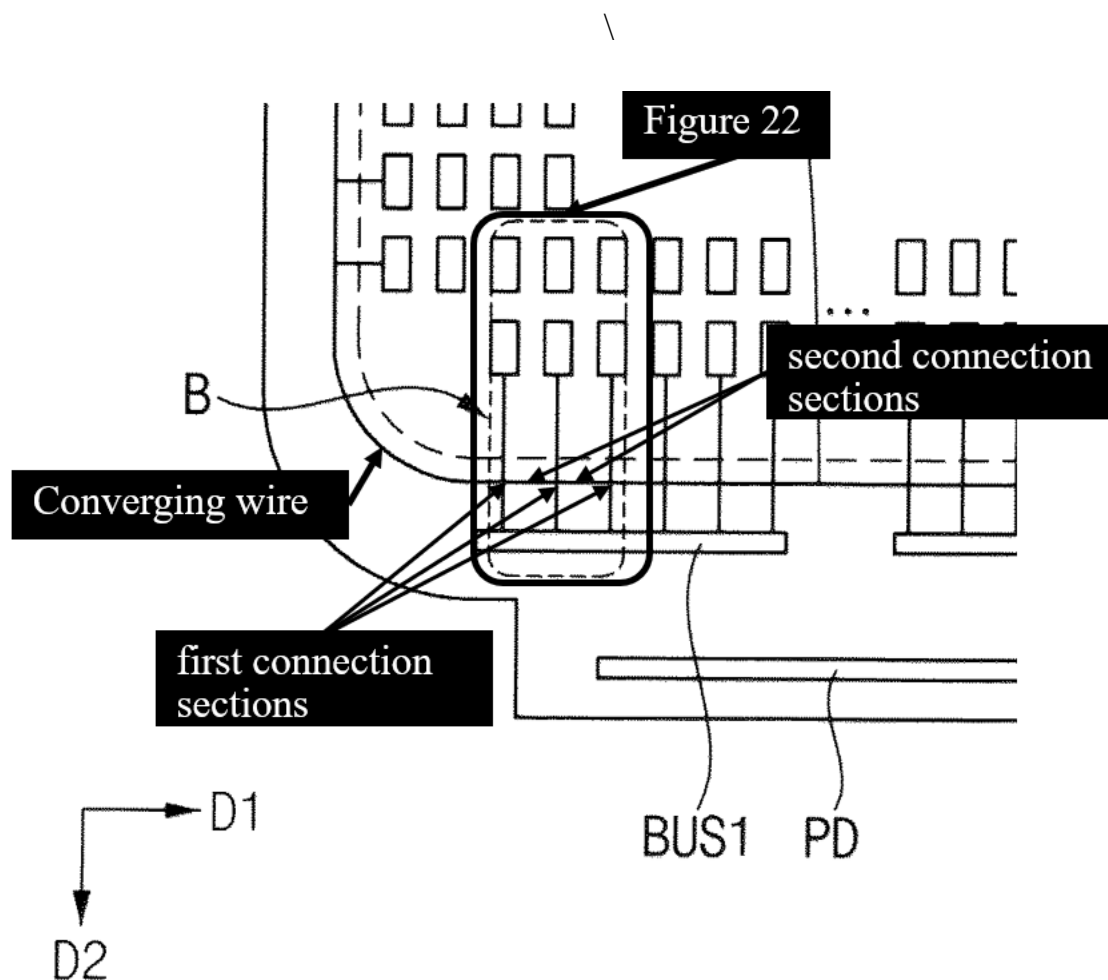


Ex-1005, Fig. 22 (annotated).

In the first connection section (red), HP1 is “connected to the power voltage bus BUS1, and the power voltage ELVDD” is provided to HP1. Ex-1005, 20:34–37. In the second connection section (green), HP1 is connected to the “unit patterns UP2 disposed at the bottom of the mesh shape among the unit patterns UP.” Ex-1005, 20:24–26.

Second, Y11 teaches that each of the plurality of second connection sections is connected between a middle portion of two adjacent first plurality of connection sections. Figure 22, which details a part of Figure 19, illustrates the connection sections. As the enlarged portion of Figure 19 demonstrates, each plurality of second connection sections (*i.e.*, the connections between unit patterns and HP1) is

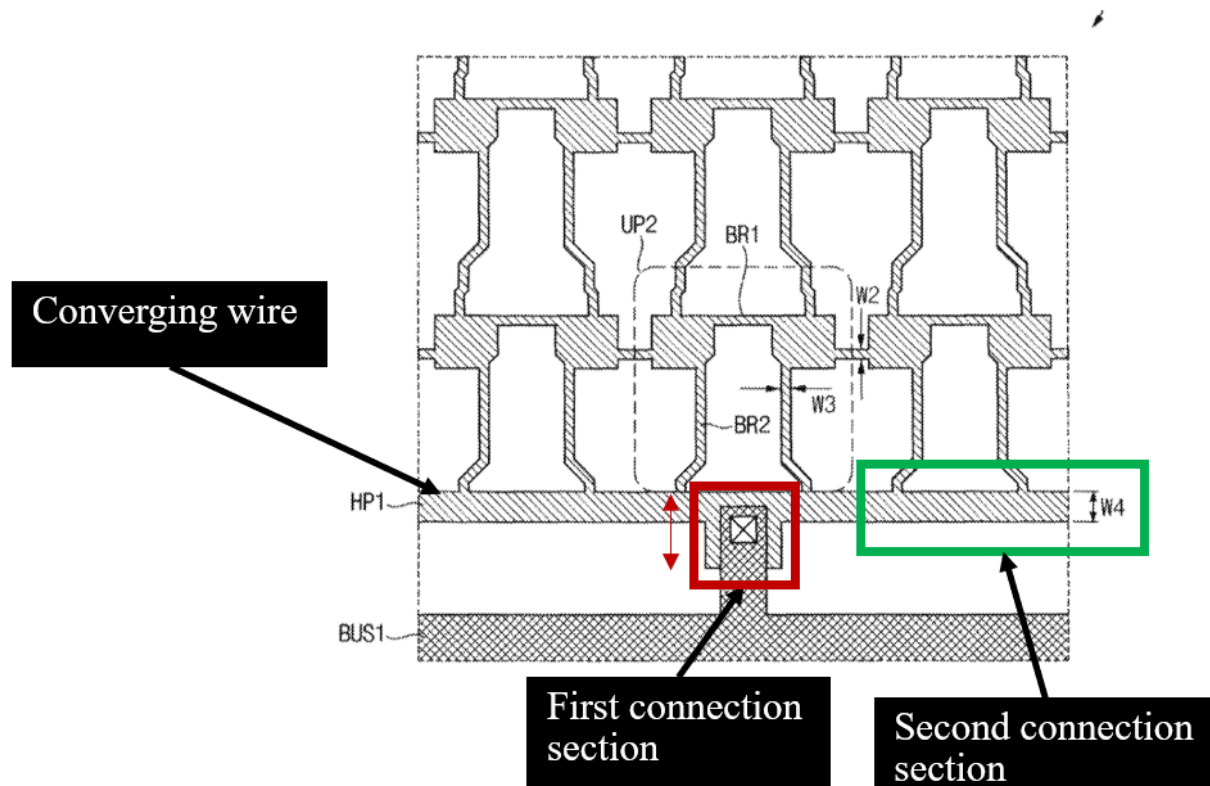
between two adjacent first connection sections (*i.e.*, where HP1 connects to BUS1).



Ex-1005, Fig. 19 (annotated; cropped).

Third, Yi1 teaches that “a width of each of the plurality of first connection sections is greater than a width of each of the plurality of second connection sections[.]” Ex-1001, 9:34–36. Looking again at Figure 22, Yi1 describes several widths: W3 is the width of the bridges between the shielding blocks and HP2, and W4 [green box] is the width of HP1 (the converging wire). Yi1 states that the

“first horizontal pattern HP1 may have a fourth width W4 in the section direction D2. The fourth width W4 may be greater than the second width W2 and the third width W3.” Ex-1005, 20:30–33. As seen in Figure 22, the width in the second connection section is W4 (green box). And the width in the first connection section (red arrow) is wider than W4, since it contains the through hole to BUS1, and is wider in an overlap region between HP1 and BUS1. Ex-1002, ¶99. This width differentiation is routine—wider sections at via landing locations reduce contact resistance and improve yield and via integrity. As a basic principle in TFT backplane design, adequate contact area at through-hole locations helps avoid resistive opens and yield loss. Ex-1002, ¶99.



Ex-1005, Fig. 22 (annotated).

Fourth, Yi1 teaches that the “plurality of power supply lines are electrically connected to the plurality of first connection sections through the plurality of through holes.” Ex-1001, 9:37–39. As Figure 22 above illustrates, the first connection section features a through hole (marked with an X).

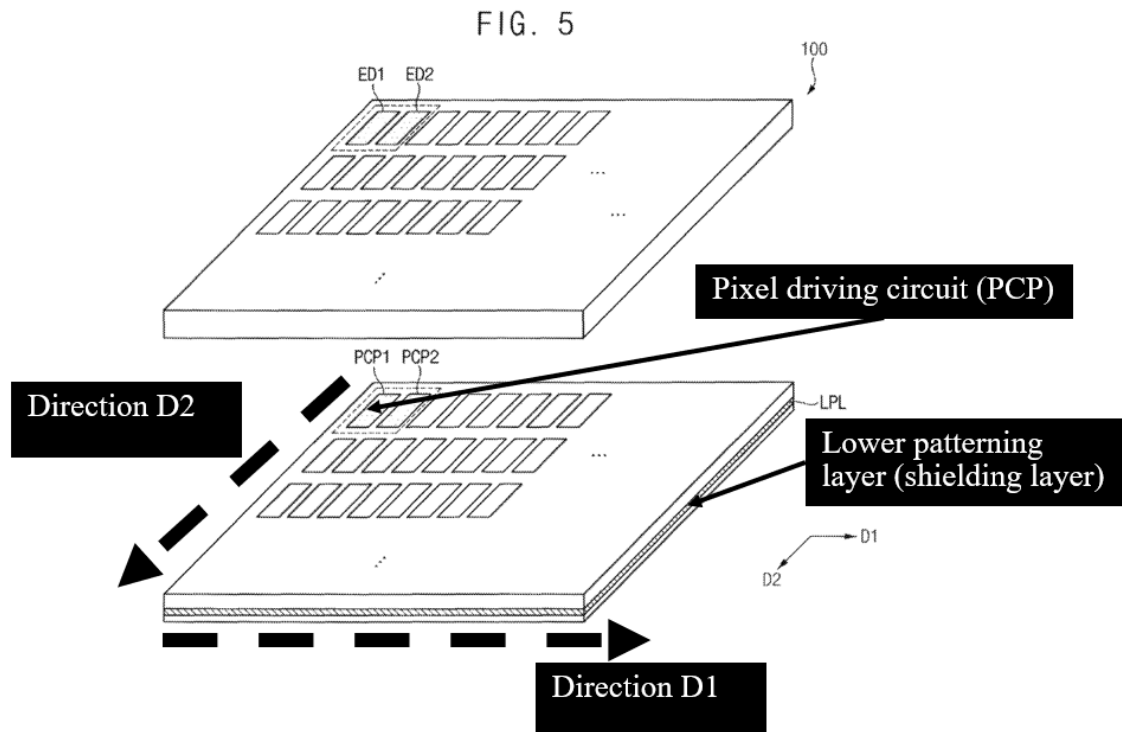
5. **Claim 5: The display panel according to claim 4, wherein the plurality of pixel driving circuits are arranged in an array in a first direction and a second direction, each of the plurality of first connection sections is electrically connected to the plurality of shielding blocks corresponding to a column of the plurality of pixel driving circuits arranged along a first direction.**

Yi1 teaches the additional limitations found in Claim 5. Ex-1002, ¶101.

First, Yi1 teaches that the “plurality of pixel driving circuits are arranged in an array in a first direction and a second direction.” Ex-1001, 9:41–42. Figure 5 is a “perspective view illustrating a display panel,” showcasing the pixel circuit parts that correspond to pixel circuits. Ex-1005, 10:22–33. These pixel circuits are arranged in a grid along D1 and D2, the two directions shown in the lower right hand corner of the figure. Ex-1002, ¶102.

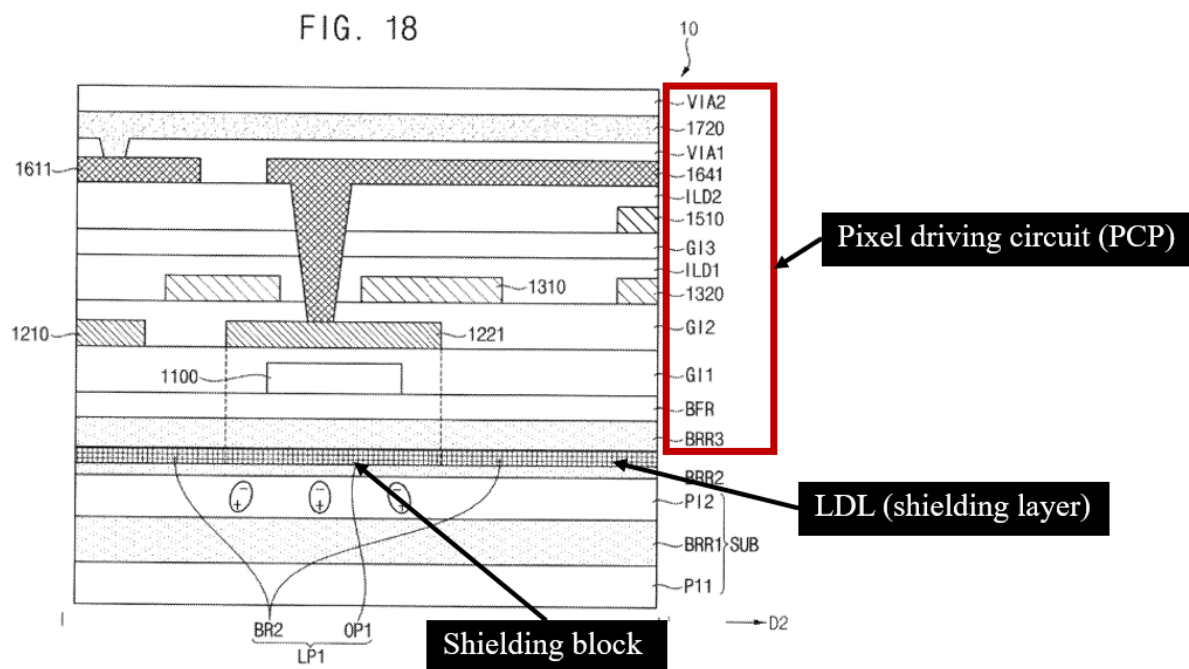
Second, Yi1 teaches that each of the plurality of first connections sections is electrically connected to the plurality of shielding blocks. *See supra* Section XII.A.4.

Third, Yi1 teaches that the plurality of shielding blocks correspond to a column of the plurality of pixel driving circuits arranged along the first direction. As demonstrated in Figure 5, the lower pattern layer that is comprised of the shielding blocks are below the pixel circuits.

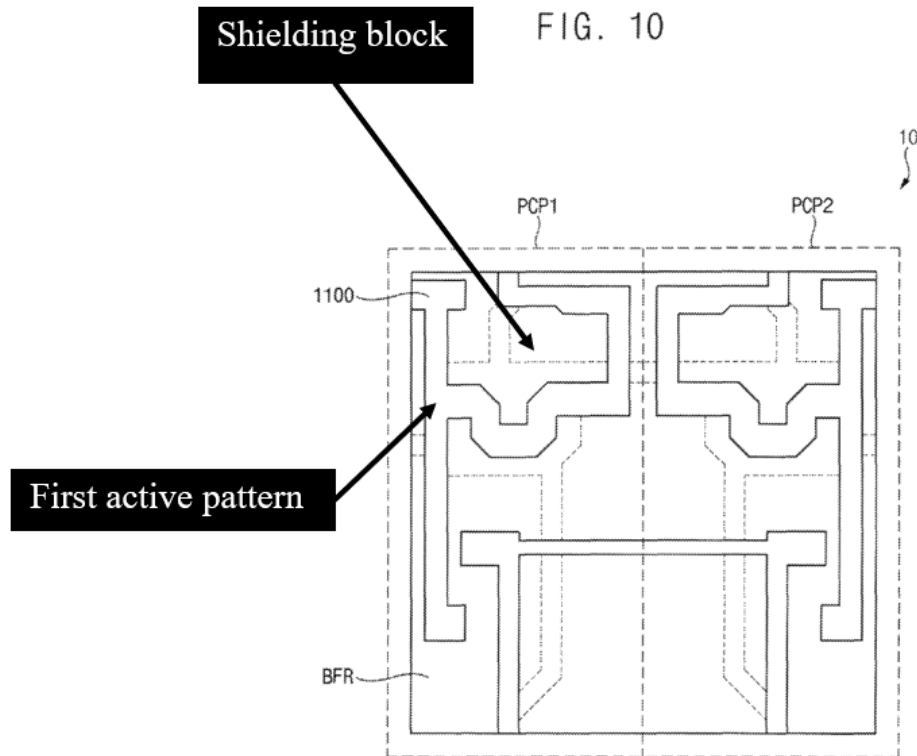


Ex-1005, Fig. 5 (annotated).

Figures 10 and 18 illustrate that the shielding blocks correspond to a column of the plurality of pixel driving circuits. Figure 18 provides a side view show the LDL, the claimed shielding layer, beneath a PCP, the claimed pixel driving circuit. Figure 10 shows that each PCP has a corresponding overlap with a shielding block.



Id. Fig. 18 (annotated).



Id. Fig. 10 (annotated).

As made plain by considering Figures 5 and 10 together, PCP1 and PCP2 are electrically connected in a column oriented along direction D1. The repeated Figure 22 also illustrates that the plurality of first connection sections are electrically connected to the plurality of shielding blocks: HP1 electrically connects the shielding blocks to the first connection sections. Accordingly, Yil renders Claim 5 obvious. Ex-1002, ¶¶104–107.

6. Claim 9

- a. 9[pre]: The display panel according to claim 1, wherein the pixel driving circuit layer comprises:**

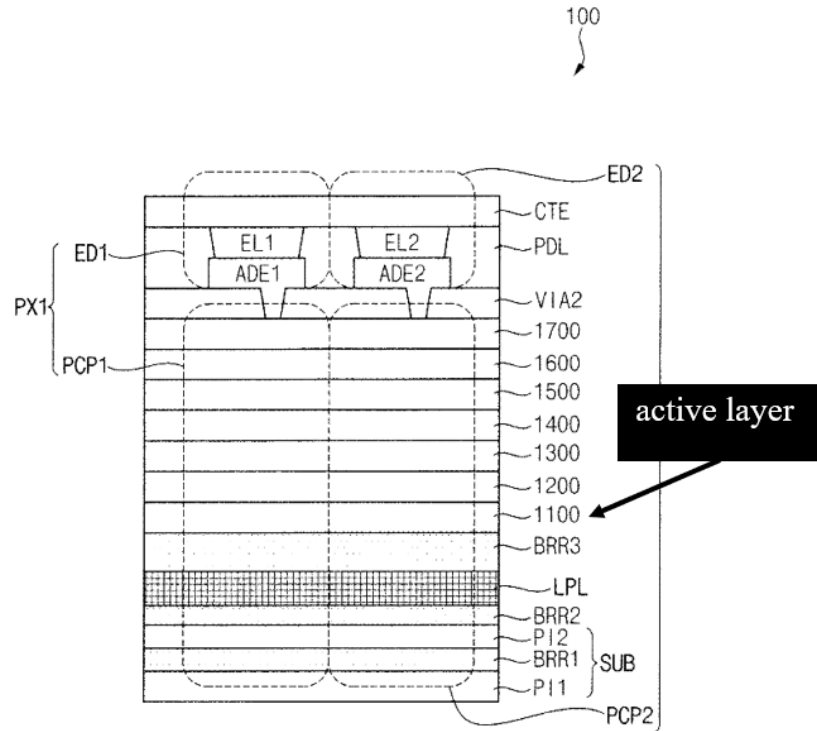
Yi1 teaches Element 9[pre]. Ex-1002, ¶108. As detailed in Section XII.A.1.d, Yi1 teaches a pixel driving circuit layer (the pixel circuit part PCP) located on the shielding layer (the LPL). Figures 4 and 18 illustrate the layer stack of the pixel driving circuit layer, which includes each of the layers recited in Elements 9[a]-9[g], as detailed below. Ex-1005, Figs. 4, 18; Ex-1002, ¶109.

- b. 9[a]: a semiconductor layer disposed on a side of the shielding layer away from the substrate;**

Yi1 teaches Element 9[a]. Ex-1002, ¶110.

Yi1's first active pattern 1100 is a semiconductor layer disposed on a side of the shielding layer (the LPL) away from the substrate: the first active pattern 1100 is disposed on the buffer layer BFR, which is disposed on the third barrier layer BRR3 covering the LPL, and the first active pattern 1100 "may include a silicon semiconductor." Ex-1005, 12:65–13:12. Figure 4 shows this active pattern in the stackup:

FIG. 4



Id. Fig. 4 (annotated).

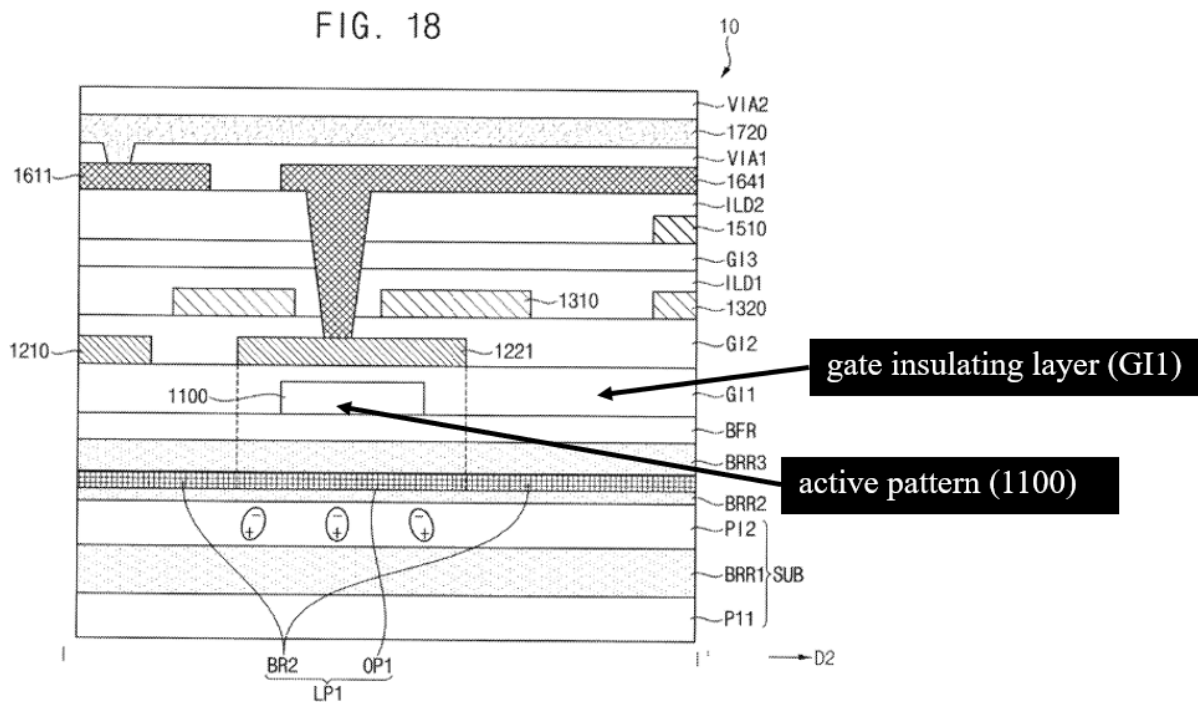
Accordingly, Yi1 teaches this limitation. Ex-1002, ¶¶110–111.

- c. **9[b]: a first insulating layer disposed on a side of the semiconductor layer away from the substrate;**

Yi1 teaches Element 9[b]. Ex-1002, ¶112.

Yi1’s first gate insulating layer GI1 is a first insulating layer disposed on a side of the semiconductor layer away from the substrate: the first gate insulating layer GI1 “may cover the first active pattern 1100 and may be disposed on the buffer layer BFR.” Ex-1005, 13:13–23. Figure 18, which shows both insulating

and active layers based on a cross section of the display device from Figure 1,
shows the gate insulating layer on top of the active pattern:



Id. Fig. 18 (annotated).

Accordingly, Yi1 teaches this limitation. Ex-1002, ¶113.

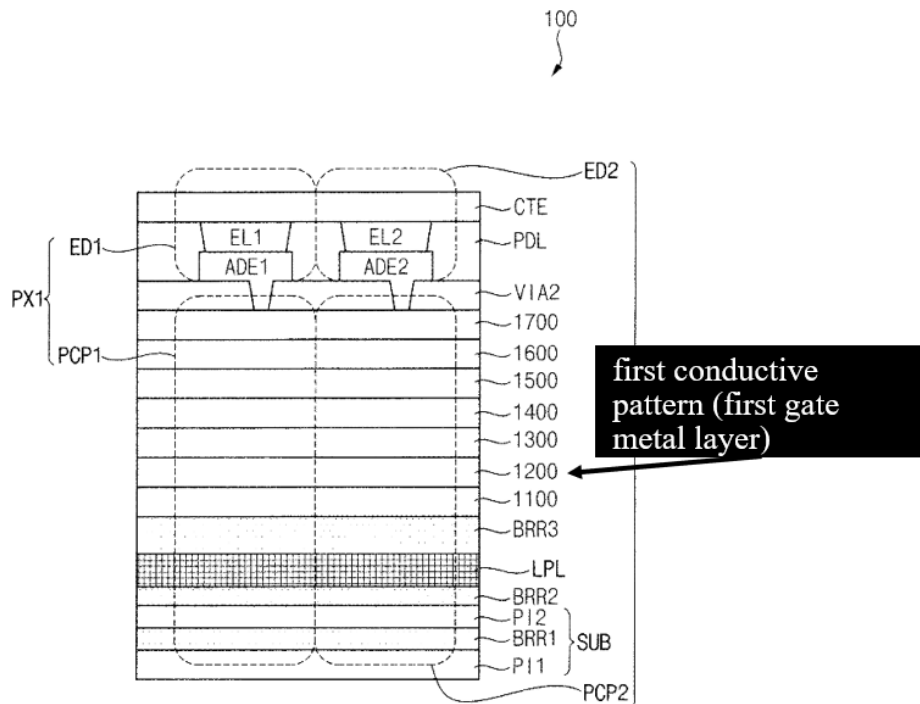
- d. **9[c]: a first gate metal layer disposed on a side of the first insulating layer away from the substrate;**

Yi1 teaches Element 9[c]. Ex-1002, ¶114.

Yi1's first conductive pattern 1200 is a first gate metal layer disposed on a side of the first insulating layer away from the substrate: "the first conductive pattern 1200 may be disposed on the first gate insulating layer GI1" and includes

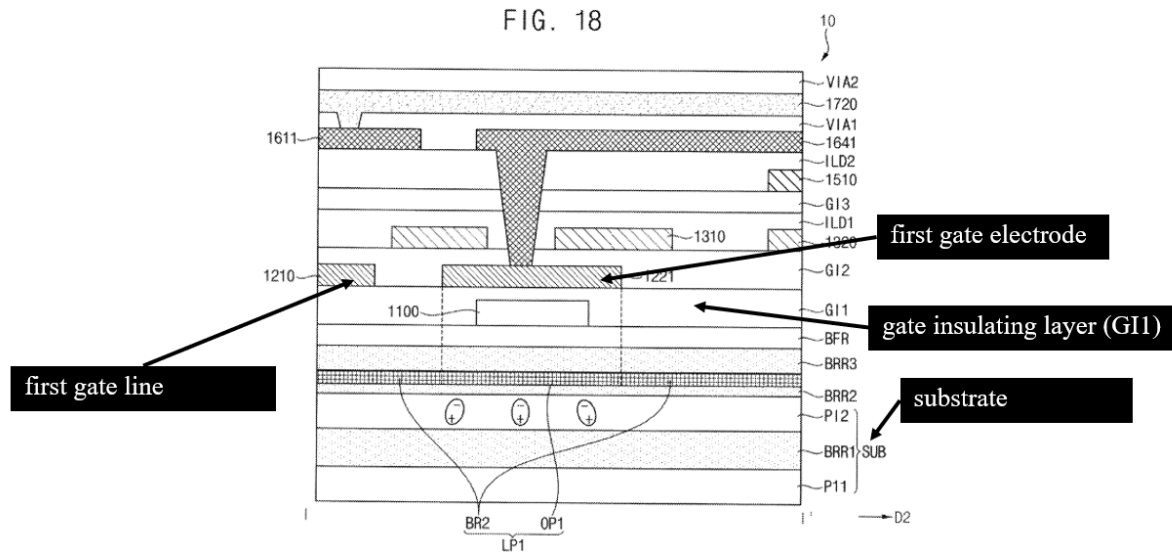
the first gate line 1210, the first and second gate electrodes 1221 and 1222, and the fourth gate line 1230. Ex-1005, 13:28–54. The first conductive pattern can be seen in Figure 4:

FIG. 4



Id. Fig. 4 (annotated).

Figure 18 shows the constituent parts of the first conductive pattern: the first gate line (1210) and the first gate electrode (1221). *Id.* Fig. 18. As Figure 18 confirms, the gate metal layer is disposed on a side of the first insulating layer (GI1) away from the substrate:



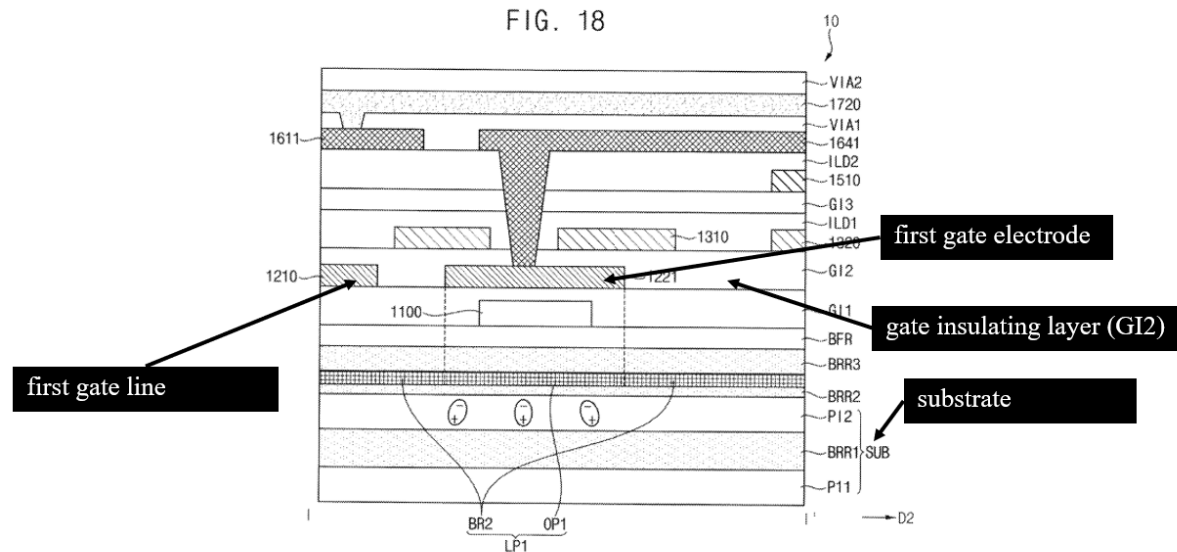
Id. Fig. 18 (annotated).

Accordingly, Yi1 teaches this claim limitation. Ex-1002, ¶¶114–116.

- e. **9[d]: a second insulating layer disposed on a side of the first gate metal layer away from the substrate;**

Yi1 teaches Element 9[d]. Ex-1002, ¶117.

Yi1’s second gate insulating layer GI2 is a second insulating layer disposed on a side of the first gate metal layer away from the substrate: the second gate insulating layer GI2 “may cover the first conductive pattern 1200 and may be disposed on the first gate insulating layer GI1.” Ex-1005, 14:8–10. Figure 18 shows the second gate insulating layer (GI2) disposed on the first gate metal layer (shown as 1210 and 1221 in Figure 18) on the side away from the substrate:



Id. Fig. 18 (annotated).

Accordingly, Yi1 teaches this limitation. Ex-1002, ¶118.

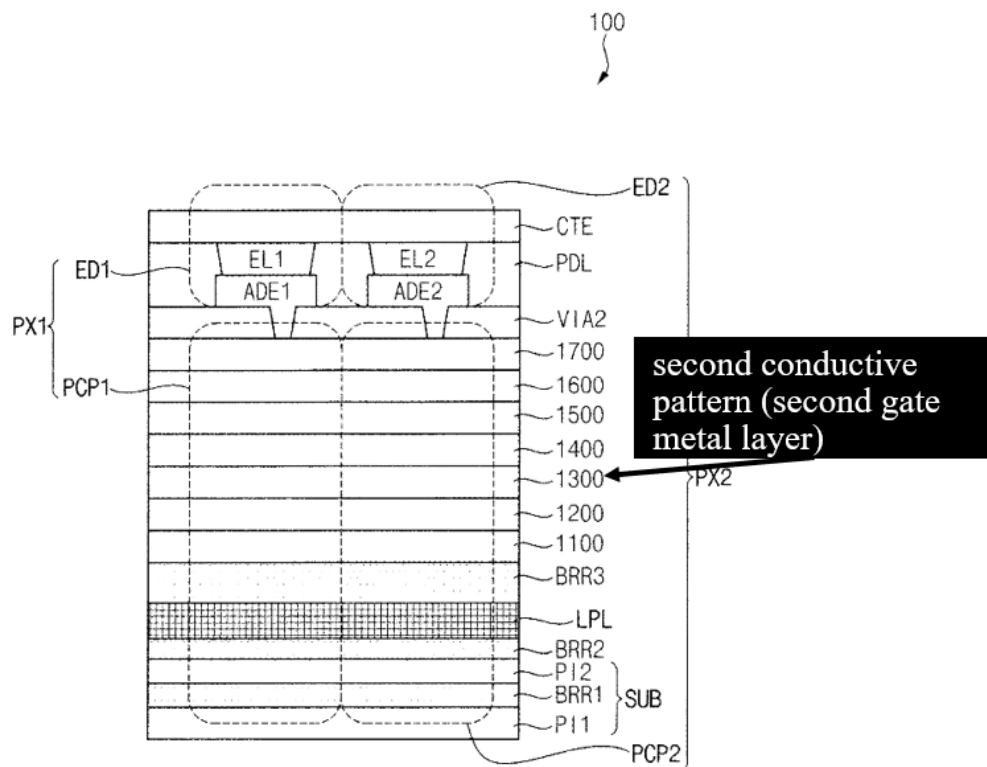
- f. **9[e]: a second gate metal layer disposed on a side of the second insulating layer away from the substrate; and**

Yi1 teaches Element 9[e]. Ex-1002, ¶119.

Yi1's second conductive pattern 1300 is a second gate metal layer disposed on a side of the second insulating layer away from the substrate: "the second conductive pattern 1300 may be disposed on the second gate insulating layer GI2" and includes the storage capacitor electrode 1310, which constitutes the storage capacitor CST together with the first gate electrode 1221. Ex-1005, 14:23–39.

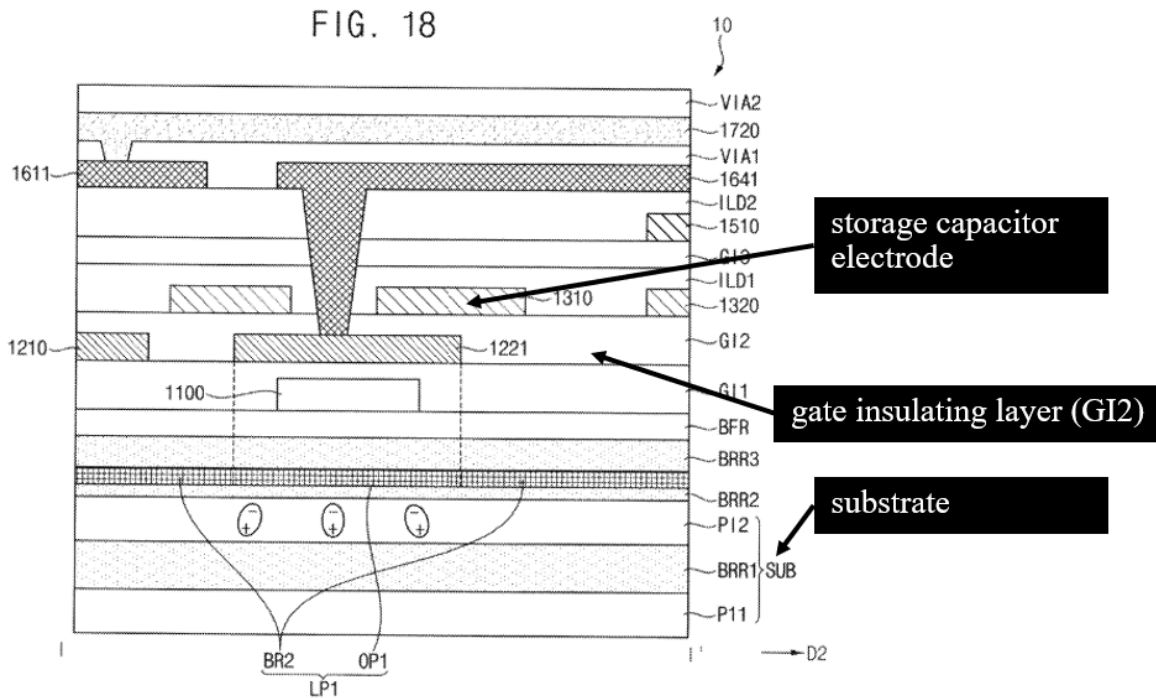
Figure 4 shows the second conductive pattern in the overall stack:

FIG. 4



Id. Fig. 4 (annotated).

Figure 18 also shows the constituent parts of the second conductive pattern, such as the storage capacitor electrode (1310):



Id. Fig. 18 (annotated).

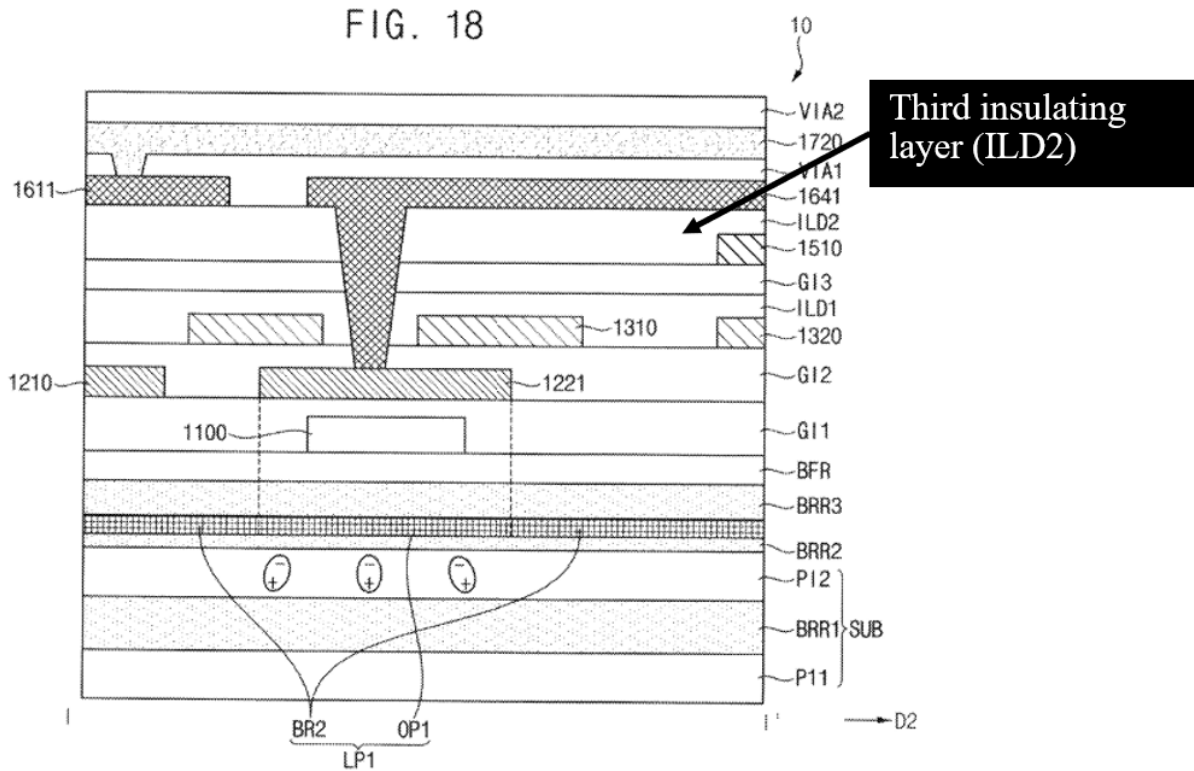
As shown in Figure 18, the second conductive layer (1300, comprising the storage capacitor electrode 1310) is disposed on a side of the second insulating layer (G12) away from the substrate.

Accordingly, Y11 teaches this limitation. Ex-1002, ¶¶119–121.

- g. 9[f]: a third insulating layer disposed on a side of the second gate metal layer away from the substrate;**

Y11 teaches Element 9[f]. Ex-1002, ¶122.

Yi1 teaches a third insulating layer disposed on a side of the second gate metal layer away from the substrate: inter-insulating layer ILD2. Ex-1005, 20:55–21:10. Figure 18 shows the third insulating layer, marked as ILD2:



ILD2 is disposed on a side of the second gate metal layer (1300, comprising electrodes at 1310) away from the substrate, as illustrated in Figure 18 above.

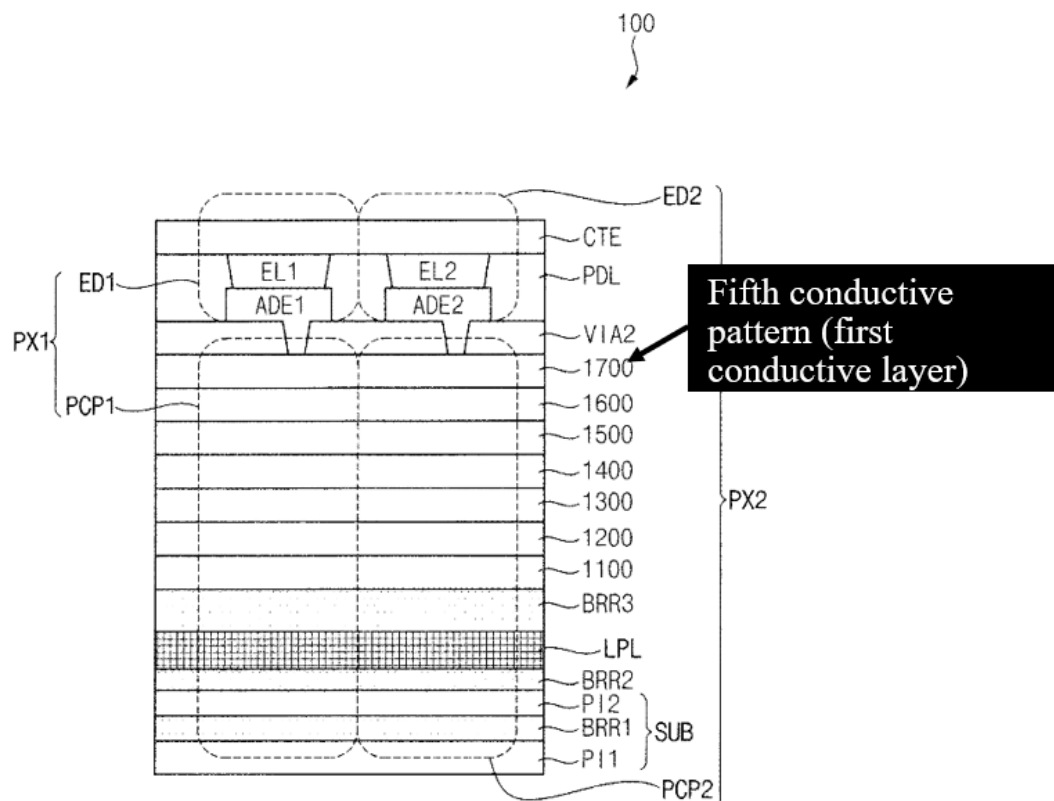
Accordingly, Yi1 teaches this limitation. Ex-1002, ¶123.

- h. 9[g]: wherein the first conductive layer is disposed on a side of the third insulating layer away from the substrate, the plurality of power supply lines of the first conductive layer are electrically connected to the converging wire through the plurality of through holes, and the plurality of through holes penetrate through the first insulating layer, the second insulating layer, and the third insulating layer.**

Yi1 teaches Element 9[g]. Ex-1002, ¶124.

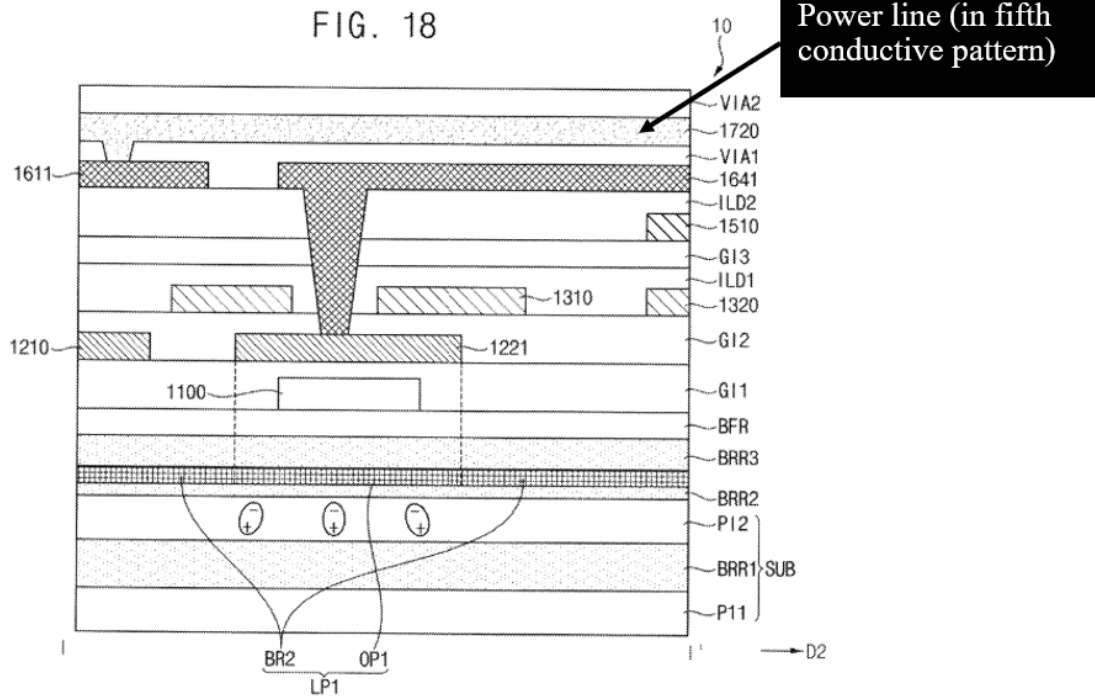
First, Yi1 teaches that the first conductive layer is disposed on a side of the third insulating layer away from the substrate. The fifth conductive pattern 1700, which includes the power voltage line 1720, is disposed above the second inter-insulating layer ILD2 on the first via-insulating layer VIA1, and the power voltage line 1720 “may provide the power voltage ELVDD.” Ex-1005, 17:29–48; *see supra* Section XII.A.1.e. Figure 4 shows the fifth conductive pattern in the stack up:

FIG. 4



Ex-1005, Fig. 4 (annotated).

Figure 18 illustrates that the fifth conductive pattern, comprising the power lines (1720), is located on a side of the third insulating layer (ILD2) away from the substrate:

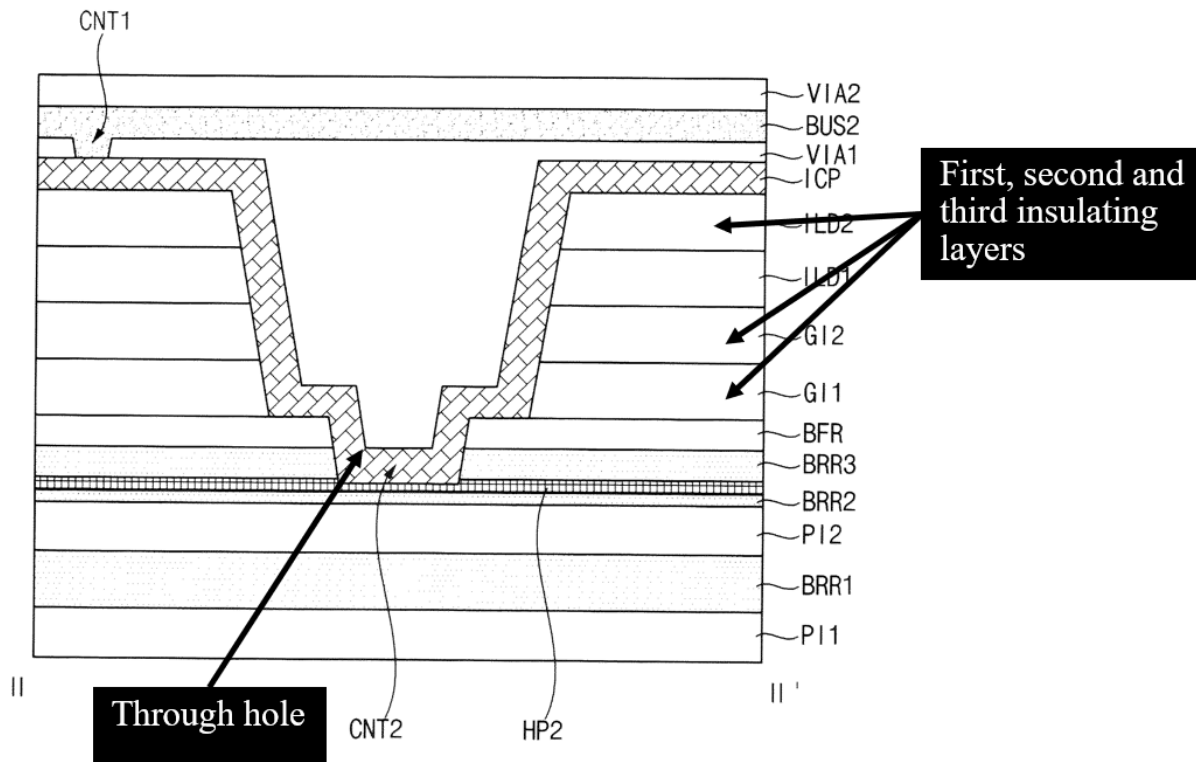


Id. Fig. 18 (annotated).

Second, Yi1 teaches that the plurality of power supply lines of the first conductive layer are electrically connected to the converging wire (HP2) through the plurality of through holes (CNT2), and that the through holes penetrate the first, second, and third insulating layers: the second contact hole CNT2 “may penetrate the third barrier layer BRR3, the buffer layer BFR, the first gate insulating layer GI1, and the second gate insulating layer GI2, the first inter-insulating layer ILD1, the third gate insulating layer GI3, and the second inter-

insulating layer ILD2.” Ex-1005, 20:55–21:10. Figure 24 illustrates CNT2 penetrating through the first, second, and third insulating layers:

FIG. 24



Id. Fig. 24 (annotated).

Accordingly, Yi1 teaches this limitation. Ex-1002, ¶¶127–128.

7. **Claim 11: A display device comprising the display panel as claimed in claim 1, wherein the display panel is an organic light-emitting diode (OLED) panel.**

Yi1 teaches the additional limitations found in Claim 11. Ex-1002, ¶129.

Yi1 teaches that “the first emitting diode ED1 may correspond to the first organic light emitting diode OLED1.” Ex-1005, 10:28–36. The first organic light

emitting diode OLED1 “may generate light based on the driving current” provided by the first pixel circuit PC1, and each of the second and third pixels has substantially the same structure. Ex-1005, 7:15–22. Because the emitting diodes of Yi1’s display panel are organic light emitting diodes, the display panel is an OLED panel. Ex-1002, ¶129.

8. **Claim 12: The display device according to claim 11, wherein the converging wire between the two adjacent through holes is linear in arrangement.**

Disclosed. *See supra* Section XII.A.2.

9. **Claim 13: The display device according to claim 12, wherein the converging wire is linear in arrangement and the plurality of through holes overlappingly disposed on the converging wire are linear in arrangement.**

Disclosed. *See supra* Section XII.A.3.

10. **Claim 14: The display device according to claim 11, wherein the converging wire comprises a first converging wire, and the first converging wire comprises a plurality of first connection sections and a plurality of second connection sections; wherein each of the plurality of second connection sections is connected between a middle portion of two adjacent first plurality of connection sections, a width of each of the plurality of first connection sections is greater than a width of each of the plurality of second connection sections, and the plurality of power supply lines are electrically connected to the plurality of first connection sections through the plurality of through holes.**

Disclosed. *See supra* Section XII.A.4.

11. **Claim 15: The display device according to claim 14, wherein the plurality of pixel driving circuits are arranged in an array in a first direction and a second direction, each of the plurality of first connection sections is electrically connected to the plurality of shielding blocks corresponding to a column of the plurality of pixel driving circuits arranged along a first direction.**

Disclosed. *See supra* Section XII.A.5.

12. **Claim 19**

- a. **19[pre]: The display device according to claim 11, wherein the pixel driving circuit layer comprises:**

Disclosed. *See supra* Section XII.A.6.a.

- b. **19[a]: a semiconductor layer disposed on a side of the shielding layer away from the substrate;**

Disclosed. *See supra* Section XII.A.6.b.

- c. **19[b]: a first insulating layer disposed on a side of the semiconductor layer away from the substrate;**

Disclosed. *See supra* Section XII.A.6.c.

- d. **19[c]: a first gate metal layer disposed on a side of the first insulating layer away from the substrate;**

Disclosed. *See supra* Section XII.A.6.d.

- e. **19[d]: a second insulating layer disposed on a side of the first gate metal layer away from the substrate;**

Disclosed. *See supra* Section XII.A.6.e.

- f. **19[e]: a second gate metal layer disposed on a side of the second insulating layer away from the substrate; and**

Disclosed. *See supra* Section XII.A.6.f.

- g. **19[f]: a third insulating layer disposed on a side of the second gate metal layer away from the substrate;**

Disclosed. *See supra* Section XII.A.6.g.

- h. **19[g]: wherein the first conductive layer is disposed on a side of the third insulating layer away from the substrate, the plurality of power supply lines of the first conductive layer are electrically connected to the converging wire through the plurality of through holes, and the plurality of through holes penetrate through the first insulating layer, the second insulating layer, and the third insulating layer.**

Disclosed. *See supra* Section XII.A.6.h.

B. Ground 2: Claims 7–8 and 17–18 Are Rendered Obvious by the Combination of Yi1 and Yi2

1. Motivation to combine

Claims 7 and 17 depend from Claims 1 and 11, respectively, each limitation of which Yi1 discloses as addressed above. *See supra* Sections XII.A.1, XII.A.7.

The combination of Yi1 and Yi2 renders Claims 7 and 17 obvious. A POSITA would have been motivated to combine Yi1 and Yi2. Ex-1002, ¶¶131–132. Yi1 and Yi2 are commonly assigned Samsung Display patent documents sharing inventor Changho Yi, were filed one week apart, and disclose nearly identical lower-pattern/shielding architectures—mesh-shaped lower patterns composed of

unit patterns UP, horizontal/transfer patterns supplying the power voltage ELVDD, and stacked contact holes connecting the power supply lines to the shielding layer. *See supra* Sections XI.A, XI.B. A POSITA implementing Yi1's display device would have naturally looked to Yi2, which describes the same architecture in a closely related application. Yi2 expressly discloses a bending area: "A fan-out line FL may be disposed in the bending area BA, and the bending area BA may be bent." Ex-1006, ¶53, Fig. 1. Incorporating Yi2's bending area BA into Yi1's display panel is the simple combination or substitution of familiar elements according to known methods, yielding no more than predictable results, as flexible OLED panels with bent non-display regions were conventional at the relevant time. Ex-1002, ¶132. As Dr. Lebby explains, by the early 2000s flexible OLED displays were already being demonstrated on polymer substrates, and the industry recognized that OLED's thin, all-solid-state construction made it especially suitable for flexible display devices. *Id.* Bending a portion of the non-display region to fold circuitry underneath the active display was also a well-known approach to achieving thinner bezels in smartphones; OLED's wide-angle emission, solid-state construction, lack of a cell gap, and absence of a separate backlight made it particularly well suited to such bending configurations. *Id.* A POSITA would have had a reasonable expectation of success given the references'

common architecture, common assignee, and substantially the same base technology. *Id.* ¶132.

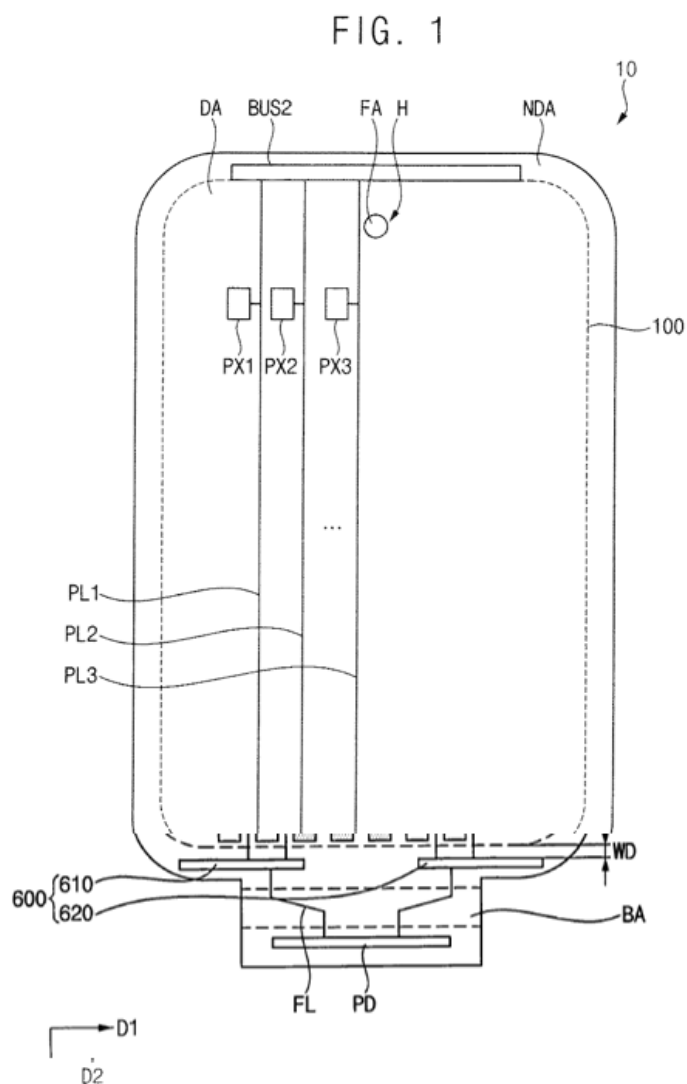
2. Claim 7

- a. 7[a]: The display panel according to claim 1, wherein the non-display region comprises: a first non-display region and a second non-display region disposed on two sides of the display region, wherein the first non-display region comprises a bending sub-region, and the display panel bends at the bending sub-region; and**

The combination of Yi1 and Yi2 teaches Element 7[a]. Ex-1002, ¶¶133–134.

In the combined device, the non-display region comprises a first non-display region and a second non-display region disposed on two sides of the display region. The first non-display region contains Yi2’s bending area BA, and the display panel bends at that bending sub-region: “A fan-out line FL may be disposed in the bending area BA, and the bending area BA may be bent.” Ex-1006, ¶53, Fig.1. The second non-display region is disposed on another side of the display region: as shown in Yi1’s Figures 1 and 19, the power voltage bus BUS1 is disposed in a bottom side of the non-display area NDA, while the power voltage pattern BUS2 is disposed in a top side of the non-display area NDA, on the opposite side of the display area. Ex-1005, 9:58–66, 20:22–42, Figs. 1, 19; Ex-1002, ¶¶135–136. The form of this combination can be seen below, where Figures

1' from both Yi1 and Yi2 are combined to show the bending area from Yi2 applied to the display device taught in Yi1:



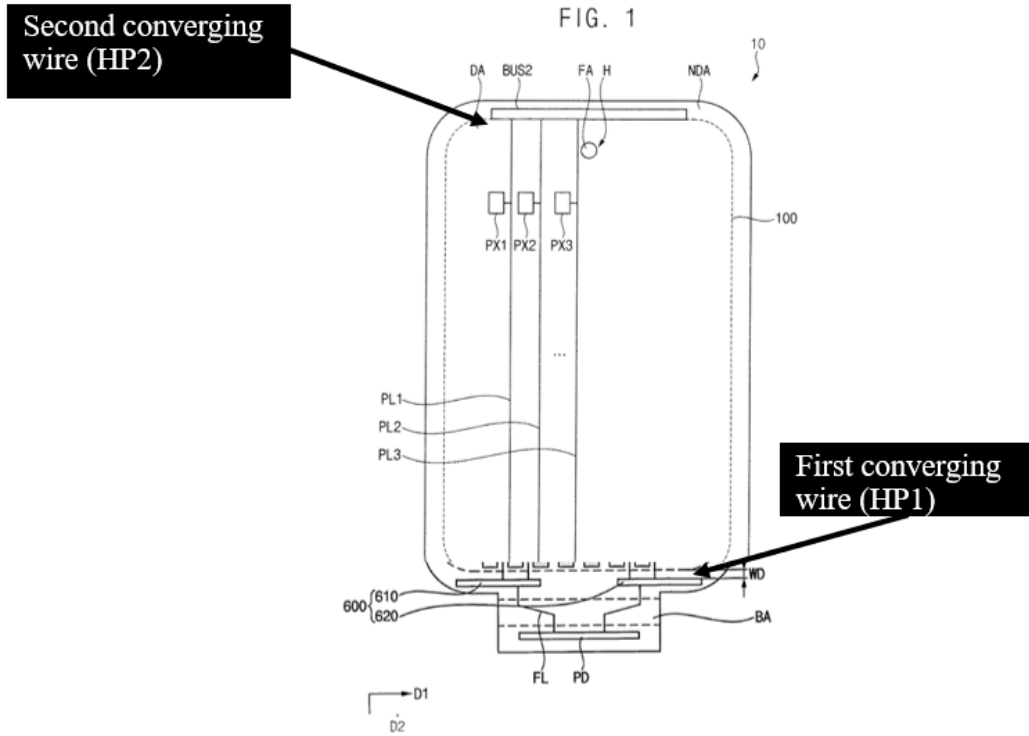
- b. 7[b]: the converging wire comprises a first converging wire arranged in the first non-display region, and the plurality of power supply lines are electrically connected to the plurality of first connection sections at least through the plurality of through holes.**

The combination of Yi1 and Yi2 teaches Element 7[b]. Ex-1002, ¶137. In the combined device, the converging wire comprises a first converging wire arranged in the first non-display region, and the plurality of power supply lines are electrically connected to the plurality of first connection sections at least through the plurality of through holes. As detailed in Section XII.A.1.e, Yi1's second horizontal pattern HP2 contacts the intermediate connection pattern ICP through the second contact hole CNT2, and the ICP in turn contacts the power voltage pattern BUS2—provided together with the power voltage line 1720—through the first contact hole CNT1. Ex-1005, 20:55–21:10, Figs. 23, 24. Additionally or alternatively, Yi2's transfer pattern 700 (including the first pattern 710 and the second pattern 720) directly contacts the second lower pattern LP2 through the contact holes CNT1 and CNT2, and the second pattern 720, integrally formed with the power voltage line 1720, contacts the first pattern 710 through the fourth contact hole CNT4. Ex-1006, ¶¶159–160, 170–171; Ex-1002, ¶¶138–139.

3. **Claim 8: The display panel according to claim 7, wherein the converging wire comprises a second converging wire arranged in the second non-display region, and the plurality of power supply lines are electrically connected to the plurality of second connection sections through the plurality of through holes.**

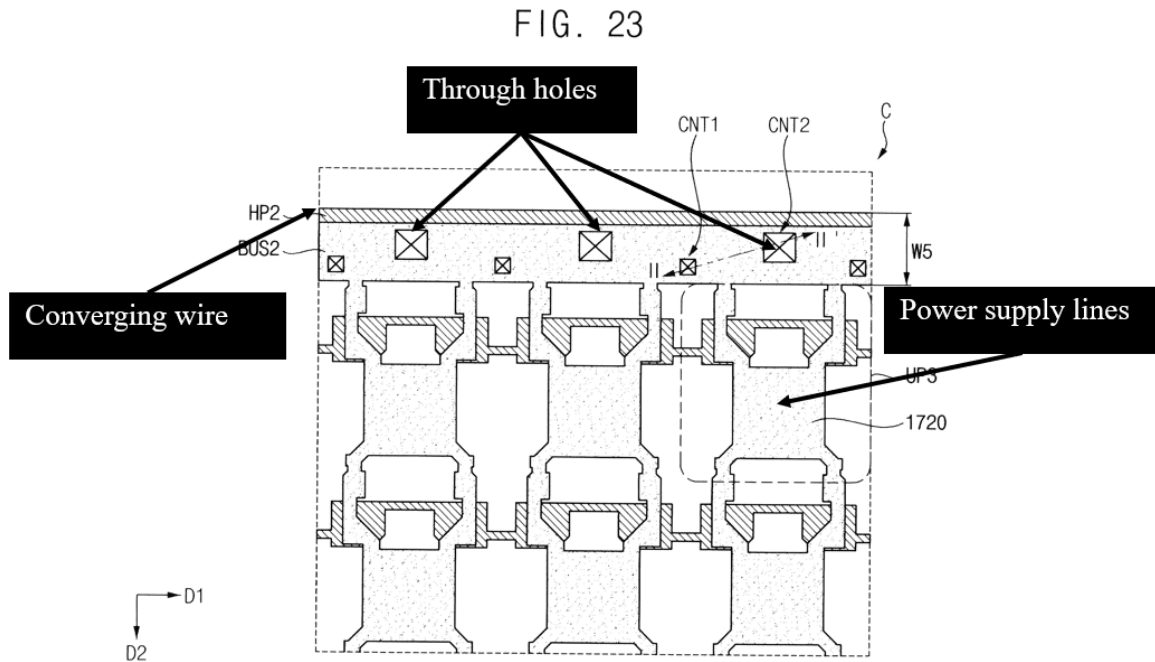
Yi1 teaches the additional limitations found in Claim 8. Ex-1002, ¶¶141–142.

First, Yi1 teaches that the converging wire comprises a second converging wire arranged in the second non-display region. As detailed in Section XII.A.1.c, Yi1's second lower pattern LP2 includes both the first horizontal pattern HP1 and the second horizontal pattern HP2. LP2 is part of the LPL, as it is “disposed in the lower pattern layer LPL together with the first lower pattern LP1.” Ex-1005, 19:6–8. HP1 is disposed at the bottom of the mesh shape, extends in the first direction D1, and is connected to the power voltage bus BUS1. Ex-1005, 20:22–42. HP2 is disposed at the top of the mesh shape and is connected to the power voltage pattern BUS2, which is “disposed in a top side of the non-display area NDA,” while BUS1 is disposed in a bottom side of the non-display area NDA. Ex-1005, 9:58–66. Figure 1' shows the HP1 and HP2 (the first and second converging wires) arranged in the non-display region around the display area:



Accordingly, HP2 is a second converging wire arranged in a second non-display region, on the opposite side of the display area from HP1 and BUS1. Ex-1002, ¶¶143–144.

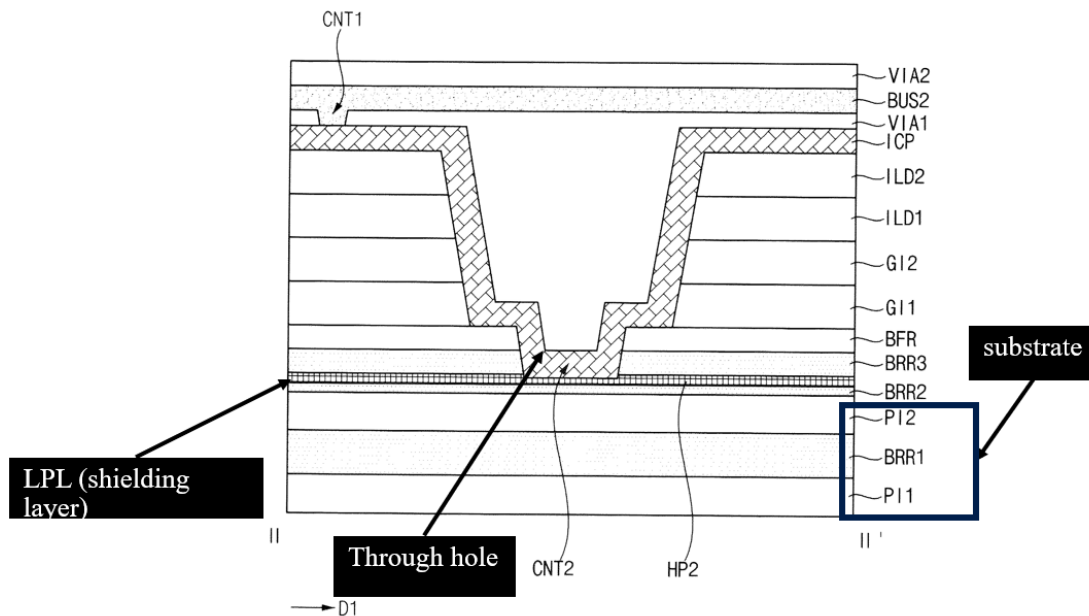
Second, Yi1 teaches that the plurality of power supply lines are electrically connected to the plurality of second connection sections through the plurality of through holes. As shown in Figure 23, HP2 is connected to the power voltage bus BUS2 through a through hole (marked with an X):



Ex-1005, Fig. 23 (annotated).

Figure 24, which is a cross section of the through holes in Figure 23, shows that the power lines (1720 above) are electrically connected to the plurality of second connection sections (*i.e.*, in the shielding layer) through the through holes CNT2, which contact the LPL:

FIG. 24



Id., Fig. 24 (annotated).

4. Claim 17

- a. 17[a]: The display device according to claim 11, wherein the non-display region comprises: a first non-display region and a second non-display region disposed on two sides of the display region, wherein the first non-display region comprises a bending sub-region, and the display panel bends at the bending sub-region; and

Disclosed. *See supra* Section XII.B.2.

- b. 17[b]: the converging wire comprises a first converging wire arranged in the first non-display region, and the plurality of power supply lines are electrically connected to the plurality of first connection sections at least through the plurality of through holes.

Disclosed. *See supra* Section XII.B.2.

5. **Claim 18: The display device according to claim 17, wherein the converging wire comprises a second converging wire arranged in the second non-display region, and the plurality of power supply lines are electrically connected to the plurality of second connection sections through the plurality of through holes.**

Disclosed. *See supra* Section XII.B.3.

C. Ground 3: Claims 6 and 16 Are Rendered Obvious by the Combination of Yi1 with Zhang

Claim 6 depends from Claim 5, which depends from Claims 4 and 1, each limitation of which Yi1 discloses as addressed above. *See supra* Sections XII.A.1, XII.A.4, XII.A.5. Claims 6 and 16 would have further been obvious over Yi1 in view of Zhang (Ex-1007), with Yi1 serving as the primary reference and Zhang supplying the recited arc-shaped geometry. Ex-1002, ¶¶147–148.

1. Motivation to combine

A POSITA would have been motivated to combine Yi1 with Zhang. Ex-1002, ¶¶147–148. Yi1 and Zhang are both directed to integrated circuit structures featuring metal interconnect patterns with alternating wide and narrow portions connected to through holes/vias. *See supra* Section XI. Zhang teaches that metal line structures having wide portions with arc-shaped (rounded) peripheries and linear narrow connecting portions are advantageous for accommodating large vias while maintaining a constant spacing between adjacent lines. Specifically, Zhang's bicycle chain structures (Fig. 1B) feature wide portions 104 with rounded

peripheries (via landing pads 106) spaced between linear narrow portions 105. Ex-1007, 5:7–26, Fig. 1B; Ex-1002, ¶147. Both references also use silicon-based materials, and a POSITA would have been familiar with silicon as a common material in via and through-hole technology. Zhang describes via fabrication processes using silicon dioxide, polysilicon, low-temperature silicon dioxide, silicon nitride, and silicon transistor substrates, while Yi1 relies on silicon semiconductors and silicon oxide, silicon nitride, and silicon oxy-nitride in its active, barrier, and insulating layers. Ex-1007, 6:40–50, 7:15–25, 9:40–55; Ex-1005, 12:55–65, 14:1–20; Ex-1002, ¶147.

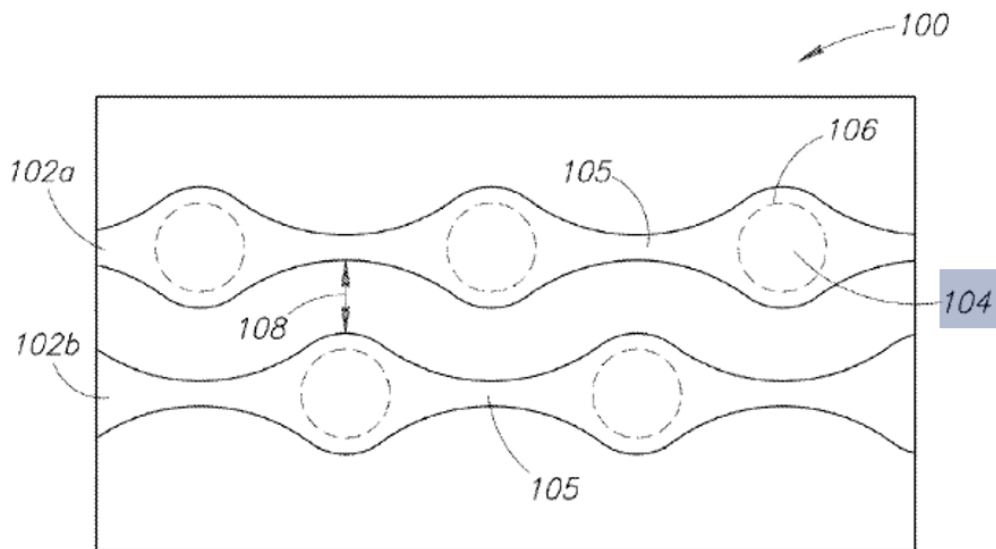


FIG.1B

Ex-1007, Fig. 1B (annotated).

Figure 7B illustrates the final wavy metal line structures with the wide portions having rounded/arc-shaped peripheries resulting from the intentional rounding of optical lithography (OPC), while the narrow portions remain linearly shaped (dark blue). Ex-1007, 5:44–57, 6:9–30, Fig. 7B. As Dr. Lebby explains, arc-shaped geometries at via landing pads are a standard layout practice in integrated circuit design. Sharp corners in metal conductors concentrate current flow, leading to electromigration and current crowding, especially in circuits carrying heavy current, ESD, or RF signals. Ex-1002, ¶148 Eliminating sharp corners is a common semiconductor-layout practice, and rounded features improve lithographic patterning margins because corners of rectangular mask features naturally transfer to the photoresist and metal trench as rounded features during optical lithography. Eliminating sharp metallic tips also reduces ESD-susceptible features, which is precisely the problem the '429 Patent purports to solve. Ex-1002, ¶¶148–149.

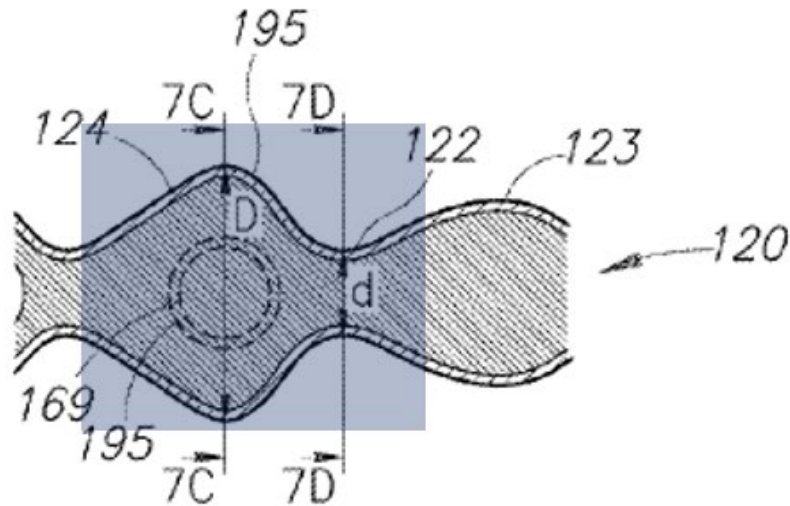


FIG. 7B

Ex-1007, Fig. 7B (annotated).

A POSITA would further be motivated to apply Zhang’s OPC process, which intentionally rounded corners, to YI1’s converging wire to achieve the benefits that Zhang describes. For example, Zhang explains that “for multiple reasons, it is advantageous for via footprints to remain large, while metal lines continue to shrink with each technology generation.” Ex-1007, 1:37–40.

Additionally, “[t]he method disclosed takes advantage of the shortcomings of optical lithography to achieve the desired wavy line pattern by anticipating

diffraction errors that will occur during exposure of the rectangular features. Such a technique is generally known in the art as optical proximity correction (OPC).” Ex-1007, 2:12–17. Moreover “severing the dependence of via dimensions on metal linewidths has important advantages and implications for future generations of integrated circuit development.” Ex-1007, 8:28–31. One advantage include that “metal line trenches are lined with a sacrificial layer that completely fills the narrow spaces while under-filling the wide spaces that correspond to via locations. The sacrificial layer thus acts as a via hard mask, allowing etching of the underlying thick dielectric block, while protecting narrow features of the trenches that correspond to the metal line interconnects. The resulting vias have an aspect ratio that is relatively easy to fill, while the larger footprint provides low via resistance.” Ex-1007, 1:63–2:5. A POSITA would have been motivated to implement Zhang’s OPC teachings with Yi1 to achieve these and other benefits. Ex-1002, ¶149.

A POSITA implementing the converging-wire connection sections of Yi1 would have found it obvious to employ arc-shaped (rounded) peripheries for the wider first connection sections (analogous to Zhang’s via landing pads) while keeping the second connection sections linear (analogous to Zhang’s narrow portions), as Zhang expressly teaches benefits of this geometry for accommodating large vias in metal interconnect structures. The combination yields first connection

sections with arc-shaped peripheries and linear second connection sections, with the maximum width of the first connection sections greater than the width of the second connection sections—exactly as recited in Claim 6. The combination would have produced predictable results, and a POSITA would have had a reasonable expectation of success. Ex-1002, ¶¶148–150.

2. Claim 6: The display panel according to claim 5, wherein a periphery of each of the plurality of first sections is arc shaped, the plurality of second sections are linearly shaped, a maximum width of each of the plurality of first sections is greater than the width of each of the plurality of second sections

The combination of Yi1 with Zhang teaches the additional limitations found in Claim 6. Ex-1002, ¶151.

First, the base structure of Claim 6 is supplied by Yi1. As detailed in Sections XII.A.4 and XII.A.5, Yi1 teaches a first horizontal pattern extending in direction D1, providing a linear converging wire with a plurality of first and second connection sections that provide power to the converging wire and connect it to the LPL, the claimed shielding layer. Ex-1005, 20:30–37, Ex-1002, ¶152.

Second, the combination teaches that a periphery of each of the plurality of first sections is arc shaped, the second sections are linearly shaped, and a maximum width of each of the plurality of first sections is greater than the width of each of the plurality of second sections. Zhang’s rounded-geometry teaching,

applied to the first connection sections of Y11 as discussed above, yields first connection sections with arc-shaped (rounded) peripheries—analogueous to Zhang’s wide portions (via landing pads) with rounded peripheries shown in Figure 7B—while the second connection sections remain linearly shaped, analogueous to Zhang’s narrow connecting portions. Ex-1007, 5:7–26, 5:44–57, 6:9–30, 8:11-18, Fig. 7B; Ex-1002, ¶153. Figure 7B of Zhang illustrates this wavy metal line geometry, below:

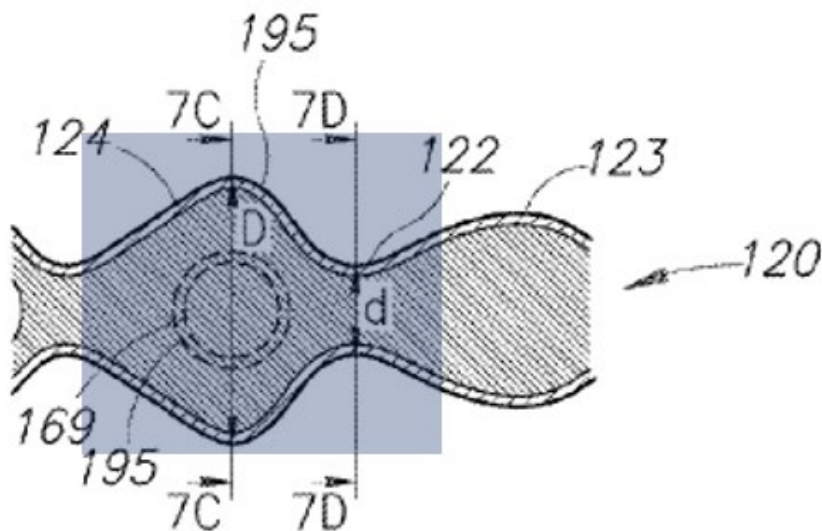
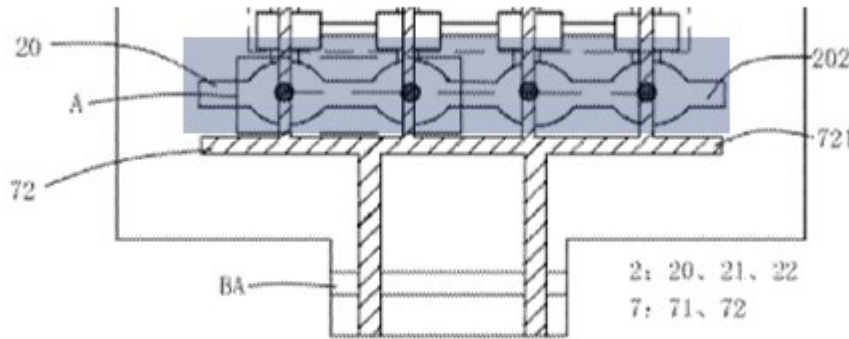


FIG. 7B

This structure is similar to that which is described in the '857 Patent, which is illustrated in Figure 2 (zoomed in, below):



Zhang also explains that through holes are formed through conventional etching techniques known in semiconductor fabrication, including wet chemical etching and reactive-ion etching. Ex-1007, 4:26–33. Conventional etching processes would result in contact holes with a circular shape, which has an arc-shaped profile. This further supports the predictable use of arc-shaped connection sections in the combined structure. Ex-1002, ¶154. Accordingly, Claim 6 would have been obvious over Yi1 in view of Zhang. Ex-1002, ¶¶151–155.

3. **Claim 16: The display device according to claim 15, wherein a periphery of each of the plurality of first sections is arc shaped, the plurality of second sections are linearly shaped, a maximum width of each of the plurality of first sections is greater than the width of each of the plurality of second sections.**

Disclosed. *See supra* Section XII.C.2.

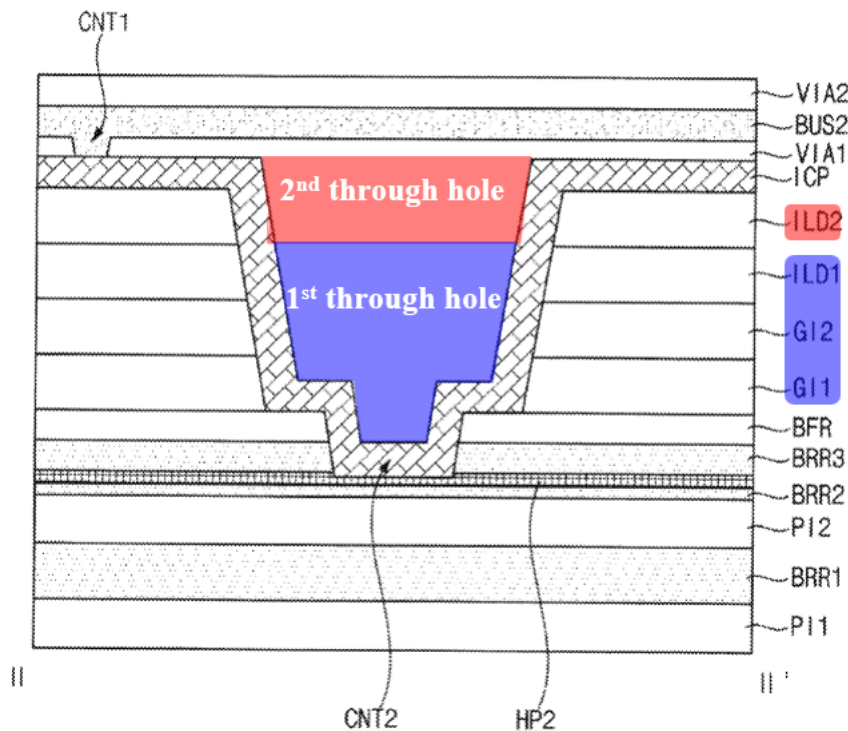
D. Ground 4: Claims 10 and 20 Are Rendered Obvious by the Combination of Yi1, Yi2, and Park

Claim 10 depends from Claim 9, each limitation of which is disclosed by Yi1, as addressed above in Ground 1. *See supra* Section XII.A.6. Claim 20 depends from Claim 19, and recites identical limitations to Claim 10. The combination of Yi1, Yi2, and Park supplies the recited relationship between the nested through holes—that a diameter of each of the plurality of second through holes is greater than a diameter of each of the plurality of first through holes.

A POSITA would have been motivated to combine Yi1, Yi2, and Park. Ex-1002, ¶¶157–160. Yi1, at Figure 24, discloses stacked, communicating contact holes connecting the power supply lines to the shielding layer through multiple insulating layers. Ex-1005, 20:55–21:5. Yi2 teaches that the lower part of the contact hole is narrower than the upper part: the “second contact hole CNT2 may be connected to the first contact hole CNT1,” and “[a] plane area of the second contact hole CNT2 may be smaller than a plane area of the first contact hole CNT1.” Ex-1006, ¶160. Park, in the same OLED display field, expressly teaches

forming an upper via hole larger than a corresponding lower contact hole to prevent patterning defects and improve processing stability and reliability. Ex-1008, 3:16–21. Park further discloses circular contact holes formed by etching. Ex-1008, 4:47–52, 5:33–37, 7:19–25. A POSITA would have applied these teachings when dimensioning the nested through holes of Y11. Dimensioning upper vias to be larger than lower contact holes is a well-known principle in semiconductor and display fabrication. Ex-1002, ¶160. The larger upper via provides alignment margin during photolithography, which is particularly important given registration tolerances in multilayer thin-film patterning. *Id.* In TFT backplane fabrication, multiple conductive and insulating layers are patterned sequentially, and contact holes must penetrate multiple insulating layers to connect different metal layers. Designing the upper via to be larger ensures that, even with registration error, the via overlaps the lower contact hole, preventing patterning defects and open circuits. A POSITA would have had a reasonable expectation of success because the combination involves routine dimensioning of known structures in a well-established multilayer TFT fabrication process.

FIG. 24



Id. Fig. 24 (annotated).

Park, in the same OLED display field, expressly teaches “forming a via hole to be larger than a contact hole in a structure where the via hole is formed corresponding to the contact hole” in order to “prevent a patterning defect on a lower electrode, and improve processing stability and reliability of a device.” Ex-1008, 3:16–21; *see also* Ex-1008, 1:46–50, Abstract. A POSITA would have applied Park’s express teaching when dimensioning the nested through holes of Y11—making the diameter of the upper (second) through hole greater than the diameter of the lower (first) through hole—to obtain precisely the manufacturing-

reliability benefits Park describes. Ex-1002, ¶¶159–160. A POSITA would have had a reasonable expectation of success because the combination involves only routine dimensioning of known structures. *Id.* ¶160.

1. Claim 10

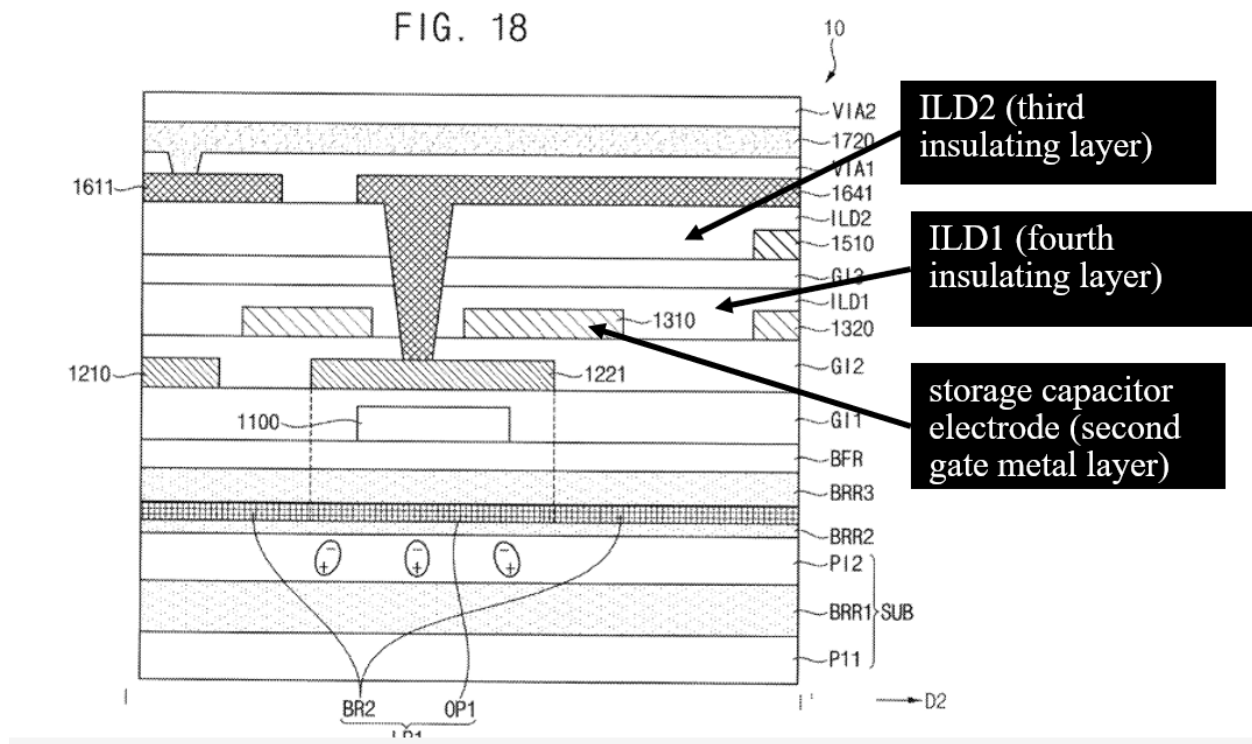
- a. 10[pre]: The display panel according to claim 9, wherein the pixel driving circuit layer further comprises:**

The combination of Yi1, Yi2, and Park teaches Element 10[pre]. Ex-1002, ¶161. Claim 10 depends from Claim 9 and recites limitations that mirror those of Claim 20 (which depends from Claim 19). As detailed in Section XII.A.6, Yi1 teaches the recited pixel driving circuit layer, which further comprises the additional layers recited in Elements 10[a]-10[c], as detailed below. Ex-1002, ¶162.

- b. 10[a]: a fourth insulating layer disposed between the second gate metal layer and the third insulating layer; and**

Yi1 teaches this limitation. Ex-1002, ¶163.

The first inter-insulating layer (ILD1) is disposed between the second conductive pattern (comprising, in part, electrodes at 1310) and ILD2. Figure 18 illustrates the relationship between these layers:



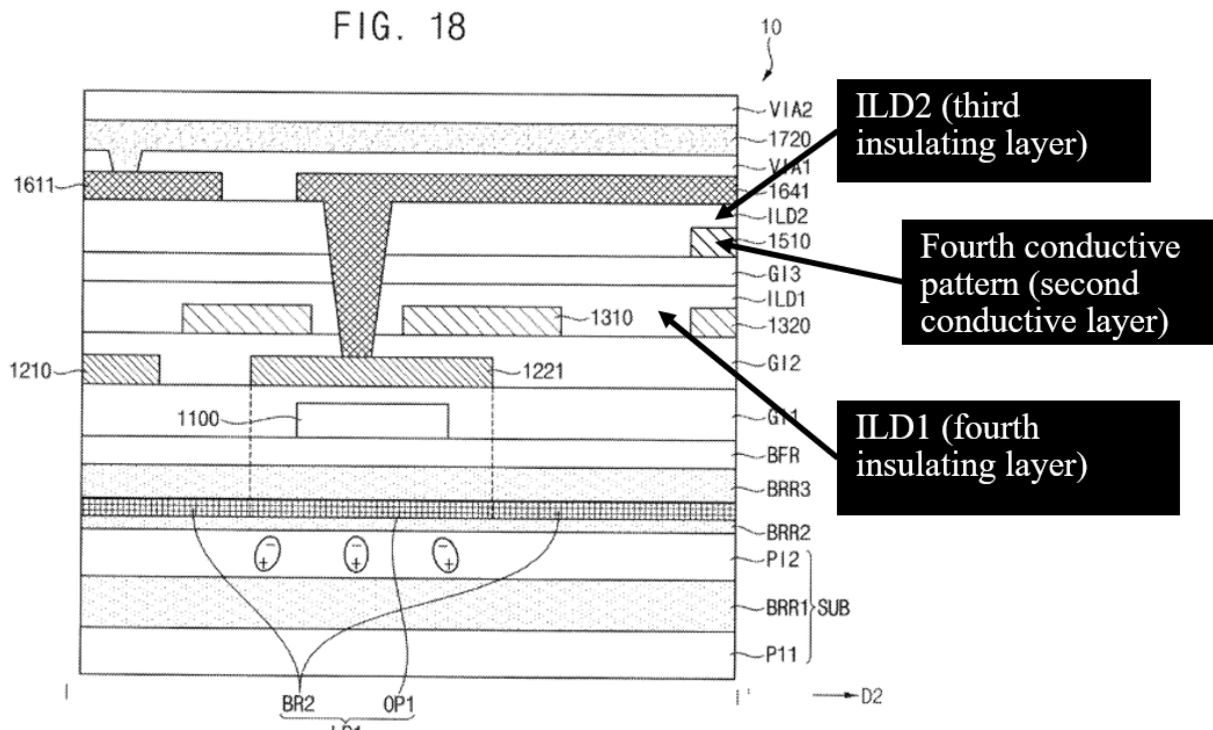
Accordingly, Yi1 teaches this limitation. Ex-1002, ¶164.

c. 10[b]: a second conductive layer disposed between the fourth insulating layer and the third insulating layer;

Yi1 teaches Element 10[b]. Ex-1002, ¶165.

Yi1 teaches a second conductive layer disposed between the fourth insulating layer and the third insulating layer: “the third conductive pattern 1500 may be disposed on the third gate insulating layer GI3. The third conductive pattern 1500 may include a third gate line 1510”. Ex-1005, 15:37–49, 18:3–12. The fourth conductive pattern comprises, in part, a “the third gate line 1510 [which] may be adjacent to the other side of the first gate electrode 1221” Ex-

1005, 18:3–12. As Figure 18 illustrates, the “fourth conductive pattern,” e.g. 1510, is between ILD1 (the fourth insulating layer) and ILD2 (the third insulating layer):



Id. Fig. 18 (annotated).

Accordingly, Y11 teaches this limitation. Ex-1002, ¶¶165–166.

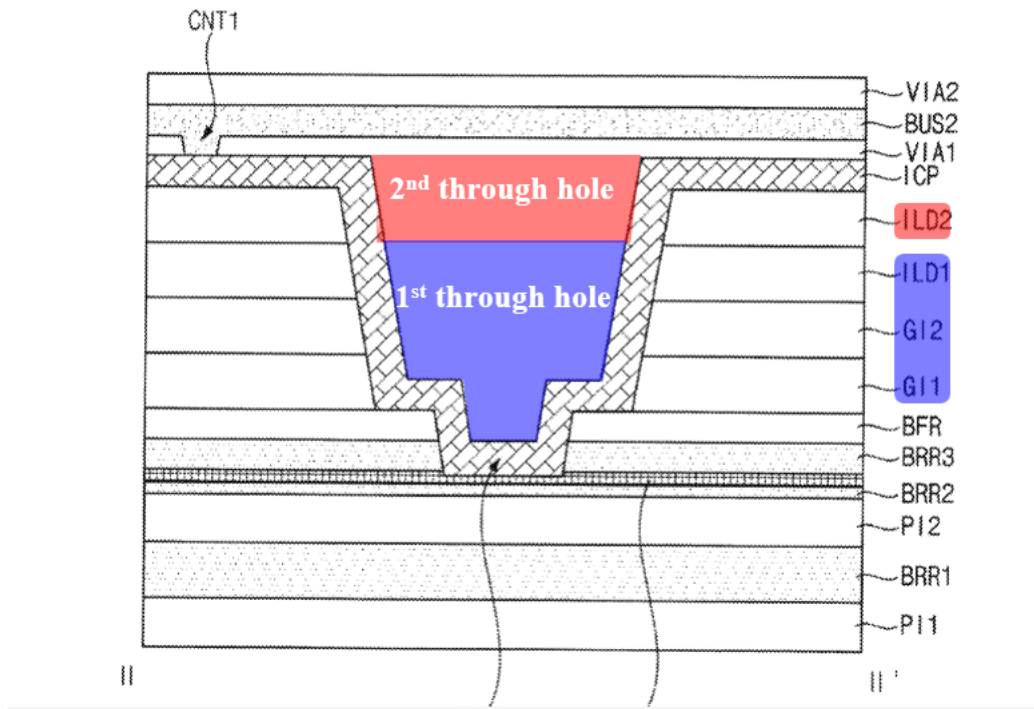
- d. **10[c]: wherein the plurality of through holes comprise a plurality of first through holes and a plurality of second through holes, the plurality of first through holes penetrates through the first insulating layer, the second insulating layer, and the fourth insulating layer, and the plurality of second through holes penetrates through the third insulating layer; wherein the plurality of first through holes are communicated with the plurality of second through holes, and a diameter of each of the plurality of second through holes is greater than a diameter of each of the plurality of first through holes.**

The combination teaches Element 10[c]. Ex-1002, ¶167.

This claim element requires the through holes to comprise two groups of through holes. The first group penetrates three layers: the first, second, and fourth insulating layers. The second group penetrates the third insulating layers. The two groups are communicated together, and the diameter of the second group is greater than the diameter of the first group. Ex-1002, ¶168.

First, Yi1 teaches a plurality of first through holes and a plurality of second through holes that are communicated with each other. The second contact hole CNT2 “may penetrate the third barrier layer BRR3, the buffer layer BFR, the first gate insulating layer GI1, and the second gate insulating layer GI2, the first inter-insulating layer ILD1, the third gate insulating layer GI3, and the second inter-insulating layer ILD2.” Ex-1005, 20:65–21:4. Figure 24 is annotated below to show the two through holes in CNT2:

FIG. 24



Id. Fig. 24 (annotated).

As can be seen above, the second through hole goes through the third insulating layer (ILD2), while the first through hole goes through ILD1, GI2, and GI1. These holes are “communicated with” each other as they are nested, as is consistent with the ’429 Patent’s own disclosures. Figure 1 of the ’429 Patent, for example, shows a “plurality of first through holes” that “are communicated with the plurality of second through holes 92.” Ex-1001, 7:37–39.

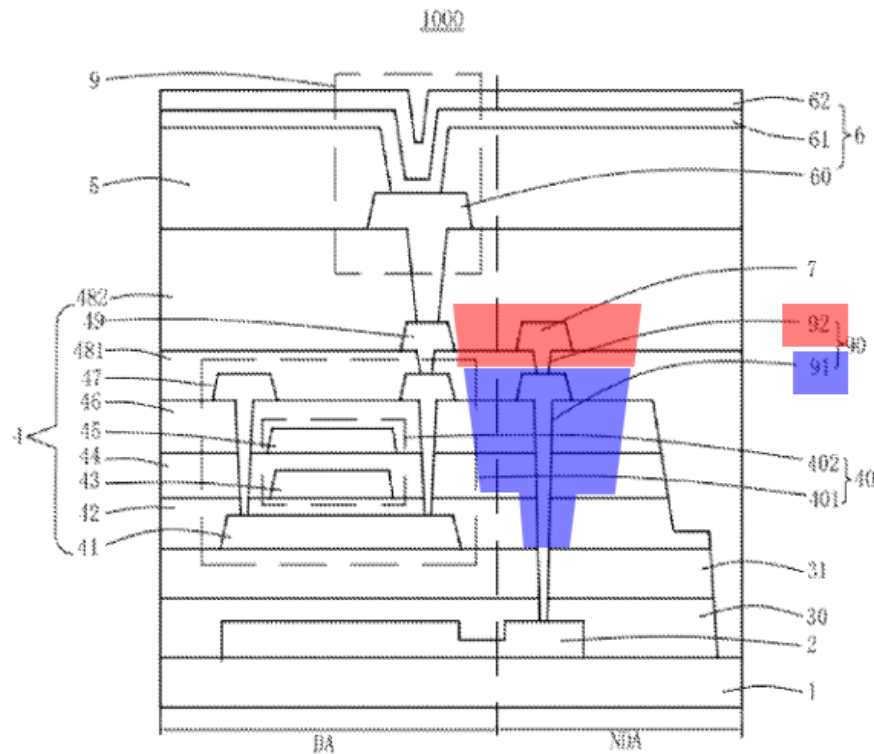


FIG. 1

Id. Fig. 1 (annotated).

Second, the recited diameter relationship—that a diameter of each of the plurality of second through holes is greater than a diameter of each of the plurality of first through holes—is taught by Park. Park teaches forming the upper via hole 267 to be larger than the underlying contact hole 235 in a structure where the via hole is formed corresponding to the contact hole, to prevent patterning defects and improve processing stability and reliability. Ex-1008, 3:16–21, 5:55-67. Figures 4A and 4B of Park show this relationship:

FIG. 4A

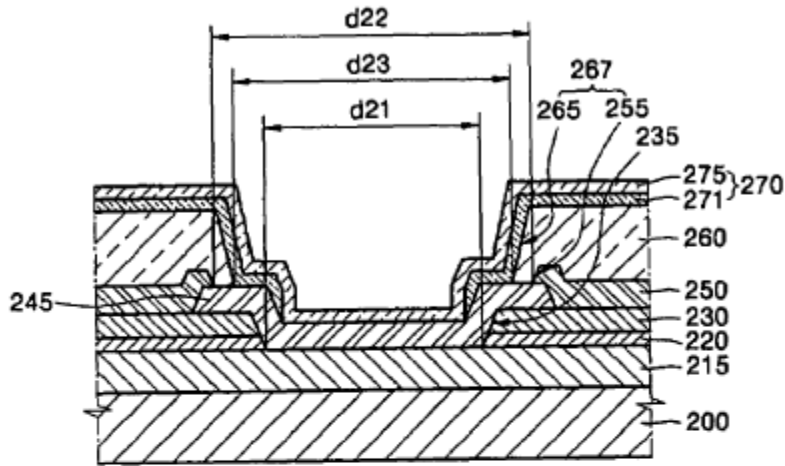
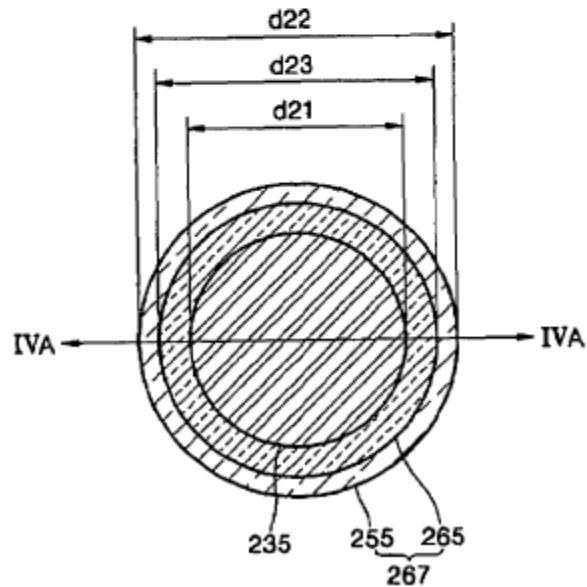


FIG. 4B



Yi2 likewise teaches that the lower part of the contact hole is narrower than the upper part. Ex-1006, ¶160. As discussed above, a POSITA would have

applied Park's teaching when dimensioning the nested through holes of Yi1. Ex-1002, ¶¶171–174.

Accordingly, Claim 10 would have been obvious over Yi1 in view of Yi2 and Park. Ex-1002, ¶175.

2. Claim 20

- a. 20[pre]: The display device according to claim 19, wherein the pixel driving circuit layer further comprises:**

Disclosed. *See supra* Section XII.D.1.a.

- b. 20[a]: a fourth insulating layer disposed between the second gate metal layer and the third insulating layer; and**

Disclosed. *See supra* Section XII.D.1.b.

- c. 20[b]: a second conductive layer disposed between the fourth insulating layer and the third insulating layer;**

Disclosed. *See supra* Section XII.D.1.c.

- d. 20[c]: wherein the plurality of through holes comprise a plurality of first through holes and a plurality of second through holes, the plurality of first through holes penetrates through the first insulating layer, the second insulating layer, and the fourth insulating layer, and the plurality of second through holes penetrates through the third insulating layer; wherein the plurality of first through holes are communicated with the plurality of second through holes, and a diameter of each of the plurality of second through holes is greater than a diameter of each of the plurality of first through holes.**

Disclosed. *See supra* Section XII.D.1.d.

E. CONCLUSION

Petitioner requests institution of IPR for Claims 1–20 of the '429 Patent based on each of the grounds in this Petition.

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner certifies that this petition includes 12,085 words, as measured by Microsoft Word, exclusive of the table of contents, mandatory notices under § 42.8, certificates of service, word count, and exhibits.

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on September 17, 2026, by filing this document through the Patent Trial and Appeal Board P-TACTS System, as well as delivering a copy via express mail upon the following attorneys of record for the Patent Owner:

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