

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD.,
Petitioner

v.

WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY
TECHNOLOGY CO., LTD.
Patent Owner.

Case No. IPR2026-00487
U.S. Patent No. 12,133,429

**DECLARATION OF DR. MICHAEL LEBBY IN SUPPORT OF PETITION
FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 12,133,429**

TABLE OF CONTENTS

I.	INTRODUCTION	6
II.	BACKGROUND AND QUALIFICATIONS	7
A.	Background	7
B.	Compensation.....	18
III.	INFORMATION CONSIDERED.....	19
IV.	RELEVANT LEGAL STANDARDS	19
A.	Claim Interpretation	19
B.	Person of Ordinary Skill in the Art	19
C.	Obviousness.....	20
D.	Secondary Considerations of Non-Obviousness.....	22
V.	LEVEL OF ORDINARY SKILL IN THE ART.....	23
VI.	SUMMARY OF MY OPINIONS	24
VII.	TECHNOLOGY BACKGROUND.....	24
VIII.	THE CHALLENGED PATENT	28
IX.	PROSECUTION HISTORY OF THE '429 PATENT.....	32
X.	PRIORITY DATE	32
XI.	CLAIM CONSTRUCTION	33
XII.	OVERVIEW OF THE APPLIED PRIOR ART REFERENCES	34
A.	Yi1 (Ex-1005).....	34
B.	B. Yi2 (Ex-1006).....	38
C.	Zhang (Ex-1007)	39
D.	Park (Ex-1008)	41
XIII.	DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS.....	44
A.	Ground 1: Claims 1–5, 9, and 11–15 Are Rendered Obvious by Yi1	44
1.	Independent Claim 1	44

Inter Partes Review – Declaration of Dr. Michael Lebby

2.	Claim 2: The display panel according to claim 1, wherein the converging wire between the two adjacent through holes is linear in arrangement.	62
3.	Claim 3: The display panel according to claim 2, wherein the converging wire is linear in arrangement and the plurality of through holes overlappingly disposed on the converging wire are linear in arrangement.	65
4.	Claim 4: The display panel according to claim 1, wherein the converging wire comprises a first converging wire, and the first converging wire comprises a plurality of first connection sections and a plurality of second connection sections; wherein each of the plurality of second connection sections is connected between a middle portion of two adjacent first plurality of connection sections, a width of each of the plurality of first connection sections is greater than a width of each of the plurality of second connection sections, and the plurality of power supply lines are electrically connected to the plurality of first connection sections through the plurality of through holes.	66
5.	Claim 5: The display panel according to claim 4, wherein the plurality of pixel driving circuits are arranged in an array in a first direction and a second direction, each of the plurality of first connection sections is electrically connected to the plurality of shielding blocks corresponding to a column of the plurality of pixel driving circuits arranged along a first direction	70
6.	Claim 9	74
7.	Claim 11: A display device comprising the display panel as claimed in claim 1, wherein the display panel is an organic light-emitting diode (OLED) panel.....	85
8.	Claims 12–15	85
B.	Ground 2: Claims 7–8 and 17–18 Are Rendered Obvious by Yi1 in View of Yi2	86
1.	Motivation to Combine Yi1 and Yi2	86
2.	Claim 7	87

Inter Partes Review – Declaration of Dr. Michael Lebby

3.	Claim 8: The display panel according to claim 7, wherein the converging wire comprises a second converging wire arranged in the second non-display region, and the plurality of power supply lines are electrically connected to the plurality of second connection sections through the plurality of through holes.....	89
4.	Claims 17–18	93
C.	Ground 3: Claims 6 and 16 Are Rendered Obvious by Yi1 in View of Zhang.....	93
1.	Motivation to Combine Yi1 and Zhang.....	93
2.	Claim 6: The display panel according to claim 5, wherein a periphery of each of the plurality of first sections is arc shaped[BH18.1][BH18.2], the plurality of second sections are linearly shaped, a maximum width of each of the plurality of first sections is greater than the width of each of the plurality of second sections	97
3.	Claim 16: The display device according to claim 15, wherein a periphery of each of the plurality of first sections is arc shaped, the plurality of second sections are linearly shaped, a maximum width of each of the plurality of first sections is greater than the width of each of the plurality of second sections.....	100
XIV.	D. GROUND 4: CLAIMS 10 AND 20 ARE RENDERED OBVIOUS BY YI1 IN VIEW OF YI2 AND PARK.....	100
1.	Motivation to Combine Yi1, Yi2, and Park.....	100
2.	Claim 10.....	103
3.	Claim 20.....	110
XVI.	CONCLUSION.....	111

LIST OF EXHIBITS

Ex. No.	Description
Ex-1001	U.S. Patent No. 12,133,429 ("the '429 Patent")
Ex-1002	Declaration of Dr. Michael Lebby
Ex-1003	Curriculum Vitae of Dr. Michael Lebby
Ex-1004	Prosecution History of U.S. Patent No. 12,133,429
Ex-1005	U.S. Patent No. 11,963,404 to Yi et al. ("Yi1")
Ex-1006	U.S. Patent Application Publication No. 2022/0199741 to Yi et al. ("Yi2")
Ex-1007	U.S. Patent No. 9,658,523 to Zhang et al. ("Zhang")
Ex-1008	U.S. Patent No. 7,335,912 to Park et al. ("Park")
Ex-1009	Takatoshi Tsujimura, <i>OLED Display Fundamentals and Applications</i> (2d ed., John Wiley & Sons, Inc. 2017).
Ex-1010	<i>Organic Light-Emitting Diodes (OLEDs): Materials, Devices and Applications</i> (Alastair Buckley ed., Woodhead Publishing Ltd. 2013).
Ex-1011	<i>Flexible Flat Panel Displays</i> (Gregory P. Crawford ed., John Wiley & Sons, Ltd. 2005).
Ex-1012	Stanley Wolf, <i>Silicon Processing for the VLSI Era, Volume 4: Deep-Submicron Process Technology</i> (Lattice Press 2002).
Ex-1013	Claim mapping table for the '429 Patent

I. INTRODUCTION

I, Michael Lebbby, declare as follows:

1. My name is Michael Lebbby, Ph.D. and I have been retained as an expert witness to prepare this declaration on behalf of Samsung Display Co., Ltd. (“Petitioner”) in connection with a petition for *inter partes* review (“IPR”) of U.S. Patent No. 12,133,429 (the “’429 Patent”). I have been informed that the petition is being submitted to the United States Patent and Trademark Office’s (“USPTO”) Patent Trial and Appeal Board (the “Board”) by the Petitioner.
2. Specifically, I have been retained as a technical expert by the Petitioner to study and provide my opinions on the technology claimed in, and the patentability or unpatentability of Claims 1–20 of the ’429 Patent (the “Challenged Claims”). For purposes of this declaration, I was not asked to provide any opinions that are not expressed herein.
3. I may offer additional opinions based on further review of materials in this case, including opinions and/or testimony of other expert witnesses. For my efforts in connection with this matter, I have been compensated at my usual and customary rate for this type of consulting activity. My compensation is in no way contingent on the substance of my opinions or on the outcome of this or any other proceedings concerning the ’429 Patent.

II. BACKGROUND AND QUALIFICATIONS

A. Background

4. I am a technologist and internationally-recognized business leader with over 30 years of experience working in integrated photonics and optoelectronics design and manufacturing. As described in this Section, and further detailed in my curriculum vitae (Exhibit 1003), over the course of my over 40-year career in electronics and optoelectronics, I have worked in nearly every aspect of the electronic and optoelectronics business, ranging from epitaxial wafer growth (compound semiconductors), electrical and optoelectronic device and circuit design, using modeling and simulation, electrical and optoelectronic device and component fabrication, testing, and qualification, to the implementation of devices into packages and panels, both hermetic and non-hermetic, as well as analysis of package/panel materials such as plastics (including plastic housings such as resin-packaged lead frame housings), optical plastics, metallic-based packages, semiconductor-based packages, and ceramic-based packages. I have also designed device and display packages (through-pin, surface mount, flip-chip, and various combinations thereof) for printed circuit board mounting. Many of the designed packages were implemented into electronic and optoelectronic modules/panels and sub-system/luminaire applications that included various electronics designs. The modules/panels have been at least fiber-optic-, display-, lighting-, imaging-, sensing-

, power-, and RF-based. Throughout the course of my educational and professional activities, I have worked extensively with devices like the light-emitting diode (LED) devices and device packaging described in the '429 Patent.

5. I have also worked in commercially based industrial research-and-development laboratories to bring new electronic, optoelectronic-, display-, and photonic-based technologies from the research proof-of-concept phase through prototyping and qualified manufacturing for volume release. This has included both transfer as well as injection molding techniques for packaging. I have been both an entrepreneur (e.g., Ignis Optics Inc, One Chip Photonics, Lightwave Logic Inc.), as well as an intrapreneur (e.g., Motorola, Intel, TE Connectivity (previously Tyco Electronics), AT&T Bell Labs), creating innovative new programs, both as venture-backed start-ups as well as corporate-funded divisions. I have built these entities to develop electronic, optoelectronics, and photonics technology from the laboratory and fabrication clean room to production factories.

6. I received a Bachelor of Engineering degree in Electrical and Electronic Engineering in 1984, a Master of Business Administration in 1985, and a Ph.D. in Semiconductor Physics in 1987, all from the University of Bradford in the United Kingdom. My Ph.D. thesis involved the design and fabrication of both optoelectronic and electronic compound semiconductor devices (such as GaAs, InP, etc.), and their associated characterization. In 2004, I was awarded a Doctor of

Engineering degree (a higher doctorate degree) with a focus in optoelectronics from the University of Bradford for my technical contributions to the field.

7. My career started in the late 1970s at the Ministry of Defense in the UK where I spent time at their R&D facility in Malvern (RSRE – Royal Signals and Radar Establishment). I worked on electronic and optoelectronic semiconductor device design, fabrication, and characterization, and especially materials using III-V compound semiconductors such as GaAs and InP. These devices included electronic transistors, optical waveguides, and optoelectronic device operation. My research work in semiconductor device design then took me to AT&T Bell Laboratories in 1985, where I pursued research in novel opto-device designs using III-V semiconductor material systems that included FETs, bipolar transistors, optical waveguides, optics, LEDs, laser diodes, and photodetectors. The devices researched became, in part, the subject of my Ph.D. thesis that was granted in 1987.

8. I moved to Motorola in 1989 to further develop my electronic, optoelectronic, semiconductor and display engineering and development skills, and I became a Research and Development Manager in Motorola, until I left the company in 1998. During my time at Motorola, I worked on many photonic, electronic, display and optical technology projects that included optical lenses, display, imaging, camera, fiber-optic optical interconnects, electronic circuits (both analog and digital), displays, LEDs, OLEDs, and laser devices, as well as the packaging and reliability

Inter Partes Review – Declaration of Dr. Michael Lebby

of mobile product prototypes. At that time, I was particularly interested in miniature displays/panels and miniature optics using a number of technologies such as LEDs, lasers, LCDs, lenses, and organic LEDs which were aimed towards (at the time) pagers, mobile phones, micro-imagers/displays, holograms, and advanced prototypes of futuristic communications hardware. I was also particularly interested in miniature color displays in which LEDs/OLEDs could be utilized, and the associated drive and processing electronics for them. One interesting patent I was a co-inventor on is called an Electronic Book which was filed in 1994 (U.S. Patent Number 5,534,888). This invention relates, in general, to optical displays and, more particularly, to optical displays in electronic books and was an early patent in the field of electronic books.

9. In aiming for miniature full color displays and associated optics, in the early 1990s, there was only red wavelength Phosphide (GaAsP and/or InGaAlP) and AlGaAs based LED technology that was advanced in technology and performance. Green wavelength Gallium Phosphide based LEDs had low emission output, and blue wavelength emission LEDs were only available using pure Silicon Carbide on Silicon Carbide substrate wafers, with very low emission output. I worked closely with Motorola's mobile divisions on new and novel display prototypes for mobile phones, etc., and optics to research and develop how best to innovate with full color red, green, and blue displays and associated electronics. A number of alternative

technologies were evaluated, such as LCD (Liquid Crystal Displays), OLED (organic LEDs), and Gallium Nitride and Indium Gallium Nitride materials grown onto Sapphire. I also explored the electronic circuits that were needed to drive, operate, and signal these types of optoelectronic displays.

10. During my time at Motorola as a Research and Development Manager, I designed optical and electrical packages/panels for these displays and devices, which included standard TO-cans, over-molded plastic DIL solutions, and ceramic-based and semiconductor-based technology.

11. The compound semiconductors used in the early 1990s at Motorola corporate research, for which I was a Research and Development Manager, included the Group III-V materials system, Group IV material system, Group VI material system, and Group III-N material system. A number of these materials included: GaAs, InP, GaN, GaP, InGaAlP, and silicon, amongst other materials, all of which were intended to be designed into various light emitting sources, detectors, and electronics in their associated optical package platforms that included optics and lens design. The research work at Motorola also included work on displays and, in particular, miniature displays and optics for pagers, clam-shell phones, and head-mounted displays that included mounting onto eyeglasses (similar in concept to Google glass™). The types of displays ranged from large arrays of visible LEDs (i.e., 10,000 LEDs on a chip) that required custom LED packaging to tiny color LCDs, where

Inter Partes Review – Declaration of Dr. Michael Lebby

work was conducted into approaches to efficiently optically package the displays as well as OLEDs, even though the technology was not mature. At the time, I explored less corrosive metallization for OLED displays as well as approaches in the fabrication processing to improve brightness and lifetime of OLED materials. On-board integrated LED driver electronic circuits were implemented in some of the prototypes. Some of the research work at Motorola utilized phosphor technology, especially for display projects that were based on field emission (i.e., the field emission display (FED)), as well as arrays of visible LED/OLED displays and optics where a full color gamut was required by both internal and external customers. The phosphor technology performed down-conversion of light energy.

12. I also initiated Motorola's work in optical interconnect (Optobus™) technology, that incorporated both transfer and injection molded optical parts. This project involved the research and development of a multi-channel electronic IC chip for parallel optical interconnect.

13. I was one of Motorola's most prolific inventors, having over 150 issued utility patents as an inventor or a co-inventor by the late 1990s. Many of the photonics, electronics, and optical/display prototypes with which I was involved were subject to reliability and stress testing that included humidity, temperature, optical, mechanical, and electrical evaluation. These consumer products all were driven

Inter Partes Review – Declaration of Dr. Michael Lebby

using standard electronic ICs and electronic signaling where I had a role in design and simulation of these circuits.

14. I filed my first GaN patent, which taught techniques using GaN and InGaN LEDs, in 1996, shortly after the invention of high performance GaN/InGaN blue LEDs by Nichia in the early 1990s. My work at Motorola addressed, in part, the big issue at the time in the mid-1990s: full color display and display electronics composed of red, green and blue LEDs that could be utilized in mobile products as well as other applications. As part of this work, I was engaged in how to optically package these technologies that allowed for electrical, optical, and thermal high performance. Examples of patents on which I am a co-inventor, with respect to high heat conductivity surface emitting optical devices, include, for example, U.S. Patent No. 5,538,919, as well as U.S. Patent No. 5,818,404, U.S. Patent No. 5,739,800, and U.S. Patent No. 5,838,703, which three patents address LED packaging solutions.

15. Another of my inventions was directed to a new semiconductor laser that had the potential to be manufactured in high volume. This device was called a VCSEL (vertical cavity surface emitting laser), and the invention was to optimize the performance using an oxide process, and is now the basis for the highest volume semiconductor laser today (with its recent implementation as a structured light sensor in facial recognition systems utilized in modern day smart mobile phones). The VCSEL is a surface emitting diode laser and operates in a similar fashion to

Inter Partes Review – Declaration of Dr. Michael Lebby

most LED chips today. Some of the goals of the research work at Motorola were to be able to optically package VCSEL laser diodes and their associated optical lenses in a similar approach to LEDs as well as drive them using novel electronic circuits. Laser diodes require thermal issues to be addressed very carefully, as they develop significant levels of heat during operation. The optical package designs at the time (including for lasers and LED packages) took into account optical lensing, thermal heat sinking and thermal paths to take the heat away from the source. My additional patents, including during my time at Motorola, are listed in my curriculum vitae (Exhibit 1003).

16. Between 1998 and 1999, I worked as the Director of Technology/ BD (Fiber Optics) for Tyco Electronics (previously AMP). I joined Tyco Electronics as a member of the Global Optoelectronics Division's management team. I was responsible for growing the optoelectronics and optical business through external interactions that included mergers, acquisitions, strategic alliances, and technical strategic planning. Much of that work was laser-and LED-based, with associated optics, and included designing and characterizing laser- and LED-based optical packages and modules for customer qualification specifications.

17. In 1999, I left Tyco and started employment at Intel. At Intel, I was involved heavily in photonic technology, especially technology that supported silicon photonic device platforms. As a culmination of this work, I was one of Intel's

Inter Partes Review – Declaration of Dr. Michael Lebby

founders of its silicon photonics division in the year 2000, and worked to set up a fabrication facility in South San Jose. The work involved integrating silicon FET electronics with optoelectronics and optics onto the same silicon semiconductor wafer. I was also part of Intel Capital's optical investment team, and participated in over 30 photonics investments into photonics, optics, and optoelectronics. Focus included optical devices, packaging and modules. Technologies investigated included lasers, LEDs, optics, and optical displays.

18. At the end of 2000, I left Intel and raised venture capital funding for a company called Ignis Optics Inc. The main goal of the company was to design and manufacture, in high volume, very high-performance fiber optic transceiver modules, and associated optics with data rates up to OC-192, or approximately 10 Gbps. The fiber optic transceiver modules have the capability of transmitting and receiving optical signals that are controlled using programmable electronics and packaged optoelectronics chips, such as laser diodes, optical lenses, and photodetectors.

19. In 2005, I took up employment for a trade association, based in Washington, D.C., called IEEE Optoelectronics Industry Development Association (OIDA). As head of this trade association, and with photonics and optics manufacturers that included fiber optics, display, cameras, sensing, defense, aerospace, LED lighting, OLED displays (including flexible), and automotive vendors as members, I was

Inter Partes Review – Declaration of Dr. Michael Lebby

responsible, in part, for industry-based technology roadmaps; and I implemented common industry roadmap methodologies with common features such as “Red Brick Walls” and transferred them into optoelectronics roadmaps for the industry in which displays as well as LEDs, OLEDs, fiber-optics, optics, fiber, cameras, optical sensors, projection techniques, and their associated packaging, were featured. OIDA roadmaps featured purple brick walls, to show differentiation from the semiconductor industry.

20. In 2010, I became the General Manager and CTO of Translucent, Inc., a high-tech start-up company which developed and manufactured silicon and rare earth oxide-based epitaxial semiconductor wafers. One of the key drivers at Translucent was to develop a new and novel platform for the growth of GaN and InGaN onto silicon for low-cost LED, RF FET, and power FET manufacturing on larger format substrate wafers (e.g., 200mm), in order to achieve economies of scale and lower chip costs. Translucent pioneered the deposition of single crystal rare earth oxides such as Erbium Oxide (ErOx), Gadolinium Oxide (GdOx), Neodymium Oxide (NdOx), etc., that, when grown, single crystal layers of GaN/InGaN/AlN could be grown on top of them. This allows a lattice-matched, and monolithic-based, wafer template to be manufactured for both FET and LED fabrication. While at Translucent, I researched various epitaxial semiconductor layer structures that utilized rare earth oxide technology in order to improve the performance of FETs

Inter Partes Review – Declaration of Dr. Michael Lebby

and LEDs. Other material growth work at Translucent focused on the growth of Silicon Germanium (SiGe) compounds with rare earth oxides, and various crystal orientation wafer substrates. I patented a number of electronic FET device designs using rare earth oxides while employed at Translucent.

21.

22. I am currently serving as the Chief Executive Officer and Chief Technology Officer of Oculi, LLC. Oculi, LLC is my consulting company through which I engage in my expert witness work. I also presently hold the position of Chief Executive Officer of Lightwave Logic Inc. where I also serve as a Director on the Board of Directors. Lightwave Logic is a company that is developing optical polymer modulators for the fiber optic communications industry.

23. Throughout my career, I have also had an active role in a number of technical professional organizations, including, among others, IEEE Components, Packaging, and Manufacturing Technology (CPMT), IEEE Electronic Components and Technology Conferences (ECTC); IEEE TC-10 (Technical Committee on Optoelectronics), and IEEE Optoelectronics Industry Development Association (OIDA). Through these organizations, I have consistently been a part of committees, events, and workshops relating to semiconductor, optoelectronics, electronics, and packaging technology. I am currently at the grade of Fellow of the IEEE, Optica and National Academy of Inventors (NAI).

24. I also serve as a Technical Expert/Consultant for the European Commission.

In my work at the European Commission, I review and advise on general electronics, semiconductors, photonics, optoelectronics, imaging, sensing, display (LCD, LED, OLED, flexible displays etc.), and related ICT (Information and communications technology) technology.

25. My work has also led to over 225 USPTO utility patents in semiconductors, electronics, optics, displays, and optoelectronics, including a number of patents relating to display technology. I am the author of more than 60 publications and over 300 media events/talks etc.

B. Compensation

26. I am being compensated for the services provided in this matter at \$550 per hour. My compensation is not conditioned on the conclusions I reach as a result of my analysis or on the outcome of this matter, and in no way affects the substance of my statements in this declaration.

27. I do not have any financial interest in the Petitioner or any of its subsidiaries. I also do not have any financial interest in the '429 Patent, and I have not had any contact with the named inventor of the '429 Patent: Xing Wu.

III. INFORMATION CONSIDERED

28. In forming my opinions, I read and considered the '429 Patent and its prosecution history, the exhibits listed in the Exhibit List filed with the IPR of the '429 Patent, as well as any other materials referenced herein.

IV. RELEVANT LEGAL STANDARDS

29. I am not an attorney and offer no legal opinions. For the purposes of my Declaration, I have been informed about certain aspects of the law that are relevant to my analysis, as summarized below.

A. Claim Interpretation

30. I have been informed and understand that in an IPR proceeding, claims are to be interpreted according to the Phillips claim construction standard. I understand that under this standard, the meaning of claim terms is considered from the viewpoint of a hypothetical “person of ordinary skill in the art” (“POSITA”) at the time of the alleged invention. I have been informed and understand that claim construction is a matter of law and that the final claim constructions for this proceeding will be determined by the Patent Trial and Appeal Board (“PTAB”).

31. I provide my opinions regarding terms that may require explicit construction to resolve the grounds I present in my Declaration in Section XI.

B. Person of Ordinary Skill in the Art

32. I have been informed and understand that a patent is to be understood from the perspective of a hypothetical POSITA. Such an individual is considered to

Inter Partes Review – Declaration of Dr. Michael Lebby

possess normal skills and knowledge in a particular technical field (as opposed to being a genius). I understand that in considering what the claims of a patent require, what was known prior to that patent, what a prior art reference discloses, and whether an invention is obvious or not, one must use the perspective of such a POSITA.

C. Obviousness

33. I have been informed and understand that a patent claim is obvious under 35 U.S.C. § 103, and therefore invalid, if the claimed subject matter, as a whole, would have been obvious to a POSITA as of the priority date of the patent based on one or more prior art references and/or the knowledge of a POSITA.

34. I understand that an obviousness analysis must consider (1) the scope and content of the prior art, (2) the differences between the claims and the prior art, (3) the level of ordinary skill in the pertinent art, and (4) secondary considerations, if any, of non-obviousness (such as unexpected results, commercial success, long-felt but unmet need, failure of others, copying by others, and skepticism of experts).

35. I understand that a prior art reference may be combined with other references to disclose each element of the invention under 35 U.S.C. § 103. I understand that a reference may also be combined with the knowledge of a POSITA, and that this knowledge may be used to combine multiple references. I further understand that a POSITA is presumed to know the relevant prior art. I understand that the

obviousness analysis may take into account the inferences and creative steps that a POSITA would employ.

36. In determining whether a prior art reference would have been combined with other prior art or other information known to a POSITA, I understand that the following principles may be considered:

- whether the references to be combined involve non-analogous art;
- whether the references to be combined are in different fields of endeavor than the alleged invention in the Patent;
- whether the references to be combined are reasonably pertinent to the problems to which the inventions of the Patent are directed;
- whether the combination is of familiar elements according to known methods that yields predictable results;
- whether a combination involves the substitution of one known element for another that yields predictable results;
- whether the combination involves the use of a known technique to improve similar items or methods in the same way that yields predictable results;
- whether the combination involves the application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;
- whether the combination is “obvious to try”;
- whether the combination involves the known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces, where the variations are predictable to a POSITA;
- whether there is some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention;

- whether the combination requires modifications that render the prior art unsatisfactory for its intended use;
- whether the combination requires modifications that change the principle of operation of the reference;
- whether the combination is reasonably expected to be a success; and
- whether the combination possesses the requisite degree of predictability at the time the invention was made.

37. I understand that in determining whether a combination of prior art references renders a claim obvious, it is helpful to consider whether there is some teaching, suggestion, or motivation to combine the references and a reasonable expectation of success in doing so. I understand, however, that a teaching, suggestion, or motivation to combine is not required.

D. Secondary Considerations of Non-Obviousness

38. I understand that certain secondary considerations may be considered in evaluating obviousness to prevent hindsight bias. These secondary considerations include the commercial success of products that practice the patent, the long-felt need for the patented technology, the failure of others to solve the problem addressed by the patent, initial skepticism by others in the industry, industry recognition and praise of the patented products, and efforts by others to copy the patented technology.

39. I have been informed that these secondary considerations of non-obviousness must be balanced against the strength of the prima facie case of obviousness. Where the invention represents no more than the predictable use of prior art elements

according to their established functions, secondary considerations are inadequate to establish non-obviousness.

V. LEVEL OF ORDINARY SKILL IN THE ART

40. I am familiar with the level of ordinary skill in the art with respect to the '429 Patent around its filing date and its claimed priority date. Based on my experience working, teaching, and conducting research in the relevant field, and based on my review of the '429 Patent specification, claims, file history, and prior art, I believe one of ordinary skill in the art around the time of the alleged invention of the '429 Patent would have had at least a bachelor's degree in electrical engineering, materials science, mechanical engineering, or a related field, and two years of experience in the design and/or development of display devices or consumer electronics, including familiarity with OLED displays, flexible display panels, display module structures, adhesives, and/or packaging technologies, with additional education substituting for experience and vice versa.

41. In determining the level of ordinary skill in the art, I considered, for example, the type of problems encountered in the art, prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field.

42. I met or exceeded the knowledge and experience that a POSITA would have had as of the priority date of the '429 Patent (March 11, 2022).

43. Consistent with this background and experience, I am also familiar with the knowledge of the POSITA as of the priority date of the '429 Patent. I can opine on how the POSITA would have understood the disclosure and claims of the '429 Patent, the disclosures of the prior art, the motivation and/or suggestion to combine the prior art, and what combinations would have been obvious to a POSITA.

VI. SUMMARY OF MY OPINIONS

44. Based on my experience, knowledge of the art as of the effective filing date of the '429 Patent, analysis of prior art references, and understanding of the claim terms (in view of the specification that a POSITA would have as of the effective filing date), it is my opinion that the Challenged Claims of the '429 Patent are unpatentable as obvious over the prior-art references discussed below.

45. As I explain in detail below, it is my opinion that Claims 1–20 of the '429 Patent would have been obvious under 35 U.S.C. § 103 on the following grounds:

- **Ground 1:** Claims 1–5, 9, and 11–15 are rendered obvious by Yi1 (Ex-1005)
- **Ground 2:** Claims 7–8 and 17–18 are rendered obvious by Yi1 in view of Yi2 (Ex-1006)
- **Ground 3:** Claims 6 and 16 are rendered obvious by Yi1 in view of Zhang (Ex-1007)
- **Ground 4:** Claims 10 and 20 are rendered obvious by Yi1 in view of Park (Ex-1008)

VII. TECHNOLOGY BACKGROUND

46. Organic light-emitting diode (“OLED”) technology has been widely adopted in modern display panels due to its advantages of lightweight construction, high

color gamut, wide viewing angles, fast response times, high contrast ratios, and self-emitting characteristics that eliminate the need for a separate backlight unit, resulting in fewer components, thinner profiles, and lower power consumptions compared to liquid crystal displays (“LCDs”). *See* Ex-1009 at 8, 101; Ex-1010 at 174, 412. By the priority date of the ’429 Patent (March 11, 2022), OLED display panels were well known in the art and had been commercially deployed in smartphones, televisions, and wearable devices for over two decades.

47. An OLED panel generally comprises a display area and a non-display area. The display area features a transparent glass cover under which an active pixel array can be used to create an image. The non-display region houses the peripheral circuitry, including power routing, driver circuit integration, and bending structures that cannot be placed within the active pixel array. In LTPS-TFT OLED displays, scan drivers and data drivers are integrated on the substrate periphery to reduce the number of external connections and the display’s footprint. *See* Ex-1009 at 198; Ex-1011 at 479.

48. OLED panels employ thin-film transistor (TFT) backplanes to drive individual sub-pixels. Active-matrix OLED displays use two-transistor, one-capacitor (2T1C) circuits at each pixel to provide a controlled current source with storage, enabling continuous pixel emission and accurate grayscale. *See* Ex-1009 at 130. A typical OLED display panel comprises a substrate (which may be a flexible

organic substrate), a pixel driving circuit layer formed of multiple patterned conductive and insulating thin-film layers (including semiconductor layers, gate metal layers, insulating layers, and source/drain metal layers that form TFTs and capacitors), and an OLED emitting layer on top. Power supply lines (e.g., ELVDD and ELVSS) provide driving voltages to the pixel circuits. The various TFT technologies used for OLED backplanes include low-temperature polysilicon (LTPS) and oxide semiconductors (such as InGaZnO), both of which provide the mobility and stability needed for current-driven OLED pixels. *See* Ex-1009 at 126, 207.

49. As OLED panels adopted flexible organic substrates, the interfaces between these organic substrates and the inorganic layers deposited thereon became susceptible to polarization effects that could alter the electrical characteristics (e.g., threshold voltage and electron mobility) of the overlying thin-film transistors. This sensitivity arises because organic polymer substrates have inherently poor barrier properties compared to glass (being roughly ten million times more permeable to water and oxygen) requiring the deposition of inorganic barrier layers (such as SiNx or Al₂O₃) directly onto the organic substrate. *See* Ex-1011 at 500; Ex-1009 at 240.

The mismatch between organic and inorganic layers at these interfaces, combined with trapped charges and ionic contaminants, introduces polarization phenomena that necessitate shielding of the active semiconductor layers. To address this, the art

developed “shielding layers”—conductive metal patterns disposed between the substrate and the pixel driving circuit layer—that shield the active semiconductor layers from polarization of organic materials in the substrate. These shielding layers (also referred to as “lower pattern layers”) were well established in the art before the priority date of the ’429 Patent.

50. To electrically bias these shielding layers and prevent electrostatic discharge (ESD) damage, it was known in the art to connect the shielding layer to a power supply voltage (e.g., ELVDD) through converging wires—horizontal conductive patterns disposed at the periphery of the shielding layer, in the non-display region—that route from the power supply lines to the mesh-shaped shielding blocks via through holes (contact holes) that penetrate the intervening insulating layers. This architecture is precisely what the ’429 Patent claims, and it was well known before the priority date.

51. In flexible OLED panels, it is also common to include a bending area in the non-display region where the panel folds to reduce the bezel width. OLED displays have been known to be flexible since at least the 2013 timeframe. Flexible OLED panels have been widely reported as enabling round-shape bezel configurations in smartphones, where the panel bends around the edge to minimize the visible border. *See* Ex-1009 at 128. The non-display region houses peripheral circuitry, fan-out wiring, and power connections that are routed through or around this bending area,

and is a standard architectural feature of flexible OLED displays. *See* Ex-1011 at 479, 489. Fan-out lines and power connections are routed through or around this bending area, and the converging wires that connect the shielding layer to the power supply lines are disposed in the non-display regions on one or both sides of the display area.

VIII. THE CHALLENGED PATENT

52. The '429 Patent, titled “Display Panel and Display Device,” names Xing Wu as its sole inventor and is assigned to Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd. Ex-1001, Cover, 1:5–11. The '429 Patent issued on October 29, 2024, from U.S. Application No. 17/764,557, which is the U.S. national stage of PCT Application No. PCT/CN2022/082256, filed March 22, 2022, and claims priority to Chinese Application No. 202210237733.1, filed March 11, 2022.

53. The '429 Patent contains 20 claims. Independent Claim 1 is directed to a display panel, and Claim 11 is directed to a display device comprising the display panel of Claim 1, “wherein the display panel is an organic light-emitting diode (OLED) panel.” Ex-1001, 8:62–9:20, 10:43–45. Dependent Claims 2–10 and 12–20 largely mirror one another, reciting parallel panel and device limitations.

54. The '429 Patent concedes that OLED panels and bottom shielding metals were already known in the art. It acknowledges that OLED screens “are currently widely

used and have advantages of light weight and high color gamut value.” Ex-1001, 1:21–23. The ’429 Patent also admits that “more and more of the OLED screens adopt bottom shielding metals to shield pixel driving circuits at the interfaces between the substrates and the inorganic layers.” Ex-1001, 1:28–31.

55. The ’429 Patent identifies only a narrow alleged problem: prior bottom shielding metals had “serrated edges,” and electro-static discharge (ESD) explosions were “likely to occur at tips of serrations, thereby affecting a display effect.” Ex-1001, 1:31–35. The purported solution involves a display panel in which the converging wire between two adjacent through holes is disposed according to the shortest distance between the two adjacent through holes, so that the “expected current path” flows within the boundary of the converging wire and charge accumulation is reduced. Ex-1001, 8:18–27.

56. Figures 1-3 of the ’429 Patent illustrate the disclosed embodiment. Figure 1 is a cross-sectional view showing the panel’s layer stack: a substrate 1 (red), a shielding layer 2 (blue) located on the substrate 1, a bottom insulating layer 30 (green), a buffer layer 31, a pixel driving circuit layer 4 (purple), and a plurality of power supply lines 7 (yellow). Ex-1001, 4:8-16, Fig. 1.

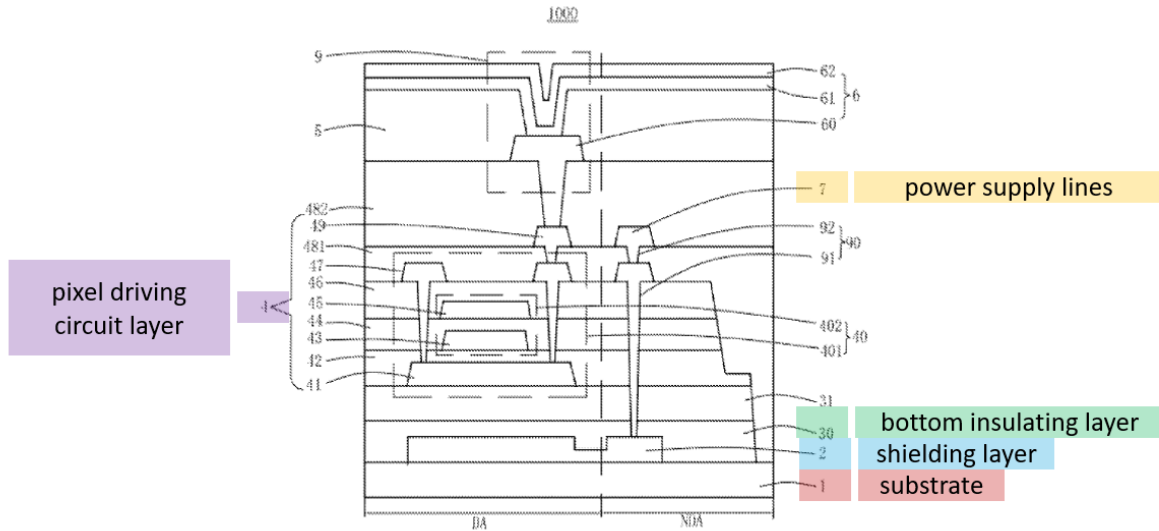
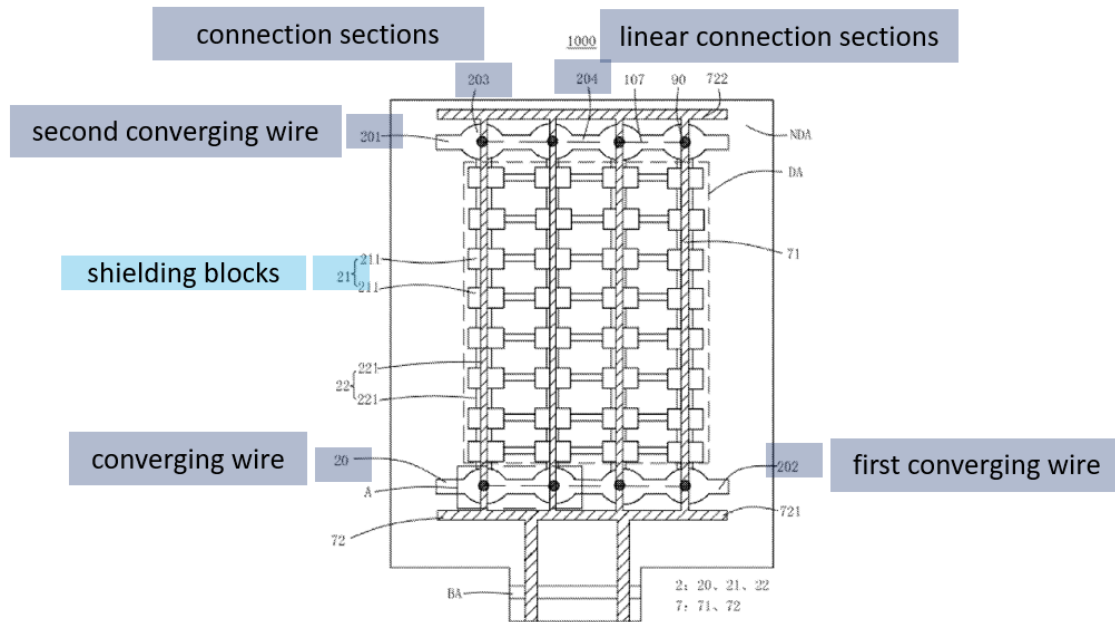


FIG. 1

57. Figure 2 shows a top-down view of the display panel. The shielding layer 2 includes a converging wire 20 located in the non-display region adjacent to the display region. Ex-1001, 4:36-42. The converging wire 20 (dark blue) includes a first converging wire 201 (dark blue) located in the first non-display region—which contains the bending sub-region BA at which the display panel bends—and a second converging wire 202 (dark blue) located in the second non-display region. Ex-1001, 4:3-7, 4:43-51. Each converging wire includes a plurality of first connection sections 203 (dark blue), the peripheries of which are arc shaped (e.g., “approximately oval or circular”), and a plurality of approximately linear second connection sections 204, each connected between a middle portion of two adjacent first connection sections 203, with a maximum width of the first connection sections 203 greater than a width of the second connection sections 204. Ex-1001, 4:51-64.

The shielding layer further includes a plurality of shielding blocks 211 arranged in an array, with each column of shielding blocks 211 (light blue) connected to a corresponding one of the first connection sections 203. Ex-1001, 5:1-13, Figs. 2, 3.



58. The pixel driving circuit layer is comprised of several sublayers: a semiconductor layer 41, a first insulating layer 42, a first gate metal layer 43, a second insulating layer 44, a second gate metal layer 45, an interlayer insulating layer 46 (i.e., a fourth insulating layer), a third metal layer 47 (i.e., a second conductive metal layer), a first planarization layer 481 (i.e., a third insulating layer), a fourth metal layer 49 (i.e., a first conductive layer), and a second planarization layer 482. Ex-1001, 5:22-46. The plurality of power supply lines 7 are disposed in the fourth metal layer 49 and are electrically connected to the first connection

sections 203 of the converging wire 20 through a plurality of through holes 90. Ex-1001, 6:47–51, 7:19-22. The through holes 90 include first through holes 91, which penetrate the first insulating layer 42, the second insulating layer 44, and the interlayer insulating layer 46, and second through holes 92, which penetrate the first planarization layer 481. The first through holes 91 “are communicated with the plurality of second through holes 92,” and the diameter of each first through hole 91 is smaller than the diameter of each second through hole 92. Ex-1001, 7:30–43.

IX. PROSECUTION HISTORY OF THE '429 PATENT

59. I have reviewed the prosecution history of the '429 Patent. The '429 Patent was allowed without any rejections. The prior art relied upon in the Petition—including Yi1, Yi2, Zhang, and Park—was not considered by the Examiner during prosecution of the '429 Patent. Therefore, the Grounds discussed in the Petition present new arguments and prior art that were not evaluated during prosecution. Ex-1004.

X. PRIORITY DATE

60. For purposes of this proceeding only, I have been asked to assume the earliest alleged priority date of the '429 Patent: March 11, 2022. Each of the prior art references relied upon in this Declaration qualifies as prior art to the '429 Patent under 35 U.S.C. § 102(a)(1) or § 102(a)(2).

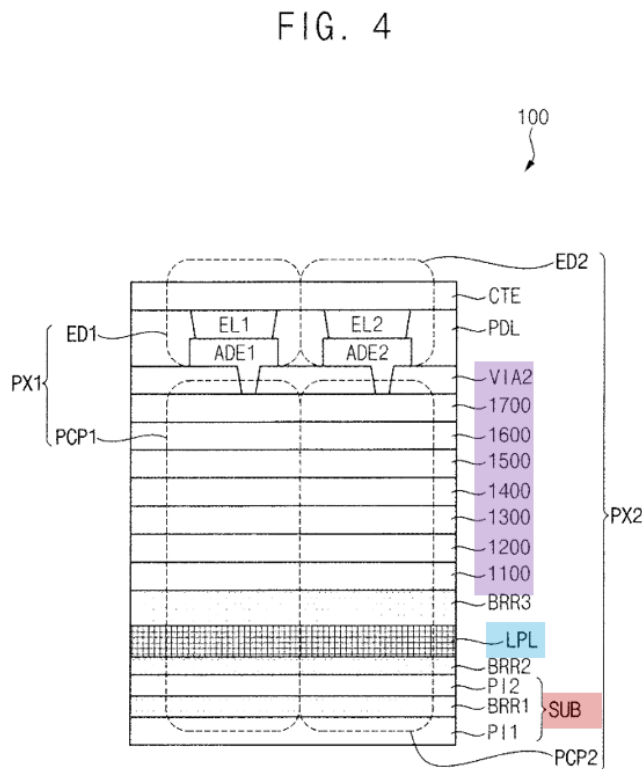
XI. CLAIM CONSTRUCTION

61. I have been informed that in an IPR proceeding, claims are interpreted under the *Phillips* standard. 37 C.F.R. §42.100(b). I understand that no term requires express construction to resolve this Petition. The claims are given their plain and ordinary meaning as understood by a POSITA in view of the specification.

XII. OVERVIEW OF THE APPLIED PRIOR ART REFERENCES**A. Yi1 (Ex-1005)**

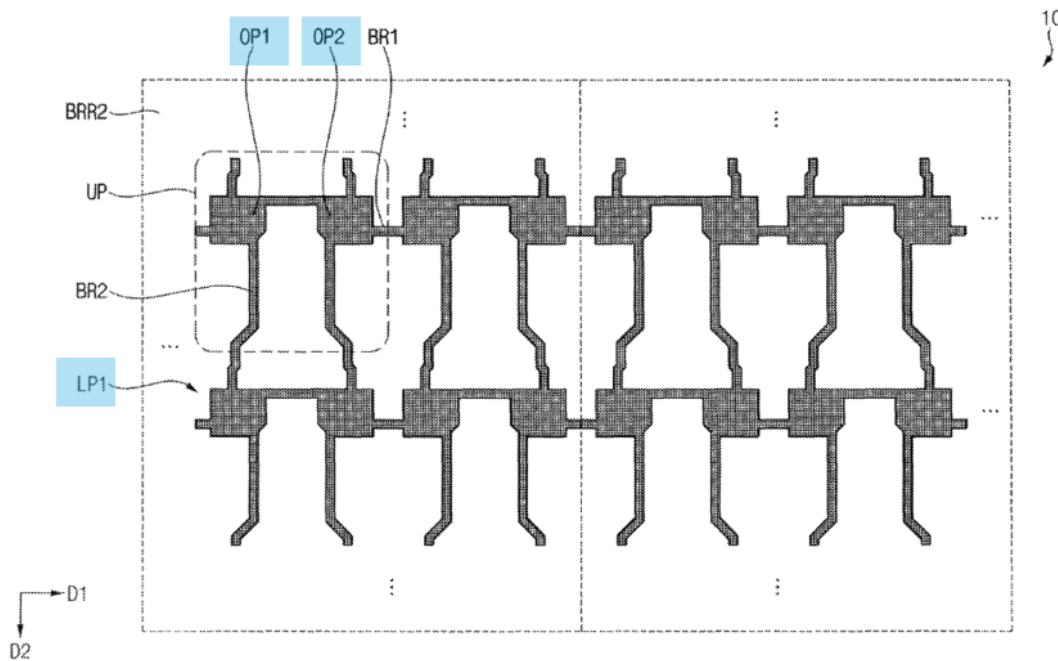
62. Yi1 (U.S. Patent No. 11,963,404) (Ex-1005) was filed on July 14, 2021, issued on April 16, 2024, and claims priority to a Korean application filed November 30, 2020. Because Yi1 was filed before the earliest alleged priority date of the '429 Patent (March 11, 2022), Yi1 is prior art to the '429 Patent under at least 35 U.S.C. §102(a)(2).

63. Yi1 is directed to a display device that includes a lower pattern layer (LPL) (light blue) disposed between the substrate (red) and the active patterns of the pixel circuits (purple). Figure 4 illustrates these layers:



64. The LPL includes a plurality of unit patterns UP—each composed of an overlap pattern OP and connecting bridges—repeatedly arranged in a mesh shape.

FIG. 8



65. The overlap patterns shield the first active pattern from polarization of organic materials in the substrate so that electrical characteristics of the transistors are not changed. A key inventive aspect of Yi1 focuses on the geometric layout, step-height, and spacing arrangement around the bending protection layer and the cover plate window module edge. The LPL is designed with dimensional boundary positioning and setback relative to the bending area, the bending protection layer, and adjacent layers.

66. Yi1's LPL is supplied with the power voltage ELVDD through horizontal patterns (HP1 (dark blue), HP2) disposed along its edges. HP1, extending linearly in direction D1, is connected to a power voltage bus BUS1. HP2 contacts an intermediate connection pattern ICP through a second contact hole CNT2, and the ICP contacts a power voltage pattern BUS2—provided together with power voltage line 1720—through a first contact hole CNT1.

FIG. 22

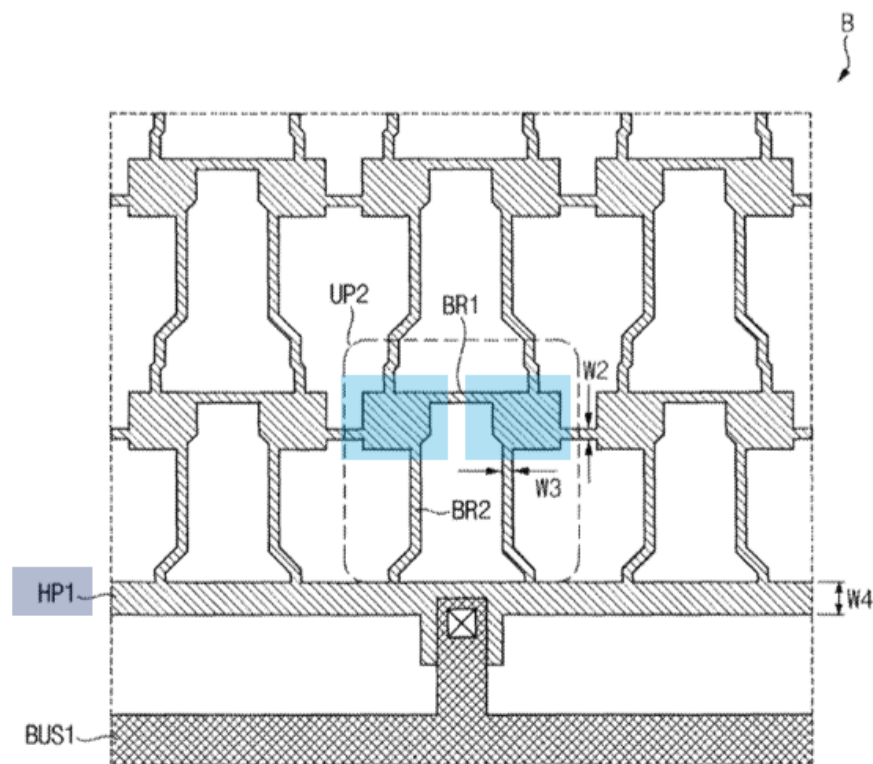
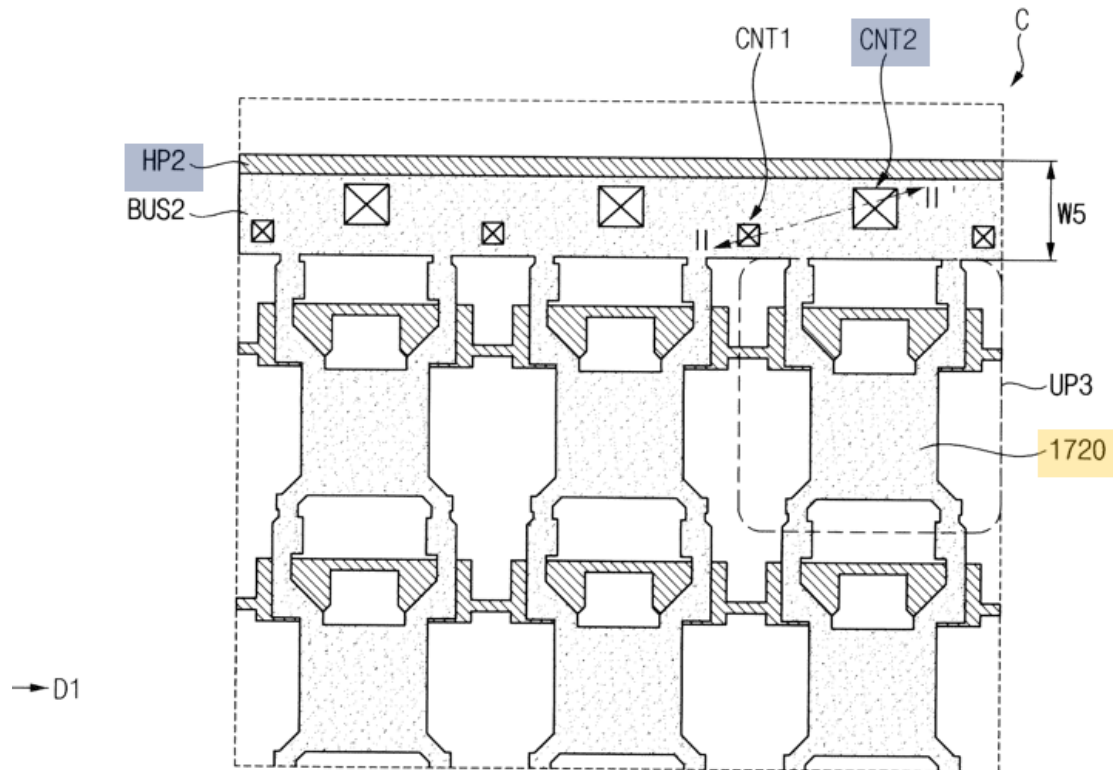


FIG. 23



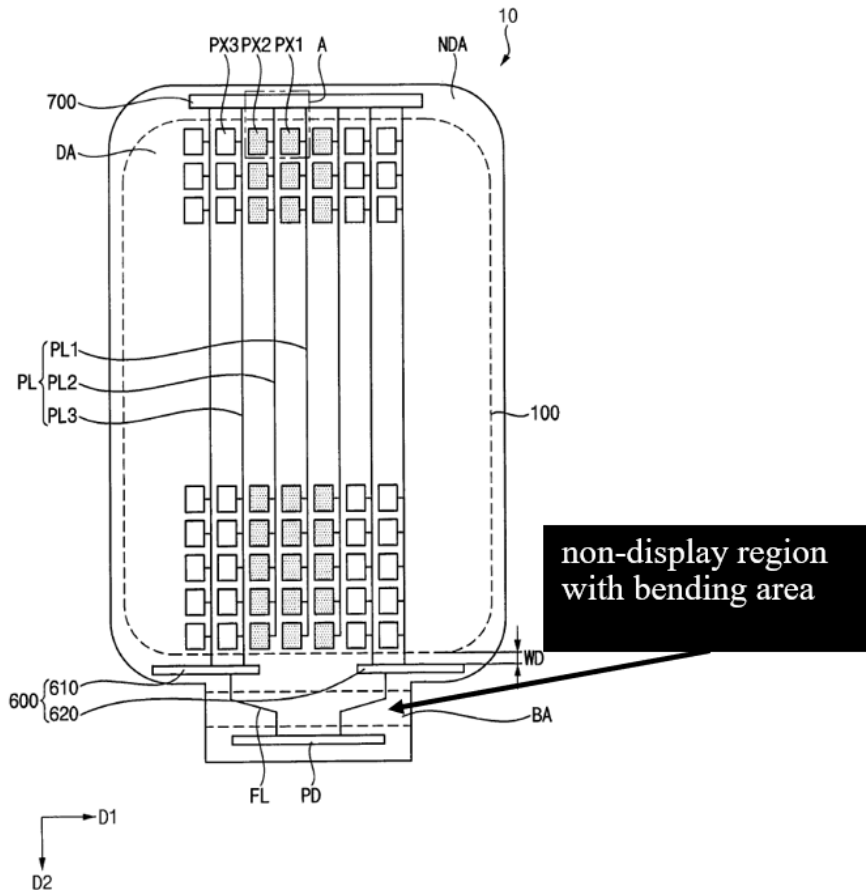
67. The horizontal patterns thereby transmit the power voltage ELVDD to the unit patterns and reduce voltage drop. Yi1 is a Samsung Display patent naming inventor Changho Yi and is directed to the same alleged invention as the '429 Patent: a display panel with a biased shielding layer disposed beneath the pixel driving circuit layer, comprising a plurality of shielding blocks and a converging wire connected to the panel's power supply lines through stacked through holes.

B. B. Yi2 (Ex-1006)

68. Yi2 (U.S. Patent Application Publication No. 2022/0199741) (Ex-1006) was filed on July 21, 2021, published on June 23, 2022, and claims priority to a Korean application filed December 18, 2020. Because Yi2 was filed before the earliest alleged priority date of the '429 Patent (March 11, 2022), Yi2 is prior art to the '429 Patent under at least 35 U.S.C. §102(a)(2).

69. Yi2 discloses a display device that is substantially similar in architecture to Yi1. Yi2's device includes a first lower pattern LP1 disposed on the substrate in the display area DA, including a plurality of unit patterns UP with overlap patterns, first bridges BR1, and second bridges BR2, repeatedly arranged in a mesh shape. Yi2 further discloses a "bending area BA" included in the "non-display area NDA." Yi1 and Yi2 are commonly assigned Samsung Display patent documents sharing inventor Changho Yi, filed one week apart, with closely analogous lower-pattern/shielding architectures and nearly identical layer stacks.

FIG. 1



C. Zhang (Ex-1007)

70. Zhang (U.S. Patent No. 9,658,523) (Ex-1007), filed on March 31, 2014, and issued on May 23, 2017, is prior art to the '429 Patent under at least 35 U.S.C. §102(a)(1). Zhang discloses an interconnect structure having wavy metal lines that accommodate large self-aligned vias. The metal line profile resembles a “bicycle chain” structure in which wide portions (via landing pads) with arc-shaped peripheries are spaced periodically between narrow linear portions. The wide portions accommodate via landing pads that exceed the width of the narrow portions,

and adjacent lines can be staggered to maintain constant spacing. Figure 1B shows this “bicycle chain:”

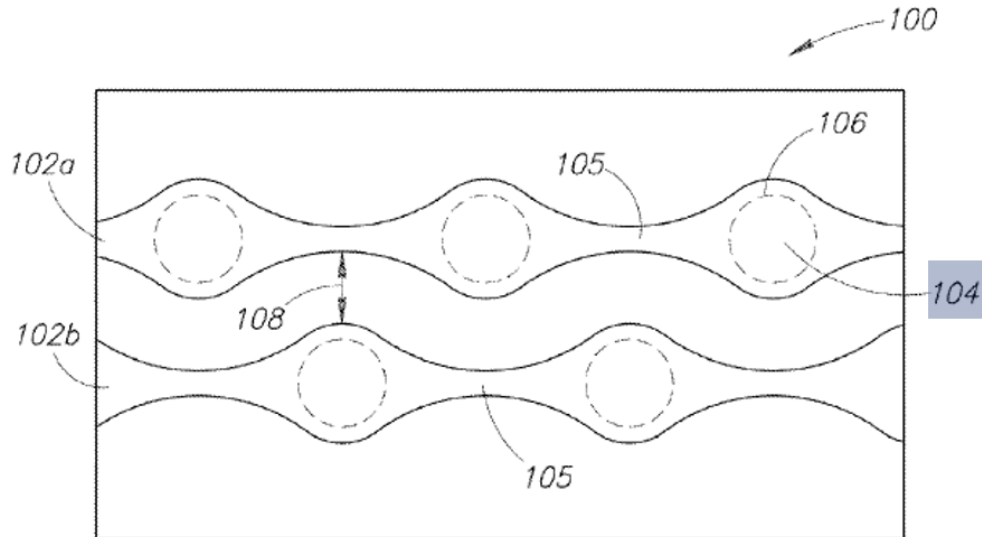


FIG.1B

71. Figure 7B shows the final wavy metal line structures 120 after metal fill, including narrow portions 122, intermediate width portions 123, and wide portions 124. Ex-1007, 5:44–57, Fig. 7B. The wide portions have rounded, arc-shaped peripheries resulting from the optical lithography process (OPC), creating a wavy undulating profile. Ex-1007, 6:5–30. The “rounded features forming the wavy metal line structures 120 are intentionally created by leveraging distortion that occurs in the lithography process”—corners of rectangular mask features “transfer to the photoresist and the metal trench as rounded features.” Ex-1007, 6:9–30. As Figure 7B illustrates, the wide portions (via landing pads) have arc-shaped (rounded)

peripheries, while the narrow portions connecting them are linearly shaped, and the maximum width of the wide portions (via landing pads) is greater than the width of the narrow connecting portions:

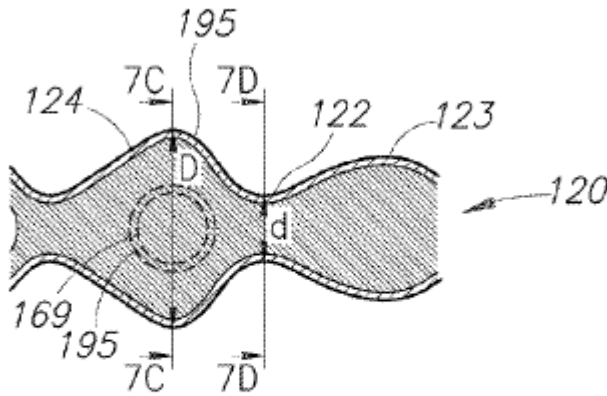


FIG. 7B

72. The rounded features are intentionally created by leveraging optical lithography distortion. Zhang supplies the recited arc-shaped geometry of dependent Claims 6 and 16.

D. Park (Ex-1008)

73. Park (U.S. Patent No. 7,335,912) (Ex-1008), issued on February 26, 2008, is prior art to the '429 Patent under at least 35 U.S.C. §102(a)(1). Park discloses an organic light emitting display having an “improved via hole.” Park explains that when the size of a via hole is reduced, a pattern defect may be generated when

patterning the lower electrode. Park solves this by forming the via hole to be larger than the contact hole in a structure where the via hole is formed corresponding to the contact hole, which prevents patterning defects and improves processing stability and reliability. Park supplies the express motivation for dimensioning stacked through holes such that the upper hole is larger than the lower hole, as recited in Claims 10 and 20.

FIG. 4A

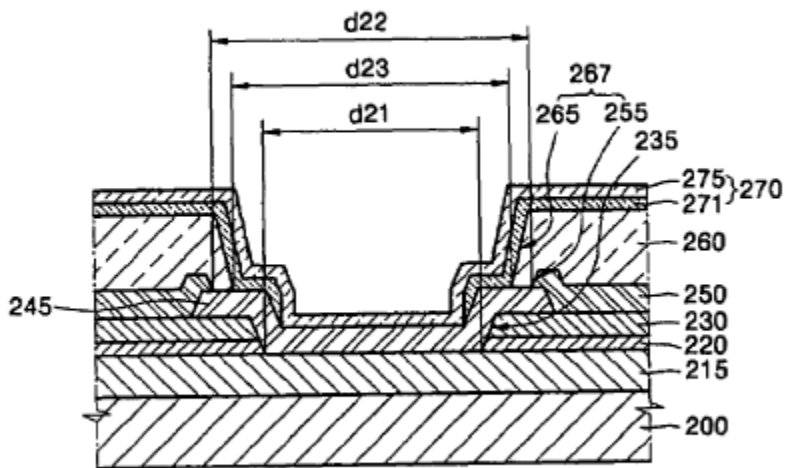
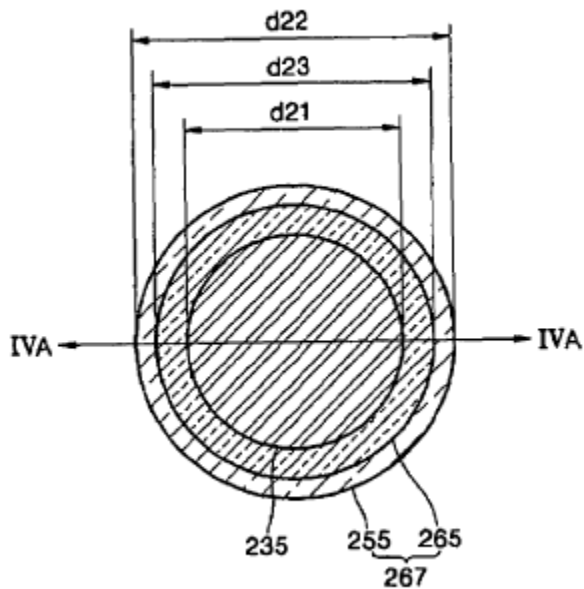


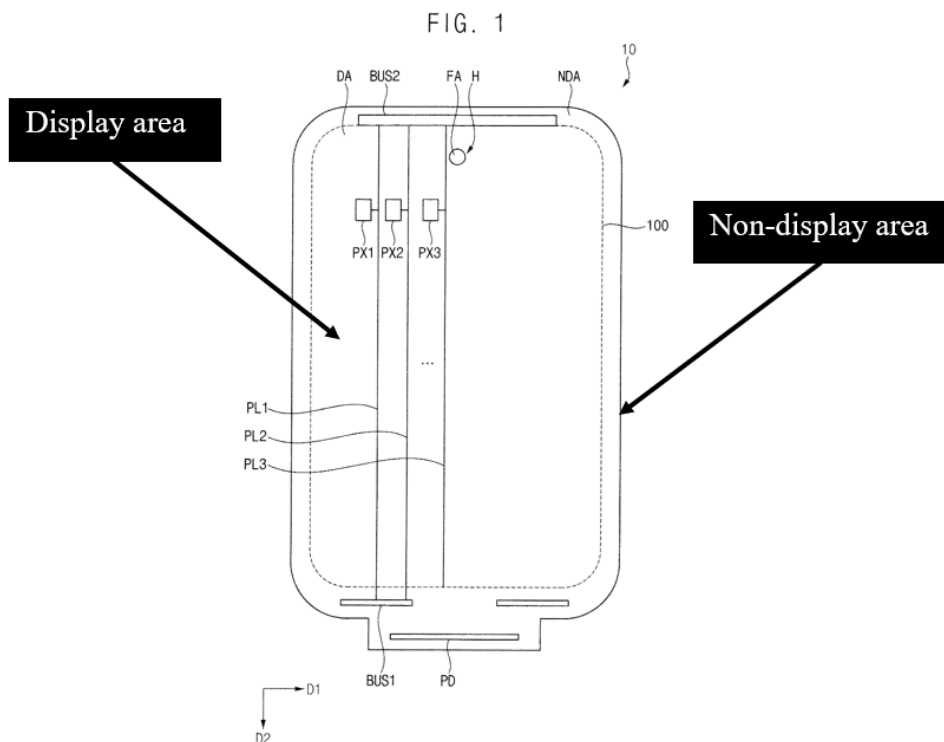
FIG. 4B



XIII. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS**A. Ground 1: Claims 1–5, 9, and 11–15 Are Rendered Obvious by Yi1****1. Independent Claim 1**

- a. Element 1[pre]: A display panel, comprising a display region and a non-display region disposed on at least one side of the display region, wherein the display panel comprises:**

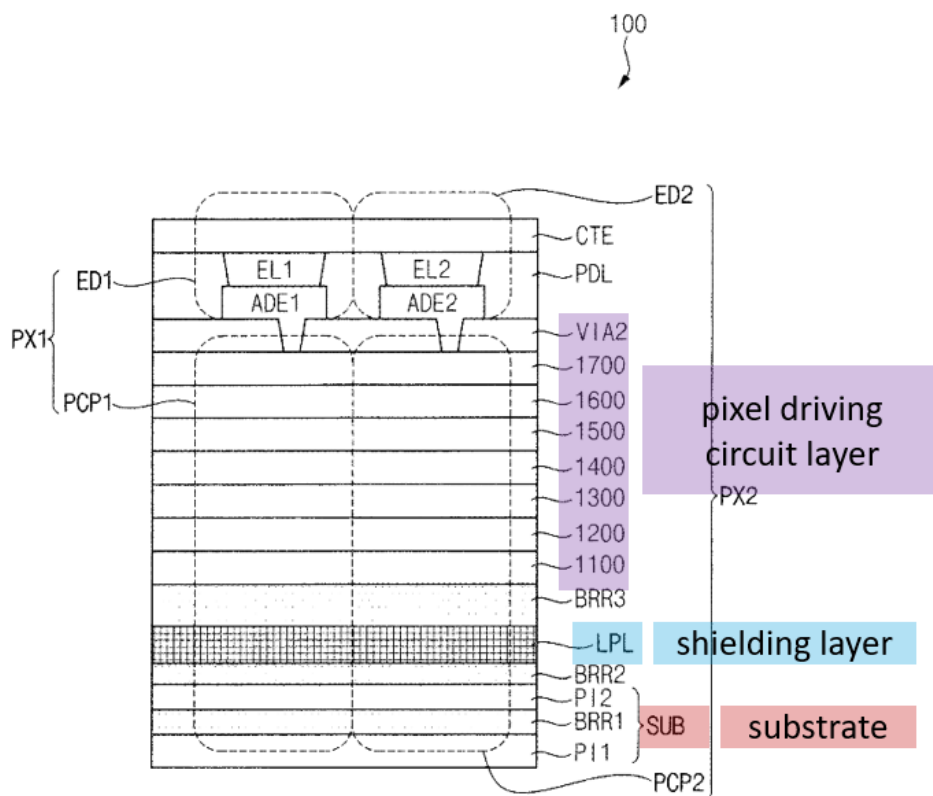
74. To the extent the preamble is limiting, Yi1 teaches a display panel, comprising a display region and a non-display region disposed on at least one side of the display region. Yi1 teaches a display device which may be “divided into a hole area FA, a display area DA, and a non-display area NDA.” Ex-1005, 6:9–11. As shown in Figure 1, the non-display area “surround[s] the display area” and is on all four sides of the display area, so is on “at least one side” of the display area. Ex-1005, 6:16–18. From a technical standpoint, this arrangement is standard practice in OLED panel design, where the non-display region houses peripheral circuitry, power routing, and bending structures that cannot be placed within the active pixel array. *See* Ex-1009, 198; Ex-1011, 479.



b. Element 1[a]: a substrate;

75. Yi1 teaches element 1[a]. Yi1 discloses a layer stack that makes up a display panel (Figure 4), which includes a “first organic film layer PI1, [a] first barrier layer BRR1, and [a] second organic film layer PI2,” and Yi1 teaches that these layers “constitute a substrate SUB.” Ex-1005, 10:51–11:5 (red in Figure 4, below). This organic substrate structure is consistent with flexible OLED panel designs, in which alternating organic and inorganic barrier layers provide both mechanical flexibility and moisture/oxygen barrier properties essential for OLED longevity. *See* Ex-1009, 85, 240; Ex-1010, 524-525; Ex-1011, 60, 74.

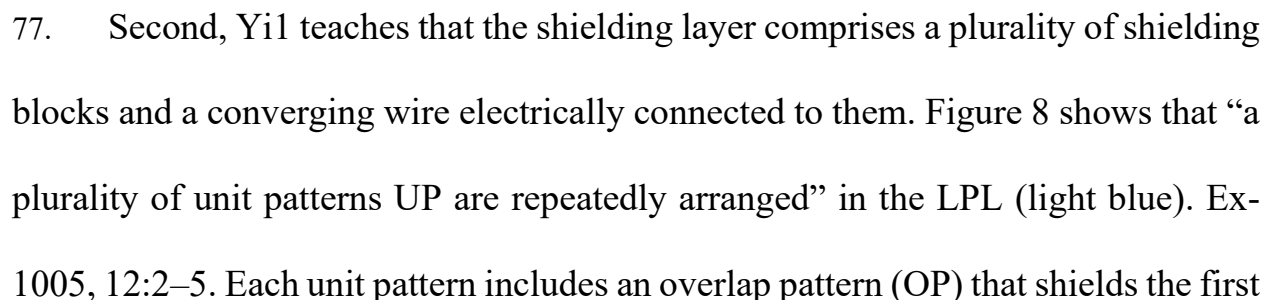
FIG. 4



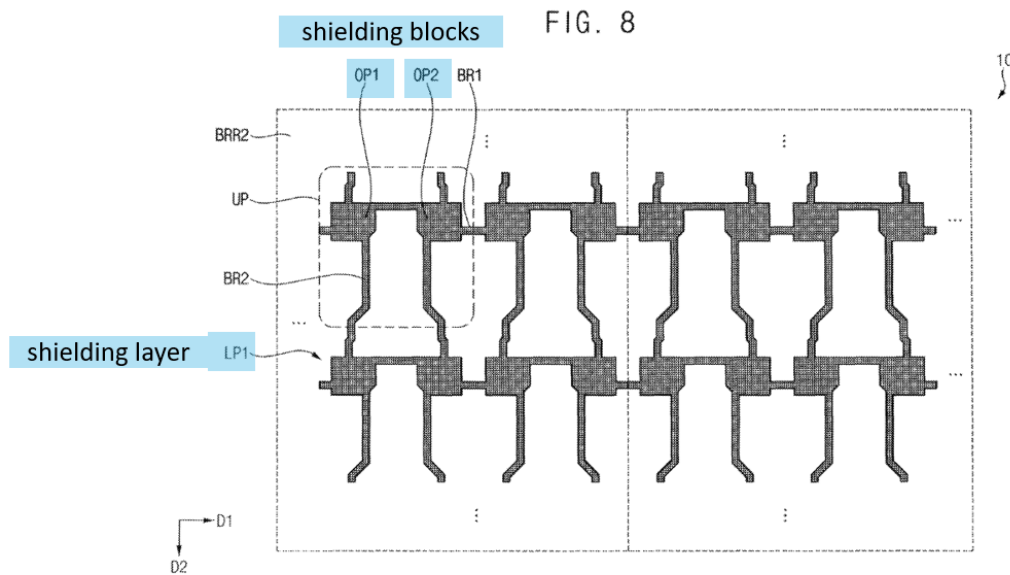
- c. **Element 1[b]: a shielding layer located on the substrate, wherein the shielding layer comprises a plurality of shielding blocks and a converging wire electrically connected to the plurality of shielding blocks, and the converging wire is located on at least one side of the plurality of shielding blocks;**

76. Yi1 teaches element 1[b]. First, Yi1 teaches a shielding layer located on the substrate. Yi1 teaches a lower pattern layer (LPL) (light blue), which shields “the polarization phenomenon from electrically affecting the first and second active patterns.” Ex-1005, 11:20–25. The LPL “shield[s] the active pattern from

FIG. 4



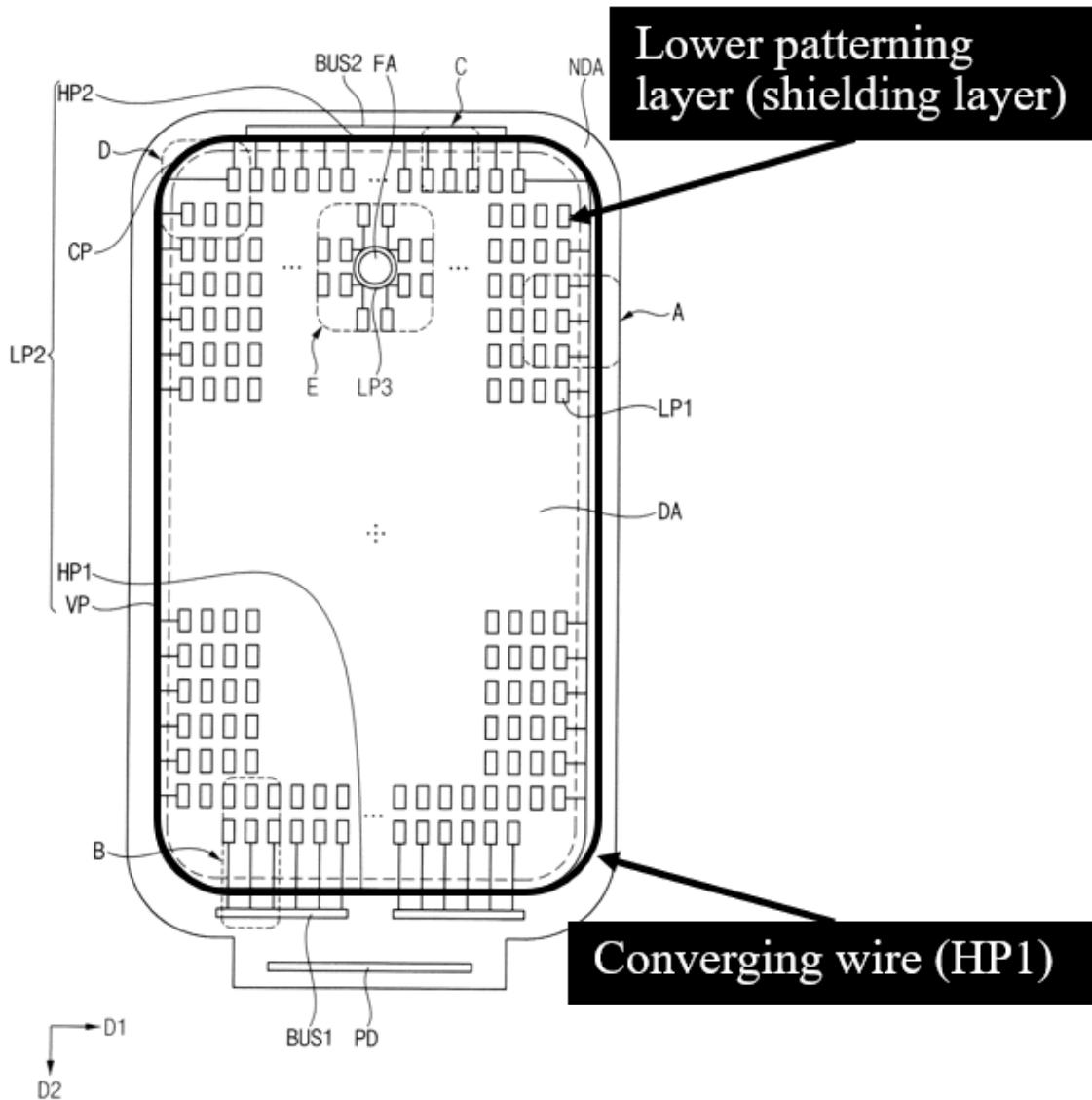
active pattern from polarization. These overlap patterns OP are the “shielding blocks.” Yi1 discloses a converging wire electrically connected to the shielding blocks. Yi1’s first horizontal pattern HP1 is “connected to the power voltage bus BUS1,” permitting the “power voltage ELVDD” to be provided to the shielding layer. Ex-1005, 20:30–40. Accordingly, HP1 is a converging wire electrically connected to the plurality of shielding blocks.



78. Third, Yi1 teaches that the converging wire is located on at least one side of the plurality of shielding blocks. As shown in Figures 19 and 22, the horizontal pattern HP1 is located at the bottom edge of the mesh-shaped LPL, i.e., on at least one side of the shielding blocks. This peripheral placement is an engineering choice that enables efficient power routing without consuming active display area—a

Inter Partes Review – Declaration of Dr. Michael Lebby
 fundamental design principle in OLED panel layout. *See* Ex-1009, 168, 186–189,
 198; Ex-1011, 479.

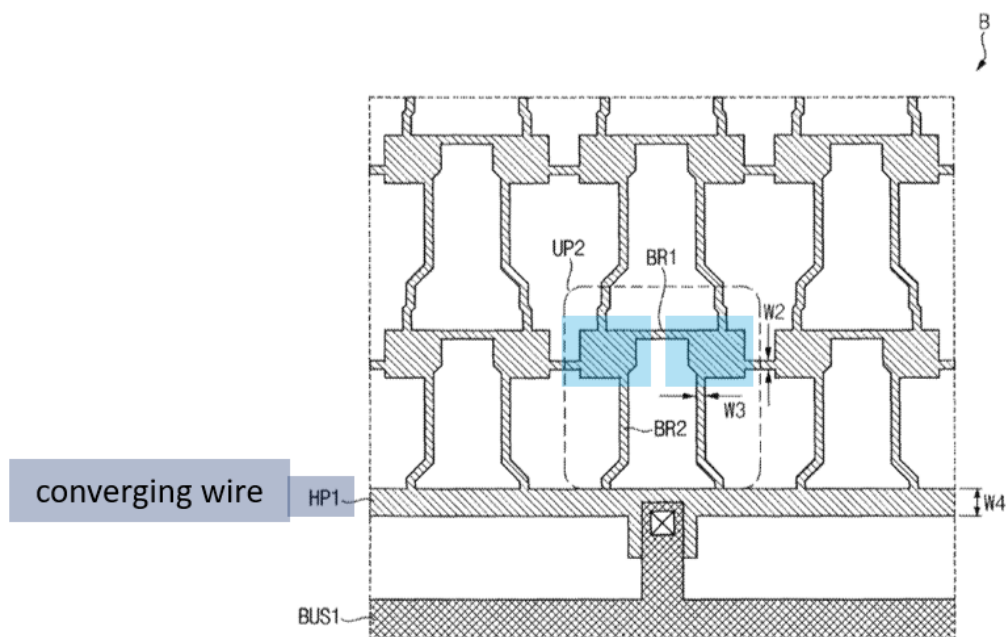
FIG. 19



79. HP1 is connected to the power voltage bus BUS1,” permitting a “power voltage ELVDD” to be provided to the shielding layer. Ex-1005, 20:30-40. And

the LPL, including the horizontal pattern, prevents “static electricity” from flowing to the “display panel,” so that “electrical breakdown [is] prevented.” Ex-1005, 23:25-29. Figure 22 provides a close up view of the relationship between the LPL (light blue), HP1 (dark blue), and the power voltage bus providing power.

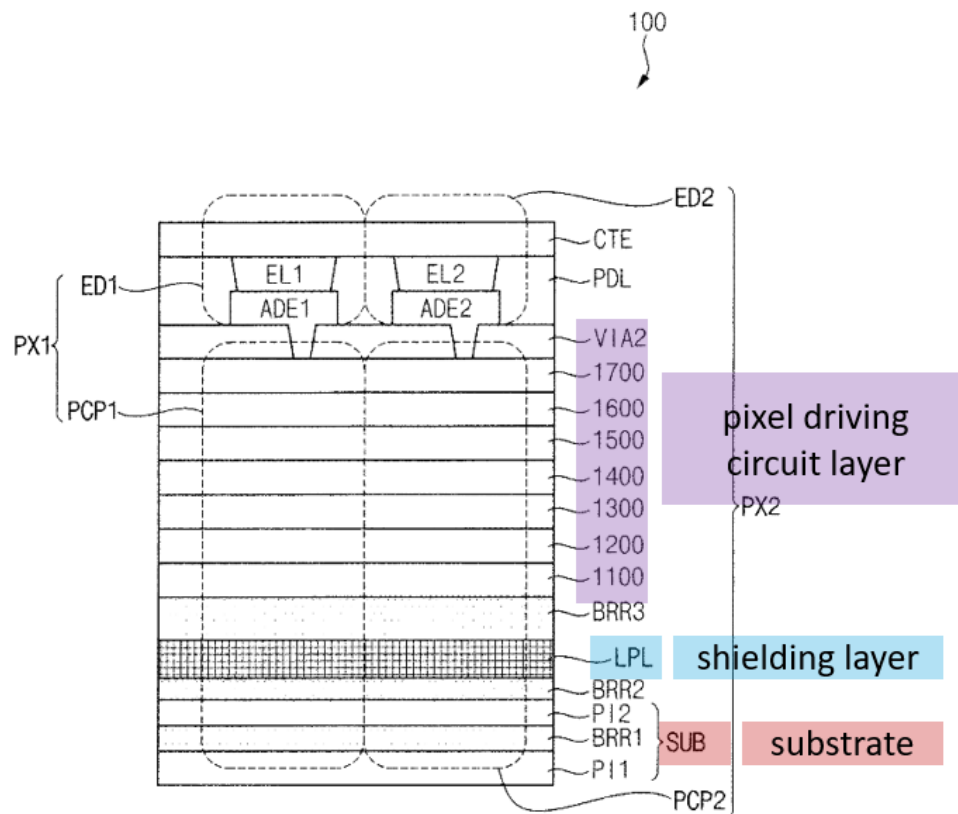
FIG. 22

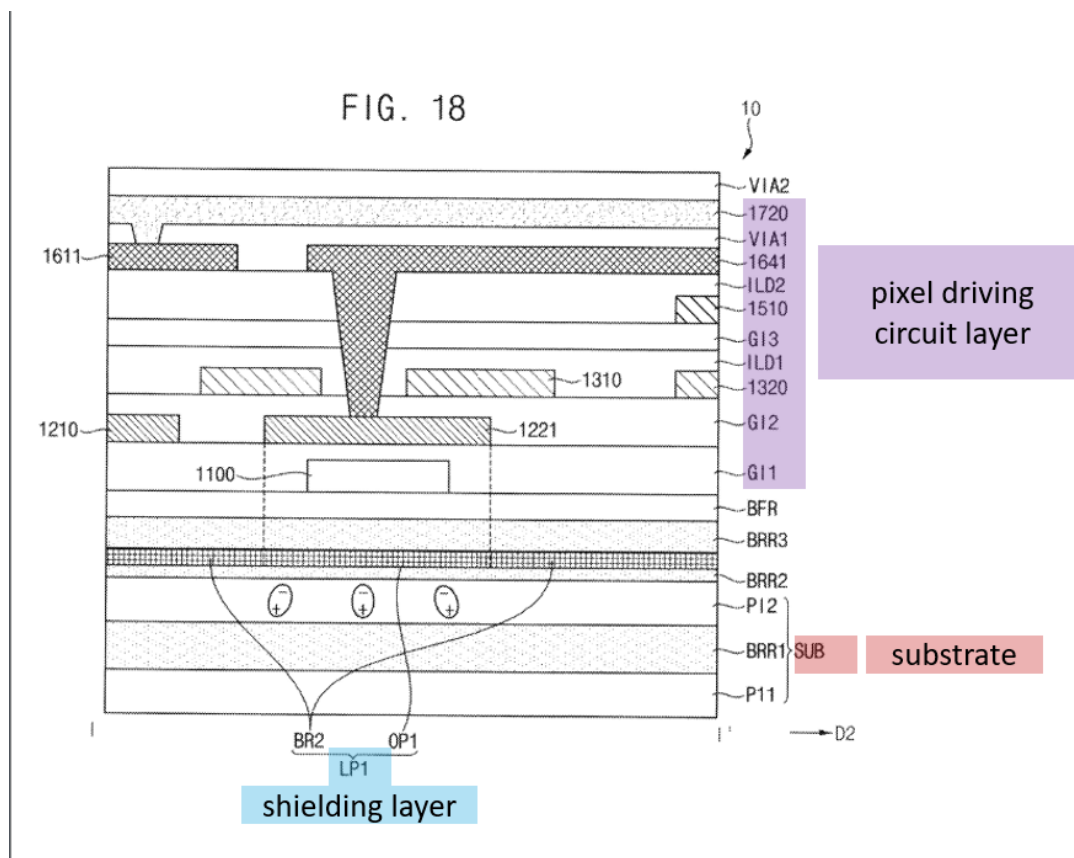


- d. **Element 1[c]: a pixel driving circuit layer located on the shielding layer, wherein the pixel driving circuit layer comprises a plurality of pixel driving circuits located in the display region, each of the plurality of pixel driving circuits at least partially overlaps a corresponding one of the shielding blocks; and**

80. Yi1 teaches Element 1[c]. Yi1 teaches a “pixel circuit part” (PCP) (purple) that includes multiple conductive and insulating layers forming the thin-film transistors that provide driving current to the emitting diodes. Ex-1005, 10:33–36. Figures 4 and 18 show the layers that make up the pixel driving circuit layer:

FIG. 4





81. As Yi1 explains, each PCP comprises a first organic film layer P11, a first barrier layer BRR1, a second organic film layer P12, a second barrier layer BRR2, a lower pattern layer LPL, a third barrier layer BRR3, a first active pattern 1100, a first conductive pattern 1200, a second conductive pattern 1300, a second active pattern 1400, a third conductive pattern 1500, a fourth conductive pattern 1600, and a fifth conductive pattern 1700. Ex-1005, 10:51-60.

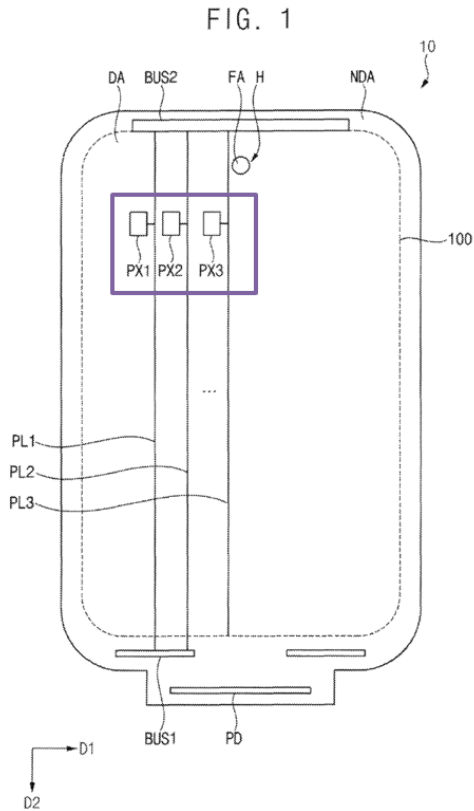
82. These layers are analogous to the layers that the '429 Patent discloses comprising the pixel driving circuit:

Referring further to FIG. 1, the pixel driving circuit layer 4 includes a semiconductor layer 41, a first insulating layer 42 located on the semiconductor layer 41, a first gate metal layer 43 located on the first insulating layer 42, a second insulating layer 44 located on the first gate metal layer 43, a second gate metal layer 45 located on the second insulating layer 44, an interlayer insulating layer 46 (i.e., a fourth insulating layer) located on the second gate metal layer 45, a third metal layer 47 (i.e., a second conductive metal layer) located on the interlayer insulating layer 46, a first planarization layer 481 (i.e., a third insulating layer) located on the third metal layer 47, a fourth metal layer 49 (i.e., a first conductive layer) located on the first planarization layer 481, and a second planarization layer 482 located on the fourth metal layer 49. The semiconductor layer 41, the first insulating layer 42, the first gate metal layer 43, the interlayer insulating layer 46, and the third metal layer 47 can jointly form the plurality of thin-film transistors 401. The first gate metal layer 43, the second insulating layer 44, and the second gate metal layer 45 can jointly form a plurality of capacitors 402. The plurality of pixel driving circuits 40 can include the plurality of capacitors 402 and the plurality of thin-film transistors 401 to drive the plurality of sub-pixels 9 to emit light.

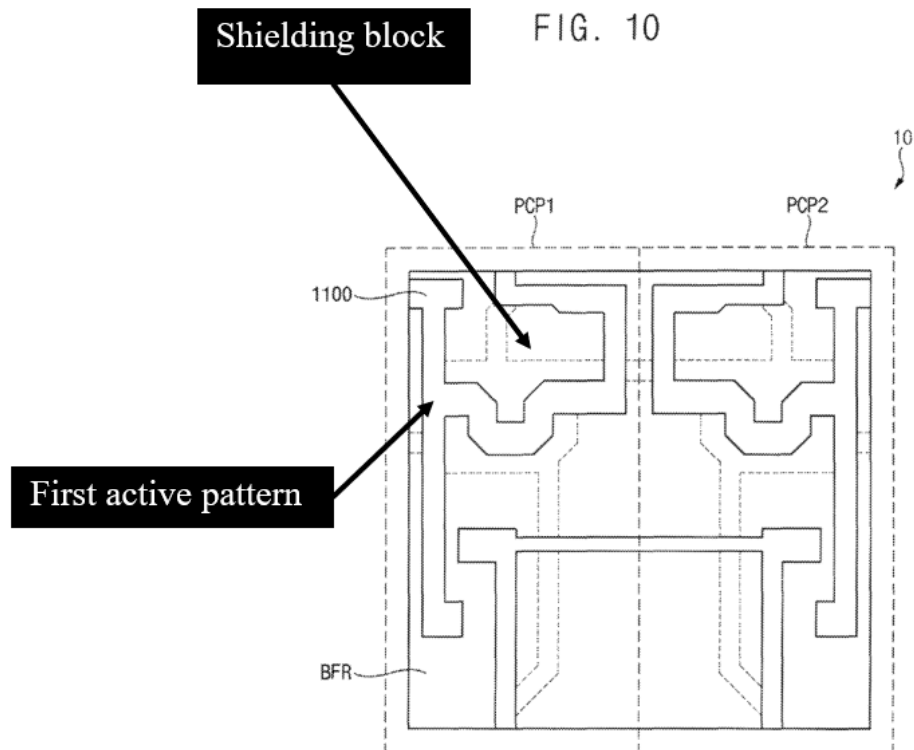
Ex-1001, 5:22-46.

83. Therefore, the Yi1's PCP is a pixel driving circuit, as claimed in the '429 Patent.

84. These pixel driving circuits are located in the display region. As Figure 1 shows, each PCP (associated with a pixel, PX1-3, boxed in purple below) is in the display region of the disclosed device.



85. Furthermore, the first active pattern (1100) of each PCP “may overlap the first lower pattern LP1.” Ex-1005, 12:65–13:7. This overlap ensures that the shielding blocks effectively shield each transistor from substrate polarization effects—confirming the spatial correspondence between each pixel driving circuit and its corresponding shielding block.



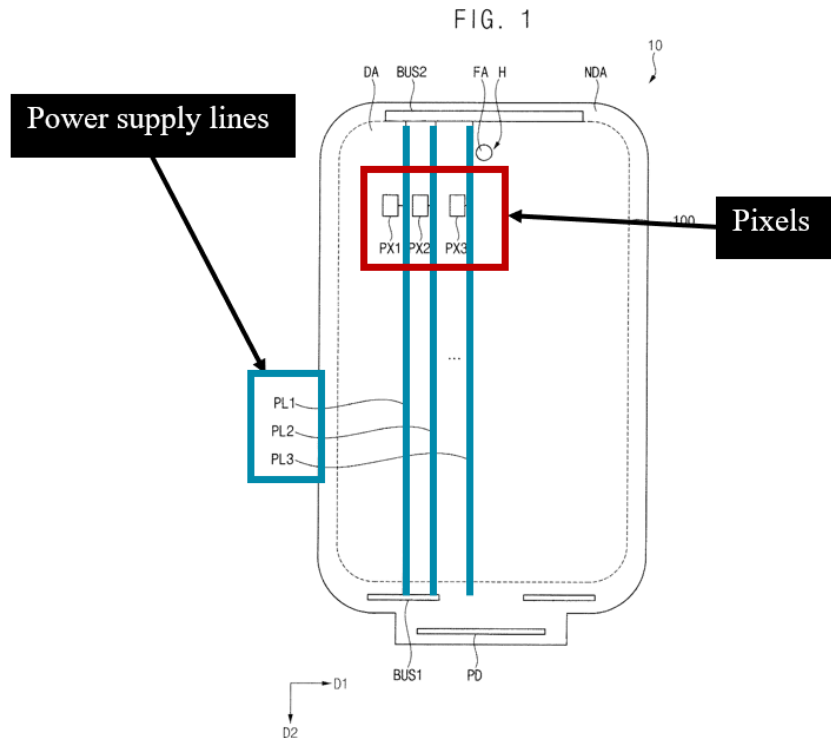
- e. **Element 1[d]: a plurality of power supply lines disposed on a side of the shielding layer away from the substrate, wherein the plurality of power supply lines are electrically connected to the converging wire through a plurality of through holes;**

86. Yi1 teaches Element 1[d]. First, Yi1 teaches a plurality of power supply lines (PL1, PL2, PL3, and 1720) disposed on a side of the shielding layer away from the substrate. Describing Figure 1, Yi1 states that

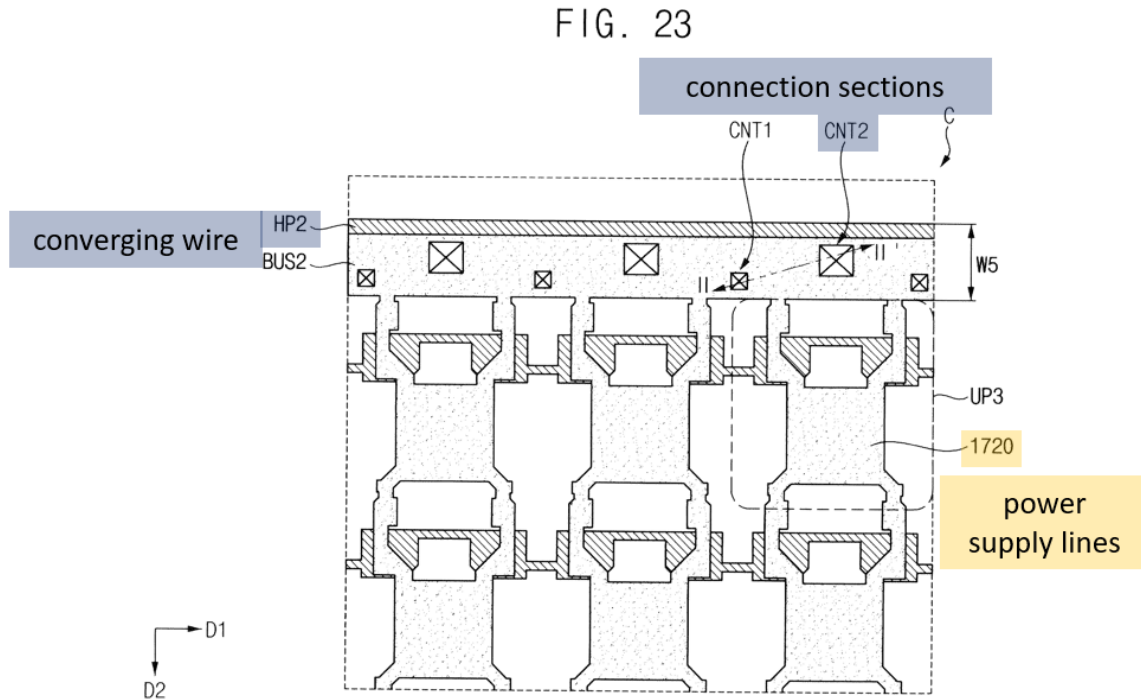
the first and second pixels PX1 and PX2 may receive the power voltage ELVDD through the first and second power voltage lines PL1 and PL2, respectively. In addition, the power voltage pattern BUS2 may receive the power voltage ELVDD through the first and second power voltage

lines PL1 and PL2. Accordingly, the third pixel PX3 may receive the power voltage ELVDD through the third power voltage line PL3.

Ex-1005, 10:4-12. These power lines highlighted in blue below:

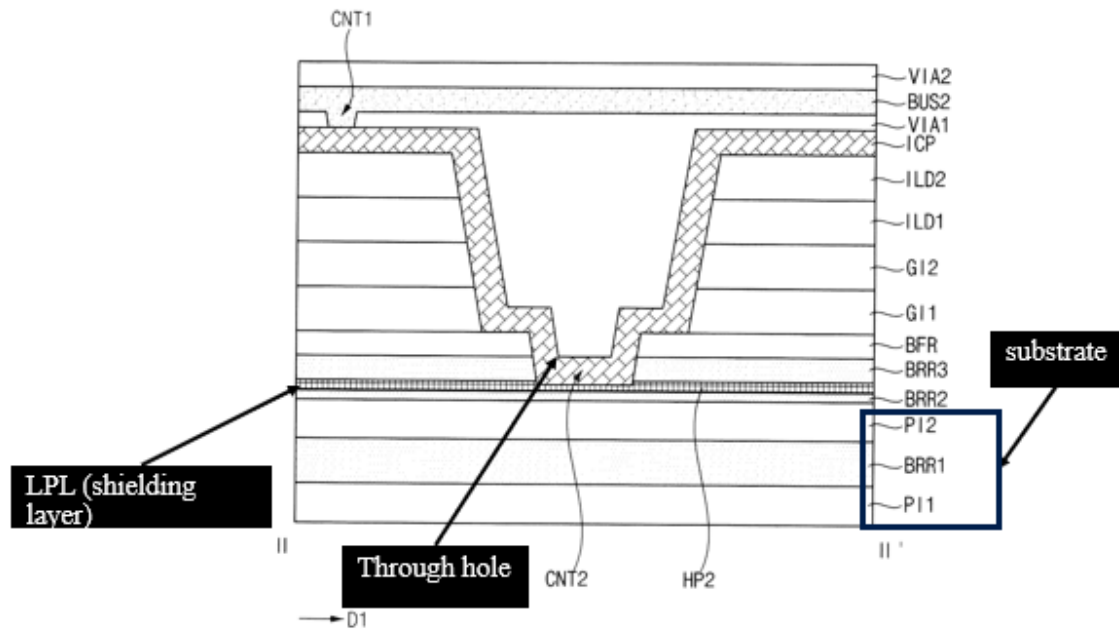


87. Second, Yil teaches that the plurality of power supply lines are electrically connected to the converging wire through a plurality of through holes. Figure 23 illustrates HP2 (the second horizontal pattern), and power supply lines (1720) are electrically connected to HP2 through through holes (CNT2). Ex-1005, 20:55–59.



88. Figure 24 provides a cross-sectional view along the line II-II' in Figure 23, illustrating the vias as etched into the layers:

FIG. 24

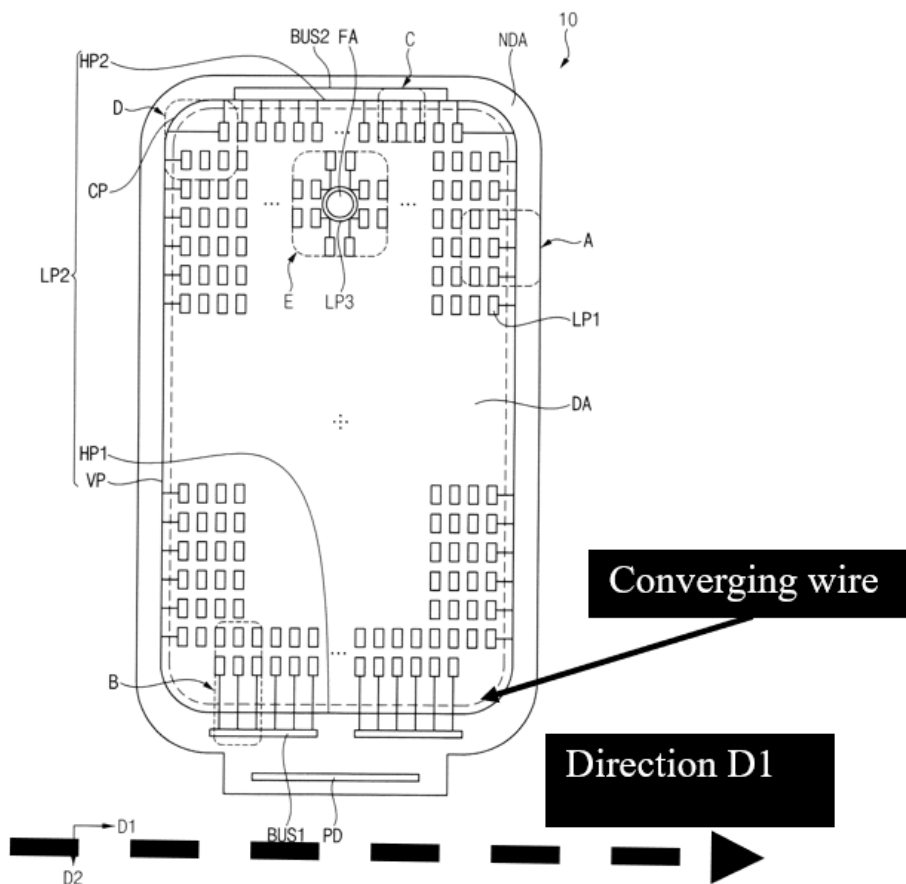


89. Y11, describing Figure 24, explains that the second horizontal pattern HP2 may contact an intermediate connection pattern ICP through a second contact hole CNT2,” which in turn contacts BUS2. Ex-1005, 20:55–59. Accordingly, Figure 24 shows that the shielding layer may include the second horizontal pattern HP2 (Ex-1005 at 20:44-46) and the power voltage lines and the power voltage pattern BUS2 may be unitary. Ex-1005 at 10:15-17. Accordingly, the power supply lines are “disposed on a side of the shielding layer away from the substrate” as they pass through CNT2 on layers above the substrate.

- f. **Element 1[e]: wherein the converging wire between two adjacent ones of the plurality of through holes is disposed according to a shortest distance between the two adjacent through holes.**

90. Yi1 teaches Element 1[e]. Figure 19 illustrates HP1, which extends linearly in one direction (D1). Yi1 notes that HP1 is “disposed at the bottom of the mesh shape and may extend in the first direction D1.” Ex-1005, 19:30–32.

FIG. 19



91. Yi1 illustrates an enlargement of the bottom of Figure 19 in Figure 22. Ex-1005, 20:20-21. HP1 is “disposed at the bottom of the mesh shape and may extend in the first direction D1.” Ex-1005, 19:30–32. As HP1 extends in one linear direction without any loops, kinks, or geometric variations, it is disposed along a straight line according to the shortest distance between adjacent through holes. Yi1 also shows this in Figure 23, annotated below. Figure 23 shows HP2, a second converging wire that runs along the top of the display, running through adjacent through holes linearly. In my opinion, this linear routing is the most obvious and predictable layout for a converging wire, as it minimizes wire resistance, reduces parasitic capacitance, and eliminates unnecessary current path deviations that could create charge accumulation points—precisely the ESD problem the ’429 Patent purports to solve.

FIG. 22

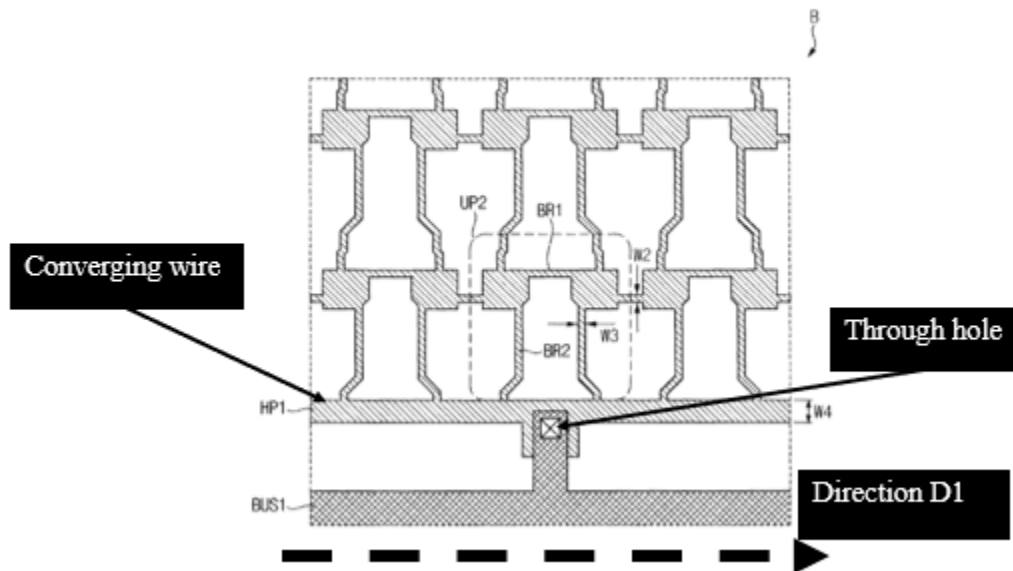
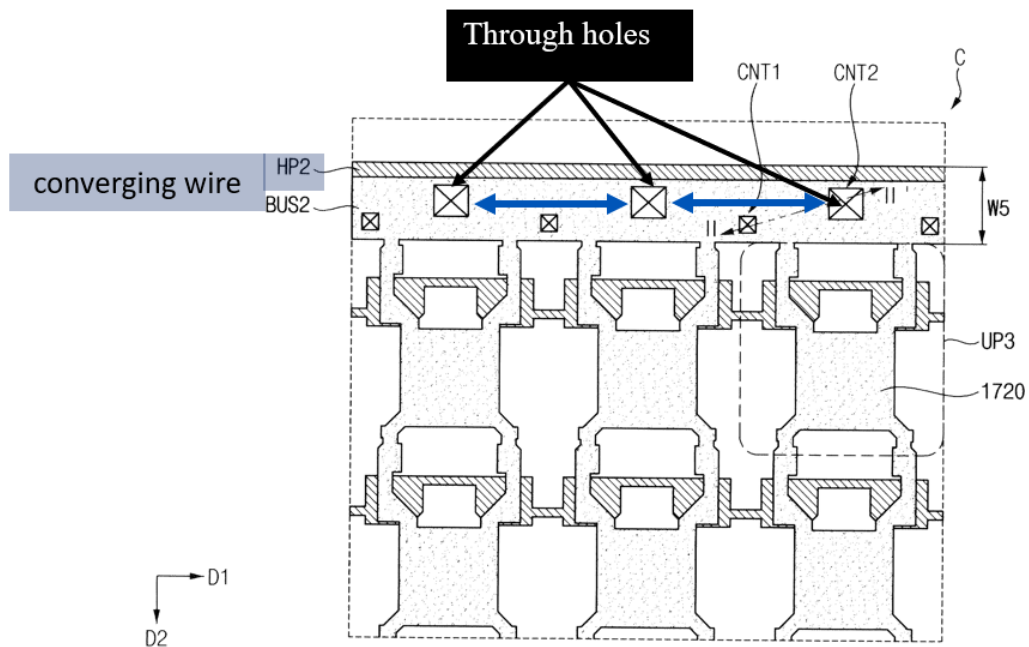


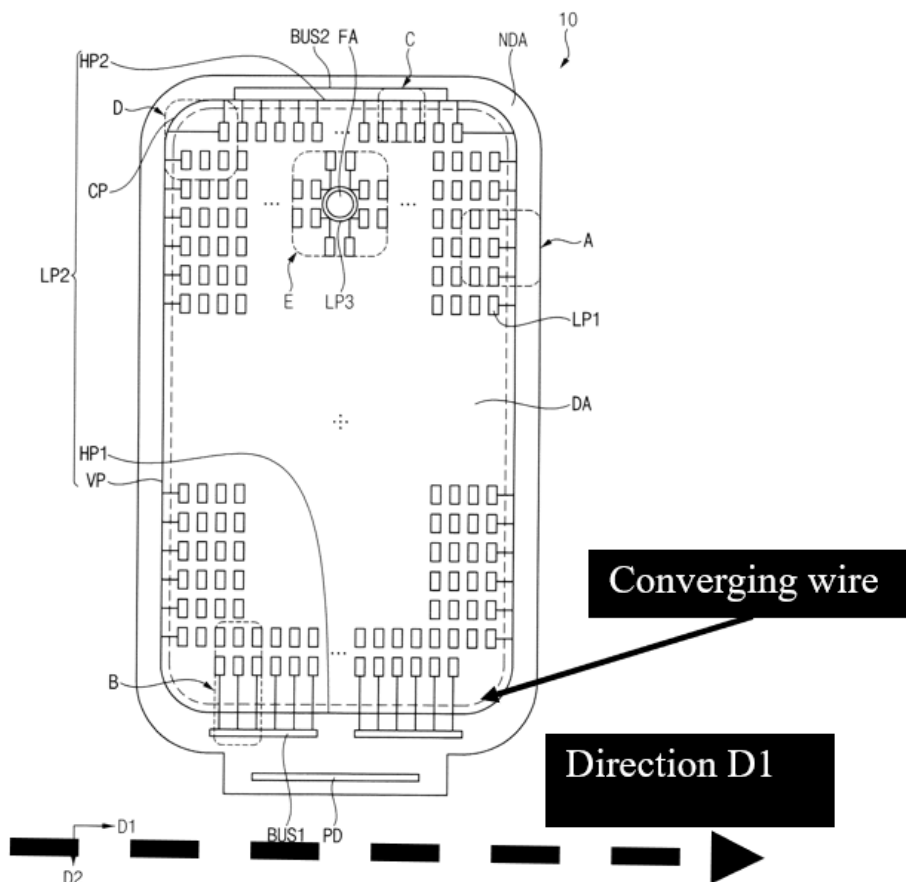
FIG. 23



2. Claim 2: The display panel according to claim 1, wherein the converging wire between the two adjacent through holes is linear in arrangement.

92. Yi1 teaches Claim 2, which requires the converging wire between the two adjacent through holes to be “linear in arrangement.” As described above, HP1 extends linearly in direction D1 through adjacent through holes. Figures 19 and 22 demonstrate this linear relationship.

FIG. 19



93. Specifically, given that Figure 22 is an enlargement of Figure 19, multiple copies of it can be lined up to illustrate the shielding layer and converging wire along the bottom of the device. When aligned, HP1 extends in one linear direction between the two adjacent through holes. This arrangement is similar to the arrangement in Figure 23, wherein HP2 (a second converging wire) runs linearly through two adjacent through holes.

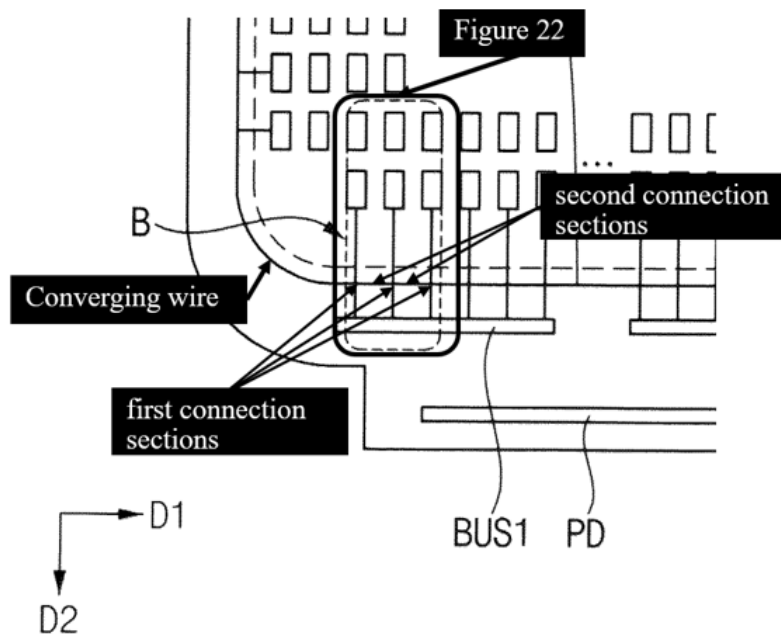


FIG. 22

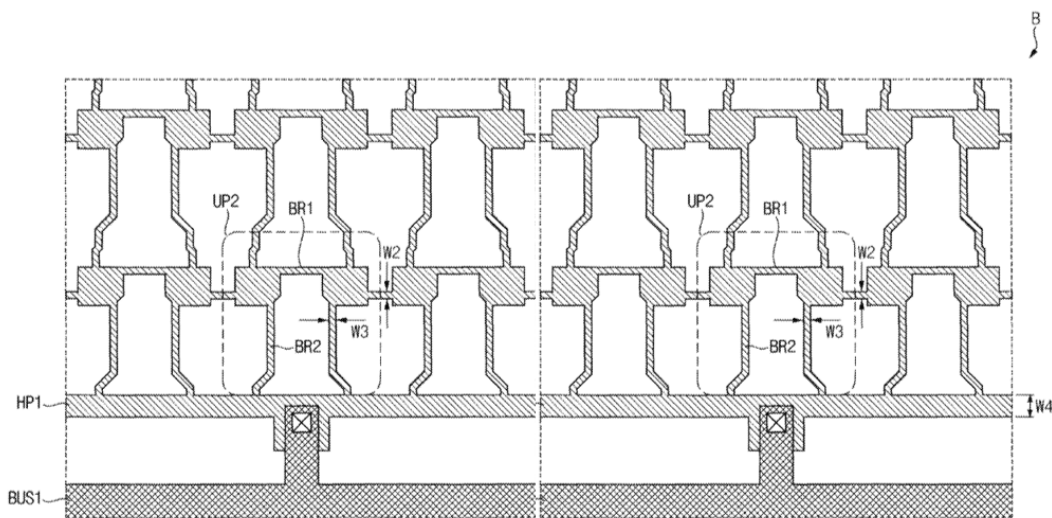
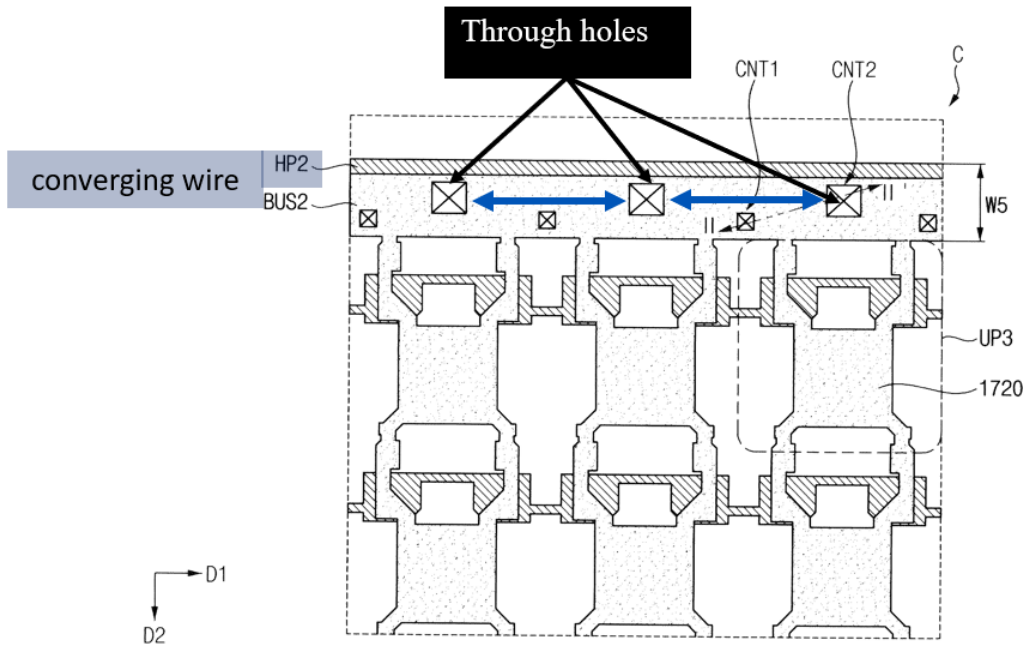


FIG. 23



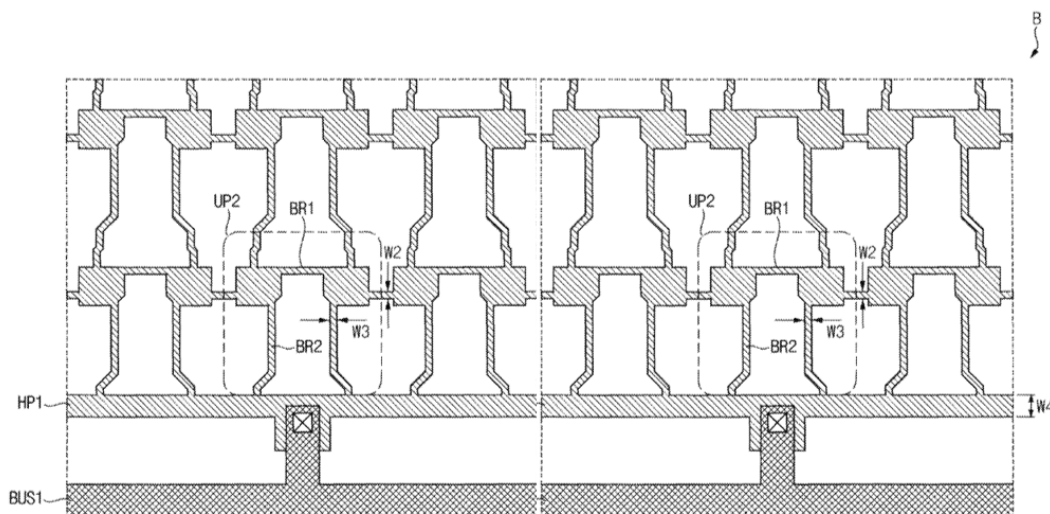
94. Therefore, it is my opinion that Yi1 renders Claim 2 obvious.

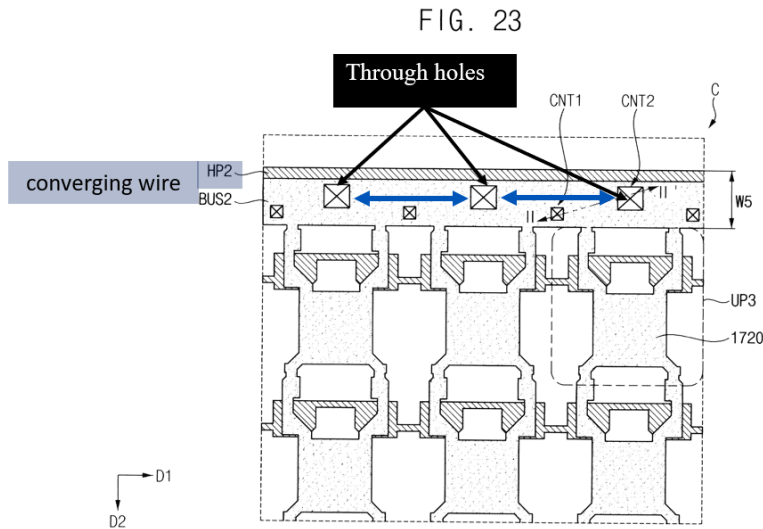
3. Claim 3: The display panel according to claim 2, wherein the converging wire is linear in arrangement and the plurality of through holes overlappingly disposed on the converging wire are linear in arrangement.

95. Yi1 teaches Claim 3, which further requires the converging wire to be “linear in arrangement” and the plurality of through holes overlappingly disposed on the converging wire to be “linear in arrangement.” As shown in Figure 22 when aligned in series, both the converging wire HP1 and the through holes are disposed linearly along direction D1. Similarly, Figure 24 shows HP2 disposed linearly and with a plurality of through holes overlappingly disposed on the converging wire linearly. A POSA would have recognized that this arrangement would be similar around the display. Accordingly, Yi1 renders Claim 3 obvious.

FIG. 22

FIG. 22





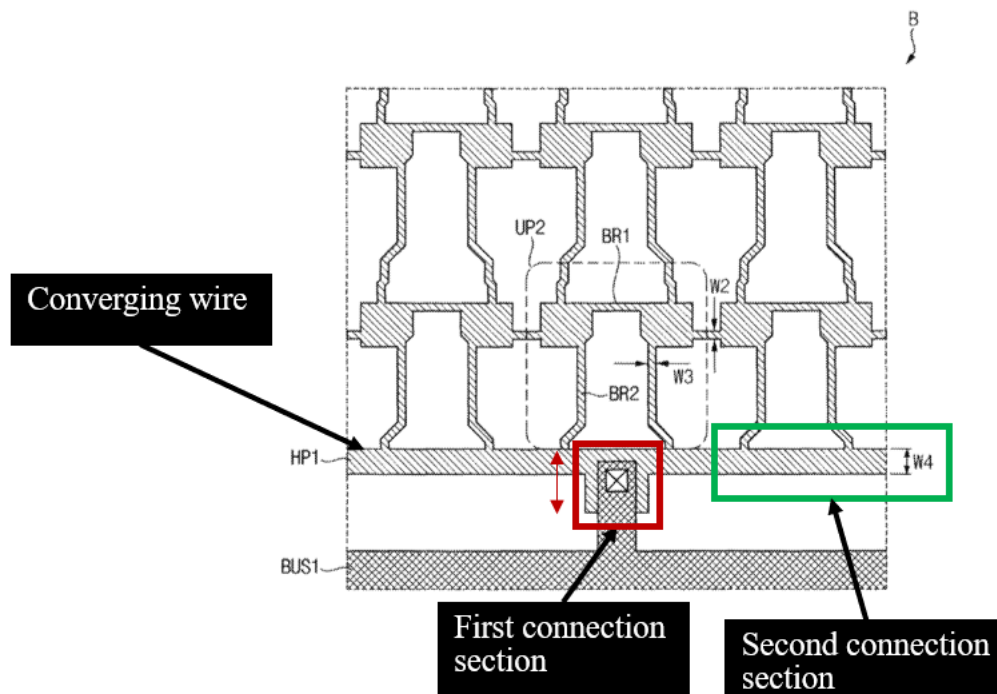
4. **Claim 4:** The display panel according to claim 1, wherein the converging wire comprises a first converging wire, and the first converging wire comprises a plurality of first connection sections and a plurality of second connection sections; wherein each of the plurality of second connection sections is connected between a middle portion of two adjacent first plurality of connection sections, a width of each of the plurality of first connection sections is greater than a width of each of the plurality of second connection sections, and the plurality of power supply lines are electrically connected to the plurality of first connection sections through the plurality of through holes.

96. Yi1 teaches Claim 4.

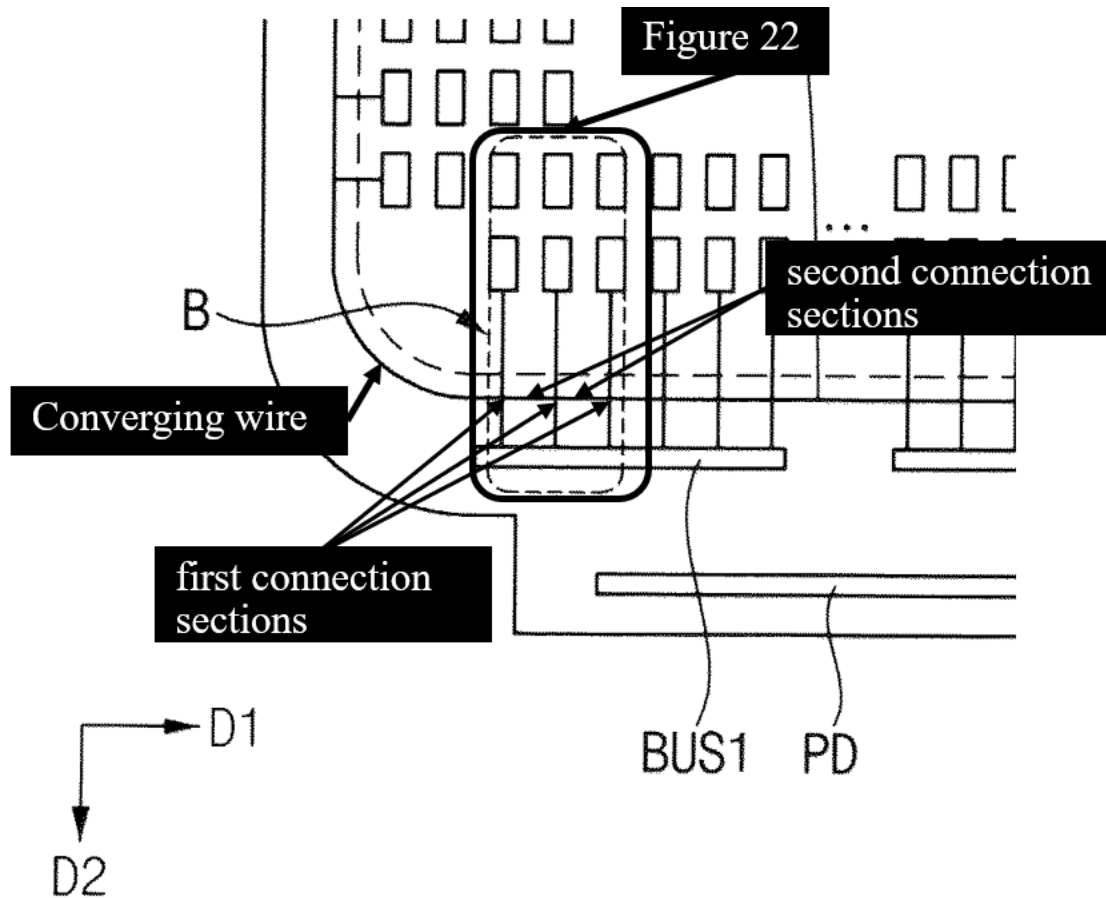
Claim 4, in plain terms, requires the converging wire to include a plurality of “first connections sections,” each of which are wider than a plurality of “second connection sections.” The power supply lines connect to the converging wire through the first connection sections. The second connection sections are disposed between two adjacent first connection sections.

97. Yi1's HP1 is a first converging wire, as I describe above in Section [[Claim 1[b]]]. HP1 comprises first connection sections (where HP1 connects to BUS1 through through holes) and second connection sections (where HP1 connects to the unit patterns UP). Ex-1005 at 20:24–37. Figure 22 shows the first connection sections (marked in a red box, width shown with arrow) and second connections (marked in a green box). In the first connection section, HP1 is “connected to the power voltage bus BUS1, and the power voltage ELVDD” is provided to HP1. Ex-1005, 20:34-37. Shown in the second connection section, HP1 is connected to the “unit- patterns UP2 disposed at the bottom of the mesh shape among the unit patterns UP.” Ex-1005, 20:24-26.

FIG. 22



98. Yi1 also teaches that the plurality of second connection sections is between a middle portion of two adjacent connection sections. Figure 19 (from which Figure 22 is derived) illustrates the relationship between the second connections and the first connection sections.



99. Yi1 also teaches that a “width of each of the plurality of first connection sections is greater than a width of each of the plurality of second connection sections.” Figure 22 shows several widths: W3 is the width of the bridges between the shielding blocks and HP2, and W4 (in the green box) is the width of HP1 (converging wire). Yi1 states that the “fourth width W4” greater than W2 and W3.

FIG. 22

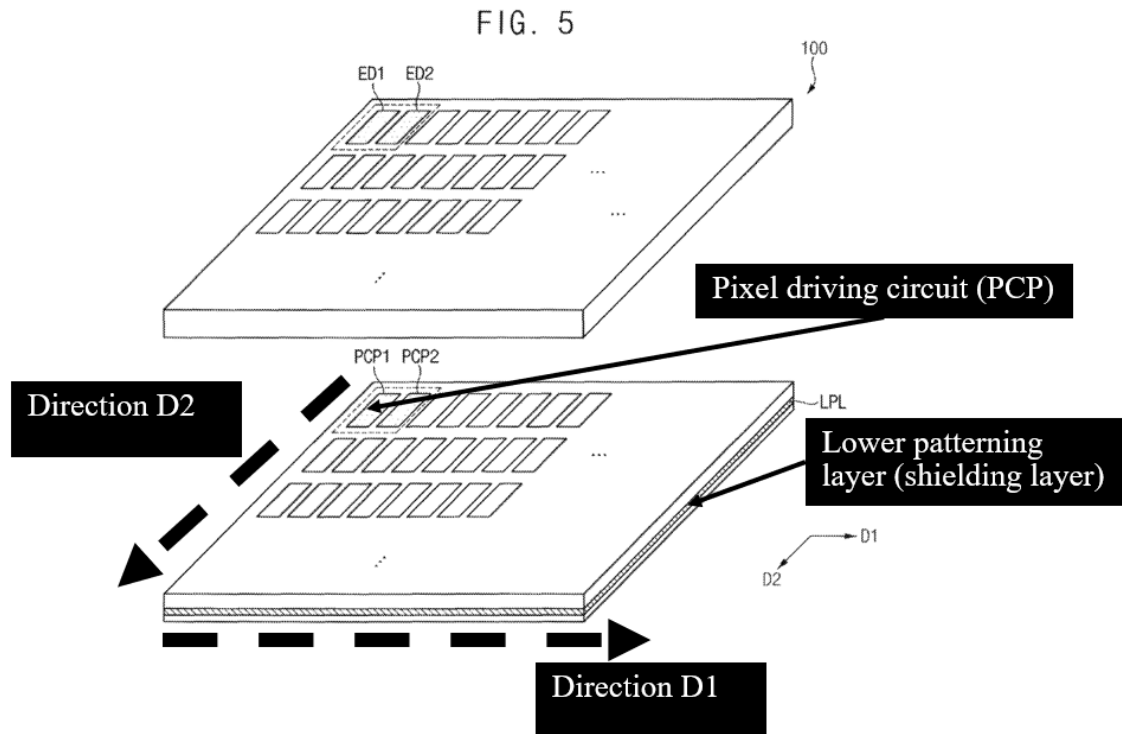


100. Therefore, it is my opinion that Yi1 renders Claim 4 obvious.

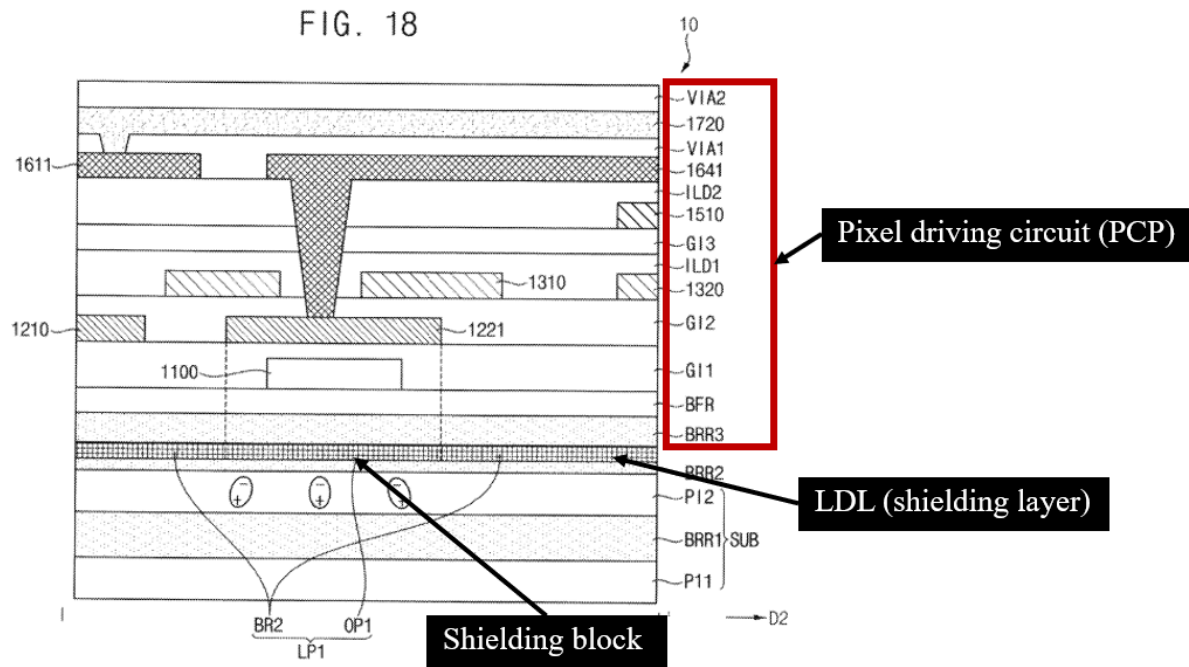
- 5. Claim 5: The display panel according to claim 4, wherein the plurality of pixel driving circuits are arranged in an array in a first direction and a second direction, each of the plurality of first connection sections is electrically connected to the plurality of shielding blocks corresponding to a column of the plurality of pixel driving circuits arranged along a first direction**

101. Yi1 teaches Claim 5.

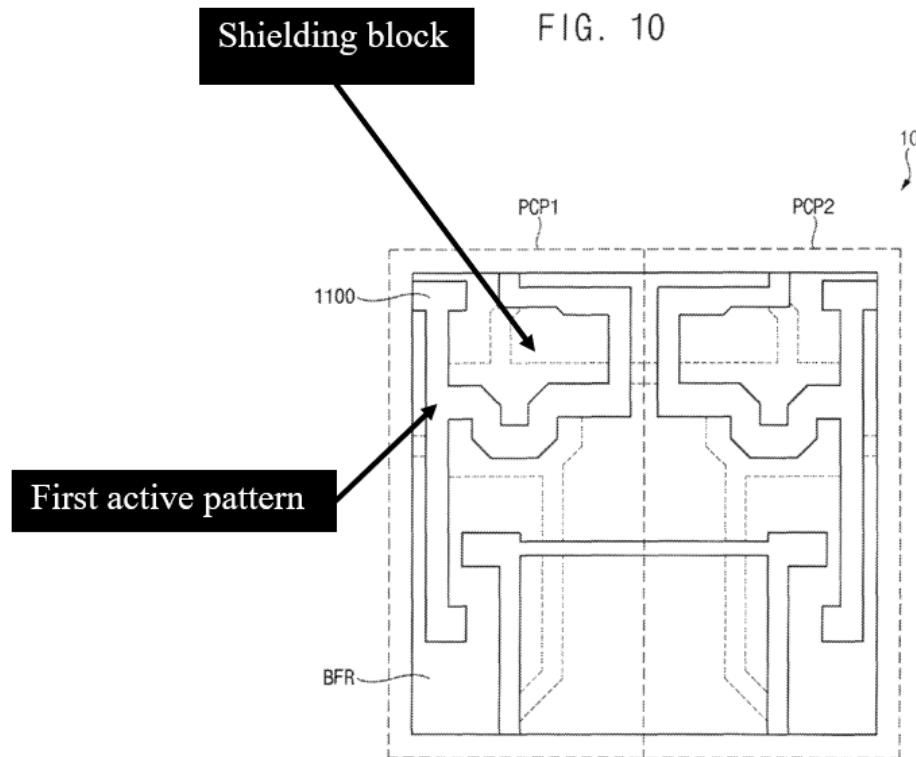
102. Yi1 teaches pixel driving circuits arranged in an array in directions D1 and D2 (Figure 5). Ex-1005, 10:22–33. Figure 5 is a “perspective view illustrating a display panel,” showcasing the pixel circuit parts that correspond to pixel circuits. Ex-1005, 10:22–33. These pixel circuits are arranged in a grid along D1 and D2, the two directions shown in the lower right hand corner of the figure.



103. Each first connection section is electrically connected to the shielding blocks corresponding to a column of pixel driving circuits along D1. Figures 10 and 18 confirm this columnar correspondence. Figure 18 shows a side view that demonstrates the full stack of layers, including the LDL (made up of the claimed shielding blocks) and the pixel driving circuit.

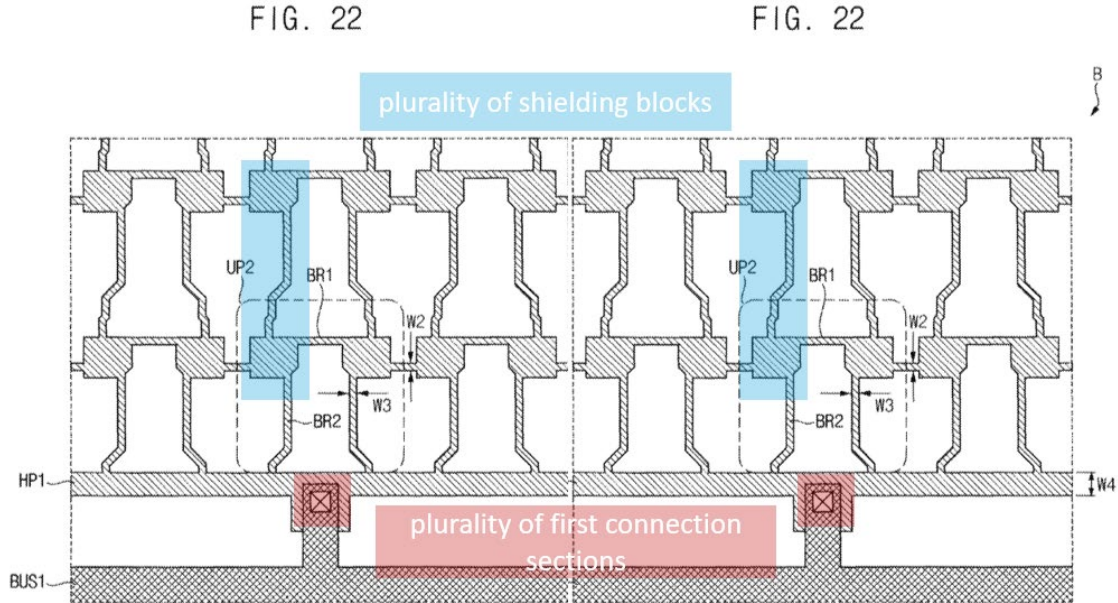


104. Figure 10 shows the overlap between a shielding block and a pixel circuit part, confirming that the shielding blocks correspond to pixel driving circuit layers.



105. Considering Figures 5 and 10 together, PCP1 and PCP2 are electrically connected in a column oriented along direction D1.

106. The repeated Figure 22 also illustrates that the plurality of first connection sections are electrically connected to the plurality of shielding blocks. As shown below, HP1 electrically connects the shielding blocks to the first connections sections.



107. Accordingly, Yi1 renders Claim 5 obvious.

6. Claim 9

a. 9[pre]: The display panel according to claim 1, wherein the pixel driving circuit layer comprises:

108. Yi1 teaches this element.

109. Yi1 teaches a pixel driving circuit layer (the PCP) located on the shielding layer (the LPL). Figures 4 and 18 illustrate the layer stack of the pixel driving circuit layer, which illustrates each of the layers recited in claim elements 9[a]-9[g].

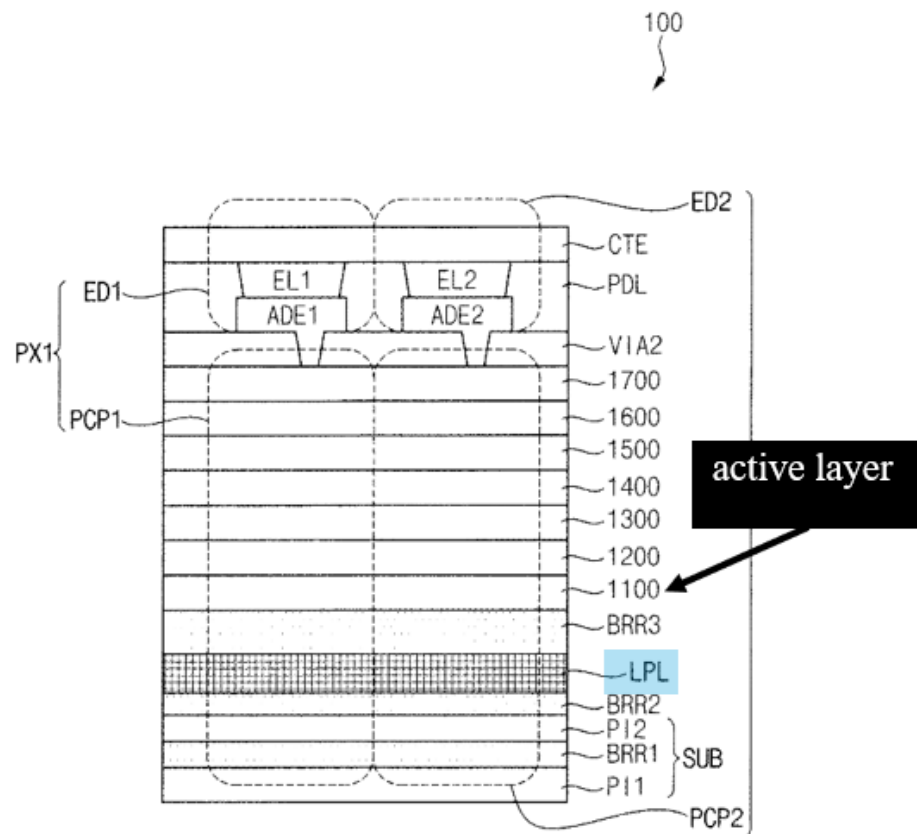
b. 9[a]: a semiconductor layer disposed on a side of the shielding layer away from the substrate;

110. In my opinion, Yi1 teaches this element.

111. Yi1's first active pattern 1100 is a semiconductor layer disposed on a side of the shielding layer (the LPL) away from the substrate: the first active pattern 1100

is disposed on the buffer layer BFR, which is disposed on the third barrier layer BRR3 covering the LPL, and the first active pattern 1100 “may include a silicon semiconductor.” Ex-1005, 12:65-13:12.

FIG. 4



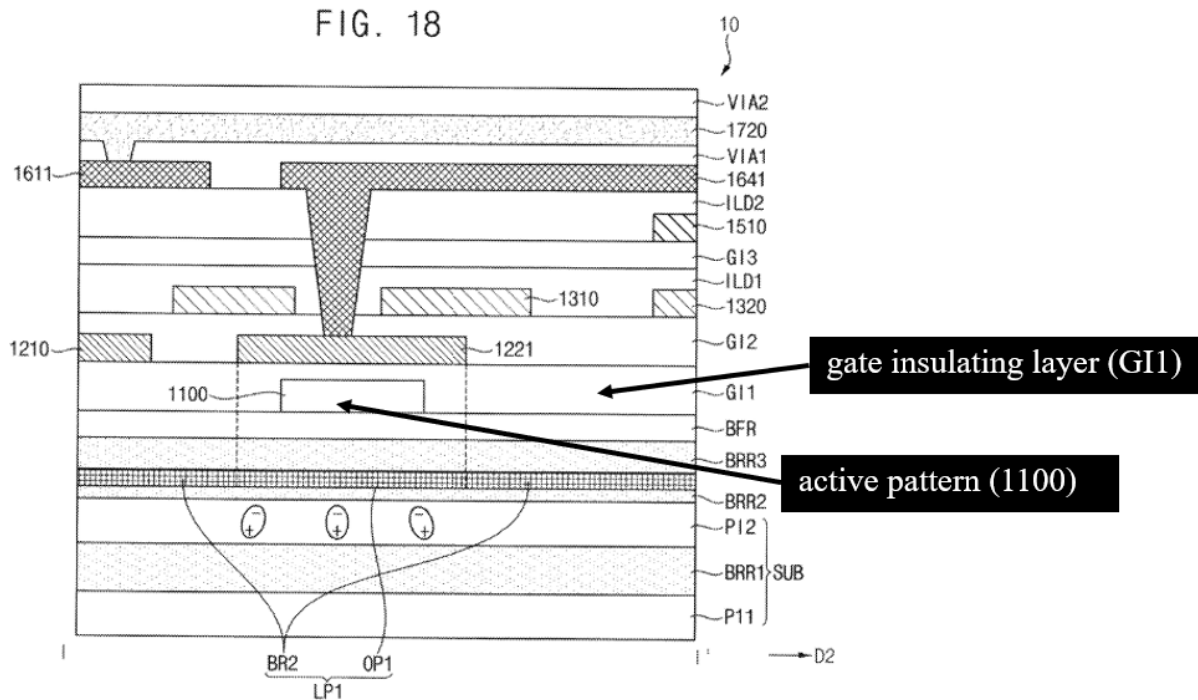
- c. **9[b]: a first insulating layer disposed on a side of the semiconductor layer away from the substrate;**

112. In my opinion, Yi1 teaches this claim element.

113. Yi1's PCP includes a first gate insulating (GI1) disposed on a side of the semiconductor layer away from the substrate. This first gate insulating layer “may

cover the first active pattern 1100 and may be disposed on the buffer layer BFR.”

Ex-1005, 13:13–23. Figure 18 shows both insulating and active layers in a cross section of a PCP, and shows the gate insulating layer atop the active pattern.



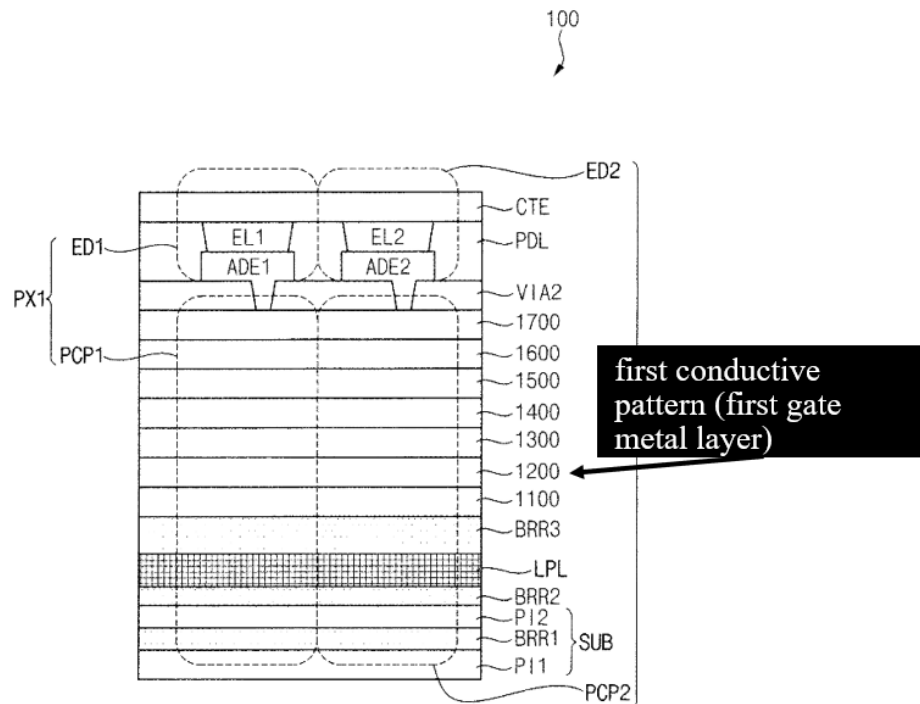
- d. **9[c]: a first gate metal layer disposed on a side of the first insulating layer away from the substrate;**

114. In my opinion, Yi1 teaches this limitation.

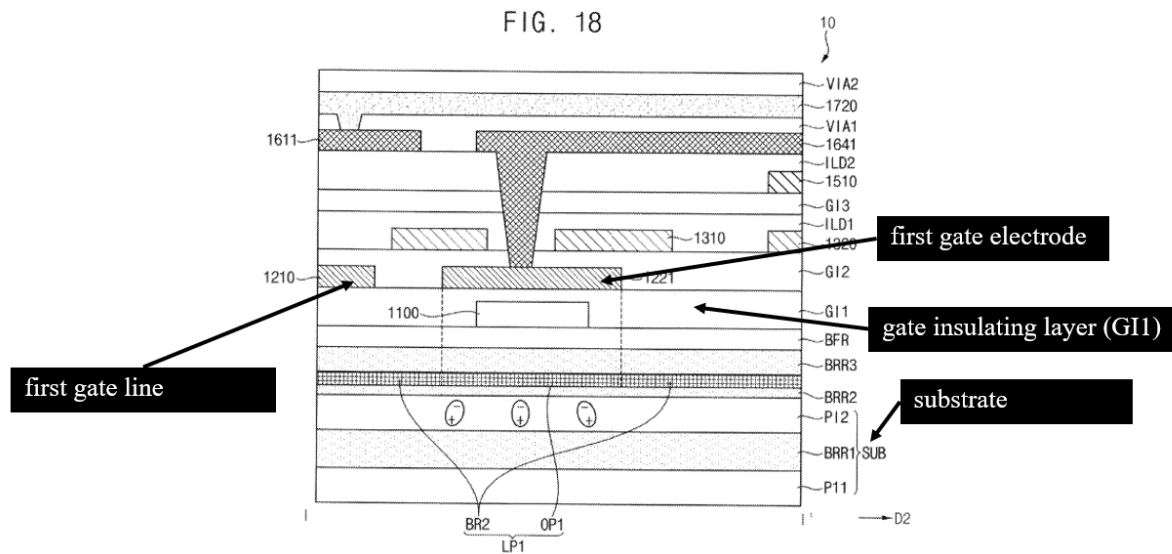
115. Yi1’s PCP includes a first conductive pattern 1200, which is a first gate metal layer disposed on a side of the first insulating layer (GI1) away from the substrate. It includes the first gate line 1210, the first and second gate electrodes 1221 and

1222, and the fourth gate line 1230. Ex-1005, 13:28–54. Yil's Figure 4 shows the first conductive pattern in the context of the stack up.

FIG. 4



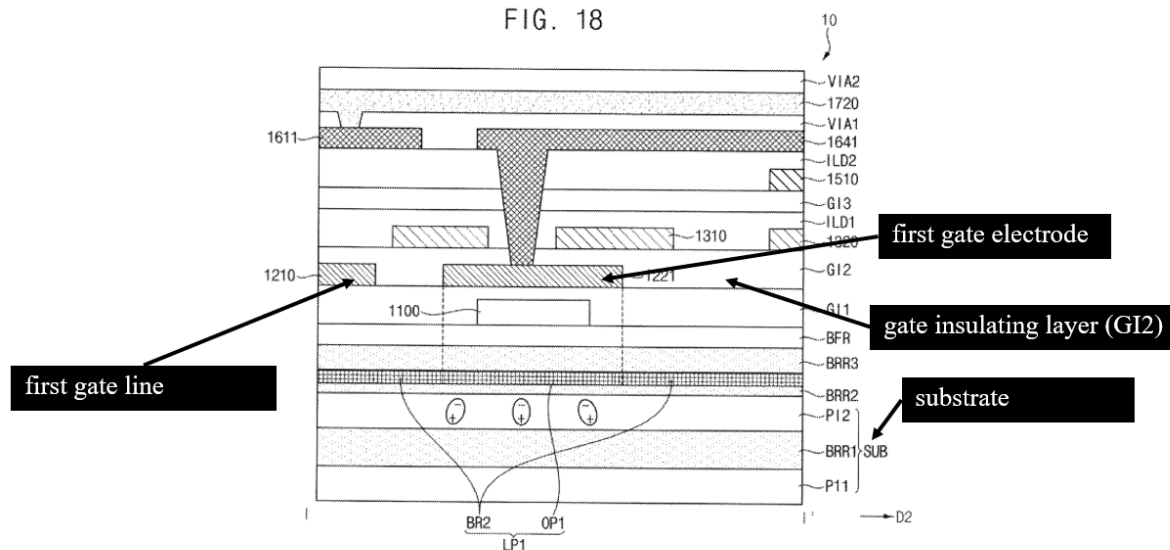
116. Figure 18, which shows both active layers and insulating layers, shows the constituent parts that comprise the first conductive pattern: the first gate line (1210) and the first gate electrode (1221).



- e. **9[d]: a second insulating layer disposed on a side of the first gate metal layer away from the substrate;**

117. In my opinion, Yi1 teaches this element.

118. The PCP includes a second gate insulating layer (GI2), which “may cover the first conductive pattern 1200 and may be disposed on the first gate insulating layer GI1.” Ex-1005, 14:8–10. Figure 18, which shows the insulating layers, shows GI2 disposed on the first gate metal layer (1210 and 1221, the constituent parts of 1200) on the side away from the substrate.

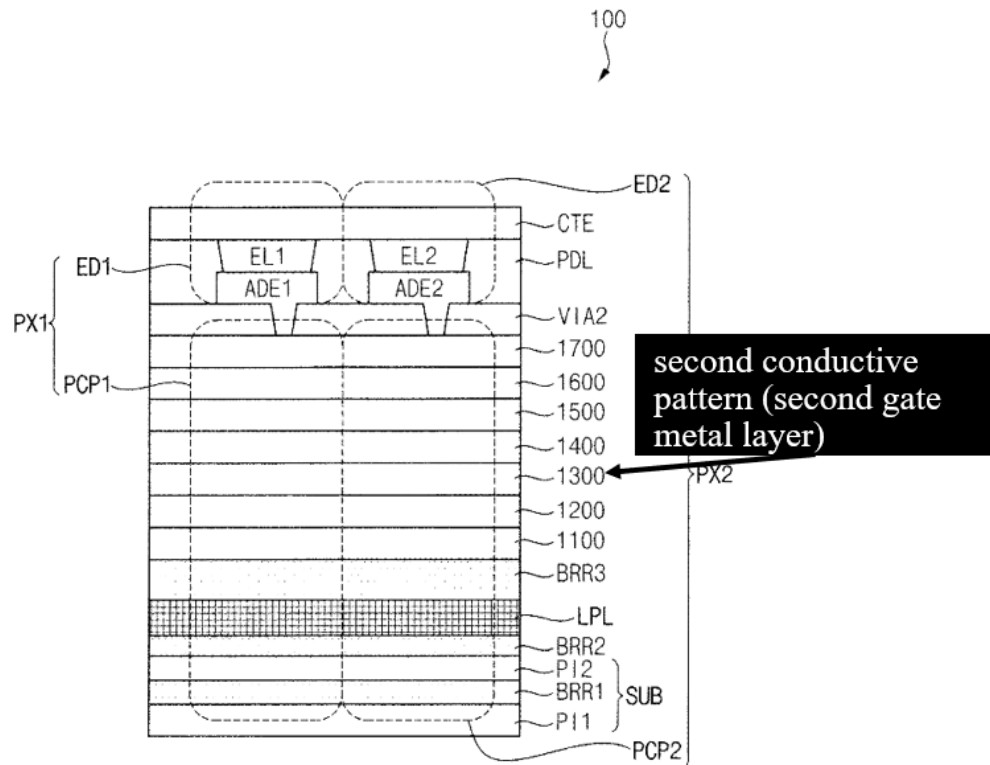


- f. 9[e]: a second gate metal layer disposed on a side of the second insulating layer away from the substrate; and

119. In my opinion, Yi1 teaches this limitation.

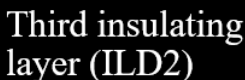
120. Yi1's second conductive pattern 1300 is a second gate metal layer that "may be disposed on the second gate insulating layer GI2." Ex-1005, 14:23–39. The layer comprises a storage capacitor electrode 1310, which constitutes the storage capacitor CST together with the first gate electrode 1221. *Id.* Figure 4 shows the second conductive pattern (layer 1300) in the overall stack.

FIG. 4



121. Figure 18 illustrates the storage capacitor electrode (1310), part of the second gate metal layer 1300, disposed on a side of GI2 away from the substrate.

FIG. 18

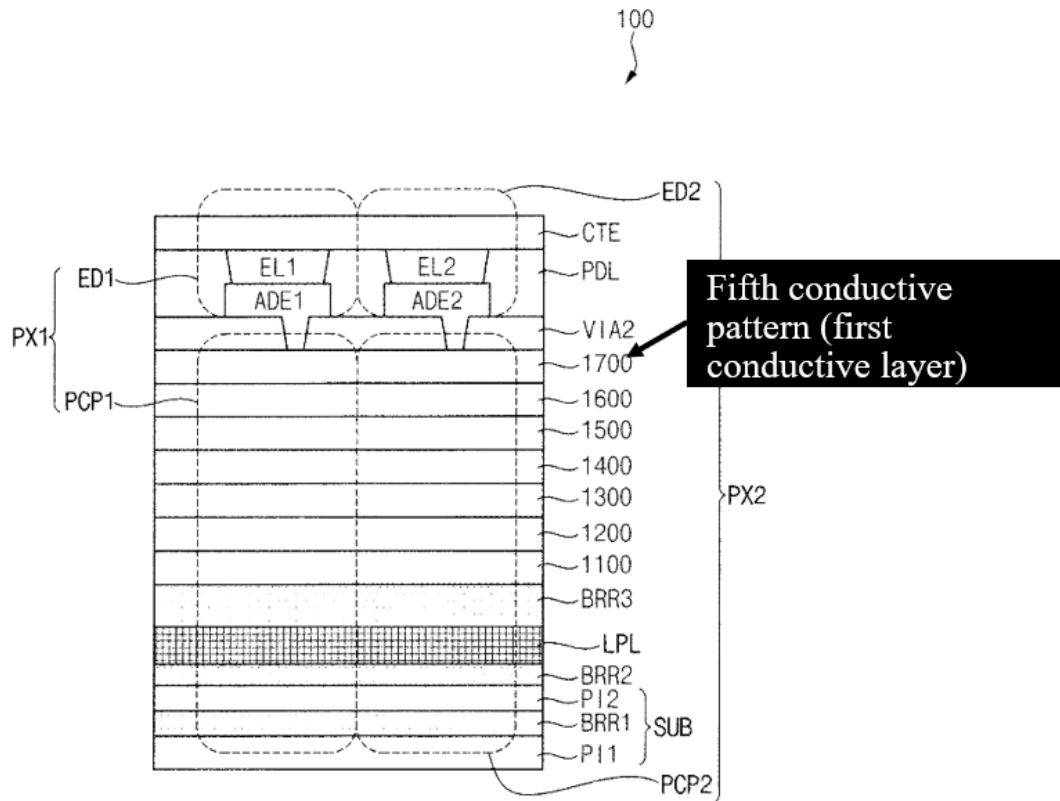


- h. 9[g]: wherein the first conductive layer is disposed on a side of the third insulating layer away from the substrate, the plurality of power supply lines of the first conductive layer are electrically connected to the converging wire through the plurality of through holes, and the plurality of through holes penetrate through the first insulating layer, the second insulating layer, and the third insulating layer.**

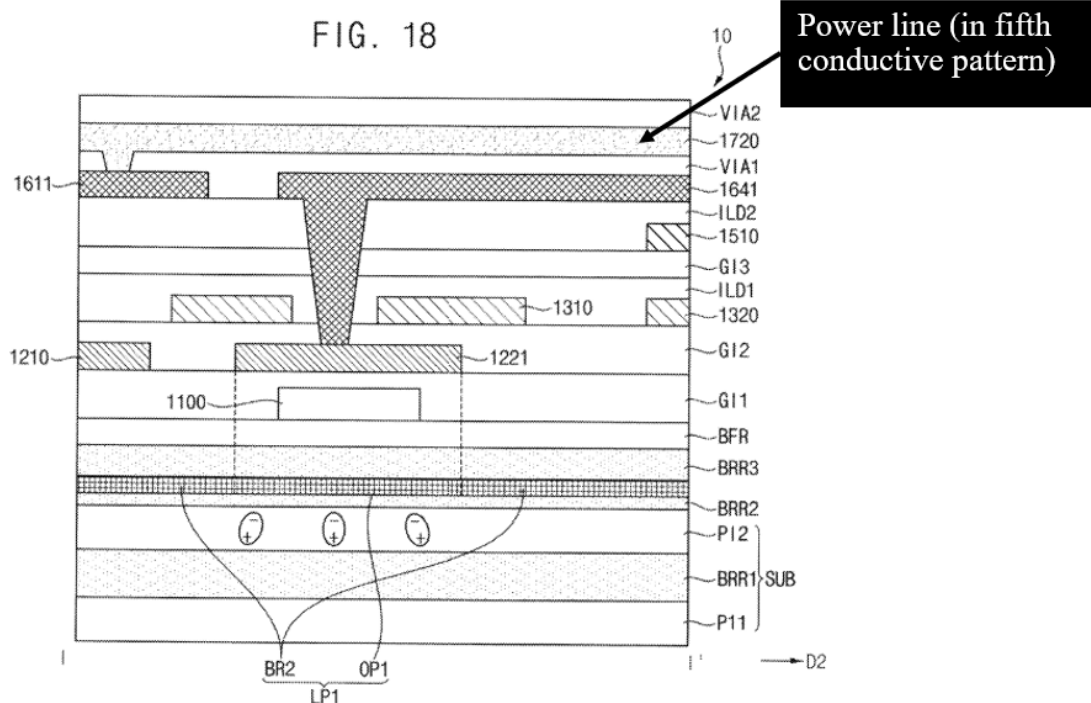
124. In my opinion, Yil teaches this element.

125. Yi1's PCP includes what it terms the "fifth conductive pattern," which is a "first conductive layer" as claimed. The fifth conductive pattern includes the power voltage lines 1720, which "provide the power voltage ELVDD." Ex-1005, 17:29–48. It is disposed on a side of the first insulating layer ILD2 away from the substrate. Figure 4 shows layer 1700 in the stackup.

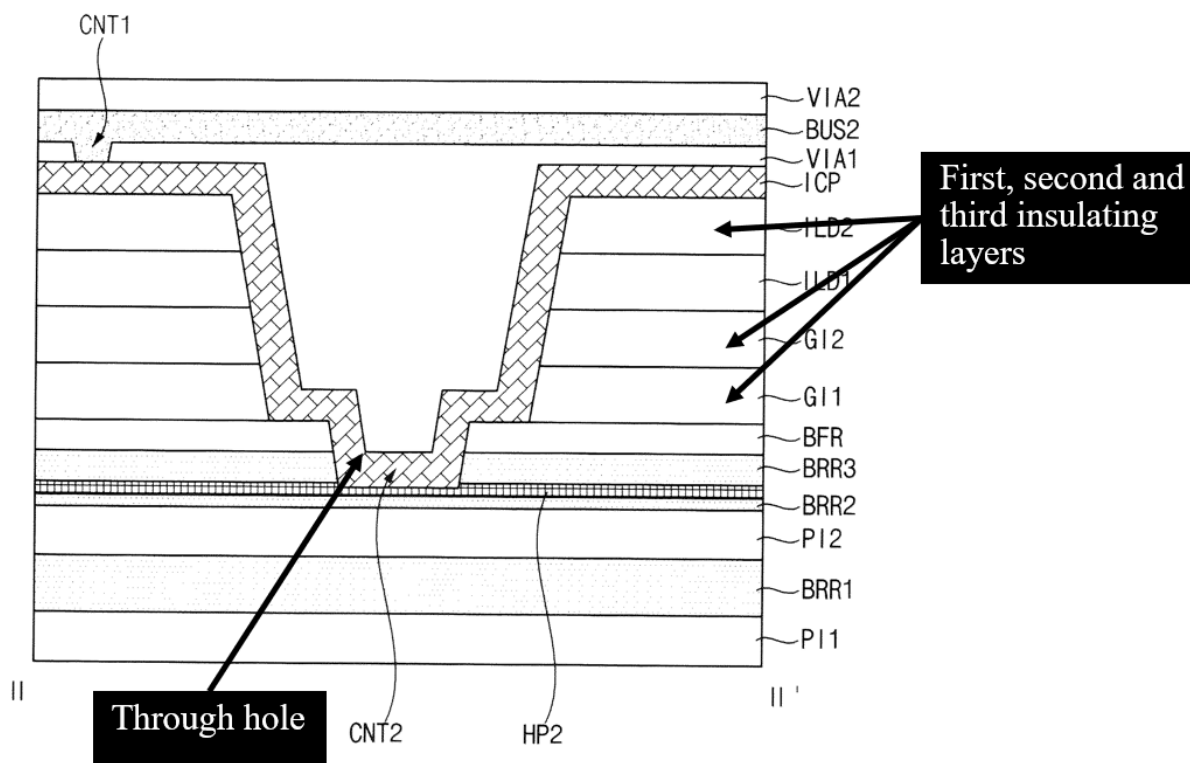
FIG. 4



126. Figure 18 shows the power lines 1720 disposed along the third insulating layer (ILD2) on a side away from the substrate.



127. Furthermore, Y11 teaches that the plurality of power supply lines of the first conductive layer are electrically connected to the converging wire (HP2) through a plurality of through holes (CNT2) (as described above in Claim 1[d]). CNT2 “penetrate[s] the third barrier layer BRR3, the buffer layer BFR, the first gate insulating layer GI1, and the second gate insulating layer GI2, the first inter-insulating layer ILD1, the third gate insulating layer GI3, and the second inter-insulating layer ILD2.” Ex-1005, 20:55–21:10. Therefore, CNT2 penetrates the first (GI1), second (GI2) and third (ILD2) insulating layers. This is demonstrated in Figure 24, which shows a cross section of CNT2 in the various layers.



128. Therefore, it is my opinion that Yi1 renders Claim 9 obvious.

7. Claim 11: A display device comprising the display panel as claimed in claim 1, wherein the display panel is an organic light-emitting diode (OLED) panel.

129. Yi1 teaches Claim 11. Yi1 teaches that “the first emitting diode ED1 may correspond to the first organic light emitting diode OLED1.” Ex-1005, 10:28–36. The display panel is therefore an OLED panel.

8. Claims 12–15

130. Claims 12–15 are device claims depending from Claim 11 that mirror Claims 2–5. For the same reasons discussed above, Yi1 renders Claims 12–15 obvious.

B. Ground 2: Claims 7–8 and 17–18 Are Rendered Obvious by Yi1 in View of Yi2

1. Motivation to Combine Yi1 and Yi2

131. A POSITA would have been motivated to combine Yi1 and Yi2. Yi1 and Yi2 are commonly assigned Samsung Display patent documents sharing inventor Changho Yi, filed one week apart, disclosing nearly identical lower-pattern/shielding architectures.

132. Yi2 expressly discloses a bending area: “A fan-out line FL may be disposed in the bending area BA, and the bending area BA may be bent.” Ex-1006, ¶53, Fig. 1. Incorporating Yi2’s bending area into Yi1 is the simple combination of familiar elements yielding predictable results, as flexible OLED panels with bent non-display regions were conventional by 2022. By the early 2000s, flexible OLED displays were already being demonstrated on polymer substrates, and the industry recognized that the very thin, all-solid-state structure of OLEDs made them ideal systems for flexible display devices because all the display components are thin solid films that can be assembled on a single thin substrate. *See* Ex-1011 at 489; Ex-1009 at 235. In particular, bending a portion of the non-display region to fold circuitry underneath the active display was a well-known approach to achieving thinner bezels in smartphones. The OLED’s Lambertian (wide-angle) emission, solid-state construction with no cell gap, and the absence of a separate backlight all make it especially well suited for bending configurations that would be problematic for LCD

technology, which relies on a constant cell gap and backlight. *See* Ex-1011 at 507.

A POSITA would have had a reasonable expectation of success given the common architecture, assignee, and base technology.

2. Claim 7

133. In my opinion, the combination of Yi1 and Yi2 renders Claim 7 obvious.

- a. **7[a]: The display panel according to claim 1, wherein the non-display region comprises: a first non-display region and a second non-display region disposed on two sides of the display region, wherein the first non-display region comprises a bending sub-region, and the display panel bends at the bending sub-region; and**

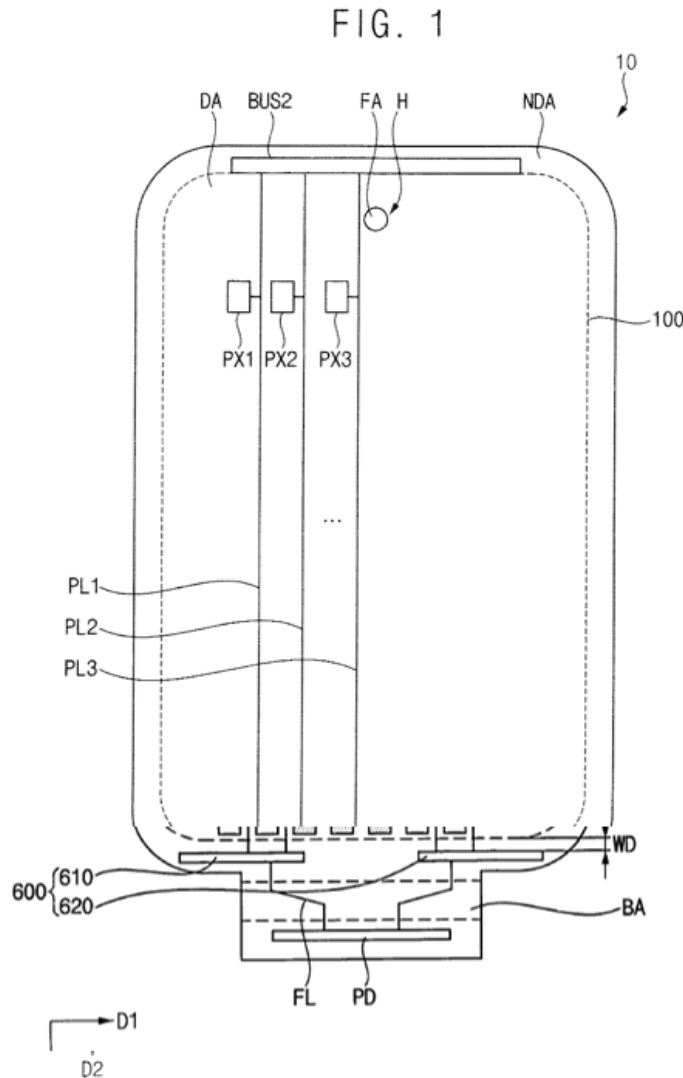
134. In my opinion, the combination of Yi1 and Yi2 teach this claim element.

135. Claim 7[a] requires a first non-display region on one side of the display region, and a second non-display region on a second side of the display region. Within the first non-display region, there must be a “bending sub-region” where the display panel bends.

136. As shown in Figure 1' below, the display panels of Yi1 and Yi2 can be combined to arrive at such a device. Yi2's display device includes a “fan-out line FL may be disposed in the bending area BA, and the bending area BA may be bent.”

Ex-1006, ¶53, Fig. 1. The second non-display region is disposed on another side of the display region: as shown in Yi1's Figures 1 and 19, the power voltage bus BUS1 is disposed in a bottom side of the non-display area NDA, while the power voltage pattern BUS2 is disposed in a top side of the non-display area NDA, on the opposite

side of the display area. Ex-1005, 9:58–66, 20:22–42, Figs. 1, 19. The combined figure below shows the combined device.



- b. 7[b]: the converging wire comprises a first converging wire arranged in the first non-display region, and the plurality of power supply lines are electrically connected to the plurality of first connection sections at least through the plurality of through holes.**

137. In my opinion, the combination of Yi1 and Yi2 teaches this element.

138. As detailed in my analysis of Claim 1[d], Yi1's second horizontal pattern HP2 contacts the intermediate connection pattern ICP through the second contact hole CNT2, and the ICP in turn contacts the power voltage pattern BUS2—provided together with the power voltage line 1720—through the first contact hole CNT1. Ex-1005, 20:55–21:10, Figs. 23, 24.

139. Yi2's transfer pattern 700 (including the first pattern 710 and the second pattern 720) directly contacts the second lower pattern LP2 through the contact holes CNT1 and CNT2, and the second pattern 720, integrally formed with the power voltage line 1720, contacts the first pattern 710 through the fourth contact hole CNT4. Ex-1006, ¶¶159-160, 170-171.

140. Accordingly, the combined device would include a converging wire in the first non-display region, around the bending sub-region.

3. Claim 8: The display panel according to claim 7, wherein the converging wire comprises a second converging wire arranged in the second non-display region, and the plurality of power supply lines are electrically connected to the plurality of second connection sections through the plurality of through holes.

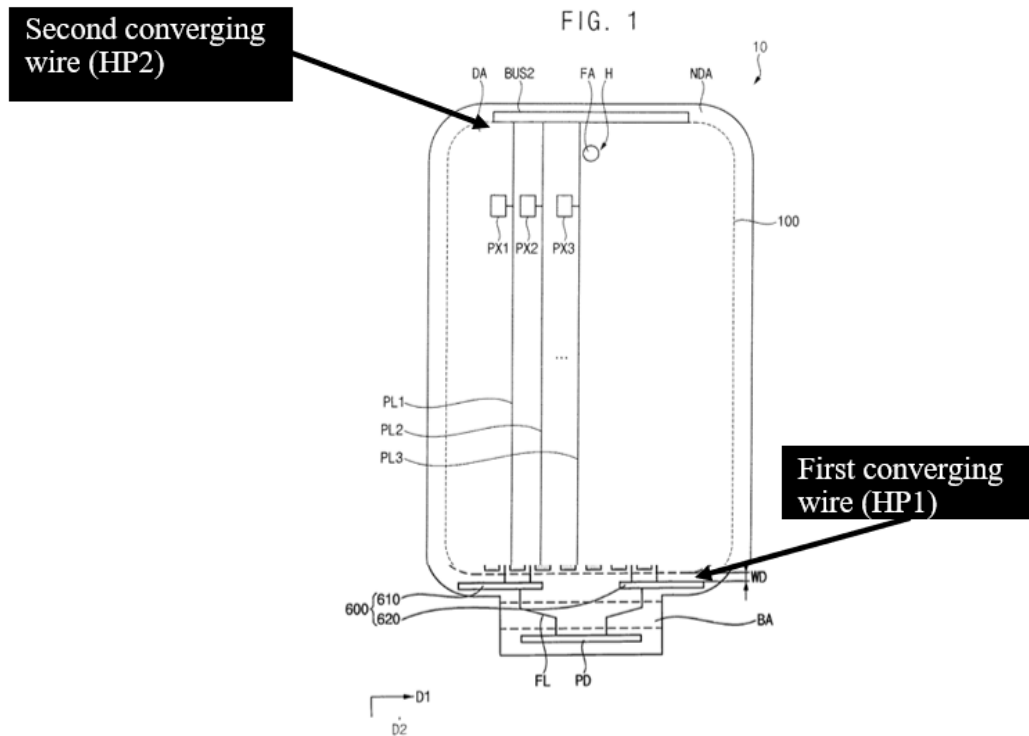
141. Yi1 teaches Claim 8.

142. Yi1 teaches that the converging wire comprises a second converging wire arranged in the second non-display region. As I describe in my analysis of Claim 1[b], Yi1's second lower pattern LP2 includes both the first horizontal pattern HP1 and the second horizontal pattern HP2. LP2 is a part of the lower pattern layer, as it

is “disposed in the lower pattern layer LPL together with the first lower pattern LP1.”

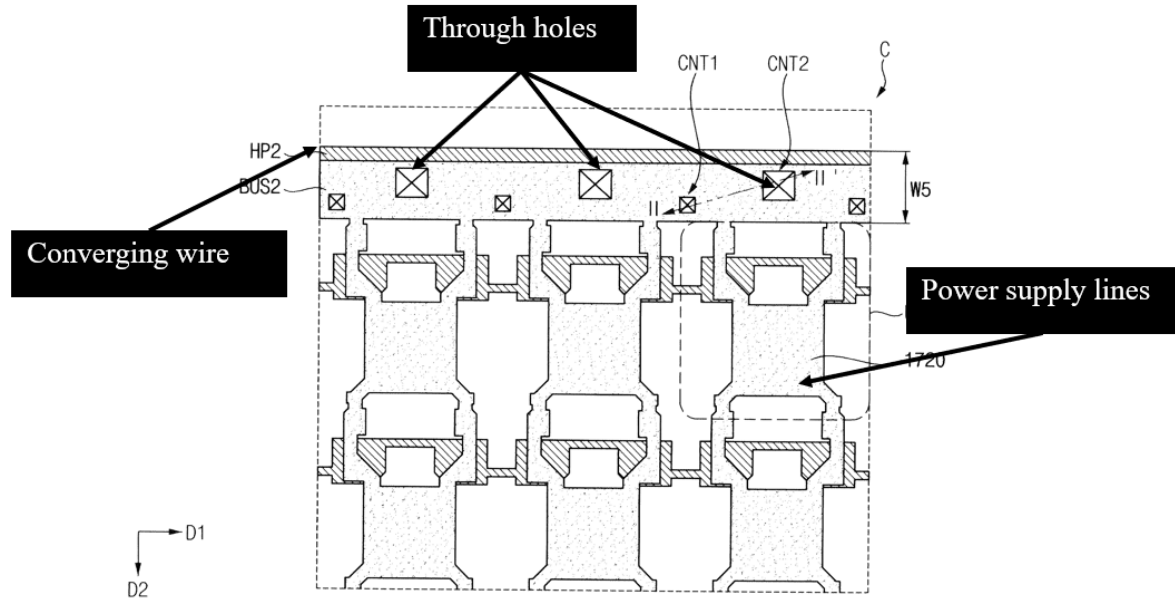
Ex-1005, 19:6-8.

143. HP1 is disposed at the bottom of the mesh shape, extends in the first direction D1, and is connected to the power voltage BUS1. Ex-1005, 20:22–42. HP2 is disposed at the top of the mesh shape and is connected to the power voltage pattern BUS2, which is “disposed in a top side of the non-display area NDA,” while BUS1 is disposed in a bottom side of the non-display area NDA. Ex-1005, 9:58–66. Figure 1’, which shows a device combining the teachings of Yi1 and Yi2, shows HP1 and HP2 (the first and second converging wires, respectively) arranged in the non-display region around the display area. HP2 is therefore a second converging wire arranged in a second non-display region, on the opposite side of the display area from HP1 and BUS1.



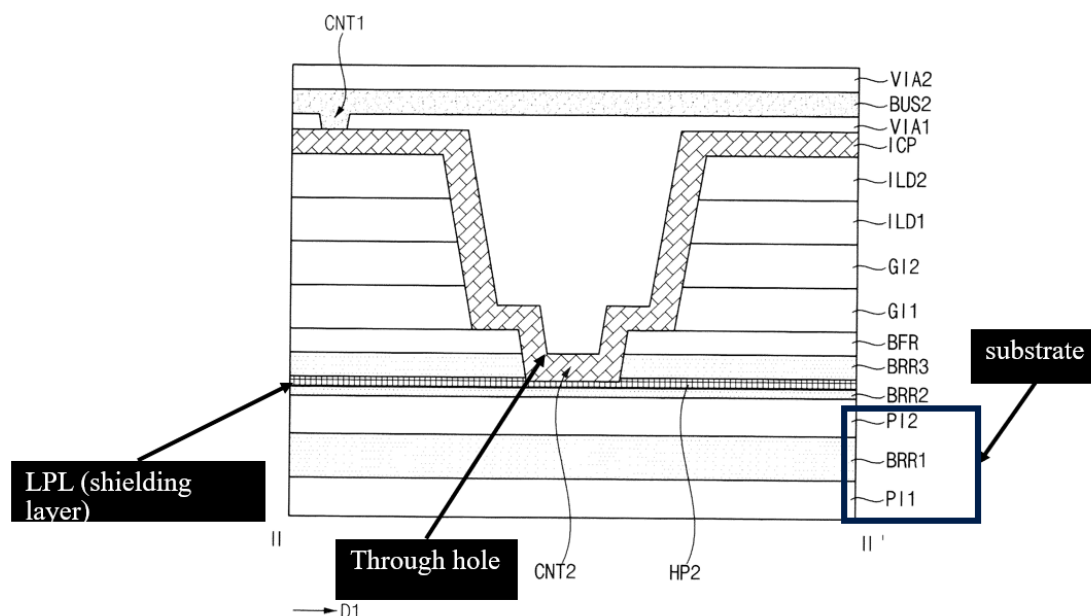
144. Yi1 also teaches that the plurality of power supply lines are electrically connected to the plurality of second connection sections through the plurality of through holes. Figure 23 shows HP2 connected to the power voltage BUS2 through a plurality of through holes (marked with an X).

FIG. 23



145. Figure 24, which is a cross section of the through holes in Figure 23, illustrates that the power lines are electrically connected to the plurality of second connection sections (*i.e.*, in the shielding layer) through the through holes CNT2. The through holes contact the LPL.

FIG. 24



4. Claims 17–18

146. Claims 17–18 are device claims mirroring Claims 7–8. For the same reasons, the combination of Yi1 and Yi2 renders Claims 17–18 obvious.

C. Ground 3: Claims 6 and 16 Are Rendered Obvious by Yi1 in View of Zhang

1. Motivation to Combine Yi1 and Zhang

147. A POSITA would have been motivated to combine Yi1 with Zhang. Both are directed to IC structures with alternating wide and narrow metal portions connected to vias. Zhang teaches arc-shaped wide portions (via landing pads) and linear narrow connecting portions for accommodating large vias while maintaining constant spacing. Ex-1007, 5:7–26, Fig. 1B. Further, both references use silicon as a common

denominator material, and a POSITA would have been aware of how silicon is utilized for via or through hole technology. Zhang describes via fabrication processes using silicon-based materials, including a dielectric block composed of silicon dioxide, a sacrificial layer used in self-aligned via formation that may comprise polysilicon, a low temperature silicon dioxide, or SiN, and silicon used in the transistor substrates. Ex-1007, 6:40-50, 7:15-25, 9:40-55. Yi1 also relies on silicon-based materials. The first active pattern includes a silicon semiconductor, the LPL may comprise a silicon semiconductor, and the barrier and gate insulating layers include silicon oxide, silicon nitride, and silicon oxy-nitride. Ex-1005, 12:55-65, 14:1-20. Both references confirm silicon-based via technology is a fundamental enabler of multi-layer electronic architectures.

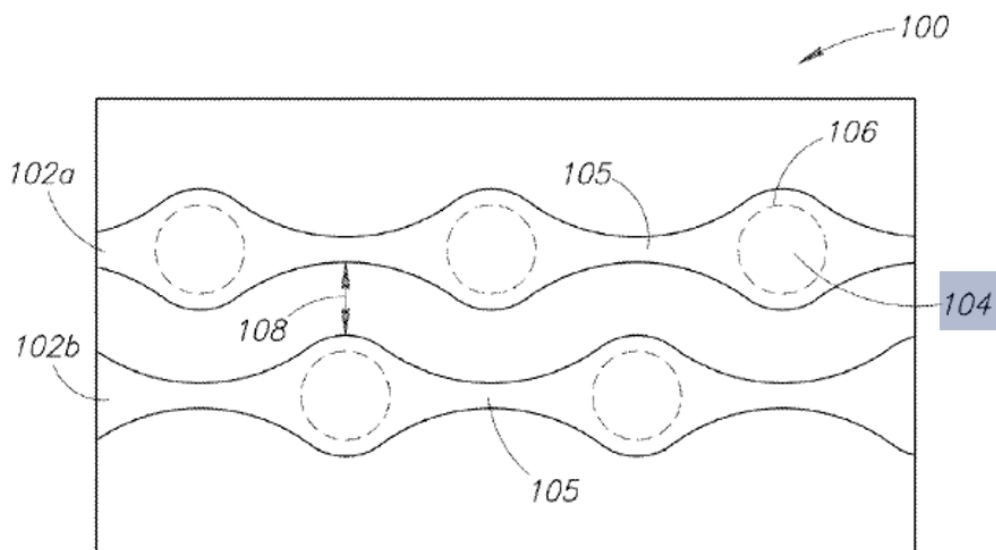


FIG.1B

148. A POSITA implementing Yil's converging-wire connection sections would have found it obvious to employ arc-shaped peripheries for the wider first connection sections while keeping the second connection sections linear. Arc-shaped (rounded) geometries at via landing pads are a standard layout practice in integrated circuit design. Sharp corners in metal conductors concentrate current flow, leading to electromigration and current crowding, especially in circuits that run heavy current, ESD, or have RF signals. Eliminating sharp corners is a common practice for semiconductor engineers. Rounded features improve lithographic patterning margins because corners of rectangular mask features naturally transfer to the photoresist and the metal trench as rounded features during optical lithography, as Zhang expressly teaches. Ex-1007, 6:9–30. Eliminating sharp metallic tips also reduces ESD-susceptible features, which is precisely the problem the '429 Patent purports to solve. A POSITA would have recognized that adopting arc-shaped connection sections in Yil's converging wire was not only predictable but represented a well-known best practice in IC layout for improving manufacturability and reliability, used for a number of decades before 2022. The combination yields predictable results with a reasonable expectation of success. Zhang Figure 7B shows an example of this arc-shaped geometry.

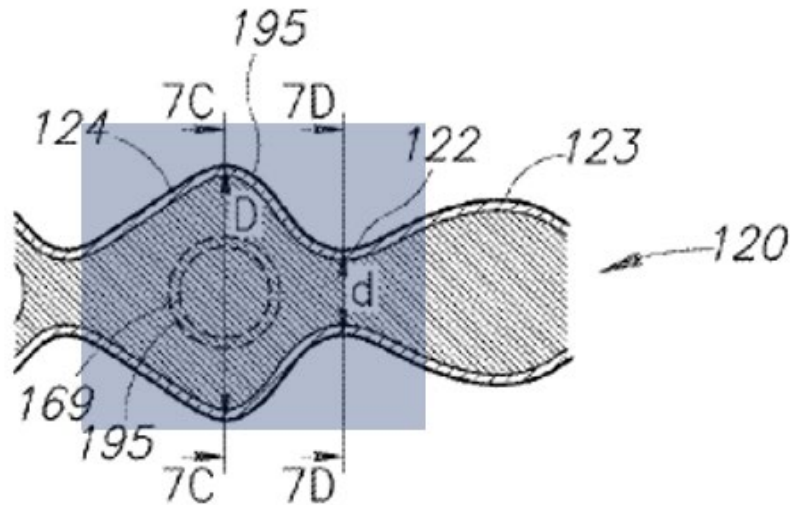


FIG. 7B

149. Furthermore, in my opinion, a POSITA would have been motivated to combine Zhang's teachings with Yi1 because Zhang describes processes that intentionally round corners and use wider vias to improve manufacturing. Zhang describes an optical proximity correction (OPC) process, and explains that "for multiple reasons, it is advantageous for via footprints to remain large, while metal lines continue to shrink with each technology generation." Ex-1007, 1:37-40. The method "takes advantage of the shortcomings of optical lithography to achieve the desired wavy line pattern by anticipating diffraction errors that will occur during exposure of the rectangular features." Ex-1007, 2:12-17. Zhang further teaches that

“severing the dependence of via dimensions on metal linewidths has important advantages and implications for future generations of integrated circuit development.” Ex-1007, 8:28-31.

150. Accordingly, applying Zhang’s teachings to Yi1 would allow the converging wire to accommodate large via footprints while preserving narrower metal-line portions, resulting in manufacturing and resistance benefits. Zhang’s teachings suggest a combination with Yi1’s teachings to improve manufacturing and yield.

2. Claim 6: The display panel according to claim 5, wherein a periphery of each of the plurality of first sections is arc shaped[BH18.1][BH18.2], the plurality of second sections are linearly shaped, a maximum width of each of the plurality of first sections is greater than the width of each of the plurality of second sections

151. In my opinion, the combination of Yi1 with Zhang renders claim 6 obvious and teaches the additional limitation “a periphery of each of the plurality of first sections is arc shaped, the plurality of second sections are linearly shaped, a maximum width of each of the plurality of first sections is greater than the width of each of the plurality of second sections.”

152. As I’ve detailed in my analysis of Claims 4 and 5, Yi1 provides the base structure by teaching a first horizontal pattern extending in direction D1, providing a linear converging wire with a plurality of first and second connection sections that provide power to the converging wire and connect it to the LPL, the claimed shielding layer. Ex-1005, 20:30-37.

153. Zhang supplies the arc-shaped rounded geometry of the connection sections. Applying it to Yil's connection sections yields first connection sections with arc-shaped (rounded) peripheries—analogueous to Zhang's wide portions (via landing pads) with rounded peripheries shown in Figure 7B—while the second connection sections remain linearly shaped, analogueous to Zhang's narrow connecting portions. Ex-1007, 5:7–26, 5:44–57, 6:9–30, 8:11–18, Fig. 7B. Figure 7B of Zhang demonstrates a wavy metal line geometry.

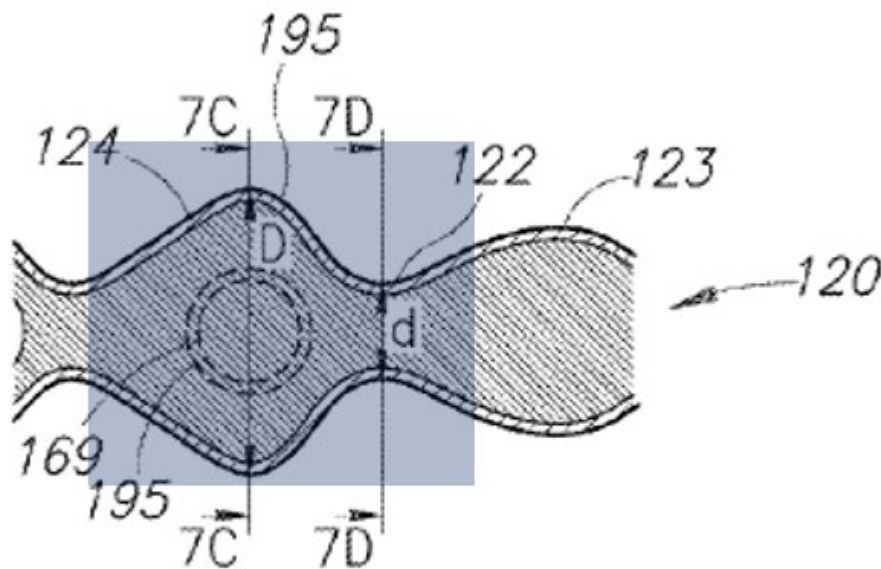


FIG. 7B

154. Zhang also notes that through holes as made in the invention are made through “conventional etching techniques known in the art of semiconductor fabrication for selective removal of polysilicon, silicon nitride, silicon dioxide, metals, photoresist, polyimide, or similar materials includes such processes as wet chemical etching, reactive ion (plasma) etching (RIE), washing, wet cleaning, pre-cleaning, spray cleaning, chemical-mechanical planarization (CMP) and the like.” Ex-1007, 4:26-33. Conventional etching processes would result in contact holes with a circular shape, which has an arc-shaped profile.

155. Zhang’s disclosure is similar to the arc-shaped connection sections described in the ’429 Patent. Figure 2 of the ’429 Patent shows these connection sections, which I have highlighted in dark blue below (zoomed in):

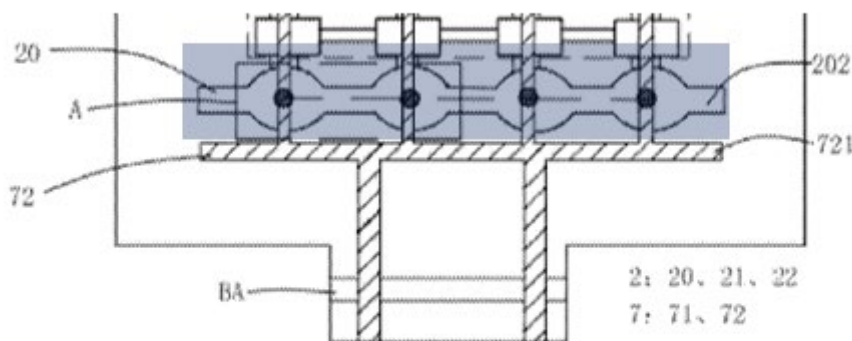


FIG. 2

3. **Claim 16: The display device according to claim 15, wherein a periphery of each of the plurality of first sections is arc shaped, the plurality of second sections are linearly shaped, a maximum width of each of the plurality of first sections is greater than the width of each of the plurality of second sections.**

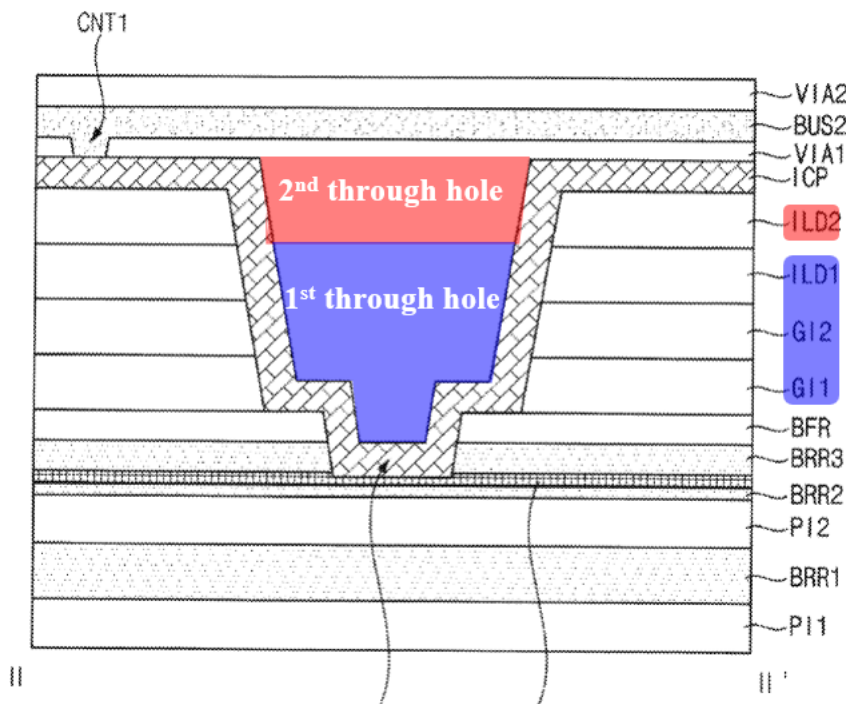
156. Claim 16 mirrors Claim 6. For the same reasons, the combination of Yi1 with Zhang renders Claim 16 obvious.

XIV. D. GROUND 4: CLAIMS 10 AND 20 ARE RENDERED OBVIOUS BY YI1 IN VIEW OF YI2 AND PARK

1. Motivation to Combine Yi1, Yi2, and Park

157. A POSITA would have been motivated to combine Yi1 with Yi2 and Park. As I detail in Section XIII.B.1, a POSITA would have been motivated to combine Yi1 and Yi2. A POSITA would have been further motivated to combine the teachings in Park with Yi1 and Yi2. Yi1 discloses stacked contact holes connecting power supply lines to the shielding layer (Figure 24). Ex-1005, 20:55–21:5.

FIG. 24



158. Yi2 teaches that area of the lower part of the contact hole is narrower than that of the upper part, as the “second contact hole CNT2 may be connected to the first contact hole CNT1.” A “plane area of the second contact hole CNT2 may be smaller than a plane area of the first contact hole CNT1.” Ex-1006, ¶160.

159. Park, in the same OLED display field, expressly teaches “forming a via hole to be larger than a contact hole” to “prevent a patterning defect on a lower electrode, and improve processing stability and reliability.” Ex-1008, 3:16–21. Park further discloses a circular contact hole formed using an etching process, as the “interlayer dielectric 230 on the gate electrode 225 and the gate insulating layer 220, the interlayer dielectric 230 and the gate insulating layer 220 may be etched to form

contact holes 231 and 235 that expose the source region 211 and the drain region 215, respectively, of the semiconductor layer 210.” Ex-1008, 4:47-52, 5:33–37, 7:19-25.

160. A POSITA would have applied Park’s teaching (*i.e.*, making the upper through hole larger than the lower contact hole) to obtain manufacturing-reliability benefits. Dimensioning upper vias to be larger than lower contact holes is a well-known principle in semiconductor and display fabrication. *See* Ex-1012 at 674-676, 690, 726-727. The larger upper via provides alignment margin during photolithography, which is particularly important given the inherent registration tolerances in multilayer thin-film patterning processes. *See* Ex-1009 at 172. In the TFT backplane fabrication process for OLED displays, multiple conductive and insulating layers are patterned sequentially, and contact holes must penetrate through multiple insulating layers to connect different metal layers. Misalignment between mask levels is unavoidable, so designing the upper via to be larger ensures that even with registration error, the via fully overlaps the lower contact hole, preventing patterning defects and open circuits. Park expressly teaches this principle in the OLED context: forming a via hole to be larger than a contact hole to prevent a patterning defect on a lower electrode, and improve processing stability and reliability. Ex-1008, 3:16–21. A POSITA would have had a reasonable expectation

of success because it involves only routine dimensioning of known structures in a well-established multilayer TFT fabrication process.

2. Claim 10

- a. 10[pre]: The display panel according to claim 9, wherein the pixel driving circuit layer further comprises:**

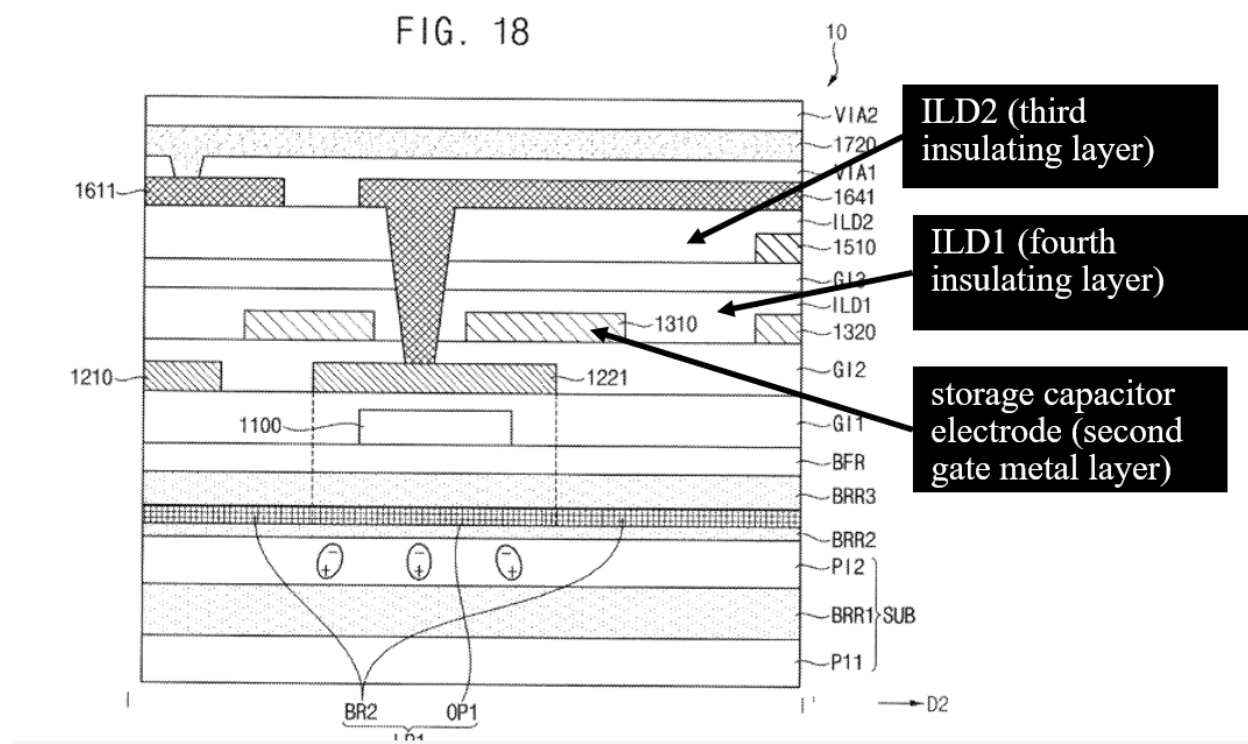
161. In my opinion, the combination of Yi1 with Park teaches this element.

162. As I detail in my analysis of Claim 9, Yi1 teaches the recited pixel driving circuit layer, including the elements 10[a]-[c], which describe in greater below. Park provides the additional requirement in 10[c] that the diameter of a second group of through holes is wider than a first group.

- b. 10[a] a fourth insulating layer disposed between the second gate metal layer and third insulating layer; and**

163. In my opinion, Yi1 teaches this element.

164. Yi1's PCP includes a first inter-insulating layer (ILD1), which is disposed between the second conductive pattern and ILD2. Figure 18 showcases this insulating layer, which is between the electrodes at 1310 (which comprise the second conductive pattern, 1300) and ILD2 (the third insulating layer).

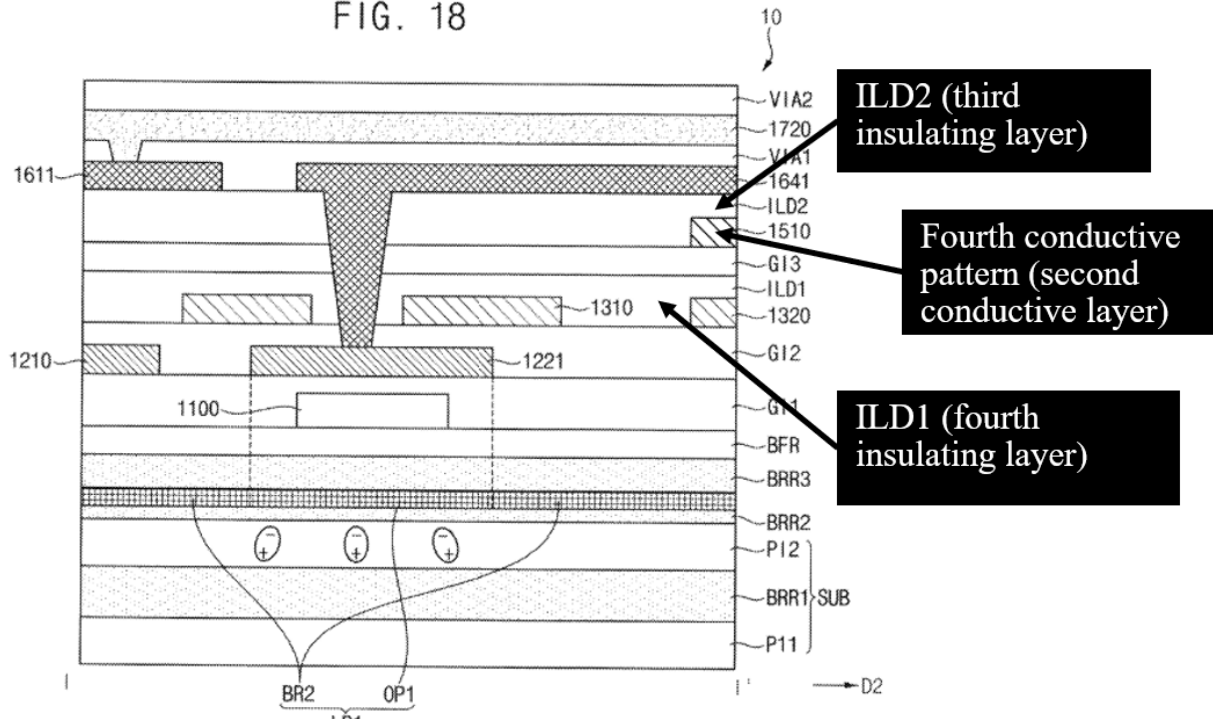


c. 10[b]: a second conductive layer disposed between the fourth insulating layer and the third insulating layer;

165. In my opinion, Yi1 teaches this element.

166. Yi1 teaches a second conductive layer disposed between the fourth insulating layer and the third insulating layer: the third conductive pattern 1500 may be disposed on the third gate insulating layer GI3. The third conductive pattern 1500 may include a third gate line 1510, which may be adjacent to the other side of the first gate electrode 1221. Ex-1005, 15:37-49, 18:3-12. As Figure 18 illustrates, the third conductive pattern 1500, e.g., the third gate line 1510, is between ILD1 (the fourth insulating layer) and ILD2 (the third insulating layer).

FIG. 18



- d. 10[c]: wherein the plurality of through holes comprise a plurality of first through holes and a plurality of second through holes, the plurality of first through holes penetrates through the first insulating layer, the second insulating layer, and the fourth insulating layer, and the plurality of second through holes penetrates through the third insulating layer; wherein the plurality of first through holes are communicated with the plurality of second through holes, and a diameter of each of the plurality of second through holes is greater than a diameter of each of the plurality of first through holes.

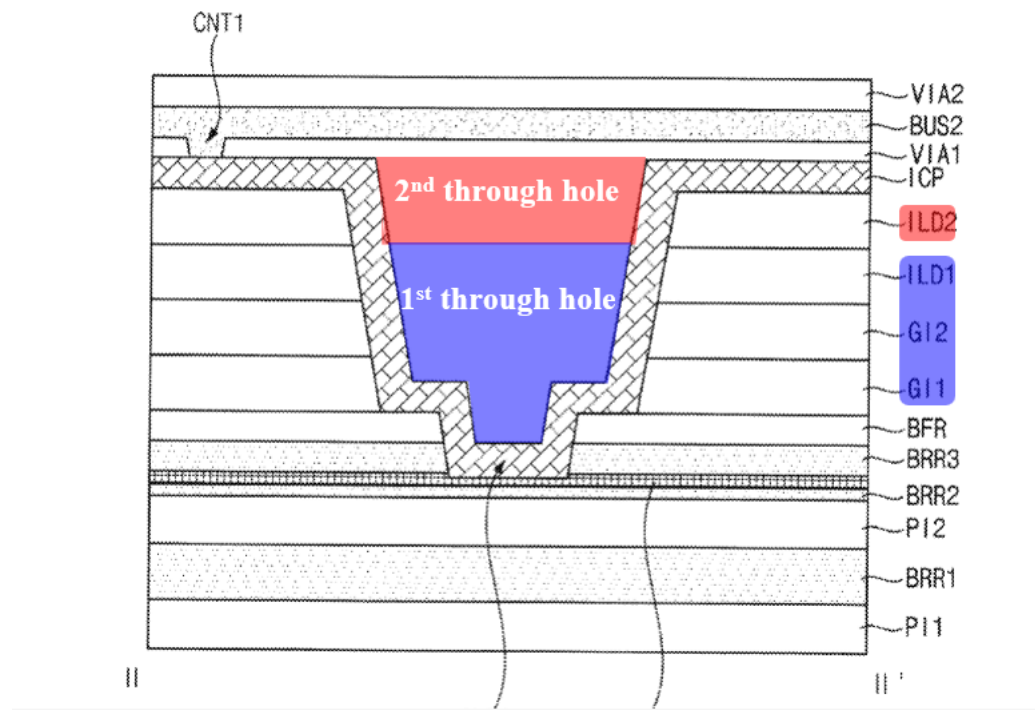
167. The combination of Yi1 and Park teach this claim element.

168. Claim element 10[c] merely requires the through holes to comprise two groups. The first group penetrates three layers: the first, second, and fourth insulating layers. The second group penetrates the third insulating layer. The two groups are

communicated, and the diameter of the second group (penetrating the third insulating layer) is wider than the diameter of the first group.

169. Yi1 teaches the first and second groups of through holes that are communicated with each other. As shown in Figure 24, the second through hole (CNT2) goes through the third insulating layer ILD2, while the first through hole of CNT2 goes through the first gate insulating layer GI1, the second gate insulating layer GI2, and the first inter-insulating layer ILD1 (the first, second, and fourth insulating layers). Ex-1005, 20:65-21:4. Figure 24, below, is annotated to show the two through holes and the layers they penetrate.

FIG. 24



170. These two through holes are “communicated with” each other because they are nested. This is consistent with the ’429 Patent’s own disclosures. Figure 1 of the ’429 patent shows a “plurality of first through holes” that “are communicated with the plurality of second through holes 92.” Ex-1001, 7:37-39.

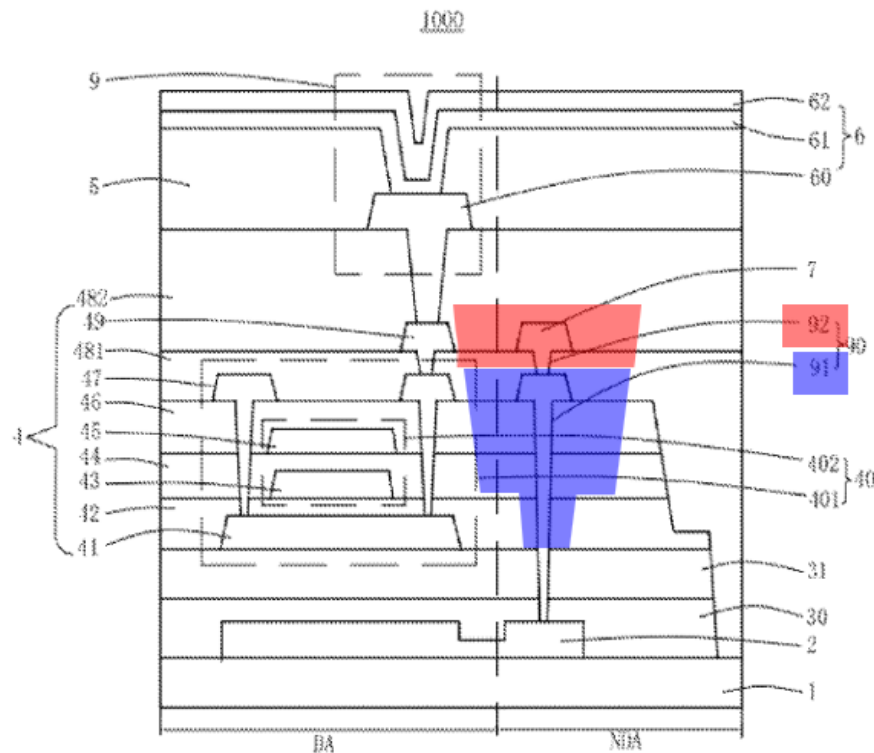
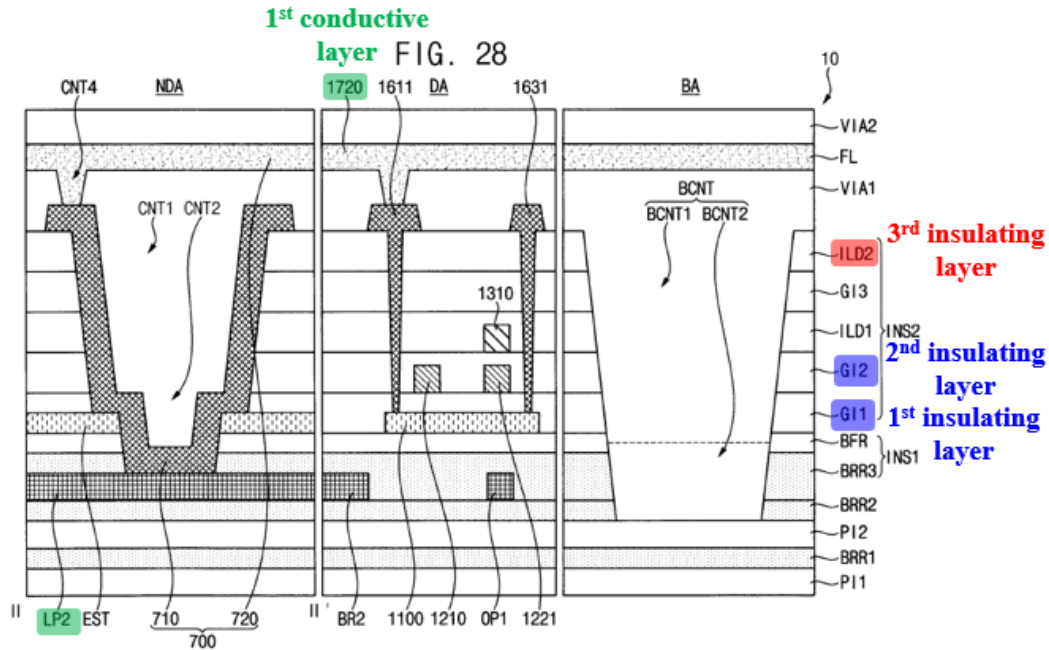


FIG. 1

171. Yi2 likewise teaches that the lower part of the contact hole is narrower than the upper part. Ex-1006, ¶160. Figure 28 of Yi shows this relationship between CNT1 and CNT2, wherein CNT2 is narrower than CNT1:



172. Park teaches forming the upper via hole 267 to be larger than the underlying contact hole 235 in a structure where the via hole is formed corresponding to the contact hole, to prevent patterning defects and improve processing stability and reliability. Ex-1008, 3:16-21, 5:55-67. Figures 4A and 4B of Park show this relationship.

173. The combination teaches Claim 10.

FIG. 4A

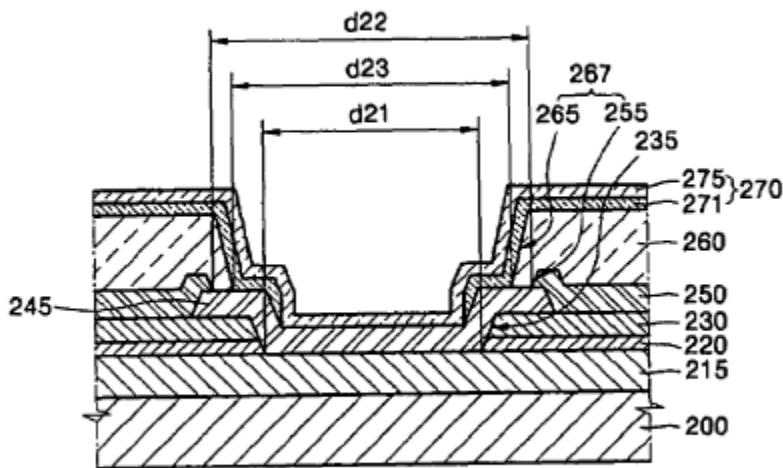
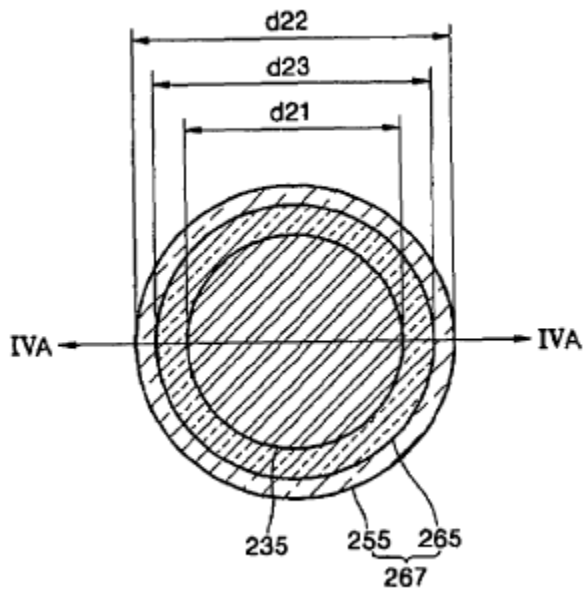


FIG. 4B



174. It would have been obvious to use Park's teaching in Yil's through holes for the reasons I discuss above in the motivation to combine.

175. Therefore, it is my opinion that the combination of Yi1 and Park render Claim 10 obvious.

3. Claim 20

176. Claim 20 mirrors Claim 10 (depending from Claim 19 which mirrors Claim 9). For the same reasons, the combination of Yi1 with Park renders Claim 20 obvious.

XVI. CONCLUSION

177. For the foregoing reasons, it is my opinion that Claims 1–20 of the '429 Patent are unpatentable as obvious under 35 U.S.C. § 103. Each element of each Challenged Claim is taught by the prior art as described above, and a POSITA would have found the claimed combinations obvious for the reasons set forth in this Declaration.

178. I reserve the right to supplement or amend this declaration based on further review of materials, including any responses, declarations, or expert testimony submitted by Patent Owner.

I declare that all statements made in this Declaration of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: Thursday, September 10, 2026



Dr. Michael Lebbey