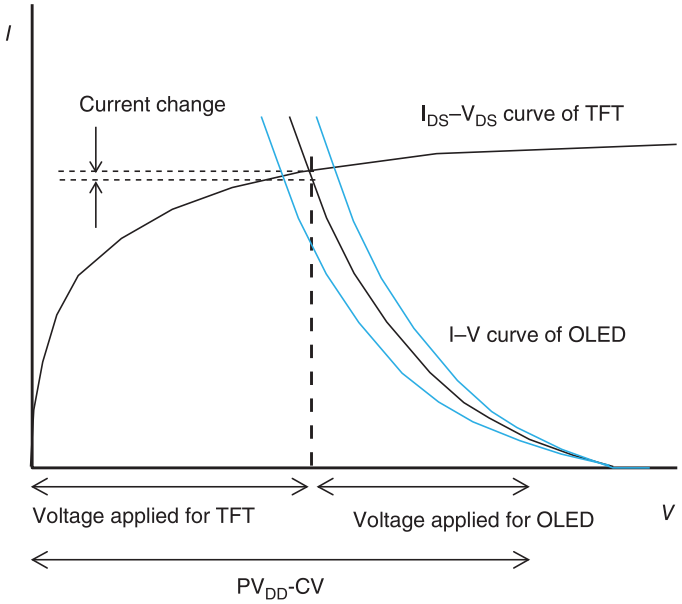


Figure 4.39 OLED current change due to OLED performance change in source-follower type.

be largely changed. However, in the case of source-follower-type configuration, unique compensation happens. As shown in Figure 4.39, because the TFT current is saturated, the OLED current does not change very much when OLED characteristics are changed. Similarly, when TFT characteristics are changed, OLED current change is reduced as shown in Figure 4.40.

In any case, OLED voltage rise, due to the driving stress has been dramatically reduced these days for the product-level OLED device, so the risk of using source-follower type is a minor issue already.

For actual implementation, more complicated circuits are often used to compensate for the current distribution of the driver TFT and OLED device or for their instabilities. These techniques are discussed in Section 6.4.4.

Figure 4.41 shows the matrix arrangement of pixels. Color can be expressed by the combination of red, green, and blue subpixels. Most data drivers can handle 6- or 8-bit grayscales, and for special applications, such as medical use, 10 or 12 bits are used.

When an 8-bit grayscale is used, each (R, B, or G) subpixel can display $2^8 = 256$ grayscales (an average computer handles the value from 0 to 255:256 grayscale in total); therefore, $256^3 = 16{,}777{,}216$.

Almost 16 million colors can be expressed; this is sometimes called a *full-color display*.

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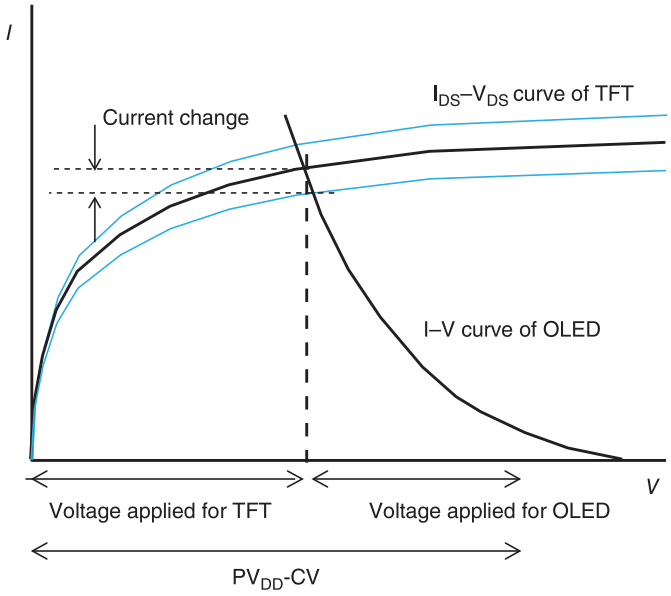


Figure 4.40 OLED current change due to TFT performance change in source-follower type.

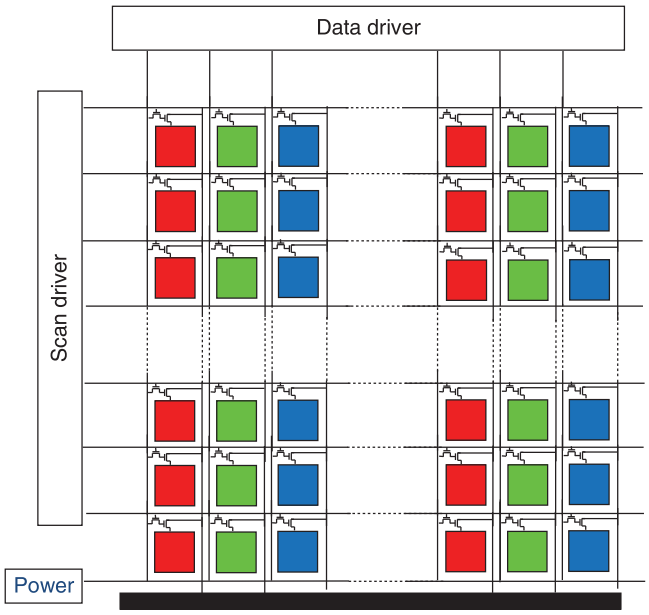


Figure 4.41 An active-matrix OLED display.

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4.4.3 Ambient Performance

As an OLED display is self-emissive, a high contrast value can be obtained if measured in a dark room. However, displays are rarely used in dark environments, so it is more useful to measure contrast ratio in actual environments. For mobile applications, legibility of characters and visibility in bright ambient light are required, so the surface treatment of a display is very important.

4.4.3.1 Living Room Contrast Ratio

As discussed, a dark contrast ratio value does not always indicate the quality of a display. Self-emissive displays show good performance in darker environments, but the image quality is degraded in brighter environments. Table 4.3 lists illuminance values in various environments.

For television applications, the contrast ratio found in home living rooms, which represents nearly the darkest illuminance in actual usage, is often discussed. This contrast ratio value in a 200 lx environment is sometimes called the *living room contrast ratio* (see Section 4.2.1.4 for detailed equation).

Figure 4.42 shows the living room contrast ratio simulation results of a 500 cd/m^2 display, with various surface reflection values without a circular polarizer; however, surface reflection can be more than 1% without it because of reflection due to electrode and wiring. Color filters are also used to absorb the reflection to enhance the living room contrast ratio of an OLED display.

On the other hand, state-of-the-art premium LCD TV displays use expensive antireflection to obtain a ~1500–1800 : 1 living room contrast ratio,

Table 4.3 Illuminance in Various Environments

Location/Environment	Illuminance (lx)
Sunny place in fine spot on warm summer day	>100,000
Shade in hot weather	10,000
Office	750
Reception room in an office	500
Conference room	300–700
Classroom	500
Showroom	500–1500
Display shelf in a shopping mall	500
Living room	200–300
Hotel room	100
Museum gallery	50
Cinema	3
Night with full moon	0.2

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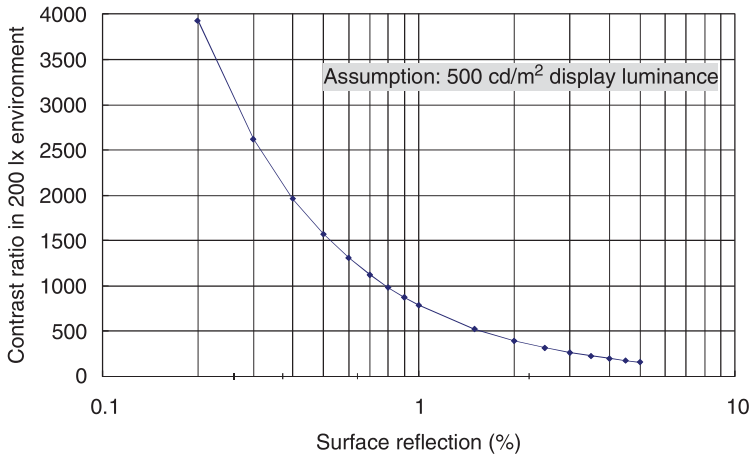


Figure 4.42 Plot of contrast ratio versus surface reflection in a living room.

so an OLED TV display may need to include a circular polarizer with high-performance antireflection.

4.4.3.2 Chroma Reduction Due to Ambient Light

Many display technologies are claiming large color reproduction in their advertisement or in the brochures these days. However, it should be noted that surface reflectance significantly reduces the color reproduction of a display, so catalog specification is not always true in ambient environment.

For example, if a display is used in illuminance E and if surface reflectance is R, luminance increase caused by reflected ambient light can be calculated as follows:

$$\Delta L = \frac{E \cdot R}{\pi} \tag{4.29}$$

For example, if $E = 10{,}000$ lx (shade in bright sunshine, Table 4.3), $R = 1\%$, luminance of reflected light would be

$$\Delta L = \frac{10000 \cdot 0.01}{\pi} = 31.8 \ \ [\mathrm{cd/m^2}]$$

It is as if all the pixels in a display get additional 31 cd/m^2 white (environmental color) emission. Even when pure colors, such as red, green, and blue, are displayed, 31 cd/m^2 white is always added to the displayed colors, which generates pink, light green, and sky blue, respectively. This effect reduces the color reproduction of a display, so low surface reflection is quite important for high-performance display.

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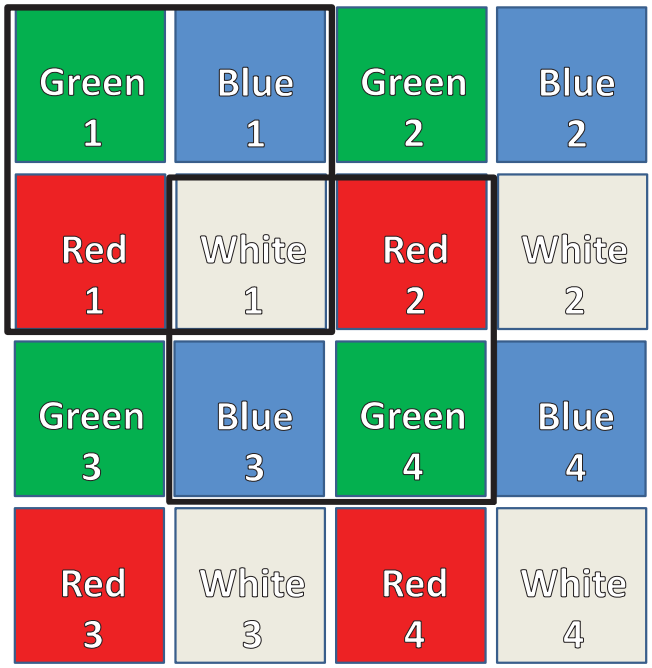


Figure 4.43 An example of an RGBW (RGB+white) pixel layout.

4.4.4 Subpixel Rendering

Figure 4.43 shows four sets of an RGBW subpixel (red, green, blue, and white) layout. As discussed in Section 7.4, the additional white subpixel provides the advantage of power reduction. The primary colors red, green, blue, and white can be used, for example, to show one pixel color (green—1, blue—1, red—1, white—1); therefore, Figure 4.43 potentially shows four pixels.

However, there are other ways of driving this subpixel set. A close scrutiny of Figure 4.43 reveals that the (white—1, red—2, blue—3, green—4) subpixel set can also be regarded as a pixel (dashed line). This kind of approach to increase the apparent resolution is called the *subpixel rendering* method, and the apparent resolution obtained by this method is sometimes called *pseudoresolution*. There are various kinds of subpixel rendering methods, such as the following:

1. Pixel configuration using red, green, blue, and white [34–36]
2. Pixel configuration by combination of large blue + green and large red + green, or two blue, one red, and one green subpixels; this is known as the *PenTile*® (Samsung Electronics) *configuration*. PenTile also includes some implementations using the RGBW pixel layout [37, 38].

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The subpixel rendering method is an effective approach to increase the apparent display resolution with only minimal increase in IC cost.

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5

OLED Color Patterning Technologies

To ensure the success of OLED technology as a major industry, it is necessary to develop strategies to achieve low cost and high productivity, and to develop improved displays to compete with conventional displays and be introduced in new applications on the market. In this chapter, we discuss the color patterning technologies, which gives major contribution to cost and productivity.

5.1 COLOR-PATTERNING TECHNOLOGIES

As OLED materials degrade under at high temperature and humidity, it is very difficult to pattern the organic layer by means of photo-patterning technology, which is normally used in semiconductors and TFTs. Therefore, the shadow mask technique has been used for the patterning, but this leads to many problems. Various approaches have been developed to deal with these problems.

5.1.1 Shadow Mask Patterning

5.1.1.1 Shadow Mask Process

Currently (as of 2017), most small- to medium-size OLED display products for mobile application use shadow masks for color patterning, as shown in Figures 5.1 and 5.2.

Criteria for optimal patterning include the following:

1. High-dimensional accuracy
2. High aperture accuracy
3. Low thermal expansion
4. Minimal shadowing effect (unintended excessive shadowing due to high-incident-angle incident molecules relative to the normal angle, which are prevented from reaching the substrate).

These criteria are important in maintaining display product quality. If they are not satisfied, an abnormal image such as that shown in Figure 5.3 is displayed

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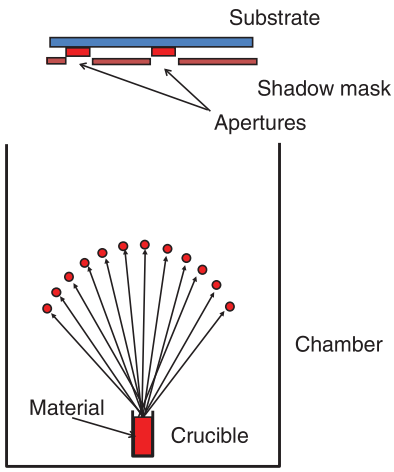


Figure 5.1 Patterning using a shadow mask.

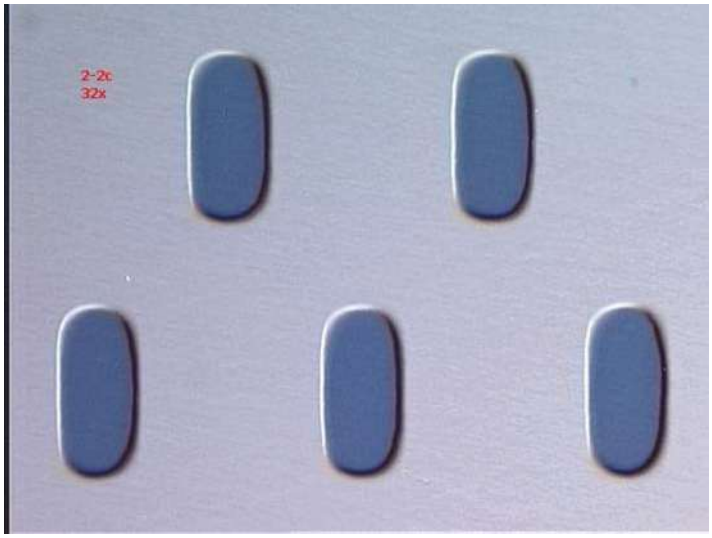


Figure 5.2 Microscopic view of a shadow mask.

and causes yield degradation, so it is very important to take these criteria into consideration.

To reduce the shadowing effect, use of a thin shadow mask with a tapered shape (Figure 5.4) in its aperture provides an effective method.

A *shadow mask* is a thin film of metal or an alloy such as invar metal (Ni alloy), which is normally made by an *etching* method or by electroplating. Features of the *etching* method are as follows:

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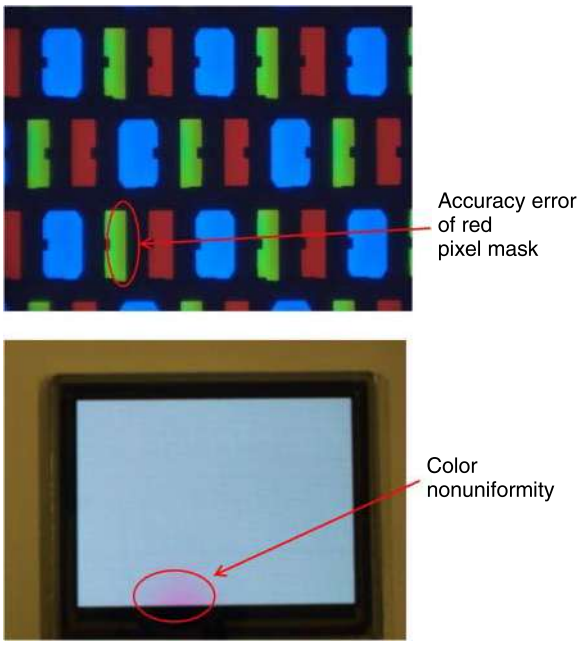


Figure 5.3 Color variation due to shadow mask deformation.

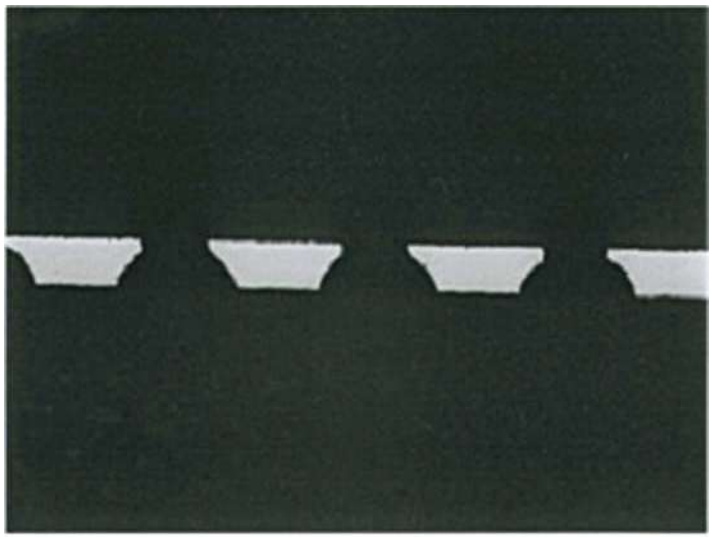


Figure 5.4 Cross-sectional view of a shadow mask.

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- A low-thermal-expansion metal such as invar can be used.
- It is relatively inexpensive.
- The corner of the shadow mask pixel area is rounded.

In contrast, the *electroplating* method can achieve a very thin mask, so it is better than etching in terms of the shadowing effect; however, thermal expansion of most electroplating type mask is not as low as with the etching method, and electroplating is normally more costly. So, the etching and electroplating methods both have pros and cons.

5.1.1.2 Blue Common Layer

Figure 5.5 shows the Blue Common Layer (BCL) structure, reported by Kim et al. [1]. In the case of red and green device, the recombination zone is located at HTL/EML interface, which results in no blue emission, as the holes are blocked by the HOMO energy gap between HTL and EML (Figure 5.6). In the case of blue device, as no EML layer exists, holes are accumulated at the HTL/BCL interface, which results in blue emission (Figure 5.7).

The alignment error described in Section 5.1.1.1 and various design margins define the minimum pixel size limitation. However, there is a trend to aim at higher resolutions to gain better user experience.

BCL idea is to circumvent the minimum pixel size limitation by using blue emission layer as common layer of green and red pixels. As blue layer does not have to be patterned to determine pixels, minimum pixel size limitation is relaxed by the factor of 1/3.

The idea is also used for solution-processed device fabrication [2].

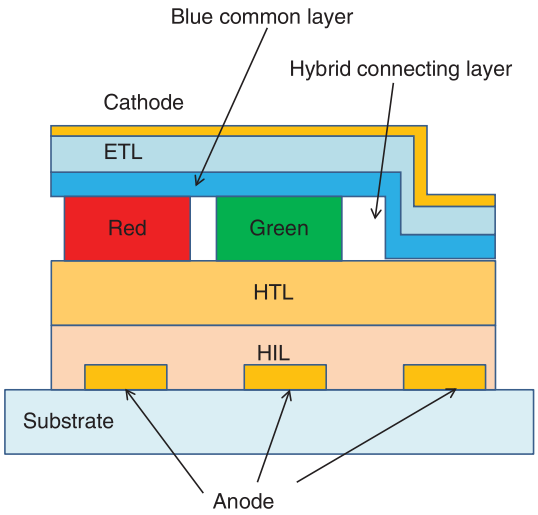


Figure 5.5 Blue Common Layer structure.

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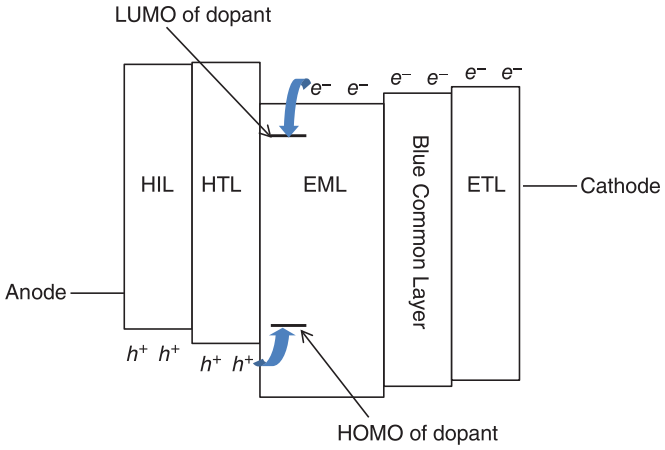
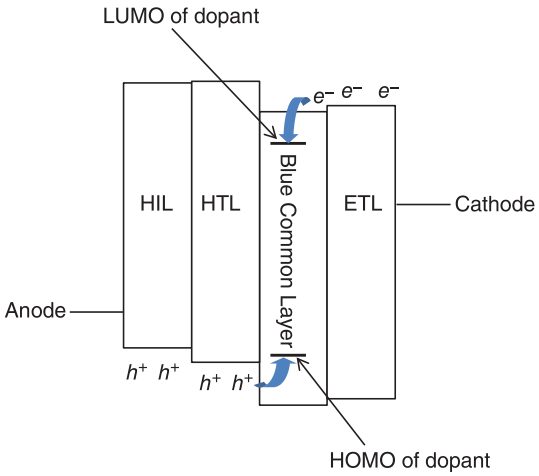


Figure 5.6 Energy diagram of red device in Blue Common Layer Structure.

Figure 5.7 Energy diagram of blue device in Blue Common Layer Structure.



5.1.1.3 Polychromatic Pixel

Figure 5.8b shows the polychromatic pixel, fabricated by vertically stacked OLED unit [3]. (The process details are discussed in Section 9.5.) In conventional pixel design, shown in Figure 5.8a, red, green, and blue subpixels are arranged next to each other so that the mixed color can be observed when the viewing distance is far enough compared with the pixel pitch. With this arrangement, high pixel current density is required to have the same display luminance due to poor aperture ratio, compared with the polychromatic pixel arrangement. High current density causes significant lifetime loss as discussed in Section 2.5.2. Contrally, polychromatic pixel arrangement has very wide

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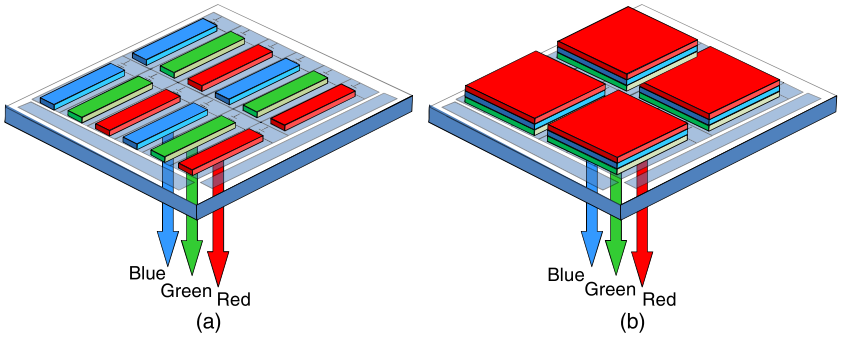


Figure 5.8 Conventional pixel arrangement (a) and polychromatic pixel arrangement (b).

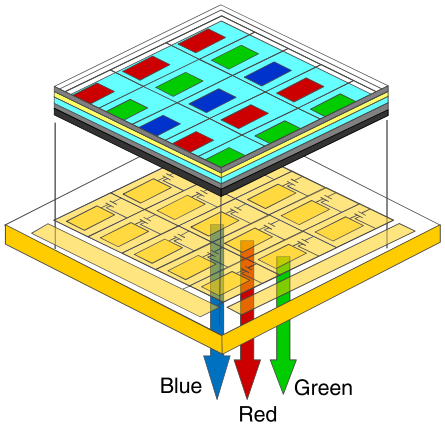


Figure 5.9 Schematic depiction of the RGB pixelation method.

emission area in a pixel, so the low pixel current density reduces the pixel luminance decay, which will lead to much longer image sticking lifetime.

5.1.2 White + Color Filter Patterning

Figure 5.9 illustrates the conventional RGB pixelation method (also called the *RGB side-by-side method*). Red, green, and blue emissive pixels are patterned by, for example, shadow masking. On the other hand, Figure 5.10 illustrates the *white + color filter method*, which displays color by white OLED device emission [4] and color filter absorption of emitted light to tune the color.

The shadow masking process, which patterns the OLED device, sometimes causes production yield issues such as shadow mask deformation and particle generation by shadow mask–TFT substrate contact. The white + color filter method has an advantage in terms of high production yield; however, it is necessary to use some technologies to reverse the emission efficiency loss due to color filter absorption. Details are discussed in Chapter 7.

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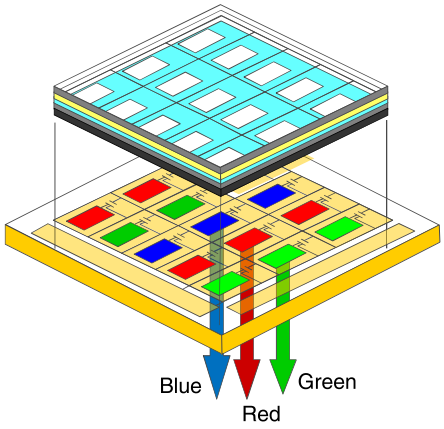


Figure 5.10 Schematic representation of the white + color filter method.

5.1.3 Color Conversion Medium (CCM) Patterning

Filtering methods other than the white + color filter method are also used to display color images. The *color conversion medium* (CCM) method [5] consists of the conversion of blue emission to a longer wavelength using a CCM layer. Unlike the color filter method, which absorbs unnecessary wavelengths and generates heat, the CCM method downconverts the light, so this method can be effective at least theoretically. However, the current CCM method entails application of a color filter to ensure good color quality and also requires a high-performance (high-efficiency and long-lifetime) blue emitter, the performance of which is normally the most difficult to maintain among all the colors, so the CCM method is not widely used these days.

5.1.4 Laser-Induced Thermal Imaging (LITI) Method

The laser-induced thermal imaging (LITI) method uses laser irradiation onto a light-to-heat conversion (LTHC) layer. The resulting local temperature rise transfers organic materials onto the substrate in a predetermined pattern. (The RIST method, discussed in Section 5.1.5, also uses laser irradiation but involves reevaporation, not material transfer as does LTHC.) Figure 5.11 shows the process flow of the LITI method.

The LTHC layer is formed on the donor film. The organic material can be either polymer OLED or small-molecule OLED. By means of laser irradiation, the LTHC layer absorbs light and generates heat. In response to the heat, the organic material layer detaches from the donor film and is transferred to the substrate.

Thus, an organic material pattern is formed on the substrate at the target location. This method can transfer either an organic material layer (donor film contains only one layer in this case) or multiple layers simultaneously (multiple layers are deposited on the donor film in advance in this case).

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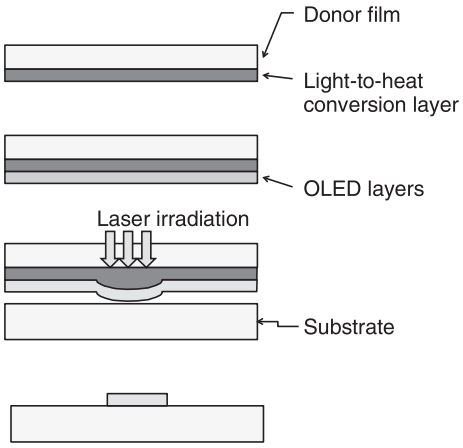


Figure 5.11 Schematic representation of organic material patterning using the laser-induced thermal imaging (LITI) method.



Figure 5.12 An active-matrix OLED display obtained using the LITI method (14-in. demonstration at SID 2004 by Samsung SDI).

Lee et al. [6] report that the donor and receptor surfaces must be in intimate contact for this process to happen. The donor film can be prepared by spin coating, web coating, or vacuum evaporation. The irradiation system used in the paper was continuous-wave 8.0 W Nd : YAG laser.

Figure 5.12 shows an example of an active-matrix OLED display prototype fabricated using the LITI method.

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5.1.5 Radiation-Induced Sublimation Transfer (RIST) Method

The radiation-induced sublimation transfer (RIST) (also called *laser-induced patternwise sublimation* [LIPS]) method involves reevaporation of organic material by laser irradiation.

Figure 5.13 shows the process flow of the RIST method. Initially, organic materials are deposited by thermal evaporation on the donor substrate. The donor substrate can be either glass or plastic. Following irradiation of laser light to the organic film on the donor substrate, reevaporation occurs locally. With this approach, organic film is deposited on the substrate at the target location from the donor substrate.

Figure 5.14 shows an example of an active-matrix OLED display prototype created using the RIST (LIPS) method.

Boroson et al. [7] report that the transfer process requires vacuum environment with the donor–receptor transfer gap of 1–10 μm. 810 nm diode laser and flash lamps with optical mask are used for the irradiation. The donor includes polyimide support (75 μm), a silicon antireflection layer (50 nm), a chromium absorption layer (40 nm), and an organic transfer layer (20–60 nm). The organic transfer layers are typically evaporated in vacuum.

As discussed, RIST uses laser to transfer the organic pattern from donor glass to device substrate, but there is another method proposed to circumvent the disadvantages of lasers, such as maintenance cost. Flash Mask Transfer Lithography (FMTL) [8] utilizes flash lamp to do the transfer instead of laser equipment.

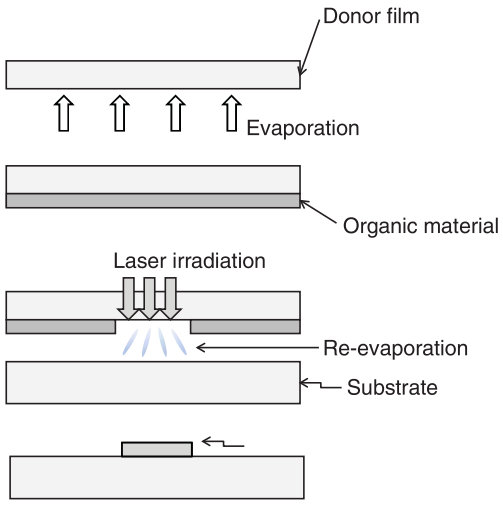


Figure 5.13 Schematic representation of organic material patterning using the radiation-induced sublimation transfer (RIST) method.

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Figure 5.14 An active-matrix OLED display obtained using the RIST method (27-in. demonstration at CEATEC 2007 by Sony).

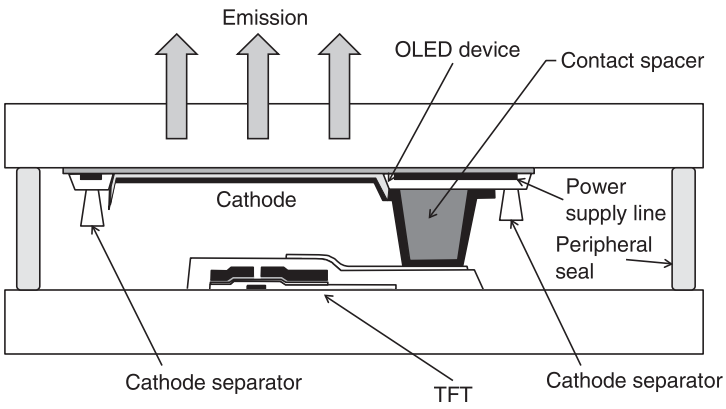


Figure 5.15 Schematic representation of a display structure obtained using the dual-plate OLED display (DOD) method.

5.1.6 Dual-Plate OLED Display (DOD) Method

The dual-plate OLED display (DOD) method fabricates TFT substrate and OLED substrate separately and combines the two substrates later. Figure 5.15 illustrates the process flow of the DOD method.

After the TFT is fabricated using a conventional TFT process, a peripheral sealing resin is dispensed on the TFT substrate. An anode bank is formed on

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the OLED substrate, and a conventional OLED process takes place on it. The TFT substrate is attached to the OLED substrate, and the seal resin is cured by UV irradiation to produce an OLED display (Figures 5.16 and 5.17).

If the attachment process is well engineered, the production yield of this method can be good because the best TFT and OLED substrates are selected before attachment; therefore, no yield loss happens due to the matching of bad TFT + good OLED or good TFT + bad OLED. However, it is important to secure the electrical contact by a contact spacer, as contact problem can cause yield loss, which may diminish the merit of this method.

5.1.7 Other Methods

Figure 5.18 shows the structure of a photopatternable PLED material. The PLED material has the same photosensitivity as that of normal photoresist, so it can be patterned by photoexposure. However, it is very difficult to have both good photosensitivity performance and good OLED device performance, so photopatternable PLED material is not widely used.

5.2 SOLUTION-PROCESSED MATERIALS AND TECHNOLOGIES

Though an OLED display consists of fewer components than an LCD, the cost is, in most case, still higher. The higher cost structure of OLED is mainly due to (1) high encapsulation cost, especially due to the use of cap glass, which requires expensive cavity formation, (2) low material utilization, and (3) low throughput of manufacturing equipment. To reduce (1), frit glass (Figure 3.32) and CVD encapsulation (discussed in Section 3.3.4) are used. To cope with (2) and (3),

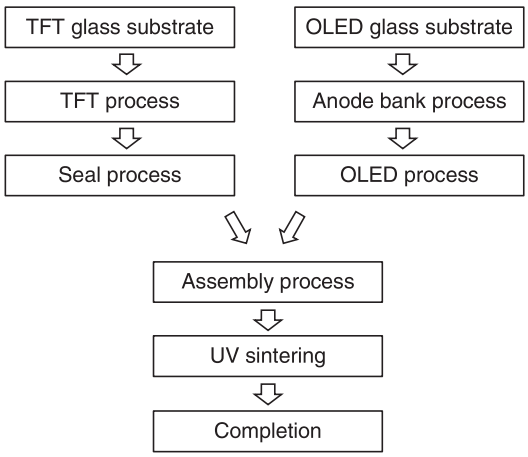


Figure 5.16 Flowchart of the DOD process.

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Figure 5.17 An example of an active-matrix OLED display obtained using the DOD method (19-in. demonstration at SID 2009 by LG Display).

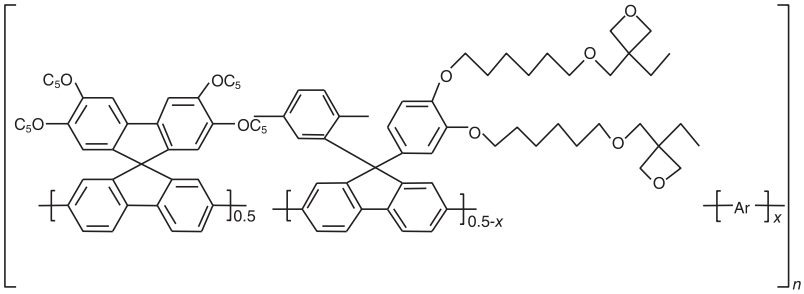


Figure 5.18 An example of a photopatternable polymer OLED (PLED) material (Reported by Becker et al. [9].]

many methods have been proposed. An approach using solution processing is discussed in this section, and another approach using a new vacuum processing method is discussed in Section 5.3. Both cases are claiming large improvements in material utilization and throughput. Figure 5.19 shows the cost simulation of active-matrix OLED display in comparison with LCD (4-in. display driven by PMOS LTPS-TFT substrate with integrated scanner and discrete source driver IC is assumed). By applying flat encapsulation glass (such as frit technology) and improvement in (2) and (3), the cost can be reduced to almost equal to that of LCDs. (This simulation is not taking cost reduction into consideration due

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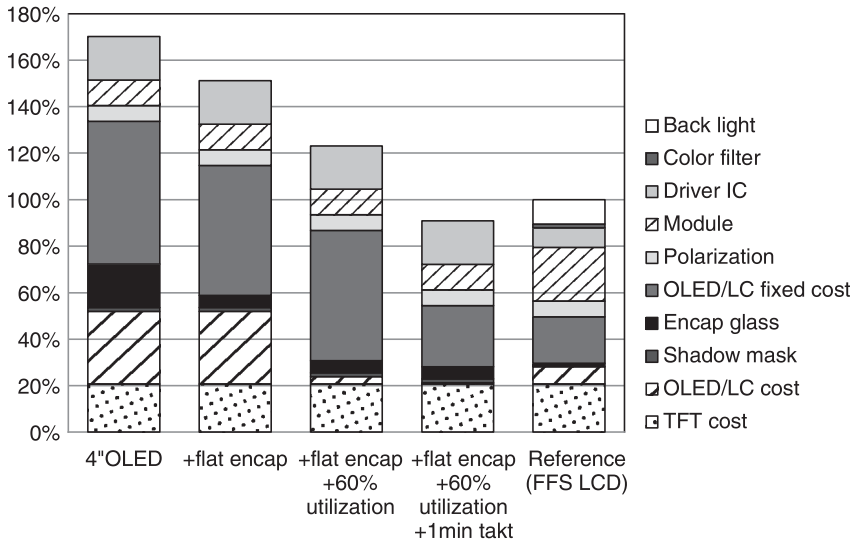


Figure 5.19 Active-matrix OLED display cost simulation.

to scale merit, so there is more room for improvement in the cost structure.) In this section, OLED device fabrication using solution processing is discussed.

To dramatically improve material utilization, several printing methods have been developed, including inkjet printing, nozzle coating [10], offset printing, and gravure printing. Here, we discuss the most popularly used method, inkjet printing.

The typical working principle of the inkjet method consists of the electrostatic acceleration and deflection of ink droplets emerging from nozzles to form designated patterns on the substrate. Ink is ejected from the nozzle by a *piezoelectric device*, which produces a mechanical force when a voltage is applied.

Application of pulse-modulated voltage to the piezoelectric device results in an instantaneous pressure increase that ejects the ink from the nozzle (Figure 5.20).

The method requires control to ensure uniform discharge speed of droplets, angle, volume, and weight. Also, to ensure optimal printing capability, the organic materials need to have the properties of a good ink, such as appropriate surface tension, viscosity, and condensation in the nozzle.

To control the placement and spreading of the ink droplets, surface energy control of the substrate by surface modification or a patterned resin (called a *bank*) is often used, as shown in Figure 5.21. With this method, accurate ink location can be achieved; this method is so reliable that a range of tens of micrometers of ink projection inaccuracy can be tolerated, as the pixel area is determined by the bank structure edge.

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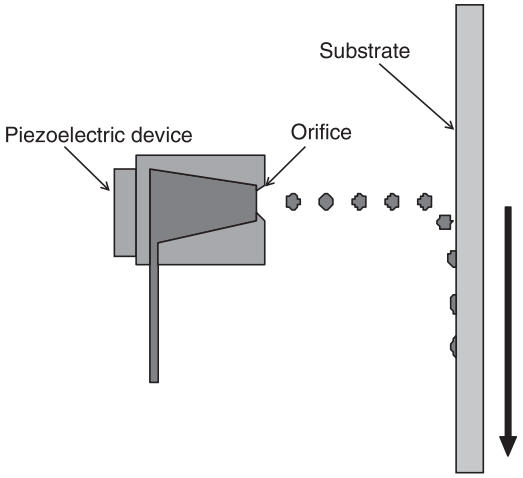


Figure 5.20 Setup for thin-film formation using the inkjet method.

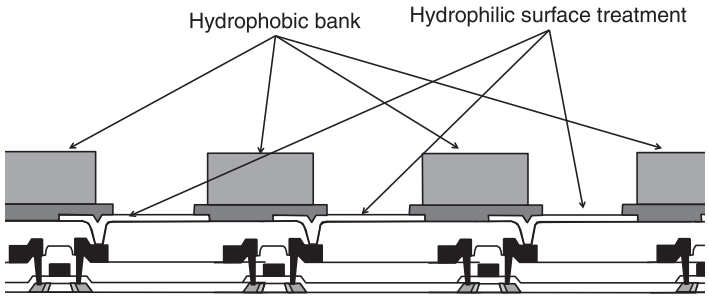


Figure 5.21 Schematic representation of a hydrophilic/hydrophobic structure designed for inkjet patterning.

To enable the hydrophilic/hydrophobic patterning discussed above, surface energy control to ensure adhesion on the pixel but not on the bank is necessary. If the combined surface energy of the substrate and a droplet before and after the droplet landing is F_b and F_a, then, as the kinetic energy (E_k) must be higher than the surface energy on the bank, the following equation must be satisfied:

$$E_\mathrm{k} > F_{a,\mathrm{bank}} - F_{b,\mathrm{bank}} \tag{5.1}$$

On the other hand, to ensure that the kinetic energy is lower than the surface energy in a pixel, the following criterion must be satisfied:

$$E_\mathrm{k} < F_{a,\mathrm{pixel}} - F_{b,\mathrm{pixel}} \tag{5.2}$$

For this kind of control, contact angle measurement such as that depicted in Figure 5.22 is effective. For example, a hydrophilic area such as the pixel

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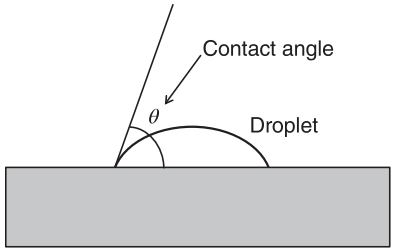


Figure 5.22 Schematic depiction of contact angle measurement.



Figure 5.23 An OLED display obtained using the PLED inkjet method (21-in. demonstration at Display 2007 by Toshiba Matsushita Display).

requires a contact angle of $\theta < 10°$ and a hydrophobic area such as the bank requires a contact angle of $\theta > 80°$ to ensure self-aligned patterning.

Regarding the inkjet method, if the droplet is small, the surface area is large relative to its volume, and unduly rapid evaporation may result. Also, the organic materials are transferred between the central, rapid-evaporation region and the slow-evaporation, bank-side regions. Therefore, both surface tension and drying conditions must be considered.

Figure 5.23 shows a 21-in. display prototype using the polymer OLED inkjet method.

Polymer OLED (PLED) materials can contain long conjugated bonds, so red-emission OLED devices tend to perform well; however, device efficiency is lower when blue-emission OLED devices are used. This is why the use of a modifying agent, such as a dendrimer—a molecular structure with soluble chains surrounding the emission center (Figure 5.24)—has been proposed.

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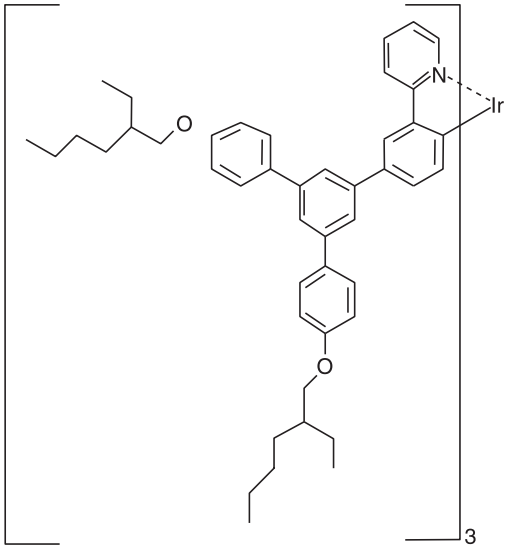


Figure 5.24 Structure of a dendrimer material (IrppyD) (Reported by Markham et al. [11]).

Dendrimers render the small-molecule material soluble and thus improve the performance and productivity of both small-molecule and PLED devices.

5.3 NEXT-GENERATION OLED MANUFACTURING TOOLS

Current OLED material is expensive, ranging from $5 to $10,000 per gram. In actual thermal evaporation manufacturing processes, OLED material deposited on the substrate constitutes only ~2–3% (including material consumption during startup, stabilization, tooling/equipment check, substrate waiting, cooldown, and unusable remained material in crucible after a week of operation) of the total amount of prepared material in the evaporation source. Low material utilization can bring high cost, so it is very critical to suppress material consumption during OLED display manufacturing. To address this situation, many high-material-utilization processes, such as the vapor injection source technology (VIST) method, hot-wall method, and organic vapor-phase deposition (OVPD), have been proposed.

5.3.1 Vapor Injection Source Technology (VIST) Deposition

The VIST method (also called Kodak vapor injection source [KVIS]) involves a procedure similar to flash evaporation, which is unique in that the deposition is effected under nonequilibrium conditions (Figure 5.25).

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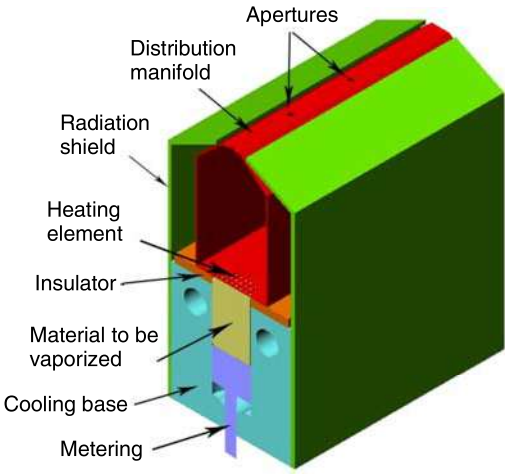


Figure 5.25 Illustration of the concept of vapor injection source technology (VIST), an application of flash evaporation.

The VIST method is applied to mitigate the trade-off between high deposition rate and material consumption, which is unavoidable with the conventional evaporation technologies. Material evaporates instantaneously on physical contact with the heated region.

In normal OLED manufacturing using conventional evaporation sources, OLED material is heated in one evaporation source for a long period, for example, 1 day or 1 week. Therefore, material decomposition is often a serious problem.

In the VIST method, powder materials transferred to the heated region are exposed to high temperatures for a much shorter time period (e.g., ~2 s), so the degree of thermal decomposition is negligible. Also, the material is maintained at room temperature before it is evaporated, so the stored material does not decompose whatsoever.

Figure 5.26 compares the performance levels of white-emission OLED devices using point-source technology (0.2 nm/s) versus VIST technology (5 nm/s) using thermally sensitive blue emission material. OLED device efficiency and voltage are almost equal, and the OLED device lifetime using VIST technology is longer than that using point source. Thus, VIST is more effective for thermally sensitive materials. In particular, many thermally sensitive materials are available on the market, so the demand for VIST may increase.

Many other high-material-utilization sources have been proposed, but doping capability is problematic for many of them. This is because most of the evaporation using these sources is controlled by equilibrium conditions, whose doping condition is subjected to the partial pressure of the organic materials to be evaporated. With VIST, most of the evaporation takes place under

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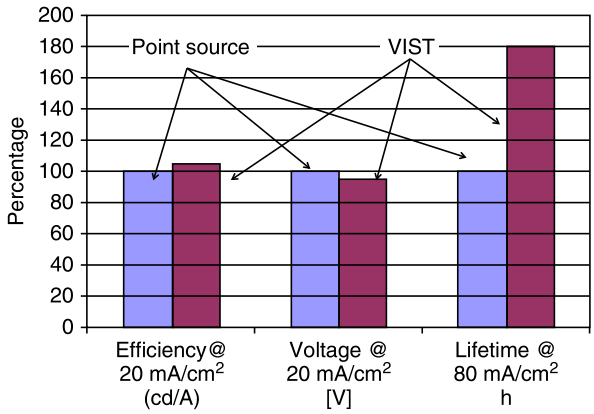
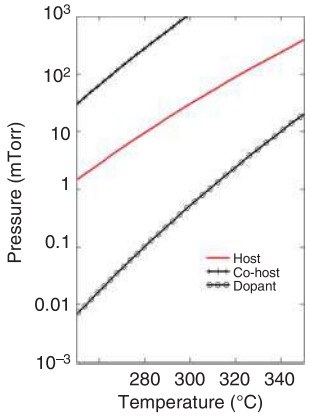


Figure 5.26 Comparison of device performance for point and VIST sources.



	Host (%)	Co-host (%)	Dopant (%)
Mixing ratio of powder material	74	25	1
Ratio of deposited material	74	25	1

Same concentration as the mixed powder

Figure 5.27 Comparison of doping performance for materials with widely different evaporation pressures.

nonequilibrium conditions. This problem can be avoided by mixing the powder materials in advance, to control the doping concentration, even for multiple materials with totally different evaporation pressures (Figure 5.27).

The VIST method (Figure 5.25) achieves uniform deposition using a gas transfer structure called a *manifold*, which is equivalent of the showerhead in CVD equipment. The manifold has multiple apertures, which connects the manifold to the material supply component, called an *injector*. As shown in Figure 5.28, it is possible to connect multiple injectors to one manifold and perform multilayer deposition using only one manifold.

There are several ways to implement the VIST method in actual equipment, such as installing multiple linear manifolds (Figure 5.29a) to produce inline

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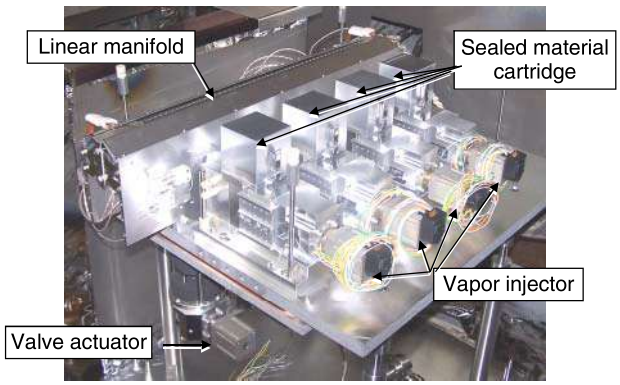


Figure 5.28 A dopant-monitoring apparatus in which multiple injectors are connected to a single manifold.

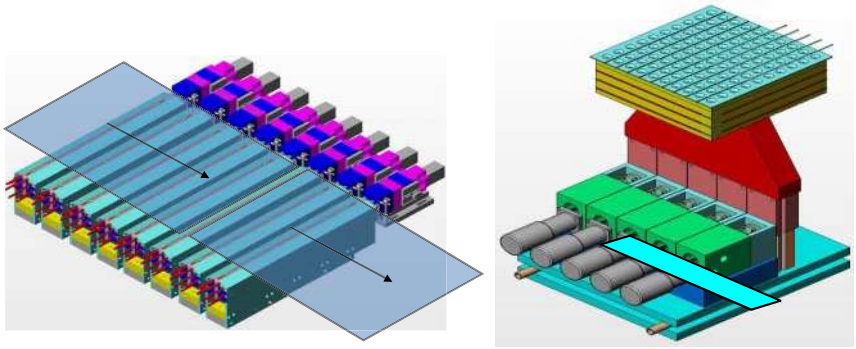


Figure 5.29 Examples of multilayer fabrication using a VIST source.

equipment or introducing an area (evaporation) manifold to deposit multiple layers in one chamber with multiple injectors connected to one manifold (Figure 5.29b). In either case, high material utilization would be possible.

One advantage of the VIST method is that the equipment can be operated without a crystal thickness monitor (discussed in Section 3.2.2.3), which requires frequent high-cost maintenance. The VIST method employs a Pirani gauge attached to the manifold to monitor pressure (Figure 5.30). Conventional vacuum evaporation used for the OLED manufacturing actually measures the deposition rate from the deposited film thickness change by monitoring the oscillation frequency of the quartz substrate (see Section 3.2.2.3 for detail). Pirani gauge directly can measure the pressure to know the deposition rate. As shown in Figure 5.31, the crystal thickness monitor and the Pirani gauge are closely correlated. As the deposition rate measurement by the Pirani gauge does not require parts exchange during manufacturing that are different

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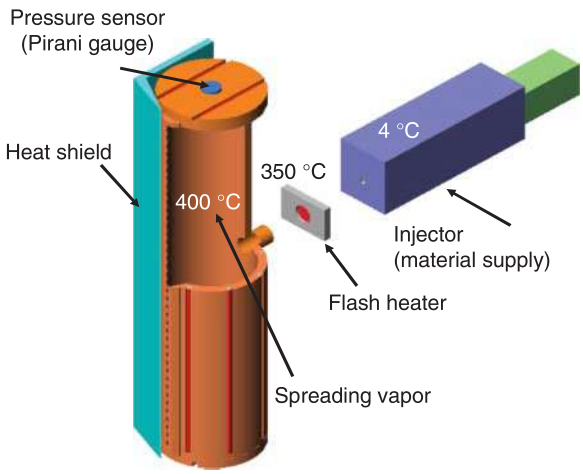


Figure 5.30 A pressure-monitoring apparatus in which a Pirani gauge is attached to a manifold.

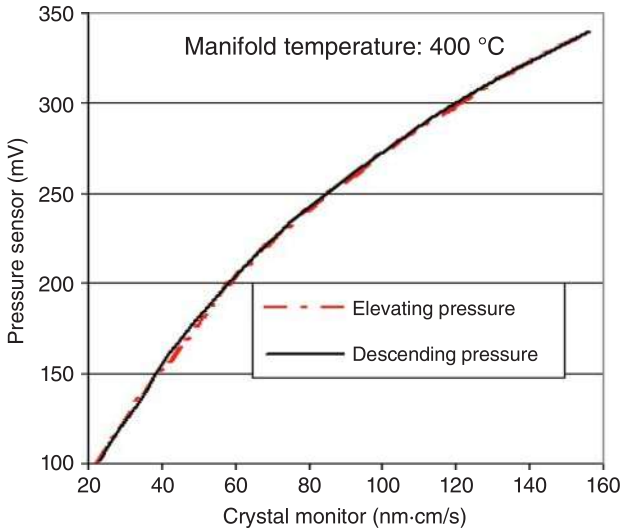


Figure 5.31 Graph illustrating correlation between crystal thickness monitoring and pressure sensing.

from those involved with the crystal monitor, the equipment utilization ratio can be increased. As shown in Figure 5.27, the doping ratio using the VIST method is determined by the mixture ratio of dopant in the powder, so the dopant concentration can be calculated from the total thickness, which can be calculated from the total pressure measured by the Pirani gauge.

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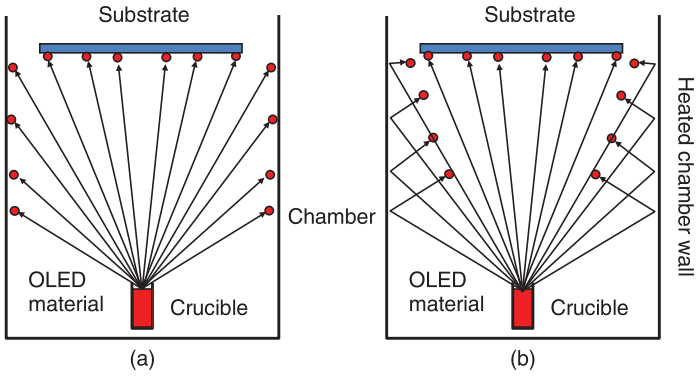


Figure 5.32 Schematic representations of OLED material deposition mechanism using (a) conventional evaporation and (b) hot-wall methods.

5.3.2 Hot-Wall Method

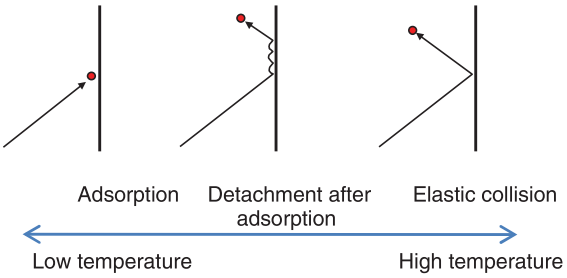
As discussed in Section 3.2.2.1, a nonnegligible amount of OLED material is actually deposited on the substrate, and most of the volume is deposited elsewhere, such as on a chamber wall, shutter, or control plate, as shown in Figure 5.32a. Because of the low utilization of OLED material, the material cost during manufacturing is both expensive and problematic.

The hot-wall method is used to avoid material deposition upon evaporation by heating the chamber wall during evaporation to achieve high material utilization (Figure 5.32b).

Figure 5.33 shows the variation in behavior of an incident molecule that hits a wall when the wall temperature changes.

- If the temperature is low (Figure 5.33a), the incident molecule hits the wall and then adheres to it.
- If the temperature is higher, the incident molecule has more kinetic energy, so after it hits the wall, it detaches from it (Figure 5.33b).
- If the temperature is much higher, the incident molecule does not adhere to the wall but makes an elastic collision (Figure 5.33c).

Figure 5.33 Schematic depiction of the behavior of an incident evaporation molecule on collision with a wall.



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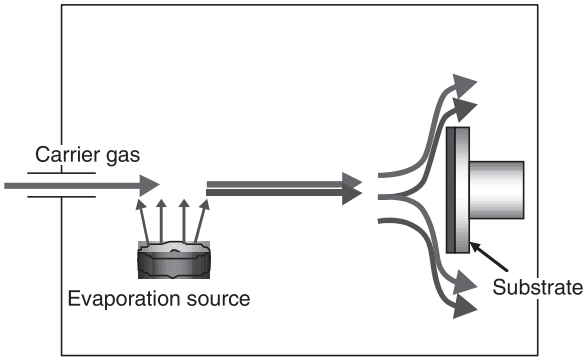


Figure 5.34 Flowchart showing thin-film deposition using the organic vapor-phase deposition (OVPD®; a trademark of Universal Display Corp.) method.

The hot-wall method has high material utilization but has drawbacks such as the following:

- Damage to OLED device due to radiant heat
- Deformation of shadow mask due to radiant heat
- Necessity for enough outgassing after maintenance to avoid the impurities coming out from the chamber wall (grease, O-ring, etc.) during the deposition process.

5.3.3 Organic Vapor-Phase Deposition (OVPD) Method

The OVPD method consists of transferring material via a carrier gas and depositing film on the cooled substrate from the shower plate (Figure 5.34) [12].

Figure 5.35 shows a simplified example of actual OVPD equipment. Material consumption can be switched on and off by valve operation, thus ensuring good material utilization as unnecessary evaporation can be suppressed, such as during substrate-handling, startup, and cooldown periods.

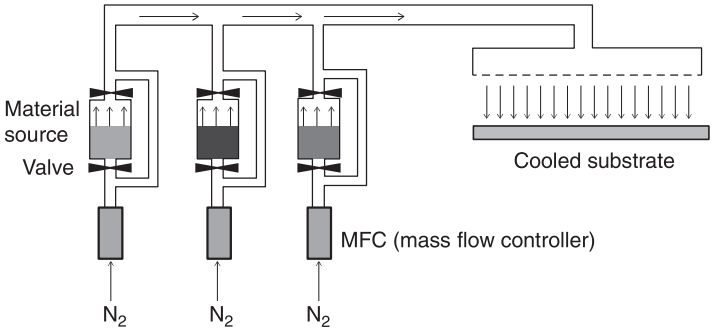


Figure 5.35 Schematic representation of the OVPD apparatus.

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Short Thermal Exposure source (STEx) further improves the merit of OVPD equipment. It maintains the organic material in a room temperature reservoir, and carrier gas with controlled concentration of organic material is made by means of flash vaporization of material supplied by aerosol method [13].

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6

TFT and Driving for Active-Matrix Display

Thin-film transistor technologies for active-matrix driving are discussed in this chapter.

6.1 TFT STRUCTURE

Figure 6.1 shows structural differences between polysilicon (polycrystalline silicon) and amorphous silicon (sometimes abbreviated as a-Si or α-Si).

As shown in the figure, amorphous silicon has an irregular structure, so the potential energy is irregularly distributed. Therefore, the moving charge is scattered and mobility is low. The binding state fluctuates as a result of trapping and detrapping, so TFT characteristics change over time. On the other hand, polysilicon inside a grain has a cubic crystalline structure similar to that of single-crystal silicon, where the charges move within a periodical potential in the same way as in a single crystal, so the mobility is very high and stable.

Figure 6.2 shows a TFT substrate used in an actual active-matrix OLED display product. It is very similar to the LCD display TFT backplane except for the existence of a driver TFT in the OLED backplane.

There are two basic types of TFT structure, according to the electrode configuration: top-gate and bottom-gate TFT [1]. When the gate electrode is located above the source–drain electrode, it is called *top-gate* (or *staggered*) *TFT*. When the source and drain are above the gate electrode, it is called *bottom-gate* (or *inverted staggered*) *TFT*. Figure 6.3 shows examples of top- and bottom-gate TFT structures. Advantages of top-gate structure include the following:

- Low-resistance wiring can be easily used because gate wiring, which is subjected to high temperatures during fabrication, is formed after high-temperature processes such as polysilicon formation or gate insulator deposition.

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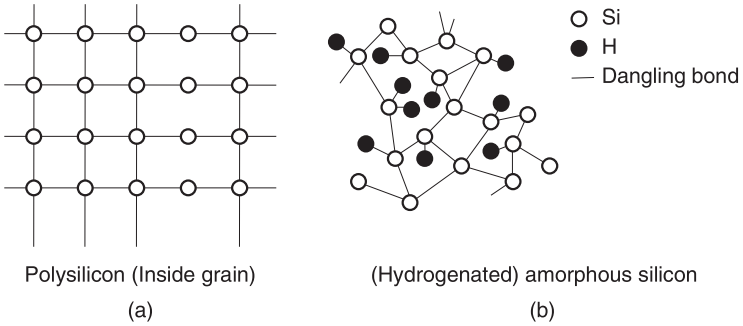


Figure 6.1 Differences between (a) polysilicon (inside grain) and (b) (hydrogenated) amorphous silicon.

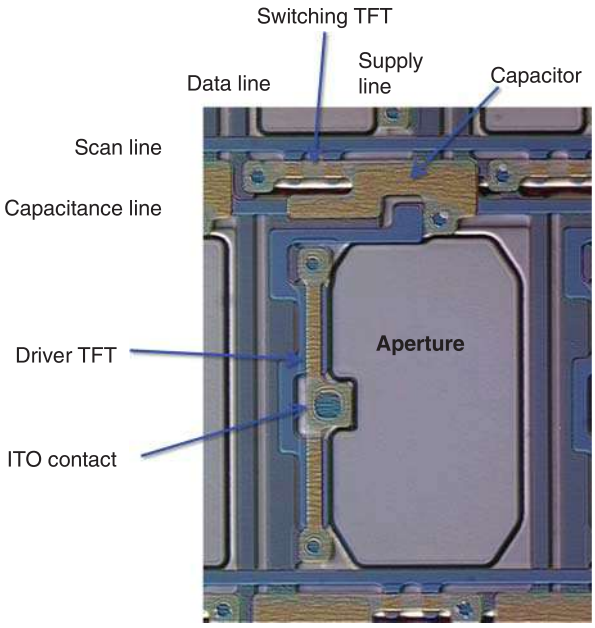


Figure 6.2 An example of a polysilicon-driven OLED display panel.

- A self-aligned doping process is available using gate metal as a mask. Self-aligned structure has a merit in reduced parasitic capacitance, which causes charging errors of the driver TFT gate node. Also accurate positioning of the doping region by self-alignment has merits in the N-region positioning control so that the hot carrier effect caused by the gate to the source electric field can be reduced.

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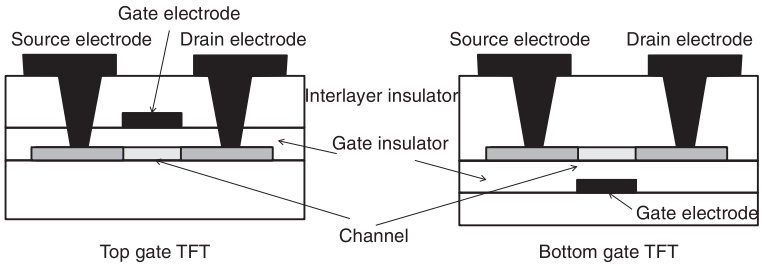


Figure 6.3 (a) Top-gate and (b) bottom-gate TFTs.

Advantages of bottom-gate TFT structure include the following:

- A low-cost amorphous silicon TFT (Figure 6.5) facility can be used for fabrication.
- Continuous deposition can be applied in a vacuum environment between the gate insulator and silicon, which provides better and more stable TFT performance.

Here, we discuss the OLED backplane, using a top-gate TFT structure.

Figure 6.4 shows a cross section of a polysilicon TFT, with an N-channel doping region and a P-channel doping region on the same substrate. This is called a complementary metal oxide semiconductor (CMOS) circuit, the main advantage of which is low-power driving (discussed in Sections 6.4.4 and 6.4.5). However, as shown in Table 6.1, CMOS process flow is more complicated than that of amorphous silicon (Figure 6.5), which has only four or five patterning steps. Thus, there is a trade-off between cost reduction by circuit integration and cost increase due to increased process complexity.

To address this issue, many companies are developing CMOS mask step reduction and single-channel (either PMOS or NMOS) circuit integration technologies (see the discussion in Section 6.4.5).

6.2 TFT PROCESS

The TFT fabrication process for OLED application is discussed in this section.

6.2.1 Low-Temperature Polysilicon Process Overview

Figure 6.6 presents one example of the polysilicon TFT fabrication process.

After amorphous silicon deposition by PECVD (plasma-enhanced chemical vapor deposition) and its dehydrogenation, the Si film is crystallized by

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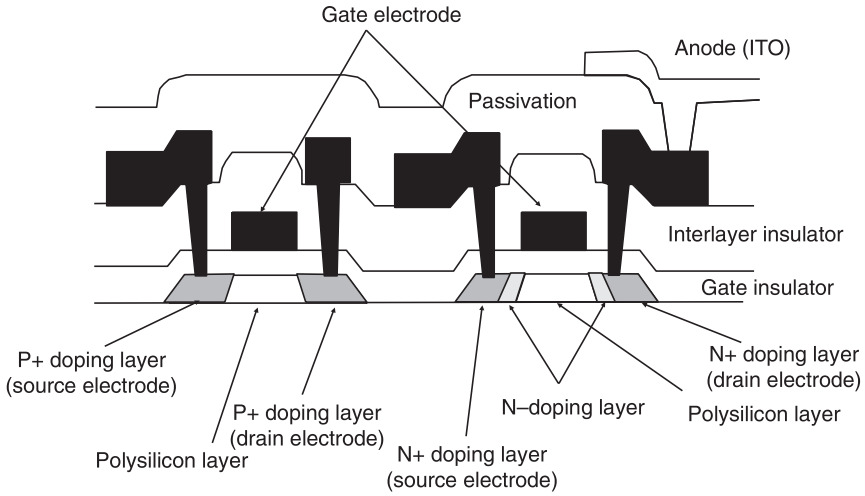


Figure 6.4 Cross section of CMOS polysilicon TFT.

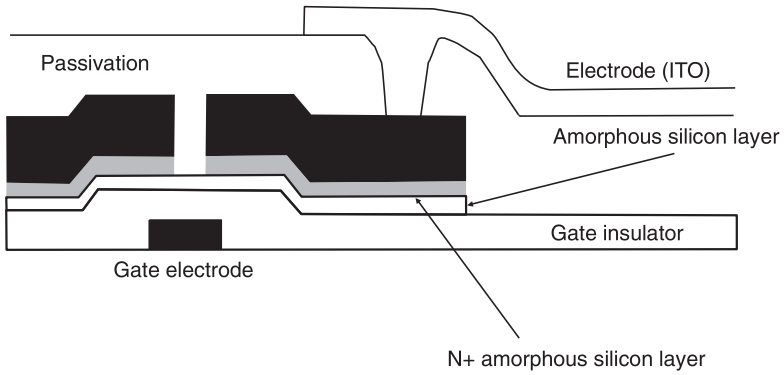


Figure 6.5 Cross section of typical amorphous silicon TFT.

excimer laser annealing (ELA) (Figure 6.6a). After polysilicon patterning, the gate insulator and gate electrode are formed (Figure 6.6b). The source–drain contact is formed by an ion doping process using the gate electrode as a mask. For the N channel, leakage current is a serious issue, as discussed in Section 6.4.1, so a lightly doped drain (LDD) region is formed by an additional low-concentration doping process using an offset created by anodic oxidation of the gate electrode or the gate electrode etching bias (Figure 6.6c). After an interlayer dielectric film is formed, contact holes are made, the source–drain layer is formed (Figure 6.6d), and then an ITO pattern, used for an OLED anode electrode, is fabricated to produce a TFT substrate.

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Table 6.1 Typical Steps in the CMOS Polysilicon TFT Process

Photoengraving Process (PEP) Step	Activity or Procedure
	Cleaning CVD (a-Si) Dehydrogenation annealing Ion doping (Br channel doping)
1	Si island resist patterning Dry etching
2	P doping mask formation Ion doping (P-channel doping) CVD (gate insulator) Sputter (gate electrode)
3	Gate electrode mask formation Dry etching Ion doping (LDD doping by P)
4	Br doping mask (P^+) formation Ion doping (Br)
5	P doping mask (N^+) formation Ion doping (P) Activation anneal
6	Contact hole mask formation Wet etching Sputter (data line)
7	Data line mask formation Wet etching CVD (passivation)
8	Passivation patterning mask Dry etching H_2 forming anneal Sputter (ITO)
9	Pixel mask formation Wet etching Inspection

Table 6.1 lists steps in a process flow for the fabrication of a CMOS backplane (a CMOS TFT circuit contains both P- and N-channel devices). In this embodiment, nine mask patterning and five doping steps are required; however, as complicated process steps result in cost increase, simplified processes for patterning and doping are employed for state-of-the-art fabrication processes.

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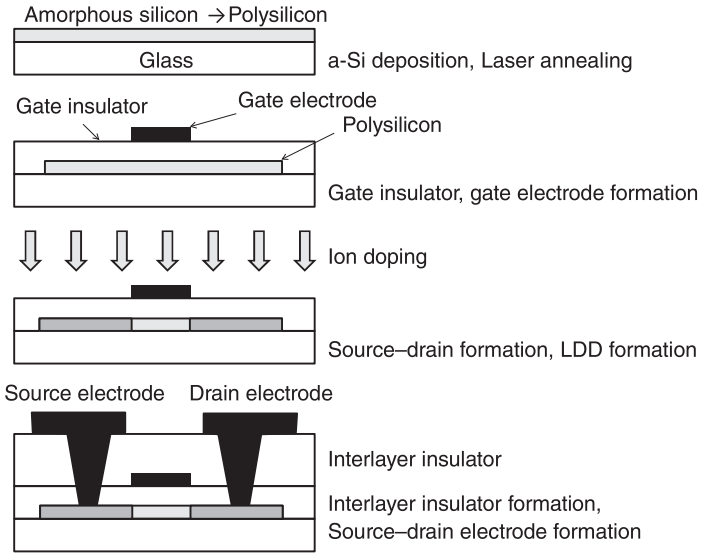


Figure 6.6 Flowchart of polysilicon TFT process.

6.2.2 Thin-Film Formation

Films used for TFT are generally prepared by two kinds of deposition methods: CVD and sputtering (also called PVD: physical vapor deposition). The films prepared by CVD for TFTs are amorphous silicon for the channel layer (polysilicon is formed by annealing an amorphous silicon film), N^+ amorphous silicon for the contact layer (although conventional polysilicon TFT has been using the doping implantation to form the contact region just like semiconductor process, the use of N^+ amorphous silicon, popularly used for amorphous silicon TFT process, is increasing to reduce mask steps), gate insulator, an interlayer dielectric, and a passivation film such as silicon oxide (SiO_x), silicon nitride (SiN_x), and silicon oxynitride. In particular, PECVD, a method involving the deposition of material created by reactions in a plasma of a gas mixture, for example, silane (SiH_4) and hydrogen (H_2) in the case of amorphous silicon deposition, are often employed (Figure 6.7a).

On the other hand, metal films such as aluminum, aluminum alloys (AlNd is often used for gate bus wiring), molybdenum, molybdenum alloys (such as MoW and MoTa), chromium, tantalum, and copper are deposited by the sputtering method. Insulators such as SiO_2 or a transparent electrode such as ITO or IZO (indium zinc oxide) can also be deposited by radiofrequency (RF) sputtering or the ion plating method. The sputtering (Figure 6.7b) method deposits onto a substrate, material ejected from the sputter target by recoil under impact by energetic bombardment of an ionized gas such as argon. Films deposited by

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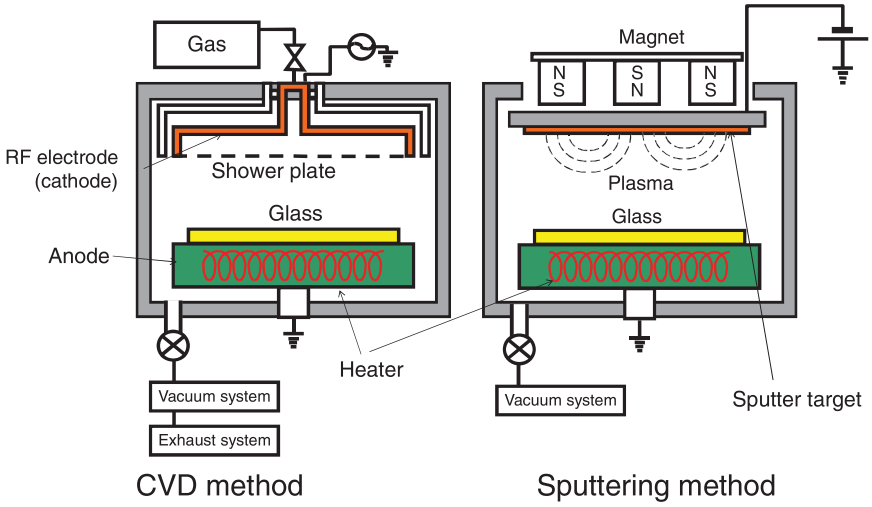


Figure 6.7 Schematic representation of equipments used to form TFT by thin-film deposition: (a) chemical vapor deposition (CVD) method; (b) sputtering method.

the sputtering method have good adhesion properties because the material is deposited with high kinetic energy. As discussed in Section 2.3.7.4, ITO used for anode electrodes needs workfunction control to have smooth hole injection into the OLED device. The workfunction of ITO needs to be close to the HOMO energy level of the organic material, which receives holes. ITO surface modification, such as oxygen plasma, UV-O_3 treatment, or CF_x plasma treatment, is made to have a workfunction deep enough to inject holes. Also, a liquid solution treatment is used to clean the surface and to deepen the workfunction to match with the HOMO of the organic layer. The roughness of the ITO is also an important factor. As the films of organic materials used to make OLEDs are very thin, the ITO needs to have a very flat and smooth surface. The roughness of ITO used for OLED is usually less than a few nanometers measured by AFM. To achieve this, some manufacturers use polished ITO. Amorphous ITO deposition and successive annealing is also used to achieve a smooth surface.

6.2.3 Patterning Technique

In Section 6.2.1, the film formation process was discussed. The deposited film is patterned by a set of processes called PEP (photoengraving process) as shown in Figure 6.8.

Photoresist resin is coated on the deposited film by spin coating or slit coating. The photoresist type that is removed by photoexposure is called *positive-type resist*. On the other hand, the photoresist that remains following photoexposure is called *negative-type resist*. Positive-type resist is more

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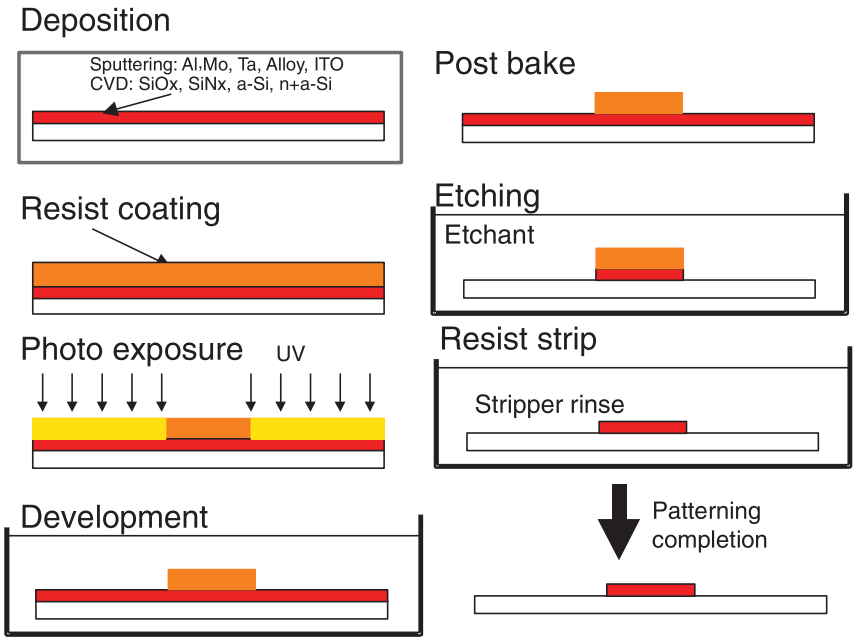


Figure 6.8 Flowchart of patterning process (photoengraving process [PEP]) for TFT fabrication.

popular than negative-type resist because a particle on the negative-type resist causes removal of the film underneath the particle in the etching process and results in an electrical short between the layers, while positive-type does not, and also because the pattern dimension does not change very much and remains accurate in terms of positive type. (Negative-type resist is used in color filters and organic black matrix layers, as such high-optical-density films cannot be sufficiently photoexposed to be removed if the resist is of the positive type.)

Most positive-type photoresist uses naphthoquinone diazide (NQD) as the photoreactive agent. Novolac resin and NQD, which are contained in positive-type photoresist, do not dissolve in an alkaline solution (the presence of NQD inhibits dissolution of the Novolac polymer due to hydrogen bonding between Novolac and NQD); however, with UV irradiation, NQD is transformed to indene carboxylic acid, which dissolves in an alkaline solution (containing, e.g., tetramethylammonium hydroxide [TMAH]) and the photoresist is patterned (Figure 6.9).

Figure 6.10 shows photoexposure equipment for resist patterning. A mercury lamp is used as a light source for the exposure. There are two types of exposure equipment: one that exposes the whole substrate simultaneously and

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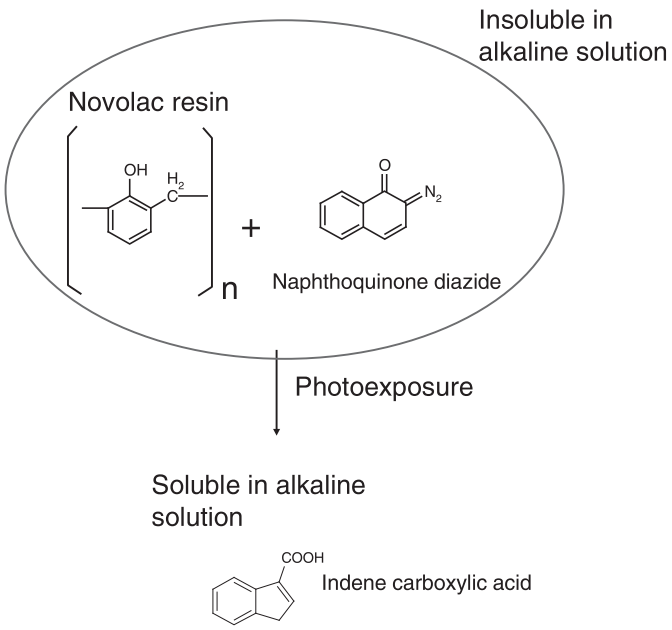


Figure 6.9 Reaction mechanism of positive resist.

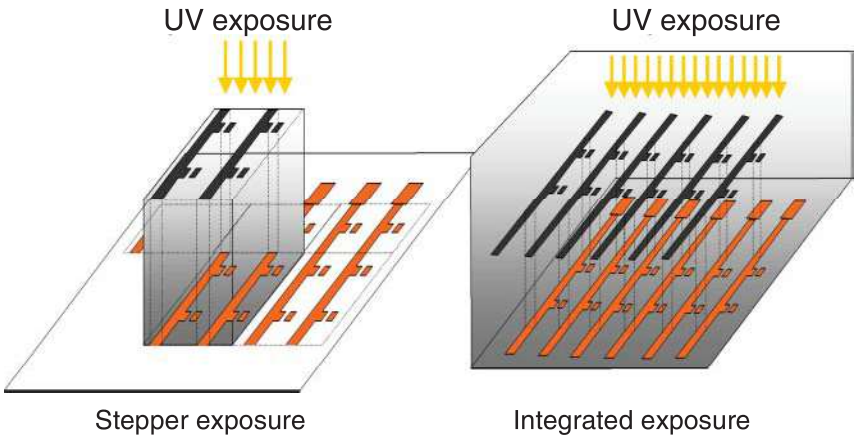


Figure 6.10 Photoexposure tools for resist patterning: (a) stepper exposure; (b) integrated exposure.

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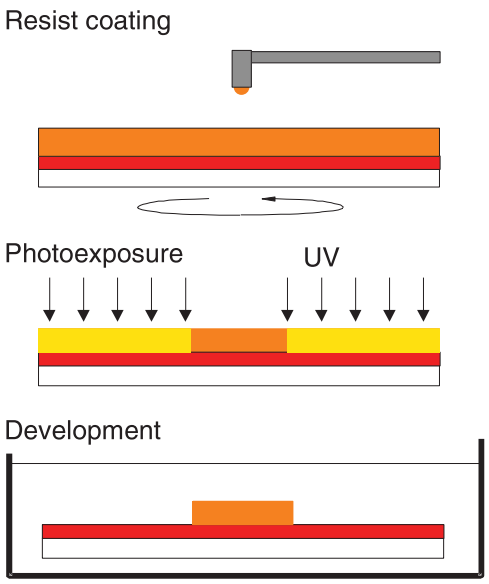


Figure 6.11 Flowchart of resist pattern formation process: (a) resist coating; (b) photoexposure; (c) development.

another that exposes areas consecutively. A mercury-vapor lamp emits line spectra including *G*-line, *H*-line, and *I*-line. The *G*-line (436 nm) is the most popular, but other wavelengths are also used. For the planarization layer and color filter patterning, a broad spectrum containing the *G*-, *H*- (405 nm), and *I*-lines (365 nm) is used. For fine patterning or planarization-layer patterning, the *I*-line is useful.

After the photoexposure (Figure 6.11a and b) stages, the target resist pattern is immersed in an alkaline solution. The film area with no photoresist coating is removed by dry or wet etching, and the film pattern is formed (Figure 6.12).

Dry etching is a method to remove a film region by chemical reaction and ion bombardment. The method is carried out in vacuum chamber and is capable of defining small feature size. However, it is normally higher cost than wet etching due to high tool cost and low throughput. It also has demerits such as poor selectivity (discussed later) and potential radiation damage. In the case of wet etching, chemical reaction etches off the film and is carried out in the bath placed in the atmospheric environment. It is lower cost than dry etching. Higher etching rate and good selectivity for most materials can be obtained. As it is isotropic etching, it is not adequate for defining small feature size [2].

Commonly used gases for dry etching are as follows [2]:

- CF_4, SF_6, and $BCl_2 + Cl_2$ for silicon
- $CHF_3 + O_2$ and $CF_4 + H_2$ for SiO_2
- —$CF_4 + O_2$ (H_2) or CHF_3 for Si_3N_4.

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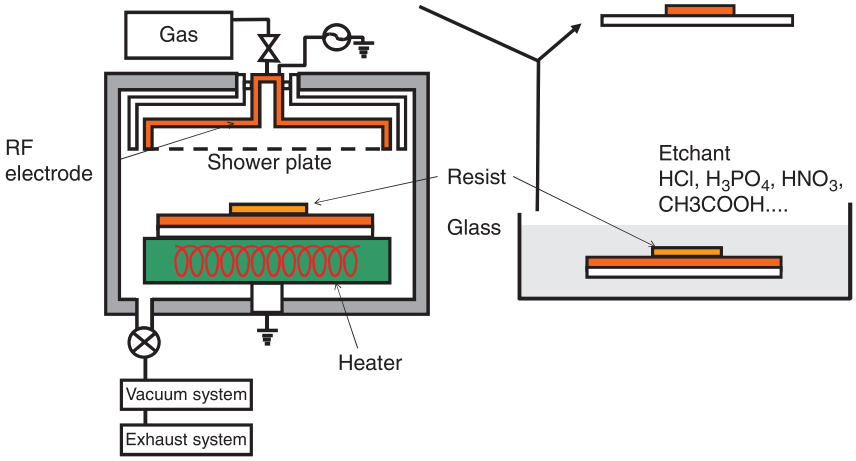


Figure 6.12 Schematic representation of film etching methods.

Commonly used etchants for wet etching are as follows [2]:

- HF and BHF for SiO_2
- HF, BHF, and H_3PO_4 for Si_3N_4
- $HCL + H_2O$ and NaOH for Al.

It is important to select the appropriate dry-etching gas (e.g., CF_4 gas etches Si_3N_4 but does not etch aluminum) or appropriate wet etchant so that the etching rate of the film to be etched is large enough compared with the etching rate of the layer beneath in order to pattern the film without damage to the underlying layer. (The etching speed differential between the layers is called the *etch selectivity*.) Photoresist is also used as a planarization layer as shown in Figure 6.13. After TFT formation, the surface becomes bumpy due to the film pattern. However, OLED films to be deposited on it are very thin (a few tens of nanometers), so the bumpy surface profile can cause OLED film pinholes, which causes an electric short between cathode and anode. A planarization layer is used to help circumvent this issue. A planarization layer also reduces the parasitic capacitance between electrode and TFT wiring so that the aperture ratio can be increased by shortening the electrode to wiring distance.

6.2.4 Excimer Laser Crystallization

Several different crystallization methods for silicon film are used, depending on how energy is applied to the film. One approach consisting of crystallization of silicon film by annealing is called *solid-phase crystallization* (SPC). As shown in Figure 6.14, the crystal grain grows from the crystalline seed, which serves as a growth center.

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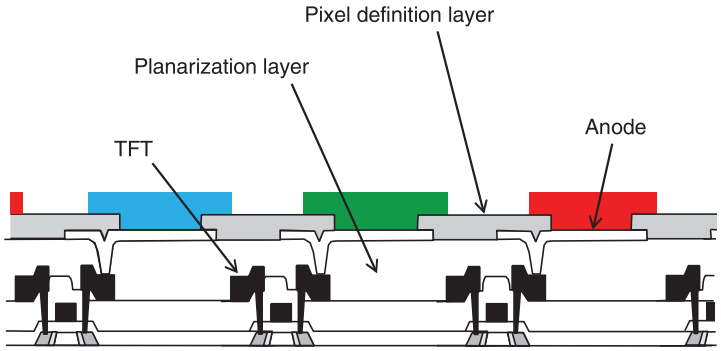


Figure 6.13 An example of a planarization layer for active-matrix OLED display pixels.

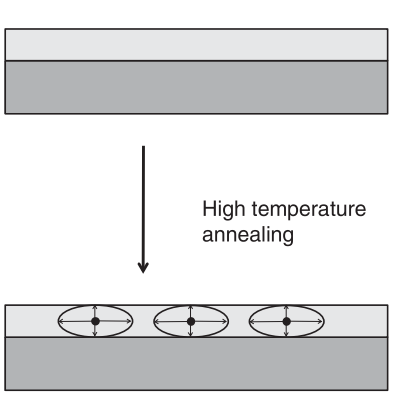


Figure 6.14 Schematic representation of polysilicon formation by the solid-phase crystallization (SPC) method.

As the use of glass substrates for OLEDs or LCDs is problematic at high temperatures, for example, strain point of 669 °C for Eagle-XG® glass substrate, while solid-phase crystallization temperature of noncrystalline silicon is over 700 °C [3]), several technologies have been developed to decrease the crystallization temperature. One of the most popular approaches is laser annealing [4, 5], which provides energy by absorption of a laser beam within the silicon film to decrease the effective temperature of the glass substrate when Si is molten. Another popular approach is metal-induced crystallization (MIC), which decreases the crystallization temperature by using nickel as a crystallization seed that has the same body-centered cubic (BCC) lattice as does a silicon crystal (see Section 6.1). These are termed *low-temperature polysilicon* (LTPS) processes, as the temperature is lower than that of the normal crystallization of silicon.

ELA is the most popular among all the low-temperature crystallization processes. An excimer laser irradiates the silicon film by transmitting a pulsed (several tens of nanoseconds) light beam of 308 nm wavelength generated by

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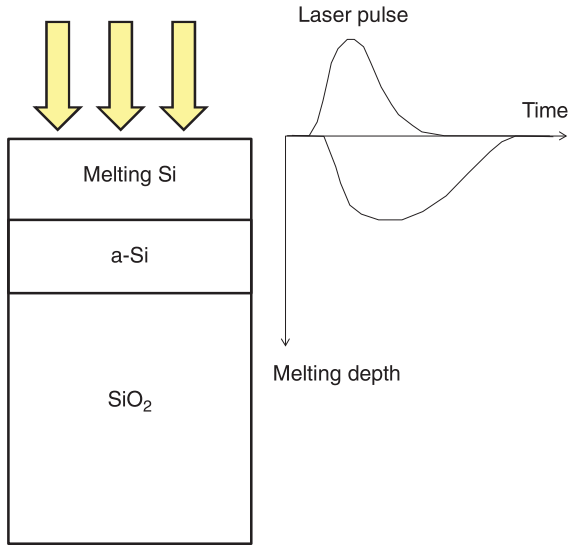


Figure 6.15 Schematic illustration of the principle of laser annealing crystallization.

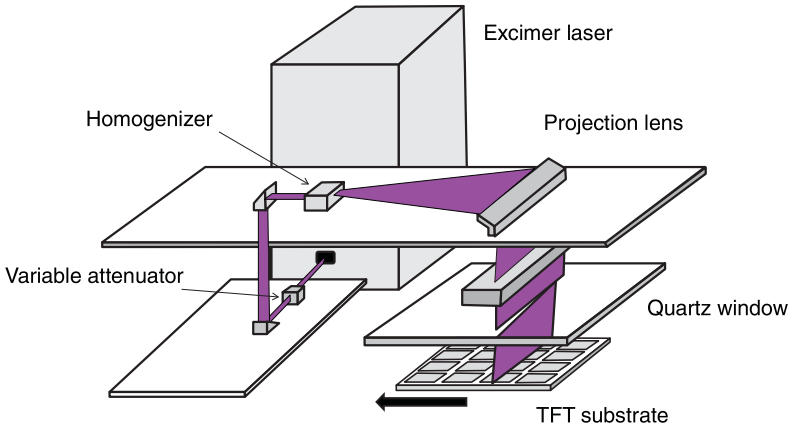


Figure 6.16 Schematic representation of apparatus used for excimer laser annealing crystallization.

XeCl, which increases the local silicon film temperature to above the melting point of silicon (Figures 6.15 and 6.16). As the film is locally heated, glass substrates that cannot withstand temperatures above 600 ~ 700 °C can be used.

Figure 6.17 shows the dependence of laser irradiation energy on crystal grain size due to ELA. As the irradiation energy increases, grain size also increases (from region *A* to *B*); however, at a certain energy level, the crystal grains acquire a fine granular shape (in region *C*). This is because the mechanism

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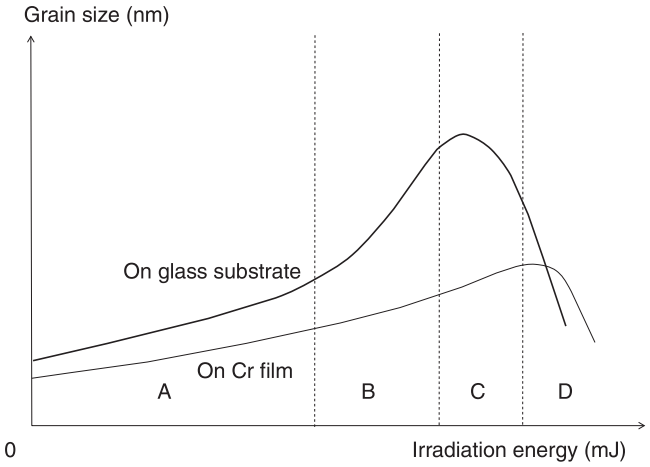


Figure 6.17 Graphical depiction of dependence of laser irradiation energy on crystal grain size.

changes in response to the supercooling process, in which the silicon film maintains itself in the molten state even after the temperature drops below the solidification point. In this state, as the temperature decreases, solidification suddenly begins. TFT characteristics such as mobility and *S* value (subthreshold slope) are improved as the grain size increases in region *B*, as shown in Figure 6.18. To ensure adequate performance, it is necessary to maintain region *B* conditions during manufacturing.

In terms of the laser, energy density is not uniform in a beam. In particular, the energy at the beam edge tends to differ widely (lower energy) from that at the center. To avoid any change in TFT characteristics at the beam edge, the beam location is shifted for every pulse to form an overlap region (e.g., 90% overlap) with the previous pulse. As a result, the same location receives multiple pulses in short time. A multibeam shot provides the advantage of grain size enlargement (Figure 6.19) but with the trade-off of lower manufacturing throughput. (To avoid this problem, the sequential lateral solidification [SLS] method has been introduced. The method is discussed in Section 6.5.1.1.)

6.3 MOSFET BASICS

Figure 6.20 shows transistor behavior in linear region operation [6]. A transistor that switches on and off depending on the gate electrode potential is called a field effect transistor (FET). Especially, an FET whose channel conductance is modulated by the gate electrode placed across the dielectric layer is called a

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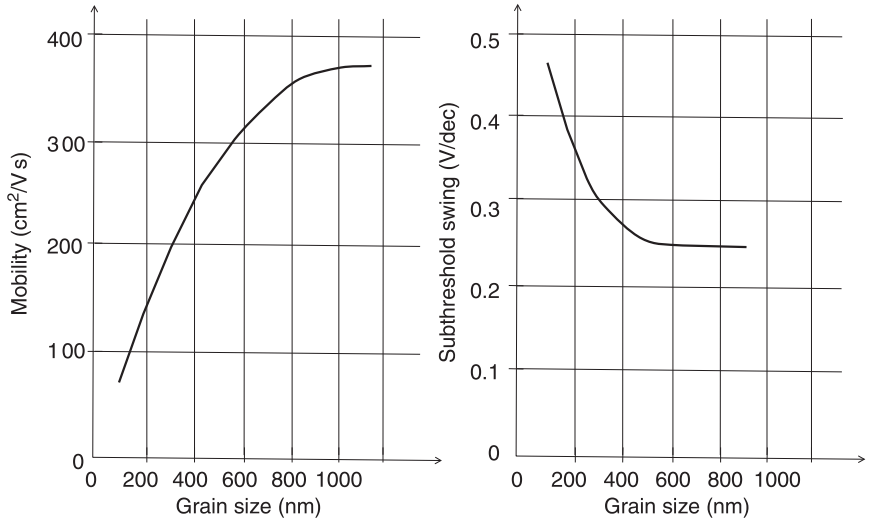


Figure 6.18 Plots showing correlation between crystal grain size and TFT characteristics.

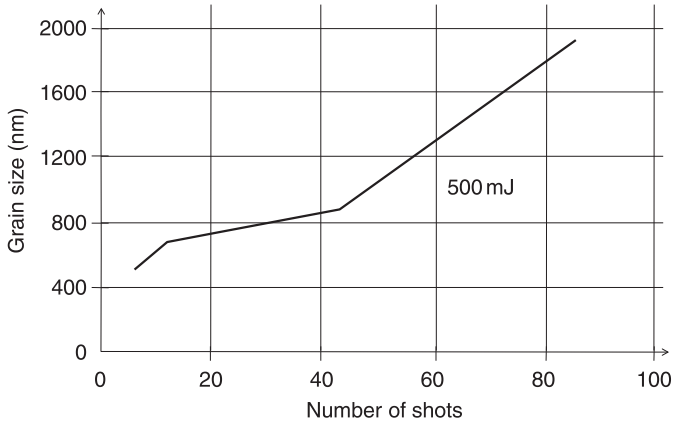


Figure 6.19 Graphical representation of correlation between laser shot number and crystal grain size.

metal oxide semiconductor field effect transistor (MOSFET) or metal insulator semiconductor field effect transistor (MISFET).

When V_{GS} (gate–source voltage; $V_G - V_S$) is higher than the threshold voltage (V_{th}), electric current is generated by V_{DS} (drain–source voltage; $V_D - V_S$). Here, we assume that $V_S = 0$ (source potential) and $V_B = 0$ (substrate potential). Also, the potential at coordinate y relative to the source potential is assumed to be $V_C(y)$. It is also assumed that V_{th} is the same in all locations in the channel

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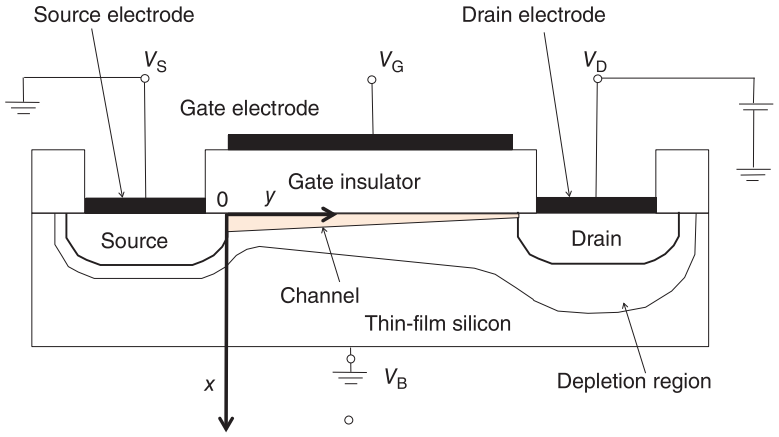


Figure 6.20 A schematic diagram of N-channel transistor operation in the linear region.

and that the y-axis electric field is dominant and the x-axis electric field is minor. This assumption is called *gradual-channel approximation*.

The following condition is also assumed:

$$V_{GS} > V_{th} \tag{6.1}$$

$$V_{GD} = V_{GS} - V_{DS} \geq V_{th} \tag{6.2}$$

The boundary condition can be expressed as

$$V_C(y = 0) = V_S = 0 \tag{6.3}$$

$$V_C(y = L) = V_{DS} \tag{6.4}$$

When the total charge in the channel is $Q(y)$, then

$$Q(y) = -C_{Ox}\{V_{GS} - V_C(y) - V_{th}\} \tag{6.5}$$

If surface mobility is μ, the resistance dR caused by a small region dy in the channel can be expressed as follows:

$$dR = -\frac{dy}{W\mu Q(y)} \tag{6.6}$$

$$dV_C = I_D dR = -\frac{I_D\, dy}{W\mu Q(y)} \tag{6.7}$$

Integrating from $y = 0$ to $y = L$ (channel length), we obtain

$$\int_0^L I_D\, dy = -W\mu \int_0^{V_{DS}} Q(y) dV_C \tag{6.8}$$

So

$$I_D = \frac{\mu C_{Ox}}{2}\frac{W}{L}\{2(V_{GS} - V_{th})V_{DS} - V_{DS}^2\} \tag{6.9}$$

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Thus, the drain current in the linear region ($V_{DS} < V_{GS} - V_{TH}$) can be expressed as

$$I_D = \mu C_{OX} \frac{W}{L} \left\{ (V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right\} \tag{6.10}$$

Here, μ is mobility, V_{th} is threshold voltage, C_{OX} is gate insulator capacitance per unit area, and W and L are channel width and channel length, respectively.

On the other hand, when V_{DS} is larger than $V_{GS}-V_{th}$, the channel disappears at the pinchoff point and the drain current does not increase, even with larger V_{DS} (saturation region operation). The current is equal to the current of

$$V_{DS} = V_{GS} - V_{th} \tag{6.11}$$

so, substituting Eq. (6.11) for Eq. (6.9), we can express the drain current in the saturation region as

$$\begin{aligned} I_D &= \frac{\mu C_{Ox}}{2} \frac{W}{L} \{2(V_{GS} - V_{th})(V_{GS} - V_{th}) - (V_{GS} - V_{th})^2\} \\ &= \frac{\mu C_{Ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 \end{aligned} \tag{6.12}$$

6.4 LTPS-TFT-DRIVEN OLED DISPLAY DESIGN

In this section, we discuss methods for designing a high-quality display with OLED devices.

6.4.1 OFF Current

One problem with an LTPS-TFT is high leakage current. The leakage current is caused by insufficient charge blocking capability of the contact region formed between the intrinsic region (nondoping region; also called the *i*-layer) and the doped region created by ion doping.

As shown in Figure 4.33, most pixel circuits contain a switching TFT, which relays the grayscale signal to the pixel, and a driver TFT, which causes electric current to flow to the OLED device for emission. The driver TFT does not need very low leakage current; however, if the switching TFT has a high leakage current, the pixel capacitor cannot retain the signal level for accurate OLED device emission, and an abnormal display image or crosstalk may result.

To suppress the leakage current of TFTs, an alternative method is to employ a double-gate structure [7] (Figure 6.21) that connects two TFTs in series or a multigate structure that connects multiple TFTs in series. (*Note*: The term *double-gate structure* can also refer to a TFT containing both top-gate electrode and bottom-gate electrodes; this term is confusing, so we must note the context when we find it.)

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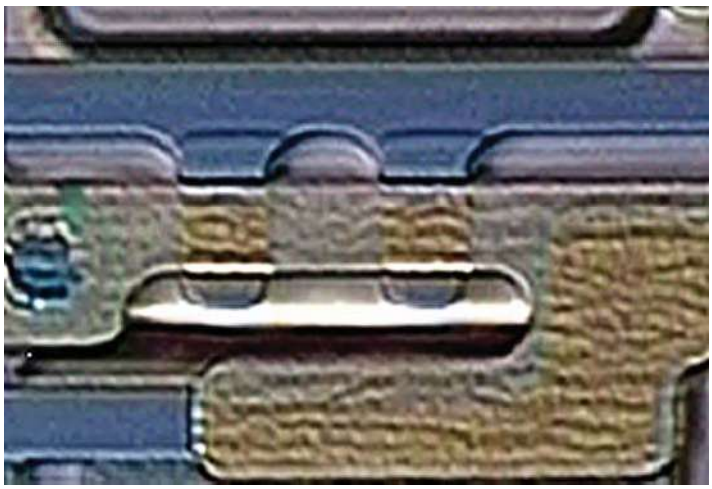


Figure 6.21 Photographic image of a double-gate TFT structure.

Also, as an N-channel LTPS-TFT normally has a high leakage current, a lightly doped drain (LDD) structure such as that shown in Figure 6.4 is often used [8]. Figure 6.22 plots the correlation between LDD length and TFT characteristics. As the LDD length increases, the OFF current is largely decreased. However, the ON current also decreases proportionally with the increase in the LDD length, so this is potentially a trade-off situation. Optimum LDD length should be chosen for the best design. LDD structure is also effective to avoid the reliability problem caused by the hot carriers, induced by the strong electric field between gate and drain. By applying an N-doping layer, the gate to drain electric field is weakened so that the damage due to hot carriers is diminished.

6.4.2 Driver TFT Size Restriction

An OLED device is driven by electric current, and to satisfy the luminance specification with respect to visibility in ambient environment conditions, a large current is necessary. Here, we explain the TFT characteristics necessary for this purpose.

The electric current necessary to drive a pixel can be expressed as

$$I_{\text{pixel}} = \frac{L_{\max} \times 9a^2}{\eta} \tag{6.13}$$

where $L_{\max}$ is the maximum display luminance, I_{pixel} the maximum current that flowing through OLED diode, η the current efficiency of OLED diode, and a the subpixel pitch.

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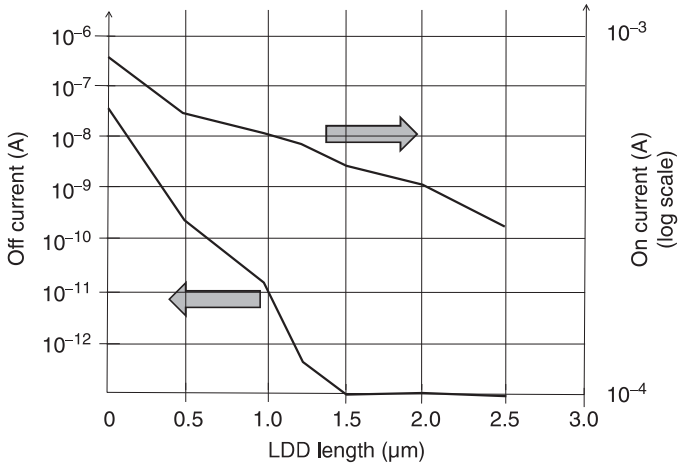


Figure 6.22 Graph depicting correlation between lightly doped drain (LDD) length and TFT characteristics.

According to Eq. (6.12), maximum current at a certain drain voltage can be described as

$$I_{\text{pixel}} = \frac{W}{2L}\mu C_{\text{Ox}}(V_{\text{GS}} - V_{\text{th}})^2 \tag{6.14}$$

where W is the driver TFT channel width, L the driver TFT channel length, μ the TFT mobility, C_{OX} the TFT channel capacitance, V_{GS} the TFT gate voltage, and V_{th} the threshold voltage.

Therefore,

$$W = \frac{18L_{\max}a^2L}{\eta\mu C_{\text{Ox}}(V_{\text{GS}} - V_{\text{th}})^2} \tag{6.15}$$

As W increases, the aperture ratio decreases in the bottom emission device, so OLED degrades more rapidly because of an increase in the current density flowing through the OLED device. An excessively high W value is considered to be disadvantageous for an OLED display, as large TFT creates much overlap region between electrodes, which increases the probability of failure due to short defects. To ensure good yield, it is necessary to design a TFT whose size is not unwieldy compared with amorphous silicon TFT-LCD, which uses a narrow channel width (e.g., $W = 20\,\mu\text{m}$).

6.4.3 Restriction Due to Voltage Drop

As an OLED is a current-driven device, it is very important to take voltage drop (Figure 6.23b) into account in designing a large display.

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(a)



(b)

Figure 6.23 Images of displays (a) without voltage drop and (b) with severe voltage drop.

Current flowing in a supply line can be described as

$$I_{\text{supply}} = 3mI_{\text{pixel}} \tag{6.16}$$

where m is the number of pixels along the horizontal direction.

Wiring resistance can be expressed as

$$R_{\text{supply}} = \frac{3ma\rho_{\text{supply}}}{d_{\text{supply}}W_{\text{supply}}} \tag{6.17}$$

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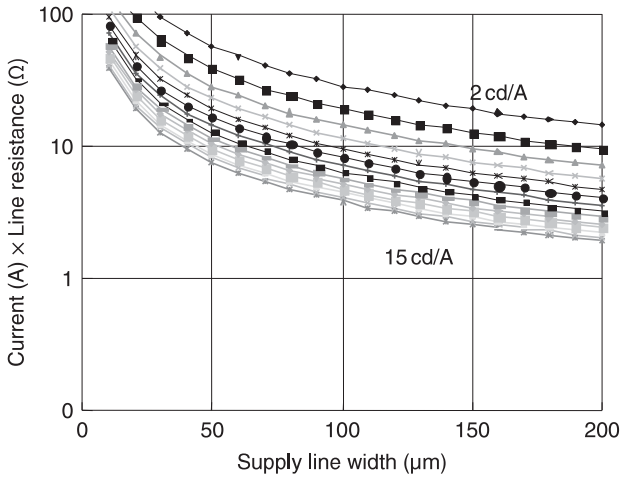


Figure 6.24 Voltage drop simulation results, assuming wiring with same parameters as those in LCDs.

where ρ_{supply} is the resistivity of supply line, d_{supply} the thickness of supply line, and W_{supply} the width of supply line.

Then the maximum voltage drop that can occur during display driving is

$$V_{\text{drop}} = I_{\text{supply}} R_{\text{supply}} = 9m^2 I_{\text{pixel}} a \frac{\rho_{\text{supply}}}{d_{\text{supply}} W_{\text{supply}}} \tag{6.18}$$

If standard resistivity value, thickness, and line width used for the LCD display are assumed, then a serious voltage drop such as that graphed in Figure 6.24 can occur. For example, if $\rho_{\text{supply}} = 4\,\mu\Omega \cdot \text{cm}$, $W_{\text{supply}} = 5\,\mu\text{m}$, $d_{\text{supply}} = 200\,\text{nm}$, and $I_{\text{pixel}} = 10\,\mu\text{A}$, then the maximum voltage drop along the supply line can be calculated as $V_{\text{drop}} = 4.22\,\text{V}$ (as shown in Figure 6.23), which is a serious problem for displaying images.

To avoid problems related to voltage drop, OLED efficiency improvement, such as the use of a phosphorescent emitter, an outcoupling enhancement, or low-resistance wiring, consisting of aluminum or copper at low impurity concentrations, is necessary.

The use of low-impurity wiring material, increase in wiring thickness with improved gate insulator coverage, increase in wiring width, and an improved driving technique can reduce the voltage drop and provide sufficient luminance uniformity, as shown in Figures 6.25 and 6.26. In particular, to achieve low-resistance wiring, taper angle control is very important in order to ensure gate insulator coverage for high production yields.

Using Eq. (6.18), we obtain

$$V_{\text{drop}} = I_{\text{supply}} R_{\text{supply}} = 9m^2 I_{\text{pixel}} a \frac{\rho_{\text{supply}}}{d_{\text{supply}} W_{\text{supply}}} \tag{6.19}$$

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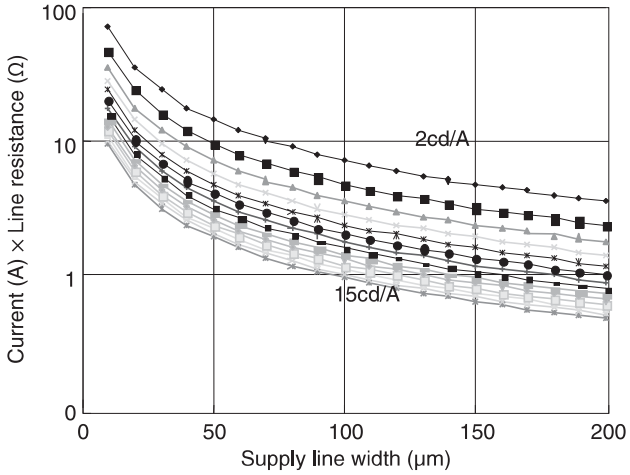


Figure 6.25 Plot showing voltage drop reduction with increase in wire thickness.

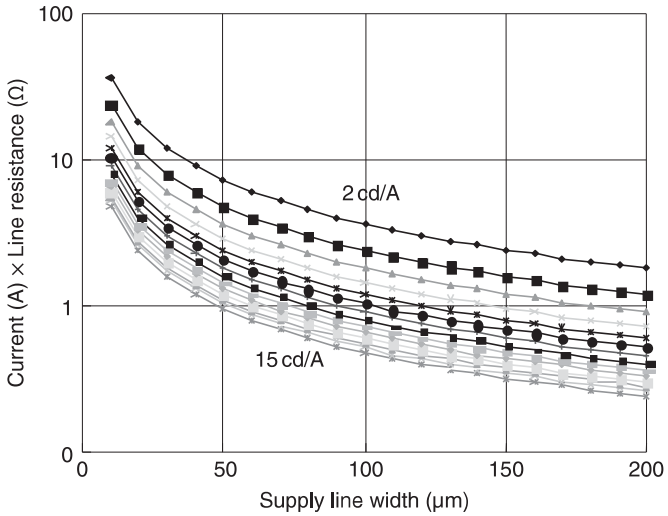


Figure 6.26 Plot showing voltage drop reduction with increase in wire thickness in a low-resistivity wiring material.

Using Eq. (6.13), we obtain

$$I_{\text{pixel}} = \frac{L_{\max} \times 9a^2}{\eta} \tag{6.20}$$

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Therefore, voltage drop can be described as

$$V_{\text{drop}} = 81m^2a^3\frac{\rho_{\text{supply}}L_{\max}}{d_{\text{supply}}W_{\text{supply}}\eta}. \tag{6.21}$$

where m is the number of pixels along the horizontal direction, α the pixel pitch, ρ_{supply} the resistivity of supply line, $L_{\max}$ the maximum luminance of display, d_{supply} the thickness of supply line, W_{supply} the width of supply line, and η the current efficiency of the OLED diode.

If the supply line width is proportional to the display size, then

$$W_{\text{supply}} = aW_0 \tag{6.22}$$

and

$$V_{\text{drop}} = 81m^2a^2\frac{\rho_{\text{supply}}L_{\max}}{d_{\text{supply}}W_0\eta} \tag{6.23}$$

When display resolution is constant, pixel pitch is proportional to the display size; therefore, Eq. (6.23) indicates that voltage drop is proportional to the square of the display size.

Therefore, to achieve a voltage drop equivalent to a 20-in. display, a 30-in. display needs to reduce the $\rho_{\text{supply}}/d_{\text{supply}}\eta$ value by $\left(\frac{20}{30}\right)^2 = \frac{1}{2.25}$ times; a 40-in. display by $\left(\frac{20}{40}\right)^2 = \frac{1}{4}$ times; and a 50-in. display by $\left(\frac{20}{50}\right)^2 = \frac{1}{6.25}$ times.

To improve the $\rho_{\text{supply}}/d_{\text{supply}}\eta$ value, tandem OLED technology (discussed in Section 2.6.3) is useful. Figure 6.27 shows the structure of a hypothetical bottom emission device. Using an N-unit tandem OLED device, the operating voltage drop and electric current stress are reduced to $1/N$, which results in N^n times the lifetime. ($n = 1.2$–1.9 as discussed in Section 2.5. If $n = 1.5$ is assumed, two-stack tandem OLED gives 2.82 times, and three-stack gives 5.20 times the lifetime, theoretically.) For example, a white emission + color filter device, discussed in Chapter 7, might use two units (three units in exceptional cases) from this perspective.

When a multiunit stack is used, voltage applied to the device is high. Driver IC cost is increased rapidly as the "design rule" (minimum width in the semiconductor design) is increased, so the operating voltage of device formulation should be minimized by optimization even with the tandem OLED structure case.

For larger displays, wiring with lower resistivity is necessary. Copper can have low resistivity values $\rho_{\text{supply}} \sim 2 \times 10^{-6}\Omega \cdot \text{cm}$, so $\rho_{\text{supply}}/d_{\text{supply}}\eta$ can be less than half that of aluminum wiring. Combined with tandem structure, very large displays would be possible using these parameters.

As the minimum requirement of any OLED display component is only a TFT glass substrate and a driver IC, an OLED display will be sufficiently

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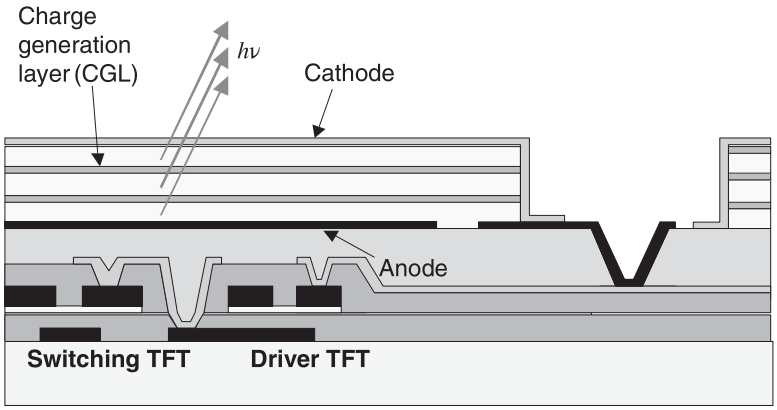


Figure 6.27 Schematic example of an active-matrix-driven tandem OLED structure.

cost-competitive with a large LCD in the near future if the manufacturing infrastructure is sufficiently developed.

6.4.4 LTPS-TFT Pixel Compensation Circuit

The liquid crystal in LCD displays is driven by voltage. (In fact, in the very early stages of LCD development, liquid crystal, e.g., that was used in dynamic scattering-mode LCD, was driven by electric current rather than voltage.) On the other hand, OLED displays are driven by electric current, so small current variations can be distinguished as nonuniformity (*mura*). Thus, a simple driving method using a 2T1C circuit (Figure 4.33), for example, tends to cause yield loss due to mura.

Figure 6.28 shows an example of luminance mura. The human eye is very sensitive to changes in luminance, so if there is driver TFT current nonuniformity in the display area, it is perceived as mura. In particular, LTPS-TFT treated by ELA has a serious mura issue, so various compensation circuits have been proposed and applied in practice.

6.4.4.1 Voltage Programming

The basic principle of V_{th} compensation is to store the driver TFT V_{th} in the gate node as $V_G = V_D + V_{th}$, by connecting gate and drain nodes as shown in Figure 6.29. This principle has been used in various compensation circuits, not only for voltage programming.

Figure 6.30 shows a V_{th} compensation circuit by voltage programming presented by Dawson et al. [9]. This circuit is thought to be the prototype of most subsequent voltage programming compensation circuits [10–15].

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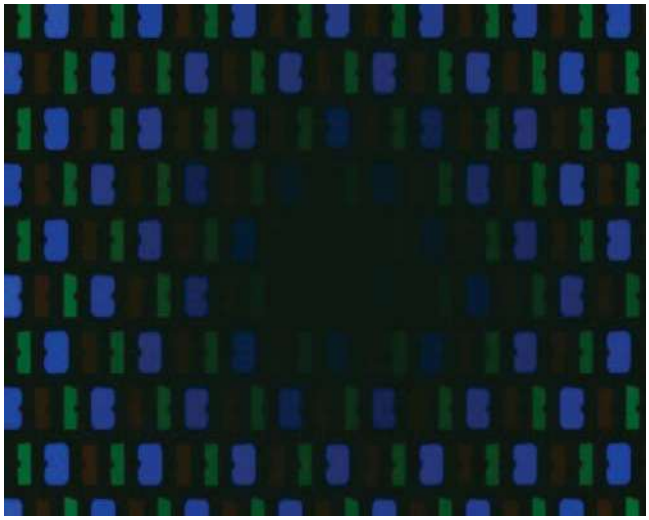
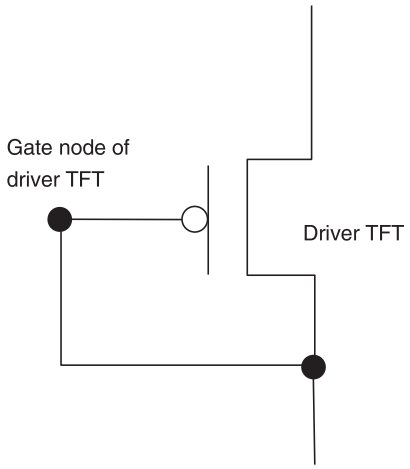


Figure 6.28 Image of luminance mura (nonuniformity) due to variation in threshold voltage.

Figure 6.29 Schematic representation of threshold voltage detection via gate–drain node connection.



Here, we discuss the working principle of the circuit, step by step:

1. The AZ line is set to negative voltage, and MN3 TFT turns on. (Note that the TFT is P-channel.)
2. The gate node and drain node of MN2 are connected and create the same scenario as shown in Figure 6.29, so the gate node of driver TFT (MN2) stores V_{th} information.
3. The data line signal voltage is added to the driver TFT gate node using capacitance coupling of C1.

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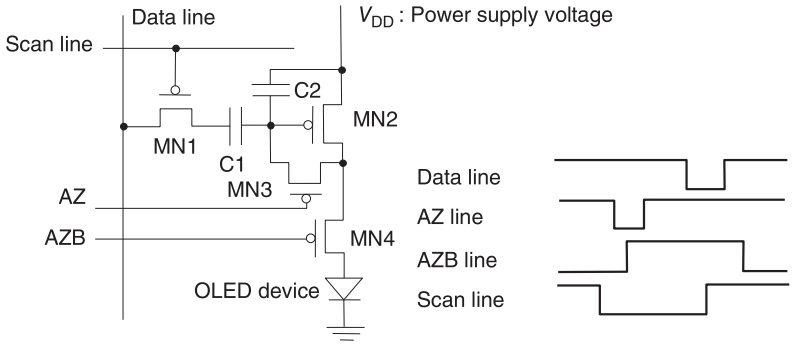


Figure 6.30 Voltage programming circuit drawn by Dawson et al. [9].

4. As the gate node of the driver TFT stores the data line signal plus V_{th}, the source–drain current of the driver TFT does not contain V_{th} information. Therefore, mura (nonuniformity) related to V_{th} variation does not take place, due to the cancellation mechanism.

Voltage programming is the method most frequently used for actual OLED display products. The major reason is that an OLED driver IC is similar to an LCD display driver IC. As many circuit design techniques for LCD drivers can be applied for voltage programming drivers, IC drivers can be designed very easily and are also relatively inexpensive.

On the other hand, IC driver voltage programming has some disadvantages such as the following:

- Inability to compensate for either mobility variation or OLED variation
- Aperture ratio loss due to the occupied space by the programming circuit in the case of bottom emission structure. (Top emission can circumvent this issue.)

Note that the lifetime is proportional to $1/J^n$, as discussed in Section 2.5 (J = current density, $n = 1.2$–1.9). As current density is inversely proportional to the aperture ratio, therefore,

$$\text{Lifetime} \propto \frac{1}{J^n} \propto AR^n$$

If $n = 1.5$, the lifetime becomes only 35% for AR = 50%, 25% for AR = 40%, and 16% for AR = 30%; this is a significant reduction, so a top emission structure is useful to avoid such problems.

6.4.4.2 Current Programming

Figure 6.31 shows one of the most widely known current programming compensations, current mirror pixel circuit designs [16]. The circuit uses four TFTs and one capacitor.

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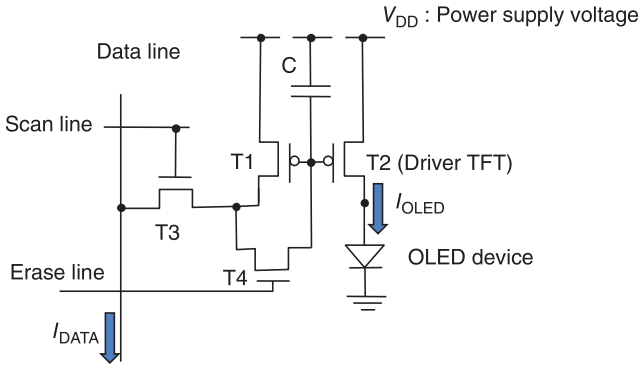


Figure 6.31 Current mirror-type compensation circuit proposed by Sasaoka et al. [16].

Here we assume that the TFT dimension T1 is equal to T2. (In actual implementations, T1 is intentionally designed with a dimension different from that of T2 to reduce the charging time.) Turning on T3 and T4, and also applying current I_{data} to T1, ensures that the gate nodes of T1 and T2 are charged to the target voltage so that the driver TFT can flow current equivalent to I_{data}. This method uses current, not voltage, as a reference, so it can compensate for V_{th} and mobility of the driver TFT and also for any variation in OLED device characteristics.

Although current programming has various advantages, it has drawbacks such as driver IC cost (discussed above), and also its long charging period for low grayscale levels. Several methods have been proposed to address this issue.

6.4.4.3 External Compensation Method

There is minimal change in LTPS-TFT performance during the driving operation. Therefore, mura (nonuniformity) can be corrected by applying an offset to the pixel by the driver IC using a factory-set value. (This is called the *external compensation* method[17, 18].) This method is promising because the cost of memory is steadily decreasing and also necessary frame buffer to store the mura information can be minimized due to the recent evolution of data compression algorithms. The information necessary to correct mura can be obtained by either electrical or optical measurements. Figure 6.32 presents an example of a product using the external compensation method by electrical inspection during the fabrication, referred to as global mura compensation (GMC). Actual uniformity data before and after implementation of the GMC method are shown in Figure 6.33.

Figure 6.34 shows the process flow of the GMC external compensation method.

The manufactured panels are inspected pixel by pixel (actual inspection equipment is shown in Figure 6.35), and the offset data are recorded in

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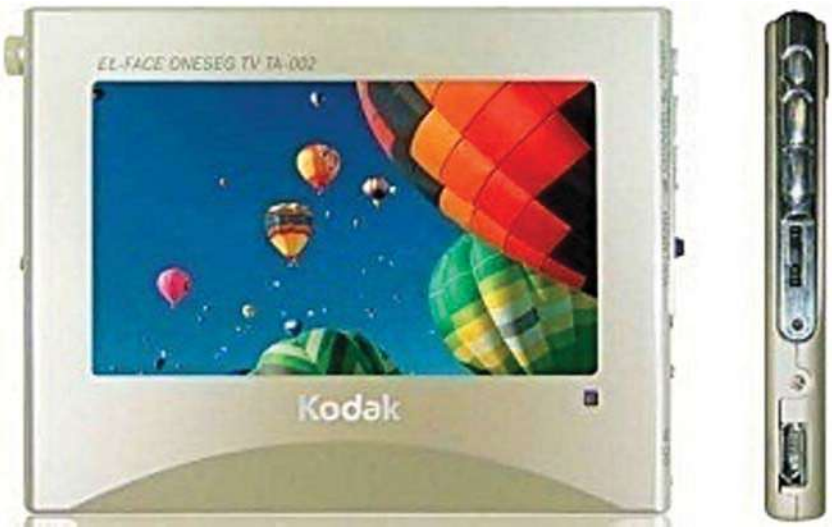


Figure 6.32 A portable television set using the external global mura compensation method (GMC) (by Eastman Kodak).

the memory mounted on each panel. Luminance error (mura) caused by LTPS-TFT current variation can be canceled by calculating the correct driver TFT gate node value (R′, G′, and B′) using an offset measured in the factory when displaying R, G, and B signals on a display.

6.4.4.4 Digital Driving

In most OLED driving methods (analog driving), the TFT is in the saturation region condition, $V_{DS} > V_{GS} - V_{th}$ (where V_{DS} is drain voltage relative to source voltage and V_{GS} is gate voltage relative to source voltage). This is because linear region driving ($V_{DS} < V_{GS} - V_{th}$) causes wide variations in TFT performance. On the other hand, saturation region driving consumes more power than does linear region operation. Normal analog driving applies almost the same source–drain voltage for both OLED and TFT drain. If the linear region method can be adopted, power consumption can be reduced by almost 50%.

To obtain this advantage, digital driving [19, 20] employs time frame modulation; specifically, the driver IC turns the current flow on and off, rather than changing the OLED current by controlling the gate node voltage of the driving TFT.

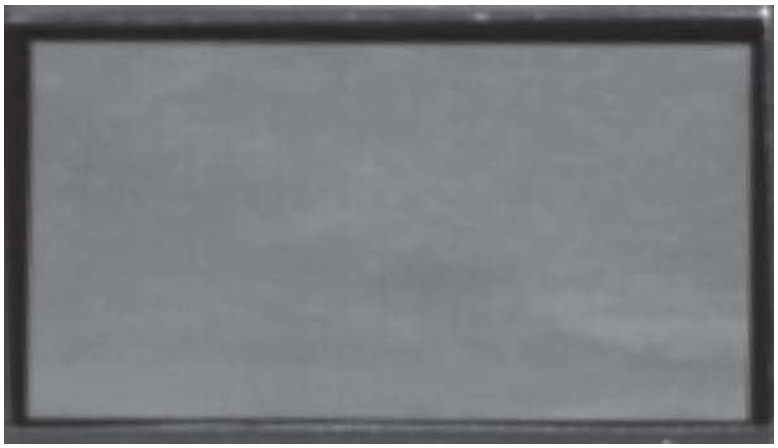
Digital driving resembles plasma display driving in terms of rapid ON/OFF switching, so it has similar issues, such as pseudocontour.

As shown in the upper segment of Figure 6.36, digital driving turns on and off multiple subframes in one frame period. (For a 60-Hz display, $\frac{1}{60} = 16.7$ is one frame period.)

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(a)



(b)

Figure 6.33 Images of luminance variation before (b) and after (a) compensation.

Here, we assume that the Nth line is ON (white) and $(N+1)$th line is OFF (black) during subframe periods 1–4. We also assume that the Nth line is OFF and the $(N+1)$th line is ON during the fifth subframe. In this condition, if the line of sight is moved from the Nth line to $(N+1)$th line, the line of sight remains in the ON region, so a white line is observed. On the other hand, if the line of sight is moved from the $(N+1)$th line to the Nth line, the line of sight line remains in the OFF region, so a black line is observed. This is the crux of the pseudocontour.

Pseudocontour has been effectively addressed in plasma display technology, and there are also many effective driving methods for avoiding pseudocontour

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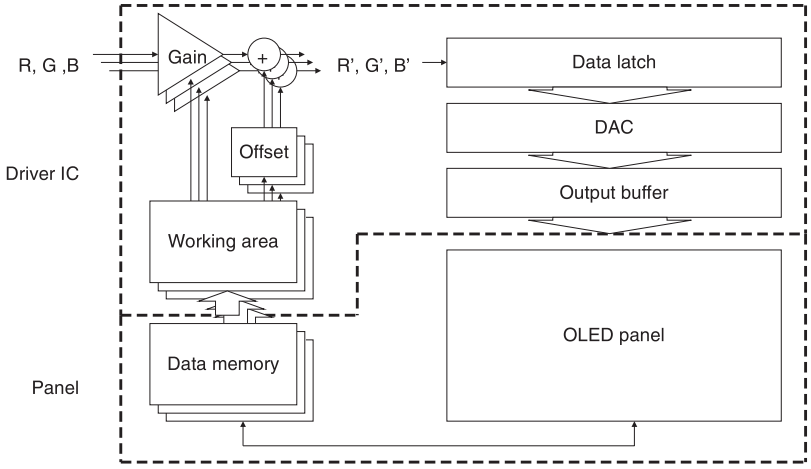


Figure 6.34 Flowchart showing operation of external GMC method.



Figure 6.35 GMC offset measurement equipment used in production.

in OLED displays. In the case of a normal digital driving scheme, a subframe is selected according to a binary number system. In binary number system emission, a consecutive grayscale can have a very different emission timing, so pseudocontour is prominent in such a case because the discontinuous emission occurs when the eye is moved. To circumvent this issue, (1) rearrangement

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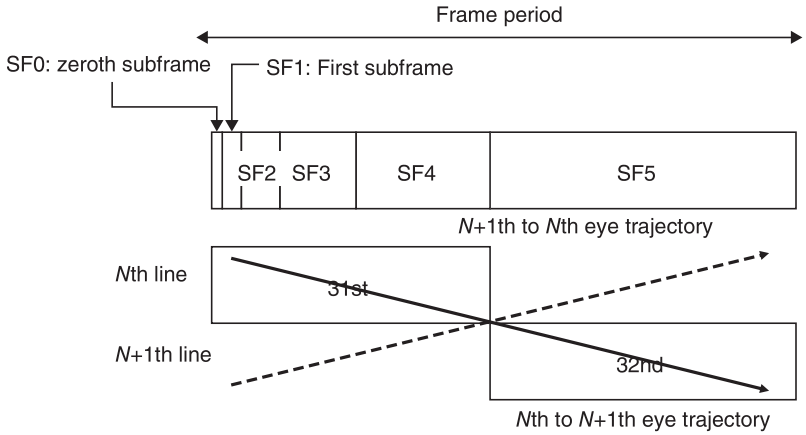


Figure 6.36 Schematic representation of the pseudocontour mechanism.

of subframe and (2) distribution of high-intensity emission in a frame by the error-diffusion method are used so that the pseudocontour becomes less visible to the human eye.

Digital driving has another issue related to the lifetime. In analog driving, resistance of a driver TFT in a pixel is comparable to that of the OLED device, as the driver TFT is driven in saturation region. So when the OLED resistance is increased due to device degradation, the change in voltage drop across the TFT-OLED connection is not very large. However, in the case of digital driving, driver TFT is driven in linear region, so the TFT resistance is much lower than that of analog driving. As a result, TFT-OLED connection voltage drop is much more subjected to the resistance change of the OLED device, so the lifetime of pixel becomes shorter in the case of digital driving. To circumvent this situation, compensation of OLED device degradation has been proposed [21].

As discussed, digital driving has large merit in power reduction. However, due to recent trends toward high resolution, the switching speed is not sufficient for such high resolution, so the actual product implementation of digital driving is decreasing.

6.4.5 Circuit Integration by LTPS-TFT

As LTPS-TFT has a high driving capability, it is possible to form various circuits on substrates, such as shift registers or multiplexers. Figure 6.37 shows an example of an integrated circuit.

A *data driver* circuit is composed of video signals 1–3 (red, green, and blue); a sampling circuit, which delivers video signals to the data line; and a shift register, which controls the timing of the sampling circuit.

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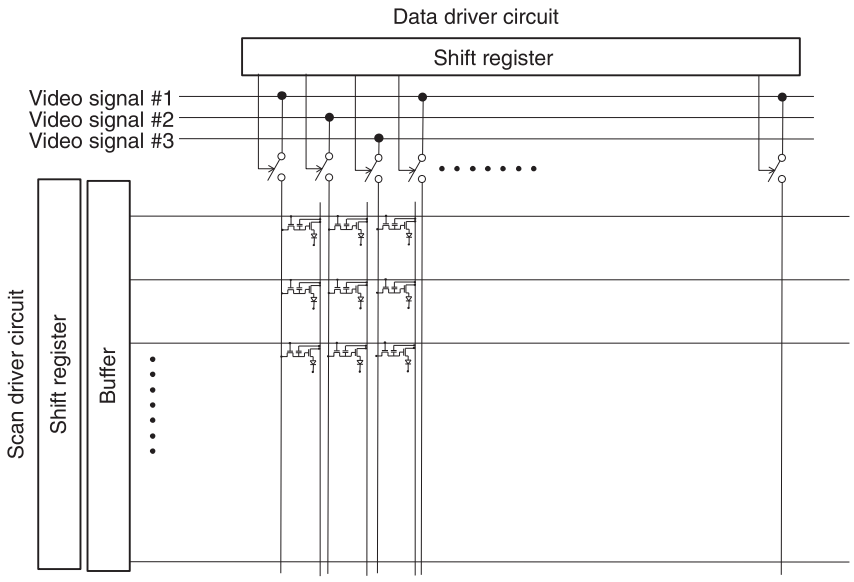


Figure 6.37 Schematic representation of circuit integration using low-temperature polycrystalline silicon (LTPS) TFTs.

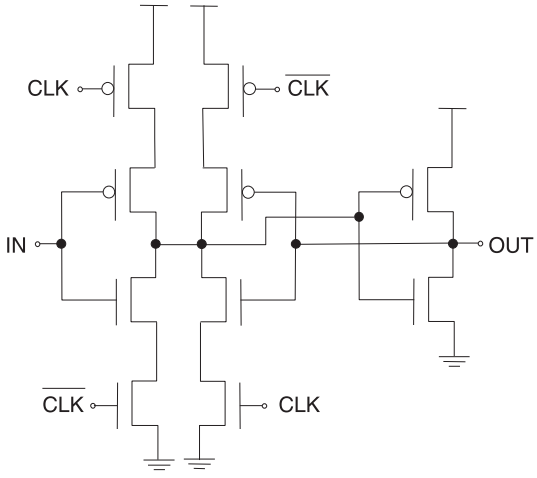


Figure 6.38 Schematic representation of a CMOS-type static shift register.

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A *scan driver* delivers signal to the selected scan line by the shift register via a buffer circuit.

As an example of circuit integration, we shall discuss the shift register circuit. For a shift register, a circuit such as that shown in Figure 6.38 is used for CMOS formats, and circuits such as those shown in Figures 6.39 and 6.40 are for NMOS and PMOS formats.

Although CMOS technology involves many process steps (discussed in Section 6.2.1) and is complicated, with multiple TFTs in the same circuitry, it is capable of driving at speeds exceeding 10 MHz. It also has relatively low power consumption and high reliability.

On the other hand, NMOS and PMOS single-channel technologies can employ short process steps, which is advantageous in terms of cost (see

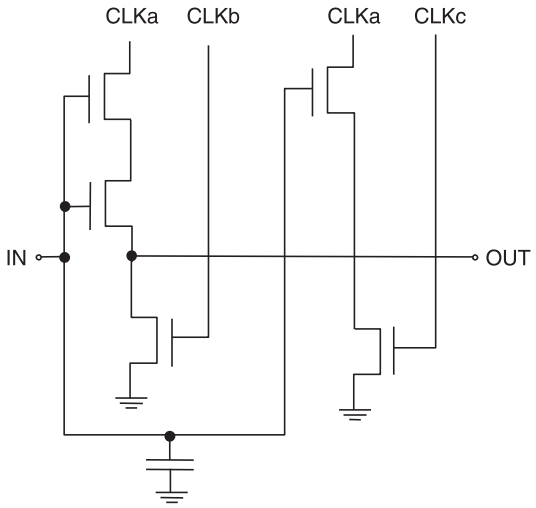


Figure 6.39 Schematic representation of an NMOS-type dynamic shift register.

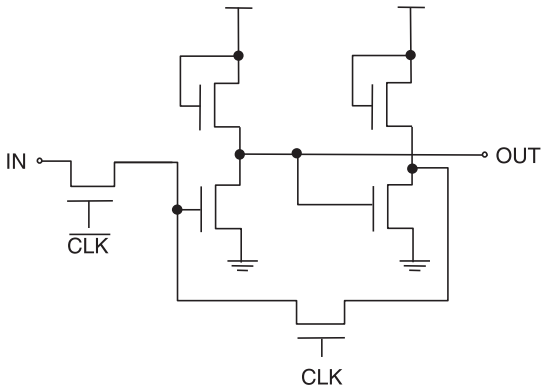


Figure 6.40 Schematic representation of an NMOS-type static shift register.

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Section 6.2.1). However, the driving speed is not very high. For example, the dynamic shift register shown in Figure 6.39 has a driving speed of 2 MHz, and the static shift register shown in Figure 6.40 has a driving speed of 500 kHz.

6.5 TFT TECHNOLOGIES FOR OLED DISPLAYS

There are many difficulties with the LTPS-TFT formation process using ELA, such as laser stability, TFT performance variation, poor laser process productivity, and lack of substrate size scalability. Here we discuss new approaches to these issues.

6.5.1 Selective Annealing Method

Conventional ELA method irradiates laser over whole substrate by step-and-repeat manner, as discussed in Section 6.2.4. However, the area to be crystallized is only TFT channels, so whole-area emission wastes laser power, which reduces the manufacturability. Several methods have been developed to irradiate the laser light only to desired locations.

6.5.1.1 Sequential Lateral Solidification (SLS) Method

The SLS method [22] employs a technique that causes silicon grains to grow perpendicularly to the boundary between the liquefied region (in which laser melting occurs) and the solid region. With this method, the grain sizes that can be obtained are about two- to threefold larger than those obtained by conventional ELA.

The SLS method controls the exposed and unexposed regions of the substrate by means of a mask that has a long line-shaped aperture. Figure 6.41 shows an example of the so-called two-shot SLS method, in which, with the first excimer laser pulse, every alternate location is molten. Crystallization takes place using a precrystallized location as a crystallization seed, so that a long crystal grain can be obtained. Using a narrow laser irradiation width (e.g., 5 μm), any spurious crystallization from the seed beyond the grain boundary can be suppressed, thus ensuring a high-quality large grain. In the SLS method, the energy profile of the beam is almost rectangular, so virtually no energy gradient occurs; thus, no overlap is required, unlike the case with conventional ELA, and this is a major advantage in terms of manufacturing throughput.

This method has been used for many of the small- to-medium-size active-matrix OLED displays on the market.

6.5.1.2 Selective Annealing by Microlens Array

Sugimoto et al. proposed a method to irradiate laser beam using microlens array only to the TFT location using Nd : YAG pulsed laser [23] (Figure 6.42).

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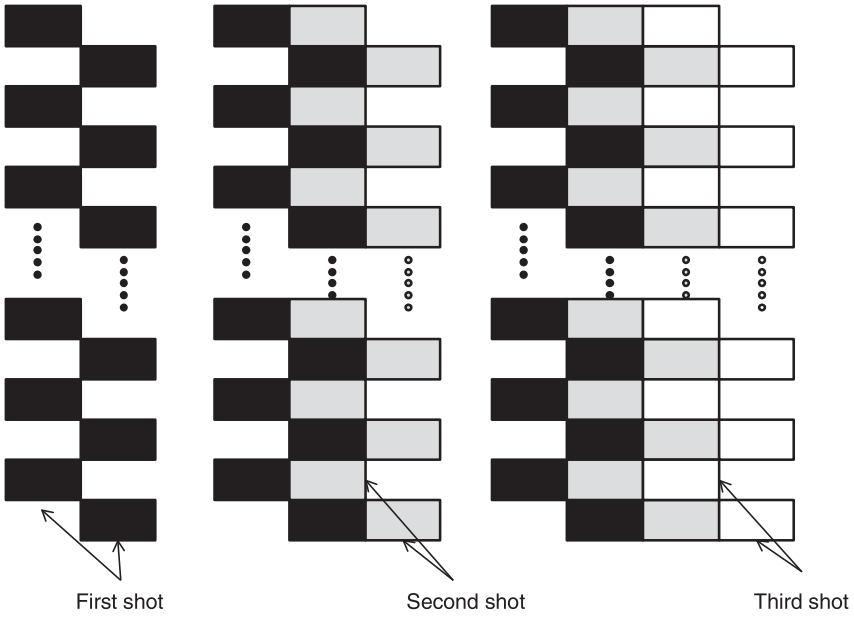


Figure 6.41 Schematic example of a display obtained using the two-shot sequential lateral solidification (SLS) method.

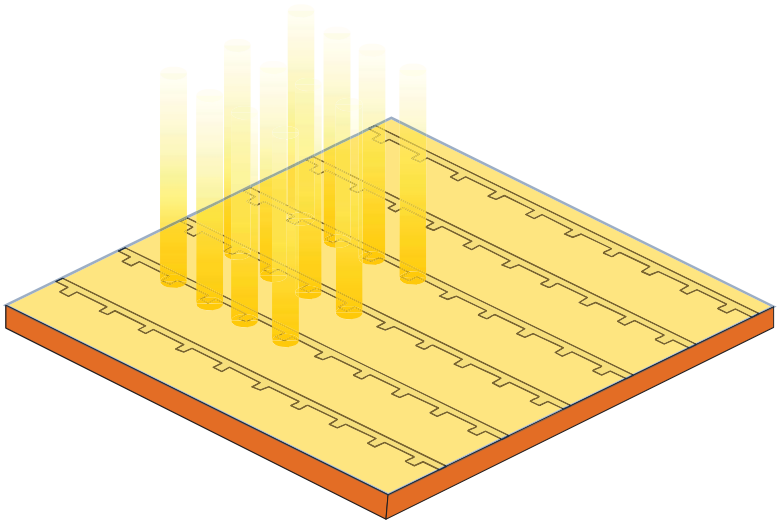


Figure 6.42 Schematic example of the selective annealing process by micro lens array.

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The system also employs a real-time mask alignment system, which enables the system to be applied to very large substrates.

Utsugi et al. presented that Sakai Display Products successfully fabricated LTPS-TFT LCD panel using this method. (PLAS: Partial Laser Anneal Silicon technology) [24]. In the past, due to the size restriction of excimer laser process, largest mother substrate used for LTPS was limited up to generation 6 (1500 mm × 1850 mm) so far when generation 10.5 (2940 mm × 3370 mm) amorphous silicon TFT plant is under construction. The selective annealing method has eliminated one important bottleneck for LTPS to use large substrates.

6.5.2 Microcrystalline and Superamorphous Silicon

The mobility of LTPS-TFT formed by ELA OLED displays fluctuates with various factors such as frequent gas exchange, laser energy instability, and transmittance loss of laser optics due to UV light and electrode degradation, so process maintenance may be problematic with the use of this method. Also, it may be difficult to apply to large substrates because of the laser width restriction due to the laser power limitation.

In 2003, Tsujimura et al. fabricated a 20-in. superamorphous silicon OLED display prototype and proved that large OLED displays could be produced without using excimer laser annealed LTPS-TFT (Figure 6.43) [25].



Figure 6.43 A large OLED display prototype obtained using a non-LTPS substrate (demonstration by IDTech/IBM/CMO in 2003).

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With the parameters $\mu = 0.5\ \text{cm}^2/(\text{V} \cdot \text{s})$ (mobility of amorphous silicon) and $L = 5\ \mu\text{m}$, the necessary TFT channel width should be in the range of hundreds of micrometers, which is larger than the pixel size. It would be possible to incorporate a large TFT in a pixel by zigzag formation, but the defect number might increase due to the long electrodes formed very closely. For this reason, Tsujimura et al. introduced the possibility of reducing the TFT dimensions through mobility improvement by using modified a-Si and introducing microcrystalline Si [26, 27]. It is believed that normal a-Si has too much instability to cope with, so more stable bonding would be necessary. If both high mobility and long-term reliability can be realized, this would represent a major breakthrough in attempts to achieve large AMOLED displays, so it was attempted to improve both Si bonding by low-cost crystallization [28]. Circuit design improvements, such as developing a pixel-level compensation circuit, are also widely discussed to cope with the instability [29, 30]. Instability of a-Si and microcrystalline silicon is mainly due to the threshold voltage shift, so voltage programming discussed in Section 6.4.4 can be applied.

The graph in Figure 6.44 indicates the process condition under which either amorphous silicon (a-Si) or microcrystalline silicon (μc-Si) can be obtained by $SiH_4 + H_2$ gas processing using the PECVD method. As the introduced power is increased, the crystallization ratio improves. Depending on the conditions,

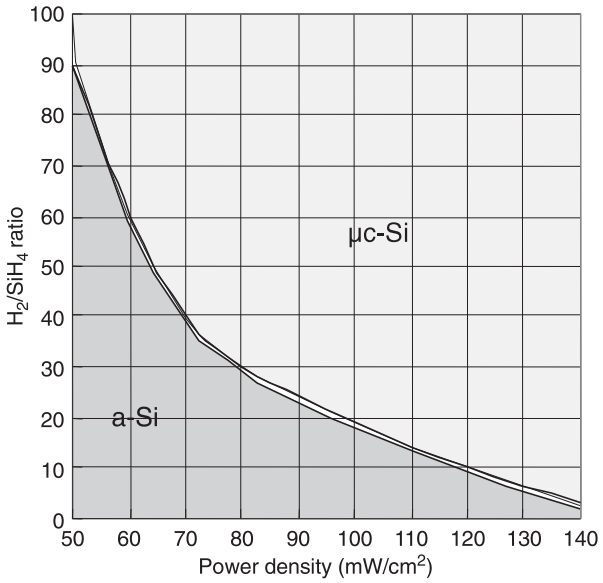


Figure 6.44 Graphical depiction of crystalline condition monitoring using the plasma-enhanced chemical vapor deposition (PECVD) method.

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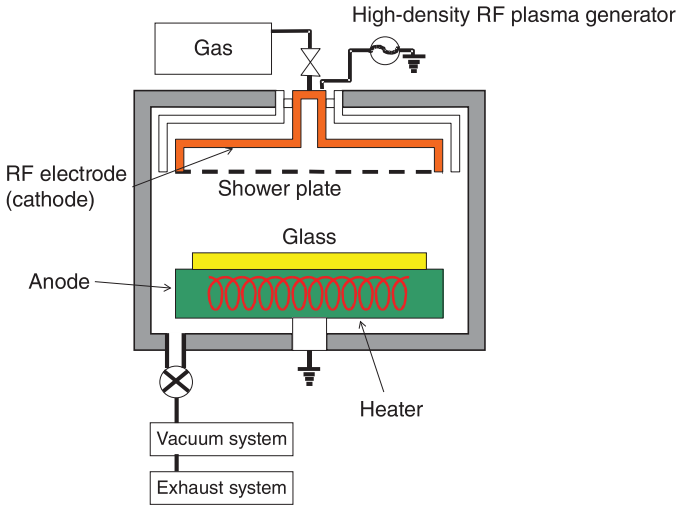


Figure 6.45 Schematic illustration of a high-density plasma CVD apparatus.

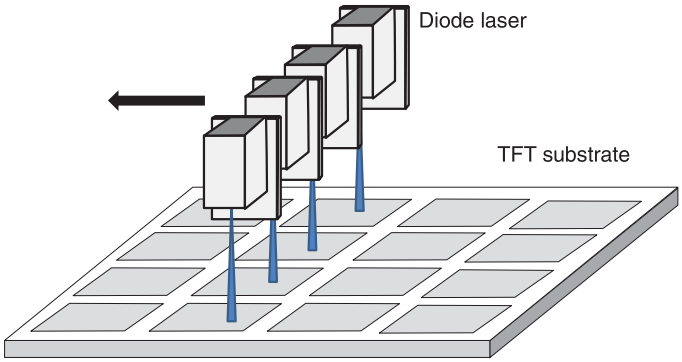


Figure 6.46 Diagram illustrating formation of microcrystalline silicon induced by diode laser annealing.

μc-Si can have higher mobility and better reliability than a-Si (amorphous silicon). Several methods can be employed to form μc-Si, including the layer-by-layer (LBL) method and high-density plasma CVD (Figure 6.45). For such methods, conventional a-Si manufacturing equipment can be used, so it is advantageous from an investment perspective and is also cost-effective because the process step is the same as that in a-Si TFT formation.

Figure 6.46 illustrates equipment used for μc-Si formation by the *diode laser thermal annealing* (DLTA) method, which converts amorphous silicon to microcrystalline silicon by diode laser annealing. In the case of microcrystalline

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silicon formation by PECVD, the process employs deposition and etching simultaneously, so it tends to result in poor thickness distribution and low deposition rate. The DLTA method can be used to avoid such problems, but the number of process steps might increase due to the use of laser annealing and etching-stopper type TFT.

The approach to use amorphous silicon and microcrystalline silicon were used for only several products. However, it was using NMOS TFT, so many development results of amorphous silicon TFT driving, such as NMOS + common cathode device structure in Figure 4.37, anode line structure in Figure 4.38, double-channel structure and pixel compensation circuit were applied to oxide semiconductor (discussed in Section 6.5.4) driving, which became mainstream of OLED television later on.

6.5.3 Solid-Phase Crystallization

Other methods can be employed to achieve the performance between amorphous silicon and laser-annealed polycrystalline silicon; the most popular methods are metal-induced crystallization (MIC) and alternating magnetic field crystallization (AMFC).

6.5.3.1 MIC and MILC Methods

The MIC method [31] applies the theory that the crystallization temperature of silicon in contact with nickel—which has the same body-centered structure as does silicon crystal—is reduced. The MIC method is widely used to control the grain boundary location by controlling the location of Ni seed to ensure crystallization growth in the lateral direction as shown in Figure 6.47. This method to control the grain boundary location by lateral crystalline growth is called *metal-induced lateral crystallization* (MILC). Figure 6.47a shows how crystalline growth takes place from both ends of the channel and then the crystals collide with each other in the center when nickel is deposited on the TFT and annealed. Processes for controlling the location of silicon grain, as in this MILC method, are collectively referred to as *location-controlled polysilicon*. Figure 6.47b shows a process in which the gate insulator aperture is opened to allow the crystallization to propagate from the area in contact with the aperture.

The MILC method does not require laser annealing control; however, the presence of any residual nickel introduces the risk of current leakage and, thus, impaired reliability. Studies are underway to reduce the amount of residual nickel.

6.5.3.2 AMFC Method

The main objective of the alternating magnetic field crystallization (AMFC) method is to reduce the crystallization temperature by the addition of an alternating magnetic field [32, 33].

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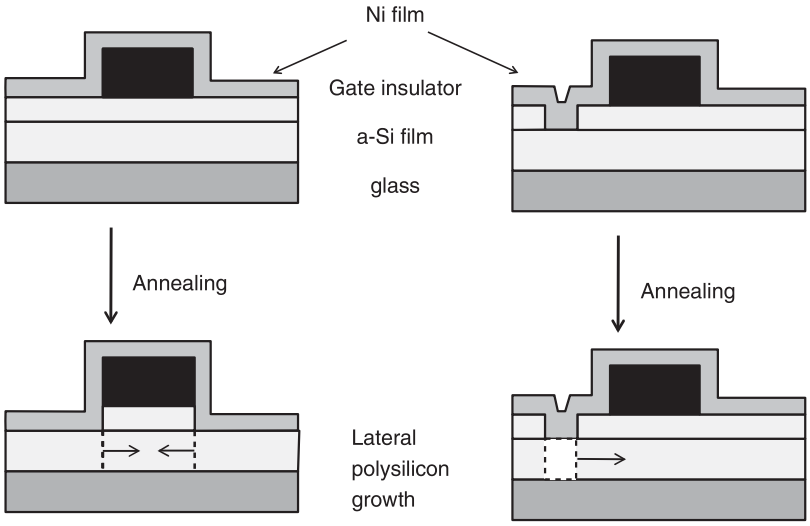


Figure 6.47 Schematic illustration of the principle of solid-phase crystallization using the metal-induced lateral crystallization (MILC) method.

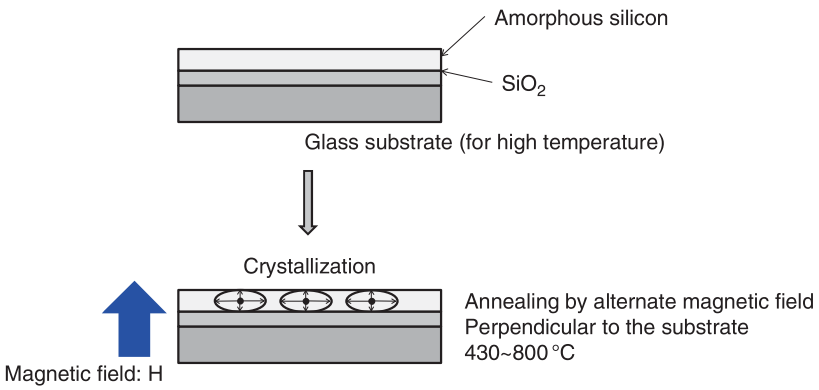


Figure 6.48 Diagram of crystallization apparatus employing the alternating magnetic field crystallization (AMFC) method.

Figure 6.48 shows crystallization using the AMFC method described by Seo et al. [34]. After deposition of SiO_2 by PECVD, 500 Å of amorphous silicon is deposited using $SiH_4 + H_2$ gas, and the amorphous silicon film is crystallized by a 500 °G (230 kHz, 50 A, 8 s) alternating magnetic field at ~430–550 °C, followed by 5 min of annealing.

The AMFC method can cause crystallization without the concern of the nickel-related issues that usually occur with the MIC or MILC method.

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6.5.4 Oxide Semiconductors

Oxide semiconductor TFTs [35–38] such as those made from ZnO or InGaZnO (also abbreviated IGZO) are attracting much attention for several reasons:

- The manufacturing process for oxide semiconductors is almost the same as that for amorphous silicon TFTs; therefore, it has cost merit compared with LTPS-TFT by ELA.
- Much higher mobility can be achieved for oxide semiconductors than for amorphous silicon, which enables integration of higher-speed circuits for low circuit cost.
- The manufacturing process is very similar to amorphous silicon TFT, so same manufacturing line can be used by adding minimum investment, such as, only oxide semiconductor deposition equipment, which promises low manufacturing cost.
- There is less performance variation related to driving stress than with amorphous silicon.
- The process temperature is lower, which is suitable for plastic substrates.
- As the channel layer is transparent, transparent displays may be possible.

The key reason of high performance with relatively easy processing lies in its conduction mechanism. The conduction band minimum (CBM) of oxide semiconductors are formed by s orbital of metal atoms. Insufficient oxygen brings about the free electron, so it normally shows *n*-type carrier conduction. The bandgap is more than 3 eV, which causes transparent appearance regarding the visible light wavelength range.

It is known that silicon-based carrier conduction is governed by sp^3 hybrid conduction mechanism as shown in Figure 6.49. For maximum conduction, large overlap of sp^3 orbital is necessary. However, the orbital shape has much anisotropy, so a little disorder causes large loss of overlap that reduces the semiconductor mobility. As a result, for example, mobility of polycrystalline TFT and amorphous silicon TFT has more than two orders of magnitude difference in field-effect mobility.

In n-type oxide semiconductors, the conduction is based on s orbital overlap as shown in Figure 6.50, which has spherical orbital shape. Spherical orbital promises good conduction even when some disorder takes place [39].

Density of states is very low in the gap, so Fermi level easily exceeds the CBM and shows the carrier transport based on the band conduction mechanism, similar to that of crystalline semiconductors, different from amorphous silicon whose driving region is in the tail state. As it is N-channel conduction with wide band gap, the hole density is very low, so no inversion region can be made, which promises very low leakage current in the negatively biased operation.

For best performance during manufacturing, many aspects must be taken into account [40].

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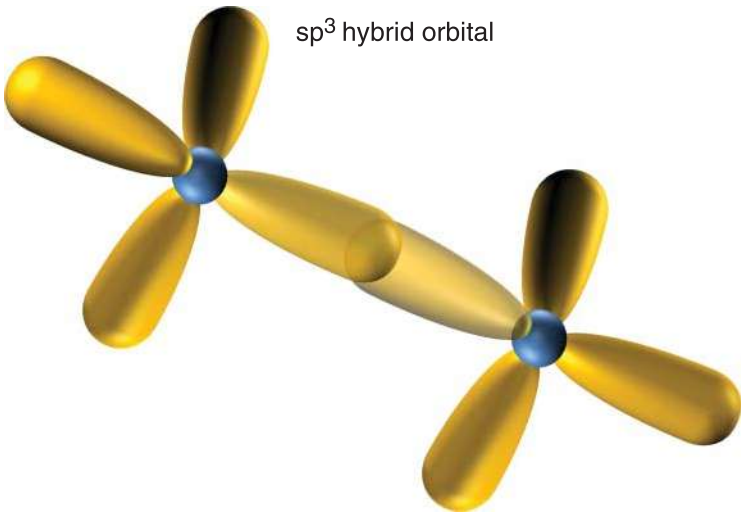


Figure 6.49 sp^3 hybrid orbital conduction mechanism by silicon-based semiconductors.

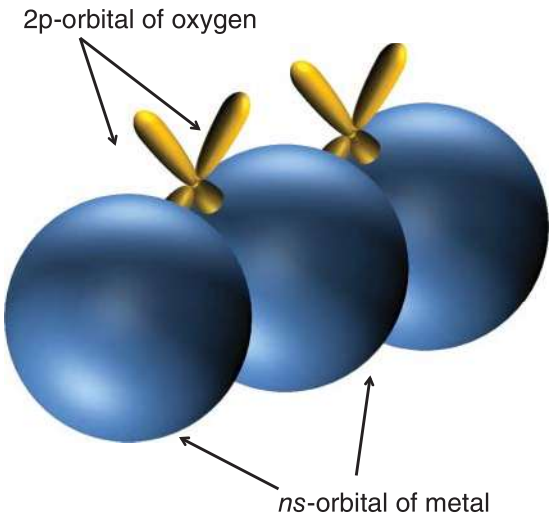


Figure 6.50 s-orbital-based conduction mechanism by oxide semiconductors.

- High mobility
- Uniform and stable amorphous film deposition
- Low-temperature deposition, compatible with low T_g substrate, such as plastic. (Currently, it is known that oxide semiconductor needs high-temperature annealing for stable operation.)
- Low carrier concentration deposition.

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For high mobility, a heavy atom ion, such as In or Sn, which has large expanded *ns* ($n > 5$) orbital as its least unoccupied state, will be effective (e.g., ITO or SnO_2). However, the demerit of such systems is that it easily causes oxygen vacancy and uncontrollable high density carrier is introduced.

To circumvent the situation, controllability of carrier density is important. By adding Ga,the oxygen vacancy can be controlled. Thus, In_3–ZnO–Ga_2O_3 system, so-called IGZO was introduced [41]. There is also an approach to use other type of crystalline oxide semiconductor systems [42].

Though oxide semiconductors, such as IGZO, show much better stability performance, they have disadvantage under illuminated condition. In the case of IGZO, occupied state higher than the CBM absorbs the short wavelength light, and threshold voltage of TFT is negatively shifted by hole creation. The phenomenon is accelerated especially in negatively biased condition. (Negative illumination bias stress: NIBS.)

Oxide semiconductors are normally deposited by sputtering or the atomic layer deposition (ALD) method. The sputtering method has been widely used for metal wiring or incorporation of pixel electrodes in TFTs and thus has achieved mature technology status in the industry. On the other hand, the ALD method can achieve very high-quality deposition, so it has the advantages of mobility and reliability. For the manufacturing of displays, sputtering is popularly used.

In the TFT fabrication process, defects are created, which causes the trap centers. To assure the stability and uniformity, thermal annealing over 350 °C is often used. Also, it is important to consider the effect of hydrogen, which can introduce oxygen vacancy in the oxide semiconductor layer.

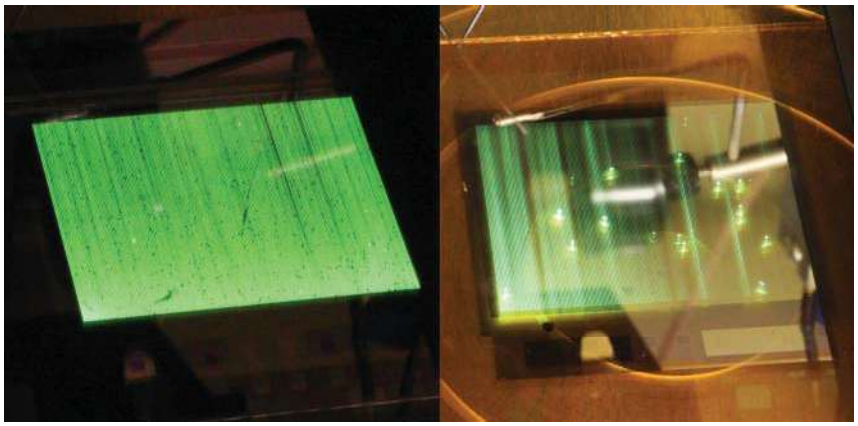


Figure 6.51 First active-matrix OLED driven by oxide semiconductor (courtesy by S.H. Park).

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Figure 6.52 OLED television product using oxide semiconductor TFT.

Oxide semiconductor is N-channel, so the pixel circuit, driving, and TFT structure are similar to the case of amorphous silicon and microcrystalline TFT, discussed in Section 6.5.2. Same approaches such as common-cathode + bottom emission (Figure 4.37), anode-line structure (Figure 4.38), double-channel, and compensation circuit have been applied.

Figure 6.51 shows the first active-matrix OLED display driven by oxide semiconductor [43, 44]. In this prototype, both TFT and OLED devices are transparent so that the transparent feature of oxide semiconductor can be fully featured. Figure 6.52 shows the AMOLED television product by oxide semiconductor. Due to the scalability of technology, oxide semiconductor has acquired the state-of-the-art position of OLED television.

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7

OLED Television Applications

The success of OLED technology in television applications is due to the superiority of its parameters, such as response speed, viewing angle, and contrast ratio.

In this section, we discuss the factors and methods involved in the design and manufacture of medium-to-large OLED displays and how to achieve high productivity, low cost, and high production yield to compete with other display technologies in the television industry.

7.1 PERFORMANCE TARGET

Table 7.1 shows the specification of commercially available OLED television [1]. As OLED is self-emissive device, there is no light emission in the black state. Therefore, the contrast ratio is infinite in dark rooms, which gives impressive image to the viewers. Also large color gamut can give fidelity to the intended image signals.

OLED power consumption depends on the image, as can be seen in the table. As the luminance is increased, the power consumption increases. With full-screen black image, the power consumption can be very small, which is mainly consumed by tuner and other electronic components. It has been reported that the average luminance of television is about 21.2% of white screen [2], so the display power consumption can be considerably reduced with normal television broadcasting condition.

OLED has been used mainly for small mobile displays. To enjoy the OLED's superior performance for television, such as excellent contrast, viewing angle, and response time, it is necessary to make large OLED television economically available for purchase by many users. To make that happen, high-yield manufacturing is inevitable.

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Table 7.1 Specification of Commercially-Available OLED Television (As of September 2016)

	OLED-TV1		OLED-TV2	
Display size	54.6-in.		54.6-in.	
Resolution	1920 × 1080 progressive		1920 × 1080 progressive	
Type	Curved		Curved	
Display mode	Dynamic	Standard	Vivid	Standard
Luminance of white (Standard) (cd/m^2): L_w	489	398	373	389
Luminance of black (cd/m^2):	0	0	0	0
Contrast ratio (dark room)	∞ : 1	∞ : 1	∞ : 1	∞ : 1
Color gamut (versus sRGB)	116%	120%	118%	118%
CCT(K)	12,580	8,945	11,030	10,230
Power (full-screen white) (W): P_W	252	219	213	210
Power(full-screen black) (W): P_K	115		51	

OLED-TV1: Samsung KN55S9CAFXZA, OLED-TV2: LG55EA9800.

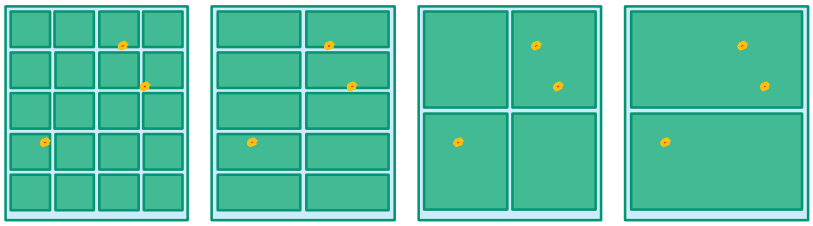


Figure 7.1 Impact of defect to the display production yield.

Figure 7.1 shows the relationship between defect and yield. In the figure, there are three defects assumed. As shown in the most right figure, if we get two large panels from one mother glass substrate, the production yield would be 0%. If we get four displays, the yield would be 50%. If 10 displays, we can get 70% yield and if 20 displays, 85% yield with this assumption. This suggests that it is not very easy to get reasonable production yield for large displays. A strategy to get reasonable production yield for large OLED display manufacturing is discussed in the following section.

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7.2 SCALABILITY CONCEPT

7.2.1 Relationship between Defect Density and Production Yield

The production yield, discussed in Figure 7.1, can be estimated using simulation theory. For the large display manufacturing, it is quite important to judge the cost increase caused by the yield loss due to the form factor change.

7.2.1.1 Purpose of Yield Simulation

Production yield simulation has been studied in the semiconductor and LCD display fields to avoid the potential for any risk associated with the production of large devices or high-resolution display [3]. The product yield simulation technique can also be applied to OLED to some extent to estimate the amount of potential risk.

7.2.1.2 Defective Pixel Number Estimation Using the Poisson Equation

The probability of k pieces of defective pixels existing on a display can be expressed as follows (Poisson distribution):

$$P_{SC}\{k\} = \frac{\lambda_{SC}^{k}}{k!} e^{-\lambda_{SC}} \tag{7.1}$$

Here, λ_{SC} is the average number of defective pixels on a display. If N_{SCT} is defined as the criterion for the maximum allowable number of defective pixels, production yield related to point defect can be expressed as follows:

$$Y_{SC} = \sum_{k=0}^{N_{SCT}} \frac{\lambda_{SC}^{k}}{k!} e^{-\lambda_{SC}} \tag{7.2}$$

Figure 7.2 compares the defective pixel number data for small and large displays by simulation. Smaller displays tend to have fewer defective pixels, and larger displays tend to have a higher number of defective pixels. In the most extreme case, the number of defective pixels is proportional to the area. Thus, a 32-in. display can have $(32/2)^2 = 256$ times the number of defective pixels in a 2-in. display.

On the other hand, the maximum allowable number of defective pixels (customer specification) does not increase with increase in display size, which causes significant reduction of production yield for large displays.

7.2.2 Scalable Technology

There is a new trend in the OLED industry to ensure the high production yield of large AMOLED displays by using a combination of scalable technologies including the white OLED emission + color filter method [4, 5]. Gen 8

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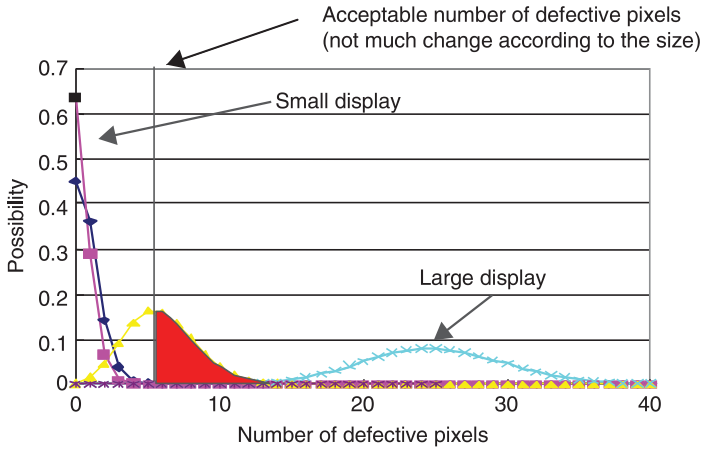


Figure 7.2 Graph illustrating defective pixel number simulation.

investment using this scalable method has been made to achieve low-cost 55-in. OLED television displays [6]. In this section, the scalable technology scenario is explained.

7.2.2.1 Scalability

One of the most important objectives in the manufacture of large TV displays is to achieve low defect density. Table 7.2 indicates which display production techniques are scalable and appropriate for manufacture of large displays.

White + color filter technology, solid-phase crystallization, amorphous silicon, microcrystalline silicon, and oxide TFT do not provide much constraint against enlarging a display, so they can be classified as scalable.

As scalable technologies do not pose much risk in the enlargement of display dimensions, if a display produced by the combination of scalable technologies can provide competitive product-level performance, and if the prototype can

Table 7.2 Examples of Scalable Technology

Technique	Small Display	Large Display
Shadow mask RGB pixilation	OK	Low yield
White OLED + color filter	OK	OK
Polysilicon TFT by ELA	OK	Tool restriction
SPC polysilicon	OK	OK
a-Si, microcrystalline Si	OK	OK
Oxide TFT	OK	OK

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attract the customer's interest, it will mean that medium-to-large AMOLED displays can be brought to the market with low risk.

To support this idea, the following three methods have been implemented together successfully to develop a 100% NTSC AMOLED display prototype [4]:

1. The white + color filter method, which can be used to produce a scalable OLED device
2. The *global mura compensation* (GMC) method, which is a scalable driving technology
3. The *solid-phase crystallization* (SPC) method, a scalable TFT backplane method.

Point 1 is discussed in Sections 7.3 and 7.4. Also Points 2 and 3 are discussed in Sections 6.4.4.3 and 6.5.4.1. The prototype detail is described in Section 7.4.1.4.

7.3 MURDOCH'S ALGORITHM TO ACHIEVE LOW POWER AND WIDE COLOR GAMUT

7.3.1 A Method for Achieving Both Low Power and Wide Color Gamut

To create a large display, the white + color filter approach is advantageous in terms of production due to its scalability and the maturity of color filter manufacturing process, which has been used in LCD industry for a long time. In spite of the secured production with high yield, a trade-off between display luminance and color gamut happens, as the color filter absorbs the light coming out from the OLED devices. To make competitive display performance with other display technologies, such trade-offs must be removed. Recent booming OLED televisions employ a method that can ensure a wide color gamut as well as low power consumption. Here we discuss a method that can help provide these.

Figure 7.3 is a histogram of every pixel color using the CIE (x, y) coordinate in 13,000 picture images stored in the Eastman Kodak library [7, 8]. It shows that most real-world colors are located in the center of the CIE coordinate, namely, near the white point. Figure 7.4 is another histogram that depicts the analysis of television image using the same method [9]. These results reveal the very interesting fact that most images can be expressed monochromatically (in white + black + gray) with some color addition [10].

The four-pixel approach (RGBW: four subpixels of red, green, blue, and white) utilizes this (monochrome) facility. (To avoid confusion with the RGB pixelation method, the RGB three-pixel method with white emission + color filter is denoted as W-RGB, and RGB four-pixel method with white emission + color filter is denoted as W-RGBW.)

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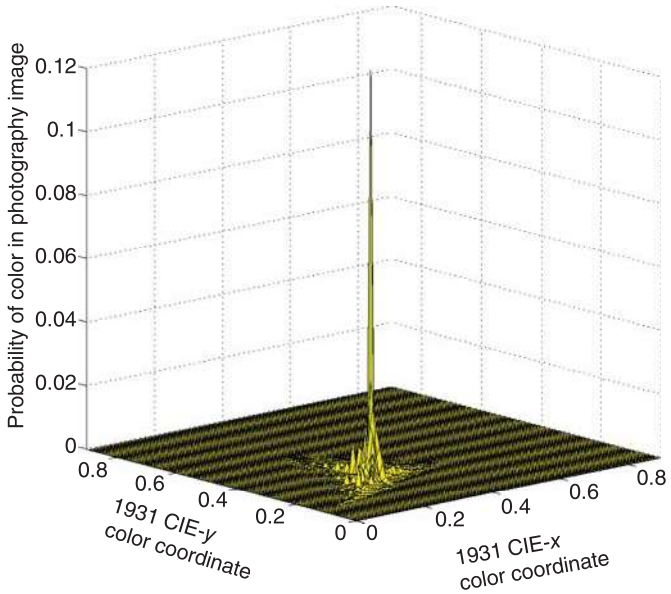


Figure 7.3 Schematic representation of a color-coordinated histogram constructed from analyses of 13,000 photographic images.

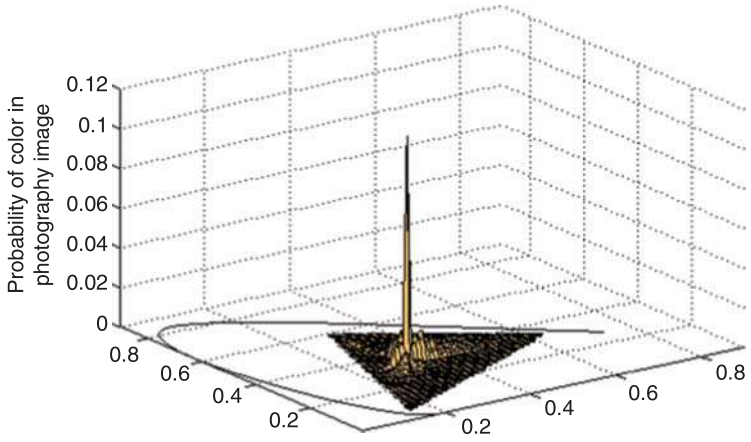


Figure 7.4 Schematic representation of a color-coordinated histogram constructed from analysis of a television signal.

With the W-RGBW method, white emission passes through a color filter with absorption for the R (red), G (green), and B (blue) subpixels. However, the white (W) subpixel does not cause absorption, so it can enable high efficiency and long lifetime. As discussed earlier, most real-world colors are near white, so the display power of a panel using the W-RGBW method does not change

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significantly even though its reproducible color gamut is wide. This ingenious strategy regarding knowledge and use of the W-RGBW method is an important breakthrough toward improving the power consumption of the white + color filter method and rendering this method competitive with the RGB pixelation method.

7.3.2 RGBW Driving Algorithm

With the RGBW driving method proposed by Murdoch et al., white emission features low-power driving capability without sacrificing color reproduction [11].

The conventional method uses red, green, and blue to display arbitrary colors (Figure 7.5). Murdoch's RGBW driving method also uses three primary colors to display arbitrary colors but selected the three primary colors according to the following rules:

- Color inside the B–G–W triangle is expressed by the three primary colors blue, green, and white, excluding red (Figure 7.6).
- Color inside the G–R–W triangle is expressed by the three primary colors green, red, and white, excluding blue (Figure 7.7).
- Color inside the R–B–W triangle is expressed by the three primary colors red, blue, and white, excluding green (Figure 7.8).

According to this approach, it is possible to fully utilize the advantage of high-efficiency white as well as the ability to display pure colors. Figure 7.9

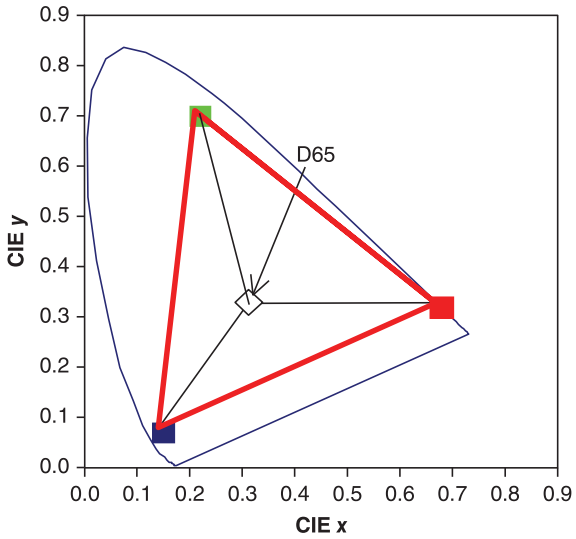


Figure 7.5 Graph illustrating color reproduction using the normal RGB method.

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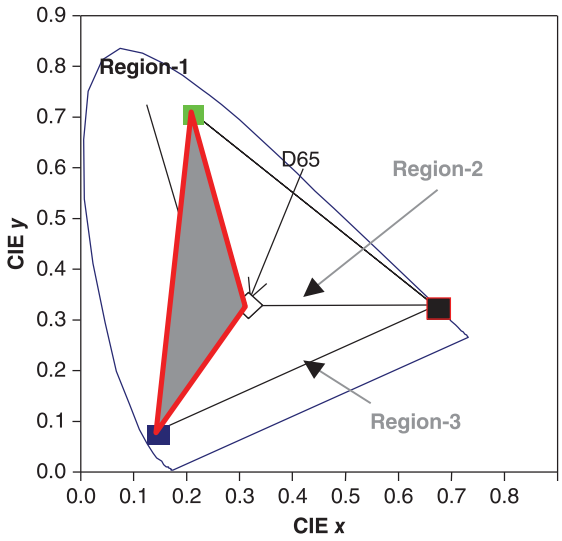


Figure 7.6 Plot showing color expression by GBW (green + blue + white) subpixels.

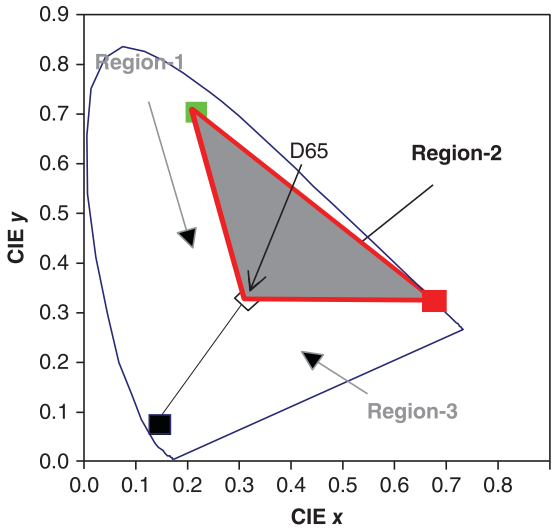


Figure 7.7 Plot showing color expression by RGW (red + green + white) subpixels.

shows the actual power consumption measurement results of W-RGB displays and W-RGBW displays using various images [8, 12]. The result shows that the W-RGBW four-subpixel method has almost half the power consumption of the W-RGB display panel. Keep in mind that that this discussion is *not* fully applicable to LCDs. The difference lies in the fact that OLED power consumption is proportional to the electric current, not aperture ratio, while an LCD's power consumption is proportional to the aperture ratio. In the LCD case, RGBW

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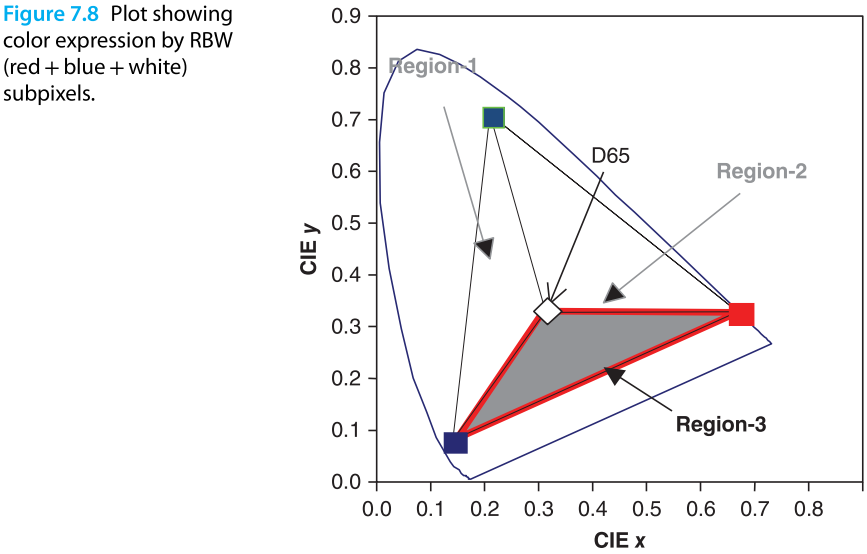


Figure 7.8 Plot showing color expression by RBW (red + blue + white) subpixels.

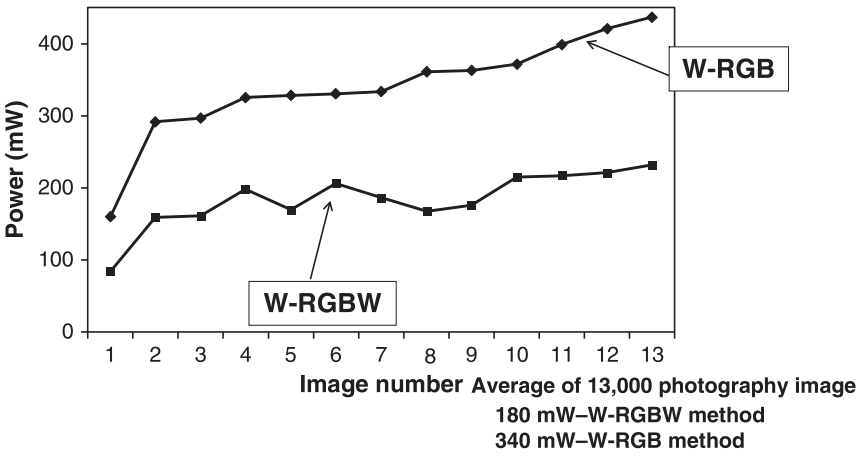


Figure 7.9 Graph comparing power consumption levels of W-RGB and W-RGBW methods for various images.

driving causes display transmittance loss due to narrower subpixel size by the use of four subpixels. Power reduction by RGBW driving is diminished by low transmittance of LCD pixels. In the case of OLED, luminous flux is almost the same regardless of aperture ratio if the electric current, namely, display luminance, is the same. So the merit of power consumption elimination can be brought about for OLED. The problem for OLED displays is the lifetime reduction due to aperture decrease.

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Figure 7.10 14-in. active-matrix OLED display by white + color filter method.

Figure 7.10 shows the 14-in. prototype by white + color filter method. The display has 1280×768 resolution, RGBW four subpixel arrangement, 78% NTSC color gamut with peak luminance 500 cd/m^2 [9].

7.4 AN APPROACH TO ACHIEVE 100% NTSC COLOR GAMUT WITH LOW POWER CONSUMPTION USING WHITE + COLOR FILTER

7.4.1 Consideration of Performance Difference between W-RGB and W-RGBW Method

7.4.1.1 Issues of White + Color Filter Method for Large Displays

Though white + color filter method can significantly reduce power consumption by using W-RGBW four-pixel approach, compared with the case of W-RGB three-pixel approach, RGB-pixelation method has been already achieving more than 100% NTSC color gamut for cellular phone displays. Then, it was investigated whether there is any way to further relax the trade-off of white+color filter approach, so that both low power consumption and high color gamut such as 100% NTSC can be satisfied [4, 5].

7.4.1.2 Analysis of W-RGBW Approach to Circumvent Its Trade-off Situation

Though power consumption can be reduced with W-RGBW method as Murdoch pointed out, the display power consumption depends on the image content, so it was not easy to calculate it without actual experiment.

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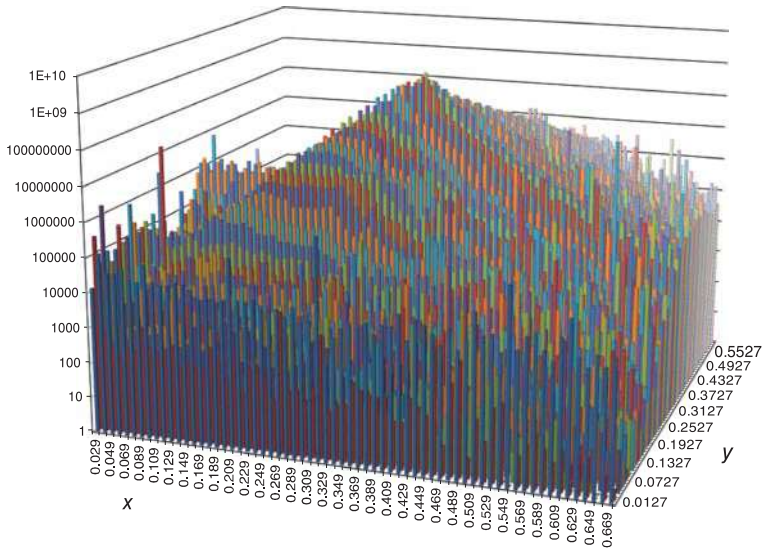


Figure 7.11 Histogram of pixel colors in 19,419 images (log scale).

Tsujimura [5] made a simulation on the 19,419 images and showed that the pixel color histogram (Figure 7.11) can be written as

$$(x - 0.31271)^2 + (y - 0.32902)^2 = [\{20.950 - \log_e(z)\}/40.516]^2 \tag{7.3}$$

Then, the probability of having color coordinate (x, y) can be calculated as

$$P(xy) = z/N_{\text{total}} = \frac{1}{N_{\text{total}}} \exp(\log_e(z_{\max}) - a\sqrt{(x - x_w)^2 + (y - y_w)^2}) \tag{7.4}$$

where $N_{\text{total}} = 52{,}464{,}357{,}936$, $a = 40.516$, $\log_e(z_{\max}) = 20.950$, $x_w = 0.31271$, and $y_w = 0.32902$.

Figure 7.12 shows the current density of (x, y) color coordinate of W-RGBW display using this statistics. Current density shows minimum value at white point and gradually increases as the color is saturated (larger chroma value). Especially, the current density shows very high value near blue color coordinate, as the current efficiency of blue is not very good, compared with other colors.

Though pure colors, especially blue, have large current consumption, the probability of having saturated colors is extremely low according to Figure 7.11. (Beware that the z axis of Figure 7.11 is logarithm scale.) To estimate the actual current consumption contribution in a display, Figure 7.11 needs to be multiplied by the value in Figure 7.12.

$$J_{\text{PICTURE}}(xy) = J_{\text{TOTAL}}(xy) \cdot P(xy) \tag{7.5}$$

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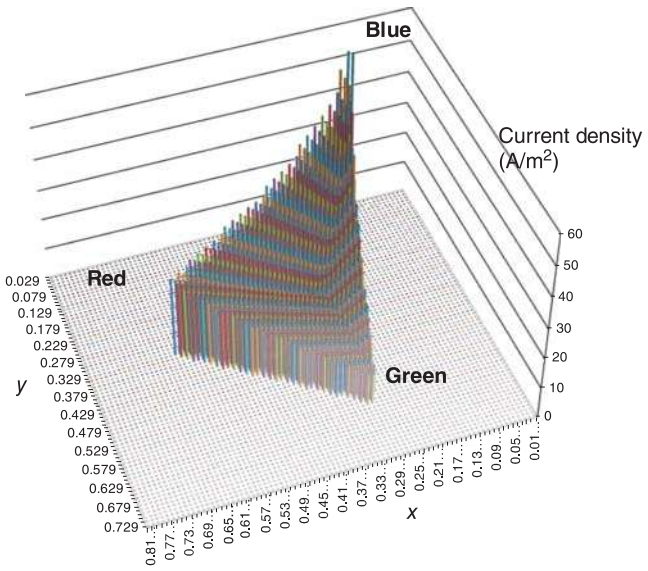


Figure 7.12 Total (W + R + G + B) driving current for W-RGBW method.

Equation 7.5 gives the histogram of current density for color coordinate (x, y) as shown in Figure 7.13. Pure colors give minor contributions and most of the current consumption is still made by near-white region.

When current efficiencies of 36.5 (cd/A) for D65 white, 7.6 (cd/A) red, 19.3 (cd/A) green, and 3.2 (cd/A) blue are assumed, by adding the current density for all the x and y, the total current density, 9.386 A/m^2, was calculated using probability distribution in Figure 7.11 for W-RGBW OLED display. Similarly, W-RGB OLED display (without white subpixel) was simulated and the current density was 21.060 A/m^2. According to this simulation, it was concluded that W-RGBW OLED display has almost half (1/2.2437) the current consumption of W-RGB OLED display. This corresponds to the observation of half power consumption by W-RGBW, discussed in Section 7.3.2.

As to the region distant from the white point, there is almost no contribution according to Figure 7.11 due to extremely low possibility of occurrence. In practice, the driving current does not change very much when the RGB subpixel efficiency is changed, as shown in Figure 7.14.

As R, G, B subpixel emissions do not affect the power consumption very much, if we can increase the white intensity without affecting the R, G, B emission intensity, the display power efficacy would be increased with no color-reproducibility handicap. However, R, G, B emission is made from white emission, so R, G, B emission should be proportional to the white emission if

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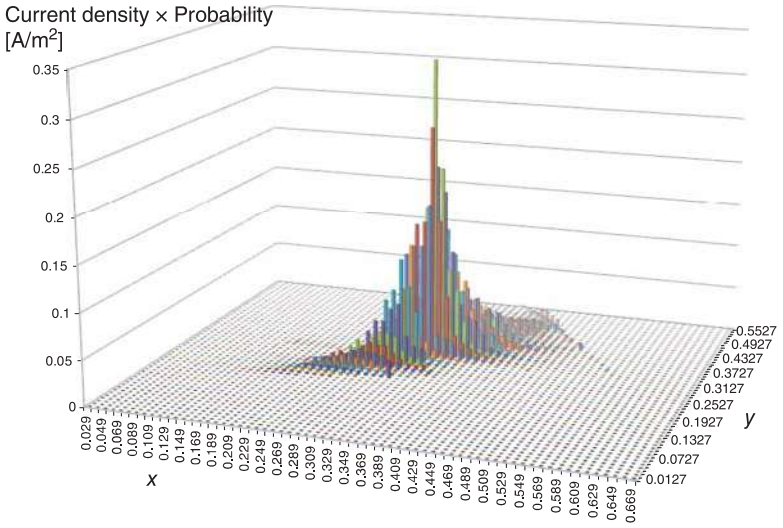


Figure 7.13 Current density of color coordinate (*x*, *y*) for actual display showing picture image.

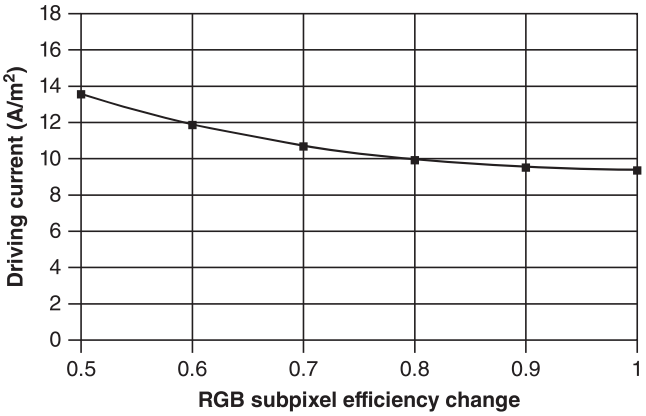


Figure 7.14 Driving current dependence of RGB subpixel efficiency in W-RGBW system.

white spectrum shape is kept the same. To overcome this situation, a trick can be applied.

Figure 7.15 shows the relationship between emission spectrum and color filter spectrum in the case of conventional design. To maximize the light output of OLED emission through color filter, the color filter peaks are normally matched with emission spectrum peak. A wide color filter pass band is used for each color so that a high transmittance and therefore brightness can be obtained for

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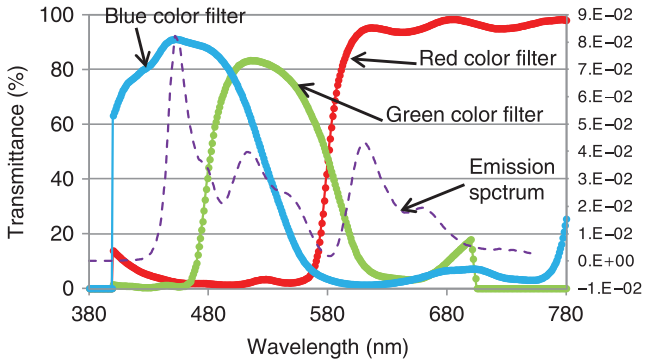


Figure 7.15 Conventional white + color filter approach.

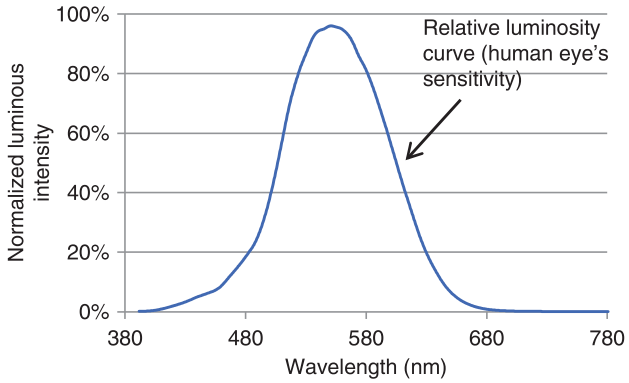


Figure 7.16 Relative luminosity curve.

each. However, the wide color filter spectrum results in desaturation of the colors and hence a poor color gamut, hence a trade-off exists between luminance and color gamut happens.

It is known that human eye's sensitivity has a peak at 555 nm wavelength as shown in Figure 7.16. If white OLED emission near the sensitivity peak is increased, the power consumption of W-RGBW display would be reduced, because most of the display power consumption is decided by white emission, as discussed. However, as 555 nm is between yellow and green, if such color appears in red, green, blue subpixels, color gamut would be reduced. Also for the high color gamut, narrow spectrum emission must be made. Therefore, it is necessary to adopt color filters with narrow spectrum width, which gives minimum overlap.

According to this analysis, two conclusions can be made for W-RGBW displays.

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Conclusion 1: Current density is not very much affected by RGB subpixel efficiency. (Display power follows the same trend.)
Conclusion 2: By increasing the white subpixel efficiency, the display power would be further improved.

If both can be achieved, low power consumption can be combined with high color gamut capability on W-RGBW displays. This concept was checked through actual display fabrication.

7.4.1.3 Design of a Prototype to Demonstrate That Low Power Consumption Can Be Achieved with Large Color Gamut

To achieve low power consumption with high color gamut, an optimized set of OLED and color filter spectra was developed and applied to a W-RGBW AMOLED display [4].

R + G + B + Yellow OLED formulation used for the prototype is shown in Figure 7.17. The additional yellow spectrum component very well matches with relative luminosity curve, so the formulation makes much higher efficiency possible than conventional RGB-peak white.

The largest hurdle was color filter (Figures 7.18 and 7.19). Existing color filter for LCD could not show large color gamut for R + G + B + Yellow formulation, because the green and red color filters transmit light in the yellow wavelength region. Also the blue color filter spectrum was not narrow enough to achieve CIE-$y = 0.06$, which is necessary for Adobe-RGB/s-RGB color space reproduction. New color pigment and special milling/dispersion technology was applied so that the OLED panel demonstrated in IDW2008 [4] achieved NTSC 100% (Figure 7.20) with lower power consumption (less than 2W for 8-in., which corresponds to 64W for 32-in. television) than LCD display products on the market.

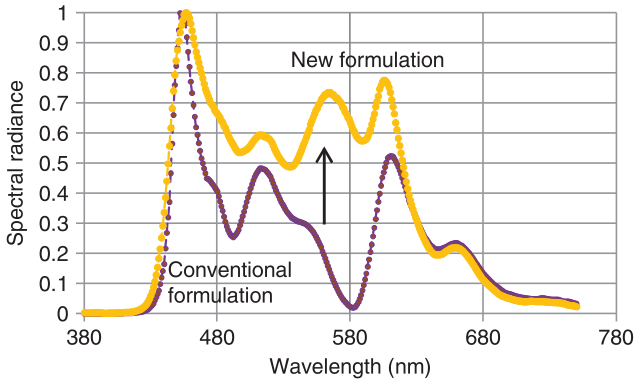


Figure 7.17 Wide spectrum white formulation for high white subpixel efficiency.

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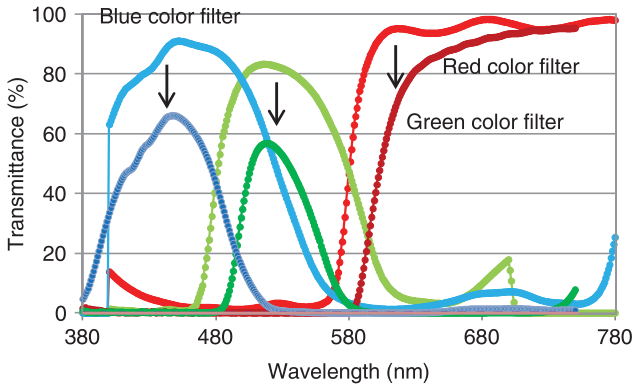


Figure 7.18 High color gamut color filter design for wide spectrum white emission.

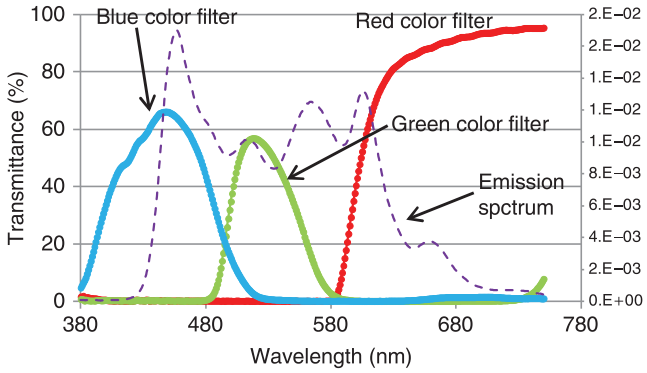


Figure 7.19 New formulation with new color filter.

The technology has been applied to state-of-the-art AMOLED displays on the market and is the dominant technology currently for the large AMOLED TVs.

7.4.1.4 Product-Level Performance Demonstration by the Combination of Scalable Technologies

Figure 7.21 a display prototype that has competitive performance as a display product including 100% NTSC color gamut, which was believed to be not achievable using the white + color filter method in combination with scalable technologies [4]. As blue is the most sensitive primary color (Figure 4.14 shows that the McAdam ellipse [the human eye perception limit] for blue is much smaller than for green or red), the blue pixel of the prototype follows $(x, y) = (0.15, 0.06)$, required for Adobe-RGB, s-RGB and Rec-709.

This 8.1-in. display has 1.5 W power consumption (300 cd/m^2 operation) using the W-RGBW approach. As 8-in. LCD displays have ~2–4 W power

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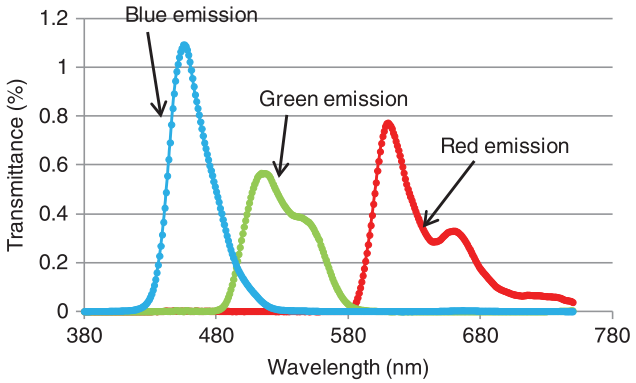


Figure 7.20 Emission output of W-RGBW display using new formulation, color filter set.



Figure 7.21 An OLED display prototype with a product-level specification using white + color filter technology (8.1-in. demonstration at SID 2008 by Eastman Kodak; this model has a 100% NTSC color gamut) [4].

consumption (data from specification sheet of eight commercially available 7~8-in. TFT LCD power consumption as of 2008), this white OLED prototype has already demonstrated competitive performance. For example, its power consumption corresponds to 64 W for a 32-in. television, and this is a sufficiently low value for a television set, which is typically 150 W in the case of an LCD television.

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Table 7.3 Scalable TFT Technologies

Technology	Example	Advantage	Disadvantage
SLS-LTPS	Samsung	High mobility	ELA-related issues
SPC(MILC)	CMEL, Samsung, Sharp	Proven mass production	Leakage current and instability due to residual Ni; 6 masks for top gate
SPC(ASPC)	LG Display, Samsung	Low leak current due to, absence of residual Ni	6 masks for top gate; glass shrinkage
μc-Si by CVD	Samsung	4 masks	Low mobility, low deposition rate, large OFF current, necessity of compensation circuit
μc-Si by diode laser	Sony	5 masks, (etch-stopper type)	Large OFF current, low throughput, necessity of compensation circuit
Oxide TFT	Samsung, LG Display, Sony, Canon	4 or 5 masks, high mobility, uniformity, low photo leak current, high aperture ratio	Negative bias stress instability under illumination, necessity of compensation circuit

This prototype proved that the display specification according to the market requirement can be achieved by the combination of high-yield (>90%) technologies, therefore means that the OLED television industry can be realized with low risk of investment.

For this proof-of-concept prototype, scalable compensation technology and scalable TFT technology was used. Regarding the compensation circuit, the GMC method, discussed in Section 6.4.4, was used. As to the TFT, Table 7.3 shows a comparison of the risk profiles for each technology when the size becomes larger. Among all these technologies, SPC polysilicon technology was used, which has been already used in manufacturing. As to the detail of scalable TFT backplanes, the SLS method, microcrystalline and amorphous silicon method, solid-phase crystallization, and oxide semiconductors are discussed in Sections 6.5.1.1, 6.5.3–6.5.5, respectively.

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8

New OLED Applications

OLED technology has been used for existing applications such as cellular phones, MP3 players, and televisions, but OLED technology also has the potential to penetrate into new applications because

1. an all-solid device (when blanket encapsulation is used) is suitable for flexible applications;
2. use of a high-transmittance electrode enables transparent displays;
3. a thin display module is suitable for overlapped tiling.

8.1 FLEXIBLE DISPLAY/WEARABLE DISPLAYS

8.1.1 Flexible Display Applications

There are many flexible display [1–4] technologies reported in the OLED field (Figure 8.1). With flexibility properties, smart phone with round boarder (Figure 4.28), rollable (Figures 8.2 and 8.3) or foldable (Figure 8.4) displays can be fabricated. Also their robust, unbreakable properties may become important for future mobile applications.

8.1.2 Flexible Display Substrates

To make a flexible OLED device, there are three substrate technologies as shown in Table 8.1 [5, 6]. Glass substrate has perfect barrier property against oxygen and humidity. Recently, very thin glass (e.g., 0.1 mm thickness) has been reported. Such thin glasses can be handled by mounting the thin glass on thick carrier glass [7]. However, glass substrate is fragile and can be broken by the damages. Breakage during manufacturing would cause suspension of processing for hours and may bring about economical loss. Also breakage of the product may occur after purchase by the end user.

In the case of polymer substrate, thinness, light weight, and flexibility can be fully enjoyed. However, humidity and oxygen might cause reliability issues, such as dark spots or pixel shrinkage.

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Figure 8.1 An example of a flexible display (demonstration at FPD International 2007 by Samsung SDI).

Regarding the metal foil substrate, barrier property is as perfect as glass substrate. However, the metal foil normally has surface spikes, which may cause interlayer shorts between OLED electrodes. (Planarization layer reduces the issue.) Also metal foil is hard to handle on a roll-to-roll processing line, due to breakage and the weight of the rolls. Among these options, a plastic substrate is viable, if its barrier properties can be sufficiently improved. Such enhanced plastic substrates with barrier properties are referred to as barrier films.

Barrier films can be made by either roll-to-roll coating of barrier layers onto a plastic substrate or can be made by a laser liftoff process during device fabrication.

8.1.3 Laser Liftoff Process

Figure 8.5 shows the laser liftoff process presented by Miyasaka et al in 2007 [8]. LTPS-TFT is fabricated from an amorphous silicon layer, deposited on a glass substrate (Figure 8.5a). The device side of the substrate is glued by

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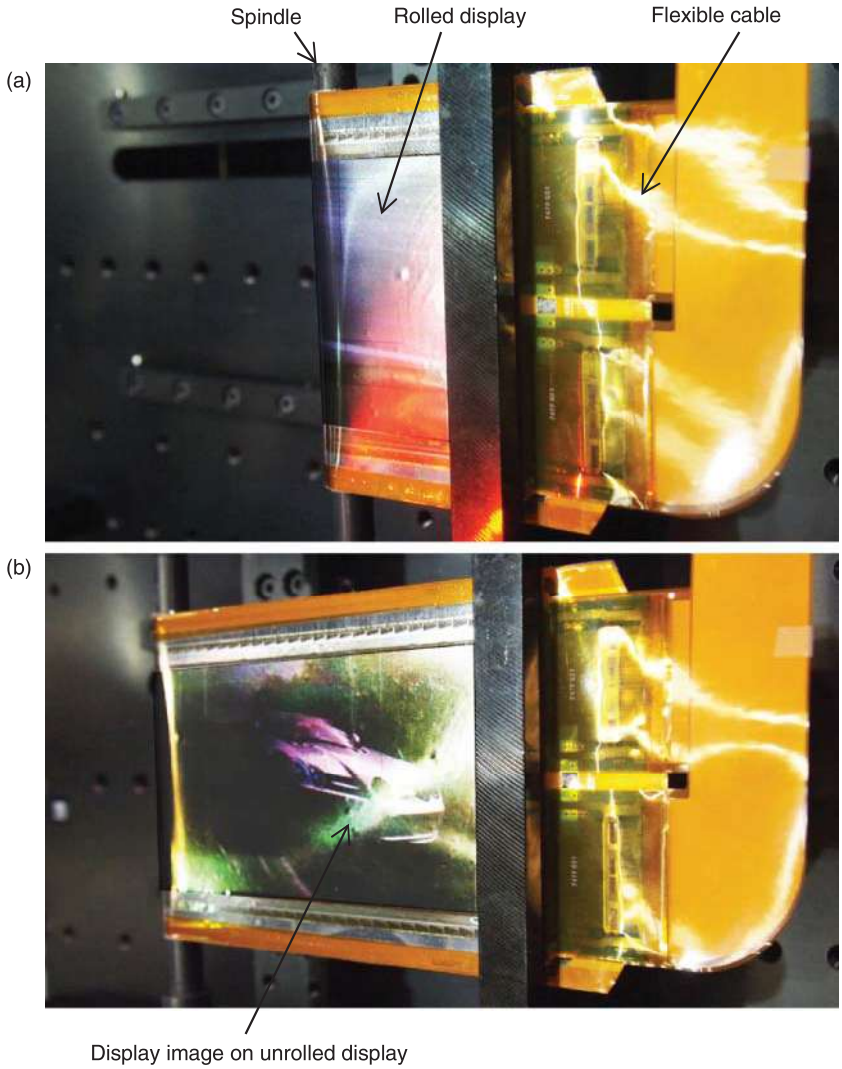


Figure 8.2 Demonstration of rollability of a flexible display: rolled (upper) and unrolled (lower) display (demonstration at SID2010 by Sony).

temporary adhesive to a temporary substrate (Figure 8.5b). XeCl excimer laser irradiation from the original glass substrate side breaks the adhesion of the TFT matrix to the original substrate and the devices are released (Figure 8.5c). The released device is glued to its final plastic substrate (Figure 8.5d). And finally, the temporary substrate is removed (Figure 8.5e).

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Figure 8.3 An example of rollable OLED display demonstrated in SID Display Week 2015 by LG display.

Since this laser transfer method was presented in 2001 [9], few such products have been reported; however, due to the improvement in barrier film technology to be applied to OLED display (discussed in Section 8.1.4), laser liftoff technology has suddenly come back under the spotlight. Curved cell phone displays fabricated by liftoff are gaining a lot of attention as product differentiators [10].

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Figure 8.4 An example of a foldable display (demonstration at SID2008 by Samsung Mobile Display).

Although laser liftoff is an attractive method, which can enable flexible displays, cost is still high due to the complicated process. Many modifications have been proposed, including the use of solid-state lasers and other kinds of release layers.

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Table 8.1 Various Substrate for Flexible OLED Device

	Pros	Cons
Thin glass	Barrier property Thinness Thermal durability	Breakage during manufacturing Product breakage
Plastic with barrier film	Flexibility Thinness Lightweight	Barrier property Thermal durability
Metal foil	Barrier property Thermal conductivity Thinness Thermal durability	Flatness (Needs insulator) Surface breakage in R2R process Needs top emission

8.1.4 Barrier Technology for Flexible Displays

Plastic substrates are normally used for flexible displays, which require barrier capability integrated in the substrates. OLEDs are subject to damage by moisture and oxygen, so the substrate needs to have low permeability. Burrows et al. report that a water vapor transmission rate (WVTR) less than 10^{-6} g/m^2·day is necessary for OLED applications [11]. WVTR can be measured by a calcium test or by a vacuum method, as discussed in Section 3.3.5.4. A barrier layer is formed on the substrate using a similar method to the thin film encapsulation of an OLED device, such as by chemical vapor deposition of $Si3N_4$ (discussed in Section 3.3.2), or by deposition of multiple organic/inorganic layers (discussed in Section 3.3.5.1). Al_2O_3 deposition by ALD (Figure 3.36) is also used for barrier-layer formation. To obtain transparency of the barrier film for high light transmission, SiO_xN_y is also used [12]. A plastic substrate has a low processing temperature limit, so it is important to keep the substrate sufficiently cool during the barrier-layer formation process. It should be noted that the maximum processing temperature must be much lower than the glass transition temperature (T_g) of the substrate. For example, the T_gs of the most popular substrates, such as polyethylene terephthalate (PET) and polyethylene naphthalate (PEN), are 150 and 180–220 °C, respectively, but the upper limit of the processing temperature needs to be lower, such as 80 °C for unannealed PET and 120 °C for unannealed PEN substrates [13]. (Annealing can increase the temperature limit to some extent, for example 120 °C for PET [14].)

There are also some examples of the use of metal foil substrates. A metal foil substrate [15] has merits in having high barrier capability and heat dissipation, which can extend the lifetime of an OLED device by achieving low-temperature operation due to the high thermal conductance of the metal electrode. A top-emission OLED structure must be used for a metal substrate.

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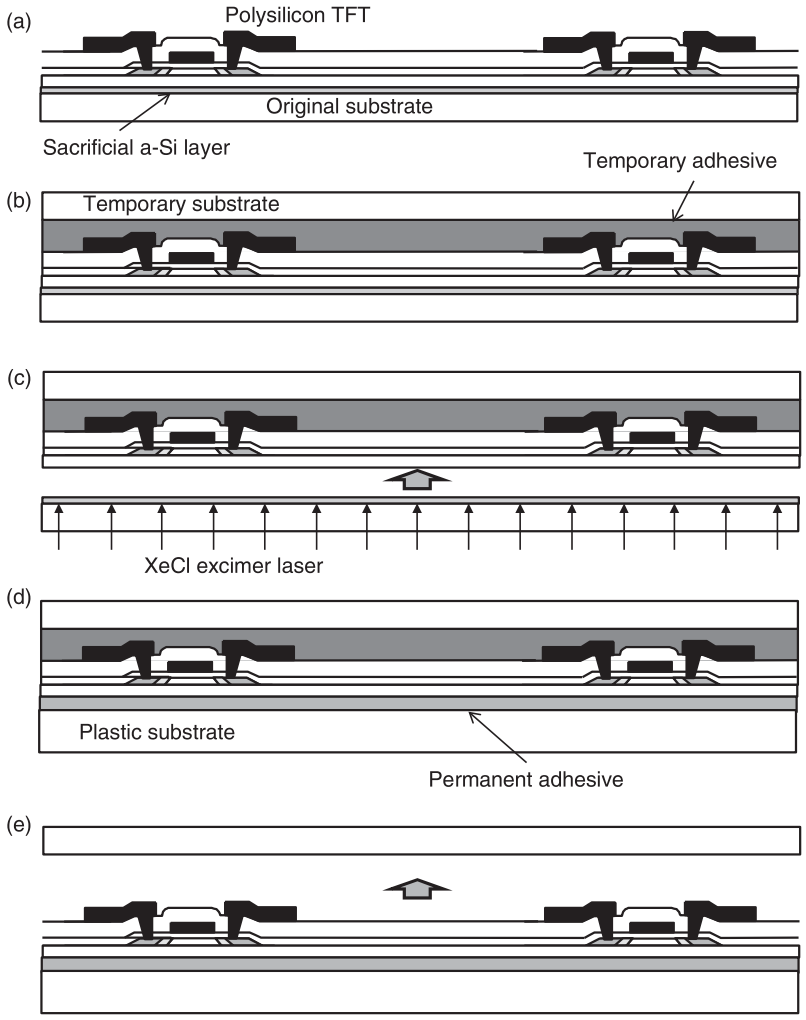


Figure 8.5 Laser liftoff process to make flexible device.

Normally, a metal foil substrate has a rough surface, so a planarization layer must be deposited before fabricating the OLED device.

8.1.5 Organic TFTs for Flexible Displays

In the case of OLED fabrication on plastic substrates, a maximum processing temperature must not be exceeded, as already discussed. Normally, the maximum processing temperature of amorphous silicon TFTs is about 300–400 °C and that of LTPS TFT is about 500 °C. There is no plastic substrate that can

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survive such high-temperature processing. Too low a process temperature during silicon TFT formation degrades the quality of the amorphous silicon film, which causes many problems, such as high leakage current, low mobility, hysteresis, and instabilities, so it is necessary for flexible display processing to use a different approach from processing on glass substrates.

There are two popular approaches to circumvent these temperature issues, that is, organic TFTs or oxide TFTs. Oxide TFTs have already been discussed in Section 6.5.5, so only organic TFTs are discussed in this section.

8.1.5.1 Organic Semiconductor Materials

Figures 8.6 and 8.7 show examples of basic polymer conductive molecules and basic small-molecule conductive molecules, respectively. Three approaches to design a conductive organic molecule [16] are as follows:

1. Implement a long series of conjugated π bonds.
2. Stack planar molecules with π electrons.
3. Utilize the charge transfer interaction. (Figure 8.8 shows an example of a charge-transfer complex. See Section 2.6.2.2.)

The left-hand molecular structure in Figure 8.7 shows the most popularly used p-type organic semiconductor, pentacene. It is composed of five benzene rings and has a relatively long conjugated structure, which enables charge conduction. The right-hand structure in Figure 8.7 shows copper phthalocyanine, which is also known as a p-type organic semiconductor. (It is also used as hole injection material as discussed in Section 3.1.1.1.) Copper acts as an electron acceptor, so the phthalocyanine structure conducts by hole transport. Phthalocyanine can also conduct electrons by electron-acceptor modification of the phthalocyanine side chains [17].

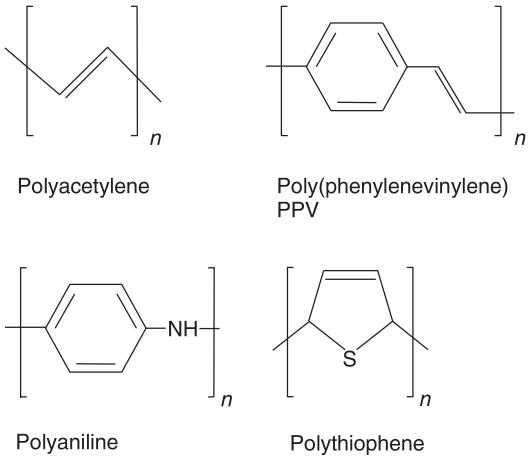


Figure 8.6 Examples of organic polymer conductors.

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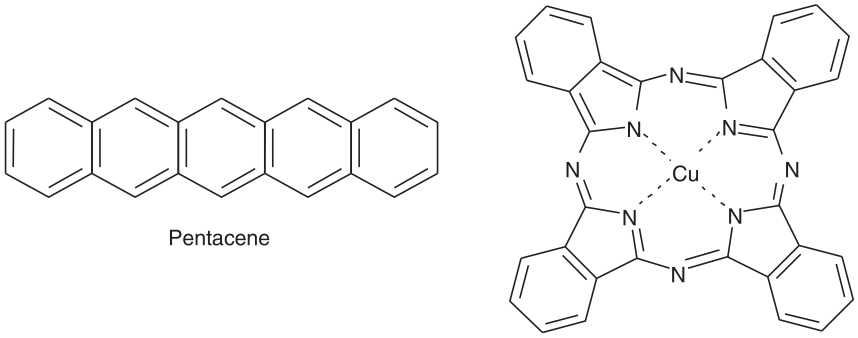


Figure 8.7 Examples of small-molecule organic semiconductors.

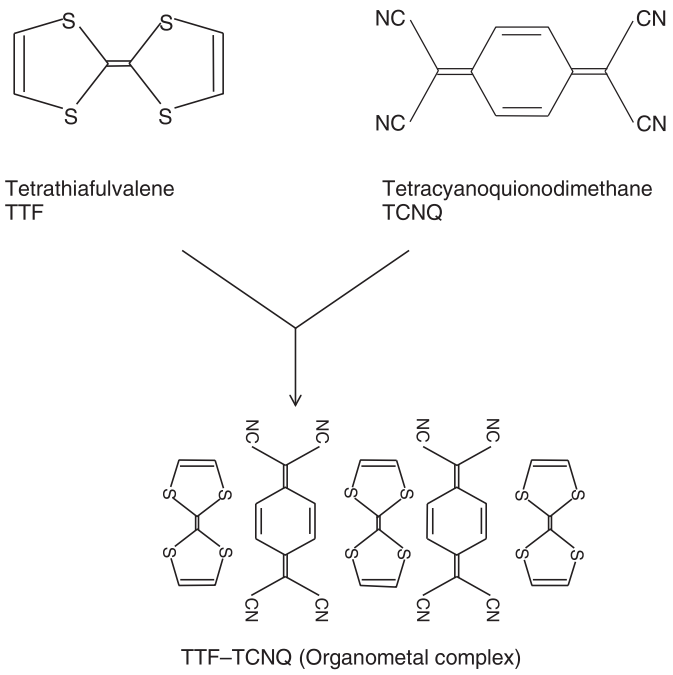


Figure 8.8 An example of a charge transfer complex.

8.1.5.2 Organic TFT Device Structure and Processing

As discussed in Section 6.1, there are two types of TFTs: bottom gate and top gate. For bottom-gate organic TFTs, an additional variation is possible. Figure 8.9a shows the top-contact bottom-gate TFT, in which the lower

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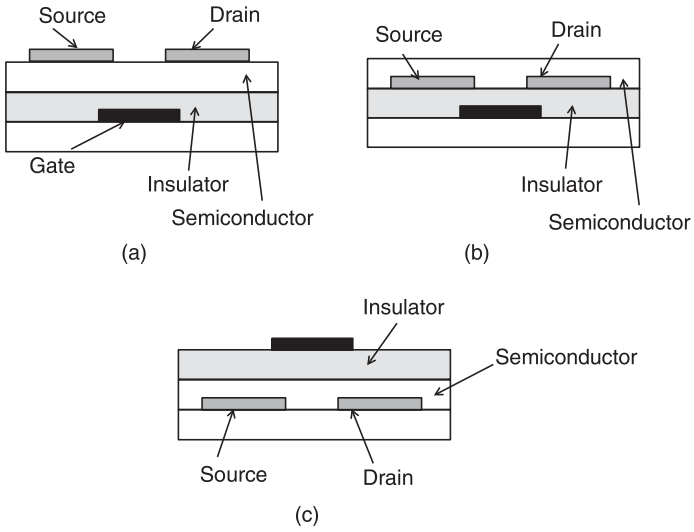


Figure 8.9 Various organic TFT structures. (a) Top-contact bottom gate TFT. (b) Bottom-contact bottom gate TFT. (c) Top gate TFT.

surfaces of the source and drain electrodes contact the semiconductor layer; Figure 8.9b shows bottom-contact bottom-gate TFT, in which the upper surfaces of the source and drain electrodes contact the semiconductor layer. The top-contact type can be fabricated with minimum exposure of the semiconductor–insulator interface to the ambient environment, so a relatively high-quality channel layer can be formed, making this the most popularly used structure in organic TFTs. On the other hand, the bottom-contact type has the merit that the semiconductor layer does not go through many processing steps after it is formed, so processing damage can be minimized.

The channel layer of an organic TFT can be described as "a π electron conduction system formed by organic molecules coupled by weak interaction caused by Van der Waals forces" [18]. To achieve high conductivity in an organic semiconductor, it is very important to maximize the intermolecular orbital overlap of π electrons. Therefore, a highly crystallized film produces higher mobility. In the case of a polycrystalline film, grain mobility dominates conduction because the mobility at the grain boundary is lower than that within a grain. That is why grain size should be maximized by process optimization so that the fraction of the semiconductor layer occupied by grain boundaries is minimized.

Organic semiconductors are susceptible to oxidation, which causes instability. To avoid this problem, molecules with lower HOMO values, which reduce oxidation, have been developed.

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8.1.5.3 Organic TFT Characteristics

The channel current of an organic TFT follows the gradual-channel approximation, the same principle discussed in Section 6.3. Current in the saturation region can be expressed as

$$I_D = \frac{\mu C_{OX}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{8.1}$$

where μ is mobility, V_{TH} is threshold voltage, C_{OX} is gate insulator capacitance per unit area, and W and L are channel width and channel length, respectively.

Normally, MOSFETs made with crystalline or polycrystalline TFTs keep a near-constant mobility value when the gate electric field is changed. However, in the case of organic TFTs, the mobility μ has a strong field dependency due to the hopping conduction mechanism, which was discussed in Section 2.3.7.3 (Poole–Frenkel conduction) and follows the equation as shown in (2.47).

$$\mu = \mu_1 \exp\left(-\frac{q}{kT}\beta\sqrt{E}\right) \tag{8.2}$$

where μ_1 is the mobility at zero electric field and β is the Poole–Frenkel factor.

8.2 TRANSPARENT DISPLAYS

Figure 8.10 shows an example of a transparent OLED display. Many companies are currently showing prototypes to explore possible markets for this new technology. They are targeting window information displays, head-mounted displays, digital speed meters, and so on. This new display technology may also open up novel applications.

To manufacture a transparent OLED display, a key technology is the transparent cathode electrode. With a conventional bottom emission structure, the cathode is made from a metal, such as aluminum. Metal is opaque, so it needs to be replaced with a transparent electrode. In the case of a top-emission structure, the cathode is made from a semitransparent metal, such as MgAg. By the combination of conventional technologies—an ITO anode, which is used for bottom emission, and a semitransparent metal cathode, which is used for top emission—a semitransparent OLED display can be fabricated. However, for an application such as a window information display, light transmittance and achromaticity are very important. A semitransparent metal cathode may not be sufficient to meet the market requirement.

To increase the transmittance, an ITO cathode is suitable. However, it is known that ITO sputtering can cause much damage to an OLED device. To circumvent this issue, the facing-target sputtering (FTS) system [19] provides a solution (Figure 8.11). FTS uses two sputtering targets face-to-face as a cathode and a magnetic field is applied perpendicular to the target faces (cf. the conventional DC sputtering system, discussed in Section 6.2.2, which

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Figure 8.10 An example of a transparent OLED display (demonstration at FPD International 2009 by LG Display).

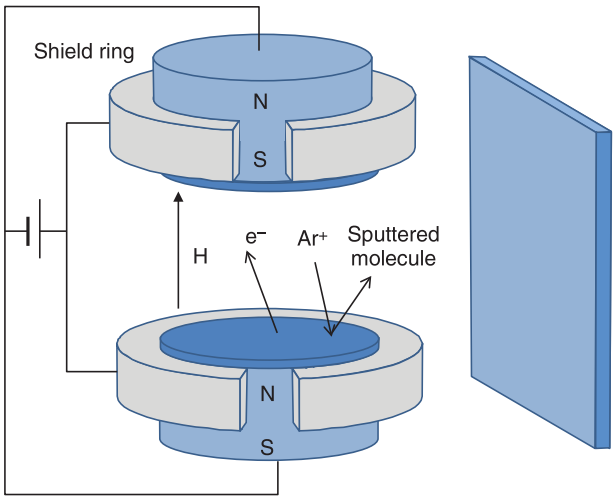


Figure 8.11 A schematic explanation of facing-target sputtering system.

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has a configuration with the sputtering target and substrate face-to-face and a DC voltage is applied between target and substrate). Using magnets, positioned behind the target, damage-free deposition can be achieved because the magnetic and electric fields are both parallel to the target, so negative ions created by sputtering gas do not bombard the substrate. Using low-damage sputtering, high-quality transparent cathode electrodes can be fabricated [20].

8.3 TILED DISPLAY

Although widescreen displays are attractive for signage or multiple viewer applications, it is not possible to make displays larger than the limitations imposed by the mother glass or equipment size restrictions, such as the excimer laser radiation length. Also there are various needs for nonstandard displays with formats other than 4 : 3 or 16 : 9. Tiling is an attractive approach to realizing these requirements.

8.3.1 Passive-Matrix Tiling

When the display unit is tiled, discontinuity between the adjacent panels must be minimized. Therefore, the discontinuity must be below the level of the human eye's perception.

Three human visual perception limits are defined: (1) the minimum visible limit, (2) the minimum separable limit (hyperacuity), and (3) the minimum resolvable limit [21]. The angle subtended at the eye at the minimum resolvable limit distance from the observed object is called the minimum angle of resolution (MAR). Visual acuity is defined as the inverse of the minimum resolvable visual angle measured in minutes of arc. Therefore, viewing distance D, the minimum resolvable limit distance d_{MIN}, the minimum angle of resolution θ_{MAR}, and visual acuity V have the following relationship:

$$d_{\mathrm{MIN}} = D \cdot \tan\left(\frac{2\pi}{V \times 21{,}600}\right) \tag{8.3}$$

Using this equation, the distance at which individual pixels can no longer be resolved can be calculated as given in Table 8.2 [22, 23].

For signage applications, viewing distance is much larger than that for television viewing at home, so pixels larger than 1 mm can be used with no problem, which makes the situation easier for tiling.

Figure 8.12 shows an actual implementation of tiled passive matrix display installed in a museum. Passive-matrix tiled panels to make a spherical OLED display [24]. Using a tiled arrangement of many small displays, the large screen achieved a curved profile using glass substrate. As this tiled display is intended for signage applications, it has a large 3 mm × 3 mm pixel pitch. (The panel

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Table 8.2 Viewing Distance Required for Signage Display

Pixel Size (mm)	Viewing Distance Required (m)
1	3.4
2	6.9
3	10.3
4	13.8
5	17.2
6	20.6
7	24.1
8	27.5
9	30.9
10	34.4

unit size is 24 mm × 96 mm before tiling.) To minimize interpanel artifacts, the interpixel distance inside the panel is the same as the interpixel distance of adjacent panels ($a = b$), as shown in Figure 8.13.

Although visual artifacts can be reduced by minimizing the nonemission region between the panels, it is very difficult to make a tile boundary invisible, because the eye is extremely sensitive to luminance or spatial discontinuities at linear boundaries, so that a luminance change of 10% of the normal visual acuity limit is detectable [25]. Lowe et al. [25] report an LCD system that removes the nonemission boundary using a seamless image guide array (Figure 8.14). LCD pixel emission (with nonboundary region) is propagated through arrays of S-shaped image guides so that the emissive area covers the whole screen with the width of the nonemission regions being equal to the width of the gaps between individual image guides. Nevertheless, extreme care must be taken if the intertile boundaries are to be invisible. The method could be applied to OLED displays to enable a seamless tiling display.

8.3.2 Active-Matrix Tiling

Large display prototypes using active-matrix tiling also have been reported [26, 27] (Figure 8.15). The main purpose of tiling is to eliminate the shadow-mask and the excimer laser annealing restrictions.

As already discussed, there are other alternate technologies developed to circumvent these issues, so the necessity of tiling technology for active-matrix displays is decreasing. The remaining merit of active-matrix tiling would be the freedom to make custom display formats and very large displays.

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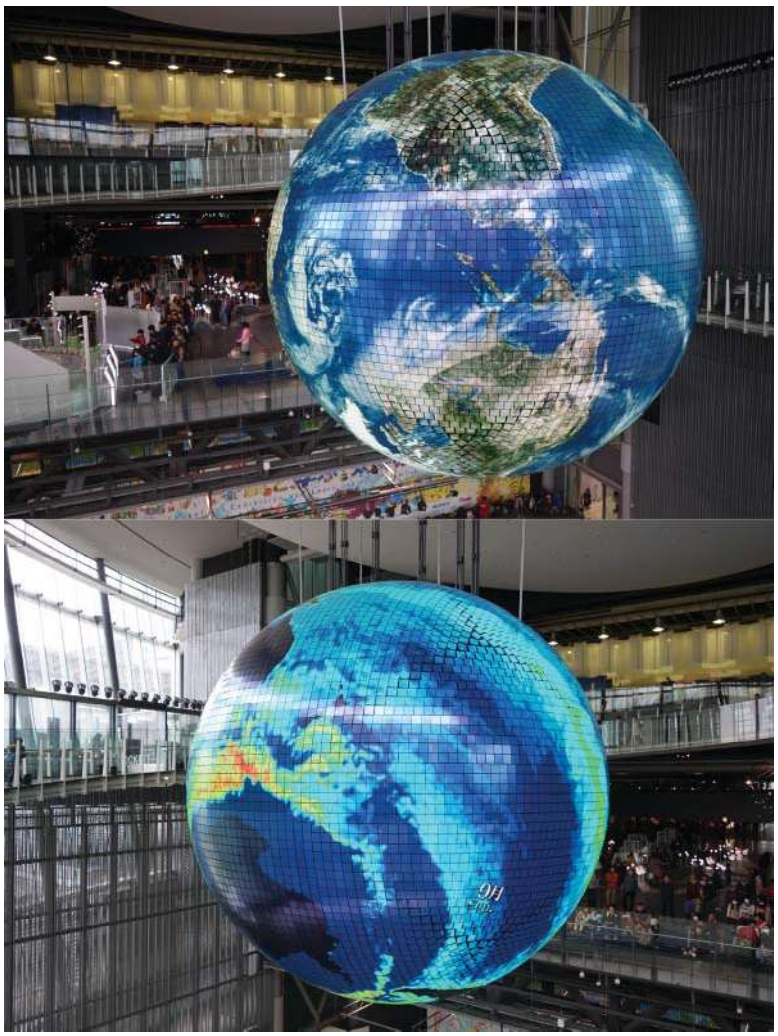


Figure 8.12 An example of a tiled passive-matrix display (demonstration at FPD International 2011"Geo-cosmos" spherical display in Miraikan museum, Japan by Mitsubishi Electric).

Figure 8.16 shows an overlapped tiling method reported by Shim et al. [27]. In the reported structure, the use of an index-matched transparent plate and the reduction of the air gap between the transparent plate and substrate 1 play very important roles to avoid the loss of emission from substrate 2. Also, use of a thin display module is very important to avoid black lines caused by the gap between substrate 1 and substrate 2 when viewed from a positive angle.

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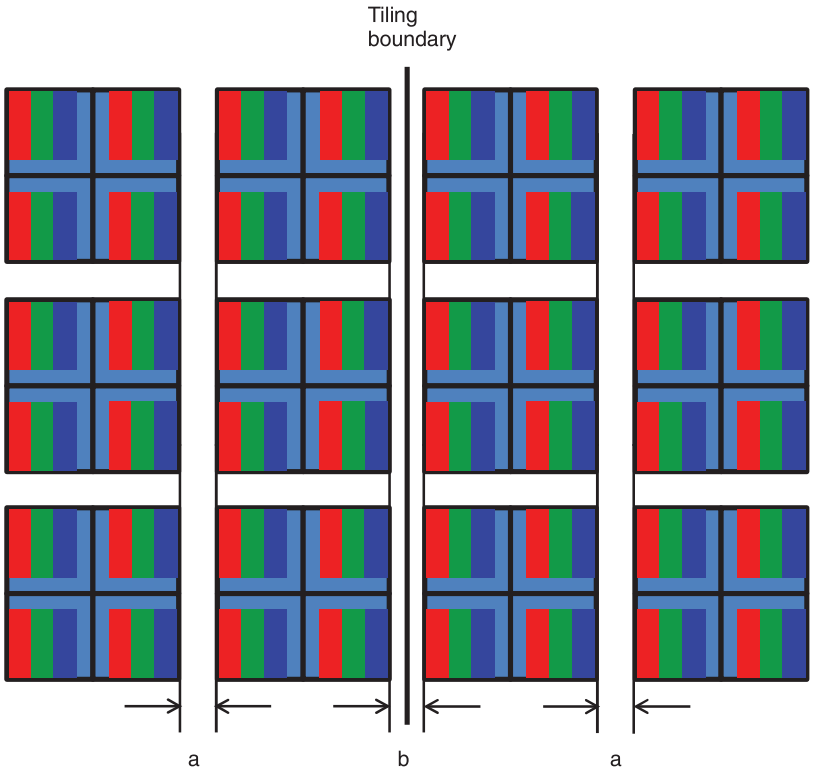


Figure 8.13 An example of a passive-matrix tiling pixel arrangement.

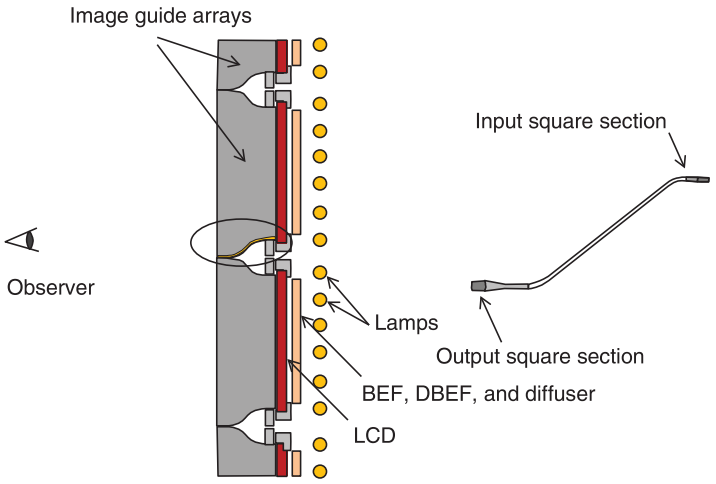


Figure 8.14 Seamless tiling using image guide arrays [25].

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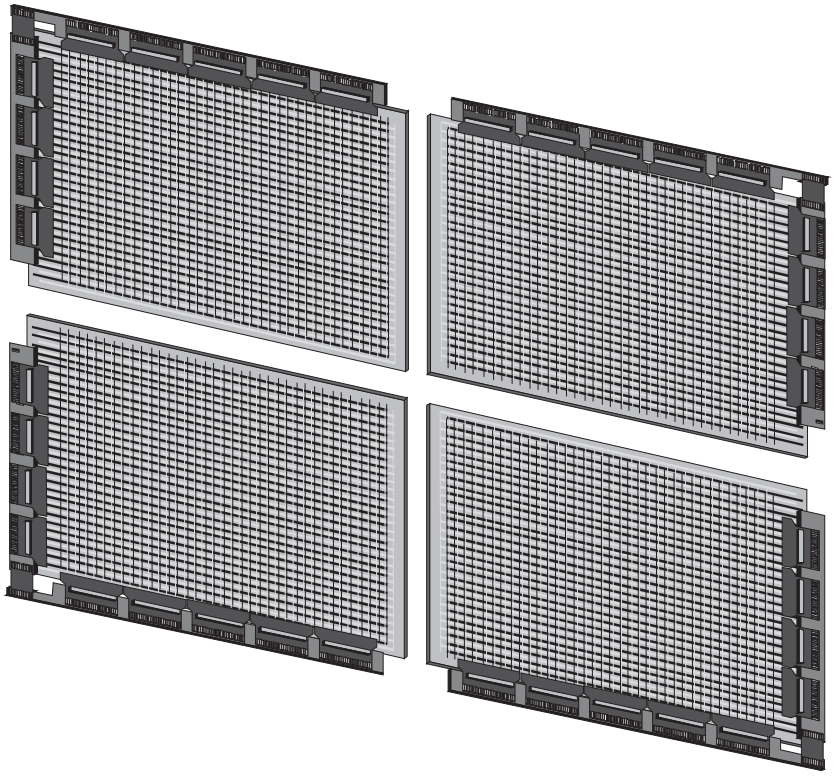


Figure 8.15 Tiling display using four OLED panels with blanket film encapsulation.

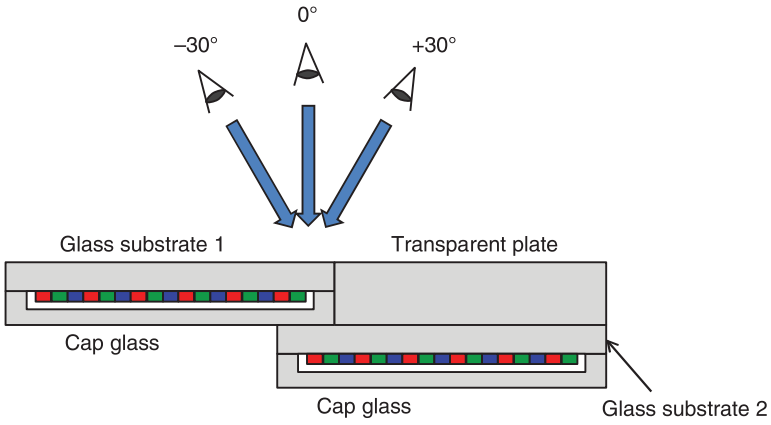


Figure 8.16 An example of active-matrix display tiling [27].

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Using an overlapped tiling approach introduces an undesired asymmetric artifact, which obscures the pixel on substrate 2 from negative observation angles.

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9

OLED Lighting

Although the efficacy of OLED lighting is still behind that of LEDs, there are several merits of OLED for lighting. As OLED is planar lighting source, the light is much softer than LEDs, which has concentrated bright light from the point source. Also the diffused light of OLED can be very close to the task surface without creating glare to the users [1].

The white-emission OLED device used for displays is very similar to the OLED lighting device (Figures 9.1 and 9.2), so the display techniques are mostly applicable in lighting applications. However, the specification for a lighting application should differ from that for a display. In particular, the light source must provide adequate color reproduction of the irradiated object. This metric is called the color rendering index (CRI).

9.1 PERFORMANCE IMPROVEMENT OF OLED LIGHTING

Figure 9.3 shows efficacy of commercial LEDs in the market [1]. The efficacy is improving year by year. Also it can be seen that the cool package LEDs have higher efficacy than warm package. Figure 9.4 shows the efficacy trend of OLED. When compared with Figure 9.3, white OLED efficacy is improving at a faster pace than LEDs.

The efficacy of fluorescent lamps on the market is around 60 lm/W, so OLED efficacy is already competitive with such conventional technologies. There is another aspect to have the best quality of light. The CRI discussed in the following section is an important metric, which quantifies apparent changes in the color of objects illuminated by a source, compared to the same objects illuminated by natural broadband sources such as daylight.

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Figure 9.1 An example of table lighting using OLED (demonstration at FPD International 2009 by Rohm).



Figure 9.2 An example of an OLED ceiling lamp (demonstration at FPD International 2009 by Lumiotec).

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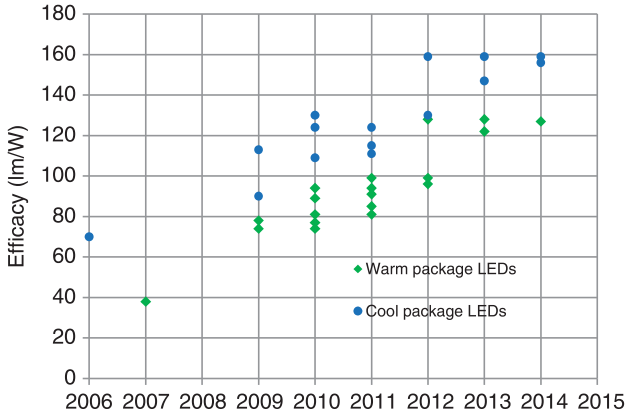


Figure 9.3 Efficacy of commercial LED packages.

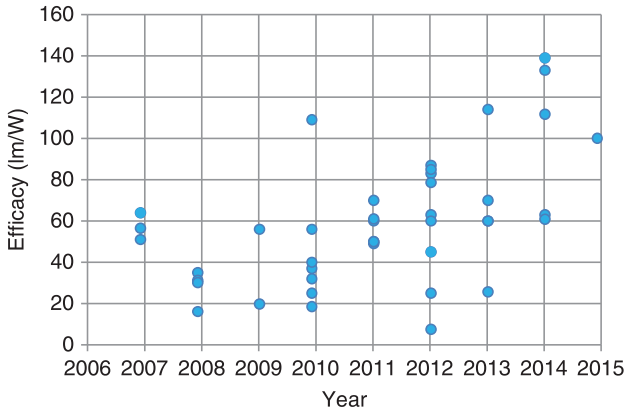


Figure 9.4 White OLED efficacy trend (extracted from SID digest database with keyword "lm/W OLED lighting").

9.2 COLOR RENDERING INDEX

The CRI is widely used to demonstrate the color reproduction of reflected light in lighting applications.

For the CRI calculation, the CIE1964 uniform color space (U^*, V^*, W^*) coordinate system is used (this color coordinate applies only to the CRI calculation):

$$W^* = 25Y^{1/3} - 17 \tag{9.1}$$

$$U^* = 13W^*(u - u_n) \tag{9.2}$$

$$V^* = 13W^*(v - v_n) \tag{9.3}$$

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Here, the coordinate set (u, v) is

$$\begin{aligned} u &= \frac{4X}{X + 15Y + 3Z} \\ &= \frac{4x}{-2x + 12y + 3} \\ v &= \frac{6Y}{X + 15Y + 3Z} \\ &= \frac{6y}{-2x + 12y + 3} \end{aligned} \tag{9.4}$$

where u_n and v_n are color coordinates of the light source.

As the color difference of the object between the standard light source and the sample light source are perceptually compensated according to color adaptation theory, so the following equations are applied:

$$\begin{aligned} u'_k &= u_r \\ v'_k &= v_r \\ u'_{ki} &= \frac{10.872 + 0.404\frac{c_r c_{ki}}{c_k} - 4\frac{d_r d_{ki}}{d_k}}{16.518 + 1.481\frac{c_r c_{ki}}{c_k} - \frac{d_r d_{ki}}{d_k}} \\ v'_{ki} &= \frac{5.520}{16.518 + 1.481\frac{c_r c_{ki}}{c_k} - \frac{d_r d_{ki}}{d_k}} \end{aligned} \tag{9.5}$$

where (u_k, v_k) is the color coordinate of the sample light source and (u_{ki}, v_{ki}) is the color coordinate of each (i)th test coupon when illuminated by the sample light source.

Coefficients c and d can be expressed as follows:

$$\begin{aligned} c &= \frac{(4.0 - u - 10.0v)}{v} \\ d &= \frac{1.708v + 0.404 - 1.481u}{v} \end{aligned} \tag{9.6}$$

Two color rendering values are commonly used: the general CRI (R_a) and the special CRI (R_i, where $i = 1$–15).

The spectrum distribution $S_r(\lambda)$ and $S_k(\lambda)$ for a standard light source and a sample light source is used to calculate the tristimulus value (X_r, Y_r, Z_r) and (X_k, Y_k, Z_k), respectively. For the ith sample color, tristimulus values for both light sources can be calculated as (X_{ri}, Y_{ri}, Z_{ri}) and (X_{ki}, Y_{ki}, Z_{ki}), respectively. Using

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Eqs. (9.4)–(9.6), we obtain

$$\begin{aligned} W_{ri}^* &= 25(Y_{ri})^{1/3} - 17 \\ U_{ri}^* &= 13W_{ri}^*(u_{ri} - u_r) \\ V_{ri}^* &= 13W_{ri}^*(v_{ri} - v_r) \\ W_{ki}^* &= 25(Y_{ki})^{1/3} - 17 \\ U_{ki}^* &= 13W_{ki}^*(u_{ki} - u_k) \\ V_{ki}^* &= 13W_{ki}^*(v_{ki} - v_k) \end{aligned} \tag{9.7}$$

Therefore, color difference (variation) ΔE_i ($i = 1, 2, 3, \ldots, 15$) in the CIE1964 color coordinate system can be calculated as follows:

$$\Delta E_i = \sqrt{(U_{ri}^* - U_{ki}^*)^2 + (V_{ri}^* - V_{ki}^*)^2 + (W_{ri}^* - W_{ki}^2)^2}. \tag{9.8}$$

The special CRI R_i is

$$R_i = 100 - 4.6\Delta E_i \tag{9.9}$$

and the general CRI R_a can be expressed as

$$R_a = \frac{1}{8}\sum_{i=1}^{8} R_i \tag{9.10}$$

A large CRI gives vivid, natural colors. Normally, blackbody radiation spectrum is used for the standard light source. According to Eqs. (9.8)–(9.10), color rendering indices show the color difference between the color made by the sample source and the color made by the standard light source; therefore, a spectrum closer to the blackbody radiation needs to be achieved for a high CRI value. This is why white OLED or white emission by LED + fluorescence shows a higher CRI than a white light made by a peaked LED emission or a peaked laser emission. In the case of display, a primary color with a broader spectrum causes narrower color reproduction of a display (calculation for the display is discussed in Section 4.2.3), so attention should be paid to the difference between lighting and display.

9.3 OLED LIGHTING REQUIREMENT

As OLED lighting [2–4] is an emerging technology, customer requirements are not yet fixed and will change over time. As to the current general requirements, the ENERGY STAR® document, prepared by the US Department of Energy, provides useful information. Here we discuss the specifications outlined in the ENERGY STAR program *Requirements for Solid-State Lighting Luminaires Eligibility Criteria*, version 1.2 (Final Criteria).

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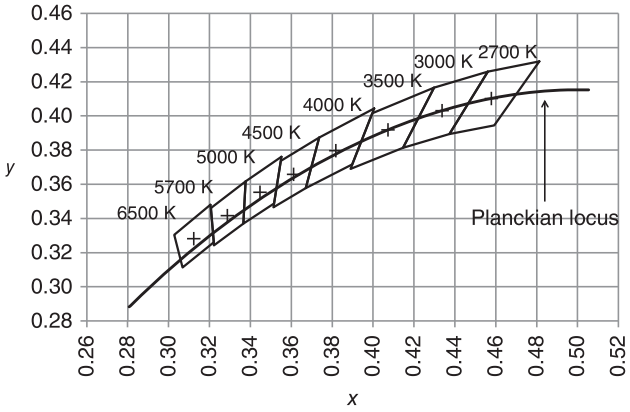


Figure 9.5 Graph showing eight nominal correlated color temperature (CCT) quadrangles on a CIE1931 chromaticity diagram.

9.3.1 Correlated Color Temperature (CCT)

As discussed in Section 4.2.5, the white color on a Planckian locus can be expressed by color temperature. However, the actual color coordinate of white emission may not be exactly on the Planckian locus. To express the color of near-white color emission not on the Planckian locus, the correlated color temperature (CCT) is used, defined as the color temperature of the (u, v) color coordinate on the Planckian locus, which is closest to the emissive color.

For CCT calculation, the CIE1976 (discussed in Section 4.2.3) color space is used, with which the color can be calculated using the following equations:

$$u' = \frac{4x}{-2x + 12y + 3} \tag{9.11}$$

$$v' = \frac{9y}{-2x + 12y + 3} \tag{9.12}$$

The distance from the Planckian locus on the CIE 1976 (u', v') coordinates is referred to as Δuv.

In the ENERGY STAR document, it is noted that a luminaire should have a CCT of 2700, 3000, 3500, 4000, 4500, 5000, 5700, or 6500 K.

The document also mentions that the luminaire must fall within the specified seven-step chromaticity quadrangles, defined by the seven-step (seven times standard deviation) McAdam ellipse (see Table 9.1 and Figure 9.5).

The human eye is very sensitive to any deviation from the blackbody line (described as the Planckian locus in Figure 9.5), so it is important to design a device formulation with a white point as close to the blackbody line as possible.

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Table 9.1 CIE Coordinates of Nominal CCTs

	2700 K		3000 K		3500 K		4000 K		4500 K		5000 K		5700 K		6500 K	
	x	*y*	*x*	*y*	*x*	*y*	*x*	*y*	*x*	*y*	*x*	*y*	*x*	*y*	*x*	*y*
Center point	0.4578	0.4101	0.4338	0.4030	0.4073	0.3917	0.3818	0.3797	0.3611	0.3658	0.3447	0.3553	0.3287	0.3417	0.3123	0.3282
Tolerance quadrangle	0.4813	0.4319	0.4562	0.4260	0.4299	0.4165	0.4006	0.4044	0.3736	0.3874	0.3551	0.3760	0.3376	0.3616	0.3205	0.3481
	0.4562	0.4260	0.4299	0.4165	0.3996	0.4015	0.3736	0.3874	0.3548	0.3736	0.3376	0.3616	0.3207	0.3462	0.3028	0.3304
	0.4373	0.3893	0.4147	0.3814	0.3889	0.3690	0.3670	0.3578	0.3512	0.3465	0.3366	0.3369	0.3222	0.3243	0.3068	0.3113
	0.4593	0.3944	0.4373	0.3893	0.4147	0.3814	0.3898	0.3716	0.3670	0.3578	0.3515	0.3487	0.3366	0.3369	0.3221	0.3261

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9.3.2 Other Requirements

Table 9.2 lists the general requirements specified by the ENERGY STAR program. It should be noted that the lifetime of a panel is defined by 70% luminance: T_{70}.

Table 9.3 lists the near-term application requirements (category A). Here, luminaire efficacy is defined as follows:

$$\eta_{\text{lum}} = \frac{P_{\text{lum,out}}}{P_{\text{lum,in}}} \tag{9.13}$$

where

η_{lum} = luminaire efficacy
$P_{\text{lum,out}}$ = luminaire light output (including fixture efficacy and thermal effects)
$P_{\text{lum,in}}$ = luminaire input power

To satisfy the entire application requirement presented in Table 9.3, an efficacy of 35 lm/W is desired for near-term application. The ENERGY STAR document also mentions that 70 lm/W is the aim in the future (category B).

9.4 LIGHT EXTRACTION ENHANCEMENT OF OLED LIGHTING

Ecology has become a matter of global interest recently, as wasted energy causes multiple issues, such as global warming, depletion of oil resource and air pollution. Due to such reasons, high-efficiency lighting technology has been desired. OLED lighting is also subjected to such requirements. To improve the luminous efficacy, various light extraction methods are used.

9.4.1 Various Light Absorption Mechanisms

As discussed in Section 2.4.3, the major reasons for OLED to lose emission energy are surface plasmons, waveguided-mode, and substrate-mode absorption.

The following sections illustrate how to reduce light absorption related to such major issues.

There is also important thing to be considered for high efficiency. During the trial to reduce the emissive energy loss, light released from surface plasmon absorption can be trapped by waveguided or substrate mode. Also light released from waveguided mode can be trapped by substrate mode. It is quite important to consider how reduced loss mechanism leads to the actual output.

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Table 9.2 General ENERGY STAR Program Requirements

All Luminaires	**Color spatial uniformity**	**Within 0.004 from weighted average point on CIE1976 (u', v') diagram**
	Color maintenance	**Within 0.007 on CIE1976 (u', v') diagram over lifetime**
	Color rendering index	**Indoor luminaire shall have a minimum CRI of 75**
Modules/arrays	L_{70}	Residential indoor: 25,000 h
		Residential outdoor: 35,000 h
		All commercial: 35,000 h
Power supplies	Power factor	Residential $\geqq$ 0.70
		Commercial $\geqq$ 0.90
	Minimum operating temperature	Minimum operating temperature −20°C or below when used in luminaires intended for outdoor applications
	Maximum measured power supply case or manufacturer designated temperature Measurement point (TMPPS) Temperature	Not to exceed the power supply manufacturer maximum recommended case temperature or TMP when measured during in situ operation
	Output operating frequency	$\geq$ 120 Hz
	Electromagnetic and radio frequency interference	Power supplies designated by the manufacturer for residential applications must meet FCC requirements for consumer use Power supplies designated by the manufacturer for commercial applications must meet FCC requirements for nonconsumer use
	Noise	Power supply shall have a Class A sound rating
	Transient protection	Power supply shall comply with IEEE C.62.41-1991, Class A operation. The line transient shall consist of seven strikes of a 100 kHz ring wave, 2.5 kV level, for both common mode and differential mode

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Table 9.3 Near-Term ENERGY STAR Application Requirements

Definition	Luminaire efficacy	Luminaire light output (includes fixture efficiency and thermal effects)/Luminaire Input Power				
Category A: Near-term Applications						
Residential Application						
	Under-cabinet kitchen lighting	Portable desk task lights	Recessed downlights and pendant-mounted downlights	Ceiling- mounted luminaires with diffusers	Cove lighting	Surface- mounted luminaires with directional head(s)
Minimum light output	125 lm (initial)	200 lm (initial)	≦ 4.5″ Aperture: 345 lumens (initial)	≤ 8″ Aperture: 375 lumens (initial)	200 lm(initial)	200 lm(initial)
			> 4.5″ Aperture: 575 lumens (initial)	> 8″ Aperture: 750 lumens (initial)		
Minimum luminaire efficacy	24 lm/W	29 lm/W	35 lm/W	30 lm/W	45 lm/W	35 lm/W
Allowable CCTs	2700, 3000, and 3500 K	2700, 3000, 3500, 4000, 4500, and 5000 K	2700, 3000, and 3500 K	2700, 3000, and 3500 K	2700, 3000, and 3500 K	2700, 3000, and 3500 K
	Outdoor wall-mounted porch lights	Outdoor step lights	Outdoor pathway lights	Outdoor pole/arm-mounted decorative luminaires		
Minimum light output	150 lm (initial)	50 lm (initial)	100 lm (initial)	300 lm (initial)		
Minimum luminaire efficacy	24 lm/W	20 lm/W	25 lm/W	35 lm/W		

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	Outdoor wall-mounted porch lights	Outdoor step lights	Outdoor pathway lights	Outdoor pole/arm-mounted decorative luminaires
Minimum light output	150 lm (initial)	50 lm (initial)	100 lm (initial)	300 lm (initial)
Minimum luminaire efficacy	24 lm/W	20 lm/W	25 lm/W	35 lm/W
	Recessed downlights and pendant-mounted downlights	Under-cabinet shelf-mounted task lighting	Portable desk task lights	Wall wash luminaires
Minimum light output	≦ 4.5″ Aperture: 345 lumens (initial) > 4.5″ Aperture: 575 lumens (initial)	125 lm (initial)	200 lm (initial)	575 lm (initial)
Minimum luminaire efficacy	35 lm/W	29 lm/W	29 lm/W	40 lm/W
Allowable CCTs	2700, 3000, 3500, 4000, 4500, and 5000 K	2700, 3000, 3500, 4000, 4500, and 5000 K	2700, 3000, 3500, 4000, 4500, and 5000 K	2700, 3000, 3500, 4000, 4500, and 5000 K
	Bollards			
Minimum light output	Luminaire shall deliver < 15% of total lumens in the 90 – 110° zone and emit no light over 110°.			
Minimum luminaire efficacy	35 lm/W			
Category B: future performance targets				
Luminaire efficacy	≧ 70 lm/W			

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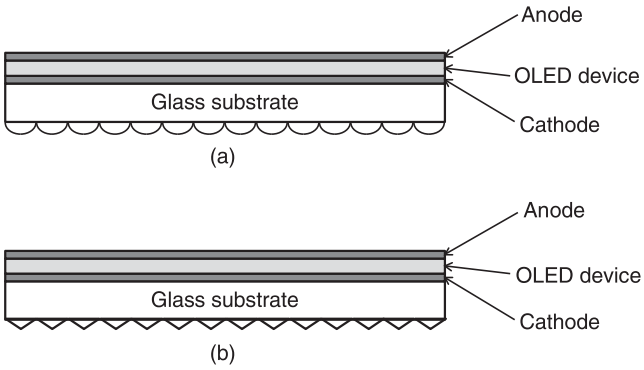


Figure 9.6 Schematic representations of (a) a microlens array and (b) a micropyramidal structure.

9.4.2 Microlens Array Structure

Figure 9.6 presents diagrams of the structures of a microlens array and a micropyramid used for light extraction.

To most effectively extract OLED emission light which propagates in a substrate, using a lens, the dimensions of the lens must be much greater than those of the emission area so that the lens covers all the luminous flux emitted from the area [5]. However, with this approach, the OLED emission area needs to be small enough compared with the lens area (e.g., to estimate the total amount of luminous flux from the emission coupon, a hemispheric lens with a much larger area than the emission coupon is used). In actual lighting panel design, it is not realistic to place a large lens structure over the emission area, so this approach is seldom used for an actual product. Instead, a microlens array with small diameters such as 10 μm is used. This light extraction method is using a different approach, such as a combination of light diffusion and refraction on the substrate surface.

9.4.3 Diffusion Structure

To extract the light in a substrate, a diffuser structure is also effective. Figure 9.7 shows the spin-coat-type diffusion layer that was reported by Tyan et al. [6].

Device A has two kinds of light scattering layers, external extraction structure (EES) at the glass–air boundary and internal extraction structure (IES) at the OLED device–glass boundary, whereas device B has EES only at the glass–air boundary. Among the total light flux emitted in the OLED device, there is (1) some that cannot exit the OLED device (waveguided mode, discussed in Section 2.4.3; waveguided-mode light is lost due to the energy loss during multiple reflection or light extraction at the OLED device edge),

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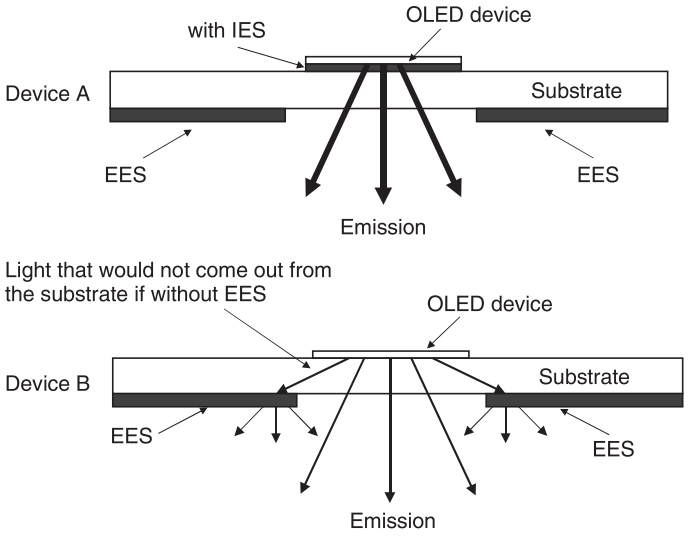


Figure 9.7 Diagrams of an internal extraction structure (IES) and an external extraction structure (EES).

(2) some that is lost due to plasmon absorption (light absorption caused by the coupling between plasmon, a type of electron vibration in metal, and the electromagnetic field of the light), (3) some successfully extracted from the OLED device, but which cannot exit the substrate (substrate mode, discussed in Section 2.4.3; substrate-mode light is also lost due to multiple reflection or extracted at the substrate edge), or (4) some extracted to the air and which reaches the observers (air mode). EES decreases the substrate-mode light and IES decreases the waveguided-mode light.

Figure 9.8 shows emission from an actual device. With IES, the intensity of the light emitted from the OLED device area is high due to light extraction from the waveguided mode. On the other hand, with only EES, emission intensity is lower in the device area due to the light loss caused by the waveguided mode, while light emission in the area surrounding the device occurs due to a larger amount of light propagated in the OLED device; some of the propagated light is extracted to the surrounding area by means of the EES structure.

Table 9.4 shows the actual experimental data. The device with EES has 1.92 times the external quantum efficiency of the non-EES device, and the device with IES has 2.28 times the external quantum efficiency. (This method is applicable for lighting but not suitable for displays because the diffusion capability of extraction layers causes image blurring and color mixture problems in the case of display applications.)

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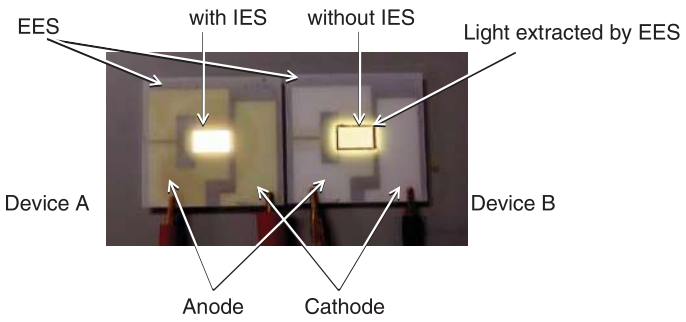


Figure 9.8 Image showing actual emission using IES and EES techniques.

Table 9.4 Light Extraction Experimental Data

Structure	Current Density (mA/cm^2)	Luminance (cd/m^2)	External Quantum Efficiency	Current efficiency (cd/A)	Color coordinate *x*	Color coordinate *y*	Voltage (V)	Power efficacies (lm/W)
—	5	651	5.7	13.0	0.493	0.434	3.1	13.0
EES only	5	1269	11.0	25.4	0.492	0.430	3.3	24.1
IES only	5	1430	13.0	28.6	0.475	0.408	3.1	29.0

9.4.4 Diffraction Structure

Diffraction structure is also used to extract the substrate-mode light. Figure 9.9 depicts the light extraction enhancement method using diffraction structure. After preparation of the diffraction structure and the high-refractive-index layer including compounds such as TiO_2 or SiN_x, the OLED device is fabricated. Periodical diffraction structure is fabricated between the substrate and the high-refractive-index layer. In the case of normal diffraction lattices in other industries, the pitch is designed so that the light path length difference between adjacent projections is equal to an integer times the wavelength of a monochromatic light. However, in the case of OLED lighting, white emission intensity with multiple wavelengths must be enhanced. To make this happen, a shorter lattice pitch close to or less than the visible-light wavelength is used. In such cases, light is scattered according to Mie scattering theory, which has minimal wavelength dependence.

9.4.5 Reduction of Plasmon Absorption

9.4.5.1 Plasmonic Loss Mechanism

Figure 9.10 shows the so-called Surface-plasmon polariton wave (SPP wave). It is a charge density oscillation, which propagates along the metal–dielectric interface.

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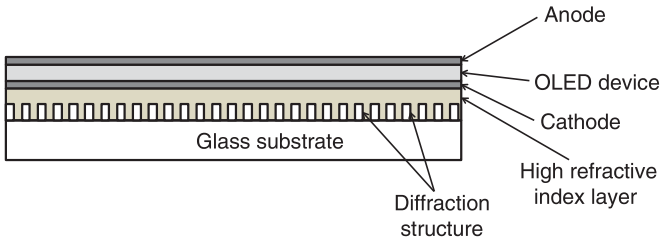
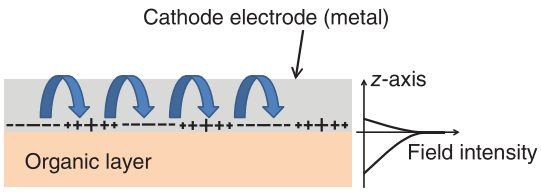


Figure 9.9 Schematic representation of light extraction enhancement employing diffraction structure.

Figure 9.10 Surface-plasmon polariton wave.



Electric dipoles associated with the OLED emitters couple with this SPP wave and lose a significant amount of energy. The electric field of the SPP is a so-called evanescent field, which decays rapidly as the distance from the dielectric–metal interface is increased.

Meerheim et al. made a quantitative study of energy loss in OLEDs by simulation [7] and showed that the surface plasmon loss can be significantly reduced by increasing the thickness of the ETL, which lies between the SPP wave and the radiative emitters. It was also concluded that the major portion of the loss is converted to a waveguided mode unless an appropriate outcoupling method is combined with surface plasmon loss reduction.

Although ETL thickness increase can reduce the plasmon loss, thick ETL causes larger voltage drop, which reduces the OLED device efficiency. Kato et al. combined ETL thickness increase with high mobility ETL and Internal Extraction Structure, and achieved very high white OLED efficacy 139 lm/W [8].

Other than the ETL thickness increase, plasmon loss can be reduced by horizontally oriented dipoles [9] (discussed in Section 2.4.3.4) or random structure in metal–dielectric contact [10, 11].

9.5 COLOR TUNABLE OLED LIGHTING

There are two types of color tunable OLED lighting devices as shown in Figure 9.11. The left structure has red, green, and blue lines, spatially allocated by mask patterning method. (Stripe-type color tunable OLED. Pixelation

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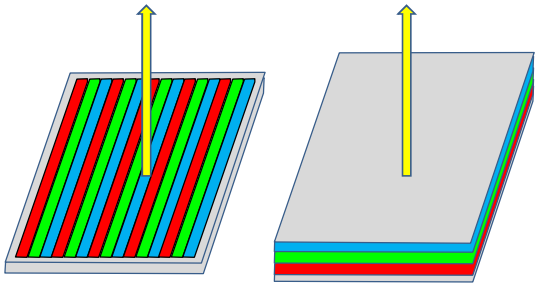


Figure 9.11 Two types of color tunable OLED device structures.

can also be used.) The structure requires photopatterning as well as shadow mask patterning to fabricate. On the other hand, the right structure in Figure 9.11 does not need color patterning, but the devices are stacked vertically. (Vertically stacked color tunable OLED. Also called polychromatic OLED.)

Stripe-type needs to mix the color to show arbitrary colors, so diffuser film needs to be attached on the structure. The OLED device can be the same as OLED display, so OLED formulation can be simple.

In the case of vertically stacked color tunable OLED, no diffuser is necessary because the color can be mixed when the light comes out. (So metallic appearance can be made when it is turned off.) It does not require fine patterning; however, it requires very low-resistance transparent conductor technology for intermediate electrode, to avoid the voltage drop of the device.

Figure 9.12 shows the structure of vertically stacked color tunable OLED device [12, 13]. As red, green, and blue OLED devices must be independently controlled, electric current is applied to intermediate electrode. Therefore, anode, intermediate electrode, and cathode electrode must have low enough resistance to avoid the voltage drop. Also to have high transmittance, each electrode needs to have low optical absorption. Eventually, vertically stacked

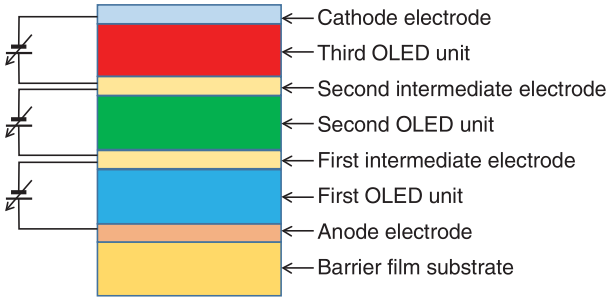


Figure 9.12 Structure of vertically stacked color tunable OLED.

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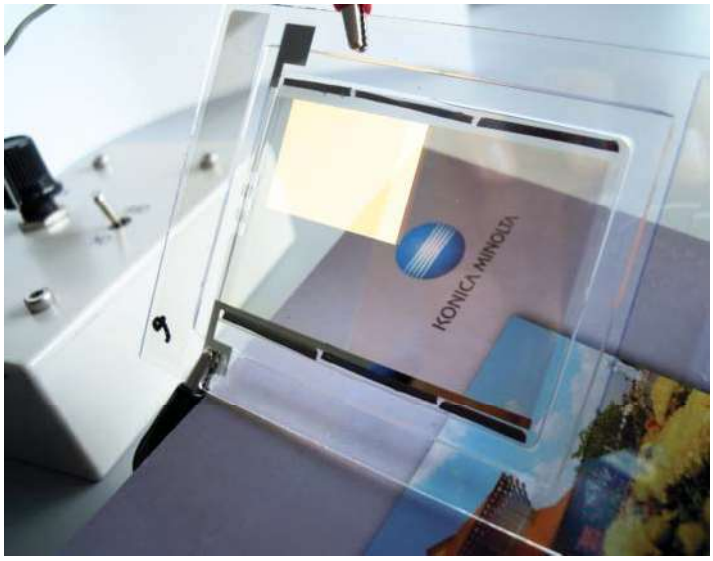


Figure 9.13 Transparent OLED lighting device [12].

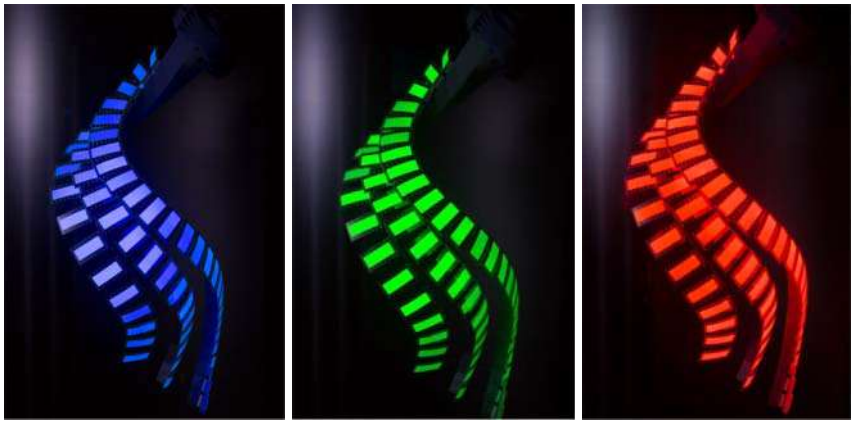


Figure 9.14 Lighting instrument using vertically stacked color tunable OLED lighting [12].

color tunable OLED is a three-unit stack of transparent OLED device. With the same technology, transparent OLED device can be fabricated as shown in Figure 9.13. By using high-transmittance and low resistance transparent conductor, three transparent OLED devices can be stacked successfully to show 16 million color reproduction of vertically stacked OLED devices as shown in Figure 9.14.

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The technology can be applied to OLED displays, which may significantly enhance the device lifetime (discussed in Section 5.1.1.3).

9.6 OLED LIGHTING DESIGN

The pixel size in an active-matrix display ranges within hundreds of micrometers, so any voltage drop occurring in a pixel is trivial. However, the dimensions of devices designed for lighting applications are much larger (e.g., within the centimeter range), so voltage drop in these devices can be significant, which may cause a serious luminance uniformity issue.

9.6.1 Resistance Reduction

The light emission side of an OLED electrode (anode electrode in the case of bottom emission structure) must be transparent, so ITO or IZO is used. As these compounds have high resistance values in the range of tens or hundreds of ohms per square, electric current should be supplied from multiple feeding points to ensure better uniformity. Moreover, the feeding points should be connected to the OLED panel pad via low-resistance (e.g., Al or Ca) wiring. (See Section 6.4.3 for voltage drop for AMOLED displays.)

Also, regarding the transparent electrode, the process should be optimized to ensure that resistivity is as low as possible and that there is good transparency.

9.6.2 Current Reduction

To reduce the electric current, several approaches are generally used in combination, including the following:

1. Current efficiency enhancement
2. Tandem device design
3. Serial connection of an OLED device.

Current efficiency enhancement can be achieved by material change, such as improving the emission capability using phosphorescent material [1, 2] (discussed in Section 2.4.2.3). Also, light extraction enhancement, discussed in Section 9.4, can reduce the electric current necessary to obtain the same panel luminance and also provide better luminance uniformity (thus eliminating mura) by reducing the lower voltage drop due to low driving current.

Use of a tandem device structure (discussed in Section 6.4.3) is also an effective approach to decrease the electric current. Theoretically, a two-stack tandem structure reduces the electric current by half, and a three-stack layout reduces the current to a third of its original value. (For better implementation, the light path length should be carefully designed for each emission layer.) Tandem structure also has the merit of extending the lifetime of an OLED device.

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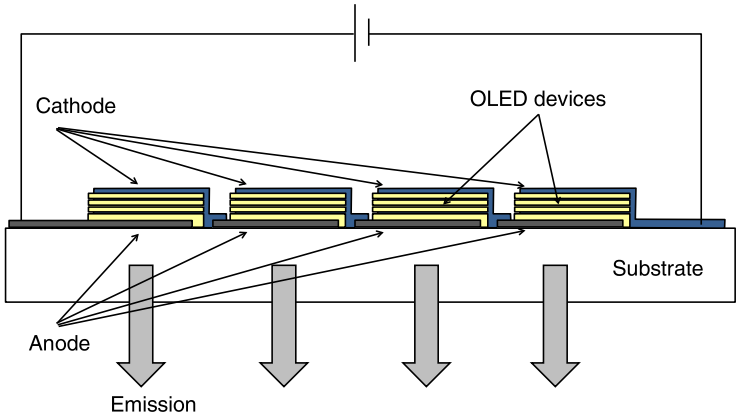


Figure 9.15 Schematic representation of a serial connection structure.

As discussed in Section 6.4.3, N times stack tandem structure results in N^n times the lifetime (two-stack tandem OLED gives 2.82 times and three-stack gives 5.20 times the lifetime, as theoretically discussed). However, creating a tandem structure entails an increased number of process steps, thus increasing the overhead manufacturing cost.

A serial connection structure such as that shown in Figure 9.15 is also used to reduce the electric current. The emission area is partitioned into several areas. By means of the normal OLED fabrication process, OLED devices are fabricated in each partition simultaneously. The cathode electrode area is extended so that it is connected to the anode electrode of the next partition. As a result, the partitions are connected in series, and, therefore, N times light flux is generated with the same current compared with a normal OLED structure. The scenario sounds similar to a tandem structure; however, unlike the tandem structure, the serial structure does not improve lifetime or device longevity because there is also a reduction in the aperture ratio, which offsets the current reduction advantage. It is important to combine all the technologies discussed above in order to design an OLED lighting panel with good uniformity.

9.7 ROLL-TO-ROLL OLED LIGHTING MANUFACTURING

Tsujimura et al. presented large-scale roll-to-roll manufacturing of OLED lighting device in 2014 [14, 15]. It was claimed that flexible OLED has advantages over LEDs in terms of lightweight, thinness, and flexibility. A flexible OLED is capable of forming arbitrary curvature, so could be used for new applications, which conventional point, linear and circular light sources could not make possible (Figure 9.16).

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Figure 9.16 OLED Tulip illumination demonstrated in Japanese theme park with shining flexible-OLED petals.

To fabricate a flexible OLED lighting panel, there are two approaches possible:

1. Laser liftoff method (Section 8.1.3)
2. Roll-to-roll method.

Laser liftoff is a method used for OLED displays. The flexible pattern is fabricated on polyimide coated onto the glass, so the pattern size can be very small due to the low thermal expansion of the glass substrate. Accurate patterning can be achieved, so high-resolution display manufacturing is possible. Roll-to-roll manufacturing cannot thus far be applied to displays, leaving the laser liftoff method as the sole option for flexible high-resolution display manufacturing.

On the other hand, OLED lighting does not require high-resolution patterning. Therefore, it is possible to adopt a manufacturing method with higher manufacturability. Roll-to-roll manufacturing has been used in many industries to achieve low manufacturing cost. Of course, the laser liftoff method can still be adopted for OLED lighting manufacturing. However, it was claimed that there are several advantages in roll-to-roll manufacturing compared with the laser liftoff method because laser lift off method has the following features:

1. Laser liftoff method requires very expensive equipment, which adds depreciation cost.

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2. The device is released after fabricating all the processing. If the device yield is lost in the release step, this impacts the device costs (variable costs).
3. The polyimide and mother glass are expensive materials, and the glass brings further costs associated with issues in recycling.
4. In the case of roll-to-roll manufacturing, no high cost equipment is necessary for making flexible device, there is no release step to affect yields and no additional cost related to flexible substrates.

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Appendix

The wavelength values of the color matching function, which is necessary for calculation of the tristimulus value x, y, z from the emission spectrum, are listed in Table A.1.

Table A.1 Color Matching Function λ Values

Wavelength (nm)	$\bar{x}(l)$	$\bar{y}(l)$	$\bar{z}(l)$
360	0.00013	3.92E−06	0.000606
365	0.000232	6.97E−06	0.001086
370	0.000415	1.24E−05	0.001946
375	0.000742	2.2E−05	0.003486
380	0.001368	0.000039	0.00645
385	0.002236	0.000064	0.01055
390	0.004243	0.00012	0.02005
395	0.00765	0.000217	0.03621
400	0.01431	0.000396	0.06785
405	0.02319	0.00064	0.1102
410	0.04351	0.00121	0.2074
415	0.07763	0.00218	0.3713
420	0.13438	0.004	0.6456
425	0.21477	0.0073	1.03905
430	0.2839	0.0116	1.3856
435	0.3285	0.01684	1.62296
440	0.34828	0.023	1.74706
445	0.34806	0.0298	1.7826
450	0.3362	0.038	1.77211

(*Continued*)

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Table A.1 (Continued)

Wavelength (nm)	$\bar{x}(l)$	$\bar{y}(l)$	$\bar{z}(l)$
455	0.3187	0.048	1.7441
460	0.2908	0.06	1.6692
465	0.2511	0.0739	1.5281
470	0.19536	0.09098	1.28764
475	0.1421	0.1126	1.0419
480	0.09564	0.13902	0.81295
485	0.05795	0.1693	0.6162
490	0.03201	0.20802	0.46518
495	0.0147	0.2586	0.3533
500	0.0049	0.323	0.272
505	0.0024	0.4073	0.2123
510	0.0093	0.503	0.1582
515	0.0291	0.6082	0.1117
520	0.06327	0.71	0.07825
525	0.1096	0.7932	0.05725
530	0.1655	0.862	0.04216
535	0.22575	0.91485	0.02984
540	0.2904	0.954	0.0203
545	0.3597	0.9803	0.0134
550	0.43345	0.99495	0.00875
555	0.51205	1	0.00575
560	0.5945	0.995	0.0039
565	0.6784	0.9786	0.00275
570	0.7621	0.952	0.0021
575	0.8425	0.9154	0.0018
580	0.9163	0.87	0.00165
585	0.9786	0.8163	0.0014
590	1.0263	0.757	0.0011
595	1.0567	0.6949	0.001
600	1.0622	0.631	0.0008
605	1.0456	0.5668	0.0006
610	1.0026	0.503	0.00034
615	0.9384	0.4412	0.00024

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Table A.1 (Continued)

Wavelength (nm)	$\bar{x}(l)$	$\bar{y}(l)$	$\bar{z}(l)$
620	0.85445	0.381	0.00019
625	0.7514	0.321	0.0001
630	0.6424	0.265	5E−05
635	0.5419	0.217	0.00003
640	0.4479	0.175	0.00002
645	0.3608	0.1382	0.00001
650	0.2835	0.107	0
655	0.2187	0.0816	0
660	0.1649	0.061	0
665	0.1212	0.04458	0
670	0.0874	0.032	0
675	0.0636	0.0232	0
680	0.04677	0.017	0
685	0.0329	0.01192	0
690	0.0227	0.00821	0
695	0.01584	0.005723	0
700	0.011359	0.004102	0
705	0.008111	0.002929	0
710	0.00579	0.002091	0
715	0.004109	0.001484	0
720	0.002899	0.001047	0
725	0.002049	0.00074	0
730	0.00144	0.00052	0
735	0.001	0.000361	0
740	0.00069	0.000249	0
745	0.000476	0.000172	0
750	0.000332	0.00012	0
755	0.000235	8.48E−05	0
760	0.000166	0.00006	0
765	0.000117	4.24E−05	0
770	8.31E−05	0.00003	0
775	5.87E−05	2.12E−05	0
780	4.15E−05	1.5E−05	0
785	2.94E−05	1.06E−05	0

(*Continued*)

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Table A.1 (Continued)

Wavelength (nm)	$\bar{x}(l)$	$\bar{y}(l)$	$\bar{z}(l)$
790	2.07E−05	7.47E−06	0
795	1.46E−05	5.26E−06	0
800	1.03E−05	3.7E−06	0
805	7.22E−06	2.61E−06	0
810	5.09E−06	1.84E−06	0
815	3.58E−06	1.29E−06	0
820	2.52E−06	9.11E−07	0
825	1.78E−06	6.42E−07	0
830	1.25E−06	4.52E−07	0

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