

U.S. Patent No. 12,133,429

1[pre]: A display panel, comprising a display region and a non-display region disposed on at least one side of the display region, wherein the display panel comprises:

1[a]: a substrate;

1[b]: a shielding layer located on the substrate, wherein the shielding layer comprises a plurality of shielding blocks and a converging wire electrically connected to the plurality of shielding blocks, and the converging wire is located on at least one side of the plurality of shielding blocks;

1[c]: a pixel driving circuit layer located on the shielding layer, wherein the pixel driving circuit layer comprises a plurality of pixel driving circuits located in the display region, each of the plurality of pixel driving circuits at least partially overlaps a corresponding one of the shielding blocks; and

1[d]: a plurality of power supply lines disposed on a side of the shielding layer away from the substrate, wherein the plurality of power supply lines are electrically connected to the converging wire through a plurality of through holes;

1[e]: wherein the converging wire between two adjacent ones of the plurality of through holes is disposed according to a shortest distance between the two adjacent through holes.

2: The display panel according to claim 1, wherein the converging wire between the two adjacent through holes is linear in arrangement.

3: The display panel according to claim 2, wherein the converging wire is linear in arrangement and the plurality of through holes overlappingly disposed on the converging wire are linear in arrangement.

4: The display panel according to claim 1, wherein the converging wire comprises a first converging wire, and the first converging wire comprises a plurality of first connection sections and a plurality of second connection sections; wherein each of the plurality of second connection sections is connected between a middle portion of two adjacent first plurality of connection sections, a width of each of the plurality of first connection sections is greater than a width of each of the plurality of second connection sections, and the plurality of power supply lines are electrically connected to the plurality of first connection sections through the plurality of through holes.

5: The display panel according to claim 4, wherein the plurality of pixel driving circuits are arranged in an array in a first direction and a second direction, each of the plurality of first connection sections is electrically

connected to the plurality of shielding blocks corresponding to a column of the plurality of pixel driving circuits arranged along a first direction.
6: The display panel according to claim 5, wherein a periphery of each of the plurality of first sections is arc shaped, the plurality of second sections are linearly shaped, a maximum width of each of the plurality of first sections is greater than the width of each of the plurality of second sections.
7[a]: The display panel according to claim 1, wherein the non-display region comprises: a first non-display region and a second non-display region disposed on two sides of the display region, wherein the first non-display region comprises a bending sub-region, and the display panel bends at the bending sub-region; and
7[b]: the converging wire comprises a first converging wire arranged in the first non-display region, and the plurality of power supply lines are electrically connected to the plurality of first connection sections at least through the plurality of through holes.
8: The display panel according to claim 7, wherein the converging wire comprises a second converging wire arranged in the second non-display region, and the plurality of power supply lines are electrically connected to the plurality of second connection sections through the plurality of through holes.
9[pre]: The display panel according to claim 1, wherein the pixel driving circuit layer comprises:
9[a]: a semiconductor layer disposed on a side of the shielding layer away from the substrate;
9[b]: a first insulating layer disposed on a side of the semiconductor layer away from the substrate;
9[c]: a first gate metal layer disposed on a side of the first insulating layer away from the substrate;
9[d]: a second insulating layer disposed on a side of the first gate metal layer away from the substrate;
9[e]: a second gate metal layer disposed on a side of the second insulating layer away from the substrate; and
9[f]: a third insulating layer disposed on a side of the second gate metal layer away from the substrate;
9[g]: wherein the first conductive layer is disposed on a side of the third insulating layer away from the substrate, the plurality of power supply lines of the first conductive layer are electrically connected to the converging wire through the plurality of through holes, and the plurality of through holes penetrate through the first insulating layer, the second insulating layer, and the third insulating layer.
10[pre]: The display panel according to claim 9, wherein the pixel driving circuit layer further comprises:
10[a]: a fourth insulating layer disposed between the second gate metal layer and the third insulating layer; and
10[b]: a second conductive layer disposed between the fourth insulating layer and the third insulating layer;

10[c]: wherein the plurality of through holes comprise a plurality of first through holes and a plurality of second through holes, the plurality of first through holes penetrates through the first insulating layer, the second insulating layer, and the fourth insulating layer, and the plurality of second through holes penetrates through the third insulating layer; wherein the plurality of first through holes are communicated with the plurality of second through holes, and a diameter of each of the plurality of second through holes is greater than a diameter of each of the plurality of first through holes.
11: A display device comprising the display panel as claimed in claim 1, wherein the display panel is an organic light-emitting diode (OLED) panel.
12: The display device according to claim 11, wherein the converging wire between the two adjacent through holes is linear in arrangement.
13: The display device according to claim 12, wherein the converging wire is linear in arrangement and the plurality of through holes overlappingly disposed on the converging wire are linear in arrangement.
14: The display device according to claim 11, wherein the converging wire comprises a first converging wire, and the first converging wire comprises a plurality of first connection sections and a plurality of second connection sections; wherein each of the plurality of second connection sections is connected between a middle portion of two adjacent first plurality of connection sections, a width of each of the plurality of first connection sections is greater than a width of each of the plurality of second connection sections, and the plurality of power supply lines are electrically connected to the plurality of first connection sections through the plurality of through holes.
15: The display device according to claim 14, wherein the plurality of pixel driving circuits are arranged in an array in a first direction and a second direction, each of the plurality of first connection sections is electrically connected to the plurality of shielding blocks corresponding to a column of the plurality of pixel driving circuits arranged along a first direction.
16: The display device according to claim 15, wherein a periphery of each of the plurality of first sections is arc shaped, the plurality of second sections are linearly shaped, a maximum width of each of the plurality of first sections is greater than the width of each of the plurality of second sections.

17[a]: The display device according to claim 11, wherein the non-display region comprises: a first non-display region and a second non-display region disposed on two sides of the display region, wherein the first non-display region comprises a bending sub-region, and the display panel bends at the bending sub-region; and
17[b]: the converging wire comprises a first converging wire arranged in the first non-display region, and the plurality of power supply lines are electrically connected to the plurality of first connection sections at least through the plurality of through holes.
18: The display device according to claim 17, wherein the converging wire comprises a second converging wire arranged in the second non-display region, and the plurality of power supply lines are electrically connected to the plurality of second connection sections through the plurality of through holes.
19[pre]: The display device according to claim 11, wherein the pixel driving circuit layer comprises:
19[a]: a semiconductor layer disposed on a side of the shielding layer away from the substrate;
19[b]: a first insulating layer disposed on a side of the semiconductor layer away from the substrate;
19[c]: a first gate metal layer disposed on a side of the first insulating layer away from the substrate;
19[d]: a second insulating layer disposed on a side of the first gate metal layer away from the substrate;
19[e]: a second gate metal layer disposed on a side of the second insulating layer away from the substrate; and
19[f]: a third insulating layer disposed on a side of the second gate metal layer away from the substrate;
19[g]: wherein the first conductive layer is disposed on a side of the third insulating layer away from the substrate, the plurality of power supply lines of the first conductive layer are electrically connected to the converging wire through the plurality of through holes, and the plurality of through holes penetrate through the first insulating layer, the second insulating layer, and the third insulating layer.
20[pre]: The display device according to claim 19, wherein the pixel driving circuit layer further comprises:
20[a]: a fourth insulating layer disposed between the second gate metal layer and the third insulating layer; and
20[b]: a second conductive layer disposed between the fourth insulating layer and the third insulating layer;
20[c]: wherein the plurality of through holes comprise a plurality of first through holes and a plurality of second through holes, the plurality of first through holes penetrates through the first insulating layer, the second insulating layer, and the fourth insulating layer, and the plurality of second through holes penetrates through the third insulating layer; wherein the plurality of first through holes are communicated with the plurality of second

through holes, and a diameter of each of the plurality of second through holes is greater than a diameter of each of the plurality of first through holes.