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Filed on behalf of **Luxottica of America Inc.** and **Meta Platforms, Inc.**

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LUXOTTICA OF AMERICA INC. AND META PLATFORMS, INC.,
Petitioners,

v.

SOLOS TECHNOLOGY LIMITED,
Patent Owner.

Case IPR2026-00512
Patent 10,651,866

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,651,866**

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LIST OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 10,651,866 to Fan et al. (“’866 patent”)
1002	File History of U.S. Patent No. 10,651,866
1003	Declaration of Thomas W. Kenny, Ph.D.
1004	Curriculum Vitae of Thomas W. Kenny, Ph.D.
1005	RESERVED
1006	European Patent App. Pub. No. 1,744,174 (“Moquin”)
1007	U.S. Patent App. Pub. No. 2007/0229336 (“Liu”)
1008	U.S. Patent No. 6,339,647 (“Andersen”)
1009	U.S. Patent No. 5,461,389 (“Dean”)
1010	U.S. Patent No. 5,203,335 (“Noujaim”)
1011	U.S. Patent No. 6,539,096 (“Sigwanz”)
1012	Tiete et al., <i>SoundCompass: A Distributed MEMS Microphone Array-Based Sensor for Sound Source Localization</i> , 14 Sensors 1918 (2014), available at https://www.mdpi.com/1424-8220/14/2/1918 .
1013	Excerpts from Microsoft Computer Dictionary, Fifth Edition, 2002
1014	Rudolf F. Graf, Excerpts from Modern Dictionary of Electronics Seventh Edition, 1999
1015	M. Brandstein and D. Ward, Eds., <i>Microphone Arrays: Signal Processing Techniques and Applications</i> . Berlin, Germany: Springer-Verlag, 2001 (“Brandstein-Ward”)
1016	R. Kneipfer, Sonar Beamforming – An Overview of Its History and Status, NUWC-NL Technical Report, 10,003, 7 April 1992 (“Kneipfer”)

Exhibit No.	Description
1017	Gannot, Sharon, and Israel Cohen. “Adaptive Beamforming and Postfiltering.” <i>Springer Handbook of Speech Processing</i> , edited by Jacob Benesty, M. Mohan Sondhi, and Yiteng Huang, Springer Berlin Heidelberg, 2008, pp. 945–978 (“Gannot-Cohen”)
1018	B. Van Veen, “Beamforming: A Versatile Approach to Spatial Filtering,” in <i>IEEE ASSP Magazine</i> , vol. 5, no. 2, pp. 4-24, April 1988 (“Van Veen”)
1019	S. R. Freeman <i>et al.</i> , “Delta-sigma oversampled ultrasound beamformer with dynamic delays,” in <i>IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control</i> , vol. 46, no. 2, pp. 320-332, March 1999
1020	C.I.C. Nilsen <i>et al.</i> , “Distortion-Free Delta-Sigma Beamforming,” in <i>IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control</i> , vol. 55, no. 8, pp. 1719-1728, 2008
1021	L. Milic <i>et al.</i> , Multirate Filters: An Overview, <i>APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems</i> , Singapore, 2006, pp. 912-915
1022	G. Moon <i>et al.</i> , Design Approach for Decimation Filter for ADC Application, <i>Int’l J. of Eng. Trends and Techn. (IJETT)</i> , vol. 10 no. 12 (2014)
1023	J. Yu <i>et al.</i> , A low-power multi-bit $\Sigma\Delta$ modulator in 90-nm digital CMOS without DEM, in <i>IEEE Journal of Solid-State Circuits</i> , vol. 40, no. 12, pp. 2428-2436, Dec. 2005
1024	RESERVED
1025	RESERVED
1026	U.S. Patent App. Pub. No. 2001/0028720 (“Hou”)
1027	U.S. Patent No. 7,936,293 (“Hamashita”)

Petitioners Luxottica of America Inc. and Meta Platforms, Inc. (“Petitioners”) request *inter partes* review (“IPR”) of claims 1-20 of U.S. Patent No. 10,651,866 (“’866 patent,” Ex.1001), which is assigned to Solos Technology Limited (“PO”).

I. INTRODUCTION

The challenged claims recite delaying and combining oversampled signals as part of beamforming, a decades-old technique that aligns and reinforces sensor signals from a desired direction while reducing noise or interference (*see* Ex.1003, ¶¶45-47 (discussing Exs.1015-1020)).

Independent claim 1 recites outputting a first oversampled digital signal from an analog-to-digital converter (ADC), delaying it, and combining it with a second oversampled digital signal to obtain a beamformed signal. Independent claims 11 and 16 recite corresponding systems. The dependent claims add known implementation details for signal capture and processing.

The prior art repeatedly disclosed the independent claims’ output-delay-combine approach. Moquin, Liu, and Andersen are representative: each discloses oversampled digital sensor signals that are delayed and combined into a beamformed output. Yet the Examiner allowed the challenged claims without any prior-art rejection.

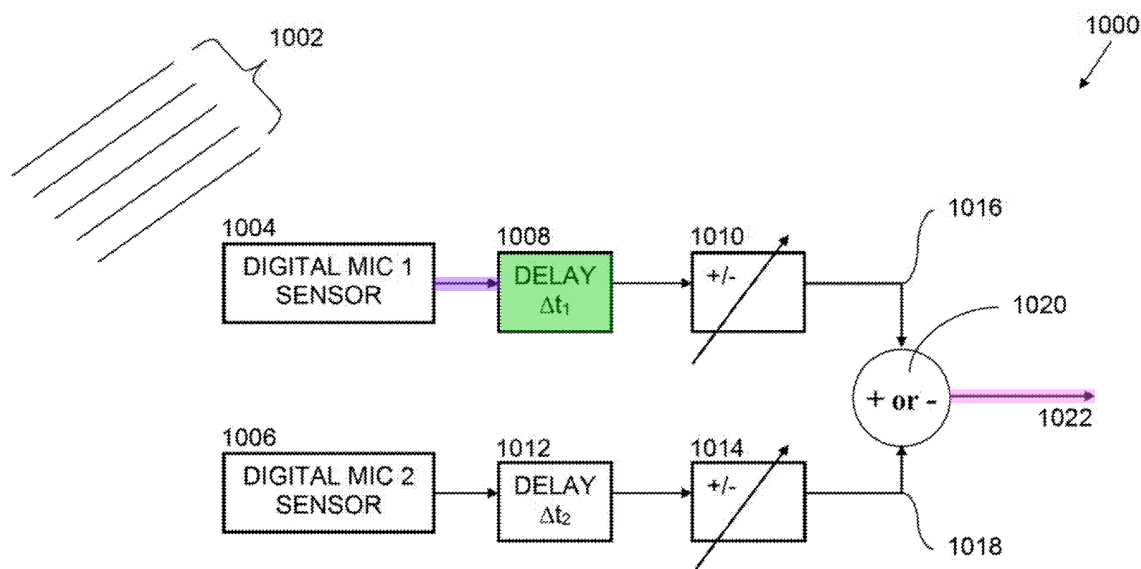
The Board should institute *inter partes* review and cancel claims 1-20.

II. THE '866 PATENT

A. Overview

The '866 patent describes a digital sensor/ADC, such as a digital microphone, that outputs an oversampled digital signal responsive to an analog field. Ex.1001, Abstract, 2:49-58; *see also* Ex.1003, ¶¶58-62. It further discloses delaying that oversampled signal by an integer number of sampling-clock cycles. Ex.1001, 3:3-67, 3:27-32.

Figure 10 illustrates that output-delay-combine architecture for beamforming. Two digital microphone sensors output oversampled digital signals (purple), delay elements (green) delay them, and arithmetic block 1020 combines them into a beamformed output (pink). *Id.*, 13:16-41.



Id., Fig.10(annotated).

Independent claim 1 recites the same basic process: outputting a first oversampled digital signal from an ADC, delaying that signal by an integer number of sampling-clock cycles, and combining the delayed signal with a second oversampled digital signal to obtain a beamformed digital signal. *Id.*, cl.1. Independent claims 11 and 16 recite system counterparts to claim 1's output-delay-combine process. Claim 11 recites first and second digital sensors, while claim 16 recites one digital sensor and a second oversampled digital output signal; both require a time-delay element and an arithmetic unit that uses the delayed signal with the second signal to produce the beamformed digital signal. *Id.*, cls.11, 16.

B. Prosecution History

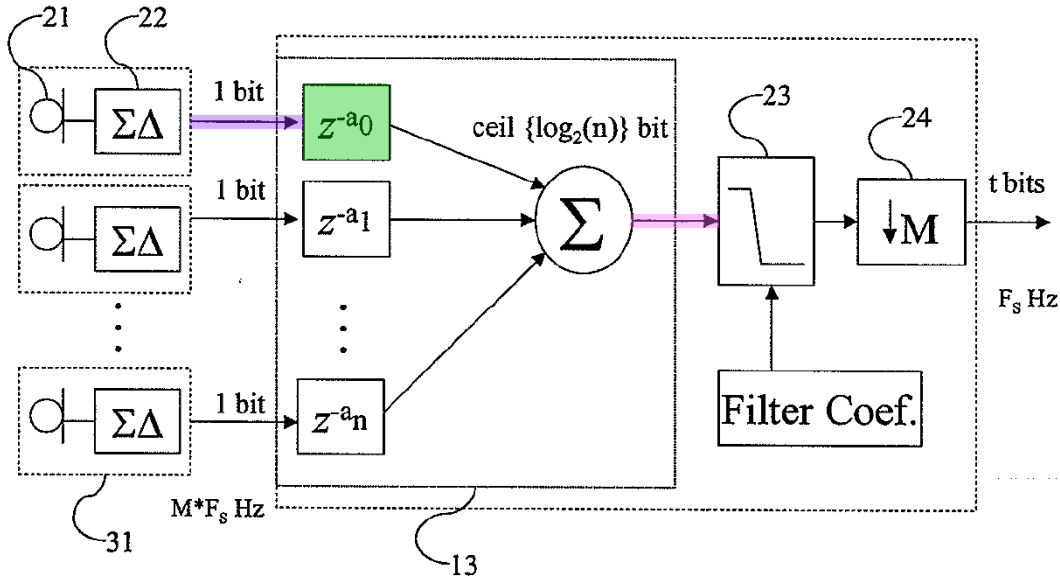
The Examiner allowed the challenged claims without rejection. Ex.1002, 124-133, 251-253, 263; *see also* Ex.1003, ¶63. No ground below relies on a reference that was before the Examiner. Ex.1001, References Cited.

III. OVERVIEW OF PRIOR ART

A. Moquin

Moquin discloses the output-delay-combine architecture recited in the independent claims. Ex.1003, ¶¶64-65. Figure 4's digital microphones use microphone elements and delta-sigma modulators/ADCs to output one-bit oversampled signals (purple) at 2,048 kHz. Ex.1006, [0005], [0014]. Shift-register taps (green) delay those signals by selected sampling-clock cycles, and the delayed

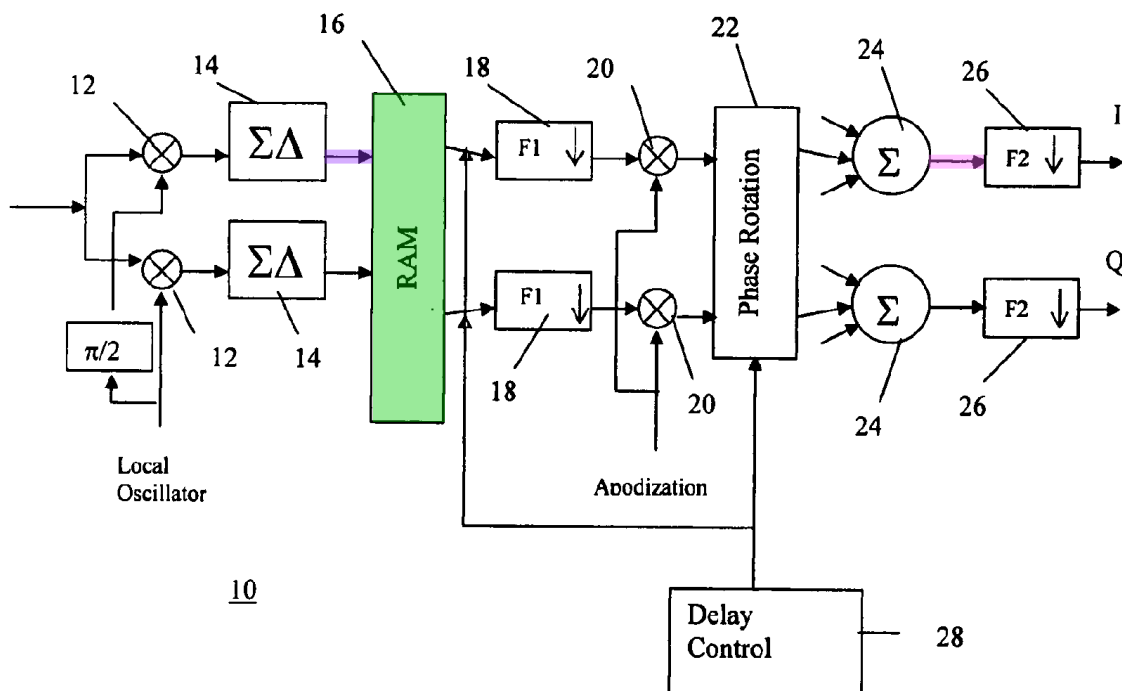
signals are summed to form a beamformed signal (pink), which filter 23 and decimator 24 then convert to lower-rate signals. *Id.*, [0012], [0014]-[0016].



Id., Fig.4(annotated).

B. Liu

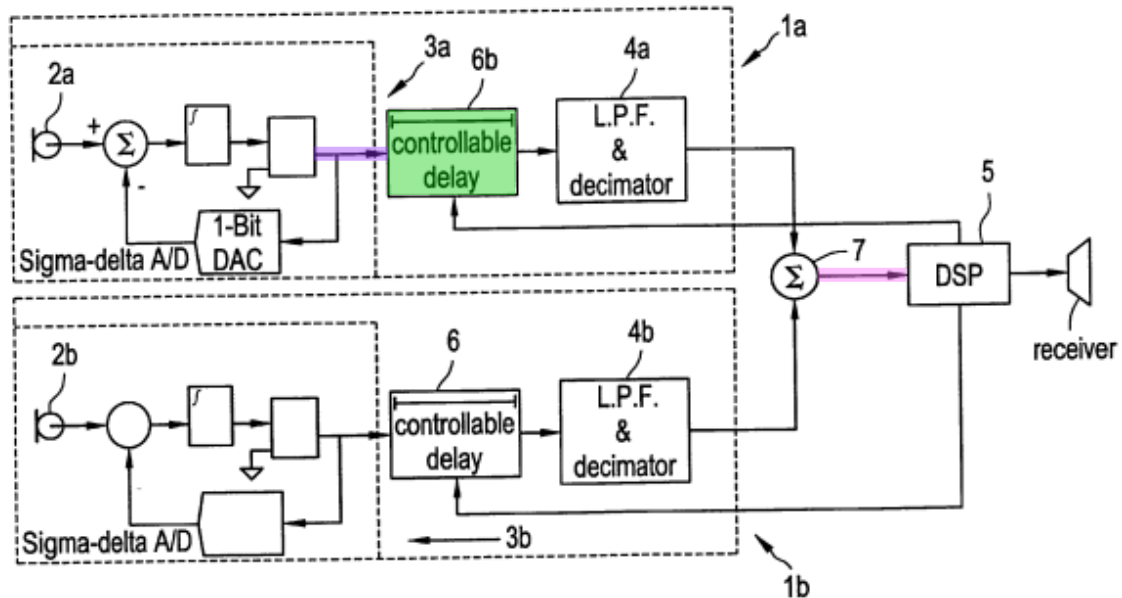
Liu likewise discloses an output-delay-combine beamforming architecture corresponding to independent claim 1. Ex.1003, ¶66. Figure 2's oversampling ADCs 14 digitize each receive channel into oversampled signals (purple), memory 16 (green) receives and stores those signals at the oversampling rate, and delay controller 28 selects stored data according to beam delay. Ex.1007, [0006]-[0007], [0024]-[0035]. Filter 18 partially reconstructs/decimates the selected samples, summer 24 sums the resulting channel signals to form the beamformed signal (pink), and filter 26 further reconstructs the beam sum. *Id.*, Abstract, [0038]-[0040], [0052], [0055]-[0057].



Id., Fig.2(annotated).

C. Andersen

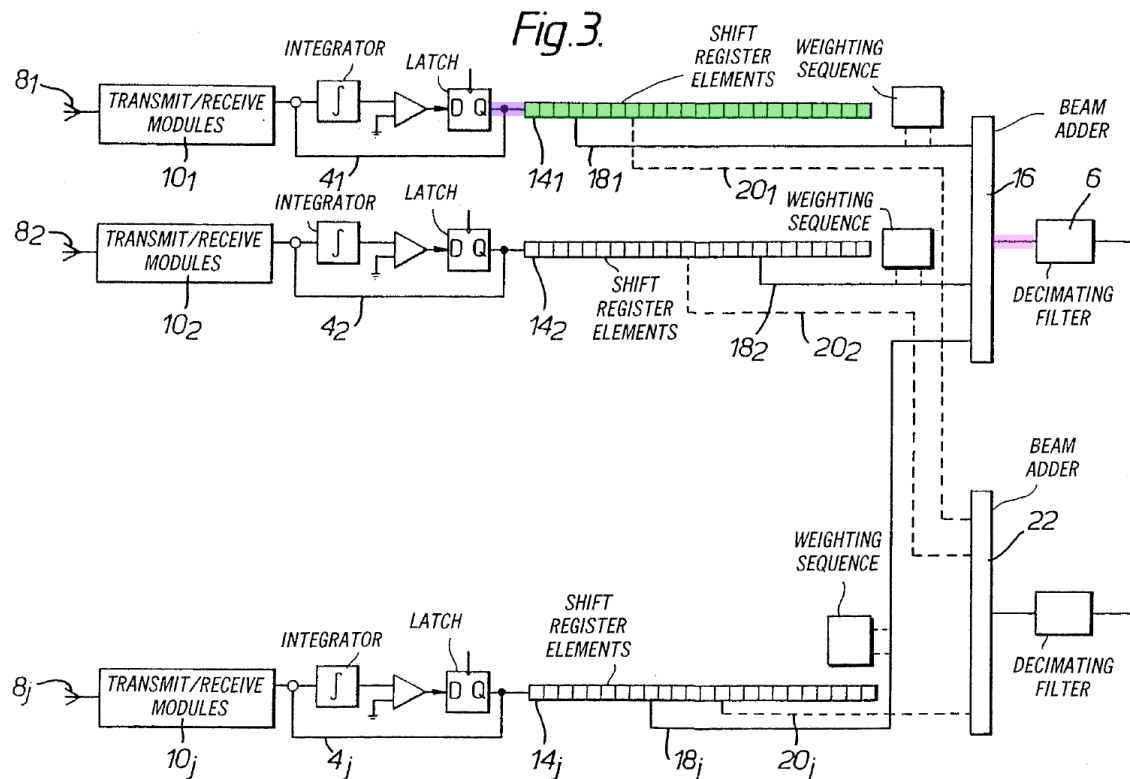
Andersen likewise discloses oversampled microphone-channel delay and beamforming combination corresponding to the independent claims. Ex.1003, ¶¶67-68. In Figure 4, each sigma-delta ADC outputs a high-clock-frequency one-bit signal (purple) that an LPF/decimator converts to lower-rate digital words, with a controllable delay (green) placed at the LPF/decimator input to delay at least one high-rate signal before lower-rate processing. Ex.1008, Abstract, 1:40-57, 2:5-25, 3:4-22. A summing circuit 7 combines the filtered/decimated channel outputs to form the beamformed output (pink) before DSP 5. *Id.*, 3:23-59.



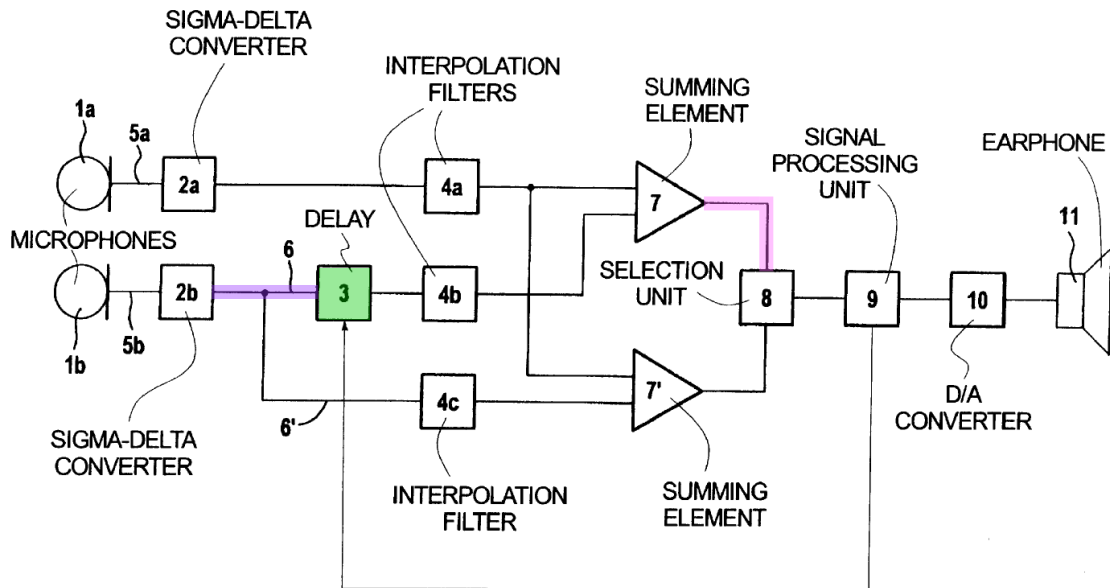
Id., Fig.4(annotated).

D. Dean, Sigwanz, and SoundCompass

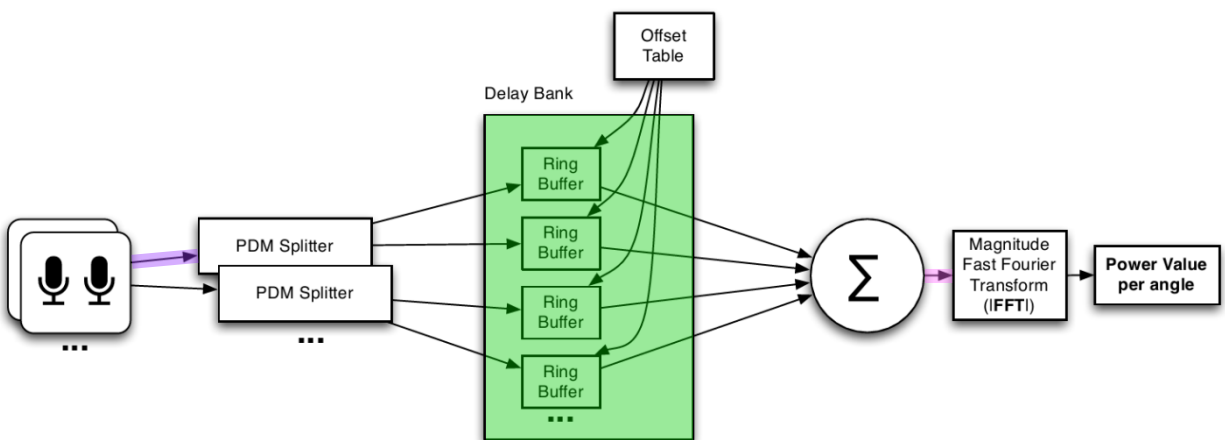
Dean discloses a digital beamforming array that converts sensor-module signals into oversampled n-bit signals, delays them with shift registers, combines them with beam adders, and filters/decimates the result. Ex.1009, Abstract, 1:45-2:67, 5:26-55; *see also* Ex.1003, ¶69.



Ex.1009, Fig.3(annotated). Sigwanz discloses microphone channels in which sigma-delta converters produce one-bit signals, and delayed and undelayed signals are filtered and combined in summing elements. Ex.1011, Abstract, 1:66-2:39, 2:65-3:29; *see also* Ex.1003, ¶70.



Ex.1011, Fig.(annotated). SoundCompass discloses a 52-microphone array whose one-bit streams pass through a ring-buffer delay bank and are summed for beamforming. Ex.1012, 6-8; *see also* Ex.1003, ¶71.



Ex.1012, Fig.4(annotated).

E. Noujaim

Noujaim discloses beamforming in which sigma-delta modulators digitize transducer-element signals into oversampled one-bit streams for delay, summation, and filtering/decimation. Ex.1010, 8:65-10:3, Fig.5; *see also* Ex.1003, ¶72.

F. Hou

Hou discloses a two-microphone directional processing system that delays one microphone signal before subtracting it from another to produce an output that suppresses unwanted interference. Ex.1026, [0039], Fig.3; *see also* Ex.1003, ¶73.

IV. LEVEL OF ORDINARY SKILL

A hypothetical person of ordinary skill in the art (“POSA”) would have had at least a bachelor’s degree in physics, electrical engineering, computer engineering, or a similar technical field, and at least two years of experience designing or implementing digital signal-processing systems for sensors or sensor arrays. Ex.1003, ¶37. Work experience could substitute for formal education, and additional formal education could substitute for work experience. *Id.*

The claims would have been obvious to a POSA under any reasonable definition. *Id.*, ¶40; *see also id.*, ¶¶36-44, 48, 57.

V. CLAIM CONSTRUCTION

PO sued Petitioners for infringement of the ’866 patent in *Solos Technology Limited v. Meta Platforms, Inc. et al.*, No. 1:26-cv-10304 (D. Mass.) (“the

Litigation”). The parties have not yet identified proposed constructions in that case and, to the best of Petitioners’ current knowledge, no claim terms require express construction to resolve the challenges here.

Claim terms receive their ordinary and customary meaning in light of the intrinsic record. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc); *see* Ex.1003, ¶¶76-79.

VI. STATEMENT OF RELIEF REQUESTED**A. Grounds**

Petitioners request IPR for the following grounds:

Ground	Reference(s)	Basis	Challenged Claims
1A	Moquin	§102	1-2, 5, 11-13, 15-18, 20
1B	Moquin	§103	4, 7-9
2	Moquin and Liu	§103	3
3	Moquin and Dean	§103	10
4	Moquin and Hou	§103	14, 19
5A	Liu	§102	1-5, 7, 10
5B	Liu	§103	4, 7-10
6	Liu and Andersen	§103	6-10
7A	Andersen	§102	1, 4-8, 11-20
7B	Andersen	§103	1-2, 5-6, 9, 11-20
8	Andersen and Liu	§103	3
9	Andersen and Noujaim	§103	9
10	Andersen and Dean	§103	10
11	Andersen and Moquin	§103	11-20

Petitioners submit the expert declaration of Dr. Thomas W. Kenny (Ex.1003).

See Ex.1003, ¶¶1-35, 520; see also Ex.1004.

B. Asserted References

The '866 patent's earliest claimed priority date is August 1, 2016. Ex.1001.

The references are prior art for the following reasons:

Ex.	Reference	Date	Art Type
1006	Moquin	Filed: Jul. 12, 2005 Published: Jan. 17, 2007	§§102(a)(1)-(2)
1007	Liu	Filed: Mar. 30, 2007 Published: Oct. 4, 2007	§§102(a)(1)-(2)
1008	Andersen	Filed: Feb. 5, 1999 Published: Jan. 15, 2002	§§102(a)(1)-(2)
1009	Dean	Filed: Jun. 30, 1994 Published: Oct. 24, 1995	§§102(a)(1)-(2)
1010	Noujaim	Filed: Mar. 2, 1992 Published: Apr. 20, 1993	§§102(a)(1)-(2)
1026	Hou	Filed: May 15, 2001 Published: October 11, 2001	§§102(a)(1)-(2)

The references are analogous art at least because they are from the same field as the '866 patent, e.g., digital signal processing for sampled sensor systems or multi-sensor directional processing. Ex.1003, ¶¶74-75; Ex.1001, 1:24-26, 2:44-48; *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1000 (Fed. Cir. 2016). They are also pertinent to a problem the inventors were focused on, e.g., implementing delay-

based beamforming or directional processing in digital sensor systems. Ex.1003, ¶74.

VII. GROUND 1A: CLAIMS 1-2, 5, 11-13, 15-18, AND 20 ARE ANTICIPATED BY MOQUIN

Moquin discloses the output-delay-combine architecture recited in claim 1 and the corresponding sensor, delay-element, and arithmetic-unit functionality recited in claims 11 and 16. Specifically, Moquin discloses a phased-array beamformer with sensors arranged in an array, ADCs generating oversampled signals, and delay-and-sum processing at the oversampling frequency to generate a beamformed output. *See* Ex.1006, Title, Abstract, [0014]-[0016], Fig.4, cls.1-2; *see also* Ex.1003, ¶¶49-56. In Figure 4, the one-bit oversampled signals are fed to delay elements, delayed by selected taps, and summed before filtering and decimation. Ex1006, [0014].

A. Claim 1

1. 1[pre]

To the extent limiting, Moquin discloses “[a] method to create a beamformed digital signal.” Ex.1003, ¶83. Moquin discloses a “phased array beamformer” that performs delay-and-sum beamforming on oversampled signals to “generate a beamformed output signal.” Ex.1006, Abstract; *see also id.*, [0006], [0013]-[0014], Fig.4, cls.1-6.

2. 1[a]

This limitation recites “outputting a first oversampled digital signal output from an analog-to-digital converter (ADC), wherein the first oversampled digital signal is responsive to an analog field and the first oversampled digital signal is created at a sampling clock frequency.” Moquin discloses this limitation. Ex.1003, ¶¶84-88.

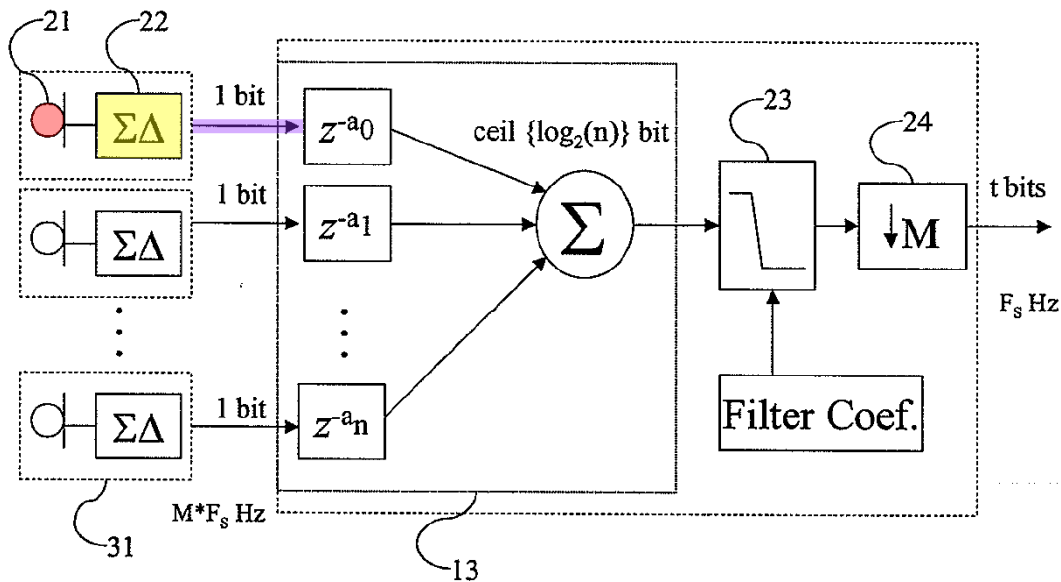
For example, in Figure 4, Moquin discloses that each sensor 31 is a “digital microphone” and includes a microphone element 11/21 and delta-sigma modulator 22. Ex.1006, [0014].¹ Moquin identifies delta-sigma modulators as oversampling ADCs and states that its Figure 4 sensors “receive and digitise input signals to the array.” *Id.*; *see also id.*, [0002], [0005], [0014]. In one embodiment, the microphone signal is sampled “at a clock rate of 2,048 kHz (M=256 times 8 kHz),” and the output is a single-bit digital stream. *Id.*, [0014]; *see also id.*, [0001], [0005].

That one-bit, high-rate stream is the claimed first oversampled digital signal. It is responsive to an analog field because it is generated from the acoustic input received by the microphone element, and it is created at a sampling clock frequency

¹ Moquin inconsistently labels the Figure 4 microphone element as 11 in paragraph [0014] and 21 in the figure; either way, it is paired with delta-sigma modulator 22. Ex.1006, [0014], Fig.4; Ex.1003, ¶86 n.3.

because Moquin samples it at the 2,048 kHz clock rate, which Moquin identifies as oversampling at 256 times the 8 kHz telephony sampling rate. *See id.*, [0005], [0009] (“[P]lane waves...impinge on the array.”), [0014]; Ex.1003, ¶88.

This is illustrated in Figure 4, which shows a microphone element (red), delta-sigma modulator (yellow), and single-bit delta modulator output (purple):



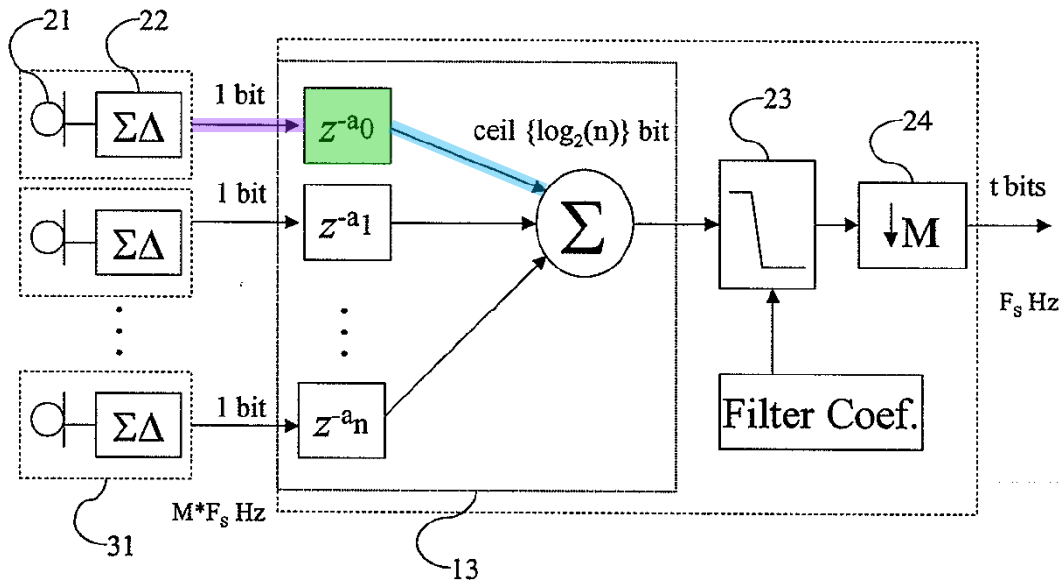
Ex.1006, Fig.4(annotated); Ex.1003, ¶¶87-88.

3. 1[b]

This limitation recites “delaying the first oversampled digital signal by a time delay wherein the time delay is equal to an integer number of sampling clock cycles to produce a time delayed first oversampled digital signal.” Moquin discloses this limitation. Ex.1003, ¶¶89-93.

Moquin delays the first oversampled digital signal (high-rate stream identified for 1[a]). In Figure 4, the “single-bit delta modulator outputs are fed to the

aforementioned delay elements (preferably a shift register with taps at the appropriate length (a_x)) to obtain a desired delay.” Ex.1006, [0014]. The delayed tap outputs are then provided to the summing node. *Id.*, Fig.4. Specifically, Figure 4 depicts a one-bit oversampled output (purple) from a delta-sigma modulator being input to a corresponding delay element (green), with the delayed output (blue) then provided to the summing node:



Id., Fig.4(annotated); Ex.1003, ¶91.

Moquin discloses that the delay is an integer number of sampling-clock cycles and explains that, in digital systems, the delay τ “can only take on values that are integer multiples of the sample time ($1/F_s$).” Ex.1006, [0012]. In Figure 4, Moquin feeds the one-bit delta-modulator outputs to these “aforementioned delay elements,” and the signal being delayed is the one-bit oversampled stream sampled at the oversampling clock rate (e.g., 2,048 kHz or $M \cdot F_s$), with Moquin’s “sample time”

being $1/(M \cdot F_s)$. *Id.*, [0014], Fig.4. Moquin’s tapped shift register provides integer-cycle delay because Moquin explains that in its digital system, delay “ τ can only take on values that are integer multiples of the sample time,” and each clock pulse advances the oversampled sample stream by one register stage, so selecting the Nth tap delays the stream by N oversampling-clock cycles—an integer multiple of the oversampled sampling period. *See* Ex.1003, ¶93(citing Ex.1013 and Ex.1014).

4. 1[c]

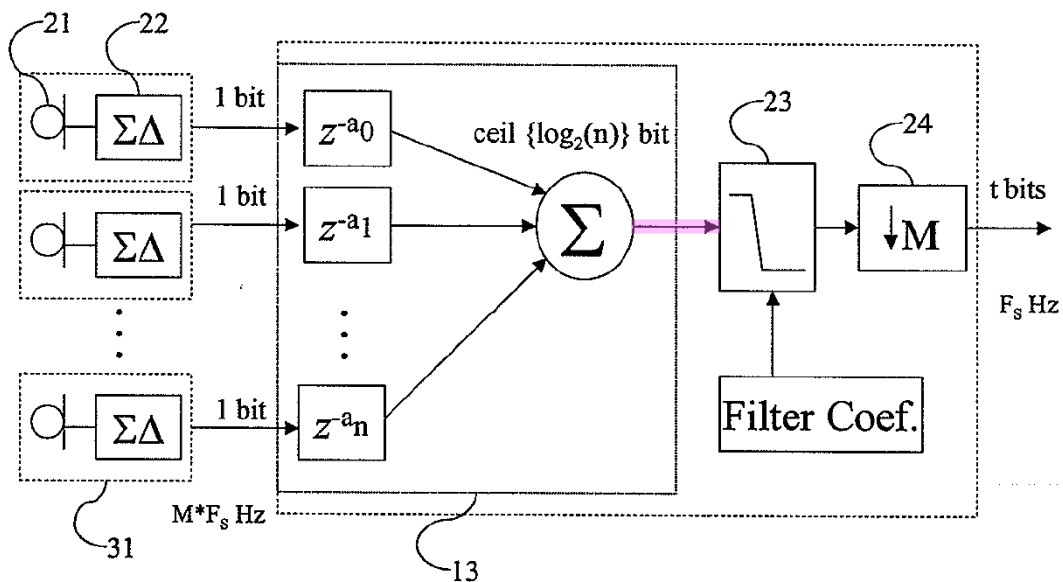
This limitation recites “combining the time delayed first oversampled digital signal with a second oversampled digital signal to obtain the beamformed digital signal, wherein the second oversampled digital signal is responsive to the analog field.” Moquin discloses this limitation. Ex.1003, ¶¶94-100.

Moquin discloses multiple digital microphones in the array. Each sensor “receive[s] and digitise[s] input signals to the array.” Ex.1006, [0014]. In one embodiment, each such sensor outputs a signal sampled “at a clock rate of 2,048 kHz ($M=256$ times 8kHz) and the output is a single bit.” *Id.* Thus, another digital microphone provides the claimed second oversampled digital signal. Ex.1003, ¶96. Like the first signal, the second signal is responsive to the analog field because it is generated from acoustic input received by a microphone element. *Id.*

Moquin combines the delayed first oversampled signal with a second oversampled channel signal. *Id.*, ¶99. Specifically, Moquin discloses that the

“single-bit delta modulator outputs are fed to the aforementioned delay elements...to obtain a desired delay,” and that “[t]he outputs are then summed together and presented to the filter 23 and decimator 24.” Ex.1006, [0014]; *see also id.*, Fig.4.

The resulting sum is the claimed beamformed digital signal. Moquin’s Abstract states that the beamformer performs delay-and-sum filtering of oversampled signals “to generate a beamformed output signal,” and claim 6 similarly recites an adder “for summing delayed signals output from said taps to generate said beamformed output signal.” Ex.1006, Abstract, cl.6; *see also id.*, cl.1. Filter 23 and decimator 24 process that already-formed beam signal (pink). *Id.*, [0014].



Id., Fig.4(annotated); Ex.1003, ¶¶99.

Accordingly, Moquin anticipates claim 1. *Id.*, ¶¶80-100.

B. Claim 2

Moquin anticipates claim 2. Ex.1003, ¶¶101-105.

Moquin explains that its combining operation is performed in an oversampled signal domain. In Moquin's Figure 4 embodiment, "the delay and sum beamformer 13 is placed before the filter 23 and decimator 24," and accordingly, the one-bit oversampled delta-sigma outputs are fed to delay elements, whose "outputs are then summed together" before being "presented to the filter 23 and decimator 24." Ex.1006, [0014], Fig.4; *see also id.*, Abstract, cl.1. Moquin confirms that "the summer and the delay lines" operate "at the higher sample rate ($M \cdot F_s$)," and that "[t]he delay and sum beamforming operation is performed at the oversampling frequency." *Id.*, [0015], Abstract.

Thus, Moquin's combining/summing is performed on oversampled signals before filtering and decimation, and therefore is performed in an oversampled signal domain. Ex.1003, ¶105.

C. Claim 5

Moquin anticipates claim 5. Ex.1003, ¶¶106-109.

With respect to Figure 4, Moquin discloses a plurality of sensors/digital microphones, each including a microphone element and a delta-sigma modulator, and each outputting a respective one-bit oversampled digital signal to beamformer 13. Ex.1006, [0014], Fig.4.

Thus, Moquin discloses first and second oversampled digital signals that correspond to signals output from two different sensors, e.g., different digital microphones 31. Ex.1003, ¶109.

D. Claim 11

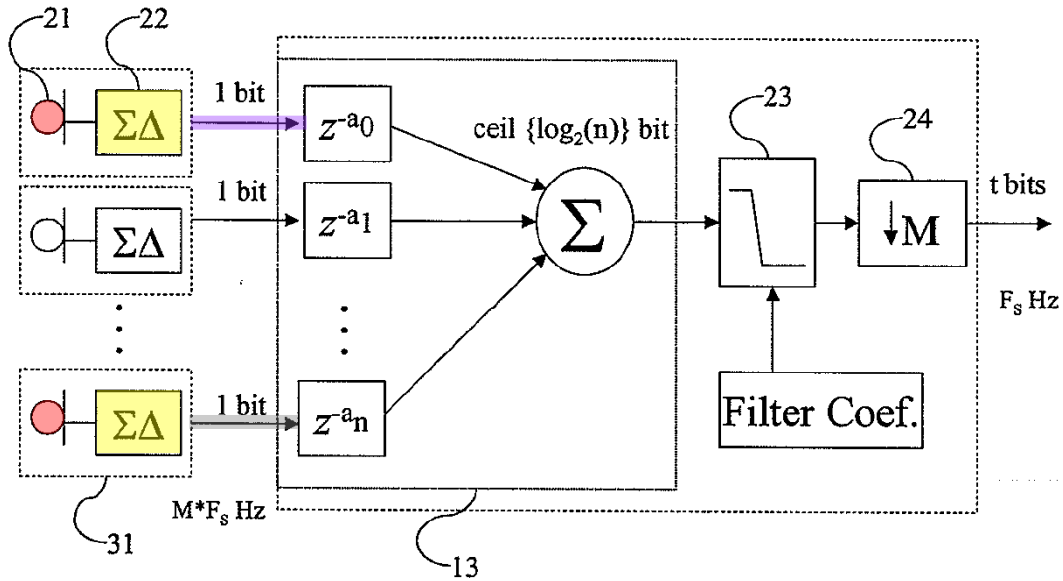
1. 11[pre]

To the extent limiting, Moquin discloses 11[pre]. Ex.1003, ¶110. Moquin’s “phased array beamformer” is a system that performs delay-and-sum filtering of oversampled sensor signals to generate a “beamformed output signal.” Ex.1006, Abstract; *see also id.*, [0014], Fig.4; *supra* §VII.A.1.

2. 11[a]-11[b]

Moquin discloses 11[a]-11[b]. Ex.1003, ¶¶111-113.

Moquin’s Figure 4 uses multiple sensors 31, each a “digital microphone” including a microphone element (red) and delta-sigma modulator (yellow), to “receive and digitise input signals to the array.” Ex.1006, [0014]. In Moquin’s microphone array, plane waves impinge on the array, and each sensor’s signal is sampled (e.g., at 2,048 kHz) and output as a single-bit oversampled stream (purple/gray). *Id.*, [0009], [0014].



Ex.1006, Fig.4(annotated). Thus, first and second sensors 31 disclose first and second digital sensors responsive to an analog field and configured to output first and second oversampled digital output signals at the same sampling clock frequency.

Ex.1003, ¶113; *see also supra* §§VII.A.2, VII.A.4.

3. 11[c]

Moquin discloses 11[c]. Ex.1003, ¶114.

As explained for 1[b], Moquin feeds each sensor's single-bit delta-modulator output to a corresponding delay element (e.g., tapped shift register) to obtain a desired delay, before summing and before filter 23/decimator 24. *Supra* §VII.A.3; *see* Ex.1006, [0014], Fig.4. The delay element for the claimed first sensor receives the first oversampled digital output signal and outputs a time-delayed oversampled digital output signal. Ex.1003, ¶114.

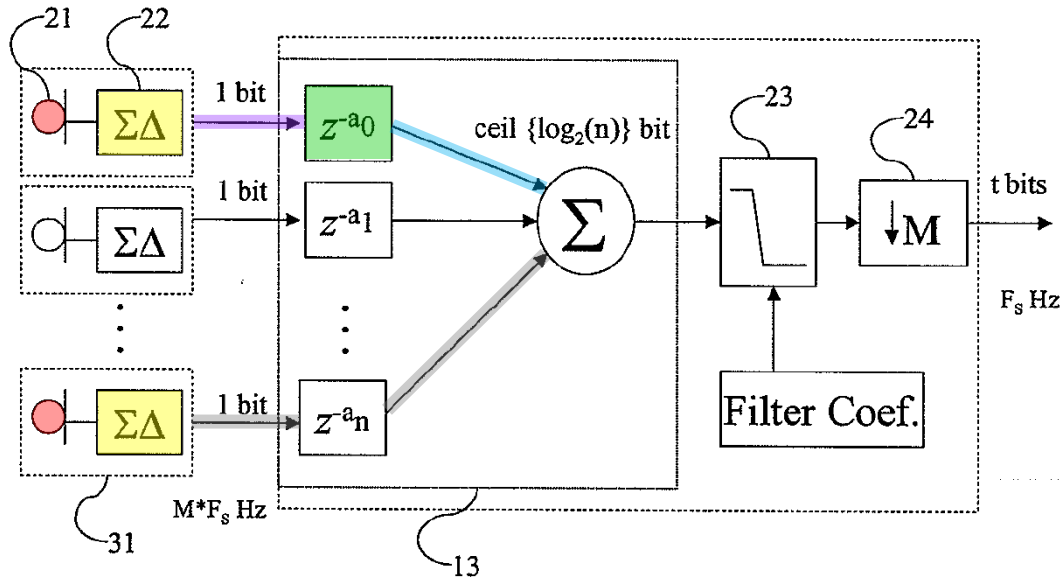
4. 11[d]

Moquin discloses 11[d]. Ex.1003, ¶¶115-120.

Moquin explains that, for a conventional array, a broadside beam is obtained by summing digitized sensor inputs with “no or equal delay,” while a steered beam is obtained by “phasing” the array elements and then summing them in delay-and-sum beamformer 13. Ex.1006, [0009]. Moquin also states that “[t]he steering angle is determined by the inter-element delay (τ),” and that, in a digital system, τ takes values that are integer multiples of the sample time. *Id.*, [0011]-[0012]. Thus, in Moquin, steering is produced by applying relative time delays between the sensor-channel signals before they are summed. Ex.1003, ¶116.

Moquin’s Figure 4 includes multiple digital microphones 31, each including a microphone element and delta-sigma modulator, that output respective one-bit oversampled streams at the oversampling clock rate. Ex.1006, [0014]. Those single-bit delta-modulator outputs are fed to delay elements (e.g., tapped shift registers “at the appropriate length (a_x)”) “to obtain a desired delay,” and “[t]he outputs are then summed together.” *Id.* Because Moquin’s steering angle is determined by the inter-element delay τ , the selected tap lengths in Figure 4 cause the delayed first-channel stream and the second-channel stream to arrive at the summing node separated by the selected steering delay. Ex.1003, ¶¶117-120. That separation is the time delay imparted by the first-channel delay element. *Id.*

In the annotated Figure 4 below, purple identifies the first sensor stream input to the first-channel delay element (green, the claimed time delay element), blue identifies the resulting time-delayed first-channel stream, and gray identifies the second sensor stream used as the reference/no-delay signal:



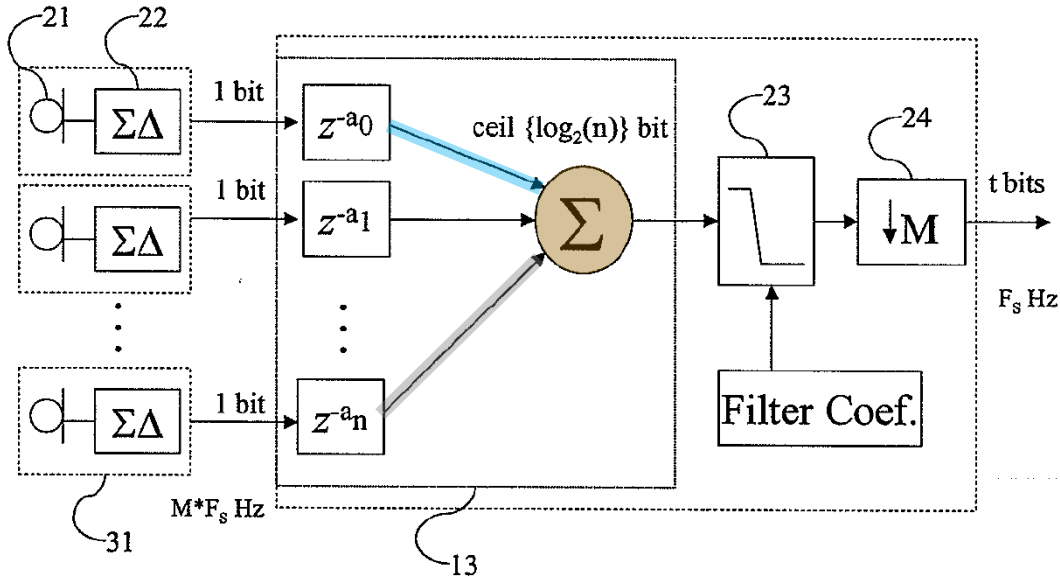
Ex.1006, Fig.4(annotated); Ex.1003, ¶120. For a steered look direction, the blue time-delayed first-channel stream and the gray second-channel stream are separated by the inter-element delay selected for steering, and Moquin discloses that this delay is obtained by the tapped delay element before the streams are summed. Ex.1003, ¶120.

5. 11[e]

Moquin discloses 11[e]. Ex.1003, ¶¶121-122.

Moquin's beamformer 13 includes a summing node/adder (Σ , tan), which is an arithmetic unit. Ex.1006, Fig.4, [0014], cl.6. As explained for 11[d], in the

reference/no-delay implementation, that arithmetic unit receives the time-delayed first-channel bit stream (blue) and the second sensor stream used as the reference/no-delay signal (gray). *Supra* §VII.D.4.



Ex.1006, Fig.4(annotated). Moquin teaches that “[t]he outputs are then summed together” before filter 23/decimator 24. *Id.*, [0014]. Moquin likewise describes delay-and-sum filtering of oversampled signals to “generate a beamformed output signal,” and recites an “adder” for summing tap outputs to generate that beamformed output. *Id.*, Abstract, cl.6.

Accordingly, Moquin anticipates claim 11. Ex.1003, ¶¶110-122.

E. Claim 12

Moquin anticipates claim 12 for the reasons explained for 11[e]. *Supra* §VII.D.5; Ex.1003, ¶123.

F. Claim 13

Moquin anticipates claim 13 for the reasons explained for claim 12. *Supra* §VII.E; Ex.1003, ¶124.

G. Claim 15

Moquin anticipates claim 15. Ex.1003, ¶¶125-129.

Delta-sigma and sigma-delta refer to the same modulator type, and a one-bit output from such a modulator is pulse density modulated (PDM). *Id.*, ¶128; *see also* Ex.1027, Abstract, 1:6-23. Thus, Moquin’s first digital sensor uses the claimed sigma-delta modulator and produces a PDM output signal at the sampling clock frequency responsive to the analog field. Ex.1003, ¶129.

H. Claim 16

1. 16[pre]

Moquin discloses 16[pre] for the reasons explained for 11[pre]. *Supra* §VII.D.1; Ex.1003, ¶130.

2. 16[a]

Moquin discloses 16[a] for the reasons explained for 11[a]. *Supra* §VII.D.2; Ex.1003, ¶131.

3. 16[b]

Moquin discloses 16[b] for the reasons explained for 11[c]. *Supra* §VII.D.3; Ex.1003, ¶132.

4. 16[c]

Moquin discloses 16[c] for the reasons explained for 11[d]. *Supra* §VII.D.4; Ex.1003, ¶133.

5. 16[d]

Moquin discloses 16[d] for the reasons explained for 11[e], 1[c], and 11[a]-11[b]. *Supra* §§VII.D.5, VII.A.4, VII.D.2; Ex.1003, ¶134. As explained for 1[c] and 11[a]-11[b], the second sensor stream—the claimed second oversampled digital output signal—is responsive to the analog field because it is generated from acoustic input received by Moquin’s second digital microphone. Ex.1003, ¶134.

Accordingly, Moquin anticipates claim 16. *Id.*, ¶¶130-135.

I. Claim 17

Moquin anticipates claim 17 for the reasons discussed for claims 12 and 16. *Supra* §§VII.E, VII.H; Ex.1003, ¶136.

J. Claim 18

Moquin anticipates claim 18 for the reasons discussed for claims 13 and 16. *Supra* §§VII.F, VII.H; Ex.1003, ¶137.

K. Claim 20

Moquin anticipates claim 20 for the reasons discussed for claims 15-16. *Supra* §§VII.G-H; Ex.1003, ¶138.

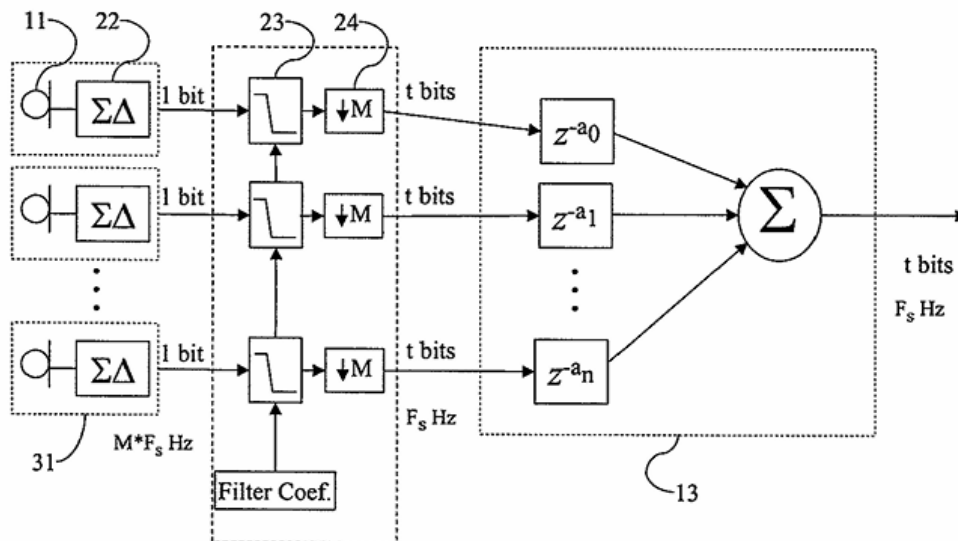
VIII. GROUND 1B: CLAIMS 4 AND 7-9 ARE OBVIOUS BASED ON MOQUIN

A. Claim 4

As explained in Ground 1A, Moquin discloses every limitation of claim 1.

Supra §VII.A. Moquin further renders claim 4 obvious. Ex.1003, ¶¶139-157.

A POSA would have found it obvious to use Moquin’s Figure 3 filter/decimator-before-beamformer ordering after Figure 4’s oversampled-domain delays. *Id.*, ¶148. In Figure 3, “[e]ach input is filtered at 23 and then decimated at 24” to produce t-bit samples at sampling frequency F_s , which are supplied to beamformer 13:



Ex.1006, [0013], Fig.3. Because each Figure 4 delay-element output remains a one-bit oversampled delta-modulator stream—the type of signal processed by Figure 3’s per-channel filter 23 and decimator 24—a POSA would have predictably placed

filter 23 and decimator 24 after each delay element and before the summer. Ex.1003, ¶¶144-148; Ex.1006, [0013]-[0015], Figs.3-4.

The resulting post-filter/decimator channel signals are baseband digital signals in Moquin’s telephony embodiment. Moquin discloses oversampling at 2,048 kHz, i.e., $M=256$ times $F_s=8$ kHz, for telephony audio whose maximum frequency of interest is about 3.5 kHz, and filter 23/decimator 24 then output t -bit samples at F_s , e.g., 16-bit samples at 8 kHz. Ex.1006, [0003], [0005], [0013]-[0014]; *see also* Ex.1001, 6:22-39 (disclosing 8 kHz as baseband audio format for telephony). The filter/decimator output is the lower-rate telephony/baseband representation of the microphone signal. Ex.1003, ¶147. This is consistent with the ’866 patent’s low-pass filtering and decimation of an oversampled signal to output a baseband digital signal at a baseband sampling rate. Ex.1001, 3:55-67, 6:22-39; Ex.1003, ¶147.

A POSA would have been motivated to use this ordering because it preserves Moquin’s fine oversampled-domain delay resolution while allowing summation of lower-rate F_s baseband signals using Figure 3’s beamformer/summer arrangement. Ex.1003, ¶¶148-156; Ex.1006, [0012]-[0015], Figs.3-4. Moquin recognizes that operating the “summer and the delay lines” at the higher oversampling rate increases complexity, and Figure 3 already discloses the corresponding design tradeoff: per-channel filtering/decimation before beamformer 13. Ex.1006, [0013], [0015]. A

POSA would have had a reasonable expectation of success because the arrangement uses Moquin’s disclosed delay elements, filter 23, decimator 24, and beamformer 13 for their known functions. Ex.1003, ¶157.

B. Claim 7

As explained in Ground 1A, Moquin discloses every limitation of claim 1. *Supra* §VII.A. Moquin further renders claim 7 obvious. Ex.1003, ¶¶158-175.

As explained for claim 4, Moquin’s Figure 3 teaches filtering/decimating each digital-microphone signal before beamformer 13, while Figure 4 teaches applying delay in the oversampled domain. *Supra* §VIII.A. It would have been obvious to apply Moquin’s filter 23 and decimator 24 to each Figure 4 channel signal after its oversampled-domain delay element and before summing. Ex.1003, ¶161. In that arrangement, Moquin’s filter/decimator is applied to the time-delayed first oversampled digital signal output from the delay element. *Id.*

Moquin’s filter 23 and decimator 24 thus disclose, or at least render obvious, the claimed low-pass filter with decimation. *Id.*, ¶¶167-168. Moquin discloses that the Figure 4 signal is sampled “at a clock rate of 2,048 kHz (M=256 times 8kHz)” and that its “filter and decimator design” produces, e.g., “16 (t=16) bits of resolution at a sampling frequency (Fs) of 8kHz.” Ex.1006, [0014]. Filter 23 provides low-pass/anti-alias filtering of the desired in-band telephony audio while decimator 24 reduces the sampling rate to Fs. Ex.1003, ¶¶162-163; *see* Ex.1006, [0014]; Ex.1014,

3-4; Ex.1021, 1; Ex.1022, 1. Applying Moquin's filter 23 and decimator 24 to the delayed oversampled signal applies a low-pass filter with decimation. Ex.1003, ¶167.

The resulting output is a baseband digital signal delayed by the selected time delay. Moquin's telephony embodiment oversamples at 2,048 kHz and downsamples to $F_s=8$ kHz for audio whose maximum frequency of interest is about 3.5 kHz, so the post-decimation F_s output is the lower-rate telephony/baseband representation of the microphone signal. Ex.1006, [0005], [0014]; Ex.1003, ¶171. This is consistent with the '866 patent's description of low-pass filtering and decimating an oversampled digital signal to output a baseband digital signal at a baseband sampling rate. Ex.1001, 3:55-67, 6:22-39; Ex.1003, ¶171. Because Moquin's filter/decimator is placed downstream of the oversampled-domain delay, it converts the already-delayed signal to baseband without undoing the selected delay; the output is therefore a baseband digital signal delayed by the same time delay. Ex.1003, ¶172.

A POSA would have been motivated to use this arrangement, with a reasonable expectation of success, for the reasons explained for claim 4: it preserves Moquin's fine oversampled-domain delay resolution while producing lower-rate baseband signals using Moquin's disclosed delay elements, filter 23, decimator 24,

and beamformer 13 for their known functions. *Supra* §VIII.A; Ex.1003, ¶174; *see* Ex.1006, [0013]-[0015], Figs.3-4.

C. Claim 8

Moquin renders claim 8 obvious. Ex.1003, ¶¶176-182.

In Moquin's Figure 4 embodiment, the oversampling clock is 2,048 kHz, i.e., $M=256$ times the 8 kHz baseband sampling frequency. Ex.1006, [0014]. Thus, one oversampling-clock period is $1/256$ of one baseband sampling period. Ex.1003, ¶180.

Moquin's tapped shift register provides delays in integer oversampling-clock-cycle increments, as explained for 1[b]. *Supra* §VII.A.3; Ex.1006, [0014]. Selecting a tap corresponding to N oversampling-clock cycles, where $N < 256$, produces a delay equal to $N/256$ of one baseband sampling period. Ex.1003, ¶181. Moquin's 180-stage shift-register example confirms such a fractional-baseband-period delay because 180 oversampling-clock cycles equals $180/256$ of one 8 kHz baseband sampling period. Ex.1006, [0014]; Ex.1003, ¶181.

A POSA would have been motivated to use such a fractional-baseband-period delay because Moquin teaches applying beamforming delays at the oversampling rate to obtain finer steering resolution than is available with baseband-rate delay increments. Ex.1003, ¶182; Ex.1006, [0004], [0006], [0012], [0014].

D. Claim 9

Moquin renders claim 9 obvious. Ex.1003, ¶¶183-189.

As explained for claims 7-8, Moquin discloses delaying at the oversampling rate, $M \cdot F_s$, and outputting a baseband signal at F_s after filtering/decimation. *Supra* §§VIII.B-C; Ex.1006, [0014]. In Moquin’s Figure 4 embodiment, the signal is sampled at 2,048 kHz, i.e., $M=256$ times the 8 kHz baseband sampling rate. Ex.1006, [0005], [0014]. Thus, one 8 kHz baseband sampling period corresponds to 256 oversampling-clock cycles. Ex.1003, ¶186.

Moquin implements delay using “a shift register with taps at the appropriate length (a_x),” and also explains that DSP implementations may use variable-length buffers as delay elements. Ex.1006, [0014], [0016]. Moquin’s 180-stage shift-register example is not limiting; it is one example for the disclosed microphone-array embodiment. *Id.*, [0014]. Selecting a tap position or buffer depth greater than 256 oversampling-clock cycles would produce a delay greater than one 8 kHz baseband sampling period. Ex.1003, ¶187.

A POSA would have been motivated to select such a delay where required by the desired steering geometry. *Id.*, ¶188. Moquin’s disclosed 50-mm telephony-array parameters, when applied to its steering relationship, require more than one 8-kHz baseband period of inter-element delay for end-fire steering. *Id.*; Ex.1006, [0003], [0011]-[0014]. Doing so would preserve Moquin’s fine oversampled-

domain delay resolution, consistent with Moquin’s purpose and its teaching that the same principles apply to other phased arrays using oversampling ADCs. Ex.1003, ¶188; *see* Ex.1006, [0002]-[0006], [0012], [0014], [0017]. A POSA would have had a reasonable expectation of success because increasing shift-register length or buffer depth merely extends Moquin’s disclosed delay mechanism without changing the delay, summing, or filtering/decimation operations. Ex.1003, ¶189.

IX. GROUND 2: CLAIM 3 IS OBVIOUS BASED ON MOQUIN AND LIU

Moquin discloses every limitation of claim 1 as explained in Ground 1A. *Supra* §VII.A. Moquin and Liu further render claim 3 obvious. Ex.1003, ¶¶190-214.

Liu discloses staged reconstruction/decimation for oversampled receive beamforming. Liu explains that “[p]artial reconstruction to a rate less than the oversampling rate, but greater than the Nyquist rate, occurs prior to summation across channels,” and that “[a]fter summation, the samples are reconstructed at a Nyquist or other rate.” Ex.1007, Abstract, [0006]. In Liu’s Figure 2 embodiment, first reconstruction/decimation filter 18 “outputs signals oversampled less than output by the oversampling converters 14 and more than output by the second filter 26,” and summer 24 then sums those signals. *Id.*, [0035], [0038]. Liu further confirms that filters 18 and 26 are operable as “decimation circuits” and that summation occurs “at a data rate less than output by the initial oversampling and

greater than the Nyquist rate or other rate above the Nyquist rate,” before later reconstruction/decimation of the beam sum. *Id.*, [0034], [0039], [0055]-[0057]. Thus, Liu discloses combining at an intermediate sampling rate. Ex.1003, ¶207.

A POSA would have found it obvious to use Liu’s staged approach in Moquin’s architecture by applying a first-stage reconstruction/decimation filter to Moquin’s delayed oversampled channel signals, summing the resulting intermediate-rate signals, and then applying a second-stage reconstruction/decimation filter after summing. *Id.*, ¶208. This would preserve Moquin’s oversampled-domain delay resolution while causing the combining to occur at Liu’s intermediate rate. *Id.* Liu’s multi-bit summer and Moquin’s Figure 3 t-bit beamformer inputs confirm that a POSA would have understood the intermediate-rate summer to operate on multi-bit post-filter/decimator signals. *Id.*; see Ex.1007, [0035], [0038]; Ex.1006, [0013], Fig.3.

A POSA would have been motivated to use Liu’s staged intermediate-rate approach because Moquin recognizes that operating “the summer and delay lines” at the higher oversampling rate increases complexity, while Liu teaches an intermediate design that reduces the summing rate without requiring full final-rate reconstruction in each channel before summation. Ex.1003, ¶191; see Ex.1006, [0015]; Ex.1007, [0019]-[0020], [0035], [0055]-[0057].

A POSA would have had a reasonable expectation of success because the combination uses Moquin's oversampled-domain delay architecture with known staged reconstruction/decimation filters and intermediate-rate summer like Liu's, with each component performing its ordinary function. Ex.1003, ¶214; *see* Ex.1006, [0013]-[0015], Figs.3-4; Ex.1007, [0035], [0038]-[0040], Fig.2.

X. GROUND 3: CLAIM 10 IS OBVIOUS BASED ON MOQUIN AND DEAN

As explained in Ground 1B, Moquin renders claim 7 obvious. *Supra* §VIII.B. Moquin and Dean further render claim 10 obvious. Ex.1003, ¶¶215-236.

Dean discloses a digital beamforming array in which signals from sensor modules are converted to “n-bit” digital signals at an oversampling rate, delayed using shift-register elements, combined by beam adders, and then decimated. Ex.1009, Abstract, 1:45-66, 2:63-3:9, 6:21-40, cls.1-2, 5. Although Dean identifies one-bit oversampled signals as useful in some implementations, Dean teaches that higher-information-flow applications use “a number of bits that is greater than 1” based on the bit-depth/oversampling-rate tradeoff. *Id.*, 3:10-30, 3:54-60. Dean also provides corresponding n-bit implementation details, including n-bit samples, n-bit shift registers, n-bit adders, and decimation. *Id.*, 6:21-40; Ex.1003, ¶¶234-236.

A POSA would have found it obvious and would have been motivated to use a more-than-one-bit oversampling/noise-shaping digitizer like Dean's in Moquin's oversampled beamformer when greater per-sample amplitude information, dynamic

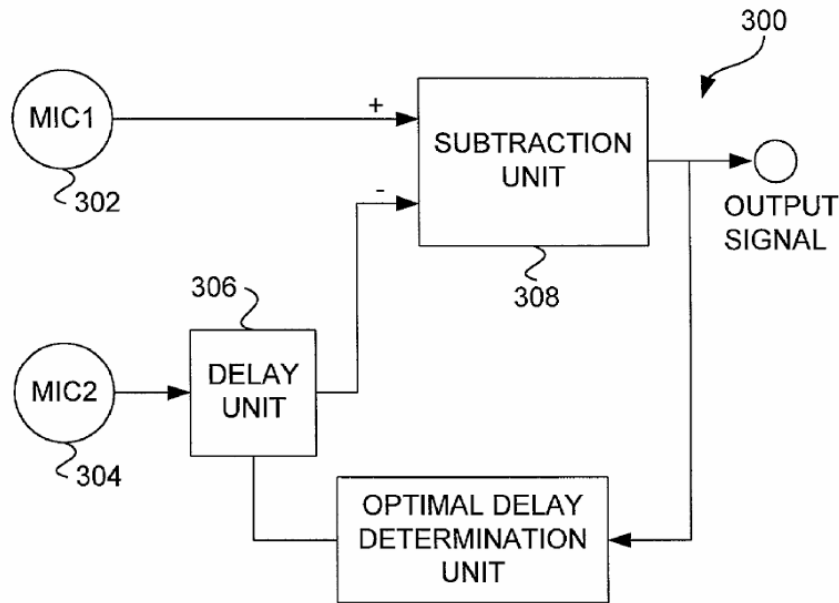
range, or a different oversampling-rate/bit-depth tradeoff was desired. Ex.1003, ¶235. Moquin already discloses oversampled-domain delay-and-combine beamforming and states that its principles apply to phased arrays using oversampling ADCs, including ultrasound, radar, and sonar; Dean likewise addresses oversampled phased-array digital beamforming and discloses a predictable n-bit implementation. Ex.1006, [0014], [0017]; Ex.1009, Abstract, 1:10-12, 2:63-3:9, 6:21-40, cls.2, 5; Ex.1003, ¶236.

A POSA would have had a reasonable expectation of success because Dean expressly discloses using n-bit samples, n-bit shift registers, and an n-bit adder in an oversampled beamforming architecture. Ex.1003, ¶¶234-236; Ex.1009, 6:21-40; *see also* Ex.1023, 1-2. This use of n-bit digitization would preserve the Moquin arrangement discussed for claim 7: the first oversampled digital signal is delayed in the oversampled domain, the delayed signal is filtered/decimated to baseband, and the resulting signal is used for subsequent beamforming processing. Ex.1003, ¶233; *supra* §VIII.B. Thus, in the Moquin-Dean combination, the first oversampled digital signal is digitized to create samples more than one bit deep. Ex.1003, ¶¶233-236.

XI. GROUND 4: CLAIMS 14 AND 19 ARE OBVIOUS BASED ON MOQUIN AND HOU

Moquin discloses every limitation of claims 11 and 16 as explained in Ground 1A. *Supra* §§VII.D, VII.H. Moquin and Hou further render claims 14 and 19 obvious. Ex.1003, ¶¶237-243.

Hou's two-microphone directional processing system includes delay unit 306 and subtraction unit 308:



Ex.1026, Fig.3. Hou explains that subtraction unit 308 “subtracts [a] delayed second electronic sound signal from [a] first electronic sound signal” to produce an output signal, thereby suppressing “unwanted interference.” *Id.*, [0039]. Hou also discloses combining first and delayed second microphone signals by adding or subtracting them. *Id.*, cls.27, 30-31.

A POSA would have been motivated to use Hou's subtraction function in Moquin's arithmetic unit to produce a directional difference beam/null and suppress unwanted interference. Ex.1003, ¶240. The modification would have predictably substituted subtraction for summation at Moquin's arithmetic unit while retaining

Moquin’s sensors, oversampled delay, filtering/decimation, and beamformed-output processing. *Id.*; Ex.1006, [0014]-[0016].

XII. GROUND 5A: CLAIMS 1-5, 7, AND 10 ARE ANTICIPATED BY LIU

A. Claim 1

Liu discloses receive beamforming using oversampled digital samples. Each receive channel includes an oversampling analog-to-digital converter, memory for storing the high-rate samples, a delay controller that selects stored samples to impose beamforming delay, reconstruction/decimation filters, and a summer that combines the channel signals to form a beam. Ex.1007, Abstract, [0006], [0022]-[0025], [0032]-[0038], Figs.2, 7. Liu’s Figure 7 summarizes the relevant sequence: oversampling received signals, relatively delaying samples, partially reconstructing the received signals, summing the delayed samples, and then further reconstructing the beam sum. *Id.*, [0046]-[0057], Fig.7; Ex.1003, ¶¶244-272.

1. 1[pre]

To the extent limiting, Liu discloses 1[pre]. Ex.1003, ¶247. Liu discloses “methods, systems, and receive beamformers for receive beamforming ultrasound information.”. Ex.1007, [0006]. Liu explains that “[t]he received signals for each channel are oversampled for conversion to digital form,” “[d]elays are implemented by selecting data from the sample stream,” and “[p]artial reconstruction...occurs prior to summation across channels.” *Id.* Liu’s Figure 7 “shows one embodiment

of a method for receive beam forming ultrasound information,” in which received channel signals are oversampled, relatively delayed, summed, and reconstructed to form the beam output. *Id.*, [0046]-[0057], Fig.7.

2. 1[a]

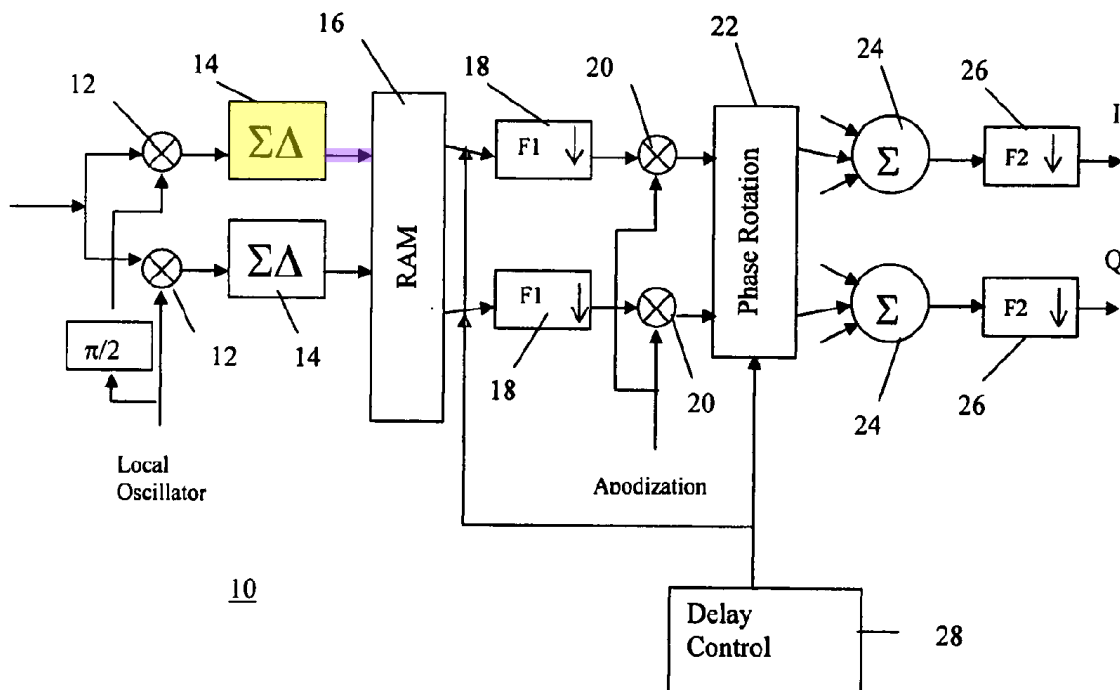
Liu discloses 1[a]. Ex.1003, ¶¶248-252.

Liu’s beamformer includes “oversampling analog-to-digital converters 14,” such as “sigma-delta or other converters,” that sample at a rate higher than Nyquist, e.g., “20-200,” times the Nyquist rate, and output digital samples. Ex.1007, [0025], [0029]-[0030]. Liu’s method likewise oversamples received signals in act 72, where “sigma-delta analog-to-digital converters oversample” and “convert[] the received signals into digital samples.” *Id.*, [0048]. Thus, converter 14 outputs a first oversampled digital signal created at a sampling clock frequency. Ex.1003, ¶250.

That signal is responsive to an analog field. Liu performs receive beamforming on ultrasound information received by transducer elements. Ex.1007, [0006], [0022]-[0023], [0046]-[0048]. In Figure 2, analog mixers 12 provide analog in-phase and quadrature (I/Q) signals, which converters 14 then oversample. Ex.1007, [0026]-[0027], [0047]-[0048]. Those mixed analog signals remain derived from, and preserve information in, the received ultrasound/acoustic field. Ex.1003, ¶251. Liu’s Figure 3 embodiment, which omits the analog mixers, further confirms

that converter 14 may oversample the received signal directly. Ex.1007, [0028]; Ex.1003, ¶251.

Figure 2 illustrates converter 14 as the ADC (yellow) and its oversampled digital output signal (purple) provided to memory 16:



Ex.1007, Fig.2(annotated); Ex.1003, ¶251.

3. 1[b]

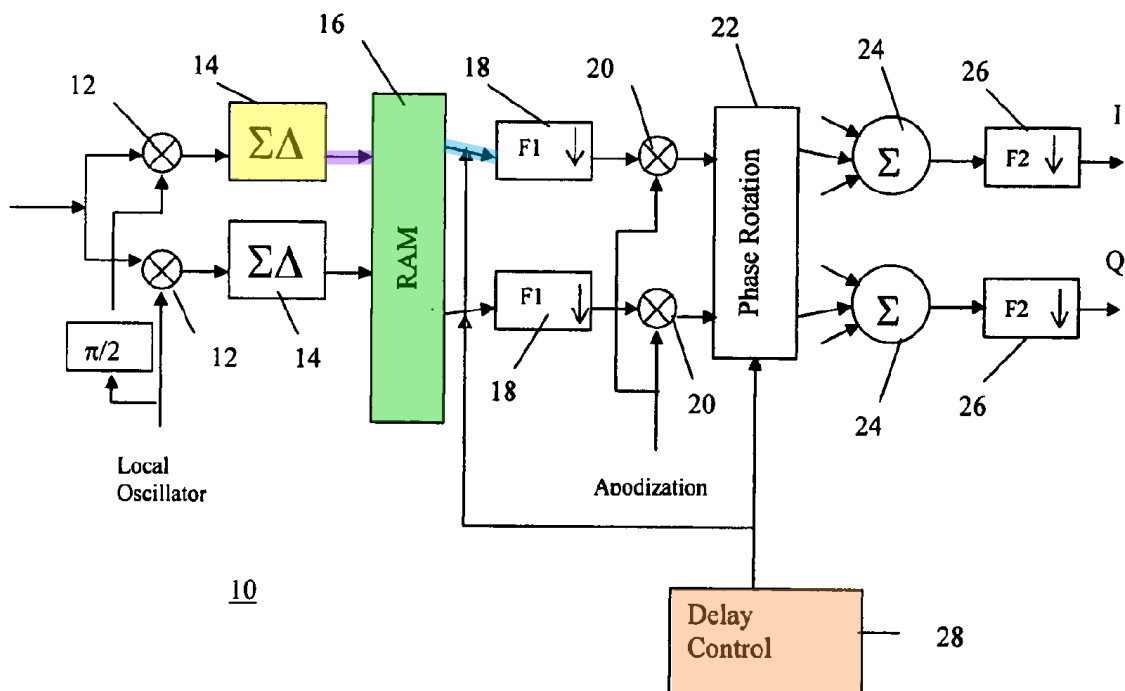
Liu discloses 1[b]. Ex.1003, ¶¶253-260.

Liu states that, in receive beamforming, “channel signals [are] relatively delayed for coherent summation,” and that “[d]elays are implemented by selecting data from the sample stream.” Ex.1007, [0004], Abstract. Liu’s Figure 7 method follows the same order: oversampling received signals in act 72, relatively delaying

samples in act 74, and only then partially reconstructing the received signals in act 76. *Id.*, Fig.7; *see also id.*, [0048]-[0052].

Liu’s Figure 2 embodiment implements that delay with memory 16 and delay controller 28. Converter 14 outputs oversampled digital samples, and memory 16 “receives samples at the oversampling rate,” stores them, and “includes sufficient memory slots to provide the needed delay range.” *Id.*, [0029]-[0032]. Delay controller 28 “controls the output of the memory 16” and “selects stored data from the memory 16 as a function of a delay for the beam,” with the selected samples output to filter 18. *Id.*, [0033]-[0034]. Thus, Liu delays the first oversampled digital signal to produce a time-delayed first oversampled digital signal. Ex.1003, ¶256.

Figure 2 illustrates converter 14 (yellow) outputting oversampled samples (purple) to memory 16 (green), delay controller 28 (orange) controlling delay selection, and selected samples (blue) being output from memory 16:



Ex.1007, Fig.2(annotated); Ex.1003, ¶256.

Liu discloses that the delay is equal to an integer number of sampling clock cycles. Converter 14 outputs samples at an oversampling rate, e.g., “at least 20, such as 20-200, times the Nyquist rate,” with example sampling rates of 240 MHz and 480 MHz. Ex.1007, [0029]-[0030]. Because delay controller 28 imposes delay by selecting samples from the stored oversampled sample stream, selecting a sample shifted by k sample positions imposes a delay of k oversampling sample periods—i.e., an integer number of converter sampling-clock cycles. Ex.1003, ¶259; *see* Ex.1007, [0032]-[0033], [0049], [0051]. Liu’s disclosure that memory 16 may be a “shift register” confirms this understanding. Ex.1003, ¶260; *see* Ex.1007, [0032].

4. 1[c]

Liu discloses 1[c]. Ex.1003, ¶¶261-272.

Liu's receive beamformer "includes a plurality of receive channels," with "[e]ach channel correspond[ing] to one or more elements." Ex.1007, [0023]. Figure 2 shows one channel, and Liu explains that "[t]he other channels have the same or different components," including "the oversampling analog-to-digital converters 14." *Id.*, [0025]. Liu's method likewise oversamples "the received signals in each channel" and "converts the received signals into digital samples." *Id.*, [0048]. Thus, Liu discloses first and second oversampled digital signals generated in respective receive channels, each responsive to the received ultrasound/acoustic field through its corresponding transducer element(s). Ex.1003, ¶265; *see* Ex.1007, [0022]-[0023], [0047]-[0048].

As explained for 1[b], Liu discloses delaying oversampled channel samples by selecting stored data from memory 16 as a function of beam delay. *Supra* §XII.A.3; *see also* Ex.1007, [0049], [0032]-[0033]. Liu's filter 18 then partially reconstructs the selected samples before combining those delayed channel signals at summer 24 to form the beam. Liu discloses that "[t]he data from the channels is summed to form data representing a beam or sub-array beam." Ex.1007, [0023]. "[S]ummer 24 sums the relatively apodized and focused signals from a plurality of channels," and Figure 7 similarly explains that "[t]he samples from the different channels are summed," and that "[b]y summing focused samples from the different channels...a beam sum is formed." *Id.*, [0038], [0046], [0055]-[0056], Figs.2, 7.

Figure 2 illustrates converter 14 (yellow) outputting oversampled samples (purple) to memory 16 (green), delay controller 28 (orange) controlling delay selection, and summer 24 (tan) combining signals from multiple channels:



Ex.1007, Fig.2(annotated); Ex.1003, ¶270.

Thus, Liu anticipates claim 1. Ex.1003, ¶¶247-272.

B. Claim 2

Liu anticipates claim 2. Ex.1003, ¶¶273-276.

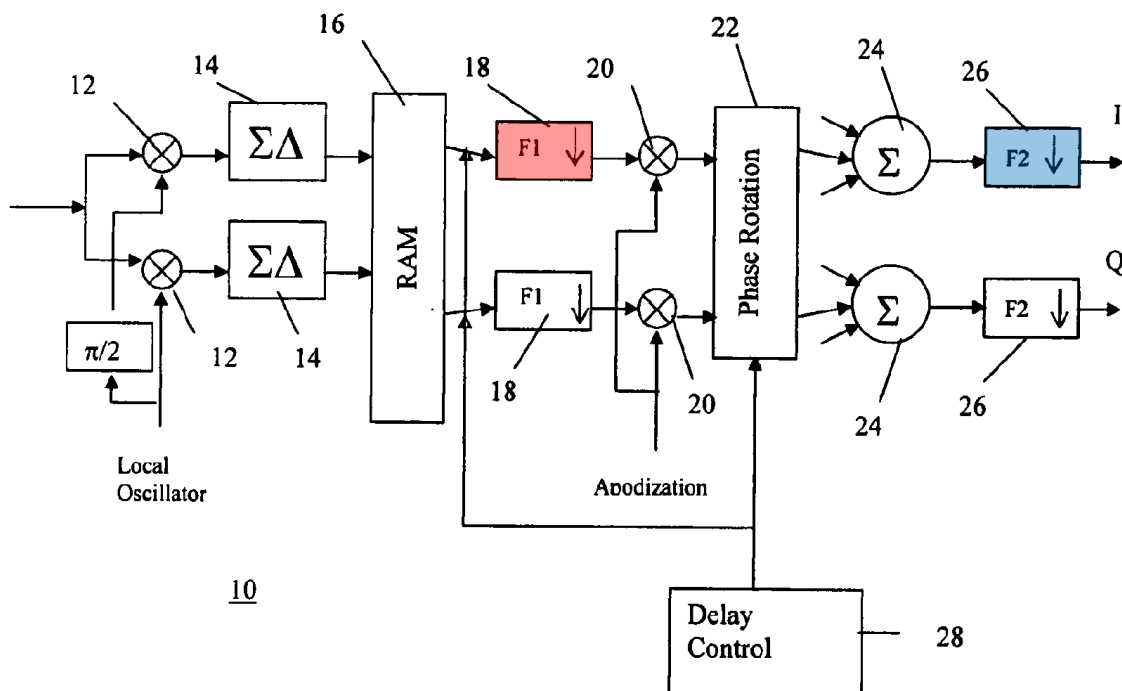
Liu discloses that the signals combined by summer 24 remain oversampled—in Liu’s staged reconstruction embodiment, filter 18 partially reconstructs the selected samples to a lower rate that is “still oversampled relative to the Nyquist rate,” and outputs signals “oversampled less than output by the oversampling converters 14 and more than output by the second filter 26.” Ex.1007, [0052], [0035], Fig.2. Liu states that, in act 80, summation is performed “at a data rate less than output by the initial oversampling and greater than the Nyquist rate or other rate above the Nyquist rate.” *Id.*, [0055], Fig.7.

Thus, Liu’s summer 24 combines signals derived from the delayed channel samples before final reconstruction/decimation, while those signals are still oversampled relative to the Nyquist rate. Ex.1003, ¶276.

C. Claim 3

Liu anticipates claim 3. Ex.1003, ¶¶277-280.

In Liu’s Figure 2 embodiment, after delay selection from memory 16, the channel signals are partially reconstructed/decimated by filter 18 (red) and then combined at summer 24 before second filter 26 (blue) further reconstructs/decimates the beam sum. *See* Ex.1007, [0033]-[0040], [0046]-[0057], Figs.2, 7.



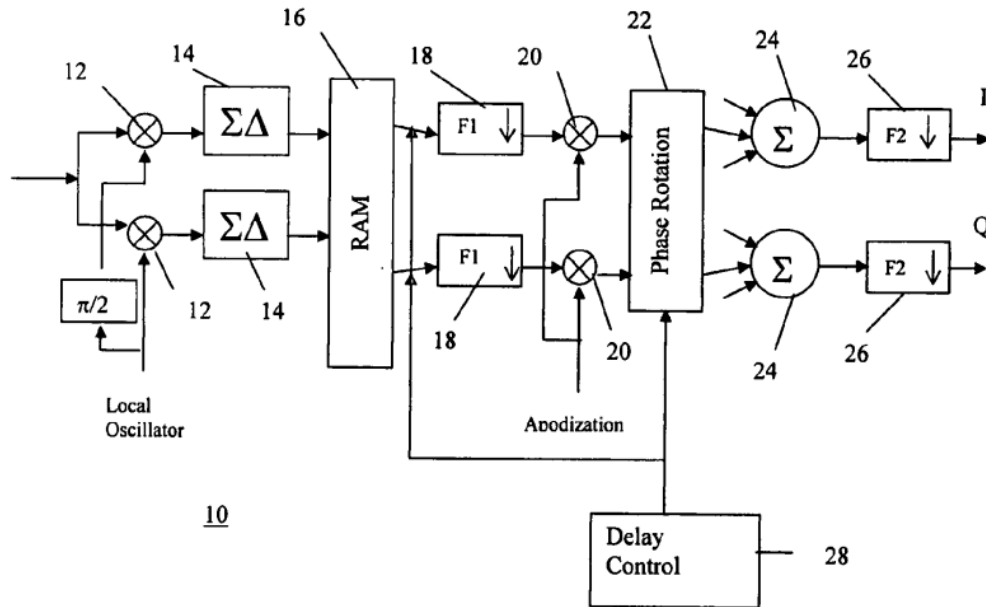
Id., Fig.2(annotated); Ex.1003, ¶279. Liu explains that “filter 18 outputs signals oversampled less than output by the oversampling converters 14 and more than output by the second filter 26.” Ex.1007, [0035]. Liu states that summation is performed “at a data rate less than output by the initial oversampling and greater than the Nyquist rate or other rate above the Nyquist rate,” and that later reconstruction reduces the beam-sum data rate. *Id.*, [0055]-[0057]. Thus, the signals combined at summer 24 are at a rate between the initial oversampling-converter rate and the later post-summation output rate, i.e., at an intermediate sampling rate. Ex.1003, ¶280.

D. Claim 4

Liu anticipates claim 4. Ex.1003, ¶¶281-284.

Liu identifies Figure 2 as a “base band receive beam former system.”

Ex.1007, [0013].



Id., Fig.2. Analog mixers 12 provide I/Q signals “at a base band frequency for base band beamforming,” and Liu explains that “base band signals are being sampled.” *Id.*, [0026], [0029]; *see also id.*, [0047]. Those I/Q signals, which Liu characterizes as baseband, are oversampled, delayed by memory 16/delay controller 28, partially reconstructed/decimated by filter 18, and summed by summer 24. *Id.*, [0035], [0038], Fig.2. Thus, to the extent PO contends that “baseband signal domain” encompasses baseband-frequency I/Q signals represented at an oversampled or intermediate rate, Liu anticipates claim 4 because summer 24 combines those signals. Ex.1003, ¶284.

E. Claim 5

Liu anticipates claim 5. Ex.1003, ¶¶285-288.

Liu explains that its receive beamformer includes “a plurality of receive channels” and that “[e]ach channel corresponds to one or more elements.” Ex.1007, [0023]. Liu further explains that “[t]he other channels have the same or different components,” including oversampling converters 14, and that “the received signals in each channel are oversampled.” *Id.*, [0025], [0047]-[0048].

Thus, Liu discloses that the first and second oversampled digital signals are obtained from different transducer elements/sensors, e.g., different receive channels associated with different ultrasound transducer elements. Ex.1003, ¶288.

F. Claim 7

Liu anticipates claim 7. Ex.1003, ¶¶289-296.

Filter 18 is a reconstruction/decimation filter that reconstructs selected samples “by filtering and/or decimating,” reduces sample rate, and functions as a “first low pass filter” that constructs higher-bit-width samples from the converter output before summation. Ex.1007, [0009], [0034]-[0035], [0052]; *see also id.*, [0009], cls.21, 23. Thus, filter 18 applies a low-pass filter with decimation to the time-delayed first oversampled digital signal output from memory 16. Ex.1003, ¶¶291-294.

To the extent PO contends that a partially reconstructed and decimated baseband-frequency I/Q signal constitutes a “baseband digital signal,” filter 18 outputs such a signal delayed by the selected time delay. Liu identifies Figure 2 as

a “base band receive beam former system,” explains that analog mixers 12 provide I/Q signals “at a base band frequency for base band beam forming,” and states that “base band signals are being sampled in the embodiment of FIG. 2.” Ex.1007, [0013], [0026], [0029]; *see also id.*, [0047]. Because converters 14 oversample those baseband I/Q signals and filter 18 filters/decimates the delayed samples selected from memory 16, filter 18 outputs delayed, lower-rate baseband I/Q channel data. Ex.1007, [0035], [0052], Fig.2; Ex.1003, ¶295. The output remains delayed because filter 18 operates on the already-selected delayed samples. Ex.1003, ¶295.

G. Claim 10

Liu anticipates claim 10. Ex.1003, ¶¶297-301.

The '866 patent uses “one bit deep” and “bit depth” to refer to the number of bits used to represent a sample. Ex.1003, ¶299; *see* Ex.1001, 4:59-5:13. As explained for 1[a], Liu’s converter 14 digitizes the received signal to produce the first oversampled digital signal. *Supra* §XII.A.2. Liu discloses sigma-delta or other oversampling converters that output samples at an oversampling rate and states that “[h]igher bit widths, such as two, four, or more, may be provided.” Ex.1007, [0029]-[0030], [0048]; *see also id.*, cl.2. Those two-bit, four-bit, or greater-bit outputs are samples more than one bit deep. Ex.1003, ¶300. Liu’s beamforming path is compatible with such samples because memory 16 may be “single or multi-bit” and summer 24 may be a “multiple bit sample summer.” Ex.1007, [0032], [0038].

XIII. GROUND 5B: CLAIMS 4 AND 7-10 ARE OBVIOUS BASED ON LIU

A. Claim 4

As discussed in Ground 5A, Liu discloses baseband-frequency combining. *Supra* §XII.D. To the extent “baseband signal domain” requires final-rate channel demodulation/reconstruction before summation, Liu renders claim 4 obvious. Ex.1003, ¶¶302-303.

Liu discloses a selectable endpoint in which “complete channel demodulation is provided by long low-pass filters for each channel and the beam sum is computed at the signal Nyquist rate.” Ex.1007, [0020]. A POSA would have been motivated to use that option when fully reconstructed baseband-rate summation was desired and its filter-length/cost tradeoff was acceptable. Ex.1003, ¶304; Ex.1007, [0019]-[0020]. That implementation would use Liu’s same oversampled-sample delay selection, reconstruct/demodulate the selected channel samples before summation, and compute the beam sum from fully reconstructed baseband channel samples. Ex.1003, ¶304; *see also* Ex.1007, [0049]-[0056].

B. Claim 7

As discussed in Ground 5A, Liu discloses filtering/decimation of the delayed samples to produce lower-rate baseband I/Q data. *Supra* §XII.F. To the extent claim 7 requires a fully reconstructed baseband-rate output, Liu renders claim 7 obvious for the reasons discussed for claim 4 in this ground. Ex.1003, ¶305.

Liu discloses a complete-channel-demodulation endpoint in which “long low-pass filters” are used for each channel and “the beam sum is computed at the signal Nyquist rate.” Ex.1007, [0020]. In that option, the selected delayed channel samples are low-pass filtered and decimated before summation to output delayed baseband-rate channel data. Ex.1003, ¶305.

It would have been obvious to use Liu’s complete-demodulation option when the design objective favored fully reconstructed baseband channel data before summation—for example, to compute the beam sum at the final signal/Nyquist rate and address the dynamic-receive-artifact concern Liu associates with the opposite, no-channel-demodulation endpoint—and when the added long-filter complexity was acceptable. *Id.*, ¶306. Such circumstances include designs not using parallel beamforming, or designs in which duplicating or time-multiplexing the long channel filters was an acceptable cost. *Id.* Liu presents a known design tradeoff, not inoperability or a reason a POSA would have avoided complete demodulation in suitable implementations. *Id.*

C. Claims 8-9

Liu renders obvious claims 8-9. Ex.1003, ¶¶307-315. As explained, Grounds 5A-5B provide alternative bases for the claim 7 limitations underlying claims 8-9. *Supra* §§XII.F, XIII.B; Ex.1003, ¶309.

For an oversampling-to-baseband ratio R , a delay of k oversampling sample-clock periods equals k/R of one baseband sampling period. Ex.1003, ¶311; *see* Ex.1001, 4:50-5:19, 7:1-19, 13:47-14:51. Thus, $k < R$ provides a fractional-baseband-period delay, and $k > R$ provides a delay greater than one baseband sampling period. Ex.1003, ¶312.

Liu discloses oversampling at “at least 20,” including “20-200” times the Nyquist rate, with fixed, programmable, or variable rates. Ex.1007, [0029]-[0030], [0048]. Liu selects earlier- or later-occurring stored samples according to the desired focusing delay, and memory 16 is sized for the needed delay range. *Id.*, [0032]-[0033], [0049]-[0051]. A non-zero offset $k < R$ provides the fractional-baseband-period delay of claim 8. Ex.1003, ¶313. For claim 9, in Liu’s disclosed Nyquist-rate baseband option, its 20x oversampling ratio means that one baseband sampling period spans 20 oversampling sample-clock periods; selecting $k > 20$ therefore provides the claimed greater-than-baseband-period delay. Ex.1007, [0020], [0030]; Ex.1003, ¶314. Liu’s focusing profile determines each channel’s desired delay, and memory 16 is sized for the needed delay range and largest delay, with controller 28 selecting earlier- or later-occurring samples accordingly. Ex.1007, [0004], [0032]-[0033], [0049]-[0051]. A POSA would therefore have regarded selecting an offset above 20 as a predictable use of Liu’s disclosed mechanism to implement the delay

specified by the focusing profile, with expected success because the same memory and controller implement that offset like any other integer offset. Ex.1003, ¶315.

A POSA would have been motivated to select the required offsets because Liu's dynamic receive focusing requires relative delays that vary with element position and imaging depth, and memory/delay controller 28 provides the needed delay range. *Id.*; see Ex.1007, [0004], [0032], [0049]-[0051].

D. Claim 10

Liu renders obvious claim 10 under either claim-7 analysis in Grounds 5A-5B, for the reasons discussed for claim 10 in Ground 5A. *Supra* §XII.G; Ex.1003, ¶316.

XIV. GROUND 6: CLAIMS 6-10 ARE OBVIOUS BASED ON LIU AND ANDERSEN

A. Claim 6

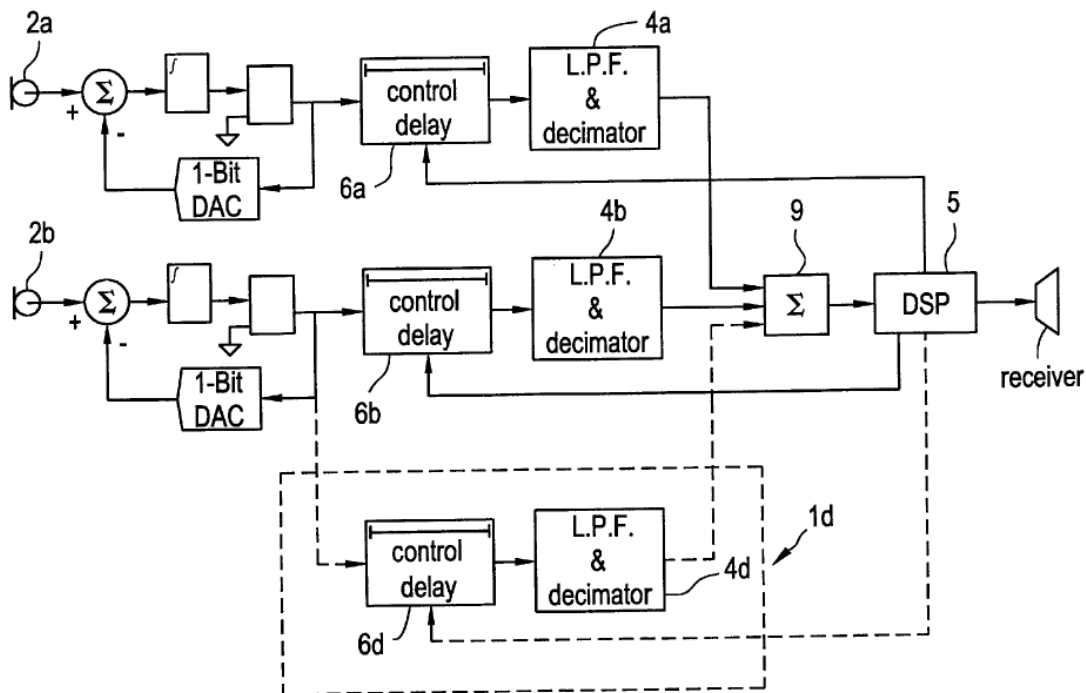
As explained in Ground 5A, Liu discloses every limitation of claim 1. *Supra* §XII.A. Liu and Andersen further render obvious claim 6. Ex.1003, ¶¶317-332.

Andersen teaches the claimed same-sensor parallel delay/filter paths. Andersen discloses a hearing aid with beamforming properties using ADC microphone channels, low-pass filters/decimators, controllable delay devices, and summing/combinator circuitry. Ex.1008, Abstract, 2:5-25, 3:24-45, Fig.3.

In Andersen's Figure 7, a single microphone channel's microphone 2b and ADC feed one path through controllable delay 6b and low-pass filter

(LPF)/decimator 4b and a parallel dotted-line path through controllable delay 6d and

LPF/decimator 4d:



Id., Fig.7, 4:18-27. Andersen explains that “at least one of the microphone channels has not only one delay device and one digital low pass filter and decimator filter but two of those in parallel,” and further discloses that more than two delay devices may be used in parallel in the same microphone channel. *Id.*, 4:18-27. Andersen’s claim 11 likewise recites a microphone channel equipped with an ADC “including at least two delay devices in parallel” operating on two low-pass filters/decimators, with the resulting outputs combined in a combination circuit. *Id.*, cl.11.

Thus, Andersen teaches multiple oversampled path signals derived from the same microphone/sensor before the parallel delay/filter paths. Ex.1003, ¶327.

A POSA would have been motivated to apply Andersen's same-sensor parallel-delay-path teaching to Liu's oversampled receive-beamforming architecture. *Id.*, ¶331. Liu already stores oversampled samples from a single receive channel in memory 16 and, under delay controller 28, makes multiple selections from the same stored data samples for different beam delays, focusing profiles, and beamforming paths. Ex.1007, [0032]-[0033], [0043]-[0044], [0049]-[0051]. Applying Andersen's teaching would provide multiple delayed sample streams from a single Liu receive channel/transducer element, increasing focusing/beamforming flexibility without adding another sensor or ADC. Ex.1003, ¶332; Ex.1008, 1:64-2:25, 3:25-45, 4:18-27.

A POSA would have had a reasonable expectation of success because the combination uses Liu's oversampling converter, memory/delay controller, filters, and summer with Andersen's known parallel delay/filter-path arrangement, preserving Liu's oversampling, delay-selection, filtering/decimation, and summing operations. Ex.1003, ¶332. Thus, in the Liu-Andersen combination, first and second oversampled digital signals are obtained from the same sensor. *Id.*

B. Claim 7

Even if neither Liu-alone claim-7 theory in Grounds 5A-5B is accepted (*supra* §§XII.F, XIII.B), the Liu-Andersen combination renders claim 7 obvious. Ex.1003, ¶¶333-351.

Liu's filter 18 is a reconstruction/decimation filter that reduces incoming sample rate and partially reconstructs the selected samples. Ex.1007, [0034]-[0035], [0052]. Andersen confirms that a conventional post-delay reconstruction/decimation filter for a sigma-delta/oversampled beamforming path is a digital low-pass filter with decimation. Ex.1003, ¶344.

Andersen discloses a hearing aid having sigma-delta microphone channels with a controllable delay in the high-clock-frequency one-bit stream before the channel's digital low-pass filter/decimator, which converts the stream to lower-clock-frequency digital words, e.g., 16 or 32 kHz, for DSP beamforming. Ex.1008, Abstract, 2:5-25, 3:24-45, Figs.3-4. Thus, Andersen discloses applying a low-pass filter with decimation to a time-delayed oversampled digital signal to produce a lower-rate digital signal delayed by the selected time delay. Ex.1003, ¶345.

It would have been obvious to implement Liu's post-delay filter 18 as a low-pass decimating reconstruction filter, as taught by Andersen. *Id.*, ¶333. Both references use oversampled/sigma-delta digitization, high-rate delay, decimation/reconstruction, and beam combining, and Liu already places filter 18 after delay selection and before summation—the same relevant ordering Andersen uses. *Id.*; see Ex.1007, [0006], [0029]-[0035], [0038], [0049]-[0056]; Ex.1008, Abstract, 2:5-25, 3:25-45, Figs.3-4.

A POSA would have been motivated to apply Andersen's low-pass-decimating filter teachings to recover the in-band/baseband signal from Liu's delayed oversampled samples, reduce sample rate, and suppress out-of-band quantization noise. Ex.1003, ¶348. A POSA would have had a reasonable expectation of success because the implementation combines Liu's delayed oversampled sample stream and post-delay filter 18 with a known low-pass-filter/decimator implementation like Andersen's to perform the same ordinary reconstruction/decimation function. *Id.*, ¶350.

To the extent PO argues that claim 7 requires a fully reconstructed signal/baseband Nyquist rate output, the Liu-Andersen combination renders that reading obvious. *Id.*, ¶351. For Liu's complete-channel-demodulation option, Andersen further discloses delaying the oversampled stream before low-pass filtering and decimation, with the resulting lower-rate channel outputs then combined. *Id.*; see Ex.1008, 3:4-45. With the implementation, the selected delayed Liu samples would be low-pass filtered/decimated before summation, so the filter output is the claimed baseband digital signal delayed by the selected time delay. Ex.1003, ¶351.

C. Claims 8-9

Even if Liu alone does not render claims 8-9 obvious as explained in Ground 5B (*supra* §XIII.C), the Liu-Andersen combination does. Ex.1003, ¶¶352-355.

Andersen places a controllable delay in the high-clock-frequency sigma-delta bitstream before low-pass filtering/decimation, teaches that delay may be implemented using a controllable tapped shift register, and explains that high-rate sampling provides much smaller delay steps than lower-rate processing. Ex.1008, 1:51-57, 2:5-25, 3:4-18, 3:25-38, cl.6. Implementing Liu's sample-selection delay with Andersen's high-rate delay line/shift register would desirably provide the claimed fractional or greater-than-baseband-period delays by selecting the needed tap/offset for Liu's dynamic receive focusing. Ex.1003, ¶355; *supra* §XIII.C. A POSA would have expected success because selecting a different tap/offset simply changes delay amount while preserving the same known high-rate, pre-filter/decimator delay mechanism. Ex.1003, ¶355.

D. Claim 10

Applying Andersen's low-pass-filter/decimator teachings in the Liu-Andersen combination does not alter Liu's upstream higher-bit-width digitization. Ex.1003, ¶356. Thus, the combination renders claim 10 obvious for the reasons explained in Grounds 5A-5B. *Id.*; *supra* §§XII.G, XIII.D.

XV. GROUND 7A: CLAIMS 1, 4-8, AND 11-20 ARE ANTICIPATED BY ANDERSEN

Andersen discloses a hearing aid with beamforming properties using at least two microphone channels. Ex.1008, Abstract, 3:25-45. Each channel includes a microphone and sigma-delta ADC that converts sound into a high-clock-frequency

one-bit stream, and at least one such stream is delayed before low-pass filtering/decimation. *Id.*, Abstract, 1:40-57, 2:5-25, 3:4-22, Fig.4. Andersen then combines the microphone-channel outputs for beamforming. *Id.*, 3:57-62.

A. Claim 1

1. 1[pre]

To the extent limiting, Andersen discloses 1[pre]. Ex.1003, ¶357. Andersen discloses a “hearing aid with beamforming properties” having multiple microphone channels whose output signals are combined in summing circuit 7 and passed to DSP 5 so that the DSP directs the “beam in desired directions.” Ex.1008, Abstract, 3:42-45, 3:57-62; *see also id.*, 1:40-47, 2:26-30, Fig.4, cls.1, 12.

2. 1[a]

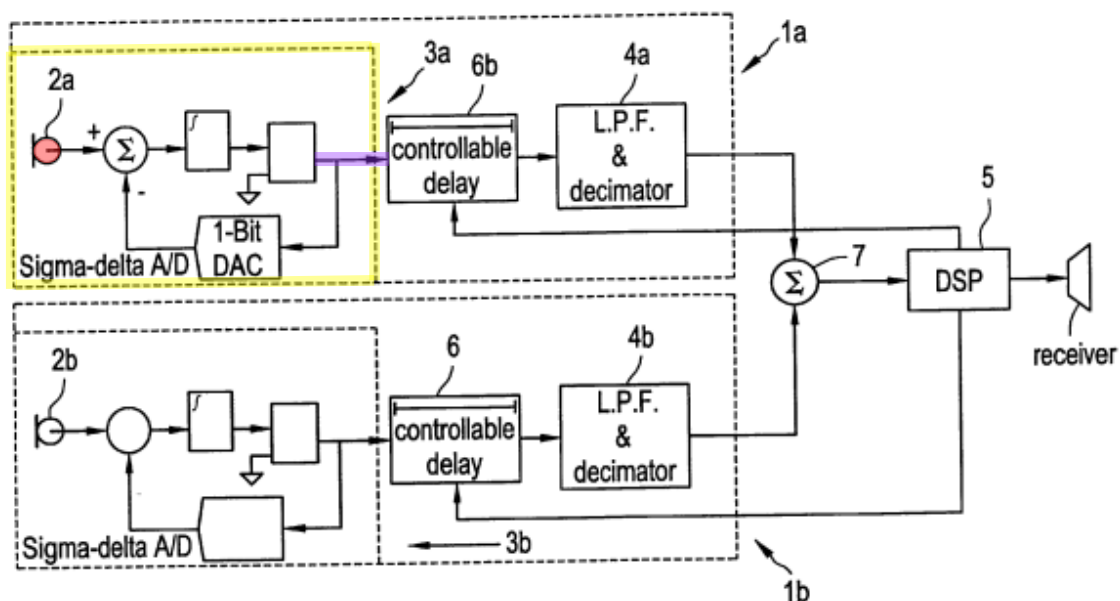
Andersen discloses 1[a]. Ex.1003, ¶¶358-363.

Andersen discloses a “hearing aid with beam forming properties, having at least two microphone channels (1a, 1b).” Ex.1008, Abstract. Each channel includes a microphone (2a/2b) and a sigma-delta analog-to-digital converter (3a/3b). *Id.*; *see also id.*, 2:40-41, 3:25-29. Andersen explains that the converter operates at a “high clock frequency,” e.g., “1 MHz or higher,” and produces a “1 bit stream” at the clock frequency, which is oversampled relative to the bandwidth of the acoustic input signal. *Id.*, 3:4-22; *see also id.*, 1:40-56, 3:30-39; Ex.1003, ¶361.

That high-clock-frequency one-bit stream is the claimed first oversampled digital signal. Ex.1003, ¶¶360-362. It is output from an ADC because it is produced by sigma-delta analog-to-digital converter 3a, and it is created at a sampling clock frequency because Andersen’s converter is clocked at the high sampling rate. *Id.*

The signal is responsive to an analog field because microphone 2a receives sound—an analog acoustic-pressure field—and provides the resulting analog microphone signal to sigma-delta analog-to-digital converter 3a. Ex.1008, Abstract, 3:25-29, 1:40-46, cl.1.

Figure 4 illustrates microphone 2a (red) providing the analog microphone signal to sigma-delta analog-to-digital converter 3a (yellow), which outputs the first oversampled digital signal (purple):



Id., Fig.4(annotated); Ex.1003, ¶361.

3. 1[b]

Andersen discloses 1[b]. Ex.1003, ¶¶364-369.

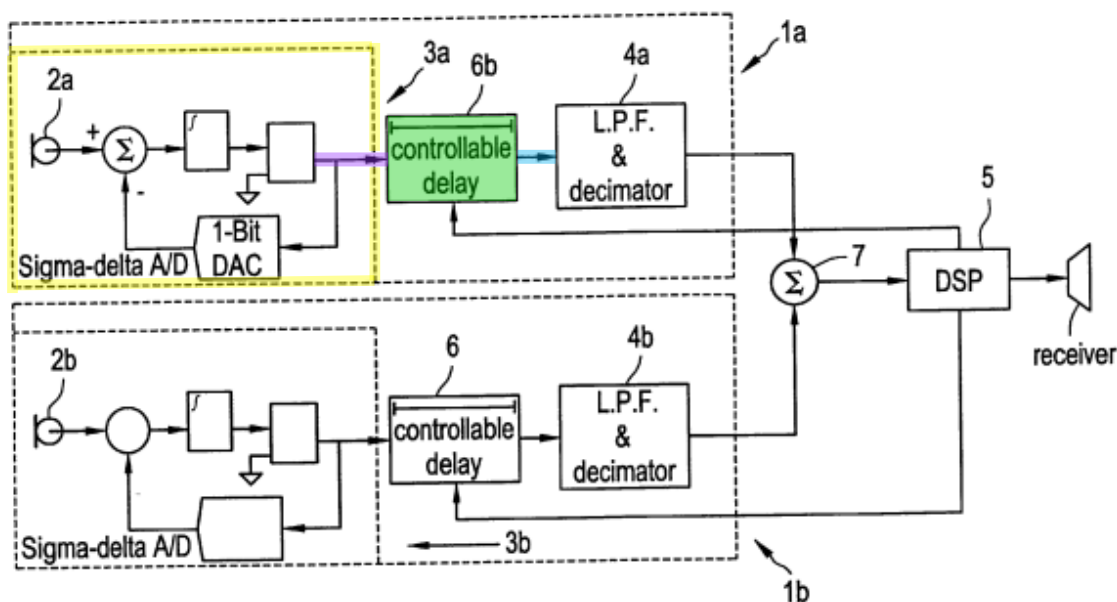
Andersen discloses delaying the first oversampled digital signal identified for 1[a]. Andersen places “a controllable delay device 6” on that bit-stream path before the channel’s digital low-pass filter/decimator. Ex.1008, 2:5-25, 3:25-29, 3:52-59, Fig.4. Andersen explains that “[t]his delay device is typically a multiple tap shift register” and that DSP 5 “will decide how many 1 bit stages each sample of the bit stream will go through (and thus be delayed by)” before being tapped and sent further in the system. *Id.*, 3:31-36. Thus, Andersen discloses delaying the first oversampled digital signal before low-pass filtering/decimation to produce a time-delayed first oversampled digital signal. Ex.1003, ¶367.

Andersen also discloses that the delay is an integer number of sampling-clock cycles. Andersen’s sigma-delta analog-to-digital converter operates at a “high clock frequency,” e.g., “1 MHz or higher,” and its controllable delay device is a one-bit adjustable digital delay line/tapped shift register in the converter bit stream. Ex.1008, 3:4-22, 3:30-38. In a tapped shift register, each clock advances the bit stream by one stage; selecting N shift-register stages delays the bit stream by N sampling-clock periods. Ex.1003, ¶368. Andersen confirms that relationship, explaining that the high-rate bit-stream delay provides “delayed difference steps of multiples of 1 usec” and that “[t]he resulting delay is equal to the number of stages

times the inverse sampling rate.” Ex.1008, 1:51-57, 3:31-39; *see also id.*, 2:21-25.

Thus, Andersen discloses a delay equal to N sampling-clock cycles, where N is an integer. Ex.1003, ¶368.

Figure 4 illustrates that the upper channel, sigma-delta analog-to-digital converter 3a (yellow) outputs the first oversampled digital signal (purple), controllable delay 6b² (green) is interposed on that bit-stream path before LPF/decimator 4a, and the bit-stream output of delay device 6b is a time delayed first oversampled digital signal (blue):



² Andersen’s text refers to Figure 4 delay devices 6a/6b, while Figure 4 labels them 6b/6; the discrepancy is immaterial to Andersen’s per-channel controllable-delay disclosure. Ex.1008, 3:52-53, Fig.4; Ex.1003, ¶369 n.12; *see also* Ex.1008, Figs.5-7.

Ex.1008, Fig.4(annotated); Ex.1003, ¶368.

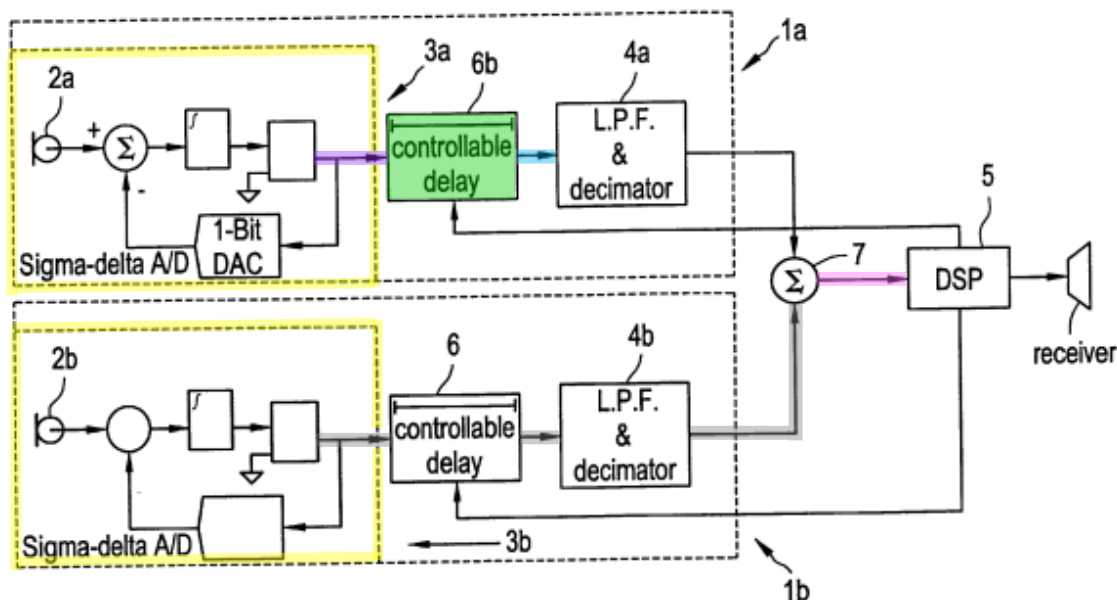
4. 1[c]

Andersen discloses 1[c]. Ex.1003, ¶¶370-375.

Andersen discloses “at least two microphone channels (1a, 1b),” each including a microphone (2a/2b) and a sigma-delta analog-to-digital converter (3a/3b). Ex.1008, Abstract, 3:25-29. As explained for 1[a]-1[b], converter 3a outputs first oversampled digital signal responsive to sound received by microphone 2a, and Andersen’s controllable delay device delays that signal before low-pass filtering/decimation. *Supra* §§XV.A.2-3. Converter 3b likewise outputs a second high-clock-frequency one-bit stream (a second oversampled digital signal) responsive to sound received by microphone 2b, and therefore responsive to the same analog acoustic field. Ex.1003, ¶372.

In Figure 4, downstream channel signals respectively derived from the time-delayed first oversampled digital signal and the second oversampled digital signal through the corresponding low-pass filters/decimators are combined in summing circuit 7 and then provided to DSP 5. Ex.1008, 3:57-59, Fig.4; Ex.1003, ¶373. Andersen explains that the controllable delay allows “the DSP [to] direct the beam in the desired directions,” and that the hearing aid “can be used for active beamforming.” Ex.1008, 3:42-45, 1:40-47; *see also id.*, 3:59-62.

Figure 4 illustrates the relevant structure: in the upper channel, converter 3a (yellow) outputs the first oversampled digital signal (purple) and controllable delay 6b (green) delays that bit stream to output a time delayed first oversampled digital signal (blue); in the lower channel, converter 3b (yellow) outputs the second oversampled digital signal (gray); and the channel signals are combined (pink) for beamforming:



Id., Fig.4(annotated); Ex.1003, ¶373.

Thus, Andersen anticipates claim 1. Ex.1003, ¶¶357-375.

B. Claim 4

Andersen anticipates claim 4. Ex.1003, ¶¶376-378.

A POSA would have understood “baseband signal domain,” in the context of the ’866 patent, to include at least the lower-rate digital signal domain produced after the receiver’s low-pass filtering/decimation has converted an oversampled digital

signal to a signal at the baseband sampling rate. *Id.*, ¶377; *see* Ex.1001, 3:6-7, 7:42-51, 8:55-56, 13:56-58, 15:9-36. For example, the '866 patent describes a receiver that low-pass filters and decimates an oversampled digital signal and outputs a “baseband digital signal,” and elsewhere identifies a 16 kHz post-decimation output as a signal at the baseband sample rate. *See* Ex.1001, 2:54-59, 3:55-67, 6:44-52, 7:20-32, 8:27-39.

Andersen discloses combining in that lower-rate post-decimation domain. Andersen’s sigma-delta analog-to-digital converters 3a/3b generate one-bit streams at a high clock frequency, and digital low-pass filter/decimator filters 4a/4b convert the corresponding one-bit streams into digital word sequences at a lower clock frequency, e.g., 16 or 32 kHz. Ex.1008, 3:4-16. Andersen then explains that “[t]he output signals of the digital low pass filter and decimator filters 4a and 4b are combined in a summing circuit 7 and passed on to the DSP.” *Id.*, 3:57-59, Fig.4. Thus, Andersen’s combining occurs after low-pass filtering and decimation have converted the high-clock-frequency bit streams into lower-rate digital word sequences that the DSP uses for further processing. Ex.1003, ¶378; *see also* Ex.1001, 7:20-32, 8:27-39, 14:45-51, cl.26 (16 kHz as a “baseband sampling frequency” or “baseband sampling rate”).

C. Claim 5

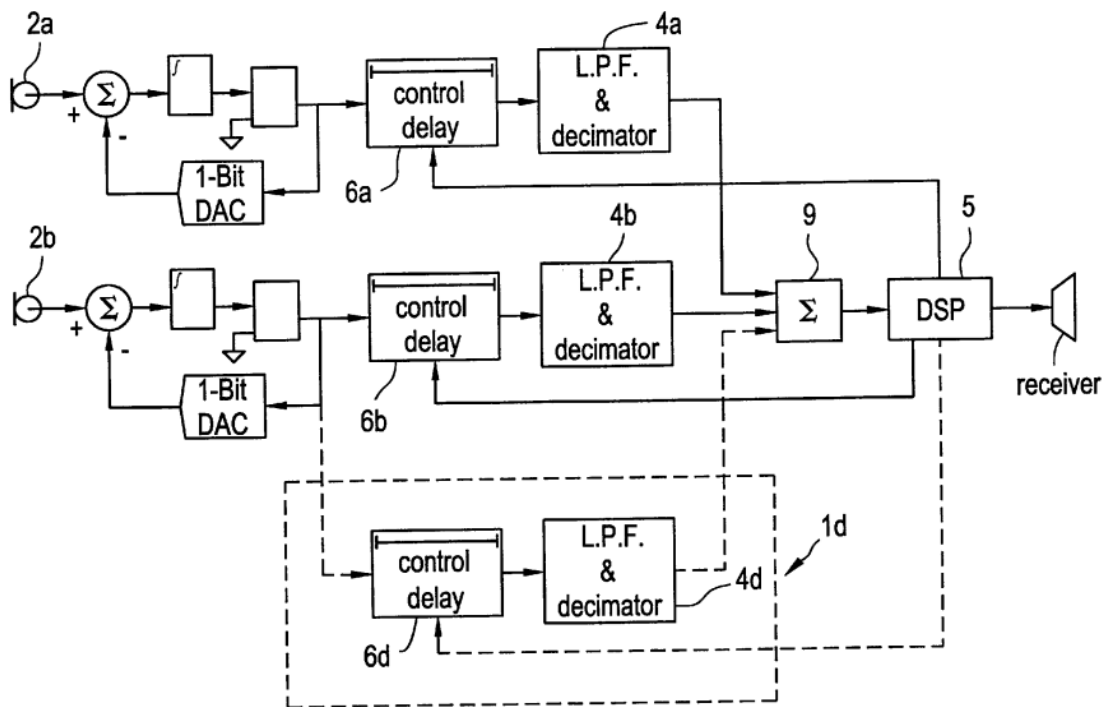
Andersen anticipates claim 5. Ex.1003, ¶¶379-381.

Andersen's hearing aid has "at least two microphone channels (1a, 1b)," with microphones "2a and 2b" and corresponding sigma-delta analog-to-digital converters "3a and 3b." Ex.1008, Abstract, 3:25-29, Fig.4. Because microphones 2a and 2b are different sensors, Andersen discloses that the corresponding oversampled digital signals are obtained from different sensors. *Id.*

D. Claim 6

Andersen anticipates claim 6. Ex.1003, ¶¶382-389.

Andersen's Figure 7 further adds parallel delay/filter paths to one microphone channel in Andersen's Figure 4 arrangement. *Id.*, ¶383. The same microphone/sensor and sigma-delta ADC feed one path through controllable delay 6b and LPF/decimator 4b and a parallel dotted-line path through controllable delay 6d and LPF/decimator 4d. Ex.1008, Fig.7, 4:18-27.



Id., Fig.7. Andersen explains that “at least one of the microphone channels has not only one delay device and one digital low pass filter and decimator filter but two of those in parallel,” and also discloses that more than two delay devices may be used in parallel in the same microphone channel. *Id.*, 4:18-27. Claim 11 likewise recites “at least one” microphone channel “equipped with a sigma-delta analog to digital converter including at least two delay devices in parallel operating on two digital low pass filters and decimators,” with the outputs of those parallel paths “being combined in a combination circuit connected to the [DSP].” *Id.*, claim 11. Thus, the first and second oversampled digital signals correspond to same-channel high-clock-frequency bit-stream signals derived from the same microphone/sensor before the parallel delay paths. Ex.1003, ¶384.

Combination circuit 9 combines downstream signals derived from the same-sensor high-clock-frequency bit streams through the respective delay and LPF/decimator paths. Ex.1008, 4:13-27, Fig.7, cl.11; Ex.1003, ¶389.

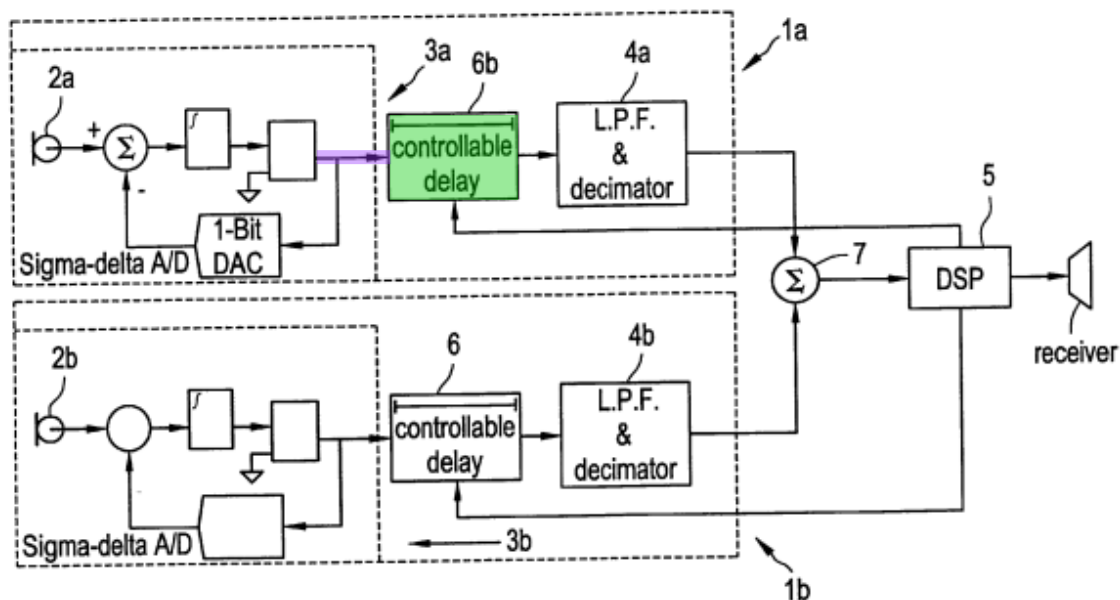
E. Claim 7

Andersen anticipates claim 7. Ex.1003, ¶¶390-393.

Andersen discloses that each microphone channel includes a “digital low pass filter and decimator” 4 that converts the high-clock-frequency one-bit stream into a sequence of digital words at a lower clock frequency, e.g., 16 or 32 kHz. Ex.1008, Abstract, 3:4-18. Thus, Andersen discloses applying a low-pass filter with decimation to the time-delayed first oversampled digital signal. Ex.1003, ¶391.

The output of Andersen’s low-pass filter/decimator is the claimed baseband digital signal delayed by the time delay. As explained for claim 4, the ’866 patent’s “baseband” discussion includes a receiver output at a baseband sampling rate, and the ’866 patent identifies 16 kHz as a baseband sampling frequency/rate. *Supra* §XV.B. Andersen likewise discloses that its LPF/decimator converts the delayed high-clock-frequency bit stream into lower-frequency digital words, including at 16 or 32 kHz. Ex.1008, 3:4-18, 3:30-38. Because the delay is imposed upstream of the LPF/decimator, the LPF/decimator processes the already-delayed bitstream, and its lower-rate/baseband digital output remains delayed by that same selected time delay. Ex.1003, ¶392.

Figure 4 illustrates this arrangement: in the upper channel, the first oversampled digital signal (purple) is delayed by controllable delay device 6b (green) before being provided to LPF/decimator 4a, which outputs the corresponding lower-rate/baseband digital signal for downstream processing and beamforming:



Ex.1008, Fig.4(annotated); Ex.1003, ¶¶392.

F. Claim 8

Andersen anticipates claim 8. Ex.1003, ¶¶394-396.

Andersen explains that conventional hearing-aid sampling intervals are “normally 32 usec,” but desired delays between microphone signals are “typically less than 32 usec,” e.g., 15 usec. Ex.1008, 1:20-25. To realize such delays, Andersen uses a sigma-delta converter clocked at 1 MHz or higher and a controllable digital delay line/tapped shift register in the bit stream, providing delays as short as

1 usec and “delayed difference steps of multiples of 1 usec.” *Id.*, 1:50-56; *see also id.*, 2:21-25 (realizing “delays as short as 1 usec”).

That disclosure concerns the delay itself, not merely its resolution: Andersen states that the “resulting delay” equals the number of delay stages times the inverse sampling rate, so one 1-MHz delay stage yields an actual 1-usec delay. *Id.*, 3:30-38; Ex.1003, ¶396. Andersen’s LPF/decimator converts the high-clock-frequency bit stream into lower-frequency/baseband digital word sequences at, e.g., 16 or 32 kHz. Ex.1008, 3:4-16. Those lower-frequency/baseband output rates correspond to baseband sampling periods of 31.25 usec and 62.5 usec, respectively. *Id.*; *see id.*, 1:20-25. Andersen’s disclosed 1- and 15-usec delays are therefore fractions of a baseband sampling period. Ex.1003, ¶396.

G. Claim 11

1. 11[pre]

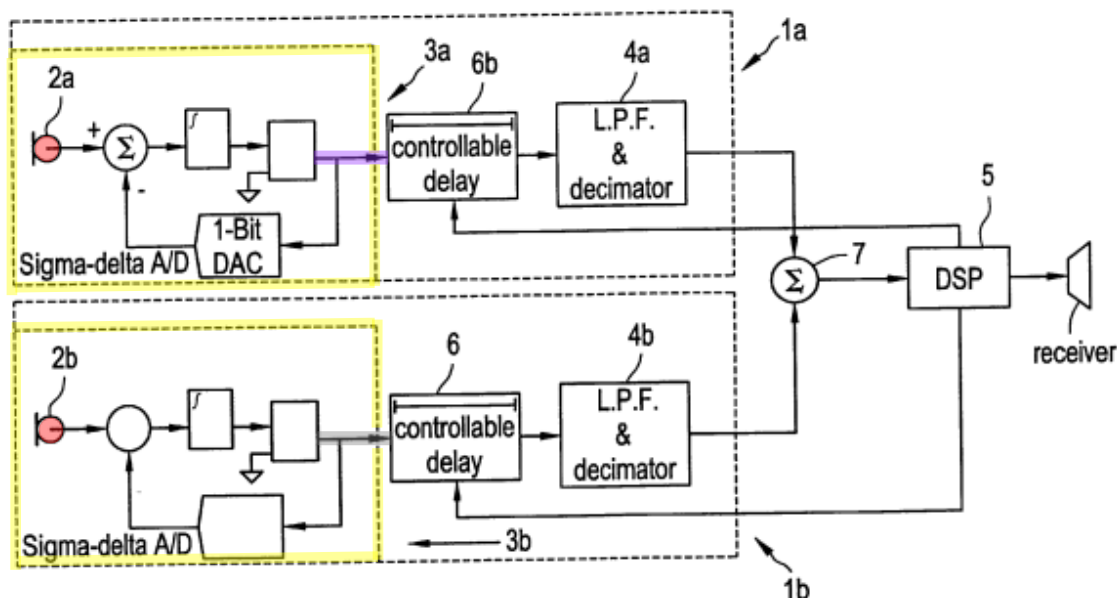
To the extent limiting, Andersen discloses 11[pre]. Ex.1003, ¶397. Andersen discloses a “hearing aid with beam forming properties” having “at least two microphone channels.” Ex.1008, Abstract. In Andersen’s Figure 4, the microphone-channel output signals “are combined in a summing circuit 7 and passed on to the DSP,” and the DSP controls delay to “direct the beam in the desired directions.” *Id.*, 3:42-45, 3:57-59, Fig.4.

2. 11[a]-11[b]

Andersen discloses 11[a]-11[b]. Ex.1003, ¶¶398-402.

For this claim-11 mapping, Petitioners map Andersen’s upper-channel microphone 2a and sigma-delta ADC 3a to the claimed first digital sensor, and Andersen’s lower-channel microphone 2b and sigma-delta ADC 3b to the claimed second digital sensor. Ex.1008, Fig.4; Ex.1003, ¶400.

Andersen discloses “at least two microphone channels (1a, 1b)” for “at least two microphones (2a, 2b),” with each channel containing a sigma-delta analog-to-digital converter. Ex.1008, Abstract, 3:25-29, 3:46-51. Andersen’s microphones (red) receive acoustic signals, and each sigma-delta ADC (yellow) outputs a “1 Bit stream of a high clock frequency” (purple/gray). *Id.*, Abstract.



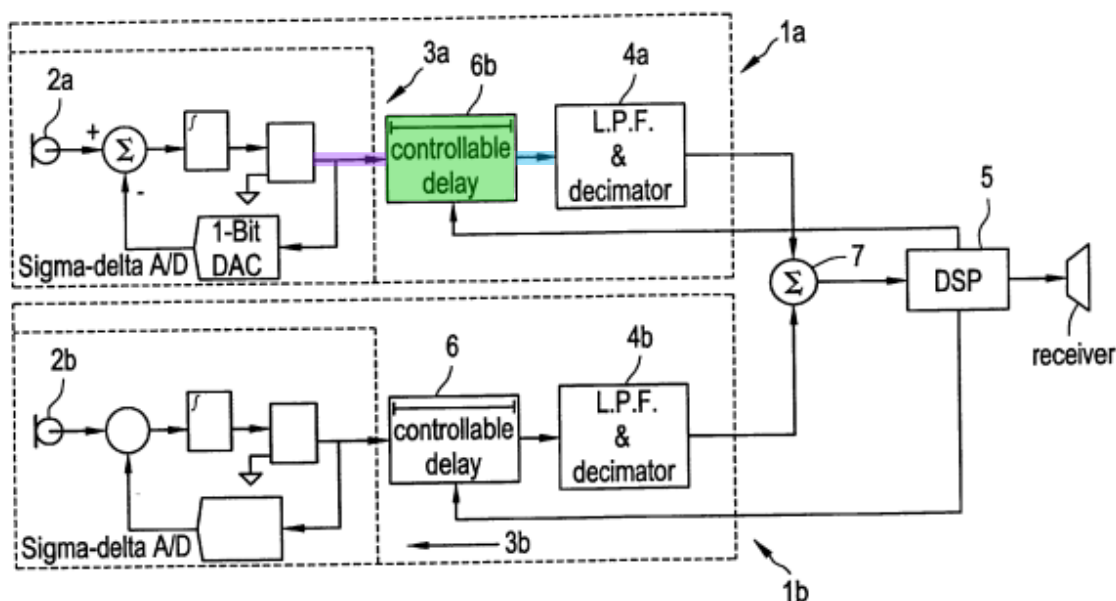
Id., Fig.4(annotated). Thus, Andersen’s upper- and lower-channel microphone/ADCs are first and second digital sensors responsive to the analog

acoustic field and configured to output first and second oversampled digital output signals at the sampling clock frequency. Ex.1003, ¶¶401-402.

3. 11[c]

Andersen discloses 11[c]. Ex.1003, ¶403.

Andersen places controllable delay device (green) on that first-channel bit-stream path before digital low-pass filter/decimator 4a:

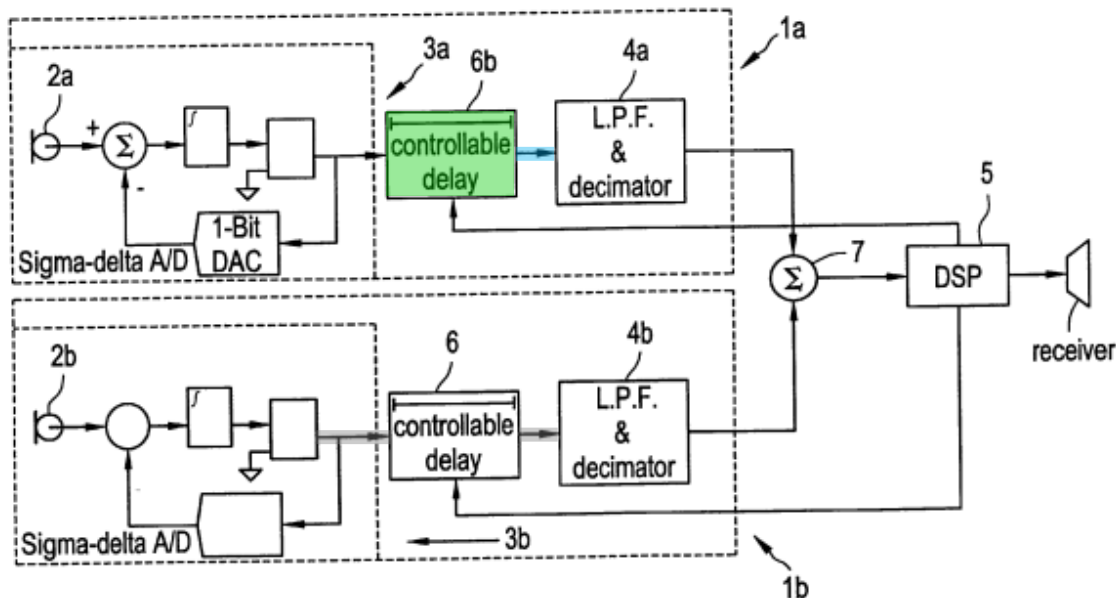


Ex.1008, Fig.4(annotated). Andersen explains that the delay device is typically a tapped shift register and that DSP 5 determines how many one-bit stages each bit-stream sample passes through “and thus be delayed by” before being sent to the LPF/decimator; in the annotated figure, purple identifies the delay-device input and blue the delayed output to LPF/decimator 4a. *See id.*, 3:30-38, 3:46-51.

4. 11[d]

Andersen discloses 11[d]. Ex.1003, ¶¶404-406.

Regarding Figure 4, Andersen discloses controllable delay devices in both microphone channels that “can...be controlled independently and separately,” and further explains that “only one of the two may be controlled whereas the other is switched off.” Ex.1008, 3:52-56; *see also id.*, 1:18-20, 3:39-51.

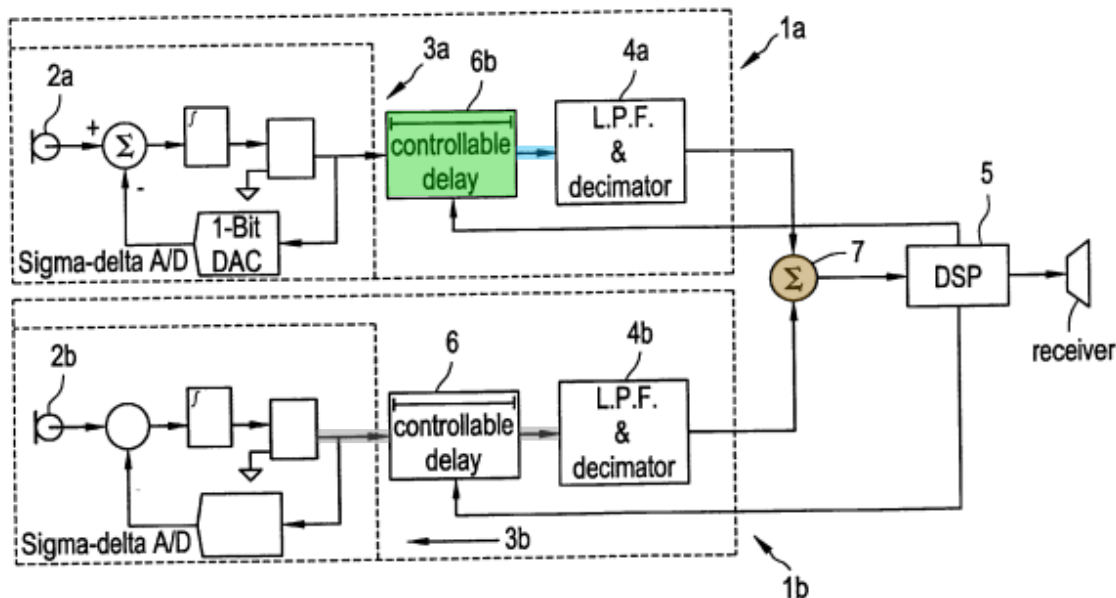


Id., Fig.4(annotated). In this figure, blue identifies the time-delayed first-channel bit stream, gray identifies the same second-channel stream used as the reference/no-delay signal, and green identifies the first-channel time delay element that imparts the relative delay between them. Ex.1003, ¶406. Thus, the time-delayed oversampled digital output signal and the second oversampled digital output signal are separated by the time delay imparted by the time delay element. *Id.*; *see also* Ex.1008, Fig.3.

5. 11[e]

Andersen discloses 11[e]. Ex.1003, ¶¶407-409.

Andersen's Figure 4 summing circuit 7 is an arithmetic unit. *Id.*, ¶407. Andersen's first-channel stream is delayed, the second-channel stream is used as the reference/no-delay stream, and the corresponding channel signals are provided to summing circuit 7 (tan). Ex.1008, Fig.4; *supra* §XV.G.4.



Ex.1008, Fig.4(annotated). Andersen explains that “[t]he output signals of the digital low pass filter and decimator filters 4a and 4b are combined in a summing circuit 7 and passed on to the DSP,” and that the DSP controls delay to “direct the beam in the desired directions.” *Id.*, 3:42-45, 3:57-59. Thus, to the extent 11[e] encompasses receipt of channel signals derived from the time-delayed first oversampled digital output signal and the second oversampled digital output signal after intervening channel processing, Andersen discloses the claimed arithmetic unit producing the beamformed digital signal. Ex.1003, ¶408.

Thus, Andersen anticipates claim 11. *Id.*, ¶¶397-409.

H. Claim 12

Andersen anticipates claim 12 for the reasons explained for 11[e] under the claim-11 mapping. *Supra* §XV.G.5; Ex.1003, ¶410.

I. Claim 13

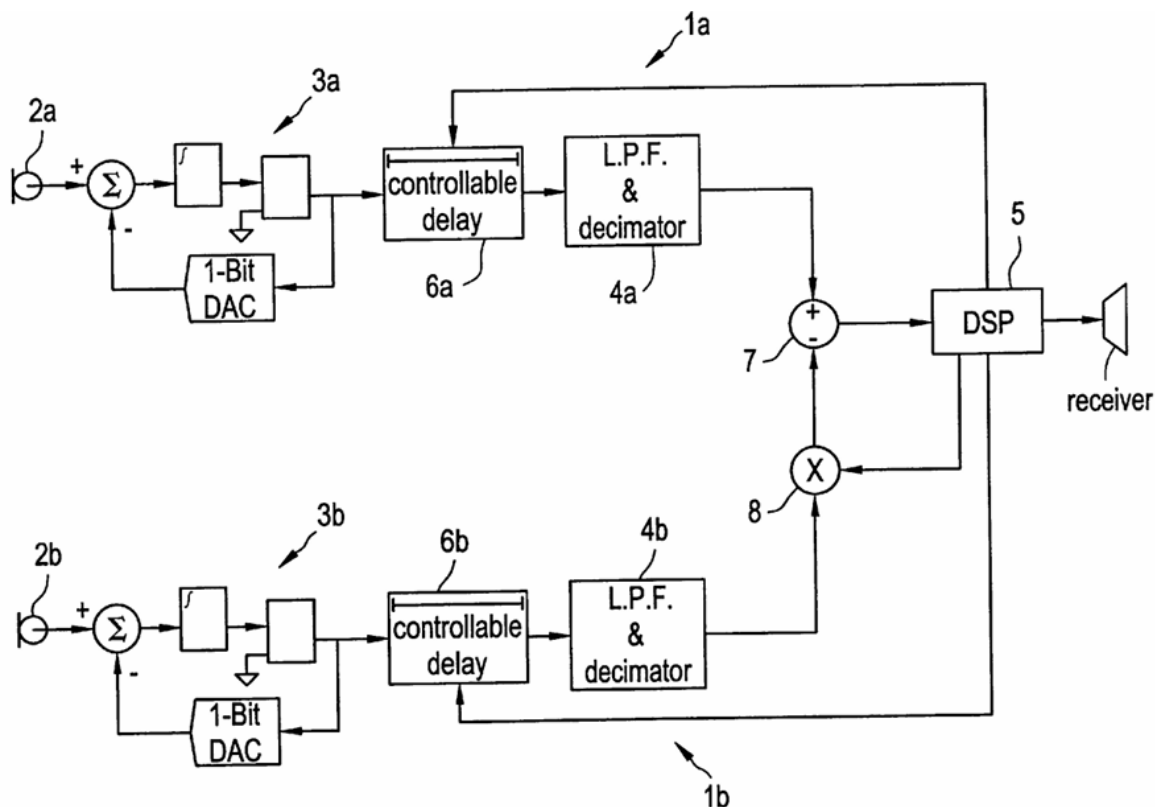
Andersen anticipates claim 13. Ex.1003, ¶¶411-413.

Andersen discloses using a summation function: Figure 4 identifies circuit 7 with the summation symbol (Σ), and Andersen describes circuit 7 as a “summing circuit” in which the first- and second-channel outputs are combined. Ex.1008, Fig.4, 3:57-59. Andersen also confirms that the two microphone signals may be “added and not subtracted from each other.” *Id.*, 2:55-59.

J. Claim 14

Andersen anticipates claim 14. Ex.1003, ¶¶414-416.

Andersen’s Figure 5 shows summing circuit 7 with positive and negative inputs. Ex.1008, Fig.5. Figure 5 is “similar to FIG. 4,” but connects the lower microphone-channel output through multiplier stage 8, whose output is applied to summing circuit 7. *Id.*, 3:63-4:3.



Id., Fig.5. Andersen explains that DSP 5 can multiply samples by factors “between -1 and $+1$.” *Id.*, 4:8-9. Applying one channel, or a scaled version of that channel, to the negative input of summing circuit 7 subtracts that channel from the other channel. Ex.1003, ¶¶415-416. Andersen confirms that addition/subtraction were known alternatives by describing a case where “the two microphone signals are added and not subtracted from each other.” Ex.1008, 2:55-59.

K. Claim 15

Andersen anticipates claim 15. Ex.1003, ¶¶417-420.

Andersen discloses that each microphone channel contains a “sigma-delta-type analog to digital converter” and that the sigma-delta ADC operates at a high

clock frequency, e.g., “1 MHz or higher,” to produce a “1 Bit stream of a high clock frequency.” Ex.1008, Abstract, 3:4-22, cls.1, 5.

Andersen’s sigma-delta ADC includes the claimed sigma-delta modulator, and its high-clock-frequency one-bit stream is a PDM output signal at the sampling clock frequency. Ex.1003, ¶420; *see also* Ex.1027, Abstract, 1:6-23. That PDM output is responsive to the analog field because it is generated from sound received by Andersen’s microphone 2a. Ex.1003, ¶420.

L. Claim 16

1. 16[pre]

Andersen discloses 16[pre] for the reasons explained for 11[pre]. *Supra* §XV.G.1; Ex.1003, ¶421.

2. 16[a]

Andersen discloses 16[a] for the reasons explained for 11[a]. *Supra* §XV.G.2; Ex.1003, ¶422.

3. 16[b]

Andersen discloses 16[b] for the reasons explained for 11[c]. *Supra* §XV.G.3; Ex.1003, ¶423.

4. 16[c]

Andersen discloses 16[c] for the reasons explained for 11[d]. *Supra* §XV.G.4; Ex.1003, ¶424.

5. 16[d]

Andersen discloses 16[d] for the reasons explained for 11[e], 1[c], and 11[a]-11[b]. *Supra* §§XV.G.5, XV.A.4, XV.G.2; Ex.1003, ¶425. As explained for 1[c] and 11[a]-11[b] specifically, the lower-channel stream—the claimed second oversampled digital output signal—is responsive to the analog field because it is generated from sound received by Andersen’s second microphone 2b and output by sigma-delta ADC 3b. Ex.1003, ¶425.

Thus, Andersen anticipates claim 16. *Id.*, ¶¶421-426.

M. Claim 17

Andersen anticipates claim 17 for the reasons discussed for claims 12 and 16. *Supra* §§XV.H, XV.L; Ex.1003, ¶427.

N. Claim 18

Andersen anticipates claim 18 for the reasons discussed for claims 13 and 16. *Supra* §§XV.I, XV.L; Ex.1003, ¶428.

O. Claim 19

Andersen anticipates claim 19 for the reasons discussed for claims 14 and 16. *Supra* §§XV.J, XV.L; Ex.1003, ¶429.

P. Claim 20

Andersen anticipates claim 20 for the reasons discussed for claims 15-16. *Supra* §§XV.K-L; Ex.1003, ¶430.

XVI. GROUND 7B: CLAIMS 1-2, 5-6, 9, AND 11-20 ARE OBVIOUS BASED ON ANDERSEN

A. Claim 1

As explained in Ground 7A, Andersen anticipates claim 1. *Supra* §XV.A. To the extent PO argues that Andersen's post-LPF/decimator summing does not satisfy 1[c], Andersen nevertheless renders claim 1 obvious. Ex.1003, ¶¶431-433.

A POSA would have been motivated to combine the delayed first-channel high-rate bit stream with the second-channel high-rate bit stream before a common downstream low-pass filter/decimator. *Id.*, ¶432. Andersen already provides both high-rate streams at the inputs to the per-channel low-pass filters/decimators, already delays the first stream at that high rate, and already combines the channel signals for beamforming. Ex.1008, 3:30-45, 3:52-59, Fig.4; Ex.1003, ¶432. Using one downstream filter/decimator for the combined beam signal would have predictably reduced duplicate per-channel filtering while preserving Andersen's fine high-rate delay control. Ex.1003, ¶433.

In that arrangement, the delayed first oversampled digital signal is combined with the second oversampled digital signal to obtain a beamformed digital signal, which is then low-pass filtered/decimated for downstream DSP processing. *Id.* A POSA would have had a reasonable expectation of success because the arrangement uses Andersen's known delay, summing, and filtering/decimation functions for the same purposes disclosed in Andersen. *Id.*

B. Claim 2

Andersen renders obvious claim 2. Ex.1003, ¶¶434-436.

Under the 1[c] arrangement described in this ground, the delayed first-channel high-rate bit stream is combined with the second-channel high-rate bit stream before a common downstream low-pass filter/decimator (*supra* §XVI.A), so the combining is performed in an oversampled signal domain. Ex.1003, ¶435.

C. Claims 5-6

Andersen renders claims 5-6 obvious for the reasons explained for claims 5-6 in Ground 7A. *Supra* §§XV.C-D; Ex.1003, ¶437. The claim-1 modification addressed in this ground (*supra* §XVI.A) does not affect Andersen’s disclosures of the additional limitations of claims 5-6. Ex.1003, ¶437.

D. Claim 9

As explained in Ground 7A, Andersen anticipates claim 7. *Supra* §XV.E. Andersen further renders claim 9 obvious. Ex.1003, ¶¶438-445.

Andersen explains that its controllable delay device is typically a multiple-tap shift register, and that the DSP determines the number of shift register stages the one-bit sigma-delta output samples traverse. Ex.1008, 3:31-36. Andersen further explains that, with a sigma-delta analog-to-digital converter clocked at “f.i. 1 MHz,” the system provides “delayed difference steps of multiple of 1 usec,” and that “[t]he resulting delay is equal to the number of stages times the inverse sampling rate.” *Id.*,

1:50-56, 3:36-38. Thus, Andersen’s programmable delay is selectable in 1-usec increments. Ex.1003, ¶440.

Andersen also discloses that its digital low-pass filter/decimator operates at a lower clock frequency, including “10 to 50 kHz,” and in one example converts the one-bit stream into digital words at “f.i. 16 or 32 kHz.” Ex.1008, 2:17-25, 3:12-18. These lower-rate/baseband outputs correspond to baseband sampling periods of 20 usec at 50 kHz, 31.25 usec at 32 kHz, and 62.5 usec at 16 kHz. Ex.1003, ¶441; *see also* Ex.1008, 1:20-29, 3:36-38.

Because Andersen’s DSP-controlled delay line selects the number of high-rate shift-register stages used to impose delay, selecting more than the corresponding number of 1-usec stages imposes a delay greater than a baseband sampling period—e.g., more than 20 stages for a 50 kHz baseband output or more than 32 stages for a 32 kHz output. Ex.1003, ¶442. A POSA would have been motivated to select such a number of stages when needed to achieve Andersen’s desired beamforming delay/directional orientation, because Andersen’s delay line is specifically provided so the DSP can actively control beam direction using the high-rate bitstream delay before low-pass filtering/decimation. *Id.*, ¶443; *see* Ex.1008, 1:40-57, 3:30-45. Implementing the selected delay in Andersen’s existing high-rate delay line also would avoid needing a separate downstream integer-delay element or moving the decimator upstream of the delay. Ex.1003, ¶443.

E. Claim 11

As explained in Ground 7A, Andersen anticipates claim 11. *Supra* §XV.G. To the extent 11[e] requires the arithmetic unit to receive the recited oversampled digital output signals before LPF/decimator processing, Andersen nevertheless renders claim 11 obvious. Ex.1003, ¶446. For the reasons explained for 1[c] in this ground, a POSA would have been motivated to combine the delayed first-channel high-rate bit stream with the second-channel high-rate bit stream before a common downstream LPF/decimator. *Supra* §XVI.A.

Andersen already provides those high-rate streams before the per-channel LPF/decimators, already delays the first stream at that high rate, and already combines the channel signals for beamforming. *See* Ex.1008, 3:30-45, 3:52-59, Fig.4. That implementation would preserve Andersen's fine high-rate delay control while reducing duplicate per-channel filtering/decimation, with a reasonable expectation of success because it uses Andersen's disclosed delay, summing, filtering, and decimation functions for their same purposes. Ex.1003, ¶446. In that implementation, summing circuit 7 receives the time-delayed oversampled digital output signal and the second oversampled digital output signal and produces the beamformed digital signal. *Id.*

F. Claim 12

Andersen renders claim 12 obvious to the extent PO argues that claim 12 requires the arithmetic unit to combine the recited oversampled digital output signals before LPF/decimator processing. Ex.1003, ¶447. In the modified configuration described for 11[e] in this ground, summing circuit 7 combines those signals before the common downstream LPF/decimator. *Supra* §XVI.E; Ex.1003, ¶447.

G. Claims 13-15

Andersen renders claims 13-15 obvious for the reasons explained for claims 13-15 in Ground 7A. *Supra* §§XV.I-K; Ex.1003, ¶448. The modification discussed for claims 11-12 in this ground (*supra* §§XVI.E-F) does not affect Andersen's disclosures of the additional limitations of claims 13-15. Ex.1003, ¶448.

H. Claim 16

As explained in Ground 7A, Andersen anticipates claim 16. *Supra* §XV.L. To the extent 16[d] requires the arithmetic unit to receive the oversampled digital output signals before LPF/decimator processing, Andersen nevertheless renders claim 16 obvious. Ex.1003, ¶449. In the modified configuration described for 1[c] and 11[e] in this ground, summing circuit 7 receives those signals before the common downstream LPF/decimator; Ground 7A further establishes that the second-channel stream is responsive to the analog field. *Supra* §§XVI.A, XVI.E, XV.L.5; Ex.1003, ¶449.

I. Claims 17-20

Andersen renders claims 17-20 obvious. Ex.1003, ¶450. The modified configuration described for claim 16 does not affect Andersen’s disclosures of the additional limitations of claims 17-20 in Ground 7A. *Supra* §§XVI.H, XV.M-P; Ex.1003, ¶450.

XVII. GROUND 8: CLAIM 3 IS OBVIOUS BASED ON ANDERSEN AND LIU

As explained in Ground 7A, Andersen anticipates claim 1. *Supra* §XV.A. Andersen and Liu further render obvious claim 3. Ex.1003, ¶¶451-474.

As explained for claim 3 in Ground 5A, Liu discloses staged reconstruction/decimation: filter 18 partially reconstructs/decimates delayed channel samples to a rate below the initial oversampling-converter rate but above the post-summation rate, so summation occurs at an intermediate sampling rate. *Supra* §XII.C. It would have been obvious to apply that approach to Andersen’s architecture described in Ground 7A (*supra* §XV.A) by using LPF/decimators 4a/4b as first-stage partial reconstruction/decimation filters and a common post-summation low-pass/decimation stage—e.g., between summing circuit 7 and DSP 5 or within DSP 5—to complete reconstruction/decimation. Ex.1003, ¶471. Andersen’s summing circuit 7 would then combine delayed microphone-channel signals after partial decimation but before final decimation, at a rate below the sigma-delta converter clock rate and above the output/baseband rate. *Id.*

A POSA would have been motivated to obtain Liu's identified benefit: reducing the per-channel data rate before summation while avoiding the two less desirable extremes. *Id.*, ¶¶472-473. A POSA would have had a reasonable expectation of success because the modification uses Andersen's sigma-delta converters, delays, LPF/decimators, summing circuit, and DSP, with Liu's staged reconstruction arrangement; Andersen already outputs lower-rate digital words for DSP processing, and Liu discloses multi-bit summing followed by downstream reconstruction/decimation. *Id.*, ¶474; *see* Ex.1008, 3:12-18, 3:57-59; Ex.1007, [0038]-[0040], [0057].

XVIII. GROUND 9: CLAIM 9 IS OBVIOUS BASED ON ANDERSEN AND NOUJAIM

As explained in Ground 7B, Andersen renders claim 9 obvious. *Supra* §XVI.D. Andersen and Noujaim further render claim 9 obvious. Ex.1003, ¶¶475-489.

Andersen's LPF/decimator outputs lower-frequency/baseband digital word sequences, e.g., at 16 or 32 kHz, corresponding to baseband sampling periods of 62.5 usec and 31.25 usec. Ex.1008, 3:4-18; Ex.1003, ¶487.

Noujaim confirms that such oversampled beamformers used multi-stage high-rate delay registers before summation and later decimation. Ex.1003, ¶488. Noujaim discloses sigma-delta modulators that output one-bit digital signals, variable delay shift registers that delay those signals before summation, and a

decimator that later reduces the beam-data sample rate. Ex.1010, Abstract, 3:26-4:5, 8:65-9:42, 10:22-40. Noujaim’s delay registers are “80 stages in length,” and the desired time delay is selected based on the shift-register stage from which the signal is output. *Id.*, 9:22-42.

A POSA would have been motivated to apply Noujaim’s multi-stage high-rate delay-register teaching in Andersen’s architecture described in Ground 7A (*supra* §XV.A) to provide for situations when the desired beamforming delay exceeded the later lower-rate/baseband sampling period. Ex.1003, ¶489. Applying Noujaim’s delay-register teaching to Andersen’s 1 MHz sigma-delta bitstream would have predictably extended Andersen’s selectable delay range, such as up to 80 us in the case of an 80-stage delay-register, exceeding Andersen’s 31.25-usec and 62.5-usec sampling periods of Andersen’s 32-kHz and 16-kHz post-decimation digital-word outputs. *Id.*

A POSA would have had a reasonable expectation of success because both Andersen and Noujaim use oversampled/sigma-delta bitstream delay before later decimation, and increasing the number of high-rate delay stages merely extends the same known delay-line mechanism without changing its operation. *Id.*, ¶¶482-483.

XIX. GROUND 10: CLAIM 10 IS OBVIOUS BASED ON ANDERSEN AND DEAN

As explained in Ground 7A, Andersen anticipates claim 7. *Supra* §XV.E. Andersen and Dean further render claim 10 obvious. Ex.1003, ¶¶490-507.

As explained in Ground 3, Dean teaches implementing oversampled beamforming using n-bit digital signals at an oversampling rate, including samples more than one bit deep, with corresponding n-bit delay/shift-register, adder, and decimation structures. *Supra* §X.

It would have been obvious to implement Andersen's oversampled converter/delay path described in Ground 7A using Dean's multi-bit oversampled-output teaching so that Andersen's first oversampled digital signal is digitized into samples more than one bit deep. Ex.1003, ¶506. A POSA would have been motivated to do so because Andersen and Dean share the relevant sampled-signal features—oversampled digitization, digital delay/beamforming, and downstream decimation—and Dean's n-bit teaching concerns that architecture rather than any radar-specific front-end. *Id.* Although Dean's example application is radar and Andersen's is a hearing aid, a POSA would have understood the same bit-depth/oversampling-rate tradeoff to apply predictably to Andersen's acoustic beamformer, where greater per-sample amplitude information and usable dynamic range would have been desirable. Ex.1003, ¶¶506-507; *see* Ex.1008, 3:4-18, 3:30-38, 3:57-59; Ex.1009, 1:44-57, 6:18-40.

A POSA would have had a reasonable expectation of success because Dean teaches the multi-bit implementation details—n-bit oversampled outputs, n-bit shift-register elements, n-bit adders, and a decimating filter—while preserving

Andersen’s sequence of oversampling, high-rate delay, low-pass filtering/decimation, and combining. Ex.1003, ¶506; *see* Ex.1009, 6:18-40.

XX. GROUND 11: CLAIMS 11-20 ARE OBVIOUS BASED ON ANDERSEN AND MOQUIN

As explained in Ground 7A, Andersen anticipates claims 11-20 under the post-LPF/decimator interpretation. *Supra* §§XV.G-P. To the extent the arithmetic unit must receive/combine the recited oversampled digital output signals before LPF/decimator processing, Andersen and Moquin render claims 11-20 obvious. Ex.1003, ¶¶508-517.

Moquin’s Figure 3 shows per-channel filtering/decimation before beamformer 13, and Figure 4 places “the delay and sum beamformer 13...before the filter 23 and decimator 24.” Ex.1006, [0013]-[0014], Figs.3-4. In Figure 4, the single-bit delta-modulator outputs are delayed, “summed together,” and then presented to filter 23/decimator 24. *Id.*, [0014].

A POSA would have found it obvious to implement Andersen’s Figure 4 system described in Ground 7A (*supra* §XV.A) using Moquin’s ordering by combining Andersen’s delayed first-channel high-rate bit stream and second-channel high-rate bit stream before a common downstream LPF/decimator. Ex.1003, ¶¶511-512. That modification would preserve Andersen’s high-rate delay resolution, while applying Moquin’s known approach of summing the oversampled delayed streams before downstream filtering/decimation. *Id.*; Ex.1008, 1:40-57,

3:30-59; Ex.1006, [0014]. A POSA would have been motivated to do so because Moquin recognizes the implementation tradeoff: although operating “the summer and the delay lines” at the higher oversampling rate increases complexity, that complexity is offset by eliminating multiple filters or an even more complex delay-and-sum structure. Ex.1006, [0015]; Ex.1003, ¶512.

A POSA would have had a reasonable expectation of success because Andersen and Moquin both use oversampled sigma-delta microphone/sensor signals, high-rate delay, beamforming combination, and downstream filtering/decimation. Ex.1003, ¶513; Ex.1008, Abstract, 3:30-59; Ex.1006, [0014]-[0017]. The modification merely uses Moquin’s disclosed ordering of those same functions in Andersen’s analogous beamforming signal path. Ex.1003, ¶514.

XXI. SECONDARY CONSIDERATIONS

Petitioners are not aware of any evidence of secondary considerations. If PO identifies evidence of secondary considerations, Petitioners request an opportunity to respond. *See* Ex.1003, ¶518.

XXII. STIPULATION

Petitioners stipulate that, if *inter partes* review is instituted, Petitioners will not pursue in the Litigation, against any challenged claim of the ’866 patent: (1) any invalidity ground that was raised or reasonably could have been raised in this IPR; or (2) any invalidity ground under 35 U.S.C. §§ 102 or 103 that relies on any prior-

art reference asserted in Grounds 1-11 of the Petition, whether alone or with system art or other prior art unavailable in IPR. If institution is denied or later vacated, this stipulation has no effect.

XXIII. MANDATORY NOTICES, GROUNDS FOR STANDING, AND FEE PAYMENT

A. Real Parties-In-Interest (37 C.F.R. §42.8(b)(1))

The real parties in interest for Petitioners are: Luxottica of America Inc.; Oakley, Inc.; EssilorLuxottica USA Inc.; and Meta Platforms, Inc.

Luxottica of America Inc. further identifies the following entities without conceding that these entities are, in fact, real parties in interest: EssilorLuxottica America SAS; Luxottica Group SPA; Essilor International SAS; EssilorLuxottica S.A.; Luxottica SRL; Luxottica Tristar (Dongguan) Optical Co. Ltd.; and EssilorLuxottica (Thailand) Ltd.

Meta Platforms, Inc. further identifies the following entity without conceding that this entity is, in fact, a real party in interest: Meta Platforms Technologies, LLC (formerly known as Facebook Technologies, LLC, which was formerly known as Oculus VR, LLC).

B. Related Matters (37 C.F.R. §42.8(b)(2))

The parties are engaged in district court litigation in *Solos Technology Limited v. Meta Platforms, Inc. et al.*, No. 1:26-cv-10304 (D. Mass.). In that action, PO asserted the '866 patent and U.S. Pat. Nos. 10,306,389 (“the '389 patent”),

11,082,055 (“the ’055 patent”), 11,871,174 (“the ’174 patent”), and 12,216,339 (“the ’339 patent”). The ’055 patent claims priority to the ’866 patent. The ’339 patent is currently the subject of AIA Review No. IPR2026-00376. The ’174 patent is currently the subject of AIA Review No. IPR2026-00413. The ’055 patent is currently the subject of AIA Review Nos. IPR2026-00412 and IPR2026-00420.

C. Lead and Backup Counsel (37 C.F.R. §42.8(b)(3))

Petitioners provide the following designation of counsel.

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D. Service Information (37 C.F.R. §42.8(b)(4))

Please direct all correspondence to lead counsel and back-up counsel at the addresses shown above. Petitioners also consent to electronic service by email to:

MLB-Luxottica-IPR-866@morganlewis.com; and

PH-Meta-Solos-IPR@paulhastings.com.

E. Standing

The '866 patent is available for IPR, and no bar or estoppel applies.

The Office may charge any fees due to Deposit Account 50-0310.

XXIV. CONCLUSION

Petitioners request institution and cancellation of claims 1-20 of the '866 patent. *See* Ex.1003, ¶519.

Dated: September 29, 2026

By: /Jacob L. Peterson/

Jacob L. Peterson (Reg. No. 65,096)

MORGAN, LEWIS & BOCKIUS LLP

*Attorney for Petitioner,
Luxottica of America Inc.*

APPENDIX: LISTING OF CLAIMS FROM U.S. PATENT NO. 10,651,866

Claim 1

- 1[pre]** A method to create a beamformed digital signal, comprising:
- 1[a]** outputting a first oversampled digital signal output from an analog-to-digital converter (ADC), wherein the first oversampled digital signal is responsive to an analog field and the first oversampled digital signal is created at a sampling clock frequency;
- 1[b]** delaying the first oversampled digital signal by a time delay wherein the time delay is equal to an integer number of sampling clock cycles to produce a time delayed first oversampled digital signal; and
- 1[c]** combining the time delayed first oversampled digital signal with a second oversampled digital signal to obtain the beamformed digital signal, wherein the second oversampled digital signal is responsive to the analog field.

Claim 2

The method of claim 1, wherein the combining is performed in an oversampled signal domain.

Claim 3

The method of claim 1, wherein the combining is performed at an intermediate sampling rate.

Claim 4

The method of claim 1, wherein the combining is performed in a baseband signal domain.

Claim 5

The method of claim 1, wherein the first oversampled digital signal and the second oversampled digital signal are obtained from different sensors.

Claim 6

The method of claim 1, wherein the first oversampled digital signal and the second oversampled digital signal are obtained from the same sensor.

Claim 7

The method of claim 1, further comprising:

applying a low pass filter with decimation to the time delayed first oversampled digital signal to output a baseband digital signal that is delayed by the time delay.

Claim 8

The method of claim 7, wherein the time delay is equal to a fraction of a baseband sampling period.

Claim 9

The method of claim 7, wherein the time delay is greater than a baseband sampling period.

Claim 10

The method of claim 7, wherein the first oversampled digital signal is digitized to create samples which are more than one bit deep.

Claim 11

11[pre] A system to create a beamformed digital signal, comprising:

- 11[a]** a first digital sensor responsive to an analog field, the first digital sensor is configured to output a first oversampled digital output signal at a sampling clock frequency;
- 11[b]** a second digital sensor responsive to the analog field, the second digital sensor is configured to output a second oversampled digital output signal at the sampling clock frequency;
- 11[c]** a time delay element, the time delay element is configured to receive as an input, the first oversampled digital output signal and to output a time delayed oversampled digital output signal,
- 11[d]** wherein the time delayed oversampled digital output signal and the second oversampled digital output signal are separated by a time delay that is imparted by the time delay element; and
- 11[e]** an arithmetic unit, the arithmetic unit is configured to receive the time delayed oversampled digital output signal and the second oversampled digital output signal, the arithmetic unit is configured to produce the beamformed digital signal from the time delayed oversampled digital output signal and the second oversampled digital output signal.

Claim 12

The apparatus of claim 11, wherein the arithmetic unit combines the time delayed oversampled digital output signal and the second oversampled digital output signal.

Claim 13

The apparatus of claim 12, wherein the arithmetic unit combines the time delayed oversampled digital output signal and the second oversampled digital output signal using a summation function.

Claim 14

The apparatus of claim 12, wherein the arithmetic unit combines the time delayed oversampled digital output signal and the second oversampled digital output signal using a subtraction function.

Claim 15

The apparatus of claim 11, further comprising:

a sigma-delta modulator, the first digital sensor utilizes the sigma-delta modulator and the first digital sensor is configured to produce a pulse density modulated (PDM) output signal at the sampling clock frequency responsive to the analog field.

Claim 16

- 16[pre]** A system to create a beamformed digital signal, comprising:
- 16[a]** a digital sensor responsive to an analog field, the digital sensor is configured to output an oversampled digital output signal at a sampling clock frequency;
- 16[b]** a time delay element, the time delay element is configured to receive as an input, the oversampled digital output signal and to output a time delayed oversampled digital output signal,
- 16[c]** wherein the time delayed oversampled digital output signal and a second oversampled digital output signal are separated by a time delay and the time delay is imparted by the time delay element; and

16[d] an arithmetic unit, the arithmetic unit is configured to receive the time delayed oversampled digital output signal and the second oversampled digital output signal, wherein the second oversampled digital output signal is responsive to the analog field, the arithmetic unit is configured to produce the beamformed digital signal from the time delayed oversampled digital output signal and the second oversampled digital output signal.

Claim 17

The apparatus of claim 16, wherein the arithmetic unit combines the time delayed oversampled digital output signal and the second oversampled digital output signal.

Claim 18

The apparatus of claim 17, wherein the arithmetic unit combines the time delayed oversampled digital output signal and the second oversampled digital output signal using a summation function.

Claim 19

The apparatus of claim 17, wherein the arithmetic unit combines the time delayed oversampled digital output signal and the second oversampled digital output signal using a subtraction function.

Claim 20

The apparatus of claim 16, further comprising:

a sigma-delta modulator, the digital sensor utilizes the sigma-delta modulator and the digital sensor is configured to produce a pulse density modulated (PDM) output signal at the sampling clock frequency responsive to the analog field.

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. §42.24(d), the undersigned certifies that this PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,651,866 contains 13,994 words according to the word-processing program used to prepare this paper. The foregoing word count complies with the 14,000-word type-volume limit specified by 37 C.F.R. §42.24(a)(1).

Dated: September 29, 2026

By: /Jacob L. Peterson/

Jacob L. Peterson (Reg. No. 65,096)

MORGAN, LEWIS & BOCKIUS LLP

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on the date below copies of the **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,651,866, PETITIONERS’ POWER OF ATTORNEY, AND EXHIBITS 1001-1004, 1006-1023, AND 1026-1027** are being served by FedEx on the Patent Owner at the correspondence address of record for the subject patent as follows:

Caldwell LLC
200 Clarendon Street
59th Floor
Boston, MA 02116

A courtesy copy is being sent by email on this day to Patent Owner’s counsel of record in the Litigation as follows:

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