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Kabbani et al.

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(54) **WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING**

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G01R 31/28 (2006.01)
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H01L 23/473 (2006.01)

(52) **U.S. Cl.**
CPC .. ***G01R 31/2887*** (2013.01); ***G01R 31/318511*** (2013.01); ***H01L 23/473*** (2013.01); *F28F 2260/02* (2013.01)

(58) **Field of Classification Search**
CPC G01R 31/2887; G01R 31/318511; G01R 31/2874; G01R 31/2875; G01R 31/2877; G01R 31/2889
See application file for complete search history.

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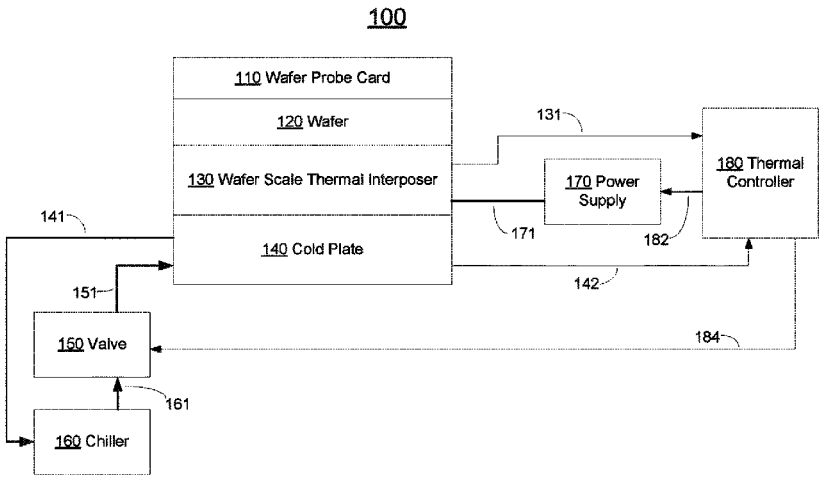
(57) **ABSTRACT**

A system for testing circuits of an integrated circuit semiconductor wafer includes a tester system for generating signals for input to the circuits and for processing output signals from the circuits for testing the wafer and a test stack coupled to the tester system. The test stack includes a wafer probe for contacting a first surface of the wafer and for probing individual circuits of the circuits of the wafer, a wafer thermal interposer (TI) layer operable to contact a second surface of the wafer and operable to selectively heat areas of the wafer, and a cold plate disposed under the wafer TI layer and operable to cool the wafer. The system further includes a thermal controller for selectively heating and maintaining temperatures of the areas of the wafer by controlling cooling of the cold plate and by controlling selective heating of the wafer TI layer.

27 Claims, 9 Drawing Sheets



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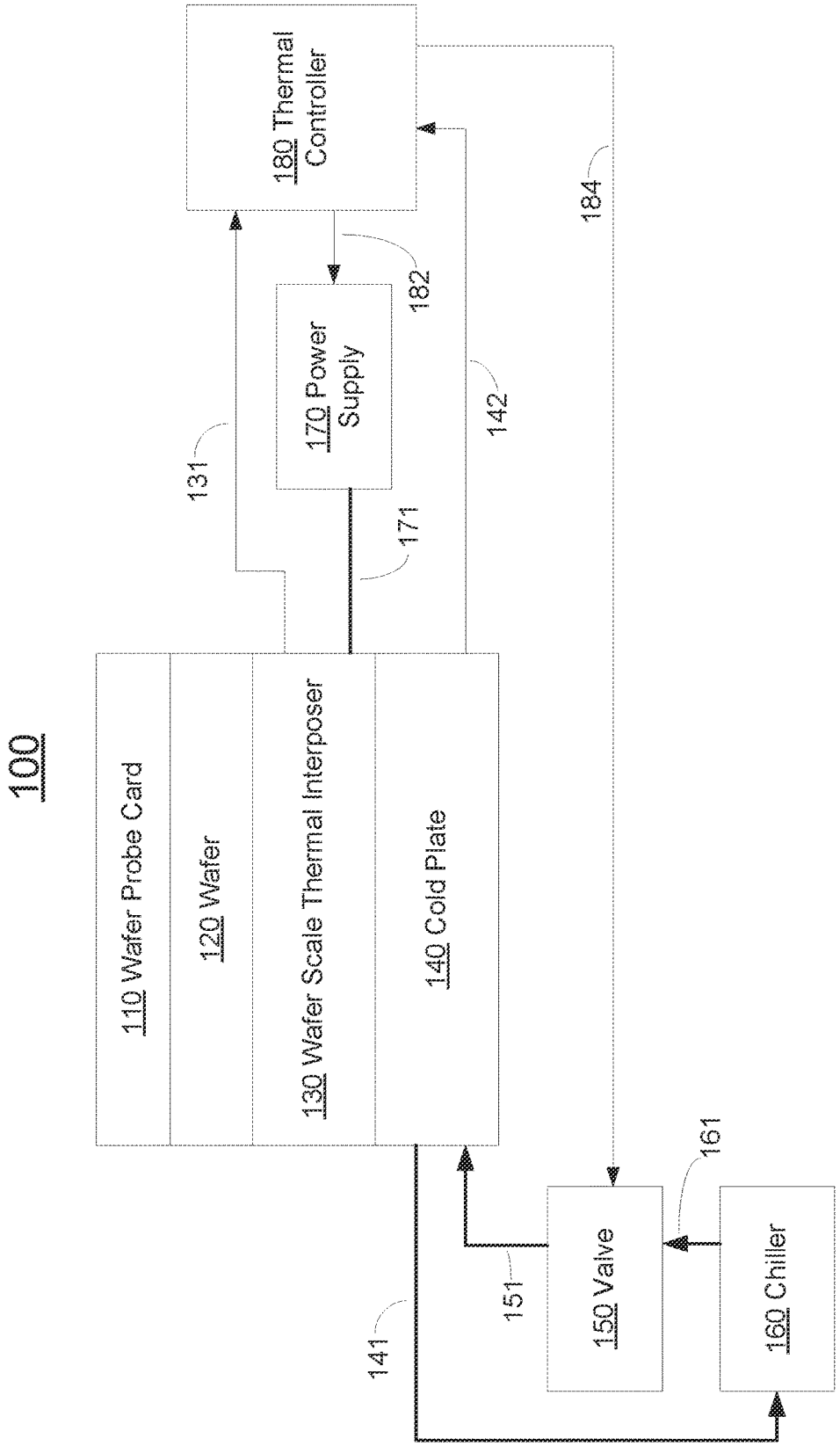

100
110 Wafer Probe Card
120 Wafer
130 Wafer Scale Thermal Interposer
140 Cold Plate
180 Thermal Controller
170 Power Supply
150 Valve
160 Chiller
131
141
142
151
161
171
182
184

Fig. 1

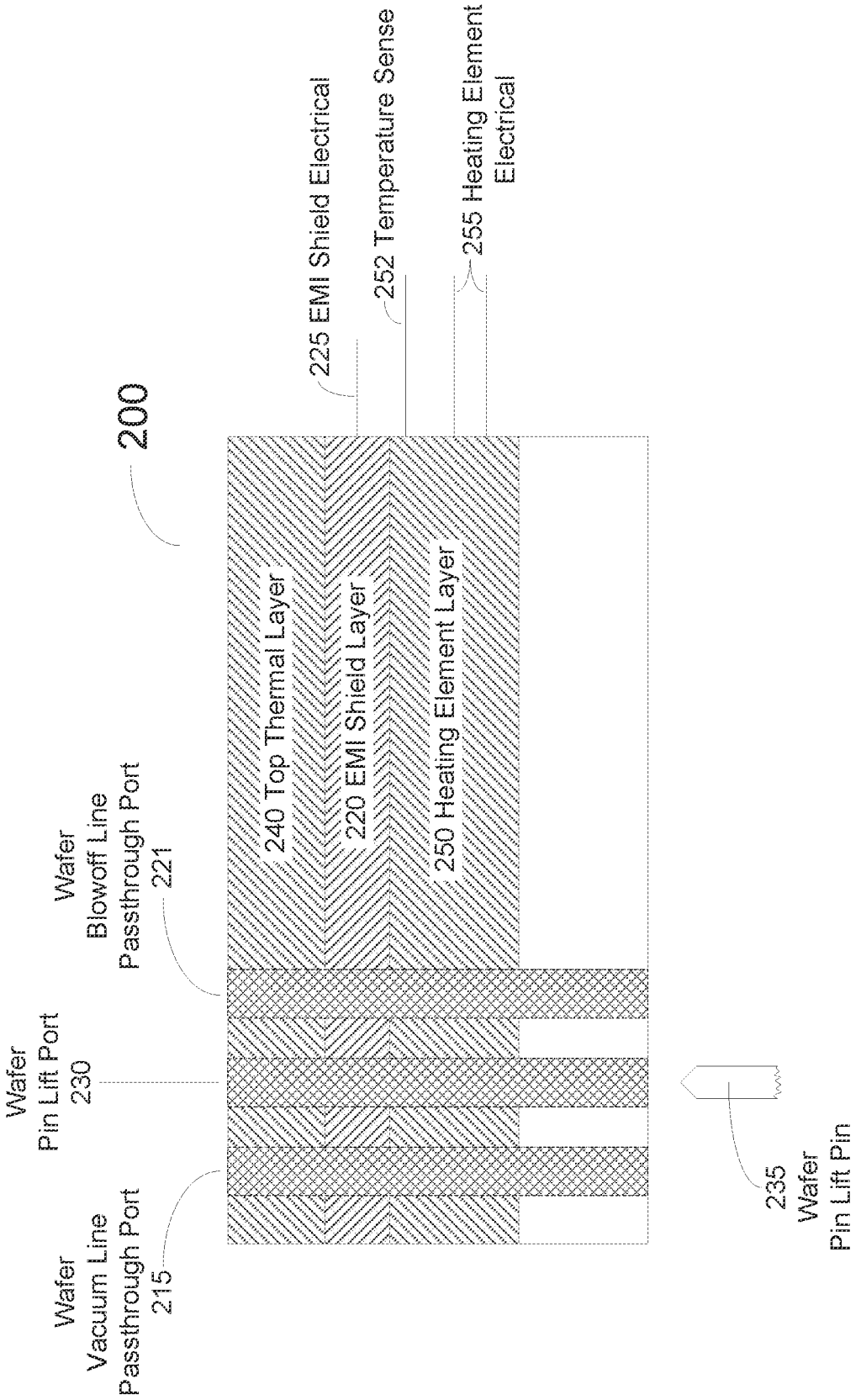

200
225 EMI Shield Electrical
252 Temperature Sense
255 Heating Element Electrical
240 Top Thermal Layer
220 EMI Shield Layer
250 Heating Element Layer
Wafer Bloweff Line Passthrough Port 221
Wafer Pin Lift Port 230
Wafer Vacuum Line Passthrough Port 215
235 Wafer Pin Lift Pin

Fig. 2

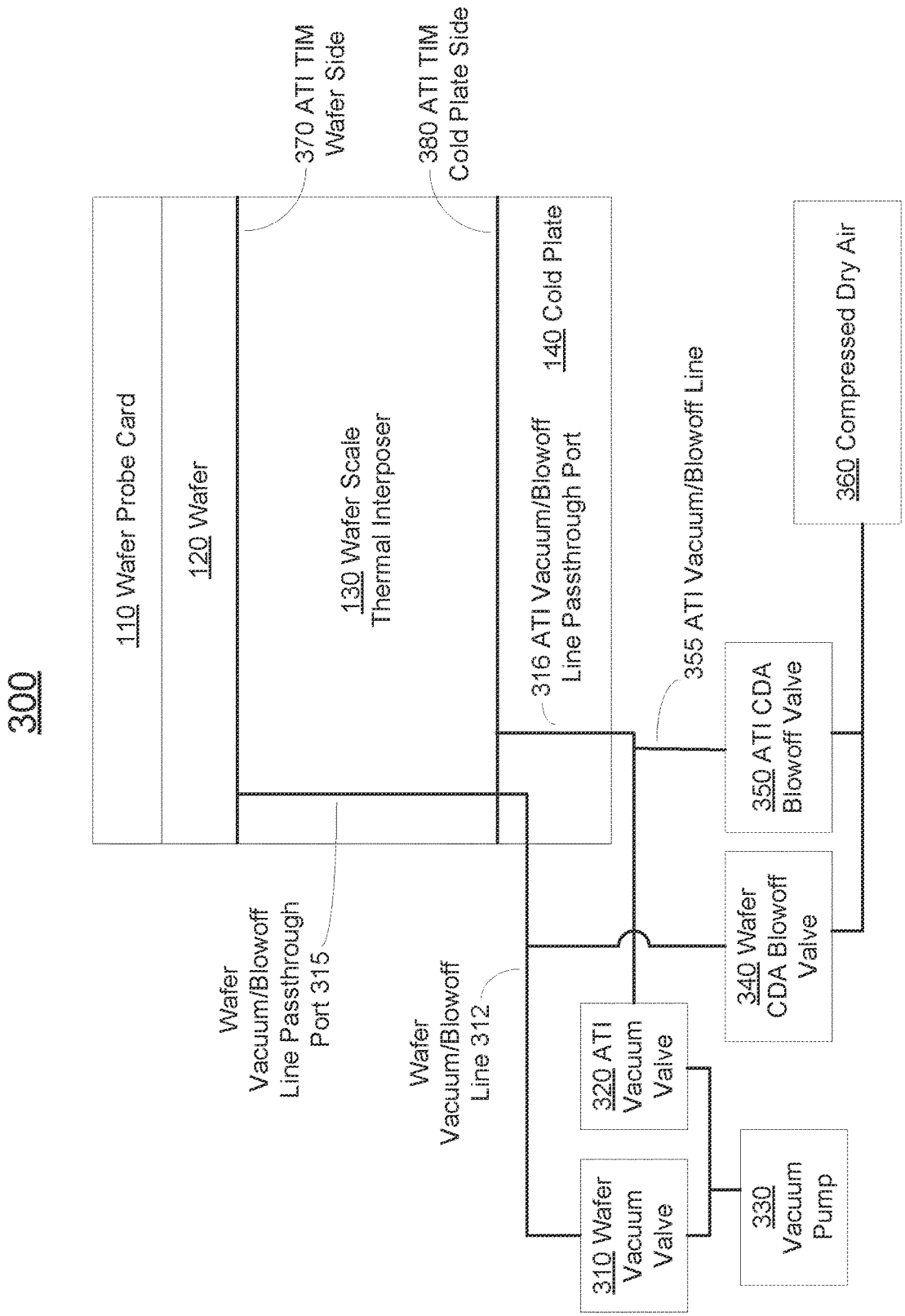
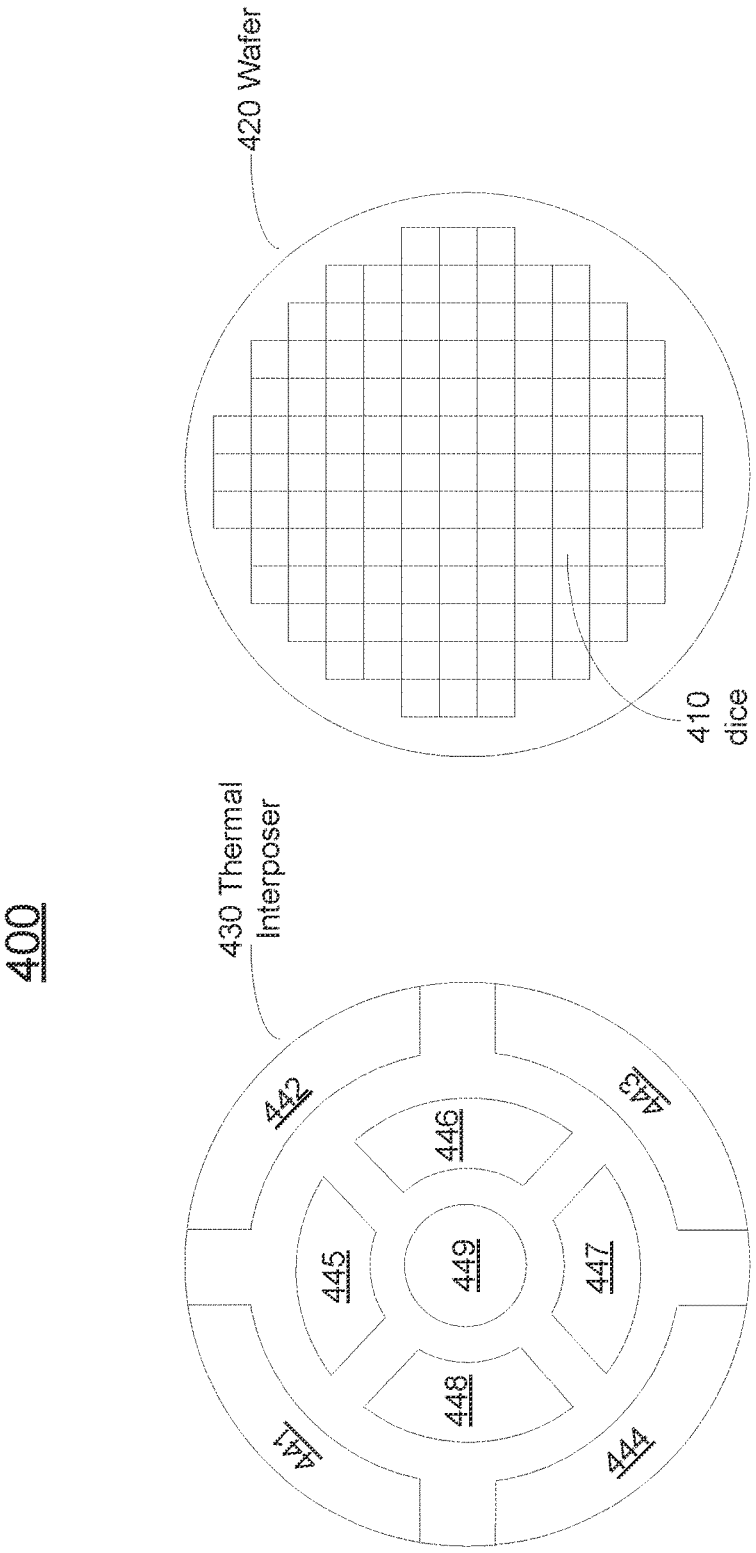

300
110 Wafer Probe Card
120 Wafer
130 Wafer Scale Thermal Interposer
370 ATI TIM Wafer Side
380 ATI TIM Cold Plate Side
140 Cold Plate
316 ATI Vacuum/Bloweff Line Passthrough Port
355 ATI Vacuum/Bloweff Line
360 Compressed Dry Air
350 ATI CDA Bloweff Valve
340 Wafer CDA Bloweff Valve
Wafer Vacuum/Bloweff Line Passthrough Port 315
Wafer Vacuum/Bloweff Line 312
320 ATI Vacuum Valve
310 Wafer Vacuum Valve
330 Vacuum Pump

Fig. 3


400
420 Wafer
410 dice
430 Thermal Interposer
442
443
441
444
445
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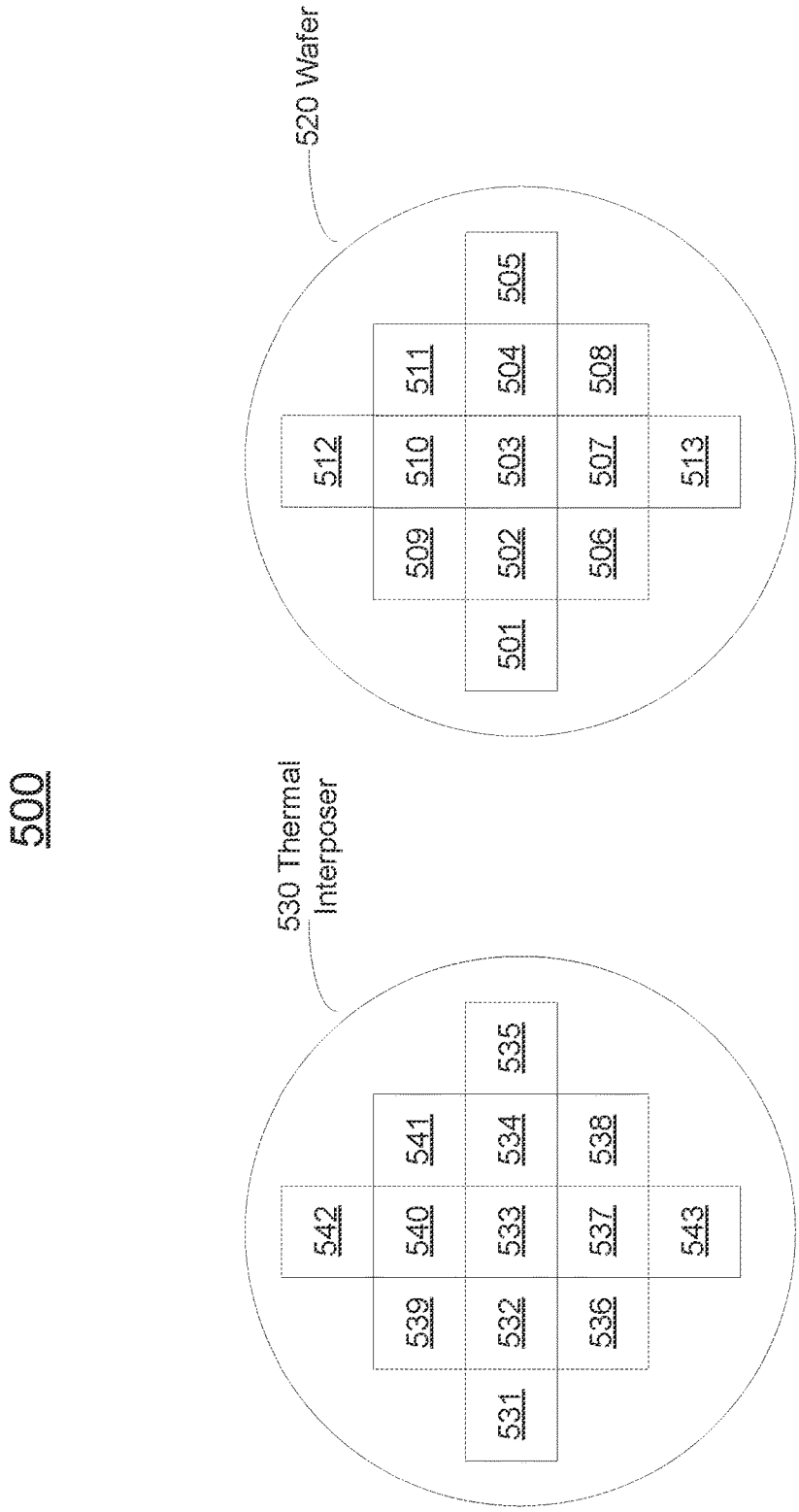
449

Fig. 4


500
520 Wafer
505
511
504
508
512
510
503
507
513
509
502
506
501
530 Thermal Interposer
535
541
534
538
542
540
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539
532
536
531

Fig. 5

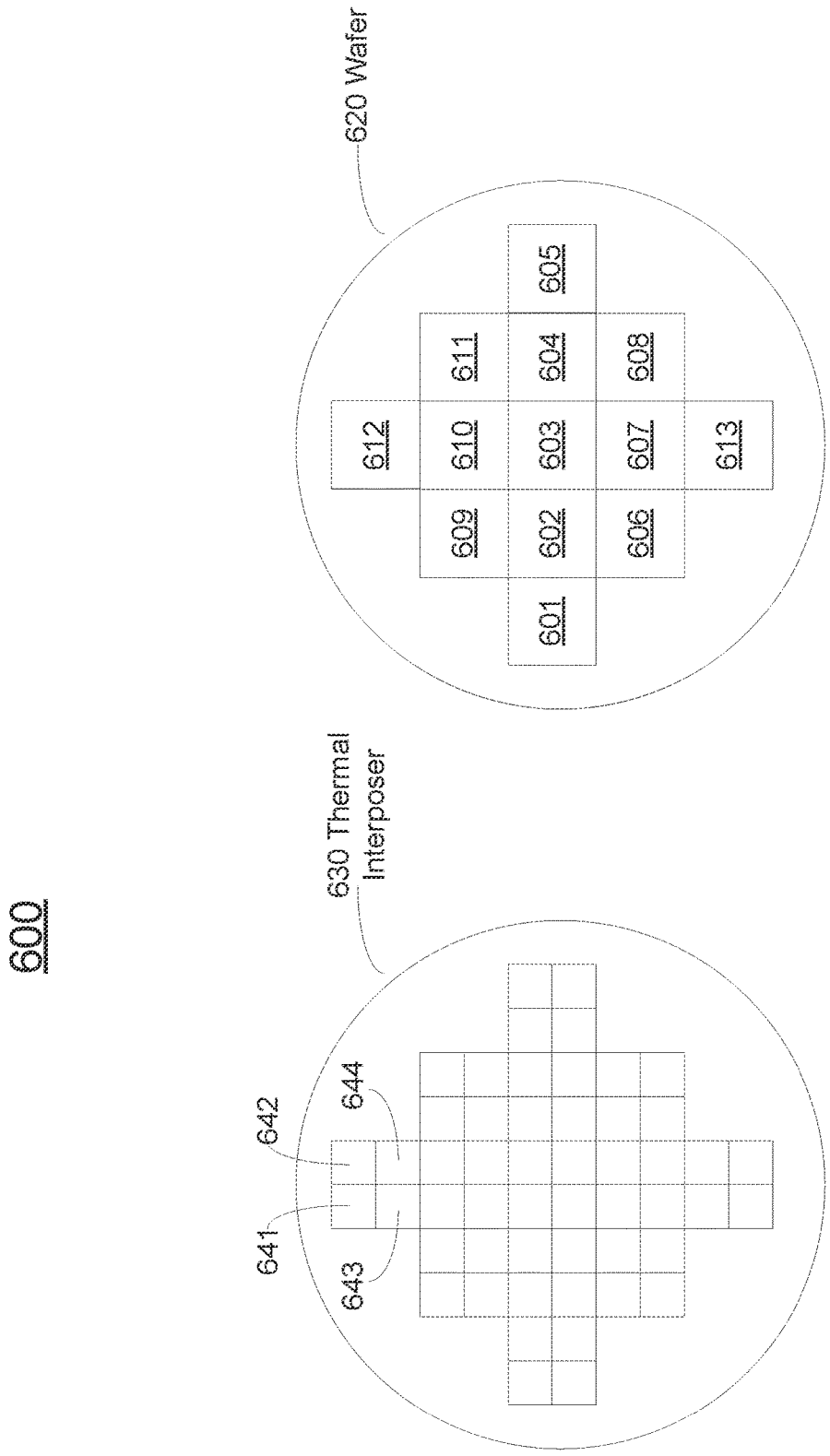
600
620 Wafer
605
611
604
608
612
610
603
607
613
609
602
606
601
630 Thermal Interposer
642
644
641
643

Fig. 6

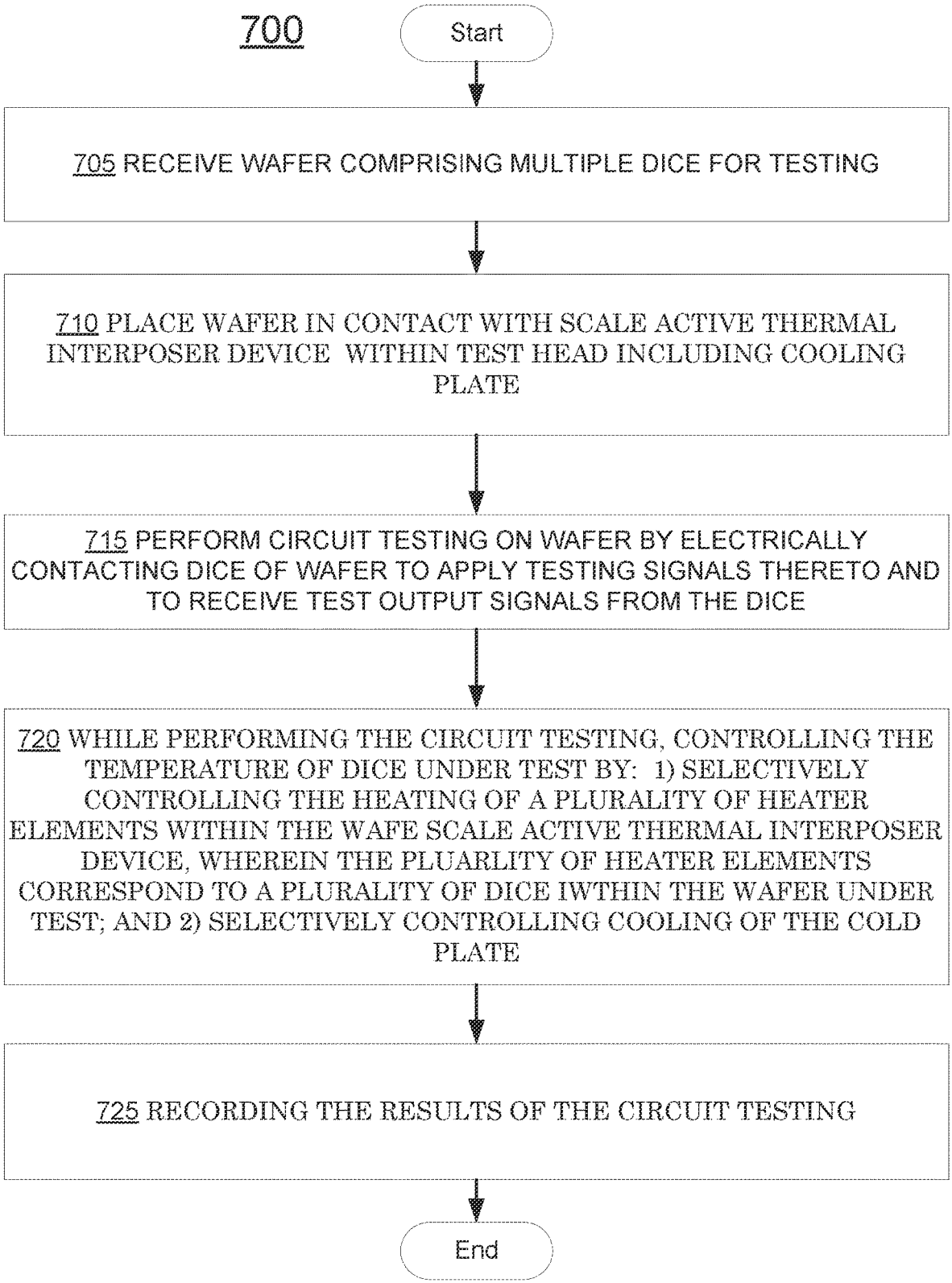
700
Start
705 RECEIVE WAFER COMPRISING MULTIPLE DICE FOR TESTING
710 PLACE WAFER IN CONTACT WITH SCALE ACTIVE THERMAL INTERPOSER DEVICE WITHIN TEST HEAD INCLUDING COOLING PLATE
715 PERFORM CIRCUIT TESTING ON WAFER BY ELECTRICALLY CONTACTING DICE OF WAFER TO APPLY TESTING SIGNALS THERETO AND TO RECEIVE TEST OUTPUT SIGNALS FROM THE DICE
720 WHILE PERFORMING THE CIRCUIT TESTING, CONTROLLING THE TEMPERATURE OF DICE UNDER TEST BY: 1) SELECTIVELY CONTROLLING THE HEATING OF A PLURALITY OF HEATER ELEMENTS WITHIN THE WAFE SCALE ACTIVE THERMAL INTERPOSER DEVICE, WHEREIN THE PLUARLITY OF HEATER ELEMENTS CORRESPOND TO A PLURALITY OF DICE IWTHIN THE WAFER UNDER TEST; AND 2) SELECTIVELY CONTROLLING COOLING OF THE COLD PLATE
725 RECORDING THE RESULTS OF THE CIRCUIT TESTING
End

Fig. 7A

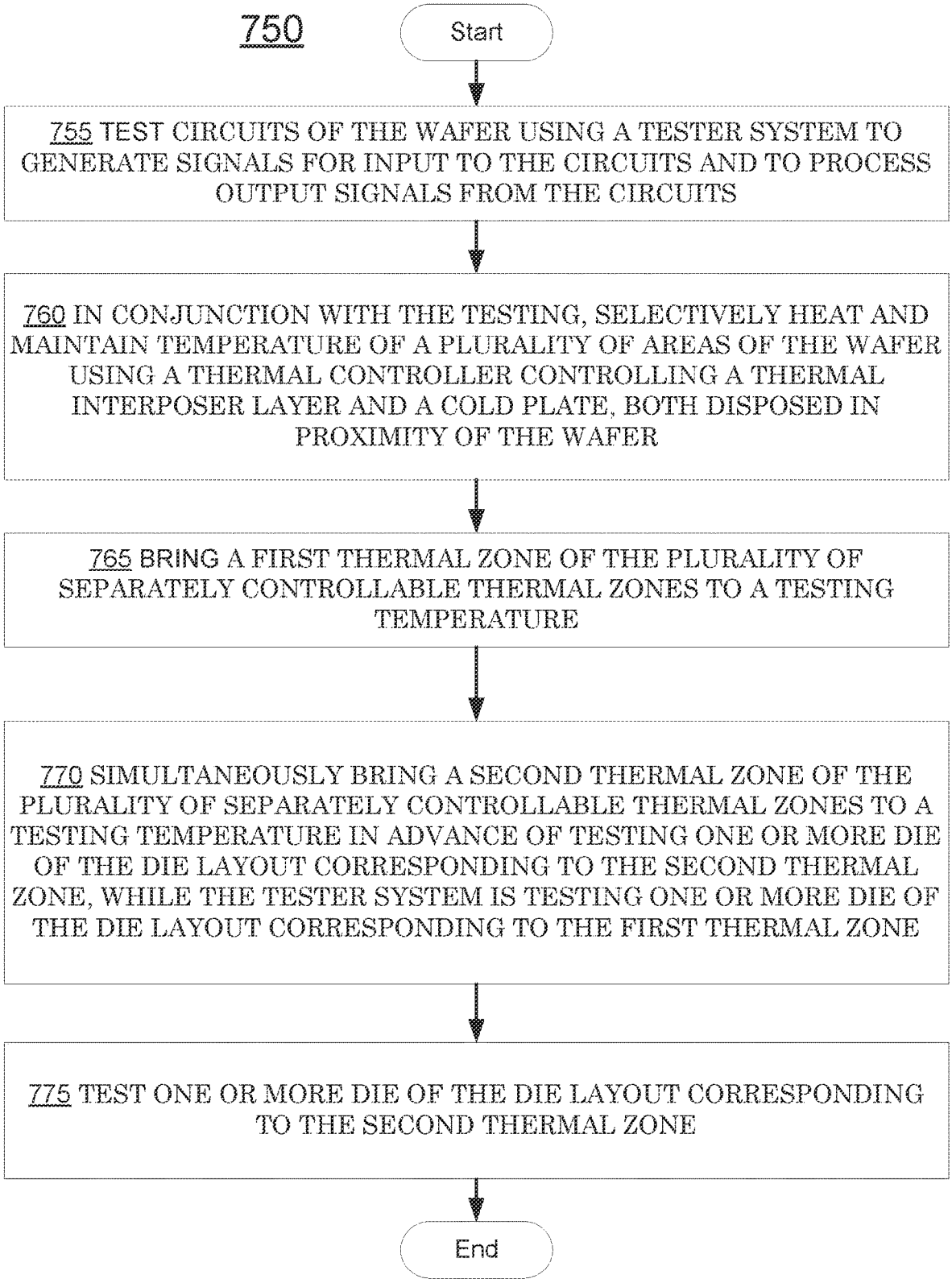
750
Start
755 TEST CIRCUITS OF THE WAFER USING A TESTER SYSTEM TO GENERATE SIGNALS FOR INPUT TO THE CIRCUITS AND TO PROCESS OUTPUT SIGNALS FROM THE CIRCUITS
760 IN CONJUNCTION WITH THE TESTING, SELECTIVELY HEAT AND MAINTAIN TEMPERATURE OF A PLURALITY OF AREAS OF THE WAFER USING A THERMAL CONTROLLER CONTROLLING A THERMAL INTERPOSER LAYER AND A COLD PLATE, BOTH DISPOSED IN PROXIMITY OF THE WAFER
765 BRING A FIRST THERMAL ZONE OF THE PLURALITY OF SEPARATELY CONTROLLABLE THERMAL ZONES TO A TESTING TEMPERATURE
770 SIMULTANEOUSLY BRING A SECOND THERMAL ZONE OF THE PLURALITY OF SEPARATELY CONTROLLABLE THERMAL ZONES TO A TESTING TEMPERATURE IN ADVANCE OF TESTING ONE OR MORE DIE OF THE DIE LAYOUT CORRESPONDING TO THE SECOND THERMAL ZONE, WHILE THE TESTER SYSTEM IS TESTING ONE OR MORE DIE OF THE DIE LAYOUT CORRESPONDING TO THE FIRST THERMAL ZONE
775 TEST ONE OR MORE DIE OF THE DIE LAYOUT CORRESPONDING TO THE SECOND THERMAL ZONE
End

Fig. 7B

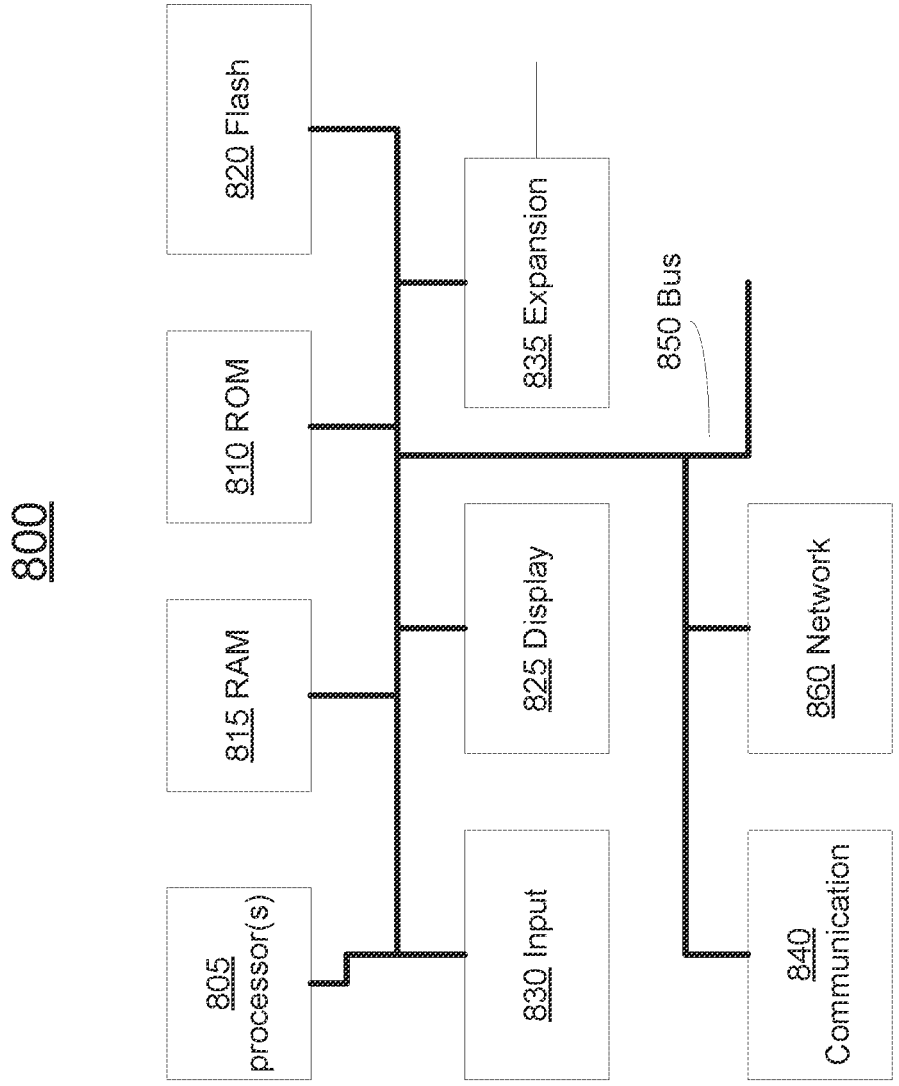
800
820 Flash
810 ROM
815 RAM
805 processor(s)
835 Expansion
825 Display
830 Input
850 Bus
860 Network
840 Communication

Fig. 8

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

RELATED APPLICATION(S)

This application claims priority to U.S. Provisional Application No. 63/115,813, filed Nov. 19, 2020, entitled "Wafer Scale Active Thermal Interposer," which is incorporated herein by reference in its entirety. This application is related to U.S. Pat. No. 9,291,667 entitled "Adaptive Thermal Control," which is incorporated herein by reference in its entirety.

FIELD OF INVENTION

Embodiments of the present invention relate to the field of integrated circuit manufacturing and test. More specifically, embodiments of the present invention relate to systems and methods for testing integrated circuit devices in wafer embodiments.

BACKGROUND

It is common to subject integrated circuits, either packaged or unpackaged, to environmental testing as an operation in a manufacturing processes. Typically in such testing, the integrated circuit devices are subject to electrical testing, e.g., "test patterns," to confirm functionality while being subjected to environmental stress. For example, an integrated circuit is heated and/or cooled to its specification limits while being electrically tested. In some cases, e.g., for qualification testing, an integrated circuit may be stressed beyond its specifications, for example, to determine failure points and/or establish "guard band" on its environmental specifications.

Traditionally, such testing has included placing one or more integrated circuits and their associated test interface(s) and support hardware into an environmental chamber. The environmental chamber would heat and/or cool the integrated circuit(s) under test, known as or referred to as a device under test, or "DUT," as well as the test interface and support hardware, to the desired test temperature. Unfortunately, use of such test chambers has numerous drawbacks. For example, the limits and/or accuracy of such testing may be degraded due to environmental limits of the test interface circuits and/or devices. In addition, due to the large volumes of air and mass of mounting structures and interface devices required within an environmental test chamber, the environment inside such a test chamber may not be changed rapidly, limiting a rate of testing. Further, placing and removing DUTs and testing apparatus into and out of such test chambers further limits rates of testing, and requires complex and expensive mechanisms to perform such insertions and removals.

Recently, environmental test systems have be created that heat and/or cool a DUT directly, without placing the DUT and test apparatus into an environmental chamber. Such "chamber-less" test systems overcome many of the limitations of chamber-based testing. Unfortunately, chamber-less test systems introduce testing difficulties, particularly related to cooling integrated circuits under test.

Cooling of integrated circuits under test is typically performed by thermally coupling a cooling structure, e.g., metal, to the device under test. A cooling fluid, e.g., comprising glycol, is circulated through a portion of the cooling structure. To adjust the temperature of the cooling structure, the temperature of the cooling fluid may be adjusted. The flow of the cooling fluid may also be adjusted, e.g., increased, reduced, started, and/or stopped.

It is desirable to perform environmental testing at a wafer level, for example, comprising tens to potentially thousands of dice, beneficially increasing manufacturing throughput. In addition, testing at a wafer level may identify defective or sub-standard die at the wafer level, avoiding the expense of additional manufacturing and test operations for such devices.

Unfortunately, precise heating and/or cooling of an individual die within a wafer is not available under the conventional art, rendering wafer-level testing under environmental conditions unavailable.

SUMMARY OF THE INVENTION

Therefore, what is needed are systems and methods for wafer scale active thermal interposer devices. What is additionally needed are systems and methods for wafer scale active thermal interposer devices operable to control different portions of a wafer to different temperatures. There is a further need for systems and methods for wafer scale active thermal interposer devices that are compatible and complementary with existing systems and methods of testing integrated circuits.

In accordance with embodiments of the present invention, a system for testing circuits of an integrated circuit semiconductor wafer includes a tester system for generating signals for input to the circuits and for processing output signals from the circuits for testing the wafer and a test stack coupled to the tester system. The test stack includes a wafer probe for contacting a first surface of the wafer and for probing individual circuits of the circuits of the wafer, a wafer thermal interposer (TI) layer operable to contact a second surface of the wafer and operable to selectively heat areas of the wafer, and a cold plate disposed under the wafer TI layer and operable to cool the wafer. The system further includes a thermal controller for selectively heating and maintaining temperatures of the areas of the wafer by controlling cooling of the cold plate and by controlling selective heating of the wafer TI layer.

In accordance with another embodiment of the present invention, a system for testing circuits of an integrated circuit semiconductor wafer includes a tester system for generating signals for input to the circuits and for processing output signals from the circuits for testing the wafer and a test stack coupled to the tester system. The test stack includes a wafer probe for contacting a top surface of the wafer and for probing individual circuits of the circuits of the wafer, a wafer thermal interposer (TI) layer operable to contact a bottom surface of the wafer and including a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of the wafer, and a cold plate disposed under the wafer TI layer and operable to cool the wafer. The system further includes a thermal controller for selectively heating and maintaining temperatures of areas of the wafer by controlling cooling of the cold plate and by controlling heating of the plurality of discretely controllable thermal zones of the wafer TI layer.

In accordance with a method embodiment of the present invention, a method for testing circuits of an integrated circuit semiconductor wafer includes testing the circuits of the wafer by using a tester system to generate signals for input to the circuits and to process output signals from the circuits, and in conjunction with the testing, selectively heating and maintaining temperatures of a plurality of areas

of the wafer by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of the wafer and wherein the thermal interposer includes a plurality of separately controllable thermal zones wherein each thermal zone is operable to be selectively heated and temperature maintained by the thermal controller.

Embodiments include a system for testing circuits of an integrated circuit semiconductor wafer device under test (DUT), the system comprising: a tester system for generating signals for input to said circuits and for processing output signals from said circuits for testing said wafer DUT; a test stack coupled to said tester system, said test stack comprising: a wafer probe for contacting a top surface of said wafer DUT and for probing individual circuits of said circuits of said wafer DUT; a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer DUT and operable to selectively heat areas of said wafer DUT; and a cold plate disposed under said wafer TI layer and operable to cool said wafer DUT, said cold plate being disposed within a thermal array; and a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer DUT by controlling cooling of said cold plate and by controlling heating of said wafer TI layer.

Embodiments include the above and further comprising a power supply coupled to provide power to said wafer TI layer and controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said heating of said wafer TI layer is based on said PWM signals. Embodiments include the above and further comprising: a chiller for cooling liquid; a valve for controlling an amount of said liquid flowing to said cold plate, wherein said valve is controlled by said thermal controller. Embodiments include the above and further comprising: a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and a second TIM layer disposed between said wafer TI layer and said wafer DUT.

Embodiments include the above and wherein said first and second TIM layers comprise indium foil. Embodiments include the above and further comprising: a first vacuum valve for establishing suction for securing said wafer DUT to said wafer TI layer; a second vacuum valve for establishing suction for securing said wafer TI layer to said cold plate; and a vacuum pump coupled to both said first and second vacuum valves. Embodiments include the above and further comprising: a first blow-off valve for controlling air to release said wafer DUT from said wafer TI layer; a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and a source of air coupled to both said first and second blow-off valves.

Embodiments include the above and wherein said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and wherein said plurality of traces are operable to selectively heat a plurality of zones of said wafer TI layer under control of said thermal controller and wherein further said plurality of zones correspond to said areas of said wafer DUT. Embodiments include the above and wherein said plurality of zones of said wafer TI layer correspond to a die layout of said wafer DUT and wherein further said wafer TI layer is customized for said wafer DUT. Embodiments include the above and wherein each zone of said plurality of zones corresponds to a respective single die of said die layout of said wafer DUT. Embodiments include the above and wherein each zone of said plurality of zones corresponds to a respective plurality of die of said die layout of said wafer DUT. Embodiments include the above and wherein each die of said die layout of said wafer DUT corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.

Embodiments include the above and further comprising a pin lift mechanism for displacing pins for lifting said wafer DUT away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical pass through channels which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer DUT. Embodiments include the above and wherein: said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and operable to selectively heat a plurality of zones of said wafer TI layer responsive to said PWM signals; and said wafer TI layer comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer DUT from EMI radiation resultant from said PWM signals applied to said plurality of traces.

Embodiments are also drawn to a system for testing circuits of an integrated circuit semiconductor wafer device under test (DUT), the system comprising: a tester system for generating signals for input to said circuits and for processing output signals from said circuits for testing said wafer DUT; a test stack coupled to said tester system, said test stack comprising: a wafer probe for contacting a top surface of said wafer DUT and for probing individual circuits of said circuits of said wafer DUT; a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer DUT and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer DUT; and a cold plate disposed under said wafer TI layer and operable to cool said wafer DUT; and a thermal controller for selectively heating and maintaining temperatures of areas of said wafer DUT by controlling cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer.

Embodiments include the above and wherein said wafer DUT comprises a die layout comprising a plurality of die and wherein further said plurality of discretely controllable thermal zones is customized to said die layout of said wafer DUT. Embodiments include the above and wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to multiple die of said die layout of said wafer DUT. Embodiments include the above and wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to a single die of said die layout of said wafer DUT. Embodiments include the above and wherein each die of said die layout of said wafer DUT corresponds to multiple thermal zones of said plurality of discretely controllable thermal zones of said wafer TI layer.

Embodiments include the above and wherein said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and operable to selectively heat and maintain temperatures of said plurality of discretely controllable thermal zones of said wafer TI layer responsive to said thermal controller. Embodiments include the above and wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and while said tester system is testing one or more die of said die layout corre-

sponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

Embodiments include the above and wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and while said tester system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

Embodiments are drawn to a method for testing circuits of an integrated circuit semiconductor wafer device under test (DUT), the method comprising: testing said circuits of said wafer DUT by using a tester system to generate signals for input to said circuits and to process output signals from said circuits; and in conjunction with said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer DUT by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of said wafer DUT and wherein said thermal interposer device comprises a plurality of separately controllable thermal zones wherein each thermal zone is operable to be selectively heated and temperature maintained by said thermal controller.

Embodiments include the above and wherein said wafer DUT comprises a die layout and wherein further said plurality of separately controllable thermal zones of said thermal interposer device layer is customized to said die layout. Embodiments include the above and wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer DUT by using a thermal controller comprises: bringing a first thermal zone of said plurality of separately controllable thermal zones to a testing temperature; and while said tester system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of separately controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

Embodiments include the above and wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer DUT by using a thermal controller comprises: bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and while said tester system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. Unless otherwise noted, the drawings may not be drawn to scale.

FIG. **1** illustrates an exemplary block diagram of elements of an automated test system environment that may serve as a platform for embodiments in accordance with the present invention.

FIG. **2** illustrates an exemplary block diagram cross sectional view of a novel wafer scale active thermal interposer device, in accordance with embodiments of the present invention.

FIG. **3** illustrates an exemplary block diagram of elements of an automated test system environment including a wafer scale active thermal interposer device, in accordance with embodiments of with the present invention.

FIG. **4** illustrates an exemplary plan view of an exemplary layout **400** of controllable regions of a wafer scale active thermal interposer device and an associated exemplary wafer, in accordance with embodiments of the present invention.

FIG. **5** illustrates an exemplary plan view layout of controllable regions of a wafer scale active thermal interposer device and an associated wafer **520**, in accordance with embodiments of the present invention.

FIG. **6** illustrates an exemplary plan view layout of controllable regions of a wafer scale active thermal interposer device and an associated wafer, in accordance with embodiments of the present invention.

FIG. **7**A illustrates an exemplary computer controller process for testing circuits of an integrated circuit semiconductor wafer comprising multiple integrated circuit dice using a wafer scale active thermal interposer device, in accordance with embodiments of the present invention.

FIG. **7**B illustrates an exemplary computer controlled method for testing circuits of an integrated circuit semiconductor wafer using a wafer scale active thermal interposer device, in accordance with embodiments of the present invention.

FIG. **8** illustrates a block diagram of an exemplary electronic system, which may be used as a platform to implement and/or as a control system for embodiments of the present invention.

DETAILED DESCRIPTION

Reference will now be made in detail to various embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with these embodiments, it is understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the invention, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be recognized by one of ordinary skill in the art that the invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the invention.

Some portions of the detailed descriptions which follow (e.g., process **700**) are presented in terms of procedures, steps, logic blocks, processing, and other symbolic representations of operations on data bits that may be performed on computer memory. These descriptions and representations are the means used by those skilled in the data

processing arts to most effectively convey the substance of their work to others skilled in the art. A procedure, computer executed step, logic block, process, etc., is here, and generally, conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, data, or the like.

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present invention, discussions utilizing terms such as "testing" or "heating" or "maintaining temperature" or "bringing" or "capturing" or "storing" or "reading" or "analyzing" or "generating" or "resolving" or "accepting" or "selecting" or "determining" or "displaying" or "presenting" or "computing" or "sending" or "receiving" or "reducing" or "detecting" or "setting" or "accessing" or "placing" or "testing" or "forming" or "mounting" or "removing" or "ceasing" or "stopping" or "coating" or "processing" or "performing" or "generating" or "adjusting" or "creating" or "executing" or "continuing" or "indexing" or "translating" or "calculating" or "measuring" or "gathering" or "running" or the like, refer to the action and processes of, or under the control of, a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

The meaning of "non-transitory computer-readable medium" should be construed to exclude only those types of transitory computer-readable media which were found to fall outside the scope of patentable subject matter under 35 U.S.C. § 101 in *In re Nuijten,* 500 F.3d 1346, 1356-57 (Fed. Cir. 1007). The use of this term is to be understood to remove only propagating transitory signals per se from the claim scope and does not relinquish rights to all standard computer-readable media that are not only propagating transitory signals per se.

Wafer Scale Active Thermal Interposer for Device Testing

FIG. **1** illustrates an exemplary block diagram of elements of an automated test system environment **100**, which utilizes a wafer scale active thermal interposer device, that may serve as a platform for embodiments in accordance with the present invention. Test system **100** receives and tests a semiconductor wafer **120**, for example comprising a plurality of integrated circuit devices or dice. A wafer probe card **110** is coupled to wafer **120**, e.g., utilizing test pads formed on the wafer **120**, to send and receive test signals and power to integrated circuit devices embodied within or on wafer **120**. Wafer probe card **110** is typically electronically coupled to, and tests, a single die of wafer **120** at a time, although that is not required.

In accordance with embodiments of the present invention, a novel wafer scale active thermal interposer device **130** is coupled to the backside of wafer **120**. Wafer scale active thermal interposer device **130** may be customized for a specific design of wafer **120**, in some embodiments. In some embodiments, there may be a thermal interface material (not shown, see FIG. **3**) disposed between wafer scale active thermal interposer device **130** and wafer **120**. Such a thermal interface material, if present, is designed to improve thermal coupling between wafer scale active thermal interposer device **130** and wafer **120**.

In some embodiments, wafer scale active thermal interposer device **130** may comprise a base layer of aluminum nitride (AlN) with tungsten and/or molybdenum traces. A high temperature co-fired ceramic (HTCC) process may be utilized. Such embodiments may be suitable for testing comparatively higher power devices. In some embodiments, a low temperature co-fired ceramic (LTCC) process, e.g., comprising aluminum oxide (Al_2O_3) may be utilized. Such embodiments may be suitable for testing comparatively lower power devices.

Wafer scale active thermal interposer device **130** is further coupled to a cold plate **140**. In some embodiments, there may be a thermal interface material (not shown) disposed between wafer scale active thermal interposer device **130** and cold plate **140**. Such a thermal interface material, if present, is designed to improve thermal coupling between wafer scale active thermal interposer device **130** and cold plate **140**.

In an embodiment, a cooling fluid, e.g., comprising glycol, although other fluids, including air, may be used, is generally circulated through cold plate **140**. To adjust the temperature of the cold plate **140**, the temperature of the cooling fluid may be adjusted, in some embodiments. In some embodiments, as illustrated in FIG. **1**, the flow rate of the cooling fluid may also be adjusted, e.g., increased, reduced, started, and/or stopped. For example, a speed of a pump and/or fan may be adjusted. In an embodiment, chiller **160** cools the cooling fluid, e.g., to −60 degrees C. The cooling fluid flows through **161** to valve **150**. Valve **150**, under the control of thermal controller **180**, regulates the flow **151** of cooling fluid to cold plate **140**. After cycling through cold plate **140**, the cooling fluid is returned **141** to the chiller **160**. In this manner, thermal controller **180** may cool wafer **120** during testing via cooling action from chiller **160** and the cold plate **140**.

In accordance with embodiments of the present invention, thermal controller **180** may implement some or all of the control processes described in U.S. Pat. No. 9,291,667 entitled "Adaptive Thermal Control," incorporated herein by reference in its entirety.

In some embodiments, cold plate **140** may comprise an evaporator and/or phase change cooling system. In such embodiments, chiller **160** may comprise a compressor and/or radiator, for example.

Wafer scale active thermal interposer device **130** functions to apply heat energy to one or more temperature regions of wafer **120**. There temperature regions may correspond, in location and shape, with the dice on the wafer **120**. To accomplish such heating, wafer scale active thermal interposer device **130** comprises one or more heating elements, as further described below. The heating elements of wafer scale active thermal interposer device **130** correspond to the temperature regions of wafer **120**. In some embodiments, the heating elements comprise resistive traces on a ceramic substrate. In some embodiments, the heating elements may be Peltier devices, capable of cooling as well. However, any suitable heating and/or cooling technology is well suited to embodiments in accordance with the present

invention. Wafer scale active thermal interposer device **130** also functions to couple heat energy from wafer **120** to cold plate **140** for cooling.

Wafer scale active thermal interposer device **130** further comprises a plurality of temperature measurement devices, e.g., thermocouples. The plurality of temperature measurement devices are configured to measure temperatures of regions of wafer **120**. The plurality of temperature measurement devices may be located within or in close proximity to the heating elements of wafer scale active thermal interposer device **130**. In some embodiments, wafer scale active thermal interposer device **130** may comprise temperature measurement devices characterized as not within or in close proximity to the heating elements of wafer scale active thermal interposer device **130**. Each of the plurality of temperature measurement devices sends a temperature signal **131** to thermal controller **180**. Wafer probe card **110**, wafer **120**, wafer scale active thermal interposer device **130**, and cold plate **140** may be collectively known as or referred to as a test stack or test head when coupled together as illustrated in FIG. **1**.

Test system **100** further comprises a thermal controller **180**. Thermal controller **180** is an intelligent device and sends control signals **182** to power supply **170** to supply electrical power **171** to one or more heating elements of wafer scale active thermal interposer device **130**. Each heating element of wafer scale active thermal interposer device **130** may be individually controlled. Accordingly, there are typically more power signals **171** than illustrated. There may be more than one power supply, in some embodiments. Based on temperature feedback **131** from one or more of the plurality of temperature measurement devices, thermal controller **180** may control power supply **170** to change the power supplied to a heating element. Power supply **170** may change a voltage level and/or pulse width modulate a voltage supplied to a heating element to control heating of the heating element, in some embodiments. Thermal controller **180** also controls the amount of heat energy extracted **141** from cold plate **140**. For example, thermal controller **180** controls the temperature of cold plate **140**. Thermal controller **180** controls valve **150** based on temperature feedback **131**.

It is to be appreciated that cold plate **140** extracts heat, through wafer scale active thermal interposer device **130**, from substantially all of wafer **120**. In addition, cold plate **140** typically has a large thermal mass, and does not change temperature quickly. Accordingly, heating elements of wafer scale active thermal interposer device **130** may often be required to overcome the cooling effect of cold plate **140**. In some embodiments, different regions of a wafer **120** may be heated and/or cooled to different temperatures based on the selective heating capability of the heaters of the wafer scale active thermal interposer device **10** and the cooling function of cold plate **140**. For example, one region of wafer **120** may be heated to 100 degrees C., e.g., via a heater element within wafer scale active thermal interposer device **130**, while another region of wafer **120** may be allowed to cool toward the temperature of cold plate **140** with no heat applied to such region by wafer scale active thermal interposer device **130**. Such differential heating and/or cooling of different regions of wafer **120** may produce a thermal gradient across or between regions of wafer **120**, in some embodiments.

FIG. **2** illustrates an exemplary block diagram cross sectional view of a novel wafer scale active thermal interposer device **200**, in accordance with embodiments of the present invention. Wafer scale active thermal interposer device **200** comprises a heating element layer **250**. Heating element layer **250** comprises a plurality of discrete and separately controllable heating elements configured to apply heat energy to a wafer (not shown). The heating elements may comprise resistive traces or other suitable types of heaters. The plurality of heating elements are coupled to a plurality of electrical signals **255**, for providing controlled power to the heating elements such that the elements are separately controllable. Heating element layer **250** may include low resistance traces, e.g., from electrical signals **255** to the actual heating elements, in some embodiments. Heating element layer **250** also comprises a plurality of temperature measurement devices, e.g., thermocouples, (not shown), which are coupled to control elements via temperature a plurality of sense signals **252**.

In accordance with embodiments of the present invention, wafer scale active thermal interposer device **200** may comprise a novel electromagnetic interference (EMI) shield layer **220** to address signal interference caused by the heater elements. Each of the plurality of heating elements in layer **250** may utilize currents of many tens of amperes. In embodiments of the present invention that utilize switching such currents to control temperature, e.g., pulse width modulation, such switching may induce unwanted electromagnetic noise signals that are deleterious to the operation and/or test of integrated circuits on a wafer, e.g., wafer **120** of FIG. **1**, coupled to the wafer scale active thermal interposer device **200**. In some embodiments, EMI shield layer **220** comprises a solid layer of conductor, e.g., conductive traces similar to those utilized in heating element layer **250**. In some embodiments, EMI shield layer **220** comprises a grid of conductive elements. The grid may be sized to attenuate desired wavelength(s) of electromagnetic interference. EMI shield layer **220** may have an electrical connection **225**, e.g., to ground, in some embodiments.

Wafer scale active thermal interposer device **200** comprises a top thermal layer **240**. Thermal layer **240** functions to couple heat energy from heating element layer **250** to a wafer under test and vice versa. Thermal layer **240** is non conductive, in some embodiments. Thermal layer **240** should have a high degree of co-planarity in order to facilitate good thermal conduction to a wafer and to promote good vacuum hold down of the wafer, in some embodiments.

Wafer scale active thermal interposer device **200** is compatible and complementary with conventional elements of wafer scale test equipment. Accordingly, in some embodiments, wafer scale active thermal interposer device **200** may comprise one or more wafer vacuum line passthrough ports **215**. Wafer vacuum line passthrough ports **215** couple to one or more conventional vacuum lines, as is typically used to hold down a wafer in place during testing. For example, wafer vacuum line passthrough port **215** mates with a vacuum port of a conventional cold plate, e.g., cold plate **140** of FIG. **1**. There may be a plurality of wafer vacuum line passthrough ports **215** in an instance of wafer scale active thermal interposer device **200**, for example three arranged in an equilateral triangle, in some embodiments. A wafer vacuum line passthrough port **215** typically extends through wafer scale active thermal interposer device **200**.

In some embodiments, wafer scale active thermal interposer device **200** may comprise one or more wafer blowoff line passthrough ports **221**. Wafer blowoff line passthrough port **221** couples to a conventional wafer blowoff line, as is typically used to break a vacuum seal of a wafer, prior to removing the wafer from the test system. For example, wafer blowoff line passthrough port **221** mates with a wafer blowoff line port of a conventional cold plate, e.g., cold plate

140 of FIG. 1. There may be a plurality of wafer blowoff line passthrough ports 221 in an instance of wafer scale active thermal interposer device 200, for example three arranged in an equilateral triangle, in some embodiments. A wafer blowoff line passthrough port 221 typically extends through wafer scale active thermal interposer device 200.

Wafer scale active thermal interposer device 200 may also comprise a wafer pin lift port 230, in some embodiments. Wafer pin lift port 230 may be aligned with a similar port or channel in a cold plate, e.g., cold plate 140 of FIG. 1. Wafer pin lift port 230 enables a wafer lift pin 235 to raise a wafer above the top of the wafer scale active thermal interposer device 200. For example, wafer handling equipment typically needs a gap under a wafer in order to lift the wafer and move the wafer to another station in a wafer manufacturing and test process. The wafer lift pin 235 typically extends from or through a cold plate, e.g., cold plate 140 of FIG. 1, and/or from a chuck mechanism (not shown). In accordance with some embodiments of the present invention, the wafer lift pin 235 may be lengthened, in contrast to a conventional lift pin, to account for the thickness of wafer scale active thermal interposer device 200. There may be a plurality of wafer pin lift ports 230 in an instance of wafer scale active thermal interposer device 200, for example three arranged in an equilateral triangle, in some embodiments. A wafer pin lift port 230 typically extends through wafer scale active thermal interposer device 200.

With respect to the wafer scale active thermal interposer device 200, wafer vacuum line passthrough ports 215, wafer blowoff line passthrough ports 221 and/or wafer pin lift ports 230 may be combined in any suitable combination, in accordance with embodiments of the present invention. For example, a wafer vacuum line passthrough ports 215 may be combined with a wafer blowoff line passthrough port 221.

FIG. 3 illustrates an exemplary block diagram of elements of an automated test system environment 300 including a wafer scale active thermal interposer device, in accordance with embodiments of with the present invention. FIG. 3 illustrates functional components of a wafer vacuum hold down and blowoff systems in combination with wafer scale active thermal interposer device 130.

Test system environment 300 comprises a vacuum pump 330 coupled to wafer vacuum valve 310 and wafer scale active thermal interposer (ATI) vacuum valve 320. Wafer vacuum valve 310 is coupled to wafer vacuum/blowoff line passthrough port 315 of wafer scale active thermal interposer device 130. In the illustrated embodiment, the vacuum passthrough and blowoff passthrough ports are combined, although this is not required and such ports may be separate. To hold down a wafer 120 prior to and during test, wafer vacuum valve 310 is opened, enabling a pressure differential between ambient atmosphere and vacuum to hold down the wafer 120 to the wafer scale active thermal interposer device 130.

ATI vacuum valve 320 is coupled to ATI vacuum/blowoff line passthrough port 316 of cold plate 140. To hold down ATI 130 prior to and during test, ATI vacuum valve 320 is opened, enabling a pressure differential between ambient atmosphere and/or ATI 130 and vacuum to hold down the ATI 130 to the cold plate 140.

Compressed dry air source (CDA) 360 is coupled to wafer CDA blowoff valve 340 and to ATI CDA blowoff valve 350. To blow the wafer off of the ATI 130, the wafer vacuum valve 310 is closed and the wafer CDA blowoff valve 340 is opened, coupling compressed dry air through the vacuum/blowoff line passthrough port 315 to break the prior vacuum seal. To remove the wafer scale active thermal interposer device 130 from the cold plate 140, for example, to change to a different wafer scale thermal interposer, the ATI vacuum valve 320 is closed and the ATI CDA blowoff valve 350 is opened, coupling compressed dry air through the ATI vacuum/blowoff line passthrough port 316 to break the prior vacuum seal.

In accordance with embodiments of the present invention, test system 300 may comprise a thermal interface material (TIM) 370 disposed at the ATI/wafer interface and/or a thermal interface material 380 disposed at the ATI/cold plate interface. The thermal interface material is operable to provide thermal coupling, e.g., has a high thermal conductance, and provides mechanical compliance to compensate for irregularities in the adjoining surfaces. The thermal interface material may be considered to be separate from the wafer scale active thermal interposer device 130, in some embodiments. For example, a thermal interface material 370 may be applied to the wafer scale active thermal interposer device 130 after the wafer scale active thermal interposer device 130 is placed in the test system 300. Any suitable thermal interface material may be used, including those comprising indium foil and/or carbon nanotubes, in accordance with embodiments of the present invention. Thermal interface material 370 may differ from thermal interface material 380 in composition and/or thickness, in some embodiments.

FIG. 4 illustrates an exemplary plan view layout of an exemplary layout 400 of controllable regions of a wafer scale active thermal interposer device 430 and an associated exemplary wafer 420, in accordance with embodiments of the present invention. The wafer scale active thermal interposer device 430 generally corresponds to wafer scale active thermal interposer device 130 as previously described in FIGS. 1, 2, and 3. The wafer scale active thermal interposer device 430 is configured to be used in testing of wafer 420.

Wafer 420 comprises a plurality of discrete dice 410. Dice 410 may be characterized as relatively small and/or designed to operate at relatively low power levels. Examples of such integrated circuits may include microcontrollers, dynamic RAMs, application-specific integrated circuits, and the like. Due to their small size and/or low power operational characteristics, such integrated circuits may not require application of large amounts of heat energy to achieve desired test temperatures. In addition, small integrated circuit die may be physically smaller than a desired minimum size of a heating element as used in wafer scale active thermal interposer device 430.

Wafer scale active thermal interposer device 430 comprises a plurality of selective heatable regions 441, 442, 443, 444, 445, 446, 447, 448 and 449. The number of heatable regions and their layout is exemplary, and may be customized to the die layout of the wafer 420. Wafer scale active thermal interposer device 430 is configured to heat and/or cool portions of wafer 420 corresponding to one or more of the selective heatable regions 441, 442, 443, 444, 445, 446, 447, 448 and 449. In accordance with embodiments of the present invention, each heatable region of wafer scale active thermal interposer device 430 corresponds to more than one die of wafer 420. For example, heatable region 449 of wafer scale active thermal interposer device 430 is configured to selectively apply heat energy to approximately nine dice of wafer 420 when coupled to wafer 420 in a test system.

FIG. 5 illustrates an exemplary plan view layout 500 of controllable regions of an exemplary wafer scale active thermal interposer device 530 and an associated exemplary wafer 520, in accordance with embodiments of the present invention. The wafer scale active thermal interposer device

530 generally corresponds to wafer scale active thermal interposer device 130 as previously described in FIGS. 1, 2, and 3. The wafer scale active thermal interposer device 530 is configured to be used in testing of wafer 520.

Wafer 520 comprises a plurality of dice 510. Dice 510 may be characterized as relatively large and/or designed to operate at relatively high power levels. Examples of such integrated circuits may include central processing units (CPUs), graphics processing units (GPUs), Network Processing Units (NPUs), multi-core processing units, power semiconductors, and the like. Due to their large size and/or high power operational characteristics, such integrated circuits may require application of large amounts of heat energy to achieve desired test temperatures.

Wafer scale active thermal interposer device 530 comprises a plurality of selectable heatable regions 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, and 543. The number of heatable regions and their layout is exemplary. Wafer scale active thermal interposer device 530 is configured to heat and/or cool portions of wafer 520 corresponding to one or more of the heatable regions 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, and 543. In accordance with embodiments of the present invention, each heatable region of wafer scale active thermal interposer device 530 corresponds to one die of wafer 520 in location and shape. For example, heatable region 542 of wafer scale active thermal interposer device 530 is configured to selectively apply heat energy to die 512 of wafer 520 when coupled to wafer 520 in a test system. In this novel manner, wafer scale active thermal interposer device 530 may selectively apply sufficient heat energy to large and/or high-power die to achieve desired test temperatures while in wafer form. The discrete dice of the wafer 520 may be selectively heated during testing by the discrete and separately controller heating elements of the wafer scale active thermal interposer device 530.

FIG. 6 illustrates an exemplary plan view layout 600 of controllable regions of a wafer scale active thermal interposer device 630 and an associated wafer 620, in accordance with embodiments of the present invention. The wafer scale active thermal interposer device 630 generally corresponds to wafer scale active thermal interposer device 130 as previously described in FIGS. 1, 2, and 3. The wafer scale active thermal interposer device 630 is configured to be used in testing of wafer 620.

Wafer 620 comprises a plurality of dice 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, and 613. Dice 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, and 613 may be characterized as relatively large and/or designed to operate at relatively high power levels. Examples of such integrated circuits may include central processing units (CPUs), graphics processing units (GPUs), Network Processing Units (NPUs), multi-core processing units, power semiconductors, and the like. Due to their large size and/or high power operational characteristics, such integrated circuits may require application of large amounts of heat energy to achieve desired test temperatures.

Large and complex integrated circuits frequently comprise a plurality of functional units, e.g., multiple processing cores, which are physically distinct. It may be desirable to test such functional units in whole or in partial isolation from other function units of a die. For example, a GPU comprising multiple floating point units may be designed to utilize a single floating point unit at times during operation, and turn off other floating point units, e.g., those that are not currently required, in order to reduce power consumption. It may be desirable to test the GPU under similar thermal conditions. For example, it may be desirable to run functional tests on a portion of the GPU corresponding to an operational floating point unit at a high temperature, while other portions of the GPU are at a different, e.g., lower, temperature, simulating non-operation.

In addition, the heat energy required to achieve a desirable test temperature for large and/or high powered die may exceed the capacity of a single heating element of a wafer scale thermal interposer. For example, conductive traces of a wafer scale thermal interposer may have current capacity limitations. Further, other components of a single heating element and/or a wafer scale thermal interposer may limit an amount of heat energy generated to be less that required to supply sufficient heat energy to achieve a desired temperature of a die under test.

Wafer scale active thermal interposer device 630 comprises a plurality of heatable regions, e.g., heatable regions 641, 642, 643, and 644. The number of heatable regions and their layout is exemplary. Wafer scale active thermal interposer device 630 is configured to selectively heat and/or cool portions of wafer 620 corresponding to one or more of the heatable regions 641, 642, 643, and 644. In accordance with embodiments of the present invention, each heatable region of wafer scale active thermal interposer device 630 corresponds to a portion of one die of wafer 620. For example, heatable region 642 of wafer scale active thermal interposer device 630 is configured to selectively apply heat energy to the right upper quadrant of die 612 of wafer 620 when coupled to wafer 620 in a test system. In this novel manner, wafer scale active thermal interposer device 630 may selectively apply sufficient heat energy to portions of large and/or high-power die to achieve desired test temperatures, including different temperatures within a single die, while in wafer form.

In accordance with embodiments of the present invention, areas of a wafer, e.g., wafer 620 of FIG. 6, which are not under test may nevertheless be opportunistically preconditioned to a desirable temperature. For example, while testing die 612 (FIG. 6) at a desired testing temperature, embodiments in accordance with the present invention may bring die 609 to a desired test temperature while die 609 is not being tested, e.g., prior to testing die 609. It is appreciated that semiconductor die have a thermal mass, and do not change temperature instantaneously. In this novel manner, a plurality of die may be opportunistically preconditioned to a desirable temperature, e.g., in advance of their testing, to increase testing throughput. Such opportunistic temperature preconditioning may beneficially increase a rate of testing of multiple dice, for example, by eliminating a time delay between testing of a first and a second die required to bring the second die, or portion thereof, to a desirable test temperature.

FIG. 7A illustrates an exemplary computer controller process 700 for testing circuits of an integrated circuit semiconductor wafer comprising multiple integrated circuit dice using a wafer scale active thermal interposer device, in accordance with embodiments of the present invention. In 705, a wafer comprising multiple dice for testing is received for testing, e.g., within an automated test equipment, for example, automated test environment 100 of FIG. 1.

In 710, a wafer, e.g., wafer 120 of FIG. 1, is placed in contact with a wafer scale active thermal interposer device, e.g., wafer scale active thermal interposer device 130 (FIG. 1). In 715, circuit testing is performed on the wafer by electrically contacting dice of the wafer to apply testing signals thereto and to receive test output signals from the dice.

In **720**, while performing the circuit testing, the temperature of dice under test is controlled by: 1) selectively controlling the heating of a plurality of heater elements within the wafer scale active thermal interposer device, wherein the plurality of heater elements correspond to a plurality of dice within the wafer under test; and 2) selectively controlling cooling of the cold plate. In optional **725**, the results of the circuit testing are recorded.

FIG. **7**B illustrates an exemplary computer controlled method **750** for testing circuits of an integrated circuit semiconductor wafer using a wafer scale active thermal interposer device, in accordance with embodiments of the present invention. In **755**, the circuits of a wafer are tested by using a tester system to generate signals for input to the circuits and to process output signals from the circuits.

In **760**, in conjunction with the testing, a plurality of areas of the wafer are selectively heated and have their temperatures maintained by using a thermal controller selectively controlling discrete heater elements of a thermal interposer layer and a cold plate, both disposed in proximity of the wafer. The thermal interposer comprises a plurality of separately controllable thermal zones wherein each thermal zone is operable to be selectively heated and temperature maintained by the thermal controller. The thermal zones may correspond in location and shape to dice on the wafer being tested. The selective heating may include bringing a first set of thermal zones of the plurality of separately controllable thermal zones to a testing temperature while the tester system is testing a first die of the die layout corresponding to the first set of thermal zones, simultaneously and opportunistically bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of the die layout corresponding to the second set of thermal zones.

In optional **765**, a first thermal zone of the plurality of separately controllable thermal zones is brought to a testing temperature. In optional **770**, a second thermal zone of the plurality of separately controllable thermal zones to is simultaneously brought to a testing temperature in advance of testing one or more die of the die layout corresponding to the second thermal zone, while the tester system is testing one or more die of the die layout corresponding to the first thermal zone. In optional **775**, one or more die of the die layout corresponding to the second thermal zone are tested.

FIG. **8** illustrates a block diagram of an exemplary electronic system **800**, which may be used as a platform to implement and/or as a control system for embodiments of the present invention. Electronic system **800** may be a "server" computer system, in some embodiments. Electronic system **800** includes an address/data bus **850** for communicating information, a central processor complex **805** functionally coupled with the bus for processing information and instructions. Bus **850** may comprise, for example, a Peripheral Component Interconnect Express (PCIe) computer expansion bus, industry standard architecture (ISA), extended ISA (EISA), MicroChannel, Multibus, IEEE 796, IEEE 1196, IEEE 1496, PCI, Computer Automated Measurement and Control (CAMAC), MBus, Runway bus, Compute Express Link (CXL), and the like.

Central processor complex **805** may comprise a single processor or multiple processors, e.g., a multi-core processor, or multiple separate processors, in some embodiments. Central processor complex **805** may comprise various types of well known processors in any combination, including, for example, digital signal processors (DSP), graphics processors (GPU), complex instruction set (CISC) processors, reduced instruction set (RISC) processors, and/or very long word instruction set (VLIW) processors. Electronic system **800** may also includes a volatile memory **815** (e.g., random access memory RAM) coupled with the bus **850** for storing information and instructions for the central processor complex **805**, and a non-volatile memory **810** (e.g., read only memory ROM) coupled with the bus **850** for storing static information and instructions for the processor complex **805**. Electronic system **800** also optionally includes a changeable, non-volatile memory **820** (e.g., NOR flash) for storing information and instructions for the central processor complex **805** which can be updated after the manufacture of system **800**. In some embodiments, only one of ROM **810** or Flash **820** may be present.

Also included in electronic system **800** of FIG. **8** is an optional input device **830**. Device **830** can communicate information and command selections to the central processor **800**. Input device **830** may be any suitable device for communicating information and/or commands to the electronic system **800**. For example, input device **830** may take the form of a keyboard, buttons, a joystick, a track ball, an audio transducer, e.g., a microphone, a touch sensitive digitizer panel, eyeball scanner, and/or the like.

Electronic system **800** may comprise a display unit **825**. Display unit **825** may comprise a liquid crystal display (LCD) device, cathode ray tube (CRT), field emission device (FED, also called flat panel CRT), light emitting diode (LED), plasma display device, electro-luminescent display, electronic paper, electronic ink (e-ink) or other display device suitable for creating graphic images and/or alphanumeric characters recognizable to the user. Display unit **825** may have an associated lighting device, in some embodiments.

Electronic system **800** also optionally includes an expansion interface **835** coupled with the bus **850**. Expansion interface **835** can implement many well known standard expansion interfaces, including without limitation the Secure Digital Card interface, universal serial bus (USB) interface, Compact Flash, Personal Computer (PC) Card interface, CardBus, Peripheral Component Interconnect (PCI) interface, Peripheral Component Interconnect Express (PCI Express), mini-PCI interface, IEEE 8394, Small Computer System Interface (SCSI), Personal Computer Memory Card International Association (PCMCIA) interface, Industry Standard Architecture (ISA) interface, RS-232 interface, and/or the like. In some embodiments of the present invention, expansion interface **835** may comprise signals substantially compliant with the signals of bus **850**.

A wide variety of well-known devices may be attached to electronic system **800** via the bus **850** and/or expansion interface **835**. Examples of such devices include without limitation rotating magnetic memory devices, flash memory devices, digital cameras, wireless communication modules, digital audio players, and Global Positioning System (GPS) devices.

System **800** also optionally includes a communication port **840**. Communication port **840** may be implemented as part of expansion interface **835**. When implemented as a separate interface, communication port **840** may typically be used to exchange information with other devices via communication-oriented data transfer protocols. Examples of communication ports include without limitation RS-232 ports, universal asynchronous receiver transmitters (UARTs), USB ports, infrared light transceivers, ethernet ports, IEEE 8394, and synchronous ports.

System **800** optionally includes a network interface **860**, which may implement a wired or wireless network interface.

Electronic system **800** may comprise additional software and/or hardware features (not shown) in some embodiments.

Various modules of system **800** may access computer readable media, and the term is known or understood to include removable media, for example, Secure Digital ("SD") cards, CD and/or DVD ROMs, diskettes and the like, as well as non-removable or internal media, for example, hard drives, solid state drive s (SSD), RAM, ROM, flash, and the like.

Embodiments in accordance with the present invention provide systems and methods for wafer scale active thermal interposer devices. In addition, embodiments in accordance with the present invention provide systems and methods for wafer scale active thermal interposer devices operable to control different portions of a wafer to different temperatures. Further, embodiments in accordance with the present invention provide systems and methods for wafer scale active thermal interposer devices that are compatible and complementary with existing systems and methods of testing integrated circuits.

Various embodiments of the invention are thus described. While the present invention has been described in particular embodiments, it should be appreciated that the invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

We claim:

1. A test system for testing circuits of an integrated circuit semiconductor wafer, the test system comprising:

a test computer for testing said circuits by generating signals for input to said circuits, processing output signals from said circuits and generating a test result thereof;

a wafer probe, coupled to said test computer, for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer;

a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer, wherein said wafer TI layer comprises a plurality of resistive traces traversing said wafer TI layer and wherein said plurality of resistive traces are operable to selectively heat a plurality of zones of said wafer TI layer that correspond to said areas of said wafer;

a cold plate disposed adjacent to said wafer TI layer and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer during said testing by controlling cooling of said cold plate and by controlling selective heating of said plurality of resistive traces of said wafer TI layer.

2. The system as described in claim **1** wherein positions of said plurality of zones of said wafer TI layer correspond to a die layout of said wafer and wherein further said wafer TI layer is customized for said wafer.

3. The test system as described in claim **2** further comprising:

a chiller for cooling liquid; and

a valve for controlling an amount of said liquid flowing to said cold plate, wherein said valve is controlled by said thermal controller.

4. The system as described in claim **2** further comprising:

a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and

a second TIM layer disposed between said wafer TI layer and said wafer.

5. The system as described in claim **4** wherein said first and second TIM layers comprise indium foil.

6. The system as described in claim **4** wherein said first and second TIM layers comprise graphite material.

7. The system as described in claim **4** further comprising:

a first vacuum valve for establishing suction for securing said wafer to said wafer TI layer;

a second vacuum valve for establishing suction for securing said wafer TI layer to said cold plate; and

a vacuum pump coupled to both said first and second vacuum valves.

8. The system as described in claim **7** further comprising:

a first blow-off valve for controlling air to release said wafer from said wafer TI layer;

a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and

a source of air coupled to both said first and second blow-off valves.

9. The system as described in claim **2** wherein each zone of said plurality of zones corresponds to a respective single die of said die layout of said wafer.

10. The system as described in claim **2** wherein each zone of said plurality of zones corresponds to a respective plurality of dice of said die layout of said wafer.

11. The system as described in claim **2** wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.

12. The system as described in claim **2** further comprising a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical pass through channels which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer.

13. The test system as described in claim **1** further comprising a power supply coupled to provide power to said wafer TI layer and controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said selective heating of said wafer TI layer is based on said PWM signals.

14. The system as described in claim **13** wherein said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from said PWM signals applied to said plurality of resistive traces.

15. A test system for testing circuits of an integrated circuit semiconductor wafer, the system comprising:

a test computer system for testing said circuits by generating signals for input to said circuits, processing output signals from said circuits and generating a test result for said circuits of said wafer;

a wafer probe for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer, said wafer probe coupled to communicate with said test computer system;

a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer and wherein further said wafer comprises a die layout comprising a plurality of dice and wherein further positions and shapes of said plurality of discretely controllable thermal zones are customized to said die layout of said wafer;

a cold plate disposed under said wafer TI layer and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of areas of said wafer, during said testing, by controlling cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer.

16. The test system as described in claim **15** wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to multiple dice of said die layout of said wafer.

17. The test system as described in claim **15** wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to a single die of said die layout of said wafer.

18. A test system as described in claim **15** wherein each die of said die layout of said wafer corresponds to multiple thermal zones of said plurality of discretely controllable thermal zones of said wafer TI layer.

19. The test system as described in claim **15** wherein said wafer TI layer comprises a plurality of resistive traces traversing said wafer TI layer and operable to selectively heat and maintain temperatures of said plurality of discretely controllable thermal zones of said wafer TI layer responsive to said thermal controller.

20. The test system as described in claim **15** wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and

while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

21. The test system as described in claim **15** wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and

while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

22. The test system as described in claim **15** further comprising: a thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer and wherein said TIM layer comprises one of: indium foil; and graphite material.

23. A method of testing circuits of an integrated circuit semiconductor wafer, the method comprising:

testing said circuits of said wafer by using a test computer system wherein said testing comprises:

generating signals for input to said circuits;

processing output signals from said circuits;

generating a test result for said circuits; and

in conjunction with performing said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of said wafer and wherein said thermal interposer comprises a plurality of separately controllable thermal zones and wherein said selectively heating comprises selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones.

24. The method as described in claim **23** wherein said wafer comprises a die layout and wherein further positions and shapes of said plurality of separately controllable thermal zones of said thermal interposer layer are customized to said die layout.

25. The method as described in claim **24** wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises:

bringing a first thermal zone of said plurality of separately controllable thermal zones to a testing temperature; and

while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of separately controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

26. The method as described in claim **24** wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises:

bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and

while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

27. The method of claim **24** wherein said plurality of separately controlled thermal zones comprise a plurality of resistive traces and wherein further said selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones comprises said thermal controller selectively energizing said plurality of resistive traces during said testing.

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