

L6	110	AND heat\$3 (wafer AND (semiconductor IC (intergrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND computer	IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/28 01:56 PM
L7	123	(wafer AND (semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND computer	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/28 03:01 PM
L8	13	L7 NOT L6	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/28 03:02 PM

L9	171	(wafer AND (semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND (computer process\$3)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/28 10:18 PM
L10	48	L9 NOT L7	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/28 10:19 PM
L11	1749756	(wafer (semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND (computer process\$3)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 12:05 AM
L12	427067	(wafer (semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL,	OR	ON	ON	2023/11/29 12:10 AM

L13	123	(computer)	NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 12:11 AM
L14	194	((semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND (computer) AND wafer	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 12:15 AM
L15	2054	((wafer die semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND (computer)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 06:54 AM
		("8653843" "6515470" "7138811" "7781883" "8970244" "9594113" "10126356" "20060158207" "20090160472" "20110050268" "20140035715" "20150137842" "20160247552" "20190271719" "20200041564" "20210183668" "20210293495" "20220206061" "5239093" "5126656" "5164661" "5315240" "5239093" "5420521"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 06:54 AM

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L16	355	"5821505" "7042240" "7830164" "6668570" "10908207" "20130285686" "6359264" "7626407" "20020118032" "20140251214" "20050151553" "20060290370" "20190346482" "20200363104") ("8653843" "6515470" "7138811" "7781883" "8970244" "9594113" "10126356" "20060158207" "20090160472" "20110050268" "20140035715" "20150137842" "20160247552" "20190271719" "20200041564" "20210183668" "20210293495" "20220206061" "5239093" "5126656" "5164661" "5315240" "5239093" "5420521" "6389225" "6498899" "6711904" "6825681" "6862405" "6985000" "7311782" "7659738" "7726145" "8343280" "8772682" "8927907" "9307578" "10056225" "10163668" "10955466" "10983145" "7755899" "20020026258" "20040017185" "20130181576" "20180189159" "20190162777" "9841772" "9080820" "7411792" "9310145" "7755899" "10354785" "6184504" "9414526" "6668570" "10908207" "7042240" "7830164" "6359264" "7626407" "9766287" "9494353" "7436059" "5821505" "9291667" "7519880" "8558540" "10656200" "7151388" "7848106" "10656200" "10775408" "11143697" "5239093" "7355428"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 06:55 AM
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L17	8	(PWM (pulse near2 width near2 modulat\$3)) AND L16	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 11:32 AM
L18	31	(pin AND channel\$1)	(US-PGPUB; USPAT;	OR	ON	ON	2023/11/29

		AND L16	USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				01:05 PM
L19	35	(shield EMI radiation) AND L16	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 01:29 PM
L20	8	((indium ADJ foil (graphite)) AND L16	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 03:09 PM
L21	2118	(Advantest near2 Test near2 Solutions).as. (Kabbani near2 Samer).in. (Ferrari near2 Paul).in. (Hiroki near2 Ikeda).in. (Toshiyuki near2 Kiyokawa).in. (Cruzan near2 Greg).in. (Ranganathan near2	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL,	OR	ON	ON	2023/11/29 09:27 PM

L22	9	Karthik).in. (wafer AND semiconductor AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate) AND L21)	PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 09:30 PM
L23	158	(wafer AND semiconductor AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 09:30 PM
L24	29205	(G01R31/2887 G01R31/318511 G01R31/2874 G01R31/2875 G01R31/2877 G01R31/2889).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 09:34 PM
L25	9	(wafer AND semiconductor AND	(US-PGPUB; USPAT; USOCR; FIT (AP, AT,	OR	ON	ON	2023/11/29 09:34 PM

		test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND L24	AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
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PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	3	((wafer AND semiconductor AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate))).clm. AND L24	(US-PGPUB; USPAT)	OR	ON	ON	2023/11/29 09:35 PM

Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	17528002
Filing Date	2021-11-16
First Named Inventor	Samer Kabbani
Art Unit	OPAP
Examiner Name	CENTRAL, DOCKET
Attorney Docket Number	AATS-0107-01U00US

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6515470		2003-02-04	SUZUKI; ET AL	
	2	7138811		2006-11-21	MAHONEY; ET AL	
	3	7781883		2010-08-24	SRI-JAYANTHA; ET AL	
	4	8970244		2015-03-03	DI STEFANO; ET AL	
	5	9594113		2017-03-14	DAVIS; ET AL	
	6	10126356		2018-11-13	BARABI; ET AL	
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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17528002
Filing Date	2021-11-16
First Named Inventor	Samer Kabbani
Art Unit	OPAP
Examiner Name	CENTRAL, DOCKET
Attorney Docket Number	AATS-0107-01U00US

1	20060158207	2006-07-20	REITINGER
2	20090160472	2009-06-25	SEGAWA; ET AL
3	20110050268	2011-03-03	CO; ET AL
4	20140035715	2014-02-06	TAKAHASHI; ET AL
5	20150137842	2015-05-21	MURAKAMI; ET AL
6	20160247552	2016-08-25	KIM; ET AL
7	20190271719	2019-09-05	STERZBACH
8	20200041564	2020-02-06	COJOCNEANU; ET AL
9	20210183668	2021-06-17	CAGLE; ET AL
10	20210293495	2021-09-23	BARAKO; ET AL
11	20220206061	2022-06-30	RANGANATHAN; ET AL

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number		17528002
Filing Date		2021-11-16
First Named Inventor	Samer Kabbani	
Art Unit	OPAP	
Examiner Name	CENTRAL, DOCKET	
Attorney Docket Number	AATS-0107-01U00US	

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	1	109716513	CN		2019-05-03	ROGERS CORP		
	2	110214270	CN		2019-09-06	TOYOTA MOTOR CO LTD		
	3	446682	TW		2001-07-21	SPEEDLINE TECHNOLOGIES INC		
	4	200620596	TW		2006-06-16	ULTRATECH INC		
	5	200628818	TW		2006-08-16	REITINGER ERICH		
	6	201226579	TW		2012-07-01	IND TECH RES INST		
	7	201229535	TW		2012-07-16	NIHON MICRONICS KK		
	8	201323883	TW		2013-06-16	CELADON SYSTEMS INC		
	9	201447325	TW		2014-12-16	SEIKO EPSON CORP		

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

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Filing Date	2021-11-16
First Named Inventor	Samer Kabbani
Art Unit	OPAP
Examiner Name	CENTRAL, DOCKET
Attorney Docket Number	AATS-0107-01U00US

10	201608254	TW	2016-03-01	R&D CIRCUITS INC
11	201712459	TW	2017-04-01	DELTA DESIGN INC
12	201834134	TW	2018-09-16	SEMES CO LTD
13	202043787	TW	2020-12-01	CELERINT LLC
14	202004980	TW	2020-01-16	APPLIED MATERIALS INC

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
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EXAMINER SIGNATURE

Examiner Signature	/TEMILADE S RHODES-VIVOUR/	Date Considered	11/29/2023
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

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Filing Date	2021-11-16
First Named Inventor	Samer Kabbani
Art Unit	OPAP
Examiner Name	CENTRAL, DOCKET
Attorney Docket Number	AATS-0107-01U00US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

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☒ A certification statement is not submitted herewith.

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Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2022-12-07
Name/Print	Anthony C. Murabito	Registration Number	35295

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	17528002
Filing Date	2021-11-16
First Named Inventor	Samer Kabbani
Art Unit	OPAP
Examiner Name	CENTRAL, DOCKET
Attorney Docket Number	AATS-0107-01U00US

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	9841772	B2	2017-12-12	BUCHER	
	2	9080820	B2	2015-07-14	BOLTON	
	3	7411792	B2	2008-08-12	RICHARDS; ET AL	
	4	9310145	B2	2016-04-12	COLONGO; ET AL	
	5	7755899	B2	2010-07-13	STENMARK	
	6	10354785	B2	2019-07-16	YAMAGUCHI; ET AL	
	7	6184504	B1	2001-02-06	CARDELLA	
	8	9414526	B1	2016-08-09	MANN; ET AL	

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Attorney Docket Number		AATS-0107-01U00US

9	6668570		2003-12-30	WALL; et al	
10	10908207		2021-02-02	BARABI; et al	
11	7042240		2006-05-09	LOPEZ; et al	
12	7830164		2010-11-09	EARLE; et al	
13	6359264		2002-03-19	SCHAPER; ET AL	
14	7626407		2009-12-01	KABBANI	
15	9766287		2017-09-19	NARASAKI; ET AL	
16	9494353		2016-11-15	YU; ET AL	
17	7436059		2008-10-14	OUYANG	
18	5821505		1998-10-13	TUSTANIWSKYJ; ET AL	
19	9291667		2016-03-22	ARMSTRONG; ET AL	

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20	7519880		2009-04-14	JOHNSON; ET AL	
21	8558540		2013-10-15	WU; ET AL	
22	10656200		2020-05-19	CRUZAN; ET AL	
23	7151388		2006-12-19	GOPAL; ET AL	
24	7848106		2010-12-07	MERROW	
25	10656200		2020-05-19	CRUZAN; ET AL	
26	10775408		2020-09-15	CARVALHO; ET AL	
27	11143697		2021-10-12	WOLFF	
28	5239093		1993-08-24	CHENG	
29	7355428		2008-04-08	KABBANI; ET AL	

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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20090218087	A1	2009-09-03	OSHIMA	
	2	20210071917	A1	2021-03-11	PEI; ET AL	
	3	20030155939	A1	2003-08-21	LUTZ; ET AL	
	4	20180218926	A1	2018-08-02	STUCKEY; ET AL	
	5	20200371155	A1	2020-11-26	WALCZYK; ET AL	
	6	20050086948	A1	2005-04-28	MILKE-ROJO; ETAL	
	7	20130285686	A1	2013-10-31	MALIK; et al	
	8	20020118032	A1	2002-08-29	NORRIS; ET AL	
	9	20140251214	A1	2014-09-11	CUVALC; ET AL	
	10	20050151553	A1	2005-07-14	KABBANI; ET AL	

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11	20200363104	A1	2020-11-19	MacDonald; et al
12	20060290370	A1	2006-12-28	LOPEZ
13	20190346482	A1	2019-11-14	KIYOKAWA; ET AL
14	20100042355	A1	2010-02-18	AUBE; ET AL
15	20050026476	A1	2005-02-03	MOK; ET AL
16	20050103034	A1	2005-05-19	HAMILTON; ET AL
17	20220082587	A1	2022-03-17	GOPAL; ET AL
18	20150226794	A1	2015-08-13	CHEN
19	20160084880	A1	2016-03-24	LoCicero; ET AL
20	20170102409	A1	2017-04-13	SARHAD; ET AL
21	20190310314	A1	2019-10-10	LIU; ET AL

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22	20150028912	A1	2015-01-29	CHO; ET AL
23	20160351526	A1	2016-12-01	BOYD; ET AL
24	20210396801	A1	2021-12-23	RANGANATHAN; ET AL
25	20220137129	A1	2022-05-05	RANGANATHAN; ET AL
26	20110074080	A1	2011-03-31	DiStefano; ET AL
27	20180024188	A1	2018-01-25	CRUZAN; ET AL
28	20190064254	A1	2019-02-28	BOWYER; ET AL
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	1	2005156172	JP	A	2005-06-16	NIPPON ENG KK ADVANTEST CORP	(with Machine Translation)	×

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2	201636618	TW	A	2014-12-24	QUALITAU INC	☐
3	201504647	TW	A	2013-07-24	ADVANTEST CORP	☐
4	3270261	EP	A1	2018-01-17	ASETEK A/S	☐
5	2008275512	JP	A	2008-11-13	ESPEC CORP	☐
6	2016122039	WO	A1	2016-08-04	UNIQUEST CO LTD.	☐
7	2017112076	WO	A1	2017-06-29	INTEL CORP.	☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
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Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2022-06-08
Name/Print	Anthony C. Murabito	Registration Number	35295

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Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009
109838	7590	12/07/2023	EXAMINER	
Advantest c/o Murabito Hao & Barnes LLP			RHODES-VIVOUR, TEMILADE S	
111 North Market Street			ART UNIT	PAPER NUMBER
Suite 700			2858	
San Jose, CA 95113			NOTIFICATION DATE	DELIVERY MODE
			12/07/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

acmadmin@mhbpatents.com
officeaction@mhbpatents.com

Continuation of Attachment(s) 2) Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date: 11/23/2021, 01/10/2022, 03/10/2022, 04/01/2022, 06/08/2022, 07/08/2022, 07/12/
2022, 09/22/2022, 12/07/2022, 01/03/2023 and 04/12/2023

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis (i.e., changing from AIA to pre-AIA) for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

1. Claim(s) 27-29, 36-38 and 41-45 is/are rejected under 35 U.S.C. 102(a)(2) as being anticipated by Chiang et al. (US PUB 2019/0162777), hereinafter Chiang [Cited BY APPLICANT ON IDS].

2. With respect to claim 27, Chiang discloses a test system (See figure 4 of Chiang) for testing circuits of an integrated circuit semiconductor wafer (See [200] in figure 4 of Chiang), the test system comprising: a test computer (See [400] in figure 4 of Chiang) for testing said circuits by generating signals for input to said circuits (See paragraph [0031] of Chiang), processing output signals from said

circuits and generating a test result thereof (See [450] in view of paragraph [0031] of Chiang); a wafer probe (See [100] in figure 4 of Chiang), coupled to said test computer (See [400] in figure 4 of Chiang), for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer (See paragraph [0031] of Chiang); a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer (See [720] in figure 16 of Chiang) and operable to selectively heat areas of said wafer (See paragraph [0034] of Chiang), wherein said wafer TI layer comprises a plurality of resistive elements traversing said wafer TI layer (See paragraph [0034] of Chiang) and wherein said plurality of resistive elements are operable to selectively heat a plurality of zones of said wafer TI layer that correspond to said areas of said wafer (See paragraph [0034] of Chiang); a cold plate disposed adjacent to said wafer TI layer and operable to cool said wafer (See [710] in figure 16 of Chiang); and a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer during said testing by controlling cooling of said cold plate and by controlling selective heating of said plurality of resistive elements of said wafer TI layer (See [700] in paragraph [0032] of Chiang).

3. With respect to claim 28, Chiang discloses the system as described in Claim 27 wherein positions of said plurality of zones of said wafer TI layer (See paragraph [0034] of Chiang) correspond to a die layout of said wafer (The examiner interprets “a die layout” as the footprint of [200] in figure 4 of Chiang) and wherein further said wafer TI layer is customized for said wafer (See paragraph [0035] of Chiang).

4. With respect to claim 29, Chiang discloses the test system as described in Claim 28 further comprising: a chiller for cooling liquid (See paragraph [0037] of Chiang); a valve for controlling an amount of said liquid flowing to said cold plate (See the pneumatic actuator disclosed in paragraph [0048] of Chiang), wherein said valve is controlled by said thermal controller (See paragraph [0048] of Chiang).

5. With respect to claim 36, Chiang discloses the system as described in Claim 28 wherein each zone of said plurality of zones corresponds to a respective single die of said die layout of said wafer (The examiner interprets the footprint of [200] in figure 4 of Chiang to contain a plurality of infinitesimal unit squares which makes up the surface area of said footprint, in view of paragraph [0034] of Chiang).

6. With respect to claim 37, Chiang discloses the system as described in Claim 28 wherein each zone of said plurality of zones corresponds to a respective plurality of dice of said die layout of said wafer (The examiner interprets the footprint of [200] in figure 4 of Chiang to contain a plurality of infinitesimal unit squares which makes up the surface area of said footprint).

7. With respect to claim 38, Chiang discloses the system as described in Claim 28 wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer (The examiner interprets the footprint of [200] in figure 4 of Chiang to contain a plurality of infinitesimal unit squares which makes up the surface area of said footprint. Furthermore, [200] inherently contains a plurality of die).

8. With respect to claim 41, Chiang discloses a test system (See figure 4 of Chiang) for testing circuits of an integrated circuit semiconductor wafer (See [200] in figure 4 of Chiang), the system comprising: a test computer system (See [400] in figure 4 of Chiang) for testing said circuits by generating signals for input to said circuits (See paragraph [0031] of Chiang), processing output signals from said circuits and generating a test result for said circuits of said wafer (See [450] in view of paragraph [0031] of Chiang); a wafer probe (See [100] in figure 4 of Chiang) for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer (See [100] in figure 4 of Chiang), said wafer probe coupled to communicate with said test computer system (See [400] in figure 4 of Chiang); a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer (See [700] in figure 4 of Chiang which connects to the top side of [200]) and comprising a plurality of discretely controllable thermal zones (See paragraph [0034] of Chiang), wherein each thermal zone is

operable to be discretely (See paragraph [0034] of Chiang) and selectively heated to selectively heat a respective area of said wafer (See paragraph [0034] of Chiang) and wherein further said wafer comprises a die layout comprising a plurality of dice and wherein further positions and shapes of said plurality of discretely controllable thermal zones are customized to said die layout of said wafer (The examiner interprets the footprint of [200] in figure 4 of Chiang to contain a plurality of infinitesimal unit squares which makes up the surface area of said footprint. Furthermore, [200] inherently contains a plurality of die); a cold plate disposed under said wafer TI layer and operable to cool said wafer (See [710] in figure 16 of Chiang); and a thermal controller for selectively heating and maintaining temperatures of areas of said wafer (See [700] in paragraph [0032] of Chiang), during said testing, by controlling cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer (See [700] in paragraph [0032] of Chiang).

9. With respect to claim 42, Chiang discloses the test system as described in Claim 41 wherein each thermal zone of said plurality of discretely controllable thermal zones (See paragraph [0034] of Chiang) corresponds to multiple dice of said die layout of said wafer (The examiner interprets the footprint of [200] in figure 4 of Chiang to contain a plurality of infinitesimal unit squares which makes up the surface area of said footprint. Furthermore, [200] inherently contains a plurality of die).

10. With respect to claim 43, Chiang discloses the test system as described in Claim 41 wherein each thermal zone of said plurality of discretely controllable thermal zones (See paragraph [0034] of Chiang) corresponds to a single die of said die layout of said wafer (The examiner interprets the footprint of [200] in figure 4 of Chiang to contain a plurality of infinitesimal unit squares which makes up the surface area of said footprint. Furthermore, [200] inherently contains a plurality of die).

11. With respect to claim 44, Chiang discloses a test system as described in Claim 41 wherein each die of said die layout of said wafer corresponds to multiple thermal zones (See paragraph [0034] of Chiang) of said plurality of discretely controllable thermal zones of said wafer TI layer (The examiner

interprets the footprint of [200] in figure 4 of Chiang to contain a plurality of infinitesimal unit squares which makes up the surface area of said footprint. Furthermore, [200] inherently contains a plurality of die).

12. With respect to claim 45, Chiang discloses the test system as described in Claim 41 wherein said wafer TI layer comprises a plurality of resistive elements traversing said wafer TI layer and operable to selectively heat and maintain temperatures of said plurality of discretely controllable thermal zones of said wafer TI layer responsive to said thermal controller (See paragraph [0034] of Chiang).

Claim Rejections - 35 USC § 103

13. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis (i.e., changing from AIA to pre-AIA) for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries for establishing a background for determining obviousness under 35 U.S.C. 103 are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claim(s) 35 and 40 is/are rejected under 35 U.S.C. 103 as being unpatentable over Chiang as applied to claim 27 above, and further in view of Narasaki et al. (US PAT 9,766,287), hereinafter Narasak [Cited BY APPLICANT ON IDS].

15. With respect to claim 35, Chiang discloses the test system as described in Claim 27 but fails to disclose further comprising a power supply coupled to provide power to said wafer TI layer and controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said selective heating of said wafer TI layer is based on said PWM signals. However, Narasaki does disclose a power supply coupled to provide power to said wafer TI layer and controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said selective heating of said wafer TI layer is based on said PWM signals (See Col. 2, lines 1-9 of Narasaki). Furthermore, it would have been obvious to one of ordinary skill in the art before the effective filing date of the invention to modify the device disclosed by Chiang to include the features disclosed by Narasaki because doing so ensures precision thermal control of the wafer TI layer.

16. With respect to claim 40, Chiang discloses the system as described in Claim 28 but fails to disclose wherein said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from said PWM signals applied to said plurality of traces. However, Narasaki does disclose wherein said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from said PWM signals applied to said plurality of traces (See Col. 4, lines 51-64 of Narasaki). Furthermore, it would have been obvious to one of ordinary skill in the art before the effective filing

Art Unit: 2858

date of the invention to modify the device disclosed by Chiang to include the features disclosed by Narasaki because doing so provides protection of sensitive equipment from EMI radiation.

17. Claim(s) 39 is/are rejected under 35 U.S.C. 103 as being unpatentable over Chiang as applied to claim 28 above, and further in view of Barabi et al. (US PAT 10,126,356), hereinafter Barabi [Cited BY APPLICANT ON IDS].

18. With respect to claim 39, Chiang discloses the system as described in Claim 28 but fails to disclose further comprising a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical pass through channels which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer. However, Barabi does disclose a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical pass through channels which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer (See Col. 2, lines 55-66 of Barabi). Furthermore, it would have been obvious to one of ordinary skill in the art before the effective filing date of the invention to modify the device disclosed by Chiang to include the feature disclosed by Barabi because doing so ensures a more secure probe contact with the chip surface without sacrificing cooling capabilities.

Allowable Subject Matter

19. Claim 30-34 and 46-48 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20. The following is a statement of reasons for the indication of allowable subject matter:

21. With respect to claim 30, the prior art of record neither shows nor suggests the combination of structural elements comprising: a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and a second TIM layer disposed between said wafer TI layer and said wafer.

22. Claims 31-34 depend from objected to claim 30 and are therefore also objected to.

23. With respect to claim 46, the prior art of record neither shows nor suggests the combination of method steps wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

24. With respect to claim 47, the prior art of record neither shows nor suggests the combination of method steps wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

25. With respect to claim 48, the prior art of record neither shows nor suggests the combination of method steps comprising: a thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer and wherein said TIM layer comprises one of: indium foil; and graphite material.

26. Claims 49-53 are allowed.

27. The following is a statement of reasons for the indication of allowable subject matter:

28. With respect to claim 49, the prior art of record neither shows nor suggests the combination of method steps comprising: selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of said wafer and wherein said thermal interposer comprises a plurality of separately controllable thermal zones and wherein said selectively heating comprises selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones.

29. Claims 50-53 depend from allowed claim 49 and are therefore also allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PUB 2011/0074080 discloses a carrier for holding microelectronic devices.

US PAT 7,781,883 discloses an electronic package with a thermal interposer and method of manufacturing the same.

US PAT 10,163,668 discloses a thermal dynamic response sensing systems for heaters.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TEMILADE S RHODES-VIVOUR whose telephone number is (571)270-5814. The examiner can normally be reached M-F (flex schedule).

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Phan can be reached on 571-272-7924. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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- 30. /TEMILADE S RHODES-VIVOUR/
Examiner, Art Unit 2858
- 31. /JERMELE M HOLLINGTON/
Primary Examiner, Art Unit 2858

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17528002
	Filing Date		2021-11-16
	First Named Inventor	Samer Kabbani	
	Art Unit	2858	
	Examiner Name	TEMILADE S RHODES-VIVOUR	
	Attorney Docket Number	AATS-0107-01U00US	

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	5738531		1998-04-14	BEAMAN; ET AL		
	2	5909657		1999-06-01	ONISHI; ET AL		
	3	6452113		2002-09-17	DIBENE, II; ET AL		
	4	7126217		2006-10-24	CHIU; ET AL		
	5	7646596		2010-01-12	NG		
	6	7929303		2011-04-19	MERROW		
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(Not for submission under 37 CFR 1.99)

Application Number		17528002
Filing Date		2021-11-16
First Named Inventor	Samer Kabbani	
Art Unit		2858
Examiner Name	TEMILADE S RHODES-VIVOUR	
Attorney Docket Number		AATS-0107-01U00US

Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050169733		2005-08-04	DRYNKIN; ET AL	
	2	20110050268		2011-03-03	CO; ET AL	
	3	20150028908		2015-01-29	KUSHNICK; ET AL	
	4	20150168450		2015-06-18	WOODEN; ET AL	
	5	20170059635		2017-03-02	ORCHANIAN;ET AL	
	6	20190064261		2019-02-28	BOWYER; ET AL	
	7	20220128597		2022-04-28	McKENNA; ET AL	
	8	20220128599		2022-04-28	CAMPBELL; ET AL	
	9	20220137092		2022-05-05	RANGANATHAN; ET AL	
	10	20220284982		2022-09-08	RANGANATHAN; ET AL	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

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Examiner Name	TEMILADE S RHODES-VIVOUR
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17528002
Filing Date	2021-11-16
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	TEMILADE S RHODES-VIVOUR
Attorney Docket Number	AATS-0107-01U00US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2024-02-20
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/528,002

RECEIPT DATE / TIME
02/20/2024 02:34:44 PM Z ET

ATTORNEY DOCKET #
AATS-0107-01U00US

Title of Invention

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 5009

FILED BY Missy Isaac

PATENT CENTER # 64378912

FILING DATE 11/16/2021

CUSTOMER # 109838

FIRST NAMED
INVENTOR Samer Kabbani

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Anthony Murabito

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
AATS-0107-01U00US_IDS.pdf	5	Information Disclosure Statement (IDS) Form (SB08)	598 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
AATS-0107-01U00US_IDS.pdf	CBB6F320A8718BF1662ABC287DAAA1AA82537707C9A81AB5 B561120155C49838B33FD79C80AF668A85D31EA830479DC53 011FD700EBF7ADB961B1C23095D354B

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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ELECTRONIC PAYMENT RECEIPT

APPLICATION # 17/528,002	RECEIPT DATE / TIME 02/20/2024 02:34:44 PM Z ET	ATTORNEY DOCKET # AATS-0107-01U00US
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Title of Invention

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5009	FILED BY	Missy Isaac
PATENT CENTER #	64378912	AUTHORIZED BY	Anthony Murabito
CUSTOMER #	109838	FILING DATE	11/16/2021
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Samer Kabbani

Payment Information

PAYMENT METHOD EFT / 055	PAYMENT TRANSACTION ID E20242JE35409784	PAYMENT AUTHORIZED BY Missy Isaac
PRE-AUTHORIZED ACCOUNT 504160	PRE-AUTHORIZED CATEGORY 37 CFR 1.21 (Miscellaneous fees and charges)	

FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
1806	SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT	260.00	1	260.00
TOTAL AMOUNT:				\$260.00

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New Applications Under 35 U.S.C. 111

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 17/528,002		Filing Date 11/16/2021		☐ To be Mailed			
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO											
APPLICATION AS FILED - PART I											
		(Column 1)		(Column 2)							
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A		N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 = *				x \$100 =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 = *				x \$480 =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL					
APPLICATION AS AMENDED - PART II											
		(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	03/15/2024	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 27	Minus	** 53	= 0			x \$100 =		0	
	Independent (37 CFR 1.16(h))	* 6	Minus	*** 6	= 0			x \$480 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
								TOTAL ADD'L FEE		0	
		(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=			x \$0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=			x \$0 =			
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
								TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.								SLIE			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".								/APRIL L. WALKER/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".											
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.											

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/528,002

RECEIPT DATE / TIME
03/15/2024 05:00:36 PM Z ET

ATTORNEY DOCKET #
AATS-0107-01U00US

Title of Invention

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 5009

FILED BY Mina Oliveri

PATENT CENTER # 64708490

FILING DATE 11/16/2021

CUSTOMER # 109838

FIRST NAMED
INVENTOR Samer Kabbani

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Anthony Murabito

Documents

TOTAL DOCUMENTS: 3

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
AATS-0107- 01U00US_20P075US02_AM DT_3-15-2024.pdf	25	-	61 KB
AATS-0107- 01U00US_20P075US02_A MDT_3-15-2024-A....pdf	(1-1) 1	Amendment/Request for Reconsideration-After Non- Final Rejection	26 KB
AATS-0107- 01U00US_20P075US02_A MDT_3-15-2024-CLM.pdf	(2-11) 10	Claims	39 KB
AATS-0107- 01U00US_20P075US02_A MDT_3-15-2024-REM.pdf	(12-25) 14	Applicant Arguments/Remarks Made in an Amendment	46 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
AATS-0107-01U00US_20P075US02_AMDT_3-15-2024.pdf	394C22DF3A8D607394930C81DC61592B0F740732C0A050B0EC5B9B2929EE528703948C1BC20DAD6B963672B42AF3C7AE3B1A9016CC52F6FD574DE4201F3C26F7
AATS-0107-01U00US_20P075US02_AMDT_3-15-2024-A....pdf	5B03699D805EDE2D34FD41320F486ECF778B2C2F99C1590D04E9D6406D188034F49603E9F7CD882A5498213A8E0A5F89C99CBD7FEF553F0424E25202E3806CA8
AATS-0107-01U00US_20P075US02_AMDT_3-15-2024-CLM.pdf	9CE423EF212205298D9BEC1BEEDA661AA7FA122CC60CDB3FC3249AF4FD0D6DB7ABBAEB6159C11E928105682E59736B50D7EDFBDB9F82220D8035D56E7DD85FD6
AATS-0107-01U00US_20P075US02_AMDT_3-15-2024-REM.pdf	EB3B0D340DE2F60F58386D2B654F1E46CBC2E3F91174DF5652CE03AF21BEE7A164549015685811F06A68B3951458DD8452BA329320E551AA336D7F1153A3970F

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/528,002	03/15/2024 05:00:36 PM Z ET	AATS-0107-01U00US

Title of Invention

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5009	FILED BY	Mina Oliveri
PATENT CENTER #	64708490	AUTHORIZED BY	Anthony Murabito
CUSTOMER #	109838	FILING DATE	11/16/2021
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Samer Kabbani

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
EFT / 055	E20243EH18118841	Mina Oliveri
PRE-AUTHORIZED ACCOUNT	PRE-AUTHORIZED CATEGORY	
504160	37 CFR 1.17 (Patent application and reexamination processing fees); 37 CFR 1.19 (Document supply fees); 37 CFR 1.20 (Post Issuance fees); 37 CFR 1.21 (Miscellaneous fees and charges)	

FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
1251	EXTENSION FOR RESPONSE WITHIN FIRST MONTH	220.00	1	220.00
TOTAL AMOUNT:				\$220.00

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement

AEM Americas, Inc. - 1018

Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kabbani et al.

Serial: 17/528,002 Confirmation No.: 5009

Filed: 11/16/2021 Group Art Unit: 2858

Examiner: Rhodes-Vivour, Temilade S.

For: Wafer Scale Active Thermal Interposer for Device Testing

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

AMENDMENT and RESPONSE

Dear Examiner Rhodes-Vivour:

In response to the Official Action mailed 12/7/2023, please enter the indicated amendments and the following remarks for filing in the above captioned patent application.

In the Claims:

1-26 (cancelled)

27. (Previously Presented) A test system for testing circuits of an integrated circuit semiconductor wafer, the test system comprising:

a test computer for testing said circuits by generating signals for input to said circuits, processing output signals from said circuits and generating a test result thereof;

a wafer probe, coupled to said test computer, for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer;

a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer, wherein said wafer TI layer comprises a plurality of resistive elements traversing said wafer TI layer and wherein said plurality of resistive elements are operable to selectively heat a plurality of zones of said wafer TI layer that correspond to said areas of said wafer;

a cold plate disposed adjacent to said wafer TI layer and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer during said testing by controlling

cooling of said cold plate and by controlling selective heating of said plurality of resistive elements of said wafer TI layer.

28. (Previously Presented) The system as described in Claim 27 wherein positions of said plurality of zones of said wafer TI layer correspond to a die layout of said wafer and wherein further said wafer TI layer is customized for said wafer.

29. (currently amended) The test system as described in Claim 28 further comprising:
| a chiller for cooling liquid; and
| a valve for controlling an amount of said liquid flowing to said cold plate, wherein said valve is controlled by said thermal controller.

30. (Previously Presented) The system as described in Claim 28 further comprising:
| a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and
| a second TIM layer disposed between said wafer TI layer and said wafer.

31. (Previously Presented) The system as described in Claim 30 wherein said first and second TIM layers comprise indium foil.

32. (Previously Presented) The system as described in Claim 30 wherein said first and second TIM layers comprise graphite material.

33. (Previously Presented) The system as described in Claim 30 further comprising:

a first vacuum valve for establishing suction for securing said wafer to said wafer TI layer;

a second vacuum valve for establishing suction for securing said wafer TI layer to said cold plate; and

a vacuum pump coupled to both said first and second vacuum valves.

34. (Previously Presented) The system as described in Claim 33 further comprising:

a first blow-off valve for controlling air to release said wafer from said wafer TI layer;

a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and

a source of air coupled to both said first and second blow-off valves.

35. (Previously Presented) The test system as described in Claim 27 further comprising a power supply coupled to provide power to said wafer TI

layer and controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said selective heating of said wafer TI layer is based on said PWM signals.

36. (Previously Presented) The system as described in Claim 28 wherein each zone of said plurality of zones corresponds to a respective single die of said die layout of said wafer.

37. (Previously Presented) The system as described in Claim 28 wherein each zone of said plurality of zones corresponds to a respective plurality of dice of said die layout of said wafer.

38. (Previously Presented) The system as described in Claim 28 wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.

39. (Previously Presented) The system as described in Claim 28 further comprising a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical pass through channels which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer.

40. (currently amended) The system as described in Claim ~~28-35~~
wherein said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from said PWM signals applied to said plurality of traces.

41. (Previously Presented) A test system for testing circuits of an integrated circuit semiconductor wafer, the system comprising:

a test computer system for testing said circuits by generating signals for input to said circuits, processing output signals from said circuits and generating a test result for said circuits of said wafer;

a wafer probe for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer, said wafer probe coupled to communicate with said test computer system;

a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer and wherein further said wafer comprises a die layout comprising a plurality of dice and wherein further positions and shapes of said plurality of discretely controllable thermal zones are customized to said die layout of said wafer;

a cold plate disposed under said wafer TI layer and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of areas of said wafer, during said testing, by controlling cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer.

42. (Previously Presented) The test system as described in Claim 41 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to multiple dice of said die layout of said wafer.

43. (Previously Presented) The test system as described in Claim 41 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to a single die of said die layout of said wafer.

44. (Previously Presented) A test system as described in Claim 41 wherein each die of said die layout of said wafer corresponds to multiple thermal zones of said plurality of discretely controllable thermal zones of said wafer TI layer.

45. (Previously Presented) The test system as described in Claim 41 wherein said wafer TI layer comprises a plurality of resistive elements

traversing said wafer TI layer and operable to selectively heat and maintain temperatures of said plurality of discretely controllable thermal zones of said wafer TI layer responsive to said thermal controller.

46. (Previously Presented) The test system as described in Claim 41 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and

while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

47. (Previously Presented) The test system as described in Claim 41 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and

while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

48. (Previously Presented) The test system as described in Claim 41 further comprising: a thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer and wherein said TIM layer comprises one of: indium foil; and graphite material.

49. (currently amended) A method of testing circuits of an integrated circuit semiconductor wafer, the method comprising:

testing said circuits of said wafer by using a test computer system wherein said testing comprises:

generating signals for input to said circuits;
processing output signals from said circuits; and
generating a test result for said circuits; and

in conjunction with performing said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of said wafer and wherein said thermal interposer

comprises a plurality of separately controllable thermal zones and wherein said selectively heating comprises selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones.

50. (Previously Presented) The method as described in Claim 49 wherein said wafer comprises a die layout and wherein further positions and shapes of said plurality of separately controllable thermal zones of said thermal interposer layer are customized to said die layout.

51. (Previously Presented) The method as described in Claim 50 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises:

bringing a first thermal zone of said plurality of separately controllable thermal zones to a testing temperature; and

while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of separately controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

52. (Previously Presented) The method as described in Claim 50 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises:

bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and

while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

53. (Previously Presented) The method of Claim 50 wherein said plurality of separately controlled thermal zones comprise a plurality of resistive elements and wherein further said selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones comprises said thermal controller selectively energizing said plurality of resistive elements during said testing.

REMARKS

Claims 27-53 are pending in the present application. Claims 1-26 were previously cancelled. Claims 29, 40, and 49 are amended herein. No new matter is added. Applicants respectfully request reconsideration of the present application in view of the indicated amendments and the following remarks.

Allowable Matter

The Office Action indicates that Claims 49-53 are allowed, and that Claims 30-34 and 46-48 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants thank the Examiner for indicating allowable matter.

Examiner Interview Summary

Applicants' under-signed representative and Examiner Rhodes-Vivour conducted an Examiner Interview via telephone on March 13, 2024. Claim 1 and the cited reference Chiang were discussed in conjunction with a submitted agenda.

The Examiner indicated that the arguments presented during the Interview were persuasive. The Examiner indicated a further search may be warranted.

Applicants thank the Examiner for the Interview.

Inherency

At item 9 on page 5, the Rejection alleges, “Furthermore, [200] [of Chiang] inherently contains a plurality of die.” This statement is repeated throughout the Rejection. Applicants traverse.

Per MPEP 2112(IV), the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 U.S.P.Q.2d 1955, 1957 (Fed. Cir. 1993). “Inherency... may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.” *In re Robertson*, 169 F.3d 743, 745, 49 U.S.P.Q.2d 1949, 1950-51 (Fed. Cir. 1999).

“In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.” *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). Applicants respectfully assert that the Rejection fails to explain any such basis in fact and/or technical reasoning to reasonably support the allegation of inherency.

Chiang teaches that DUT 200 is “an Integrated Circuit (IC) or other electronic device” [0002]. As is known to those of ordinary skill in the art, an IC may comprise a single die. A device described as “an Integrated Circuit (IC)” does not inherently comprise multiple dice.

In sum, the Rejection fails to provide a basis in fact and/or technical reasoning to establish that Chiang DUT “[200] inherently contains a plurality of die,” as alleged. Moreover, the Rejection fails to demonstrate that Chiang must always test multiple dice, and further fails to establish that Chiang cannot be used with an IC consisting of a single die, as required by the Rejection’s alleged inherency.

Accordingly, the Rejection’s finding of “inherency” is unsupported and improper. The rejections of Claims 36, 37, 38, 41, 42, 43, and 44 are specifically

based on this alleged inherency. Accordingly, at least these Claims overcome the rejections of record. To the extent that any other Claims are rejected based on this alleged inherency, such claims also overcome the rejections of record.

Infinitesimal Unit Squares

At item 5 on page 4, the Rejection states:

The examiner interprets the footprint of [200] in figure 4 of Chiang to contain a plurality of infinitesimal unit squares which makes up the surface area of said footprint, in view of paragraph [0034] of Chiang.

Similar statements are repeatedly made throughout the Rejection. Applicants traverse. The rejection uses this interpretation to improperly conclude that DUT 200 comprises a plurality of dice.

However, there is no teaching or suggestion in Chiang that DUT 200 comprises multiple dice. Chiang teaches that DUT 200 is “an Integrated Circuit (IC) or other electronic device” [0002]. As is known to those of ordinary skill in the art, an IC may consist of a single die. It is noted that the Rejection fails to cite a portion of Chiang alleged to teach or suggest that DUT 200 comprises multiple dice. The cited paragraph [0034] does not discuss DUT 200.

As is known to those of ordinary skill in the art, a die is a small block of semiconducting material on which a given functional integrated circuit is fabricated. A die is a physical item, and thus cannot be of “infinitesimal” size. Under the Rejection’s interpretation, any device under test would comprise an infinite number of die. Moreover, in rejecting Claim 36 at item 5 on page 4, for example, the Rejection appears to allege an impossibility, namely that Chang teaches an infinitely large number of heating zones for selectively heating an infinitely large number of infinitesimally small dice.

For at least this reason, Applicants assert that all rejections based on the Rejection’s interpretation of “infinitesimal unit squares” are overcome. The rejections of Claims 36, 37, 38, 41, 42, 43, and 44 are specifically based on this improper interpretation. Accordingly, at least these Claims overcome the rejections of record. To the extent that any other Claims are rejected based on this rationale, such claims also overcome the rejections of record.

35 U.S.C. § 102

Claims 27-29, 36-38, and 41-45 stand rejected under 35 U.S.C. § 102(a)(2) as allegedly unpatentable over Chiang et al. (US Patent Publication 2019/0162777, “Chiang”). Applicants respectfully assert that the instant Claims overcome the rejections of record for at least the following reasons.

With respect to independent Claim 27, Chiang fails to teach or suggest the claimed limitations of:

a wafer probe, coupled to said test computer, for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer

as recited by Claim 27.

As best understood, the Rejection cites “socket 100” as allegedly suggesting these recited elements. However, “socket 100” is not a “wafer probe,” as recited. Namely, Chiang teaches that socket 100:

is adapted to receive the DUT 200, is mounted on the PCB 300 to electrically connect the contacts on the PCB 300 to corresponding contacts on the DUT 200. [0002].

Socket 200 is not taught or suggested to contact a surface of a wafer, as recited. The term “socket” is not generally used to describe a contacting mechanism for a wafer. Devices for contacting a wafer are differentiated from the taught “socket” by their nomenclature, e.g., “wafer probe,” as recited. A “wafer probe,” as recited, is not generally “mounted to (a) PCB.” As DUT 200 is taught to be

“an Integrated Circuit (IC)...” [0002], one of ordinary skill in the art would understand the taught socket 200 to be a socket for accepting a packaged IC. *See*, for example, https://en.wikipedia.org/wiki/Dual_in-line_package#Socket, which illustrates a common type of IC socket, as would be understood in view of Chiang. While there may be other types of sockets, in general, and in Chiang, the socket 200 is neither intended nor taught to be a “wafer probe,” as recited.

For at least this reason, Claim 1 overcomes the rejections of record, and is patentable over the cited art.

In addition with respect to independent Claim 27, Chiang fails to teach or suggest the claimed limitations of:

a wafer thermal interposer (TI) layer ... operable to selectively heat areas of said wafer, ... operable to selectively heat a plurality of zones of said wafer TI layer that correspond to said areas of said wafer

as recited by Claim 27.

As best understood, the Rejection cites “thermal plate 720” as allegedly suggesting these claimed limitations. However, thermal plate 720 is taught to heat the entire bottom of the DUT 200. Thermal plate 720 does not selectively

heat areas of a wafer, as recited. For example, Chiang teaches one temperature for the thermal plate 720, and one temperature for the DUT 200.

When the DUT 200 is being tested by the test system, a top surface of the DUT 200 makes physical contact with the bottom surface of the thermal plate 720, so that heat is transferable between them. Thus, the temperature being sensed by the temperature sensor 724 is indicative of the temperature of the DUT 200 after the respective temperatures of the bottom surface of the thermal plate 720 and the top surface of the DUT 200 stabilize to the same temperature. [0035, emphasis added]

Further,

During testing of the DUT 200, the thermal forcing system 900 controls the temperature of the DUT 200, as sensed by one or more temperature sensors 724, so that the temperature of the DUT 200 is raised to, lowered to, and/or maintained at a setpoint temperature. [0032, emphasis added].

Accordingly, Chiang teaches one heating element that applies heat to the entire DUT 200 to maintain a single setpoint temperature, and thus fails to teach or suggest the instant claimed limitations of “selectively heat a plurality of zones of said wafer TI layer that correspond to said areas of said wafer,” as recited.

For at least this additional reason, Claim 27 overcome the rejections of record, and is patentable over the cited art.

Further with respect to independent Claim 27, Chiang fails to teach or suggest the claimed limitations of:

a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer during said testing by controlling cooling of said cold plate and by controlling selective heating of said plurality of resistive elements of said wafer TI layer

as recited by Claim 27.

As previously presented, Chiang teaches control of one single temperature for the entire thermal plate 720 and the entire DUT 200. Chiang teaches:

During testing of the DUT 200, the thermal forcing system 900 controls the temperature of the DUT 200, as sensed by one or more temperature sensors 724, so that the temperature of the DUT 200 is raised to, lowered to, and/or maintained at a setpoint temperature. [0032, emphasis added].

In teaching one single temperature for the entire DUT, Chiang cannot and does not teach or suggest the claimed limitations of:

a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer during said testing by controlling cooling of said cold plate and by controlling selective heating of said plurality of resistive elements of said wafer TI layer

as recited by Claim 27.

For at least this further reason, Claim 27 overcomes the rejections of record and is patentable over the cited art.

Dependent Claims 28-40, including presently rejected Claims 28, 29, and 36-38 overcome the rejections of record at least by virtue of their dependence from Claim 27, and are patentable over the cited art.

With respect to independent Claim 41, Claim 41 overcomes the rejections of record for at least the rationales previously presented with respect to Claim 27, *mutatis mutandis*.

As previously presented, Chiang fails to teach or suggest the claimed limitations of:

a wafer probe for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer

as recited by Claim 41.

In contrast, Chiang teaches an IC socket, with no application to wafers taught or understood by those of ordinary skill in the art.

As previously presented, Chiang fails to teach or suggest the claimed limitations of:

a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer

as recited by Claim 41.

In contrast, Chiang teaches one heater (thermal plate 720) for keeping the thermal plate and the entire DUT at one single temperature.

As previously presented, Chiang fails to teach or suggest the claimed limitations of:

a thermal controller for selectively heating and maintaining temperatures of areas of said wafer, during said testing, by controlling

cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer.

as recited by Claim 41.

In contrast, Chiang teaches one heater (thermal plate 720) for keeping the thermal plate and the entire DUT at one single temperature.

Accordingly, Chiang fails to teach or suggest at least these multiple claimed limitations. For at least this reason, Claim 41 overcomes the rejections of record, and is patentable over the cited art.

Claims 42-48, including presently rejected Claims 42-45, overcome the rejections of record at least by virtue of their dependence from Claim 41, and are patentable over the cited art.

35 U.S.C. § 103

Dependent Claims 35 and 40 are rejected under 35 U.S.C. 103 as allegedly being unpatentable over Chiang as applied to claim 27 above, and further in view of Narasaki et al. (US Patent 9,766,287, “Narasaki”).

Claims 35 and 40 overcome the rejections of record at least by virtue of their dependence from Claim 27, and are patentable over the cited art.

Claim 39 is rejected under 35 U.S.C. 103 as allegedly being unpatentable over Chiang as applied to claim 28 above, and further in view of Barabi et al. (US Patent 10,126,356, "Barabi"). Applicants respectfully assert that the instant Claim overcomes the rejections of record for at least the following reasons.

Claim 39 overcomes the rejections of record at least by virtue of its dependence from Claim 27, and is patentable over the cited art.

CONCLUSION

Claims 27-53 are pending in the present application. Applicants understand all Claims to be in condition for allowance, and such allowance is earnestly sought.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 504160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Date: March 15, 2024

/Anthony C. Murabito/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009
109838	7590	03/28/2024	EXAMINER	
Advantest c/o Murabito Hao & Barnes LLP			RHODES-VIVOUR, TEMILADE S	
111 North Market Street			ART UNIT	PAPER NUMBER
Suite 700			2858	
San Jose, CA 95113			NOTIFICATION DATE	DELIVERY MODE
			03/28/2024	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

acmadmin@mhbpatents.com
officeaction@mhbpatents.com
tbettencourt@mhbpatents.com

<i>Applicant-Initiated Interview Summary</i>	Application No. 17/528,002	Applicant(s) Kabbani et al.		
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858	AIA (First Inventor to File) Status Yes	Page 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	Title	Type
TEMILADE S RHODES-VIVOUR	Examiner	Telephonic
Anthony C. Murabito (Reg. No. 35,295)	Attorney of Record	

Date of Interview: 13 March 2024

Issues Discussed:

35 U.S.C. 102

The attorney of record presented arguments directed to differences between the Chiang reference and the instant application which were convincing. The examiner conceded that the arguments overcome the rejection of record.

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858	/HUY Q PHAN/ Supervisory Patent Examiner, Art Unit 2858
<p>Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04</p> <p>Please further see: MPEP 713.04 Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b) 37 CFR § 1.2 Business to be transacted in writing</p>	

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Notice of References Cited	Application/Control No. 17/528,002		Applicant(s)/Patent Under Reexamination Kabbani et al.	
	Examiner TEMILADE S RHODES-VIVOUR		Art Unit 2858	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date YYYY-MM-DD	Name	CPC Classification	US Classification
*	A	US-20150035554-A1	2015-02-05	Dang; Bing	G01R31/2607	428/408
*	B	US-20100155888-A1	2010-06-24	Christo; Michael Anthony	H01L22/14	257/532
*	C	US-20150226794-A1	2015-08-13	CHEN; Chien-Ming	G01R1/0433	324/756.02
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date YYYY-MM-DD	Country	Name	CPC Classification
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	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in YYYY-MM-DD format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
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11	38	✓	=							
12	39	✓	=							
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15	41	✓	=							
16	42	✓	=							

<i>Index of Claims</i> 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
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CLAIM		DATE								
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26	52	=	=							
27	53	=	=							

<i>Issue Classification</i> 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858

CPC						
Symbol					Type	Version
G01R	/	31	/	2887	F	2013-01-01
H01L	/	23	/	473	I	2013-01-01
G01R	/	31	/	318511	I	2013-01-01
F28F	/	2260	/	02	A	2013-01-01

CPC Combination Sets					
Symbol				Type	Set
	/		/		

TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858 (Assistant Examiner)	05 April 2024 (Date)	Total Claims Allowed: 27	
/JERMELE M HOLLINGTON/ Primary Examiner, Art Unit 2858 (Primary Examiner)	16 April 2024 (Date)	O.G. Print Claim(s) 27	O.G. Print Figure 1

Issue Classification 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G01R31/28	/	31	/ 28
H01L23/473	/	23	/ 473
G01R31/3185	/	31	/ 3185
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
324	754.07

CROSS REFERENCES(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858 (Assistant Examiner)	05 April 2024 (Date)	Total Claims Allowed: 27	
/JERMELE M HOLLINGTON/ Primary Examiner, Art Unit 2858 (Primary Examiner)	16 April 2024 (Date)	O.G. Print Claim(s) 27	O.G. Print Figure 1

Issue Classification 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS															
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-	9	-	18	1	27	9	36	19	45						

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858 (Assistant Examiner)	05 April 2024 (Date)	Total Claims Allowed: 27	
/JERMELE M HOLLINGTON/ Primary Examiner, Art Unit 2858 (Primary Examiner)	16 April 2024 (Date)	O.G. Print Claim(s) 27	O.G. Print Figure 1

Search Notes 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858

CPC - Searched*		
Symbol	Date	Examiner
G01R31/2887 G01R31/318511 G01R31/2874 G01R31/2875 G01R31/2877 G01R31/2889	11/29/2023	TRV
G01R31/2887 G01R31/318511 G01R31/2874 G01R31/2875 G01R31/2877 G01R31/2889	04/05/2024	TRV

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Conducted InnovationQ search	11/29/2023	TRV
Conducted PE2E keyword, cpc, inventor/assignee names and interference searches.	11/29/2023	TRV
Searches updated	04/05/2024	TRV

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858	/JERMELE M HOLLINGTON/ Primary Examiner, Art Unit 2858
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<i>Search Notes</i> 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	G01R31/2887 G01R31/318511 G01R31/2874 G01R31/2875 G01R31/2877 G01R31/2889	11/29/2023	TRV
	G01R31/2887 G01R31/318511 G01R31/2874 G01R31/2875 G01R31/2877 G01R31/2889	04/05/2024	TRV

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858	/JERMELE M HOLLINGTON/ Primary Examiner, Art Unit 2858
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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	6	"17528002"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/14 01:31 PM
L2	9657	("20220276301" "202234082" I813074 "20220068939" "11774492" "20220326299" "11567119" "20220187361" "20230129112" "20220268831" "11609266" "20220079467" "11754620" "20220178991" "20220079465" "202229914" "20230296667" I807516 "202240186" I806272 "20220097269" "11573262" "20220206061" "20230103082" "202242431" I816250 "1461628" "20040065310" "1940213" "2003058264" "1461628" "20100052714" "20050206397" "7863915" "7579847" "6891385" "20030122567" "4484520" "2005514627" "20220299563" "202217345"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/27 04:01 PM

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L4	157	(wafer AND semiconductor AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/27 06:31 PM
L5	148	(wafer AND semiconductor AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB,	OR	ON	ON	2023/11/28 08:16 AM

		AND (cold ADJ plate)) AND heat\$3	HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L6	110	(wafer AND (semiconductor IC (intergrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND computer	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/28 01:56 PM
L7	123	(wafer AND (semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND computer	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/28 03:01 PM
L8	13	L7 NOT L6	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2023/11/28 03:02 PM

L9	171	(wafer AND (semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND (computer process\$3)	IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/28 10:18 PM
L10	48	L9 NOT L7	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/28 10:19 PM
L11	1749756	(wafer (semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND (computer process\$3)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 12:05 AM
L12	427067	(wafer (semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS,	OR	ON	ON	2023/11/29 12:10 AM

		AND (cold ADJ plate)) AND heat\$3 AND (computer)	IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L13	123	((semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND (computer) AND wafer	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 12:11 AM
L14	194	((wafer die semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND (computer)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 12:15 AM
L15	2054	("8653843" "6515470" "7138811" "7781883" "8970244" "9594113" "10126356" "20060158207" "20090160472" "20110050268" "20140035715" "20150137842" "20160247552" "20190271719" "20200041564" "20210183668" "20210293495" "20220206061" "5239093" "5126656"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 06:54 AM

		"5164661" "5315240" "5239093" "5420521" "6389225" "6498899" "6711904" "6825681" "6862405" "6985000" "7311782" "7659738" "7726145" "8343280" "8772682" "8927907" "9307578" "10056225" "10163668" "10955466" "10983145" "7755899" "20020026258" "20040017185" "20130181576" "20180189159" "20190162777" "9841772" "9080820" "7411792" "9310145" "7755899" "10354785" "6184504" "9414526" "6668570" "10908207" "7042240" "7830164" "6359264" "7626407" "9766287" "9494353" "7436059" "5821505" "9291667" "7519880" "8558540" "10656200" "7151388" "7848106" "10656200" "10775408" "11143697" "5239093" "7355428" "20090218087" "20210071917" "20030155939" "20180218926" "20200371155" "20050086948" "20130285686" "20020118032" "20140251214" "20050151553" "20200363104" "20060290370" "20190346482" "20100042355" "20050026476" "20050103034" "20220082587" "20150226794" "20160084880" "20170102409" "20190310314" "20150028912" "20160351526" "20210396801" "20220137129" "20110074080" "20180024188"					
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L16	355	"20190064254" "20220044084" "5821505" "7042240" "7830164" "6668570" "10908207" "20130285686" "6359264" "7626407" "20020118032" "20140251214" "20050151553" "20060290370" "20190346482" "20200363104") ("8653843" "6515470" "7138811" "7781883" "8970244" "9594113" "10126356" "20060158207" "20090160472" "20110050268" "20140035715" "20150137842" "20160247552" "20190271719" "20200041564" "20210183668" "20210293495" "20220206061" "5239093" "5126656" "5164661" "5315240" "5239093" "5420521" "6389225" "6498899" "6711904" "6825681" "6862405" "6985000" "7311782" "7659738" "7726145" "8343280" "8772682" "8927907" "9307578" "10056225" "10163668" "10955466" "10983145" "7755899" "20020026258" "20040017185" "20130181576" "20180189159" "20190162777" "9841772" "9080820" "7411792" "9310145" "7755899" "10354785" "6184504" "9414526" "6668570" "10908207" "7042240" "7830164" "6359264" "7626407" "9766287" "9494353" "7436059" "5821505" "9291667" "7519880" "8558540" "10656200" "7151388" "7848106"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 06:55 AM
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L17	8	"10656200" "10775408" "11143697" "5239093" "7355428" "20090218087" "20210071917" "20030155939" "20180218926" "20200371155" "20050086948" "20130285686" "20020118032" "20140251214" "20050151553" "20200363104" "20060290370" "20190346482" "20100042355" "20050026476" "20050103034" "20220082587" "20150226794" "20160084880" "20170102409" "20190310314" "20150028912" "20160351526" "20210396801" "20220137129" "20110074080" "20180024188" "20190064254" "20220044084" "5821505" "7042240" "7830164" "6668570" "10908207" "20130285686" "6359264" "7626407" "20020118032" "20140251214" "20050151553" "20060290370" "20190346482" "20200363104").pn. (PWM (pulse near2 width near2 modulat\$3)) AND L16	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO;	OR	ON	ON	2023/11/29 11:32 AM
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L18	31	(pin AND channel\$1) AND L16	JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 01:05 PM
L19	35	(shield EMI radiation) AND L16	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 01:29 PM
L20	8	((indium ADJ foil) (graphite)) AND L16	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 03:09 PM
L21	2118	(Advantest near2 Test near2 Solutions).as. (Kabbani near2 Samer).in. (Ferrari near2 Paul).in. (Hiroki near2 Ikeda).in.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 09:27 PM

L22	9	(Toshiyuki near2 Kiyokawa).in. (Cruzan near2 Greg).in. (Ranganathan near2 Karthik).in.	HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 09:30 PM
L23	158	(wafer AND semiconductor AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate) AND L21)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 09:30 PM
L24	29205	(G01R31/2887 G01R31/318511 G01R31/2874 G01R31/2875 G01R31/2877 G01R31/2889).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 09:34 PM

L25	9	(wafer AND semiconductor AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND L24	IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 09:34 PM
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PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	3	((wafer AND semiconductor AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate))).clm. AND L24	(US-PGPUB; USPAT)	OR	ON	ON	2023/11/29 09:35 PM

Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17528002
	Filing Date		2021-11-16
	First Named Inventor	Samer Kabbani	
	Art Unit	2858	
	Examiner Name	TEMILADE S RHODES-VIVOUR	
	Attorney Docket Number	AATS-0107-01U00US	

U.S.PATENTS							Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	5738531		1998-04-14	BEAMAN; ET AL		
	2	5909657		1999-06-01	ONISHI; ET AL		
	3	6452113		2002-09-17	DIBENE, II; ET AL		
	4	7126217		2006-10-24	CHIU; ET AL		
	5	7646596		2010-01-12	NG		
	6	7929303		2011-04-19	MERROW		
	7	11493551		2022-11-08	RANGANATHAN; ET AL		
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STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		17528002
Filing Date		2021-11-16
First Named Inventor	Samer Kabbani	
Art Unit		2858
Examiner Name	TEMILADE S RHODES-VIVOUR	
Attorney Docket Number		AATS-0107-01U00US

Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050169733		2005-08-04	DRYNKIN; ET AL	
	2	20110050268		2011-03-03	CO; ET AL	
	3	20150028908		2015-01-29	KUSHNICK; ET AL	
	4	20150168450		2015-06-18	WOODEN; ET AL	
	5	20170059635		2017-03-02	ORCHANIAN;ET AL	
	6	20190064261		2019-02-28	BOWYER; ET AL	
	7	20220128597		2022-04-28	McKENNA; ET AL	
	8	20220128599		2022-04-28	CAMPBELL; ET AL	
	9	20220137092		2022-05-05	RANGANATHAN; ET AL	
	10	20220284982		2022-09-08	RANGANATHAN; ET AL	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17528002
Filing Date	2021-11-16
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	TEMILADE S RHODES-VIVOUR
Attorney Docket Number	AATS-0107-01U00US

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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		☐

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EXAMINER SIGNATURE

Examiner Signature	/TEMILADE S RHODES-VIVOUR/	Date Considered	04/05/2024
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17528002
Filing Date	2021-11-16
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	TEMILADE S RHODES-VIVOUR
Attorney Docket Number	AATS-0107-01U00US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2024-02-20
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Bibliographic Data

Application No: 17/528,002

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged:

/TEMILADE S RHODES-
VIVOUR/

Examiner's Signature

Initials

Title:

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE
TESTING

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/16/2021	324	2858	AATS-0107-01U00US
RULE			

APPLICANTS

Advantest Test Solutions, Inc., San Jose, CA,

INVENTORS

Samer Kabbani, San Jose, CA, UNITED STATES

Paul Ferrari, San Jose, CA, UNITED STATES

Ikeda Hiroki, San Jose, CA, UNITED STATES

Kiyokawa Toshiyuki, San Jose, CA, UNITED STATES

Greg Cruzan, San Jose, CA, UNITED STATES

Karthik Ranganathan, San Jose, CA, UNITED STATES

CONTINUING DATA

This application has PRO of 63115813 11/19/2020

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

11/30/2021

STATE OR COUNTRY

UNITED STATES

ADDRESS

Advantest c/o Murabito Hao & Barnes LLP

111 North Market Street

Suite 700

San Jose, CA 95113

UNITED STATES

FILING FEE RECEIVED

\$2,580



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

109838 7590 04/29/2024
Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

EXAMINER	
RHODES-VIVOUR, TEMILADE S	
ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 04/29/2024

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009

TITLE OF INVENTION: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	07/29/2024

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009

TITLE OF INVENTION: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	07/29/2024

EXAMINER	ART UNIT	CLASS-SUBCLASS
RHODES-VIVOUR, TEMILADE S	2858	324-754070

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via the USPTO patent electronic filing system ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009
EXAMINER				
RHODES-VIVOUR, TEMILADE S				
ART UNIT			PAPER NUMBER	
2858				
DATE MAILED: 04/29/2024				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013).

<https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf>

Routine uses of the information in this record may include disclosure to:

- 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
- 2) a federal, state, local, or international agency, in response to its request;
- 3) a contractor of the USPTO having need for the information in order to perform a contract;
- 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;
- 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;
- 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;
- 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;
- 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));
- 9) the Office of Personnel Management (OPM) for personnel research purposes; and
- 10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Notice of Allowability	Application No. 17/528,002	Applicant(s) Kabbani et al.	
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the arguments filed on 03/15/2024.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 27-53. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov**.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>02/20/2024</u> . 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
---	--

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858	/JERMELE M HOLLINGTON/ Primary Examiner, Art Unit 2858
---	---

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Response to Arguments

1. Applicant's arguments, see pages 1-14 of the remarks, filed 03/15/2024, with respect to claims 27-53 have been fully considered and are persuasive. The 35 USC 102 rejection of claims 27-29, 36-38, 41-45 and the 35 USC 103 rejection of claims 35, 39 and 40 have been withdrawn.

Allowable Subject Matter

2. Claims 27-53 are allowed.
3. The following is an examiner's statement of reasons for allowance:
4. With respect to claim 27, the prior art of record neither shows nor suggests the combination of structural elements comprising a test computer for testing said circuits by generating signals for input to said circuits, processing output signals from said circuits and generating a test result thereof; a wafer probe, coupled to said test computer, for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer: a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer, wherein said wafer TI layer comprises a plurality of resistive elements traversing said wafer TI layer and wherein said plurality of resistive elements are operable to selectively heat a plurality of zones of said wafer TI layer that correspond to said areas of said wafer; a cold plate disposed adjacent to said wafer TI layer and operable to cool said wafer; and a thermal controller for selectively heating and maintaining

temperatures of said areas of said wafer during said testing by controlling cooling of said cold plate and by controlling selective heating of said plurality of resistive elements of said wafer TI layer.

5. Claims 28-40 depend from allowed claim 27 and are therefore also allowed.

6. With respect to claim 41, the prior art of record neither shows nor suggests the combination of structural elements comprising a wafer probe for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer, said wafer probe coupled to communicate with said test computer system; a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer and wherein further said wafer comprises a die layout comprising a plurality of dice and wherein further positions and shapes of said plurality of discretely controllable thermal zones are customized to said die layout of said wafer; a cold plate disposed under said wafer TI layer and operable to cool said wafer; and a thermal controller for selectively heating and maintaining temperatures of areas of said wafer, during said testing, by controlling cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer.

7. Claims 42-48 depend from allowed claim 41 and are therefore also allowed.

8. With respect to claim 49, the prior art of record neither shows nor suggests the combination of method steps of generating signals for input to said circuits; processing output signals from said circuits; as generating a test result for said circuits; ass in conjunction with performing said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of said wafer and wherein said thermal interposer comprises a plurality of separately controllable thermal zones and wherein said selectively heating comprises selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones.

9. Claims 50-53 depend from allowed claim 49 and are therefore also allowed.
10. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PUB 2015/0035554 discloses a wafer debonding using mid-wavelength infrared radiation ablation.

US PUB 2010/0155888 discloses a silicon interposer testing for three dimensional chip stack.

US PUB 2015/0226794 discloses an apparatus for Testing Package-on-Package Semiconductor Device and Method for Testing the Same.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TEMILADE S RHODES-VIVOUR whose telephone number is (571)270-5814. The examiner can normally be reached M-F (flex schedule).

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Phan can be reached on 571-272-7924. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2858

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: <https://patentcenter.uspto.gov>. Visit <https://www.uspto.gov/patents/apply/patent-center> for more information about Patent Center and <https://www.uspto.gov/patents/docx> for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/TEMILADE S RHODES-VIVOUR/
Examiner, Art Unit 2858

/JERMELE M HOLLINGTON/
Primary Examiner, Art Unit 2858



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US

CONFIRMATION NO. 5009

109838
Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

37 CFR 1.48(f)
ACKNOWLEDGEMENT LETTER



OC000000072277592

Date Mailed: 05/07/2024

NOTICE OF ACCEPTANCE OF REQUEST UNDER 37 CFR 1.48(f)

This is in response to the applicant's request under 37 CFR 1.48(f) submitted on 02/10/2023.

The request under 37 CFR 1.48(f) to correct the inventorship, to correct or update the name of an inventor, or to correct the order of names of joint inventors is accepted.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/byemane/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
17/528,002	11/16/2021	2858	2680	AATS-0107-01U00US	26	3

CONFIRMATION NO. 5009

UPDATED FILING RECEIPT



00000000/2277593

109838

Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

Date Mailed: 05/07/2024

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Samer Kabbani, San Jose, CA;
Paul Ferrari, San Jose, CA;
Ikeda Hiroki, San Jose, CA;
Kiyokawa Toshiyuki, San Jose, CA;
Gregory Cruzan, San Jose, CA;
Karthik Ranganathan, San Jose, CA;

Applicant(s)

Advantest Test Solutions, Inc., San Jose, CA;

Power of Attorney: The patent practitioners associated with Customer Number 109838

Domestic Priority data as claimed by applicant

This appln claims benefit of 63/115,813 11/19/2020

Foreign Applications for which priority is claimed (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 11/30/2021

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/528,002**

Projected Publication Date: 05/19/2022

Non-Publication Request: No

Early Publication Request: No
Title

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Preliminary Class

324

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

Mina Oliveri (Typed or printed name)

/Mina Oliveri/ (Signature)

July 29, 2024 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009

TITLE OF INVENTION: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	07/29/2024

EXAMINER	ART UNIT	CLASS-SUBCLASS
RHODES-VIVOUR, TEMILADE S	2858	324-754070

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
Advantest Test Solutions, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)
San Jose, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☒ Electronic Payment via the USPTO patent electronic filing system ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 504160

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Anthony C. Murabito/

Date July 29, 2024

Typed or printed name Anthony C. Murabito

Registration No. 35295



UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #
17/528,002

RECEIPT DATE / TIME
07/29/2024 09:33:32 PM Z ET

ATTORNEY DOCKET #
AATS-0107-01U00US

Title of Invention

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 5009

FILED BY Mina Oliveri

PATENT CENTER # 66568995

AUTHORIZED BY Anthony Murabito

CUSTOMER # 109838

FILING DATE 11/16/2021

CORRESPONDENCE
ADDRESS -

FIRST NAMED
INVENTOR Samer Kabbani

Payment Information

PAYMENT METHOD
EFT / 055

PAYMENT TRANSACTION ID
E20247SL35189409

PAYMENT AUTHORIZED BY
Mina Oliveri

PRE-AUTHORIZED ACCOUNT
504160

PRE-AUTHORIZED CATEGORY

37 CFR 1.17 (Patent application and reexamination processing fees); 37 CFR 1.19 (Document supply fees); 37 CFR 1.20 (Post issuance fees); 37 CFR 1.21 (Miscellaneous fees and charges)

FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
1806	SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT	260.00	1	260.00
1501	UTILITY ISSUE FEE	1200.00	1	1200.00
TOTAL AMOUNT:				\$1,460.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/528,002

RECEIPT DATE / TIME
07/29/2024 09:33:32 PM Z ET

ATTORNEY DOCKET #
AATS-0107-01U00US

Title of Invention

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 5009

FILED BY Mina Oliveri

PATENT CENTER # 66568995

FILING DATE 11/16/2021

CUSTOMER # 109838

FIRST NAMED
INVENTOR Samer Kabbani

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Anthony Murabito

Documents

TOTAL DOCUMENTS: 4

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Eng_Abstract.pdf	2	Abstract	147 KB
FR_Ref.pdf	23	Foreign Reference	1568 KB
Issue_Fee_Trans.pdf	1	Issue Fee Payment (PTO-85B)	131 KB
AATS-0107-01U00US_IDS.pdf	4	Information Disclosure Statement (IDS) Form (SB08)	1313 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
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Eng_Abstract.pdf	F808FA7207761B2DC0171EE30908799DE54D5AC5047A95BAD CC89B2A351DE31627223E474F51B97A289CBF7C2E4E175442 2170A79AABBBFF5EFC4FA75A352EE
FR_Ref.pdf	53F653A963FA53BCED585E51F561A98A6ED9AC5D4B5204197 65C26327ADED8605164DE0BF33356F8B4B43BE82CE33A091 ADB14266E536A106830A7734558561
Issue_Fee_Trans.pdf	DA8FA7A0506F453A4130D28B3AA5EF6C36A44F4A3731BF4A7 5B3B11B96B631597846028A468E26D97B90E1775E003B3E0B1 01B761843A512202B9CCEC0B51B90
AATS-0107-01U00US_IDS.pdf	3A1A4832CBD76F91F5EA3DDD8FF166413EA8CD4B6CF88AAE 033445CAEB9A1C4CE1319EF9E745B5C09B58E0DAE6AD2989 5AC726E7B3C257C4B516EFCC6030F39A

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17528002
	Filing Date		2021-11-16
	First Named Inventor	Samer Kabbani	
	Art Unit	2858	
	Examiner Name	Temilade S. Rhodes-Vivour	
	Attorney Docket Number	AATS-0107-01U00US	

U.S.PATENTS							Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
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	1	20070027524	KR	A	2007-03-09	WELLS CTI LLC		☒

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NON-PATENT LITERATURE DOCUMENTS				Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17528002
Filing Date	2021-11-16
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	Temilade S. Rhodes-Vivour
Attorney Docket Number	AATS-0107-01U00US

1		☐
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If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17528002
	Filing Date		2021-11-16
	First Named Inventor	Samer Kabbani	
	Art Unit	2858	
	Examiner Name	Temilade S. Rhodes-Vivour	
	Attorney Docket Number	AATS-0107-01U00US	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97(e) to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☐ A certification statement is not submitted herewith.

FEE

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

COPIES

☐ An identification of an earlier application pursuant to 37 CFR 1.98 (d) (1) is attached.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2024-07-29
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009
109838	7590	08/30/2024	EXAMINER	
Advantest c/o Murabito Hao & Barnes LLP			RHODES-VIVOUR, TEMILADE S	
111 North Market Street			ART UNIT	PAPER NUMBER
Suite 700			2858	
San Jose, CA 95113			NOTIFICATION DATE	DELIVERY MODE
			08/30/2024	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

acmadmin@mhbpatents.com
officeaction@mhbpatents.com
tbettencourt@mhbpatents.com

Corrected Notice of Allowability	Application No. 17/528,002	Applicant(s) Kabbani et al.	
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the IDS filed on 07/29/2024.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 27-53 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)

2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 07/29/2024.

3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.

4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.

5. ☐ Examiner's Amendment/Comment

6. ☐ Examiner's Statement of Reasons for Allowance

7. ☒ Other PTO-90C and RUSH doc.

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858	/HUY Q PHAN/ Supervisory Patent Examiner, Art Unit 2858
---	--

**UNITED STATES DEPARTMENT OF COMMERCE****U.S. Patent and Trademark Office**

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR/ PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
17/528,002	11/16/2021	Kabbani et al.	AATS-0107-01U00US

Advantest c/o Murabito Hao & Barnes LLP 111 North Market Street Suite 700 San Jose, CA 95113		EXAMINER	
		TEMILADE S RHODES-VIVOUR	
		ART UNIT	PAPER
		2858	20240826

DATE MAILED: 27 August 2024

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

IDS submitted on 07/29/2024 has been considered by the examiner and the references thereof have been determined to not affect allowability

/TEMILADE S RHODES-VIVOUR/
Examiner, Art Unit 2858

/HUY Q PHAN/
Supervisory Patent Examiner, Art Unit 2858

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-22)

Approved for use through 05/31/2024. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17528002	
	Filing Date		2021-11-16	
	First Named Inventor	Samer Kabbani		
	Art Unit	2858		
	Examiner Name	Temilade S. Rhodes-Vivour		
	Attorney Docket Number	AATS-0107-01U00US		

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T ⁵
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.						T ⁵

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17528002
	Filing Date		2021-11-16
	First Named Inventor	Samer Kabbani	
	Art Unit		2858
	Examiner Name	Temilade S. Rhodes-Vivour	
	Attorney Docket Number		AATS-0107-01U00US

	1		☐
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If you wish to add additional non-patent literature document citation information please click the Add button

Add

EXAMINER SIGNATURE

Examiner Signature	/TEMILADE S RHODES-VIVOUR/	Date Considered	08/27/2024
--------------------	----------------------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17528002
Filing Date	2021-11-16
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	Temilade S. Rhodes-Vivour
Attorney Docket Number	AATS-0107-01U00US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97(e) to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☐ A certification statement is not submitted herewith.

FEE

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

COPIES

☐ An identification of an earlier application pursuant to 37 CFR 1.98 (d) (1) is attached.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2024-07-29
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	17528002
Filing Date	2021-11-16
First Named Inventor	Samer Kabbani
Art Unit	OPAP
Examiner Name	CENTRAL, DOCKET
Attorney Docket Number	AATS-0107-01U00US

U.S.PATENTS

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	5126656		1992-06-30	Jones	
	2	5164661		1992-11-17	Jones	
	3	5315240		1994-05-24	Jones	
Change(s) applied to document, /J.G./ 5/8/2024	4	5239093		08-1993 1004-07-12	Cheng Okano	
	5	5420521		1995-05-30	Jones	
	6	6389225		2002-05-14	Malinoski , et al.	
	7	6498899		2002-12-24	Malinoski , et al.	
	8	6711904		2004-03-30	Law , et al.	



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	10/01/2024	12105140	AATS-0107-01U00US	5009

109838 7590 09/11/2024
Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at <https://patentcenter.uspto.gov/>. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

The USPTO is implementing electronic patent issuance with a transition period, during which period the USPTO will mail a ceremonial paper copy of the electronic patent grant to the correspondence address of record. Additional copies of the patent (i.e., certified and presentation copies) may be ordered for a fee from the USPTO's Certified Copy Center at <https://certifiedcopycenter.uspto.gov/index.html>. The Certified Copy Center may be reached at (800)972-6382.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 226 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Center (<https://patentcenter.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PATENT CENTER site <https://patentcenter.uspto.gov> for additional inventors):

Samer Kabbani, San Jose, CA;
Paul Ferrari, San Jose, CA;
Ikeda Hiroki, San Jose, CA;
Kiyokawa Toshiyuki, San Jose, CA;
Gregory Cruzan, San Jose, CA;

APPLICANT(s) (Please see PATENT CENTER site <https://patentcenter.uspto.gov> for additional applicants):

Advantest Test Solutions, Inc., San Jose, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit [SelectUSA.gov](https://selectusa.gov).



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GRANT LETTER

APPLICATION #	DECISION DATE	DECISION ON PETITION #	ATTORNEY DOCKET NUMBER
17/528,002	09/26/2024	37 CFR 1.313(c)(2)	AATS-0107-01U00US

Title of Invention

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

In re Application of Samer Kabbani

This is an electronic decision on the petition under 37 CFR 1.313(c)(2), filed September 26, 2024 to withdraw the above-identified application from issue after payment of the issue fee.

The request is **GRANTED**.

The above-identified application is withdrawn from issue for consideration of a submission under 37 CFR 1.114 (request for continued examination). See 37 CFR 1.313(c)(2).

Petitioner is advised that the issue fee paid in this application cannot be refunded. If, however, this application is again allowed, petitioner may request that it be applied towards the issue fee required by the new Notice of Allowance.

The application is being referred to Technology Center AU for processing of the request for continuing examination under 37 CFR 1.114 .

Telephone inquired concerning this decision should be directed to the Patent Electronic Business Center (EBC) at 866-217-9197.

Office of Petitions

**REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)**

Application Number	17/528,002	Filing Date	2021-11-16	Docket Number (if applicable)	AATS-0107-01U00US	Art Unit	2858
First Named Inventor	David WYATT			Examiner Name	TEMILADE S. RHODES-VIVOUR		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____☐ Other _____☒ Enclosed☐ Amendment/Reply☒ Information Disclosure Statement (IDS)☐ Affidavit(s)/ Declaration(s)☐ Other _____**MISCELLANEOUS**☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)☐ Other _____**FEES****The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
Deposit Account No 504160**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED**☒ Patent Practitioner Signature☐ Applicant Signature

Signature of Registered U.S. Patent Practitioner			
Signature	/Jose S. Garcia/	Date (YYYY-MM-DD)	2024-09-26
Name	Jose S. Garcia	Registration Number	43,628

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/528,002

RECEIPT DATE / TIME
09/26/2024 07:55:10 PM Z ET

ATTORNEY DOCKET #
AATS-0107-01U00US

Title of Invention

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # 12105140

CONFIRMATION # 5009

FILED BY Jose Garcia

PATENT CENTER # 67344058

FILING DATE 11/16/2021

CUSTOMER # 109838

FIRST NAMED
INVENTOR Samer Kabbani

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY -

Documents

TOTAL DOCUMENTS: 9

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
petition-request.pdf	2	ePetition Request Form	29 KB
KR20170137334A.pdf	14	Foreign Reference	932 KB
KR20130093262A.pdf	16	Foreign Reference	1310 KB
KR20180061754A.pdf	15	Foreign Reference	1198 KB
AATS-0107- 01U00US_IDS_transmittal_fo rm.pdf	4	Information Disclosure Statement (IDS) Form (SB08)	1313 KB
JP2007248317A.pdf	15	Foreign Reference	786 KB
AATS-0107- 01U00US_RCE_9-26- 2024.pdf	3	Request for Continued Examination (RCE)	1628 KB

KR20200063664A.pdf	19	Foreign Reference	6022 KB
KR20200089714A.pdf	25	Foreign Reference	6510 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
petition-request.pdf	A4A2DCFC4490E9783E1A6E0E07770F7001268E42B4995DFFE C6B32C221CBE3DB39A9C5FC0A61D892B9798A04C6EA5377F D365AD288A942CBEEA7845DFE747B2E
KR20170137334A.pdf	E8E685B302576EA64798DB5B5B8DEC3DB717EF68874321A47 AC30E4F3F29B0F8B3E153514CF29B072390685E7B1AC11BD1 C84B4A1883610AE866949CE153D917
KR20130093262A.pdf	68ABA39428FD47B84E24974CA39CD742BD95869FA7B5710CF 669B6CB39F11710E0D5726B35155697C2E94546D331FC4D18 D3F0A6971F487F530EE45DA3C00C65
KR20180061754A.pdf	188AAD7579EE970766050F8F04DA8043D09D087D3724B63AE 2ECE898483B9409B857CC7FEFB47B871CFDDF6D995F3D466 CBB19DBADECD5A420C9311040F3F12F
AATS-0107- 01U00US_IDS_transmittal_for m.pdf	F374E82E4793B3CFEBCC9E211AB407536F957955CB7290ABF BFE486DB29D537D2929AA1B24EAA0322FAC92A74507C2FA3 47334F2867F24719920FF07225295E5
JP2007248317A.pdf	970A74ED294C29003AB26A5773DFC8A8354F060F35CF48AE9 FD1E53EC8D8A7B512AC74BB2ACBB52E3CA7840BE74FD61F 83F3E12FA787A3F47C93FCD67BCAA672
AATS-0107-01U00US_RCE_9- 26-2024.pdf	60EBFE6A1B7E3684CC2A89DE3064BE0E36E1C567D4D6F0C6 E1CA6817019C8D68EB37147253144FF496E9E0171CE6F1BBA BA6F1ADB4B5FF2B31D9A14A27D13D51
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KR20200089714A.pdf	DB99784281BD25FB1858248C2FD360243CB354F5B18F55A82 14BE972461818573A1B8F20BAA19235FF1AE2E484AD71E253 AFB2B281F1F32CB4B4CBB6DF76C100

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17528002	
	Filing Date		2021-11-16	
	First Named Inventor	Samer Kabbani		
	Art Unit	2858		
	Examiner Name	TEMILADE S. RHODES-VIVOUR		
	Attorney Docket Number	AATS-0107-01U00US		

U.S.PATENTS							Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1						

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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
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FOREIGN PATENT DOCUMENTS									Remove
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² i	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T ⁵	
	1	20170137334	KR		2017-12-13	SEMES CO LTD		☐	
	2	20200089714	KR		2020-07-27	TOKYO ELECTRON LTD		☐	
	3	2007248317	JP		2007-09-27	SUMITOMO ELECTRIC INDUSTRIES		☐	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number		17528002
Filing Date		2021-11-16
First Named Inventor	Samer Kabbani	
Art Unit	2858	
Examiner Name	TEMILADE S. RHODES-VIVOUR	
Attorney Docket Number	AATS-0107-01U00US	

4	20180061754	KR		2018-06-08	SEMES CO LTD		☐
5	20130093262	KR		2013-08-22	SEMES CO LTD		☐
6	20200063664	KR		2020-06-05	KOREA INST IND TECH		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17528002
	Filing Date		2021-11-16
	First Named Inventor	Samer Kabbani	
	Art Unit	2858	
	Examiner Name	TEMILADE S. RHODES-VIVOUR	
	Attorney Docket Number	AATS-0107-01U00US	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97(e) to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ A certification statement is not submitted herewith.

FEE

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

COPIES

☐ An identification of an earlier application pursuant to 37 CFR 1.98 (d) (1) is attached.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jose S. Garcia/	Date (YYYY-MM-DD)	2024-09-26
Name/Print	Jose S. Garcia	Registration Number	43,628

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/528,002	09/26/2024 07:55:10 PM Z ET	AATS-0107-01U00US

Title of Invention

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	12105140
CONFIRMATION #	5009	FILED BY	Jose Garcia
PATENT CENTER #	67344058	AUTHORIZED BY	-
CUSTOMER #	109838	FILING DATE	11/16/2021
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Samer Kabbani

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
EFT / 055	E20249PJ55477000	Jose Garcia

FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
1464	PETITIONS REQUIRING THE PETITION FEE SET FORTH IN 37 CFR 1.17(H) (GROUP III)	140.00	1	140.00
1801	REQUEST FOR CONTINUED EXAMINATION (RCE) - 1ST REQUEST (SEE 37 CFR 1.114)	1360.00	1	1360.00
TOTAL AMOUNT:				\$1,500.00

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New Applications Under 35 U.S.C. 111

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Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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PETITION TO WITHDRAW AN APPLICATION FROM ISSUE AFTER PAYMENT OF THE ISSUE FEE UNDER 37 CFR 1.313(c)(2) with Assigned Patent Number

APPLICATION #
17528002

ATTORNEY DOCKET #
AATS-0107-01U00US

FILING DATE
11/16/2021

Title of Invention

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Application Information

CONFIRMATION # 5009

FILING DATE 11/16/2021

ART UNIT 2858

FIRST NAMED INVENTOR Samer Kabbani

EXAMINER TEMILADE RHODES-VIVOUR

An application may be withdrawn from issue for further action upon petition by the applicant. To request that the Office withdraw an application from issue, applicant must file a petition under this section including the fee set forth in § 1.17(h) and a showing of good and sufficient reasons why withdrawal of the application from issue is necessary.

APPLICANT HEREBY PETITIONS TO WITHDRAW THIS APPLICATION FROM ISSUE UNDER 37 CFR 1.313(c).

A grantable petition requires the following items:

- (1) Petition fee; and
- (2) One of the following reasons: A grantable petition requires the following items: (a) Unpatentability of one or more claims, which must be accompanied by an unequivocal statement that one or more claims are unpatentable, an amendment to such claim or claims, and an explanation as to how the amendment causes such claim or claims to be patentable;
- (b) Consideration of a request for continued examination in compliance with § 1.114 (for a utility or plant application only); or
- (c) Express abandonment of the application. Such express abandonment may be in favor of a continuing application, but not a CPA under 37 CFR 1.53(d).

Reason for withdrawal

Consideration of a request for continued examination - RCE request, submission, and fee are attached

Applicant claims the following entity status

Regular Undiscounted

Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

An attorney or agent registered to practice before the Patent and Trademark Office who has been given power of attorney in this application

Signature

Name

Registration #

/Jose S. Garcia/

Jose Garcia

43628

<i>Search Notes</i> 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858

CPC - Searched*		
Symbol	Date	Examiner
G01R31/2887 G01R31/318511 G01R31/2874 G01R31/2875 G01R31/2877 G01R31/2889	11/29/2023	TRV
G01R31/2887 G01R31/318511 G01R31/2874 G01R31/2875 G01R31/2877 G01R31/2889	04/05/2024	TRV

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Conducted InnovationQ search	11/29/2023	TRV
Conducted PE2E keyword, cpc, inventor/assignee names and interference searches.	11/29/2023	TRV
Searches updated	04/05/2024	TRV
IDS of 09/26/2024 has been searched.	11/29/2024	TRV

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858	/JERMELE M HOLLINGTON/ Primary Examiner, Art Unit 2858
---	---

<i>Search Notes</i> 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	G01R31/2887 G01R31/318511 G01R31/2874 G01R31/2875 G01R31/2877 G01R31/2889	11/29/2023	TRV
	G01R31/2887 G01R31/318511 G01R31/2874 G01R31/2875 G01R31/2877 G01R31/2889	04/05/2024	TRV

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858	/JERMELE M HOLLINGTON/ Primary Examiner, Art Unit 2858
---	---

<i>Issue Classification</i> 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858

CPC						
Symbol					Type	Version
G01R	/	31	/	2887	F	2013-01-01
H01L	/	23	/	473	I	2013-01-01
G01R	/	31	/	318511	I	2013-01-01
F28F	/	2260	/	02	A	2013-01-01

CPC Combination Sets								
Symbol					Type	Set	Ranking	Version
	/		/					

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858		Total Claims Allowed:	
(Assistant Examiner)	(Date)	27	
/HUY Q PHAN/ Supervisory Patent Examiner, Art Unit 2858		O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	27	1

Issue Classification 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G01R31/28	/	31	/ 28
H01L23/473	/	23	/ 473
G01R31/3185	/	31	/ 3185
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
324	754.07

CROSS REFERENCES(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858 (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 27	
/HUY Q PHAN/ Supervisory Patent Examiner, Art Unit 2858 (Primary Examiner) _____ (Date) 29 November 2024		O.G. Print Claim(s) 27	O.G. Print Figure 1

Issue Classification 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
-	1	-	10	-	19	2	28	10	37	20	46				
-	2	-	11	-	20	3	29	11	38	21	47				
-	3	-	12	-	21	4	30	12	39	22	48				
-	4	-	13	-	22	5	31	14	40	23	49				
-	5	-	14	-	23	6	32	15	41	24	50				
-	6	-	15	-	24	7	33	16	42	25	51				
-	7	-	16	-	25	8	34	17	43	26	52				
-	8	-	17	-	26	13	35	18	44	27	53				
-	9	-	18	1	27	9	36	19	45						

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858 (Assistant Examiner) (Date)		Total Claims Allowed: 27	
/HUY Q PHAN/ Supervisory Patent Examiner, Art Unit 2858 (Primary Examiner) (Date)		O.G. Print Claim(s) 27	O.G. Print Figure 1

<i>Index of Claims</i> 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	11/29/2023	04/05/2024	11/29/2024						
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3	29	✓	=	=						
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5	31	O	=	=						
6	32	O	=	=						
7	33	O	=	=						
8	34	O	=	=						
13	35	✓	=	=						
9	36	✓	=	=						
10	37	✓	=	=						
11	38	✓	=	=						
12	39	✓	=	=						
14	40	✓	=	=						
15	41	✓	=	=						
16	42	✓	=	=						

<i>Index of Claims</i> 	Application/Control No. 17/528,002	Applicant(s)/Patent Under Reexamination Kabbani et al.
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858

CLAIM		DATE								
Final	Original	11/29/2023	04/05/2024	11/29/2024						
17	43	✓	=	=						
18	44	✓	=	=						
19	45	✓	=	=						
20	46	O	=	=						
21	47	O	=	=						
22	48	O	=	=						
23	49	=	=	=						
24	50	=	=	=						
25	51	=	=	=						
26	52	=	=	=						
27	53	=	=	=						

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	6	"17528002"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/14 01:31 PM
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L4	157	(wafer AND semiconductor AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/27 06:31 PM
L5	148	(wafer AND semiconductor AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB,	OR	ON	ON	2023/11/28 08:16 AM

		AND (cold ADJ plate)) AND heat\$3	HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L6	110	(wafer AND (semiconductor IC (intergrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND computer	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/28 01:56 PM
L7	123	(wafer AND (semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND computer	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/28 03:01 PM
L8	13	L7 NOT L6	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2023/11/28 03:02 PM

L9	171	(wafer AND (semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND (computer process\$3)	IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/28 10:18 PM
L10	48	L9 NOT L7	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/28 10:19 PM
L11	1749756	(wafer (semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND (computer process\$3)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 12:05 AM
L12	427067	(wafer (semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS,	OR	ON	ON	2023/11/29 12:10 AM

		AND (cold ADJ plate)) AND heat\$3 AND (computer)	IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L13	123	((semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND (computer) AND wafer	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 12:11 AM
L14	194	((wafer die semiconductor IC (integrated ADJ (circuit chip))) AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND heat\$3 AND (computer)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 12:15 AM
L15	2054	("8653843" "6515470" "7138811" "7781883" "8970244" "9594113" "10126356" "20060158207" "20090160472" "20110050268" "20140035715" "20150137842" "20160247552" "20190271719" "20200041564" "20210183668" "20210293495" "20220206061" "5239093" "5126656"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 06:54 AM

		"5164661" "5315240" "5239093" "5420521" "6389225" "6498899" "6711904" "6825681" "6862405" "6985000" "7311782" "7659738" "7726145" "8343280" "8772682" "8927907" "9307578" "10056225" "10163668" "10955466" "10983145" "7755899" "20020026258" "20040017185" "20130181576" "20180189159" "20190162777" "9841772" "9080820" "7411792" "9310145" "7755899" "10354785" "6184504" "9414526" "6668570" "10908207" "7042240" "7830164" "6359264" "7626407" "9766287" "9494353" "7436059" "5821505" "9291667" "7519880" "8558540" "10656200" "7151388" "7848106" "10656200" "10775408" "11143697" "5239093" "7355428" "20090218087" "20210071917" "20030155939" "20180218926" "20200371155" "20050086948" "20130285686" "20020118032" "20140251214" "20050151553" "20200363104" "20060290370" "20190346482" "20100042355" "20050026476" "20050103034" "20220082587" "20150226794" "20160084880" "20170102409" "20190310314" "20150028912" "20160351526" "20210396801" "20220137129" "20110074080" "20180024188"					
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L16	355	"20190064254" "20220044084" "5821505" "7042240" "7830164" "6668570" "10908207" "20130285686" "6359264" "7626407" "20020118032" "20140251214" "20050151553" "20060290370" "20190346482" "20200363104") ("8653843" "6515470" "7138811" "7781883" "8970244" "9594113" "10126356" "20060158207" "20090160472" "20110050268" "20140035715" "20150137842" "20160247552" "20190271719" "20200041564" "20210183668" "20210293495" "20220206061" "5239093" "5126656" "5164661" "5315240" "5239093" "5420521" "6389225" "6498899" "6711904" "6825681" "6862405" "6985000" "7311782" "7659738" "7726145" "8343280" "8772682" "8927907" "9307578" "10056225" "10163668" "10955466" "10983145" "7755899" "20020026258" "20040017185" "20130181576" "20180189159" "20190162777" "9841772" "9080820" "7411792" "9310145" "7755899" "10354785" "6184504" "9414526" "6668570" "10908207" "7042240" "7830164" "6359264" "7626407" "9766287" "9494353" "7436059" "5821505" "9291667" "7519880" "8558540" "10656200" "7151388" "7848106"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 06:55 AM
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L17	8	"10656200" "10775408" "11143697" "5239093" "7355428" "20090218087" "20210071917" "20030155939" "20180218926" "20200371155" "20050086948" "20130285686" "20020118032" "20140251214" "20050151553" "20200363104" "20060290370" "20190346482" "20100042355" "20050026476" "20050103034" "20220082587" "20150226794" "20160084880" "20170102409" "20190310314" "20150028912" "20160351526" "20210396801" "20220137129" "20110074080" "20180024188" "20190064254" "20220044084" "5821505" "7042240" "7830164" "6668570" "10908207" "20130285686" "6359264" "7626407" "20020118032" "20140251214" "20050151553" "20060290370" "20190346482" "20200363104").pn. (PWM (pulse near2 width near2 modulat\$3)) AND L16	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO;	OR	ON	ON	2023/11/29 11:32 AM
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L18	31	(pin AND channel\$1) AND L16	JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 01:05 PM
L19	35	(shield EMI radiation) AND L16	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 01:29 PM
L20	8	((indium ADJ foil) (graphite)) AND L16	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 03:09 PM
L21	2118	(Advantest near2 Test near2 Solutions).as. (Kabbani near2 Samer).in. (Ferrari near2 Paul).in. (Hiroki near2 Ikeda).in.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB,	OR	ON	ON	2023/11/29 09:27 PM

L22	9	(Toshiyuki near2 Kiyokawa).in. (Cruzan near2 Greg).in. (Ranganathan near2 Karthik).in.	HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 09:30 PM
L23	158	(wafer AND semiconductor AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate) AND L21)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 09:30 PM
L24	29205	(G01R31/2887 G01R31/318511 G01R31/2874 G01R31/2875 G01R31/2877 G01R31/2889).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 09:34 PM

L25	9	(wafer AND semiconductor AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate)) AND L24	IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/29 09:34 PM
L26	72	("20170137334" "20200089714" "2007248317" "20180061754" "20130093262" "20200063664")	IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/29 03:41 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	3	((wafer AND semiconductor AND test\$3 AND (cpu process\$3) AND probe\$1 AND ((thermal ADJ interposer) TI) AND (cold ADJ plate))) .clm. AND L24	(US-PGPUB; USPAT)	OR	ON	ON	2023/11/29 09:35 PM

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-22)

Approved for use through 05/31/2024. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17528002	
	Filing Date		2021-11-16	
	First Named Inventor	Samer Kabbani		
	Art Unit	2858		
	Examiner Name	TEMILADE S. RHODES-VIVOUR		
	Attorney Docket Number	AATS-0107-01U00US		

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	1	20170137334	KR		2017-12-13	SEMES CO LTD		☐
	2	20200089714	KR		2020-07-27	TOKYO ELECTRON LTD		☐
	3	2007248317	JP		2007-09-27	SUMITOMO ELECTRIC INDUSTRIES		☐

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17528002
Filing Date	2021-11-16
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	TEMILADE S. RHODES-VIVOUR
Attorney Docket Number	AATS-0107-01U00US

	4	20180061754	KR		2018-06-08	SEMES CO LTD		☐
	5	20130093262	KR		2013-08-22	SEMES CO LTD		☐
	6	20200063664	KR		2020-06-05	KOREA INST IND TECH		☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button **EXAMINER SIGNATURE**

Examiner Signature	/TEMILADE S RHODES-VIVOUR/	Date Considered	11/29/2024
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17528002
Filing Date	2021-11-16
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	TEMILADE S. RHODES-VIVOUR
Attorney Docket Number	AATS-0107-01U00US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97(e) to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ A certification statement is not submitted herewith.

FEE

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

COPIES

☐ An identification of an earlier application pursuant to 37 CFR 1.98 (d) (1) is attached.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jose S. Garcia/	Date (YYYY-MM-DD)	2024-09-26
Name/Print	Jose S. Garcia	Registration Number	43,628

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

109838 7590 12/18/2024
Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

EXAMINER	
RHODES-VIVOUR, TEMILADE S	
ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 12/18/2024

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009

TITLE OF INVENTION: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1290	\$0.00	\$1200.00	\$90	03/18/2025

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009

TITLE OF INVENTION: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1290	\$0.00	\$1200.00	\$90	03/18/2025

EXAMINER	ART UNIT	CLASS-SUBCLASS
RHODES-VIVOUR, TEMILADE S	2858	324-754070

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via the USPTO patent electronic filing system ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009
109838	7590	12/18/2024	EXAMINER	
Advantest c/o Murabito Hao & Barnes LLP			RHODES-VIVOUR, TEMILADE S	
111 North Market Street			ART UNIT	
Suite 700			PAPER NUMBER	
San Jose, CA 95113			2858	
DATE MAILED: 12/18/2024				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013).

<https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf>

Routine uses of the information in this record may include disclosure to:

- 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
- 2) a federal, state, local, or international agency, in response to its request;
- 3) a contractor of the USPTO having need for the information in order to perform a contract;
- 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;
- 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;
- 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;
- 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;
- 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));
- 9) the Office of Personnel Management (OPM) for personnel research purposes; and
- 10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Corrected Notice of Allowability	Application No. 17/528,002	Applicant(s) Kabbani et al.	
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the IDS filed on 09/26/2024.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 27-53 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 09/26/2024.	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858	/HUY Q PHAN/ Supervisory Patent Examiner, Art Unit 2858
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DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 09/26/2024 has been entered.
2. The information disclosure statement (IDS) submitted on 09/26/2024 was filed after the mailing date of the corrected notice of allowance on 08/30/2024. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

3. Claims 27-53 are allowed.
4. The following is an examiner's statement of reasons for allowance:
5. With respect to claim 27, the prior art of record neither shows nor suggests the combination of structural elements comprising a test computer for testing said circuits by generating signals for input to said circuits, processing output signals from said circuits and generating a test result thereof; a wafer

probe, coupled to said test computer, for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer; a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer, wherein said wafer TI layer comprises a plurality of resistive elements traversing said wafer TI layer and wherein said plurality of resistive elements are operable to selectively heat a plurality of zones of said wafer TI layer that correspond to said areas of said wafer; a cold plate disposed adjacent to said wafer TI layer and operable to cool said wafer; and a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer during said testing by controlling cooling of said cold plate and by controlling selective heating of said plurality of resistive elements of said wafer TI layer.

6. Claims 28-40 depend from allowed claim 27 and are therefore also allowed.

7. With respect to claim 41, the prior art of record neither shows nor suggests the combination of structural elements comprising a wafer probe for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer, said wafer probe coupled to communicate with said test computer system; a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer and wherein further said wafer comprises a die layout comprising a plurality of dice and wherein further positions and shapes of said plurality of discretely controllable thermal zones are customized to said die layout of said wafer; a cold plate disposed under said wafer TI layer and operable to cool said wafer; and a thermal controller for selectively heating and maintaining temperatures of areas of said wafer, during said testing, by controlling cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer.

8. Claims 42-48 depend from allowed claim 41 and are therefore also allowed.

9. With respect to claim 49, the prior art of record neither shows nor suggests the combination of method steps of generating signals for input to said circuits; processing output signals from said circuits; as generating a test result for said circuits; and in conjunction with performing said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of said wafer and wherein said thermal interposer comprises a plurality of separately controllable thermal zones and wherein said selectively heating comprises selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones.

10. Claims 50-53 depend from allowed claim 49 and are therefore also allowed.

11. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TEMILADE SRHODES-VIVOUR whose telephone number is (571)270-5814. The examiner can normally be reached M-F (flex schedule).

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Phan can be reached on 571-272-7924. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To

Art Unit: 2858

file and manage patent submissions in Patent Center, visit: <https://patentcenter.uspto.gov>. Visit

<https://www.uspto.gov/patents/apply/patent-center> for more information about Patent Center and

<https://www.uspto.gov/patents/docx> for information about filing in DOCX format. For additional

questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like

assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or

571-272-1000.

/TEMILADE SRHODES-VIVOUR/

Examiner, Art Unit 2858

/HUY Q PHAN/

Supervisory Patent Examiner, Art Unit 2858

Corrected Notice of Allowance - Correction of Issue Fee Amount

Due to a technical problem, the Notice of Allowance and Fee(s) Due mailed in this application specified an incorrect fee amount (the amount effective on January 19, 2025 for Notices of Allowance mailed on or after January 19, 2025). Corrected Notices of Allowance are being mailed to all applicants who are affected. This is necessary because the statute requires the applicant to pay the fee that is specified on the Notice of Allowance.

A Corrected Notice of Allowance is attached which specifies the correct issue fee. The time period for payment of the issue fee set forth in the previous Notice of Allowance and Fee(s) Due is being restarted to run THREE MONTHS from the "DATE MAILED" of the attached Corrected Notice of Allowance. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE

For applicants who replied prior to receiving the Corrected Notice of Allowance:

Applicant must still file a completed Part B – Fee(s) Transmittal, Form PTOL-85 Part B, or an equivalent, in reply to the Corrected Notice of Allowance since the Corrected Notice of Allowance sets forth a time period for reply. This applies to those situations in which applicant's reply was not processed before the Corrected Notice of Allowance was mailed (e.g., the reply crossed in the mail with the Corrected Notice of Allowance) and those situations in which applicant's reply was already processed. Applicants should check the appropriate box in section 4b of Form PTOL-85 Part B, such as the box authorizing the Director to "charge the required fee(s), any deficiency, or credit any overpayment" to a deposit account number. If this box is checked, the applicant will be refunded the amount of any overpayment to the designated deposit account. In addition, by checking the appropriate box in section 4b of Form PTOL-85, Part B, the applicant requests the Office to "first reapply any previously paid fee shown above," as stated on the form. Applicant may also include an explanatory cover letter, if desired. If, however, applicant prefers to file an equivalent of Form PTOL-85, Part B, and if applicant paid an increased issue fee amount as specified on the Notice of Allowance, applicant may request a refund of the difference between the incorrect amount specified on the Notice of Allowance and the correct amount specified on the Corrected Notice of Allowance.

For questions regarding the issue fee amount calculation, please contact the Application Assistance Unit at 888-786-0101 or HelpAAU@uspto.gov.

For assistance with Patent Center or other Patent Electronic Systems, please contact the Patent EBC at 1-866-217-9197 or ebc@uspto.gov.



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CORRECTED NOTICE OF ALLOWANCE AND FEE(S) DUE

109838 7590 12/20/2024
Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

EXAMINER	
RHODES-VIVOUR, TEMILADE S	
ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 12/20/2024

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009

TITLE OF INVENTION: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$1200.00	\$0	03/20/2025

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009

TITLE OF INVENTION: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$1200.00	\$0	03/20/2025

EXAMINER	ART UNIT	CLASS-SUBCLASS
RHODES-VIVOUR, TEMILADE S	2858	324-754070

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via the USPTO patent electronic filing system ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009
109838	7590	12/20/2024	EXAMINER	
Advantest c/o Murabito Hao & Barnes LLP			RHODES-VIVOUR, TEMILADE S	
111 North Market Street			ART UNIT	
Suite 700			PAPER NUMBER	
San Jose, CA 95113			2858	
DATE MAILED: 12/20/2024				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013).

<https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf>

Routine uses of the information in this record may include disclosure to:

- 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
- 2) a federal, state, local, or international agency, in response to its request;
- 3) a contractor of the USPTO having need for the information in order to perform a contract;
- 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;
- 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;
- 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;
- 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;
- 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));
- 9) the Office of Personnel Management (OPM) for personnel research purposes; and
- 10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kabbani et al.

Serial: 17/528,002 Confirmation No.: 5009

Filed: 11/16/2021 Group Art Unit: 2858

Examiner: Rhodes-Vivour, Temilade S.

For: Wafer Scale Active Thermal Interposer for Device Testing

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER NOTICE OF ALLOWANCE

(Rule 312)

Dear Examiner Rhodes-Vivour:

In response to the Notice of Allowance mailed 12/20/2024 in the above captioned Patent Application, Applicants respectfully request the Examiner to enter the following amendments under 37 C.F.R. § 1.312.

In the Claims:

1-26 (cancelled)

27. (Previously Presented) A test system for testing circuits of an integrated circuit semiconductor wafer, the test system comprising:

a test computer for testing said circuits by generating signals for input to said circuits, processing output signals from said circuits and generating a test result thereof;

a wafer probe, coupled to said test computer, for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer;

a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer, wherein said wafer TI layer comprises a plurality of resistive elements traversing said wafer TI layer and wherein said plurality of resistive elements are operable to selectively heat a plurality of zones of said wafer TI layer that correspond to said areas of said wafer;

a cold plate disposed adjacent to said wafer TI layer and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer during said testing by controlling

cooling of said cold plate and by controlling selective heating of said plurality of resistive elements of said wafer TI layer.

28. (Previously Presented) The system as described in Claim 27 wherein positions of said plurality of zones of said wafer TI layer correspond to a die layout of said wafer and wherein further said wafer TI layer is customized for said wafer.

29. (Previously Presented) The test system as described in Claim 28 further comprising:

a chiller for cooling liquid; and

a valve for controlling an amount of said liquid flowing to said cold plate, wherein said valve is controlled by said thermal controller.

30. (Previously Presented) The system as described in Claim 28 further comprising:

a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and

a second TIM layer disposed between said wafer TI layer and said wafer.

31. (Previously Presented) The system as described in Claim 30 wherein said first and second TIM layers comprise indium foil.

32. (Previously Presented) The system as described in Claim 30 wherein said first and second TIM layers comprise graphite material.

33. (Previously Presented) The system as described in Claim 30 further comprising:

a first vacuum valve for establishing suction for securing said wafer to said wafer TI layer;

a second vacuum valve for establishing suction for securing said wafer TI layer to said cold plate; and

a vacuum pump coupled to both said first and second vacuum valves.

34. (Previously Presented) The system as described in Claim 33 further comprising:

a first blow-off valve for controlling air to release said wafer from said wafer TI layer;

a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and

a source of air coupled to both said first and second blow-off valves.

35. (Previously Presented) The test system as described in Claim 27 further comprising a power supply coupled to provide power to said wafer TI

layer and controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said selective heating of said wafer TI layer is based on said PWM signals.

36. (Previously Presented) The system as described in Claim 28 wherein each zone of said plurality of zones corresponds to a respective single die of said die layout of said wafer.

37. (Previously Presented) The system as described in Claim 28 wherein each zone of said plurality of zones corresponds to a respective plurality of dice of said die layout of said wafer.

38. (Previously Presented) The system as described in Claim 28 wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.

39. (Previously Presented) The system as described in Claim 28 further comprising a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical pass through channels which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer.

40. (currently amended) The system as described in Claim 35 wherein said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from said PWM signals applied to said plurality of ~~traces~~ resistive elements.

41. (Previously Presented) A test system for testing circuits of an integrated circuit semiconductor wafer, the system comprising:

a test computer system for testing said circuits by generating signals for input to said circuits, processing output signals from said circuits and generating a test result for said circuits of said wafer;

a wafer probe for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer, said wafer probe coupled to communicate with said test computer system;

a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer and wherein further said wafer comprises a die layout comprising a plurality of dice and wherein further positions and shapes of said plurality of discretely controllable thermal zones are customized to said die layout of said wafer;

a cold plate disposed under said wafer TI layer and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of areas of said wafer, during said testing, by controlling cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer.

42. (Previously Presented) The test system as described in Claim 41 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to multiple dice of said die layout of said wafer.

43. (Previously Presented) The test system as described in Claim 41 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to a single die of said die layout of said wafer.

44. (Previously Presented) A test system as described in Claim 41 wherein each die of said die layout of said wafer corresponds to multiple thermal zones of said plurality of discretely controllable thermal zones of said wafer TI layer.

45. (Previously Presented) The test system as described in Claim 41 wherein said wafer TI layer comprises a plurality of resistive elements

traversing said wafer TI layer and operable to selectively heat and maintain temperatures of said plurality of discretely controllable thermal zones of said wafer TI layer responsive to said thermal controller.

46. (Previously Presented) The test system as described in Claim 41 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and

while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

47. (Previously Presented) The test system as described in Claim 41 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and

while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

48. (Previously Presented) The test system as described in Claim 41 further comprising: a thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer and wherein said TIM layer comprises one of: indium foil; and graphite material.

49. (Previously Presented) A method of testing circuits of an integrated circuit semiconductor wafer, the method comprising:
testing said circuits of said wafer by using a test computer system wherein said testing comprises:
generating signals for input to said circuits;
processing output signals from said circuits;
generating a test result for said circuits; and
in conjunction with performing said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of said wafer and wherein said thermal interposer

comprises a plurality of separately controllable thermal zones and wherein said selectively heating comprises selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones.

50. (Previously Presented) The method as described in Claim 49 wherein said wafer comprises a die layout and wherein further positions and shapes of said plurality of separately controllable thermal zones of said thermal interposer layer are customized to said die layout.

51. (Previously Presented) The method as described in Claim 50 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises:

bringing a first thermal zone of said plurality of separately controllable thermal zones to a testing temperature; and

while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of separately controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

52. (Previously Presented) The method as described in Claim 50 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises:

bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and

while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

53. (Previously Presented) The method of Claim 50 wherein said plurality of separately controlled thermal zones comprise a plurality of resistive elements and wherein further said selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones comprises said thermal controller selectively energizing said plurality of resistive elements during said testing.

REMARKS

Claims 27-53 are pending in the present application. Claims 1-26 were previously canceled. Claim 40 is amended for correct minor informalities. No new matter is added. Applicants respectfully request reconsideration of the present application in view of the indicated amendments.

CONCLUSION

Claims 27-53 are pending in the present application. Applicants understand all Claims to be in condition for allowance, and such allowance is earnestly sought.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 504160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Date: March 17, 2025

/Anthony C. Murabito/

Anthony C. Murabito

Reg. No. 35,295

1500 E. Hamilton Ave.

Suite 118

Campbell, California 95008

(408) 938-9060



UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/528,002

RECEIPT DATE / TIME
03/17/2025 02:26:49 PM Z ET

ATTORNEY DOCKET #
AATS-0107-01U00US

Title of Invention

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 5009

FILED BY Mina Oliveri

PATENT CENTER # 69610726

FILING DATE 11/16/2021

CUSTOMER # 109838

FIRST NAMED
INVENTOR Samer Kabbani

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Anthony Murabito

Documents

TOTAL DOCUMENTS: 3

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
AATS-0107-01U00US_Amdt_After_Allowance_3-17-2025.pdf		13	-	61 KB
AATS-0107-01U00US_Amdt_After_Allowance_3-17-2025-A.NA.pdf	(1-1)	1	Amendment after Notice of Allowance (Rule 312)	24 KB
AATS-0107-01U00US_Amdt_After_Allowance_3-17-2025-CLM.pdf	(2-11)	10	Claims	55 KB
AATS-0107-01U00US_Amdt_After_Allowance_3-17-2025-REM.pdf	(12-13)	2	Applicant Arguments/Remarks Made in an Amendment	25 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
AATS-0107-01U00US_Amdt_After_Allowance_3-17-2025.pdf	A3EE45D26735ACF04AEBE6044141B4E8FF445DEFF59356F6A B0B37F8C51C6EEA52C7E7AF527161D49D75FB97A3B32AC32 6F050963538B8E59C7276243516210B
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AATS-0107-01U00US_Amdt_After_Allowance_3-17-2025-CLM.pdf	0C85B06E27297B3C4E4460981D99492F9DC594D4B76F38AD0 EC5EDAE6D94E4D48DAB8839CD23C77F899F9090AE809EC2 A5E3DEDDD0141A61F80B0BE2C38D566E
AATS-0107-01U00US_Amdt_After_Allowance_3-17-2025-REM.pdf	7069B29BD64AD66E5F32D99C9535687B80070973D5F155BF97 B021FBF2033C0394A222302B8396E50F63CD72E6E819EE2600 8FB7EE4113D43D70859D0A362CDE

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

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Mina Oliveri	(Typed or printed name)
/Mina Oliveri/	(Signature)
3/18/2025	(Date)



109838 7590 12/20/2024
Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009

TITLE OF INVENTION: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$1200.00	\$0	03/20/2025

EXAMINER	ART UNIT	CLASS-SUBCLASS
RHODES-VIVOUR, TEMILADE S	2858	324-754070

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

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1 _____
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

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(A) NAME OF ASSIGNEE
Advantest Test Solutions, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)
San Jose, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

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☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 50-4160

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Anthony C. Murabito/

Date 03/18/2025

Typed or printed name Anthony C. Murabito

Registration No. 35,295

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Mina Oliveri	(Typed or printed name)
/Mina Oliveri/	(Signature)
3/18/2025	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009

TITLE OF INVENTION: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$1200.00	\$0	03/20/2025

EXAMINER	ART UNIT	CLASS-SUBCLASS
RHODES-VIVOUR, TEMILADE S	2858	324-754070

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

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(A) NAME OF ASSIGNEE
Advantest Test Solutions, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)
San Jose, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required)

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☐ Applicant asserting small entity status. See 37 CFR 1.27

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Authorized Signature /Anthony C. Murabito/

Date 03/18/2025

Typed or printed name Anthony C. Murabito

Registration No. 35,295



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PATENT AND TRADEMARK OFFICE

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APPLICATION #
17/528,002

RECEIPT DATE / TIME
03/18/2025 09:51:56 PM Z ET

ATTORNEY DOCKET #
AATS-0107-01U00US

Title of Invention

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 5009

FILED BY Mina Oliveri

PATENT CENTER # 69639008

FILING DATE 11/16/2021

CUSTOMER # 109838

FIRST NAMED
INVENTOR Samer Kabbani

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Anthony Murabito

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Issue_Fee_Paid.pdf	1	Issue Fee Payment (PTO-85B)	105 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
Issue_Fee_Paid.pdf	007E0518131A7E114D4B2DAAEC2F6F01D76D17F3585A37578 7310A3985ED0C320FCADFE78008A5F679E41C57A89F7B71AD 7E1B0EAE6BE3310B908489612D1C28

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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United States Patent and Trademark Office

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Document Code:WFEE

User :Sengpheth Sandara

Sale Accounting Date:03/20/2025

Sale Item Reference Number

17528002

Effective Date

03/18/2025

Document Number

I20253J700087810

Fee Code

1501

Fee Code Description

UTILITY APPL ISSUE FEE

Amount Paid

\$1,200.00

Payment Method

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/528,002

RECEIPT DATE / TIME
04/16/2025 02:06:43 PM Z ET

ATTORNEY DOCKET #
AATS-0107-01U00US

Title of Invention

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 5009

FILED BY Mina Oliveri

PATENT CENTER # 70033176

FILING DATE 11/16/2021

CUSTOMER # 109838

FIRST NAMED
INVENTOR Samer Kabbani

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Anthony Murabito

Documents

TOTAL DOCUMENTS: 3

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
AATS-0107-01U00US_AMEND_AFTER_ALLOWANCE.pdf		13	-	55 KB
AATS-0107-01U00US_AMEND_AFTER_ALLOWANCE-SA...pdf	(1-1)	1	Supplemental Response or Supplemental Amendment	24 KB
AATS-0107-01U00US_AMEND_AFTER_ALLOWANCE-CLM.pdf	(2-11)	10	Claims	34 KB
AATS-0107-01U00US_AMEND_AFTER_ALLOWANCE-REM.pdf	(12-13)	2	Applicant Arguments/Remarks Made in an Amendment	34 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
AATS-0107- 01U00US_AMEND_AFTER_AL LOWANCE.pdf	D0FDB5EB2A35EF48E95E15222C31BAC6584E41B3C9E5C21C 8BDA383654C391E1D04EC65B29388ED104CB3D83B93140F7 C92380CEC52B7DDCDC5453D440B14A40
AATS-0107- 01U00US_AMEND_AFTER_AL LOWANCE-SA...pdf	12241E5FF07F27CE335E64AD24D9EE98198104D309AD684D6 12851A0ED2C4E432D8951E64DA7F06C679FC3CDBE8A8586A EC4725592C01B603E542B4C0D32B1D3
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AATS-0107- 01U00US_AMEND_AFTER_AL LOWANCE-REM.pdf	7462393BD31C196ED43C0C7146138413249FE79D62BB079B5 4366E1ED1F77C7668C48F11A383D66B607A17ABF3883ADF29 C4D9F1E6DBFA059A6D0AB72224BD0B

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kabbani et al.

Serial: 17/528,002 Confirmation No.: 5009

Filed: 11/16/2021 Group Art Unit: 2858

Examiner: Rhodes-Vivour, Temilade S.

For: Wafer Scale Active Thermal Interposer for Device Testing

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL AMENDMENT

AFTER NOTICE OF ALLOWANCE

(Rule 312)

Dear Examiner Rhodes-Vivour:

In response to the Notice of Allowance mailed 12/20/2024 in the above captioned Patent Application, and the Amendment After Notice of Allowance (Rule 312) submitted March 17, 2025, Applicants respectfully request the Examiner to enter the following supplemental amendments under 37 C.F.R. § 1.312.

In the Claims:

1-26 (cancelled)

27. (Currently Amended) A test system for testing circuits of an integrated circuit semiconductor wafer, the test system comprising:

a test computer for testing said circuits by generating signals for input to said circuits, processing output signals from said circuits and generating a test result thereof;

a wafer probe, coupled to said test computer, for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer;

a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer, wherein said wafer TI layer comprises a plurality of resistive traces ~~elements~~ traversing said wafer TI layer and wherein said plurality of resistive traces ~~elements~~ are operable to selectively heat a plurality of zones of said wafer TI layer that correspond to said areas of said wafer;

a cold plate disposed adjacent to said wafer TI layer and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer during said testing by controlling

cooling of said cold plate and by controlling selective heating of said plurality of resistive traces ~~elements~~ of said wafer TI layer.

28. (Previously Presented) The system as described in Claim 27 wherein positions of said plurality of zones of said wafer TI layer correspond to a die layout of said wafer and wherein further said wafer TI layer is customized for said wafer.

29. (Previously Presented) The test system as described in Claim 28 further comprising:

a chiller for cooling liquid; and

a valve for controlling an amount of said liquid flowing to said cold plate, wherein said valve is controlled by said thermal controller.

30. (Previously Presented) The system as described in Claim 28 further comprising:

a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and

a second TIM layer disposed between said wafer TI layer and said wafer.

31. (Previously Presented) The system as described in Claim 30 wherein said first and second TIM layers comprise indium foil.

32. (Previously Presented) The system as described in Claim 30 wherein said first and second TIM layers comprise graphite material.

33. (Previously Presented) The system as described in Claim 30 further comprising:

a first vacuum valve for establishing suction for securing said wafer to said wafer TI layer;

a second vacuum valve for establishing suction for securing said wafer TI layer to said cold plate; and

a vacuum pump coupled to both said first and second vacuum valves.

34. (Previously Presented) The system as described in Claim 33 further comprising:

a first blow-off valve for controlling air to release said wafer from said wafer TI layer;

a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and

a source of air coupled to both said first and second blow-off valves.

35. (Previously Presented) The test system as described in Claim 27 further comprising a power supply coupled to provide power to said wafer TI

layer and controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said selective heating of said wafer TI layer is based on said PWM signals.

36. (Previously Presented) The system as described in Claim 28 wherein each zone of said plurality of zones corresponds to a respective single die of said die layout of said wafer.

37. (Previously Presented) The system as described in Claim 28 wherein each zone of said plurality of zones corresponds to a respective plurality of dice of said die layout of said wafer.

38. (Previously Presented) The system as described in Claim 28 wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.

39. (Previously Presented) The system as described in Claim 28 further comprising a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical pass through channels which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer.

40. (Currently Amended) The system as described in Claim 35 wherein said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from said PWM signals applied to said plurality of resistive traces ~~elements~~.

41. (Previously Presented) A test system for testing circuits of an integrated circuit semiconductor wafer, the system comprising
a test computer system for testing said circuits by generating signals for input to said circuits, processing output signals from said circuits and generating a test result for said circuits of said wafer;

a wafer probe for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer, said wafer probe coupled to communicate with said test computer system;

a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer and wherein further said wafer comprises a die layout comprising a plurality of dice and wherein further positions and shapes of said plurality of discretely controllable thermal zones are customized to said die layout of said wafer;

a cold plate disposed under said wafer TI layer and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of areas of said wafer, during said testing, by controlling cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer.

42. (Previously Presented) The test system as described in Claim 41 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to multiple dice of said die layout of said wafer.

43. (Previously Presented) The test system as described in Claim 41 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to a single die of said die layout of said wafer.

44. (Previously Presented) A test system as described in Claim 41 wherein each die of said die layout of said wafer corresponds to multiple thermal zones of said plurality of discretely controllable thermal zones of said wafer TI layer.

45. (Currently Amended) The test system as described in Claim 41 wherein said wafer TI layer comprises a plurality of resistive traces ~~elements~~

traversing said wafer TI layer and operable to selectively heat and maintain temperatures of said plurality of discretely controllable thermal zones of said wafer TI layer responsive to said thermal controller.

46. (Previously Presented) The test system as described in Claim 41 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and

while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

47. (Previously Presented) The test system as described in Claim 41 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and

while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

48. (Previously Presented) The test system as described in Claim 41 further comprising: a thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer and wherein said TIM layer comprises one of: indium foil; and graphite material.

49. (Previously Presented) A method of testing circuits of an integrated circuit semiconductor wafer, the method comprising:
testing said circuits of said wafer by using a test computer system wherein said testing comprises:
generating signals for input to said circuits;
processing output signals from said circuits;
generating a test result for said circuits; and
in conjunction with performing said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of said wafer and wherein said thermal interposer

comprises a plurality of separately controllable thermal zones and wherein said selectively heating comprises selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones.

50. (Previously Presented) The method as described in Claim 49 wherein said wafer comprises a die layout and wherein further positions and shapes of said plurality of separately controllable thermal zones of said thermal interposer layer are customized to said die layout.

51. (Previously Presented) The method as described in Claim 50 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises:

bringing a first thermal zone of said plurality of separately controllable thermal zones to a testing temperature; and

while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of separately controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

52. (Previously Presented) The method as described in Claim 50 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises:

bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and

while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

53. (Currently Amended) The method of Claim 50 wherein said plurality of separately controlled thermal zones comprise a plurality of resistive traces ~~elements~~ and wherein further said selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones comprises said thermal controller selectively energizing said plurality of resistive traces ~~elements~~ during said testing.

REMARKS

Claims 27-53 are pending in the present application. Claims 1-26 were previously canceled. Claims 27, 40, 45 and 53 are amended herein to correct minor informalities. No new matter is added. Applicants respectfully request reconsideration of the present application in view of the indicated amendments.

CONCLUSION

Claims 27-53 are pending in the present application. Applicants understand all Claims to be in condition for allowance, and such allowance is earnestly sought.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 504160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Date: April 16, 2025

/Anthony C. Murabito/

Anthony C. Murabito

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1500 E. Hamilton Ave
Suite 118
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(408) 938-9060



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009
109838	7590	05/05/2025	EXAMINER	
Advantest c/o Murabito Hao & Barnes LLP			RHODES-VIVOUR, TEMILADE S	
1500 E Hamilton Ave			ART UNIT	PAPER NUMBER
Suite 118			2858	
Campbell, CA 95008			NOTIFICATION DATE	DELIVERY MODE
			05/05/2025	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

acmadmin@mhbpatents.com
officeaction@mhbpatents.com

Response to Rule 312 Communication	Application No. 17/528,002	Applicant(s) Kabbani et al.	
	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on 16 April 2025 under 37 CFR 1.312 has been considered, and has been:

a) ☐ entered.

b) ☒ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

f) ☐ not entered because the supplemental or corrected Application Data sheet (ADS)

☐ was not accompanied by a petition to accept an unintentionally delayed claim under 37 CFR 1.55 or 27 CFR 1.78;
☐ did not identify the information being changed in accordance with 37 CFR 1.76(c)(2);
☐ was not properly signed in accordance with 37 CFR 1.76(e) (or 37 CFR 1.33(b) for applications filed prior to September 16, 2012).

/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858	/HUY Q PHAN/ Supervisory Patent Examiner, Art Unit 2858
---	--

AATS-0107-01U00US (20P075US02)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kabbani et al.

Serial: 17/528,002 Confirmation No.: 5009

Filed: 11/16/2021 Group Art Unit: 2858

Examiner: Rhodes-Vivour, Temilade S.

For: Wafer Scale Active Thermal Interposer for Device Testing

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL AMENDMENT

AFTER NOTICE OF ALLOWANCE

(Rule 312)

Dear Examiner Rhodes-Vivour:

In response to the Notice of Allowance mailed 12/20/2024 in the above captioned Patent Application, and the Amendment After Notice of Allowance (Rule 312) submitted March 17, 2025, Applicants respectfully request the Examiner to enter the following supplemental amendments under 37 C.F.R. § 1.312.

AATS-0107-01U00US/ACM/NAO
Examiner: Rhodes-Vivour, T. S.

1

Serial No.: 17/528,002
Group Art Unit: 2858



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009
109838	7590	05/12/2025		
Advantest c/o Murabito Hao & Barnes LLP			EXAMINER	
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			05/12/2025	ELECTRONIC

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	Examiner TEMILADE S RHODES-VIVOUR	Art Unit 2858	AIA (FITF) Status Yes

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1. ☒ The amendment filed on 16 April 2025 under 37 CFR 1.312 has been considered, and has been:

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e) ☐ entered in part. See explanation below.

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/TEMILADE S RHODES-VIVOUR/ Examiner, Art Unit 2858	/HUY Q PHAN/ Supervisory Patent Examiner, Art Unit 2858
---	--

AATS-0107-01U00US (20P075US02)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kabbani et al.

Serial: 17/528,002 Confirmation No.: 5009

Filed: 11/16/2021 Group Art Unit: 2858

Examiner: Rhodes-Vivour, Temilade S.

For: Wafer Scale Active Thermal Interposer for Device Testing

Honorable Commissioner for Patents
PO Box 1450
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SUPPLEMENTAL AMENDMENT

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AATS-0107-01U00US/ACM/NAO
Examiner: Rhodes-Vivour, T. S.

1

Serial No.: 17/528,002
Group Art Unit: 2858



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	06/03/2025	12320841	AATS-0107-01U00US	5009

109838 7590 05/21/2025
Advantest c/o Murabito Hao & Barnes LLP
1500 E Hamilton Ave
Suite 118
Campbell, CA 95008

ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at <https://patentcenter.uspto.gov/>. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

The USPTO is implementing electronic patent issuance with a transition period, during which period the USPTO will mail a ceremonial paper copy of the electronic patent grant to the correspondence address of record. Additional copies of the patent (i.e., certified and presentation copies) may be ordered for a fee from the USPTO's Certified Copy Center at <https://certifiedcopycenter.uspto.gov/index.html>. The Certified Copy Center may be reached at (800)972-6382.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 163 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Center (<https://patentcenter.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PATENT CENTER site <https://patentcenter.uspto.gov> for additional inventors):

Samer Kabbani, San Jose, CA;
Paul Ferrari, San Jose, CA;
Ikeda Hiroki, San Jose, CA;
Kiyokawa Toshiyuki, San Jose, CA;
Gregory Cruzan, San Jose, CA;

APPLICANT(s) (Please see PATENT CENTER site <https://patentcenter.uspto.gov> for additional applicants):

Advantest Test Solutions, Inc., San Jose, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit [SelectUSA.gov](https://selectusa.gov).



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/528,002	11/16/2021	Samer Kabbani	AATS-0107-01U00US	5009
109838	7590	06/03/2025		
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APPLICATION NO.	ISSUE DATE	PATENT NO.
17/528,002	03-Jun-2025	12320841

Advantest c/o Murabito Hao & Barnes LLP
1500 E Hamilton Ave
Campbell, CA 95008

EGRANT NOTIFICATION

Your electronic patent grant (eGrant) is now available, which can be accessed via Patent Center at <https://patentcenter.uspto.gov>

The electronic patent grant is the official patent grant under 35 U.S.C. 153. For more information, please visit <https://www.uspto.gov/electronicgrants>

To:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Southern District of California on the following: X Patents or Trademarks:

DOCKET NO.	DATE FILED	US District Court Southern District of California
3:25-cv-02604-JES-BJW	10/1/25	San Diego, CA
PLAINTIFF		DEFENDANT
Advantest Test Solutions, Inc.		AEM Holdings Ltd., et al.
PATENT OR TRADEMARK NO.	PATENT OR TRADEMARK NO.	PATENT OR TRADEMARK NO.
1. 11,674,999	6. 12,259,428	11.
2. 12,320,841	7.	12.
3. 12,013,432	8.	13.
4. 12,085,609	9.	14.
5. 12,000,885	10.	15.

In the above-entitled case, the following patents(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY	
	<u> </u> Amendment <u> </u> Answer <u> </u> Cross Bill <u> </u> Other Pleading	
PATENT OR TRADEMARK NO.	PATENT OR TRADEMARK NO.	PATENT OR TRADEMARK NO.
1.	6.	11.
2.	7.	12.
3.	8.	13.
4.	9.	14.
5.	10.	15.

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGMENT

CLERK	(BY) DEPUTY CLERK	DATE
John Morrill		