

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AEM AMERICAS, INC.,

Petitioner

v.

ADVANTEST TEST SOLUTIONS, INC.,

Patent Owner

Case IPR2027-00005

U.S. Patent No. 12,320,841

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 12,320,841

**Mail Stop PATENT BOARD
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450**

TABLE OF CONTENTS

	<u>Page</u>
I. INTRODUCTION.....	1
II. TECHNOLOGY BACKGROUND.....	1
III. STATEMENT OF PRECISE RELIEF REQUESTED	2
IV. THE '841 PATENT	2
A. SPECIFICATION AND CLAIMS	3
B. PROSECUTION HISTORY	5
V. PERSON OF ORDINARY SKILL IN THE ART	7
VI. CLAIM CONSTRUCTION.....	7
VII. IDENTIFICATION OF CHALLENGES AND PRIMARY PRIOR ART 7	
A. Reference #1: DiBattista (U.S. Patent No. 6,549,026 B1)	8
B. Reference #2: Herchen-1 (U.S. Patent Application Publication No. 2011/0000426)	9
C. Reference #3: Herchen-2 (U.S. Patent Application Publication No. 2008/0160462)	10
D. Reference #4: Pease (U.S. Patent Application Publication No. 2013/0220989)	11
E. Reference #5: Sugiyama (U.S. Patent Application Publication No. 2004/0227536)	12
F. Reference #6: Costello (U.S. Patent Application Publication No. 2002/0017916)	13

G. Reference #7: Parkhe (U.S. Patent Application Publication No. 2016/0111315)	14
---	-----------

VIII. GROUND 1: CLAIMS 1-27 ARE RENDERED OBVIOUS OVER DIBATTISTA IN VIEW OF HERCHEN-1, HERCHEN-2, PEASE, AND NATSUHARA	16
---	-----------

A. OVERVIEW OF GROUND 1.....	16
-------------------------------------	-----------

B. INDEPENDENT CLAIM 1.....	20
------------------------------------	-----------

C. CLAIM 2	24
-------------------------	-----------

D. CLAIM 3	24
-------------------------	-----------

E. CLAIM 4	25
-------------------------	-----------

F. CLAIM 5	25
-------------------------	-----------

G. CLAIM 6	25
-------------------------	-----------

H. CLAIM 7	26
-------------------------	-----------

I. CLAIM 8	27
-------------------------	-----------

J. CLAIM 9	27
-------------------------	-----------

K. CLAIM 10	27
--------------------------	-----------

L. CLAIM 11	28
--------------------------	-----------

M. CLAIM 12	28
--------------------------	-----------

N. CLAIM 13	29
--------------------------	-----------

O. CLAIM 14	30
--------------------------	-----------

P. INDEPENDENT CLAIM 15.....	31
-------------------------------------	-----------

Q. CLAIM 16	33
--------------------------	-----------

R. CLAIM 17	34
--------------------------	-----------

S. CLAIM 18	34
--------------------------	-----------

T. CLAIM 19	34
U. CLAIM 20	35
V. CLAIM 21	35
W. CLAIM 22.....	36
X. INDEPENDENT CLAIM 23.....	36
Y. CLAIM 24	38
Z. CLAIM 25	38
AA. CLAIM 26.....	38
BB. CLAIM 27.....	38

**IX. GROUND 2: CLAIMS 1-27 ARE RENDERED OBVIOUS OVER
DIBATTISTA IN VIEW OF COSTELLO, HERCHEN-1, AND CRIMINALE**

39

A. OVERVIEW OF GROUND 2.....	39
B. INDEPENDENT CLAIM 1.....	40
C. CLAIM 2	43
D. CLAIM 3	43
E. CLAIM 4	43
F. CLAIM 5	44
G. CLAIM 6	45
H. CLAIM 7	45
I. CLAIM 8	45
J. CLAIM 9	46
K. CLAIM 10	46

L. CLAIM 11	46
M. CLAIM 12	47
N. CLAIM 13	47
O. CLAIM 14	49
P. INDEPENDENT CLAIM 15.....	49
Q. CLAIM 16	50
R. CLAIM 17	50
S. CLAIM 18	50
T. CLAIM 19	50
U. CLAIM 20	50
V. CLAIM 21	51
W. CLAIM 22.....	51
X. INDEPENDENT CLAIM 23.....	51
Y. CLAIM 24	53
Z. CLAIM 25	53
AA. CLAIM 26.....	53
BB. CLAIM 27.....	53
X. GROUND 3: CLAIMS 1-27 ARE RENDERED OBVIOUS OVER SUGIYAMA IN VIEW OF PARKHE, NATSUHARA, CRIMINALE, AND KNOWLEDGE OF A POSITA	53
A. OVERVIEW OF GROUND 3.....	53
B. INDEPENDENT CLAIM 1.....	56
C. CLAIM 2	59

D. CLAIM 3	59
E. CLAIM 4	60
F. CLAIM 5	60
G. CLAIM 6	61
H. CLAIM 7	61
I. CLAIM 8	61
J. CLAIM 9	62
K. CLAIM 10	63
L. CLAIM 11	63
M. CLAIM 12	63
N. CLAIM 13	64
O. CLAIM 14	65
P. INDEPENDENT CLAIM 15.....	66
Q. CLAIM 16	67
R. CLAIM 17	67
S. CLAIM 18	67
T. CLAIM 19	67
U. CLAIM 20	67
V. CLAIM 21	68
W. CLAIM 22.....	68
X. INDEPENDENT CLAIM 23.....	68
Y. CLAIM 24	70
Z. CLAIM 25	70

AA. CLAIM 26.....	70
BB. CLAIM 27.....	70
XI. GROUNDS FOR STANDING.....	70
XII. MANDATORY NOTICES	70
XIII. CONCLUSION	73
XIV. CLAIMS APPENDIX.....	74

TABLE OF AUTHORITIES

Statutes and Other Authorities

35 U.S.C. § 102	8
35 U.S.C. § 103	<i>passim</i>
35 U.S.C. §§ 311-319	2
37 C.F.R. § 42.100	2

EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 12,320,841 (“the ’841 Patent”)
1002	Excerpts of File history of the ’841 Patent, Part 1
1003	Declaration of Joseph McAlexander III, P.E.
1004	<i>Curriculum Vitae</i> of Joseph McAlexander III, P.E.
1005	Declaration of Pradeep Lall, Ph.D.
1006	<i>Curriculum Vitae</i> of Pradeep Lall, Ph.D.
1007	U.S. Patent No. 6,549,026 (“DiBattista”)
1008	U.S. Patent Application Publication No. 2011/0000426 (“Herchen-1”)
1009	U.S. Patent Application Publication No. 2008/0160462 (“Herchen-2”)
1010	U.S. Patent Application Publication No. 2013/0220989 (“Pease”)
1011	U.S. Patent Application Publication No. 2004/0227536 (“Sugiyama”)
1012	U.S. Patent Application Publication No. 2002/0017916 (“Costello”)
1013	U.S. Patent Application Publication No. 2016/0111315 (“Parkhe”)
1014	U.S. Patent Application Publication No. 2003/0155939 (“Lutz”)
1015	U.S. Patent Application Publication No. 2007/0205787 (“Natsuhara”)

1016	U.S. Patent Application Publication No. 2017/0347492 (“Cola”)
1017	U.S. Patent Application Publication No. 2020/0294836 (“Criminale”)
1018	Excerpts of File history of the ’841 Patent, Part 2

I. INTRODUCTION

AEM Americas, Inc. (“Petitioner”) petitions for *inter partes* review and cancellation of claims 1-27 of U.S. Patent No. 12,320,841 (“the ’841 Patent,” EX1001), assigned to Advantest Test Solutions, Inc. (“Patent Owner”). The challenged claims recite a wafer-test system that uses a wafer thermal interposer layer to selectively heat areas of a semiconductor wafer while a cold plate cools it, all coordinated by a thermal controller during testing. That architecture was not new. It was disclosed years earlier through numerous references.

II. TECHNOLOGY BACKGROUND

Integrated-circuit devices are tested before shipment to verify performance; and it is desirable to test them as early as possible so non-functioning devices can be removed before further expensive processing is incurred. U.S. Patent No. 6,549,026 to DiBattista et al. (“DiBattista”) at 1:26-31. The earliest stage at which full functionality can be tested is at the wafer level, in a process “often known as ‘wafer probing,’” in which “temporary contacts such as needles are placed into electrical contact with pads formed on the device, such as for power and input/output signals” and “[a] test pattern is then applied via these pads.” DiBattista at 1:34-43.

Controlling device temperature during test has long been recognized as necessary because devices self-heat during operation. The conventional approach in wafer probing was “to provide a thermal mass in the form of a heated and/or cooled

chuck on which the wafer is placed during testing,” but such a single-mass chuck cannot “respond to localized temperature changes arising from an individual high performance device on a wafer being tested at speed.” DiBattista at 2:41-52. DiBattista and others solved that problem by providing per-device, zone-level temperature control during test - the same solution the ’841 Patent claimed two decades later.

III. STATEMENT OF PRECISE RELIEF REQUESTED

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100 et seq., Petitioner requests *inter partes* review and cancellation of claims 1-27 of the ’841 Patent on the following ground:

Ground 1: Claims 1-27 are rendered obvious over DiBattista in view of Herchen-1, Herchen-2, Pease, and Natsuhara under 35 U.S.C. § 103.

Ground 2: Claims 1-27 are rendered obvious over DiBattista in view of Costello, Herchen-1, and Criminale under 35 U.S.C. § 103.

Ground 3: Claims 1-27 are rendered obvious over Sugiyama in view of Parkhe, Natsuhara, Criminale, and knowledge of a POSITA under 35 U.S.C. § 103.

IV. THE ’841 PATENT

The ’841 Patent is directed to a wafer-scale active thermal interposer system for device testing. It issued June 3, 2025 from Application No. 17/528,002, filed November 16, 2021, and claims priority to Provisional Application No. 63/115,813,

filed November 19, 2020. For purposes of this Petition, the effective filing date of claims 1-27 of the '841 Patent is November 19, 2020.

The '841 Patent describes a system in which a wafer probe contacts one surface of a wafer while a wafer thermal interposer (TI) layer contacts the opposite surface and selectively heats zones corresponding to areas of the wafer, a cold plate cools the wafer, and a thermal controller coordinates heating and cooling during test.

A. SPECIFICATION AND CLAIMS

The challenged independent claims (claims 1, 15, and 23) recite a wafer-test architecture built from four cooperating components: (i) a test computer or test computer system that generates input signals, processes output signals, and generates a test result; (ii) a wafer probe that contacts a surface of the wafer to probe individual circuits; (iii) a wafer TI layer that contacts the opposite surface and, through a plurality of resistive traces (claim 1) or discretely controllable thermal zones (claim 15), selectively heats areas of the wafer; and (iv) a cold plate and thermal controller that cool the wafer and coordinate selective heating during testing. Independent claim 23 recites a corresponding method. The dependent claims add features such as zone-to-die correspondence (claims 2, 9, 10, 16, 17), a chiller and flow-control valve (claim 3), thermal interface material layers (claims 4-6, 22), vacuum and blow-off valves (claims 7, 8), a pin lift mechanism (claim 12), pulse-width-modulated power

(claim 13), a grounded shield (claim 14), and preconditioning methods (claims 20, 21, 25, 26.

According to the '841 Patent, integrated circuits are electrically tested while heated and/or cooled to their specification limits. Traditional chamber-based testing is slow and imprecise because of the large air volume and mounting mass, and even newer “chamber-less” systems that heat/cool the device directly struggle with cooling during test. The patent states that, while wafer-level testing is desirable for throughput and early defect screening, precise heating and/or cooling of an individual die within a wafer is not available under the conventional art. The '841 Patent discloses a system which pairs a tester and wafer probe card with a “test stack:” a wafer probe contacting the first (circuit) surface of the wafer, a wafer thermal interposer (TI) layer contacting the second (back) surface to selectively heat areas of the wafer, and a cold plate under the TI layer to cool the wafer. A thermal controller maintains the temperatures of wafer areas by controlling both the cold-plate cooling and the selective heating of the TI layer.

The thermal interposer layer (“TI layer”) contains a plurality of discrete, separately controllable heating elements that apply heat to regions of the wafer corresponding in location and shape to the dice. The heating elements comprise resistive traces on a ceramic substrate - e.g., an aluminum nitride base with tungsten/molybdenum traces (HTCC) for higher-power devices, or an alumina

LTCC process for lower-power devices - though Peltier devices or any suitable heating and/or cooling technology may be used. Zone layout is exemplary and may be customized to the die layout; a single region may span multiple dice (e.g., ~9 dice). Temperature-measurement devices (e.g., thermocouples) feed the controller for closed-loop control. '841 Patent, 9:4-10, 8:63-65.

A chiller cools circulating fluid (e.g., glycol) to the cold plate through a controller-regulated valve; the controller adjusts both cold-plate temperature and heater power based on temperature feedback and may pulse-width modulate the heater voltage. '841 Patent, 8:28-44. Different wafer regions can be held at different temperatures, producing a thermal gradient across the wafer. The controller may implement processes from the inventors' incorporated-by-reference patent on "Adaptive Thermal Control." '841 Patent, 8:45-54.

B. PROSECUTION HISTORY

The '841 Patent issued from Application No. 17/528,002 ("the '002 Application"). None of the references in this Petition were applied by the Examiner during prosecution.

The '002 Application was filed November 16, 2021 and claims the benefit of provisional application No. 63/115,813, filed November 19, 2020. On May 4, 2022, applicant filed a preliminary amendment cancelling original claims 1-26 and adding new claims 27-53. EX1002; EX1018. On December 7, 2023, the Examiner issued a

non-final office action. The sole substantive rejection came in the non-final office action of pending claims 27-53, which is summarized below:

- § 102(a)(2) - anticipation. Claims 27-29, 36-38, and 41-45 were rejected as anticipated by Chiang et al. (US 2019/0162777), based on Chiang's test system, wafer probe, thermal interposer, and cold plate
- § 103 - obviousness. Claims 35 and 40 were rejected over Chiang in view of Narasaki et al. (US 9,766,287); claim 39 over Chiang in view of Barabi et al. (US 10,126,356).

The Examiner noted that claims 30-34 and 46-48 would be allowable if rewritten in independent form and claims 49-53 were allowed outright. EX1002; EX1018.

An Examiner interview was held by telephone on March 13, 2024, addressing the Chiang reference; the Examiner indicated the arguments were persuasive. On March 15, 2024, Applicant filed an amendment and response, making claim amendments and arguing that Chiang's device-under-test does not "inherently" contain a plurality of dice, and inherency cannot rest on mere possibility. EX1002; EX1018. The Applicant also argued that the Examiner's reading of the DUT as containing infinite "infinitesimal unit squares" (dice) was untenable and that Chiang's "socket 100" is not a "wafer probe," and its thermal plate 720 and controller heat the entire DUT to a single setpoint rather than selectively heating discrete zones as claimed. Ex. 1002.

The Examiner found the March 15, 2024 arguments persuasive and withdrew the § 102 and § 103 rejections of claims 27-29, 35-45. The stated reasons for allowance were that the prior art neither showed nor suggested the claimed combination - a wafer probe contacting a first surface, a wafer thermal-interposer layer with resistive elements selectively heating a plurality of zones, a cold plate, and a thermal controller. EX1002; EX1018.

V. PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) as of the November 19, 2020 effective filing date would have held at least a bachelor’s degree in electrical engineering, mechanical engineering, or a related field, together with approximately two to three years of experience in semiconductor test equipment or thermal management of electronic devices. Additional education could substitute for experience, and vice versa. The analysis in this Petition does not change under any reasonable alternative definition. EX1003, ¶¶29-32, EX1005, ¶¶37-40.

VI. CLAIM CONSTRUCTION

In this proceeding, the challenged claims are given their ordinary and customary meaning as understood by a POSITA at the time of the invention, in light of the specification and the prosecution history. Petitioner submits that no term requires express construction to resolve the challenges below.

VII. IDENTIFICATION OF CHALLENGES AND PRIMARY PRIOR ART

Systems for controlling the temperature of integrated-circuit devices during wafer-level testing existed long before the November 19, 2020 effective filing date of the '841 Patent. The prior art relied upon in this Petition predates that effective filing date by a number of years (and sometimes decades) and thus qualifies as prior art under 35 U.S.C. § 102(a)(1) and cannot be excepted under 35 U.S.C. § 102(b)(1).

Petitioner's challenge is set forth in Grounds 1-3 below.

A. Reference #1: DiBattista (U.S. Patent No. 6,549,026 B1)

DiBattista, titled "Apparatus and Method for Temperature Control of IC Device During Test," issued April 15, 2003 and was filed July 14, 2000. It names Larry DiBattista, Mark Malinoski, and Tomoya Shitara as inventors and Delta Design, Inc. as assignee.

DiBattista discloses "an apparatus for controlling the temperature, during testing, of IC devices formed on a wafer" that "includes a chuck for locating the devices during testing and multiple temperature control devices arranged on the chuck to correspond with the arrangement of the devices being tested on the wafer." DiBattista, Abstract. As shown in Figs. 2A-2C and 4, the chuck is fluid-cooled and carries an array 129 of independently controlled resistive heating elements 149, each sized and shaped to a corresponding IC device on the wafer, all governed by a temperature control system 140 during test. As shown below, DiBattista discloses the same wafer-test architecture claimed in the '841 Patent.

DiBattista issued April 15, 2003-more than seventeen years before the effective filing date-and is, therefore, non-excepted prior art to the '841 Patent.

B. Reference #2: Herchen-1 (U.S. Patent Application Publication No. 2011/0000426)

Herchen-1 is titled “Substrate Processing Apparatus with Heater Element Held by Vacuum,” and published January 6, 2011, naming Harald Herchen as inventor and assigned to Sokudo Co., Ltd. It claims the benefit of a provisional application filed July 6, 2009. Because it was published more than nine years before the '841 Patent's November 19, 2020 effective filing date, Herchen-1 qualifies as prior art.

Herchen-1 describes a semiconductor substrate heating apparatus - a bake plate for a track-lithography tool - built around a layered heater held between two planar plates by vacuum. Herchen-1, Abstract. Herchen-1 discloses patterned, zone-selective resistive heater traces. Herchen-1 discloses a conducting layer 304 (Fig. 3) whose heater elements are “arranged in a predetermined pattern,” “etched onto conducting layer 304,” and “arranged to form six independent heating zones with a separate temperature sensor for each zone,” each individually controlled, within a multi-layer stack of alternating insulating and conducting layers. *See, e.g.*, Herchen-1 at [0051].

Herchen-1 discloses a movable top cooling plate 220, raised and lowered by air cylinders, together with a non-movable bottom cooling plate 230 having “one or more fluid channels” for a coolant such as deionized water - positioned below the heater-bearing planar members to draw heat away. *See, e.g.*, Herchen-1 at [0050].

A top cooling plate carries thermal material 221, a Kapton thermal pad on its upper surface that aids in efficient removal of heat. *See, e.g.*, Herchen-1 at [0049]. Herchen-1 also discloses that a plurality of lift pins holes 210 may extend from a lower surface of bottom planar member 203 to the upper surface of top planar member 201, with lift pins passing through during load/unload. It also discloses vacuum ports that hold the substrate down and, when the inter-plate region is evacuated, trap the heater layer between the plates, all fed by a common house vacuum system. *See, e.g.*, Herchen-1 at [0045].

C. Reference #3: Herchen-2 (U.S. Patent Application Publication No. 2008/0160462)

Herchen-2 is titled “Method and System for Bake Plate Heat Transfer Control in Track Lithography Tools,” and published July 3, 2008, naming Harald Herchen, Kim Vellore, and Erica Renee Porras as inventors and assigned to Sokudo Co., Ltd. It claims the benefit of a provisional application filed January 3, 2007. Because it was published more than nine years before the ’841 Patent’s November 19, 2020 effective filing date, Herchen-2 qualifies as prior art.

Herchen-2 discloses methods and systems to measure wafer shape and actively control bake plate heat transfer in track lithography tools to improve thermal uniformity. Herchen-2, Abstract. A thermal unit includes a bake plate with a process surface, electrodes for capacitive sensing, proximity pins, flexible members coupling the plate to a chill plate, and chambers supplied with controllable pressurized fluid. *See, e.g.*, Herchen-2 at [0046-47]. The system can apply vacuum to draw the plate into contact with a chill plate for rapid, particle free cooling during or after baking. *See, e.g.*, Herchen-2 at [0056].

D. Reference #4: Pease (U.S. Patent Application Publication No. 2013/0220989)

Pease is titled “Multiplexed Heater Array Using AC Drive for Semiconductor Processing,” and published August 29, 2013. Inventors are John Pease and Nell Benjamin. Because it published more than seven years before the ’841 Patent’s November 19, 2020 effective filing date, Pease qualifies as prior art.

Pease describes a heating plate for a substrate-support assembly (an electrostatic chuck) in a semiconductor plasma-processing apparatus, built around a scalable, multiplexed array of independently controllable planar heater zones over a fluid-cooled cooling plate. Pease, Abstract. Pease discloses fine, die-scale, independently controllable heating zones. Pease, [0017]. Pease teaches that the substrate support assembly includes multiple independently controllable planar

heater zones that enable the apparatus to actively create and maintain the desired spatial and temporal temperature profile. Each zone is of similar size to or smaller than a single device die or group of device dies on the substrate so that the substrate temperature can be controlled for each device die position to maximize the yield of devices from the substrate, and the “scalable architecture” accommodates “die-by-die substrate temperature control (typically more than 100 dies on a substrate of 300-mm diameter).” Pease, [0030].

Pease’s heater elements “may be thin film resistive heaters” and “may be screen printed, wire wound or etched foil heaters.” Pease, [0017]. Further, Pease discloses pulse-width-modulation power control. Pease discloses a controller 1000 that includes a DC power supply, an AC power supply, and logic (hardware or software) to control at least one power supply, and teaches that digital switching control “is then effected by time division multiplexing and Pulse Width Modulation (PWM) techniques.” Pease, [0050].

Pease also discloses “a cooling plate 105 containing channels 106 for coolant flow” (a fluid-cooled heat sink), and states that the assembly can comprise features such as lift pins for lifting the substrate,” with lead wires routed “through holes or conduits in the cooling plate. Pease, [0018].

E. Reference #5: Sugiyama (U.S. Patent Application Publication No. 2004/0227536)

Sugiyama is titled “Prober and Probe Testing Method for Temperature-Controlling Object to be Tested,” and published November 18, 2004. Listed inventors are Masahiko Sugiyama and Yoshinori Inoue. Because it published decades before the ’841 Patent’s November 19, 2020 effective filing date, Sugiyama qualifies as prior art.

Sugiyama discloses probers and probe-testing methods that electrically test devices on a wafer under controlled temperature with improved speed and accuracy. Sugiyama, Abstract. Conventional probers heat or cool large chuck areas and can tilt under probe pressure at wafer edges, causing contact errors and inefficiency. Sugiyama disclosed a main chuck with multiple heaters sized to individual devices or device groups, each with a temperature sensor, and a heat exchanger governed by a temperature controller. Sugiyama, [0020]. These heaters are disclosed as being arranged as cell structures aligned to device locations, with each cell including its own heater, sensor, and heat exchanger, with heat insulators between cells. Sugiyama, [0022]. The controller independently regulates heaters and cooling based on sensor feedback to set predetermined temperatures at selected cells.

F. Reference #6: Costello (U.S. Patent Application Publication No. 2002/0017916)

Costello is titled “Temperature-Controlled Semiconductor Wafer Chuck System,” and published February 14, 2002. Listed inventors are Simon Costello and

Tuyen Pham. Because it published decades before the '841 Patent's November 19, 2020 effective filing date, Costello qualifies as prior art.

Costello discloses a temperature-controlled semiconductor wafer chuck system designed for prober stations to independently control top and bottom chuck temperatures while maintaining mechanical rigidity. Costello, Abstract. The system uses a multilayer heat sink with an internal coolant conduit divided by load-bearing pillars to remove heat and to transmit probe forces without significant deformation. Costello, [0012]. A primary heater is positioned near the top surface to directly heat the wafer side, and a secondary heater is positioned near the bottom surface to regulate the chuck base temperature. The heat sink conduit is preferably U-shaped with adjacent inlet and outlet, formed by machining or casting, and incorporates pillars arranged substantially uniformly with corners to promote turbulent coolant flow. Materials such as aluminum or stainless steel are used and layers are vacuum or dip brazed to form an integral, stiff structure including heater cover plates and a base plate. Through-holes accommodate wafer loading pins, and the chuck top surface has vacuum grooves for wafer hold-down. Costello, [0080]. Embodiments include a ceramic insulation layer between the heat sink and the prober stage for thermal and electrical isolation, with optional secondary cooling channels in the insulator. Costello, [0049], [0054].

G. Reference #7: Parkhe (U.S. Patent Application Publication No.

2016/0111315)

Parkhe is titled “Electrostatic Chuck Assembly for High Temperature Processes,” and published April 21, 2016. The listed inventor is Vijay Parkhe. Because it published before the ’841 Patent’s November 19, 2020 effective filing date, Parkhe qualifies as prior art.

Parkhe discloses an electrostatic chuck assembly designed for high temperature semiconductor processing, featuring a puck metal-bonded to a cooling plate and fastened for uniform load and heat transfer. Parkhe, Abstract. The puck includes an electrically insulative upper puck plate with embedded heating elements and electrodes, bonded to a lower puck plate by a metal bond such as an aluminum or AlSi alloy diffusion bond. Parkhe, [0046]. The lower puck plate has multiple fastener-accommodating features arranged at different radii from center to distribute approximately equal fastening force. The cooling plate is mechanically coupled to the puck through these fasteners to promote uniform thermal contact and predictable heat transfer.

The assembly can keep the puck at about 180-300° C while the cooling plate remains below about 120° C, enabling high temperature processing with thermal isolation. Parkhe, [0053]. In another embodiment, the cooling plate includes a base and a spring-loaded inner heat sink with springs pressing the heat sink against the

puck, optionally with a low thermal conductivity gasket and an optional grafoil layer. Parkhe, [0052].

VIII. GROUND 1: Claims 1-27 are Rendered Obvious Over DiBattista in View of Herchen-1, Herchen-2, Pease, and Natsuhara

A. OVERVIEW OF GROUND 1

DiBattista discloses a wafer-level test system in which an array 129 of independently controlled resistive heating elements 149 is disposed on a fluid-cooled chuck 122 in one-to-one correspondence with the integrated-circuit devices under test on the wafer, and in which a temperature control system 140 maintains each device at a set-point temperature by controlling both the liquid cooling of the chuck and the selective heating of the individual elements. DiBattista at 6:7-16, 6:21-37, 6:38-42, 7:37-44, 7:59-8:2, 8:50-57. DiBattista, therefore, supplies the test architecture, the zone-selective heating mapped to circuit positions, the cold plate, and the dual heating-and-cooling thermal controller recited in claim 1.

To the extent the Patent Owner contends that DiBattista's array of trace-based heating elements does not, standing alone, satisfy the requirement of "a plurality of resistive traces traversing said wafer TI layer" arranged to selectively heat "a plurality of zones" corresponding to areas of the wafer, Herchen-1 expressly discloses that limitation. Herchen-1 discloses a heater layer in which a conducting layer 304 carries heater elements arranged in a predetermined pattern, etched onto the conducting layer and arranged to form six independent heating zones, each

individually controlled and each having a separate temperature sensor. Herchen-1 at [0051], [0054], FIG. 5. Herchen-1 further discloses a movable top cooling plate 220 and a fluid-channel bottom cooling plate 230 positioned below the heater-bearing planar members, together with lift-pin holes 210 extending through the plate stack. Herchen-1 at [0048]-[0050].

DiBattista discloses the wafer-test architecture recited in claim 1, including an array 129 of independently controlled resistive heating elements 149 disposed on a fluid-cooled chuck in correspondence with the integrated-circuit devices under test, each element implemented with a “heater trace” that “provides the heat energy,” each “controlled independently of the others,” and a temperature control system 140 that maintains each device at a set-point temperature. DiBattista at 6:7-16, 6:21-37, 6:38-42, 7:59-8:2.

Pease supplies the added features of the dependent claims addressed in this Ground. Pease discloses “multiple independently controllable planar heater zones in the substrate support assembly to enable the apparatus to actively create and maintain the desired spatial and temporal temperature profile,” Pease at [0014], in which each zone is “of similar size to or smaller than a single device die or group of device dies on the substrate so that the substrate temperature . . . can be controlled for each device die position to maximize the yield of devices from the substrate.” Pease at [0030]. Pease’s “scalable architecture” accommodates “die-by-die substrate

temperature control (typically more than 100 dies on a substrate of 300-mm diameter),” Pease at [0030], with a heating plate that “can have at least 10, at least 100 and up to 1000 heater zones.” Pease at [0049]. The heater elements “may be thin film resistive heaters” and “may be screen printed, wire wound or etched foil heaters.” Pease at [0017]. Pease further discloses a controller 1000 that includes “logic (hardware or software) to control at least one power supply,” Pease at [0041], digital power control in which “control is then effected by time division multiplexing and Pulse Width Modulation (PWM) techniques,” Pease at [0050], “a cooling plate 105 containing channels 106 for coolant flow,” Pease at [0018], and “lift pins for lifting the substrate.” Pease at [0030].

A person of ordinary skill in the art would have had a reasonable expectation of success in combining these references. EX1003, ¶¶53-56, EX1005, ¶¶137. A person of skill in the art would have been motivated to combine DiBattista and Pease in order to have more directed control of temperature in areas immediately surrounding a die under test to achieve greater temperature control and uniformity. EX1005, ¶¶137.

A person of ordinary skill in the art would have been motivated to combine DiBattista and Herchen-1. Both references address the same problem - spatially controlled, zone-selective heating of a wafer-scale substrate using a patterned resistive heater layer over a liquid-cooled plate. Implementing DiBattista’s per-die

heater array with Herchen-1's etched, patterned resistive heater traces arranged in individually controlled zones traversing the heater layer amounts to no more than applying a known heater-trace construction to a known wafer-test chuck ready for improvement, combining prior-art elements according to known methods to yield the entirely predictable result of zone-selective heating mapped to the die layout. A skilled artisan would have had a reasonable expectation of success in doing so. EX1003, ¶¶58-60; EX1005, ¶¶138-39.

Further, combining with Herchen-2 would have been obvious. Herchen-1 and Herchen-2 share an inventor. Both references are directed to thermal processing in track lithography tools used for photolithography sequences including bake and chill operations in multi-chamber systems. Herchen-2 addresses non-uniform heat transfer arising from wafer bow and varying wafer-to-plate air gaps and provides methods to measure wafer shape and compensate by deforming a flexible bake plate using chambered pressure control. Herchen-1 addresses limitations of conventional heaters that are bonded or printed onto plates, including CTE mismatch warping, maintenance cost, and inflexibility, by holding a multilayer heater between top and bottom planar members using vacuum in an evacuated region.

Herchen-2 teaches that gap non-uniformity from wafer bow degrades uniform heating and proposes active plate shape control via chamber pressures informed by capacitive measurements. Herchen-1 teaches vacuum-held heater layers to avoid

CTE-induced warping from permanent bonds and to enable easy replacement or reconfiguration of heater elements, reducing CoO. A POSITA would have recognized that integrating a vacuum-retained multilayer heater (Herchen-1) with a deformable, pressure-actuated bake plate with sensing (Herchen-2) addresses both heat-transfer uniformity and maintainability in the same thermal module, thereby maintaining uniform wafer-to-interposer contact so that each resistive-trace zone selectively heats its corresponding area of a bowed wafer uniformly during test. EX1003, ¶¶61-65; EX1005, ¶¶140-43.

Further, Herchen-2 contemplates heater elements embedded in or forming electrodes on a thin bake plate surface, and multi-zone heating is conventional in this context. EX1005, ¶¶142. Herchen-1 provides a known multilayer heater architecture with single- and multi-zone patterns that is designed to be sandwiched between planar members and held by vacuum. Substituting Herchen-1's multilayer, vacuum-held heater for the heater implementation in Herchen-2's bake plate is a like-for-like swap of heater technology in an established bake plate assembly to achieve predictable heating functionality with improved serviceability. EX1005, ¶¶142; EX1003, ¶¶63.

B. INDEPENDENT CLAIM 1

DiBattista in view of Herchen-1, Herchen-2, and Pease render obvious every limitation of claim 1, as set forth element-by-element below.

1. [1.pre]

DiBattista discloses a system for “the temperature control of integrated circuit (‘IC’) devices during testing . . . at wafer level.” DiBattista at 1:19-22. DiBattista provides “a method for testing IC devices at wafer level in which the temperature of each device on the wafer is controlled independently of the other devices on the wafer during a test.” DiBattista at 12:25-30. To the extent the preamble is limiting, DiBattista discloses it.

2. [1.a]

DiBattista discloses a test head interface 130 providing electrical connections to the power and input/output pads on the devices, coupled to the test head of an available test system, “such as the ITS 9000 IX . . . of Schlumberger Technologies, Inc.” DiBattista at 7:50-58. Functional testing is performed to “verify performance” of the devices, generating a test result. DiBattista at 1:26-31.

3. [1.b]

DiBattista discloses a wafer prober 100 including a stage 110 carrying a chuck 120 that carries the wafer on which the IC devices are formed. DiBattista at 7:37-44. In wafer probing, “temporary contacts such as needles are placed into electrical contact with pads formed on the device,” contacting the surface of the wafer to probe the individual devices. DiBattista at 1:34-43.

4. [1.c]

DiBattista discloses an array 129 of heating elements 149 disposed on the upper surface of the chuck between the chuck and the wafer, where “[e]ach heating element 149 in the array 129 has a size and shape corresponding to that of the associated IC device to be tested on the wafer and the pattern of heating elements 149 matches that of the devices on the wafer,” so that “each device will be sitting on top of a heating element 149.” DiBattista at 6:21-37. The heating elements are “resistive heaters,” each implemented with a “heater trace” that “provides the heat energy.” DiBattista at 6:7-16. Each heating element is controlled independently of the others, providing selective heating of areas of the wafer in one-to-one correspondence with the devices under test. DiBattista at 6:38-42, 5:54-61, 12:25-30.

To the extent the Patent Owner contends that DiBattista’s trace-based heating elements do not literally constitute “a plurality of resistive traces traversing said wafer TI layer” arranged to heat “a plurality of zones,” it would have been obvious to implement DiBattista’s heater array using the patterned resistive heater traces taught by Herchen-1. Herchen-1 discloses a conducting layer 304 whose heater elements are “arranged in a predetermined pattern,” “etched onto conducting layer 304,” and “arranged to form six independent heating zones with a separate temperature sensor for each zone,” each individually controlled. Herchen-1 at [0051]; *see also id.* at [0054], FIG. 5. Applying Herchen-1’s etched, zone-forming

resistive traces to DiBattista's wafer-test chuck yields the claimed plurality of resistive traces traversing the layer and selectively heating a plurality of zones corresponding to areas of the wafer.

5. [1.d]

DiBattista discloses a fluid-cooled chuck 122 incorporating a fluid cavity 124, a fluid inlet 126, and a fluid outlet 128, disposed adjacent to the array 129 of heating elements. DiBattista at 6:21-37. The chuck "acts as a heat sink by absorbing heat energy from the heating element 149," cooling the wafer. DiBattista at 8:50-57. Herchen-1 likewise discloses a movable top cooling plate 220 and a non-movable bottom cooling plate 230 having "one or more fluid channels" positioned below the heater-bearing planar members to draw heat away. Herchen-1 at [0049]-[0050].

6. [1.e]

DiBattista discloses a temperature control system 140 comprising a system controller 160 and a liquid cooling and recirculation system 170. DiBattista at 7:59-8:2. The temperature of the fluid can be adjusted. DiBattista at 8:12-32. The system supplies a heater power signal to each heating element 149. DiBattista at 9:16-22. Using multiple boards, it enables "simultaneous operation of a plurality of heating elements 149," each thermally coupled to individual devices. DiBattista at 9:44-55. A "feedback loop is used to control the operation of the heating element while the liquid cooled heat exchanger is operated as a set point heat sink," thereby selectively

heating and maintaining temperatures during testing by controlling both the cold plate and the resistive heating elements. DiBattista at 12:19-24.

C. CLAIM 2

DiBattista in view of Herchen-1 renders claim 2 obvious. In DiBattista, “[e]ach heating element 149 in the array 129 has a size and shape corresponding to that of the associated IC device to be tested on the wafer and the pattern of heating elements 149 matches that of the devices on the wafer.” DiBattista at 6:21-37. The regions of the chuck “correspond to respective ones of the plurality of integrated circuit devices formed on the wafer,” so the positions of the heating zones correspond to, and the layer is customized for, the die layout of the wafer. DiBattista at 3:15-20. Herchen-1’s etched heater elements likewise are arranged in a predetermined pattern forming individually controlled zones. Herchen-1 at [0051]. EX1003, ¶66.

D. CLAIM 3

DiBattista discloses this claim. Its liquid cooling and recirculating system 170 “includes a chiller system 200, a filter 210, and a flow control 212,” and the chiller system comprises a “pressurized coolant reservoir 202, a pump 204, a heat exchange (heating/cooling) system 206, a temperature sensor 208, and a pressure relief valve 218.” DiBattista at 8:12-18. The flow control 212 regulates the coolant flowing to the fluid-cooled chuck (cold plate), and the cooling and recirculating system 170 is

part of, and controlled by, the temperature control system 140. DiBattista at 7:59-8:2.

E. CLAIM 4

Herchen-1 discloses a thermal interface material between the heater-bearing planar member and the cooling plate: cooling plate 220 “may include thermal material 221 disposed on its upper surface,” a “thermal pad” that “aid[s] in efficient removal of heat from the lower planar member.” Herchen-1 at [0049]. It would have been obvious to provide such a TIM layer both between the cold plate and the wafer TI layer and between the wafer TI layer and the wafer of the DiBattista-Herchen-1 system, as the mere duplication of a known thermal-interface layer to improve heat transfer at each interface yields a predictable result. EX1005, ¶144.

F. CLAIM 5

Herchen-1 discloses a thermal-interface pad (Kapton® thermal material 221) at the cooling interface. Herchen-1 at [0049]. Indium foil is a well-known compliant TIM, as confirmed by expert testimony and by the prior art disclosing compliant thermal-interface materials used to improve heat transfer across stacked wafer-test interfaces. *See generally* Cola (EX1016) at [0019], [0086]; EX1005, ¶145. Indium would have been an obvious choice among a limited number of known thermal-interface materials.

G. CLAIM 6

As with claim 5, Herchen-1 discloses a thermal-interface pad at the cooling interface, Herchen-1 at [0049]. Graphite is a well-known compliant TIM, as confirmed by expert testimony and by the prior art disclosing compliant thermal-interface materials used to improve heat transfer across stacked wafer-test interfaces. *See generally* Cola (EX1016) at [0167], [0171]; EX1005, ¶146. Graphite would have been an obvious choice among a limited number of known thermal-interface materials. *See also* Herchen-2 at [0042], [0044], [0052].

H. CLAIM 7

Herchen-1 discloses vacuum securing at both interfaces through a single vacuum source. Vacuum ports 214 in the top planar member secure the substrate by “applying vacuum on the backside of the substrate,” Herchen-1 at [0046], and vacuum applied to region 202 through vacuum port 213 draws the planar members together and traps the heater layer 215 between them. Herchen-1 at [0047]. Vacuum ports 222 provide a “cooling path” and “uniform load” between the lower planar member 203 and the cooling plate 220. Herchen-1 at [0049]. Each vacuum line is regulated (regulators 251, 261, 271) and connected to a common “house vacuum system 290,” which corresponds to the recited vacuum pump coupled to both vacuum valves. Herchen-1 at [0046]-[0049]. It would have been obvious to secure the wafer to the wafer TI layer and the wafer TI layer to the cold plate of the DiBattista-Herchen-1 system using these known vacuum arrangements.

I. CLAIM 8

Herchen-1 discloses regulated vacuum lines at both interfaces (ports 214 and 222, regulators 251, 271, house vacuum system 290) that are relieved to release the substrate and separate the plates during load/unload. Herchen-1 at [0046]-[0049]. It would have been obvious to a POSITA to use a positive-pressure blow-off valve or an air source for releasing the wafer. Releasing a vacuum-secured substrate with a positive air pulse is a conventional complement to vacuuming. EX1003, ¶67.

J. CLAIM 9

DiBattista discloses this claim. Its heating elements 149 and the DUTs 182 are “preferably in a one-to-one correspondence,” which “provides the ability to control independently the temperature of each DUT 182 during a test.” DiBattista at 5:54-61. Because “each device will be sitting on top of a heating element 149,” each heating zone corresponds to a respective single die of the die layout. DiBattista at 6:21-37.

K. CLAIM 10

DiBattista teaches that each heating element has “a size and shape corresponding to that of the associated IC device,” DiBattista at 6:21-37, and Herchen-1 teaches a conducting layer 304 whose heater elements form a limited number of individually controlled zones (e.g., six independent zones), Herchen-1 at [0051]. It would have been obvious to size the zones of the DiBattista-Herchen-1

heater layer so that each zone corresponds to a respective plurality of dice, as a matter of routine design choice in matching zone granularity to the die layout, yielding predictable temperature control of groups of dice. EX1003, ¶68.

L. CLAIM 11

DiBattista in view of Pease renders claim 11 obvious. DiBattista discloses per-device heating elements each having “a size and shape corresponding to that of the associated IC device,” each “controlled independently of the others.” DiBattista at 6:21-37, 6:38-42. Pease discloses that the planar heater zones can be made finer than a die: “each planar heater zone of the heating plate is of similar size to or smaller than a single device die or group of device dies on the substrate so that the substrate temperature . . . can be controlled for each device die position to maximize the yield of devices from the substrate.” Pease at [0030]. Pease’s “scalable architecture” accommodates “die-by-die substrate temperature control (typically more than 100 dies on a substrate of 300-mm diameter),” Pease at [0030], and the heating plate “can have at least 10, at least 100 and up to 1000 heater zones.” Pease at [0049]. Applying Pease’s sub-die zone granularity to DiBattista’s wafer-test chuck yields a wafer TI layer in which each die of the die layout corresponds to multiple respective zones, achieving the predictable benefit of finer intra-die thermal control. EX1003, ¶69.

M. CLAIM 12

DiBattista in view of Pease renders claim 12 obvious. Pease discloses a lift-pin mechanism for the substrate support. Although the pins are not separately illustrated, Pease teaches that “the substrate support assembly can comprise features such as lift pins for lifting the substrate,” Pease at [0030], and describes “a lifting pin arrangement for raising and lowering a substrate.” Pease at [0055]. Pease further discloses routing conductors “through holes or conduits in the cooling plate,” Pease at [0040], with “feedthroughs in the cooling plate,” Pease at [0030], confirming that vertical pass-through features extending through the cooling plate were conventional. It would have been obvious to provide DiBattista’s fluid-cooled chuck with Pease’s lift-pin arrangement and to align the pass-through channels through both the cold plate and the wafer TI layer, so that the pins pass through both the cold plate and the wafer TI layer to lift the wafer. A POSITA would have been motivated to add such a lift-pin mechanism to load and unload wafers from the heated surface without side access. EX1003, ¶70.

N. CLAIM 13

DiBattista in view of Pease discloses this claim. DiBattista discloses a power amplifier 258 that “provides a heater power I_h to the heating element 149” under control of the temperature control system. DiBattista at 9:16-22. Pease supplies the pulse-width-modulation control of the heater power supply. Pease teaches that the switching/control circuits that distribute power to the heater zones may use digital

control, in which “control is then effected by time division multiplexing and Pulse Width Modulation (PWM) techniques.” Pease at [0050]. Pease likewise claims “a power controller capable of producing at least one of time-division multiplexed power, pulse-width modulated power, alternating current power, or direct current phase alternating power,” Pease at claim 20, implemented by a controller 1000 that includes “logic (hardware or software) to control at least one power supply,” Pease at [0041]. It would have been obvious to control the heater power supply of the DiBattista-Herchen-1-Pease system via PWM signals, so that the selective heating of the wafer TI layer is based on those PWM signals - an application of Pease’s express PWM power control to DiBattista’s heater power supply that yields predictable results.

O. CLAIM 14

Herchen-1 discloses a multi-layer heater stack with insulating layers 301, 303, 305 isolating the conducting layers. Herchen-1 at [0051]-[0052]. Adding a grounded shield layer would have been obvious due to known need to shield electrical components from electrical radiation. EX1003, ¶71.

A POSITA would have been specifically motivated to combine Natsuhara with DiBattista and Herchen-1. Natsuhara discloses a wafer holder for wafer probing in which the resistance heat generator that heats the chuck top is covered by an insulating layer that is in turn covered by an electrically conductive layer, primarily

of iron or nickel, that blocks the electromagnetic waves which interfere with the low-current electrical measurements taken during probing. Natsuhara (EX1015) at Abstract, [0009], [0012], [0024]. The DiBattista-Herchen-1 system likewise applies power to resistive heater traces positioned directly beneath the wafer under test, generating electromagnetic radiation of the same kind in the same probing environment, and Herchen-1 already provides a multi-layer heater stack with insulating layers onto which such a conductive shield can be added. A POSITA concerned with the accuracy of the electrical measurements would therefore have been motivated to add Natsuhara's grounded, electrically conductive shield layer to the DiBattista-Herchen-1 wafer TI layer to protect the wafer from the EMI generated by the heater traces. Doing so amounts to no more than applying a known technique to a known device ready for improvement and combining prior-art elements according to known methods, to yield the predictable result of reduced electromagnetic interference and improved measurement accuracy during test. A POSITA would have had a reasonable expectation of success in doing so.

P. INDEPENDENT CLAIM 15

1. [15.pre]

As shown for limitation [1.pre], DiBattista discloses a system for temperature-controlled testing of IC devices at wafer level. DiBattista at 1:19-22, 12:26-31. To the extent the preamble is limiting, DiBattista in view of Herchen-1 discloses it.

2. [15.a]

As shown for limitation [1.a], DiBattista discloses a test head interface 130 coupled to an available test system such as the ITS 9000 IX, which generates input signals, processes output signals, and generates a test result verifying device performance. DiBattista at 7:50-58, 1:26-31.

3. [15.b]

As shown for limitation [1.b], DiBattista discloses a wafer prober 100 with a stage 110 and chuck 120 carrying the wafer, using needle contacts to probe the individual devices, coupled through the test head interface 130 to the test system. DiBattista at 7:37-44, 1:34-43, 7:50-58.

4. [15.c]

DiBattista discloses an array 129 of heating elements 149 contacting the wafer, each “controlled independently of the others,” providing a plurality of discretely controllable thermal zones each selectively heating a respective area of the wafer. DiBattista at 6:38-42, 5:54-61. Because each element has “a size and shape corresponding to that of the associated IC device” and “the pattern of heating elements 149 matches that of the devices on the wafer,” the positions and shapes of the zones are customized to the die layout. DiBattista at 6:21-37, 3:15-20. Herchen-1 confirms the discretely controllable zone construction, disclosing etched heater elements “arranged to form six independent heating zones with a separate

temperature sensor for each zone,” each individually controlled. Herchen-1 at [0051].

5. [15.d]

As shown for limitation [1.d], DiBattista discloses a fluid-cooled chuck 122 disposed under the heating-element array that “acts as a heat sink by absorbing heat energy from the heating element 149,” cooling the wafer. DiBattista at 6:21-37, 8:50-57. Herchen-1 likewise discloses top and bottom cooling plates 220, 230, the latter with fluid channels, positioned below the heater-bearing planar members. Herchen-1 at [0049]-[0050].

6. [15.e]

As shown for limitation [1.e], DiBattista discloses a temperature control system 140 that maintains each device at a set-point temperature by controlling both the liquid cooling and the heating of the individual elements, using a “feedback loop . . . to control the operation of the heating element while the liquid cooled heat exchanger is operated as a set point heat sink.” DiBattista at 7:59-8:2, 9:44-55, 12:20-25.

Q. CLAIM 16

DiBattista in view of Pease renders claim 16 obvious. Pease discloses sizing each planar heater zone to a group of dies. In Pease, each planar heater zone may be “not larger than four device dies . . . or not larger than two device dies . . . or not

larger than one device die . . . to correspond to the device dies on the substrate,” Pease at [0017], and is “of similar size to or smaller than a single device die or group of device dies on the substrate.” Pease at [0030]. It would have been obvious to size the discretely controllable zones of the DiBattista–Pease heater layer so that each zone corresponds to multiple dice, as a routine matching of zone granularity to the die layout that yields predictable temperature control of groups of dice.

R. CLAIM 17

As shown for claim 9, DiBattista discloses heating elements 149 and DUTs 182 “in a one-to-one correspondence,” so that each discretely controllable thermal zone corresponds to a single die. DiBattista at 5:54-61, 6:21-37.

S. CLAIM 18

DiBattista in view of Pease renders claim 18 obvious. For the reasons given for claim 11, Pease’s sub-die zones - each “of similar size to or smaller than a single device die,” Pease at [0030], and scalable to “up to 1000 heater zones,” Pease at [0049] - make it obvious to subdivide the DiBattista-Pease heating pattern so that each die of the die layout corresponds to multiple discretely controllable zones, achieving the predictable benefit of finer intra-die thermal control.

T. CLAIM 19

As shown for limitation [1.c], DiBattista discloses resistive heating elements each implemented with a “heater trace” that “provides the heat energy,” DiBattista

at 6:7-16, and Herchen-1 discloses heater elements “etched onto conducting layer 304” and arranged in a predetermined pattern forming individually controlled zones, Herchen-1 at [0051], [0054], FIG. 5. The combination therefore provides a plurality of resistive traces traversing the wafer TI layer that selectively heat and maintain the temperatures of the discretely controllable zones responsive to the thermal controller.

U. CLAIM 20

DiBattista discloses independent control of each heating element, DiBattista at 6:38-42, and testing “at high speed” with the temperature of each device “controlled independently of the other devices on the wafer during a test,” DiBattista at 12:26-31, executed by a system controller 160, DiBattista at 7:59-8:2. Staged preconditioning follows from DiBattista’s independent zone control and high-speed testing. EX1003, ¶72; EX1005, ¶¶147-48. Programming the controller to precondition a next zone during testing would have been obvious to ensure expediency of testing.

V. CLAIM 21

For the reasons given for claim 20, the recited preconditioning of a second set of zones while a first set’s die is tested would have been obvious to a POSITA and follows from DiBattista’s independent zone control and high-speed testing. DiBattista at 6:38-42, 12:26-31. EX1003, ¶73; EX1005, ¶149.

W. CLAIM 22

Herchen-1 discloses a TIM layer between the heater-bearing planar member and the cooling plate-thermal material 221 disposed on the upper surface of cooling plate 220 to aid heat removal. Herchen-1 at [0049]. *See* discussion in Claims 5 and 6 regarding obviousness of this element. *See also* Herchen-2 at [0042], [0044], [0052].

X. INDEPENDENT CLAIM 23

1. [23.pre]

DiBattista discloses “a method for testing IC devices at wafer level in which the temperature of each device on the wafer is controlled independently of the other devices on the wafer during a test.” DiBattista at 12:26-31; *see also* 4:6-15. To the extent the preamble is limiting, the DiBattista-Herchen-1 combination discloses it.

2. [23.a]

DiBattista tests the wafer’s circuits using a test system (e.g., the ITS 9000 IX) coupled through the test head interface 130. DiBattista at 7:50-58; *see also* 4:6-15 (testing the individual devices on the wafer).

3. [23.b]

DiBattista’s test head interface 130 provides electrical connections applied to the power and input/output pads of the devices, through which the test system generates and applies input signals. DiBattista at 7:50-58, 1:34-43.

4. [23.c]

The same test head interface 130 carries the input/output signals from the devices to the test system for processing. DiBattista at 7:50-58. Functional testing verifies performance of the devices, which entails processing the devices' output signals.

5. [23.d]

DiBattista's functional testing verifies device performance "so that any non-functioning devices can be removed from the process," which necessarily generates a test result for the circuits. DiBattista at 3:1-2.

6. [23.e]

DiBattista performs temperature control in conjunction with testing: its temperature control system 140 maintains each device at a set-point temperature during the test by controlling both the fluid-cooled chuck (cold plate) and the array 129 of independently controlled heating elements 149 (the thermal interposer layer with separately controllable zones). DiBattista at 6:38-42, 7:59-8:2, 8:12-57, 12:20-31. Herchen-1 confirms the separately controllable thermal zones, disclosing etched heater elements forming six independently controlled zones over a fluid-channel cooling plate. Herchen-1 at [0050]-[0051]. The combination thus selectively heats and maintains the temperatures of a plurality of separately controllable zones while testing.

Y. CLAIM 24

As shown for claim 2, DiBattista's heating elements have "a size and shape corresponding to that of the associated IC device," with the pattern matching the devices on the wafer, so the positions and shapes of the zones are customized to the die layout. DiBattista at 6:21-37, 3:15-20. Herchen-1's patterned, etched zones further confirm this construction. Herchen-1 at [0051].

Z. CLAIM 25

As with claim 20, this preconditioning sequence would have been obvious to a POSITA and follows from DiBattista's independent per-element control and high-speed testing. DiBattista at 6:38-42, 12:26-31. *See* discussion in Ground 1, claim 20 regarding obviousness of this claim. EX1003, ¶74; EX1005, ¶¶151.

AA. CLAIM 26

For the reasons given for claims 21 and 25, the set-wise preconditioning sequence would have been obvious to a POSITA and follows from DiBattista's independent zone control and high-speed testing. DiBattista at 6:38-42, 12:26-31. *See* discussion in Ground 1, claims 21 and 25 regarding obviousness of this claim. EX1003, ¶75; EX1005, ¶152.

BB. CLAIM 27

As shown for limitations [1.c] and [1.e], DiBattista's zones comprise resistive heater traces (each element implemented with a "heater trace" that "provides the heat

energy”), and the temperature control system selectively energizes those elements during testing by supplying heater power under feedback control. DiBattista at 6:7-16, 9:16-22, 12:20-25. Herchen-1 confirms the resistive-trace construction with its etched heater elements arranged in individually controlled zones. Herchen-1 at [0051]. The combination therefore energizes a plurality of resistive traces to selectively heat the separately controllable zones during testing. EX1003, ¶76; EX1005, ¶¶153-55.

IX. GROUND 2: Claims 1-27 are Rendered Obvious Over DiBattista in View of Costello, Herchen-1, and Criminale

A. OVERVIEW OF GROUND 2

See description of DiBattista contained in Ground 1.

A person of ordinary skill would have been motivated to combine DiBattista’s per-device, feedback-controlled thermal regulation at wafer level with Costello’s mechanically rigid, dual-sided thermally managed chuck architecture and noise/leakage mitigation to achieve improved probe-test performance, with a reasonable expectation of success. EX1003, ¶¶79-83; EX1005, ¶¶158-61. DiBattista teaches an apparatus with a heat exchanger/chuck having a surface divided into regions corresponding to IC devices, where each device’s temperature is individually controlled during testing. It further teaches embodiments with multiple heating elements on a fluid-cooled chuck acting as a heat sink, and alternative

separate heat exchanger bodies, enabling rapid compensation for device self-heating and per-DUT control. *Id.*

A POSITA would have been motivated to combine DiBattista and Costello as DiBattista targets per-DUT temperature accuracy and Costello provides arrays of sensors and controller algorithms to detect and address localized non-uniformities and hotspots. EX1003, ¶80. DiBattista provides per-device temperature control during test and Costello teaches multiple sensors and algorithms (e.g., averaging, hotspot-focused control) to handle local non-uniformities.

A person of ordinary skill would view Costello's sensor arrays and control strategies as directly complementary to DiBattista's per-DUT loops, improving spatial resolution and dynamic response to device self-heating and local hotspots that DiBattista seeks to counteract. EX1003, ¶80. DiBattista's multiple heaters with a fluid-cooled heat sink enable rapid compensation for device self-heating. Deploying Costello's multi-sensor feedback with DiBattista's power-following control would increase robustness against local thermal anomalies, yielding tighter per-DUT temperature regulation during probing. *Id.*

B. INDEPENDENT CLAIM 1

DiBattista in view of Costello discloses or renders obvious every limitation of claim 1, as set forth element-by-element below.

1. [1.pre]

See discussion of DiBattista for this element in Ground 1.

Costello also discloses this element. Costello at Abstract, [0012], [0049-50], claim 30. For example, Costello discloses a system integrated into an automatic wafer probe test station, with the chuck on a prober stage, vacuum grooves on the top surface, a controller and heater power source, a chiller circulating coolant via an umbilical, and a touch-screen user interface. Costello at [0049]-[0050]. Probe pins on a probe card connect to an electrical test system, and dies are tested sequentially by aligning the wafer with the pins while the thermal chuck system cooperates with the prober and test system. *Id.*

2. [1.a]

See discussion of DiBattista for this element in Ground 1.

Costello discloses this element. Costello at [0050]. For example, Costello discloses that each die is electrically tested by connecting it to test equipment, with probe pins mounted on a probe card and connected to an electrical test system that tests the individual dies in cooperation with the temperature-controlled chuck.

3. [1.b]

See discussion of DiBattista for this element in Ground 1.

Costello discloses this element. Costello at [0049-50]. For example, Costello discloses probe pins mounted on a probe card that are aligned with and brought into contact with the wafer to connect and test the individual dies.

4. [1.c]

See discussion of DiBattista for this element in Ground 1.

In the DiBattista-Costello combination, DiBattista supplies the plurality of resistive-trace heating elements arranged in one-to-one correspondence with the devices on the wafer, selectively heating a plurality of zones corresponding to areas of the wafer, as set forth for this element in Ground 1. Costello supplies the mechanically rigid, dual-sided temperature-controlled chuck and the array of temperature sensors that localize control of hot spots at each device under test. Costello at [0054-56], [0016], [0079], [0066]. Costello discloses a chuck top plate carrying a primary resistance-coil heater directly beneath the wafer, together with an array of temperature sensors enabling localized temperature control at the device under test. A POSITA would have implemented DiBattista's per-device resistive-trace zones on Costello's rigid, sensor-instrumented chuck, yielding a wafer TI layer whose resistive traces selectively heat a plurality of zones corresponding to areas of the wafer under closed-loop, localized control. EX1003, ¶85.

5. [1.d]

See discussion of DiBattista for this element in Ground 1.

Costello discloses this element. Costello at [0012-14], [0051], [0055-056], [0060-62]. For example, Costello discloses a heat sink with internal cooling channels

through which a chilled coolant fluid is recirculated to remove heat, positioned beneath the heater to cool the wafer.

6. [1.e]

See discussion of DiBattista for this element in Ground 1.

Costello discloses this element. Costello at [0012-13], [0017], [0049-52], [0064-66], [0079]. For example, Costello discloses a system controller that maintains target temperatures by varying the current supplied to the resistance heaters and adjusting the recirculated coolant based on feedback from the temperature sensors, including localized control of individual regions using an array of sensors.

C. CLAIM 2

See discussion of DiBattista for this claim in Ground 1.

D. CLAIM 3

See discussion of DiBattista for this claim in Ground 1.

Costello discloses this claim. Costello at [0049], [0049-54], [0064-65]. For example, Costello discloses a chiller that cools and recirculates the coolant fluid under control of the system controller, together with controller-actuated valve apparatus that regulates the coolant flow through the chuck.

E. CLAIM 4

See discussion of DiBattista and Herchen-1 for this claim in Ground 1.

Costello discloses or renders obvious this claim in light of Herchen-1. Costello at [0072], [0075-76], claims 13 and 29. A POSITA working from Costello would have been motivated to add TIM layers at the two relevant mechanical/thermal junctions - (i) between the cold plate (*i.e.*, Costello's cooled heat sink/thermal base) and an intermediate wafer thermal-interface ("wafer TI") layer, and (ii) between that wafer TI layer and the wafer - because Costello not only discloses adding an electrically conductive layer, but is expressly concerned with achieving uniform temperature control at the wafer during probing and maintaining planarity/flatness and minimizing distortion under substantial probe-pin loading, while still enabling heating/cooling transitions. A thermally conductive layer accomplishes these goals more effectively. EX1005, ¶163; *see generally* Cola (EX1016) at [0019], [0086].

F. CLAIM 5

See discussion of DiBattista for this claim in Ground 1.

Indium foil is a well-known compliant thermal-interface material, as confirmed by expert testimony and by the prior art disclosing compliant thermal-interface materials used to improve heat transfer across stacked wafer-test interfaces. *See* Cola (EX1016) at [0019], [0086]. Indium would have been an obvious choice among a limited, well-characterized set of known thermal-interface materials. EX1005, ¶165.

G. CLAIM 6

See discussion of DiBattista for this claim in Ground 1.

Graphite is a well-known compliant thermal-interface material, as confirmed by expert testimony and by the prior art disclosing compliant, carbon-based thermal-interface materials. *See* Cola (EX1016). Graphite would have been an obvious choice among a limited, well-characterized set of known thermal-interface materials. EX1005, ¶167.

H. CLAIM 7

See discussion of DiBattista for this claim in Ground 1.

Costello discloses this claim. Costello at [0022], [0049], [0052-54], [0074], [0083-87]. For example, Costello discloses securing the wafer by applied vacuum through vacuum grooves and conduits in the chuck top, with controller-actuated valving governing the vacuum and coolant connections.

I. CLAIM 8

See discussion of DiBattista and Herchen-1 for this claim in Ground 1.

Costello discloses or renders obvious this claim in light of Herchen-1. Costello at [0052-53]. It would have been obvious to a POSITA to use a positive-pressure blow-off valves or an air source for releasing the wafer. Releasing a vacuum-secured substrate with a positive air pulse is a conventional complement to vacuuming. EX1003, ¶87.

J. CLAIM 9

See discussion of DiBattista for this claim in Ground 1.

K. CLAIM 10

See discussion of claim 9, directly above.

L. CLAIM 11

Costello and DiBattista render this claim obvious. DiBattista targets per-die thermal control by matching an independently controlled heater array to the wafer die layout, expressly to overcome whole-wafer chuck limitations and to handle localized power dissipation during wafer probing (e.g., Figs. 8A, 10A-10B; discussion of individualized control).

A POSITA seeking improved temperature uniformity and faster, localized response for high-power or non-uniform dies would have been motivated to marry DiBattista's per-die, independently controlled heater array with Costello's layered, independently controlled thermal paths and localized sensing/control. Doing so predictably yields finer-granularity thermal management at the wafer-contact interface and layered control authority over each die location. EX1005, ¶168-72.

Both references operate in wafer probing contexts and integration is routine engineering: define multiple independently controllable thermal "zones" that influence each die area, leveraging known controls and sensor feedback to meet

uniformity targets. Nothing in either reference suggests incompatibility. EX1005, ¶168-72.

M. CLAIM 12

See discussion of DiBattista for this claim in Ground 1.

Costello discloses this claim. Costello at [0080]. It would have been obvious to a POSITA to use loading pins, as such were known and common method to load and unload wafers being tested. EX1003, ¶93.

N. CLAIM 13

Costello, DiBattista, and Criminale render this claim obvious. Taken together, the references teach both elements the claim targets: (i) a power supply path that provides power to wafer-contact heating elements/thermal layer, and (ii) a controller that modulates heater power responsive to thermal feedback to achieve selective heating across independently controlled regions. Costello identifies DC resistance heaters on the chuck, a system controller and heater power source that vary heater power to achieve setpoints, and sensor feedback via RTDs at the top and bottom surfaces; it also presents sensor arrays for localized temperature management and algorithms for selecting or averaging sensors. *See, e.g.*, Costello at [0079]. DiBattista details a control chain in which a thermal control circuit computes a control signal from setpoint, sensed forcing temperature, and device power, and then drives a power amplifier stage that delivers heater current to each heating element, with

multiple boards enabling independent per-heater control for spatial selectivity. *See, e.g.,* DiBattista at 9:18-24; EX1003, ¶¶ 95, 97.

A POSITA would have been specifically motivated to combine Criminale with DiBattista and Costello. Criminale discloses a PWM heater controller connected to a plurality of independently and spatially tunable heaters embedded in a semiconductor chuck, which are individually controlled to adjust localized power and thereby tune the temperature profile across the substrate. Criminale (EX1017) at Abstract, [0007]. DiBattista and Costello each teach multi-zone resistive heating of a wafer-scale substrate under closed-loop, sensor-based control, which necessarily requires adjustable per-zone heater power to hold each zone's setpoint. A POSITA seeking to regulate the average power delivered to each such zone would have looked to Criminale's PWM heater controller as a known and proven implementation of exactly that function in the same wafer-chuck thermal environment, and would have recognized that Criminale's spatially tunable, individually controlled heater zones map directly onto DiBattista's per-die heater array and Costello's independently controlled, sensor-instrumented thermal paths. Applying Criminale's PWM heater control to the DiBattista-Costello heater array amounts to no more than combining prior-art elements according to known methods, and applying a known technique to a known device ready for improvement, to yield the predictable result of precise, decoupled per-zone average-power control using

the already-disclosed temperature-feedback paths. A POSITA would have had a reasonable expectation of success in doing so. EX1003, ¶¶95-97.

O. CLAIM 14

See discussion of DiBattista for this claim in Ground 1.

Costello discloses or renders obvious this claim. Costello at [0019-21], [0070-76], [0083]. For example, Costello discloses an electrically conductive guard layer that, together with the heat sink connected as a shield, shields the wafer and chuck top from electrical noise coupled from the heaters and prober, addressing the electromagnetic fluctuations produced by changes in heater current. EX1003, ¶99.

P. INDEPENDENT CLAIM 15

1. [15.pre]

As shown for limitation [1.pre], DiBattista and Costello disclose or render obvious this element.

2. [15.a]

As shown for limitation [1.a], DiBattista and Costello disclose or render obvious this element.

3. [15.b]

As shown for limitation [1.b], DiBattista and Costello disclose or render obvious this element.

4. [15.c]

As shown for limitation [1.c], DiBattista and Costello disclose or render obvious this element.

5. [15.d]

As shown for limitation [1.d], DiBattista and Costello disclose or render obvious this element.

6. [15.e]

As shown for limitation [1.e], DiBattista and Costello disclose or render obvious this element.

Q. CLAIM 16

See discussion of claim 10, above.

R. CLAIM 17

See discussion of claim 9, above.

S. CLAIM 18

See discussion of claim 11, above.

T. CLAIM 19

As shown for limitation [1.c], DiBattista and Costello disclose or render obvious this claim.

U. CLAIM 20

DiBattista discloses independent control of each heating element, DiBattista at 6:38-42, and testing “at high speed” with the temperature of each device “controlled independently of the other devices on the wafer during a test,” DiBattista

at 12:26-31, executed by a system controller 160, DiBattista at 7:59-8:2. Staged preconditioning follows from DiBattista's independent zone control and high-speed testing. EX1003, ¶100, EX1005, ¶¶174-75. Programming the controller to precondition a next zone during testing would have been obvious to ensure expediency of testing.

V. CLAIM 21

For the reasons given for claim 20, the recited preconditioning of a second set of zones while a first set's die is tested would have been obvious to a POSITA and follows from DiBattista's independent zone control and high-speed testing. DiBattista at 6:38-42, 12:26-31. EX1003, ¶101, EX1005, ¶¶176-79.

W. CLAIM 22

See discussion of claims 5 and 6, above.

X. INDEPENDENT CLAIM 23

1. [23.pre]

See discussion of DiBattista for this element in Ground 1.

Costello discloses this element. Costello at [0050], [0073-76]. For example, Costello discloses a method of testing the wafer's dies in which each die is sequentially connected to the electrical test system while the temperature-controlled chuck holds it at the desired test temperature.

2. [23.a]

See discussion of DiBattista for this element in Ground 1.

Costello discloses this element. Costello at [0050]. For example, Costello discloses testing the wafer's dies through the cooperative action of the electrical test system and the temperature-controlled chuck.

3. [23.b]

See discussion of DiBattista for this element in Ground 1.

Costello discloses this element. Costello at [0050]. For example, Costello discloses using the electrical test system, connected to the probe pins, to test the individual dies.

4. [23.c]

See discussion of DiBattista for this element in Ground 1.

Costello discloses this element. Costello at [0050], [0051]. For example, Costello discloses that the electrical test system connected to the probe pins tests the individual dies and receives their output during testing.

5. [23.d]

See discussion of DiBattista for this element in Ground 1.

Costello discloses this element. Costello at [0050], [0075-76]. For example, Costello discloses that testing each die through the cooperative action of the electrical test system and the chuck produces a test result for the die.

6. [23.e]

See discussion of claim 1, above.

Y. CLAIM 24

See discussion of claim 2, above.

Z. CLAIM 25

See discussion of claim 20, above. EX1003, ¶102, EX1005, ¶181.

AA. CLAIM 26

See discussion of claim 21, above. EX1003, ¶103, EX1005, ¶182.

BB. CLAIM 27

See discussion of claim elements [1.c] and [1.e], above.

X. GROUND 3: Claims 1-27 are Rendered Obvious Over Sugiyama in View of Parkhe, Natsuhara, Criminale, and knowledge of a POSITA

A. OVERVIEW OF GROUND 3

Sugiyama discloses probers and probe testing methods enabling accurate, efficient temperature control of wafer-level test sites, Sugiyama at [0015], [0016], while preventing chuck tilt under probe load. Sugiyama at [0017]. A first aspect provides a prober with a main chuck on a Z stage, X-Y positioning, a probe card above, and multiple heaters sized to individual devices or device groups, each with temperature sensors and a heat exchanger controlled by a temperature controller. Sugiyama at [0019], [0020], [0067], [0068], [0069]. These heaters can be organized as cell structures aligned to die locations or die groups, each cell optionally including

its own heater, sensor, and heat exchanger (Sugiyama at [0022], [0070]), with heat insulators between cells to reduce thermal cross-talk. Sugiyama at [0023], [0071].

Operation includes placing and fixing a wafer, aligning in X, Y, and theta (Sugiyama at [0072]), contacting probes by raising the Z stage, overdriving, and testing after bringing the selected site to a set temperature. Sugiyama at [0073].

This structure prevents main chuck tilt from probe needle pressure, particularly at wafer peripheries, improving stable contact. Sugiyama at [0084], [0094]. The probing stage can incorporate a heater, temperature sensor, and heat exchanger sized to the single site or multi-site region contacted by the probes (Sugiyama at [0030], [0031], [0085]), allowing rapid, low-energy thermal control of only the tested region. Sugiyama at [0086]. The probing stage is preferably aluminum, detachably mounted for exchange to match site size (Sugiyama at [0087]), and its compact mass reduces thermal inertia for faster heating and cooling. Sugiyama at [0089]. Wafer fixing options include vacuum grooves or ports (Sugiyama at [0066], [0077]), hinged retainers (Sugiyama at [0077]), and a vertically actuated ring with support columns (Sugiyama at [0078]), and the chuck plate can be detachable. Sugiyama at [0079]. A method is claimed that sequences placement, X-Y-theta alignment, raising the probing stage to support the wafer, bringing probes into contact, overdriving, temperature conditioning to a target, electrical testing, and separation, repeated across sites. Sugiyama at [0039], [0088].

Parkhe is directed to electrostatic chuck (ESC) assemblies usable for high-temperature semiconductor processing (Parkhe at [0002]), addressing failures above about 120°C (Parkhe at [0005]) by providing a puck with an electrically insulative upper plate (with heating elements and electrodes) metal-bonded to a lower plate, fastener-coupled to a cooling plate with controlled force distribution (Parkhe at [0006], [0017]) and optional thermal choke features (Parkhe at [0052]) to achieve uniform heat transfer and high-temperature operation. Parkhe at [0016], [0053].

It would have been obvious to integrate Sugiyama's localized, cell based temperature control paradigm (Sugiyama at [0070], [0071]) into Parkhe's high temperature ESC architecture by implementing multiple, spatially distributed heating/cooling control zones within or functionally coupled to the Parkhe puck/cooling plate interface, each zone sized and positioned to correspond to regions of the substrate requiring differential thermal management (e.g., die clusters or annular/radial segments), and governed by a controller using temperature sensor feedback. Parkhe at [0029]. EX1003, ¶109.

Further, Sugiyama teaches that heating/cooling large chuck areas is inefficient and slow (Sugiyama at [0009]), and advocates localized, cell matched heaters/heat exchangers with sensors to reduce energy use and time to temperature. Sugiyama at [0070], [0086]. Parkhe seeks high temperature ESC operation with uniform heat transfer and controlled thermal choke between puck and cooling plate. Parkhe at

[0016], [0052], [0053]. Combining Sugiyama's localized control with Parkhe's robust high temperature ESC predictably improves spatial uniformity, transient response, and energy efficiency - recognized goals in wafer processing and testing. EX1003, ¶110.

It would have been obvious to substitute one known element for another. Sugiyama explicitly discloses temperature control elements comprising heaters with associated heat exchangers and sensors arranged as cells and controlled by a temperature controller. Sugiyama at [0022], [0070], claim 4. Parkhe's ESC already integrates heaters, sensors, and cooling channels/conduits (Parkhe at [0028], [0029]) and even references multiple heating zones and thermal isolators to shape lateral profiles. Parkhe at [0028], [0029]. EX1005, ¶191. Replacing or augmenting Parkhe's broader zones with Sugiyama's finer cell architecture is a straightforward substitution of known temperature control topologies, expected to yield predictable improvements. EX1005, ¶¶184-91.

B. INDEPENDENT CLAIM 1

Sugiyama in view of Parkhe discloses or renders obvious every limitation of claim 1, as set forth element-by-element below.

1. [1.pre]

Sugiyama discloses this element. Sugiyama at claim 1, [0015], [0025-26]. Sugiyama discloses a prober with a chamber, a stage base, an X-Y stage with a

driving mechanism, a Z stage with an elevating mechanism, a main chuck with rotational drive, multiple heaters, a heat exchanger, and a temperature controller, and a probe card with multiple probes. *Id.* The heaters are sized to heat individual objects or groups of objects and include temperature sensors, while the heat exchanger cools heated objects, and the temperature controller regulates at least the heaters or heat exchanger based on sensor feedback. *Id.*

2. [1.a]

Sugiyama discloses this element. Sugiyama at [0039], [0061], [0073-74], [0082-83], Fig. 1. For example, Sugiyama discloses a tester, coupled through a test head and probe card, that tests the electrical characteristics of the objects on the wafer.

3. [1.b]

Sugiyama discloses this element. Sugiyama at [0030], [0039], [0061], [0067], [0079], [0085-86], [0096], Fig. 1. For example, Sugiyama discloses a probe card carrying a plurality of probes that are brought into contact with the wafer to probe and test the electrical characteristics of the individual objects.

4. [1.c]

Sugiyama discloses this element. Sugiyama at [0067], [0070], [0071], [0092], claims 1-3. For example, Sugiyama discloses a main chuck carrying a plurality of heaters, each sized to and positioned in correspondence with an individual object or

group of objects and each having its own temperature sensor, organized as thermally isolated cell structures whose temperatures are separately controlled to selectively heat areas of the wafer.

To the extent Sugiyama does not disclose this element, Parkhe does, and it would have been obvious to supplement Sugiyama's disclosure with Parkhe for the reasons stated above. Parkhe at [0029-30], [0046], [0048], [0049], claim 1, claim 9, Fig. 1.

5. [1.d]

Sugiyama discloses this element. Sugiyama at [0068-69], [0070-72], [0085-86], Abstract. Portion 20a of FIG. 2 acts as a cold plate as it is a plate-like structure forming a complete layer underneath the heating elements 18 of the main chuck 6.

To the extent Sugiyama does not disclose this element, Parkhe does, and it would have been obvious to supplement Sugiyama's disclosure with Parkhe for the reasons stated above. Parkhe at [0023], [0067-68], [0051], Fig. 6, Fig. 1.

6. [1.e]

Sugiyama discloses this element. Sugiyama at Abstract, [0020-23], [0068-69], [0085]. For example, Sugiyama discloses a temperature controller connected to the heaters, temperature sensors, and heat exchanger that maintains each object at its target temperature by controlling both the selective heating of the heaters and the cooling provided by the fluid-cooled heat exchanger based on sensor feedback.

To the extent Sugiyama does not disclose this element, Parkhe does, and it would have been obvious to supplement Sugiyama's disclosure with Parkhe for the reasons stated above. Parkhe at Fig. 1, [0029].

C. CLAIM 2

Sugiyama discloses this claim. Sugiyama at [0022-23], [0067-69], [0072-73], [0092]. For example, Sugiyama discloses that the heaters and cell structures are arranged to correspond in position to the objects on the wafer, matching the zones to the die layout.

To the extent Sugiyama does not disclose this claim, Parkhe does, and it would have been obvious to supplement Sugiyama's disclosure with Parkhe for the reasons stated above. Parkhe at [0029].

D. CLAIM 3

Sugiyama discloses this claim. Sugiyama at [0068-70]. For example, Sugiyama discloses a heat exchanger having a fluid supply/drain channel and a fluid supply unit that circulates a cooling fluid to cool the objects, regulated by the temperature controller.

To the extent Sugiyama does not disclose this claim, Parkhe does, and it would have been obvious to supplement Sugiyama's disclosure with Parkhe for the reasons stated above. Parkhe at [0029], [0051], [0065-66].

A controller-actuated valve regulating coolant flow to the cold plate would have been obvious to a POSITA implementing Sugiyama's per-cell temperature control. Per-cell heat exchangers under per-cell temperature control mean the controller must differentially regulate cooling among cells. Differential regulation of a circulating coolant, at the granularity of each cell's exchanger, necessarily occurs by controlling coolant flow or capacity to each cell. In a fluid circuit, that modulation is performed by flow-control elements - i.e., valves - actuated under the controller's commands to increase/decrease coolant flow to a given cell to meet its setpoint. EX1005, ¶¶192-95; *see* Lutz, claims 12, 14, and 16.

E. CLAIM 4

This claim would have been obvious in light of Sugiyama and Parkhe. *See* Parkhe at [0055-56], [0071]. A POSITA working from Sugiyama would have been motivated to add TIM layers at the two relevant mechanical/thermal junctions - (i) between a cold plate and an intermediate wafer thermal-interface ("wafer TI") layer, and (ii) between that wafer TI layer and the wafer - because Sugiyama is concerned with achieving temperature control at the wafer during probing, while still enabling heating/cooling transitions. A thermally conductive layer accomplishes these goals more effectively. EX1005, ¶¶196-97; Cola at [0019].

F. CLAIM 5

Indium foil is a well-known compliant thermal-interface material, as confirmed by expert testimony and by the prior art disclosing compliant thermal-interface materials used to improve heat transfer across stacked wafer-test interfaces. *See* Cola (EX1016) at [0019], [0086]; EX1005, ¶198. Indium would have been an obvious choice among a limited, well-characterized set of known thermal-interface materials, obvious for the reasons set forth in claim 4, above.

G. CLAIM 6

Parkhe discloses a grafoil layer disposed between the puck 166 and the cooling plate. Parkhe at [0055-56], [0071]. Graphite is a well-known compliant thermal-interface material, as confirmed by expert testimony and by the prior art disclosing compliant, carbon-based thermal-interface materials. EX1005, ¶199.

H. CLAIM 7

Sugiyama discloses this claim. Sugiyama at Figs. 3, 10, 12, [0066], [0077-78]. For example, Sugiyama discloses fixing the wafer by vacuum suction through grooves and suction/exhaust ports evacuated by a vacuum pump, so that controlling the applied vacuum secures and releases the wafer.

I. CLAIM 8

This claim is rendered obvious given Sugiyama's disclosure of a vacuum. *See* Sugiyama at Figs. 3, 10, 12, [0066], [0077]. It would have been obvious to a POSITA to release the vacuum-secured wafer and TI layer using a positive-pressure blow-off

valve and air source. Releasing a vacuum-secured substrate with a positive air pulse is a conventional complement to vacuum securing and applying that known technique to Sugiyama's vacuum-secured chuck yields the predictable result of controlled wafer release. EX1003, ¶114.

J. CLAIM 9

Sugiyama discloses or renders obvious this element. Sugiyama at [0022-23], [0067-68], [0071-72], [0080], [0091-92], claims 2-3. For example, Sugiyama discloses heaters and cell structures each sized to and coinciding with a single object to be tested, so that each zone corresponds to a respective single die.

Sugiyama teaches partitioning temperature-control functionality on the chuck into multiple independently controllable "cells" or zones whose sizes are selected to match either a single object-under-test (i.e., a single die on the wafer) or a small group of such objects, and to control each such cell based on local sensing. Sugiyama at [0067-68]. Because Sugiyama discloses (i) heaters sized to one object or a group, (ii) per-cell temperature sensors and heat exchange, (iii) heat-insulating partitions between cells, and (iv) the benefits of minimizing heated area to reduce thermal lag/energy while improving accuracy, a POSITA would be motivated to select the finest practical granularity - one die per zone - when die-level electrical probing is performed, thereby making each zone correspond to a respective single die layout position. EX1003, ¶¶115-16. Since electrical probe testing is conducted at the die

(object) level with a defined probe footprint, and Sugiyama provides cells/heaters “corresponding to” individual objects and sized to that region, a POSITA would configure each zone to the die footprint so that each probed die is temperature-controlled independently during its testing. EX1003, ¶¶115-16.

K. CLAIM 10

Sugiyama discloses or renders obvious this claim. Sugiyama at [0022-23], [0067], [0071], [0080], [0091-92], claims 2-3. *See* discussion in claim 9, above. Further, it would be obvious to try, based on the desire to increase testing throughput, to adjust the heating zones to cover a plurality of dice. EX1003, ¶117.

L. CLAIM 11

Sugiyama in light of knowledge of a POSITA discloses or renders obvious this claim. Sugiyama at [0022-23], [0069], [0067-71], [0080], [0091-92], claims 2-3. *See* discussion in claim 9, above. Further, it would be obvious to try, based on the desire for more granular testing ability, to adjust the heating zones such that multiple zones covered a single die. EX1003, ¶118.

M. CLAIM 12

It would have been obvious to supplement Sugiyama’s disclosure with Parkhe for the reasons stated above. Parkhe at [0033]. It would further have been obvious to a POSITA to use loading pins, as such were known and common method to load and unload wafers being tested. EX1003, ¶119.

N. CLAIM 13

This claim is obvious. *See* Sugiyama at [0066-70], [0085], [0090]. Both Sugiyama and Parkhe require independently maintaining distinct temperatures per zone using a controller that responds to multiple temperature sensors, which calls for per-zone modulation of heater power. EX1003, ¶120.

A POSITA would have been specifically motivated to combine Criminale with Sugiyama and Parkhe. Criminale discloses a PWM heater controller connected to a plurality of independently and spatially tunable heaters embedded in a semiconductor chuck, which are individually controlled to adjust localized power and thereby tune the temperature profile across the substrate. Criminale (EX1017) at Abstract, [0007]. Sugiyama teaches cell-structured, independently controlled heaters sized to individual dies or die groups, each with its own sensor, and Parkhe teaches an electrostatic chuck with embedded heating elements and multiple heating zones under controller-based, sensor-driven regulation; both therefore require adjustable per-zone heater power to maintain distinct zone setpoints. A POSITA seeking to regulate the average power delivered to each such zone would have looked to Criminale's PWM heater controller as a known and proven implementation of exactly that function in the same wafer-chuck thermal environment, and would have recognized that Criminale's spatially tunable, individually controlled heater zones map directly onto Sugiyama's per-cell heater

array and Parkhe's multi-zone ESC architecture. Applying Criminale's PWM heater control to the Sugiyama-Parkhe system amounts to no more than combining prior-art elements according to known methods and applying a known technique to a known device ready for improvement, to yield the predictable result of precise, decoupled per-zone average-power control using the already-disclosed temperature-feedback paths. A POSITA would have had a reasonable expectation of success in doing so. EX1003, ¶120.

O. CLAIM 14

Sugiyama in light of Natsuhara renders this claim obvious. Adding a grounded shield layer would have been obvious due to known need to shield electrical components from electrical radiation. EX1003, ¶121.

A POSITA would have been specifically motivated to combine Natsuhara with Sugiyama. Natsuhara discloses a wafer holder for wafer probing in which the resistance heat generator that heats the chuck top is covered by an insulating layer that is in turn covered by an electrically conductive layer, primarily of iron or nickel, that blocks the electromagnetic waves which interfere with the low-current electrical measurements taken during probing. Natsuhara (EX1015) at Abstract, [0009], [0012], [0024]. Sugiyama likewise energizes resistive heaters positioned at the wafer under test and performs sensitive electrical probe testing of the devices in the same environment, so the heater-generated electromagnetic radiation would interfere with

those measurements in the same way. A POSITA concerned with the accuracy of the electrical measurements would therefore have been motivated to add Natsuhara's grounded, electrically conductive shield layer over the heater of Sugiyama's chuck to protect the wafer from that EMI. Doing so amounts to no more than applying a known technique to a known device ready for improvement and combining prior-art elements according to known methods, to yield the predictable result of reduced electromagnetic interference and improved measurement accuracy during test. A POSITA would have had a reasonable expectation of success in doing so.

P. INDEPENDENT CLAIM 15

1. [15.pre]

As shown for limitation [1.pre], Sugiyama discloses or renders obvious this element.

2. [15.a]

As shown for limitation [1.a], Sugiyama discloses or renders obvious this element.

3. [15.b]

As shown for limitation [1.b], Sugiyama discloses or renders obvious this element.

4. [15.c]

As shown for limitation [1.c], Sugiyama and Parkhe disclose or render obvious this element.

5. [15.d]

As shown for limitation [1.d], Sugiyama and Parkhe disclose or render obvious this element.

6. [15.e]

As shown for limitation [1.e], Sugiyama and Parkhe disclose or render obvious this element.

Q. CLAIM 16

See discussion of claim 10, above.

R. CLAIM 17

See discussion of claim 9, above.

S. CLAIM 18

See discussion of claim 11, above.

T. CLAIM 19

As shown for limitation [1.c], Sugiyama and Parkhe disclose or render obvious this claim.

U. CLAIM 20

Sugiyama discloses independent control of each heating element, Sugiyama at [0020-22]. For example, Sugiyama discloses independent control of each heater

and cell and a temperature controller that brings the objects to a predetermined temperature in advance of testing.

As noted above, Sugiyama discloses a controller for controlling independent heating elements. Staged preconditioning follows from Sugiyama's independent zone control and wafer testing system based on knowledge of a POSITA. Sugiyama at [0062-67]; EX1003, ¶125. Programming the controller to precondition a next zone during testing would have been obvious to ensure expediency of testing. EX1005, ¶¶200-01.

V. CLAIM 21

For the reasons given for claim 20, the recited preconditioning of a second set of zones while a first set's die is tested would have been obvious to a POSITA and follows from Sugiyama's independent zone control and wafer testing system. EX1003, ¶126; EX1005, ¶202.

W. CLAIM 22

See discussion of claims 5 and 6, above.

X. INDEPENDENT CLAIM 23

1. [23.pre]

Sugiyama discloses this element. Sugiyama at [0039-40], [0060], Fig. 1. For example, Sugiyama discloses a method of testing the objects on a wafer in a prober,

including placing and aligning the wafer, bringing the probes into contact, overdriving, and testing the electrical characteristics under temperature control.

2. [23.a]

Sugiyama discloses this element. Sugiyama at [0061], [0073], Fig. 1. For example, Sugiyama discloses testing the wafer's circuits with a tester that measures the electrical characteristics of each object through the probes once the object reaches its test temperature.

3. [23.b]

Sugiyama discloses this element. Sugiyama at [0039], [0061], [0073-74], [0082-83], Fig. 1. For example, Sugiyama discloses that the tester applies electrical signals to the objects through the probes during testing of their electrical characteristics.

4. [23.c]

Sugiyama discloses this element. Sugiyama at [0039], [0061], [0073-74], [0082-83], Fig. 1. For example, Sugiyama discloses that the tester measures and processes the resulting output from the objects through the probes.

5. [23.d]

Sugiyama discloses this element. Sugiyama at [0039], [0061], [0073-74], [0082-83], Fig. 1. For example, Sugiyama discloses that the tester generates a test result reflecting the measured electrical characteristics of the objects.

6. [23.e]

See discussion of claim 1, above.

Y. CLAIM 24

See discussion of claim 2, above.

Z. CLAIM 25

See discussion of claim 20, above. EX1003, ¶127; EX1005, ¶204.

AA. CLAIM 26

See discussion of claim 21, above. EX1003, ¶128; EX1005, ¶205.

BB. CLAIM 27

See discussion of claim elements [1.c] and [1.e], above.

XI. GROUNDS FOR STANDING

Petitioner certifies the '841 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of any '841 Patent claim.

XII. MANDATORY NOTICES

Real Party-in-Interest (37 C.F.R. § 42.8(b)(1)): The real parties-in-interest are:

1. AEM HOLDINGS LTD.;
2. AEM SINGAPORE PTE. LTD.;
3. AEM AMERICAS, INC.;
4. DB Design Group, Inc.;
5. Afore Oy;

6. Iris Solution Pte. Ltd.;
7. Mu-Test SAS;
8. AEM TesTech (Shanghai) Co., Ltd.; and
9. AEM International (Korea) Ltd.

Related Matters (37 C.F.R. § 42.8(b)(2)): Advantest Test Solutions, Inc. has sued AEM Holdings Ltd., AEM Singapore Pte. Ltd., and AEM Americas, Inc. in the district court for the Southern District of California (Case No.: 3:25-cv-02604-JES-BJW) asserting Pat. Nos. 11,674,999 and 12,320,841. The case was filed October 1, 2025.

Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3)):

Lead Counsel

Timothy J. Maier (Reg. No. 51,986)
tjm@maierandmaier.com

MAIER & MAIER PLLC
345 South Patrick Street
Alexandria, VA 22314
(703) 740-8322 (phone)
(703) 991-7071 (fax)

Backup Counsel

Siddhesh V. Pandit (Reg. No. 58,572)
svp@maierandmaier.com
Michael R. Casey (Reg. No. 40,294)
mrc@maierandmaier.com

MAIER & MAIER PLLC
345 South Patrick Street
Alexandria, VA 22314
(703) 740-8322 (phone)
(703) 991-7071 (fax)

Thomas J. Gohn (Reg. No. 72,122)
tjg@maierandmaier.com

MAIER & MAIER PLLC
8750 N. Central Expressway
Suite 1850
Dallas, Texas 75231
(703) 740-8322 (phone)
(703) 991-7071 (fax)

Service Information (37 C.F.R. § 42.8(b)(4)): Please direct all correspondence regarding this Petition to counsel at the above addresses. Petitioner consents to service by email at the addresses above.

XIII. CONCLUSION

Petitioner respectfully requests the Board institute review and cancel challenged claims as unpatentable.

Respectfully submitted,

MAIER & MAIER, PLLC

/ Thomas J. Gohn /

XIV. CLAIMS APPENDIX

Claim / Element	Claim Language
[1.pre]	A test system for testing circuits of an integrated circuit semiconductor wafer, the test system comprising
[1.a]	a test computer for testing said circuits by generating signals for input to said circuits, processing output signals from said circuits and generating a test result thereof.
[1.b]	a wafer probe, coupled to said test computer, for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer
[1.c]	a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer, wherein said wafer TI layer comprises a plurality of resistive traces traversing said wafer TI layer and wherein said plurality of resistive traces are operable to selectively heat a plurality of zones of said wafer TI layer that correspond to said areas of said wafer;
[1.d]	a cold plate disposed adjacent to said wafer TI layer operable to cool said wafer; and
[1.e]	a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer during said testing by controlling cooling of said cold plate and by controlling selective heating of said plurality of resistive traces of said wafer TI layer
2	The system as described in claim 1 wherein positions of said plurality of zones of said wafer TI layer correspond to a die layout of said wafer and wherein further said wafer TI layer is customized for said wafer.
3	The test system as described in claim 2 further comprising: a chiller for cooling liquid; and a valve for controlling an amount of said liquid flowing to said cold plate, wherein said valve is controlled by said thermal controller.
4	The system as described in claim 2 further comprising: a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and a second TIM layer disposed between said wafer TI layer and said wafer

Claim / Element	Claim Language
5	The system as described in claim 4 wherein said first and second TIM layers comprise indium foil.
6	The system as described in claim 4 wherein said first and second TIM layers comprise graphite material.
7	The system as described in claim 4 further comprising: a first vacuum valve for establishing suction for securing said wafer to said wafer TI layer a second vacuum valve for establishing suction for securing said wafer TI layer to said cold plate; and a vacuum pump coupled to both said first and second vacuum valves
8	The system as described in claim 7 further comprising: a first blow-off valve for controlling air to release said wafer from said wafer TI layer; a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and a source of air coupled to both said first and second blow-off valves
9	The system as described in claim 2 wherein each zone of said plurality of zones corresponds to a respective single die of said die layout of said wafer.
10	The system as described in claim 2 wherein each zone of said plurality of zones corresponds to a respective plurality of dice of said die layout of said wafer.
11	The system as described in claim 2 wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.
12	The system as described in claim 2 further comprising a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical pass through channels which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer.
13	The test system as described in claim 1 further comprising a power supply coupled to provide power to said wafer TI layer and controlled by said thermal controller via pulse-

Claim / Element	Claim Language
	width modulation (PWM) signals, wherein said selective heating of said wafer TI layer is based on said PWM signals
14	The system as described in claim 13 wherein said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from said PWM signals applied to said plurality of resistive traces
[15.pre]	A test system for testing circuits of an integrated circuit semiconductor wafer, the system comprising
[15.a]	a test computer system for testing said circuits by generating signals for input to said circuits, processing output signals from said circuits and generating a test result for said circuits of said wafer
[15.b]	a wafer probe for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer, said wafer probe coupled to communicate with said test computer system
[15.c]	a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer and wherein further said wafer comprises a die layout comprising a plurality of dice and wherein further positions and shapes of said plurality of discretely controllable thermal zones are customized to said die layout of said wafer
[15.d]	a cold plate disposed under said wafer TI layer and operable to cool said wafer; and
[15.e]	a thermal controller for selectively heating and maintaining temperatures of areas of said wafer, during said testing, by controlling cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer.
16	The test system as described in claim 15 wherein each thermal zone of said plurality of discretely controllable

Claim / Element	Claim Language
	thermal zones corresponds to multiple dice of said die layout of said wafer.
17	The test system as described in claim 15 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to a single die of said die layout of said wafer
18	A test system as described in claim 15 wherein each die of said die layout of said wafer corresponds to multiple thermal zones of said plurality of discretely controllable thermal zones of said wafer TI layer.
19	The test system as described in claim 15 wherein said wafer TI layer comprises a plurality of resistive traces traversing said wafer TI layer and operable to selectively heat and maintain temperatures of said plurality of discretely controllable thermal zones of said wafer TI layer responsive to said thermal controller
20	The test system as described in claim 15 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone
21	The test system as described in claim 15 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and while said test computer system is testing a first die of said die layout

Claim / Element	Claim Language
	corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones
22	The test system as described in claim 15 further comprising: a thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer and wherein said TIM layer comprises one of: indium foil; and graphite material.
[23.pre]	A method of testing circuits of an integrated circuit semiconductor wafer, the method comprising
[23.a]	testing said circuits of said wafer by using a test computer system wherein said testing comprises
[23.b]	generating signals for input to said circuits
[23.c]	processing output signals from said circuits
[23.d]	generating a test result for said circuits; and
[23.e]	in conjunction with performing said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of said wafer and wherein said thermal interposer comprises a plurality of separately controllable thermal zones and wherein said selectively heating comprises selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones
24	The method as described in claim 23 wherein said wafer comprises a die layout and wherein further positions and shapes of said plurality of separately controllable thermal zones of said thermal interposer layer are customized to said die layout.
25	The method as described in claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises: bringing a first thermal zone of said plurality of separately controllable thermal zones to a testing temperature; and while said test computer system is testing one or more die of

Claim / Element	Claim Language
	said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of separately controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.
26	The method as described in claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises: bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.
27	The method of claim 24 wherein said plurality of separately controlled thermal zones comprise a plurality of resistive traces and wherein further said selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones comprises said thermal controller selectively energizing said plurality of resistive traces during said testing.

CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

This Petition for *Inter Partes* Review complies with the type-volume limitation of 14,000 words, comprising 13,914 words, excluding the parts exempted by 37 C.F.R. § 42.24(a)(1).

This Petition for *Inter Partes* Review complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word in 14-point Times New Roman font.

Respectfully submitted,

MAIER & MAIER, PLLC

/ *Thomas J. Gohn* /

CERTIFICATE OF SERVICE (37 C.F.R. §§ 42.6(e), 42.105(a))

I certify that the above-captioned **PETITION FOR *INTER PARTES* REVIEW FOR U.S. PATENT NO. 12,320,841** and associated Exhibits 1001-1018 were served in their entireties upon the Patent Owner on October 5, 2026, via courier at the following address:

Advantest c/o Murabito Hao & Barnes LLP
1500 E Hamilton Ave
Suite 118
Campbell, CA 95008

Patent Owner's Correspondence Address of Record for U.S. Patent No. 12,320,841

Respectfully submitted,

MAIER & MAIER, PLLC

/ Thomas J. Gohn /

Thomas J. Gohn
(Reg. No. 72,122)
Counsel for Petitioner