

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AEM AMERICAS, INC.,

Petitioner

v.

ADVANTEST TEST SOLUTIONS, INC.,

Patent Owner

Case IPR2027-00005

U.S. Patent No. 12,320,841

DECLARATION OF PRADEEP LALL, PH.D.

UNDER 37 C.F.R. § 1.68 IN SUPPORT OF PETITION

FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 12,320,841

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I. Introduction

1. I, Pradeep Lall, Ph.D. declare as follows:

2. I have been retained as an expert consultant by Maier and Maier PLLC on behalf of AEM Americas, Inc. (“Petitioner”) in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 12,320,841 (“the ’841 Patent”) (Ex 1001). I have been asked to provide my technical review, analysis, insights, and opinions regarding the references that form the basis for the alleged grounds of unpatentability set forth in the Petition. For this work, I am being compensated for my time, and I am reimbursed for actual expenses. I have no interest in the outcome of this proceeding, and my compensation is not dependent on the content of my opinions or the outcome of this proceeding.

II. Qualifications

3. I am an independent consultant. All opinions stated in this Declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience relating to the technology referenced in this Declaration.

4. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. A copy of my current curriculum vitae, which includes a more detailed summary of my education and

professional experience, is provided as Appendix A to this Declaration. The following provides an overview of some of my technical background and experience that is relevant to the matters set forth in this Declaration.

5. As indicated in my Curriculum Vitae, I received a Bachelor of Engineering (B.E.) degree in Mechanical Engineering from the Delhi College of Engineering in 1988, a Master of Science (M.S.) degree in Mechanical Engineering from the University of Maryland, College Park in 1989, a Doctor of Philosophy (Ph.D.) degree in Mechanical Engineering from the University of Maryland, College Park in 1993, and a Master of Business Administration (M.B.A.) degree in Finance and Strategy from the Kellogg School of Management at Northwestern University in 2002.

6. From 1992 to 1994, I was an Assistant Director at the CALCE Electronic Packaging & Systems Center at the University of Maryland, College Park.

7. From 1994 to 2002, I held various positions at Motorola, Inc., including Lead Engineer (1994-1997), Senior Staff Engineer of the Component & Interconnect Reliability Laboratory (1997-1999), Manager (1999-2001), and Distinguished Member of Technical Staff (2001-2002). My work at Motorola focused the incorporation of ball-grid array and flip-chip packaging into communication

handheld products. I worked on the development of processes for flip-chip assembly in ball-grid array packages such as during the development of the slightly larger than IC carrier package or the SLICC. My work included study of the effects on thermal expansion on reliability in the manufacture and assembly of area-array packages. I also worked on the manufacturing and assembly of fine-pitch packaging into communication products.

8. From 2002 to present, I have been on the faculty of Auburn University, where I am currently the John and Anne MacFarlane Endowed Distinguished Professor and Alumni Professor in the Department of Mechanical Engineering with a courtesy joint appointment in the Department of Electrical and Computer Engineering. Since 2008, I have been the Director of the NSF-CAVE3 Electronics Research Center now named the Auburn University Electronics Packaging Research Institute. I am the founding director of the Alabama Node of NextFlex since 2025 and also member of the Technical-Council of the NextFlex National Manufacturing Institute since 2015. In addition, I am a member of the Governing Council of the NextFlex National Manufacturing Institute. I am the academic co-lead of the automotive and asset monitoring technical working groups. In these roles, I work on the design, manufacturing, and reliability of electronics in various extreme environments including temperature, humidity, high-g acceleration, and vibration.

9. I have taught courses in various aspects of mechanical engineering, business, electronics design, and manufacturing at Auburn University, national and international Conferences. The courses I teach include topics related to the '841 patent subject matter. In addition, I am the lead author of the book titled "Influence of Temperature on Microelectronics and System Reliability," published by CRC Press in 1997. The book focuses on the failure mechanisms activated by exposure to temperature, including sustained temperature, thermal cycling, temperature gradients, and time-dependent temperature change. These are the kinds of failure mechanisms that are intended to be activated in tests discussed in the 841 patent.

10. During my tenure at Auburn University, I have worked on various aspects of single-chip and multichip packaging. Specifically, I have worked on the design, reliability, and manufacturing of large ball-grid arrays for harsh environment applications, including automotive underhood, aerospace, and downhole. In addition to large ball grid arrays, I have worked on chip-scale packages, multichip packages, and flip-chip configurations, studying various related aspects such as reliability, stresses, interconnects, and manufacturing processes. More recently, I have studied the processes for ultra-thin chips fabrication and assembly onto flexible substrates for flexible hybrid electronics applications.

11. I have served on the technical program committee for numerous conferences with peer-reviewed proceedings, including ASME International Mechanical Engineering Congress and Exposition, EuroSIME, IEEE Prognostics Health Management Conference, ITHERM Conference, and ASME InterPACK Conference. These activities reflect my focus on the manufacture, reliability, test, life-prediction of electronics and finite-element analysis of electronics.

12. I have written over 1000 papers, 2 books, and 15 book chapters in the field of semiconductor packaging. A few of my representative co-authored publications in the area of thermo-mechanical reliability of electronics, which is relevant to the technology at issue are listed below. A complete list of my publications can be found in my CV:

- Lall, P., Bhat, C., Hande, M., More, V., Vaidya, R., Goebel, K., Prognostication of Residual Life and Latent Damage Assessment in LeadFree Electronics Under Thermo-mechanical Loads, IEEE Transactions on Industrial Electronics, Vol. 58, No. 7, pp. 2605-2616, July 2011.
- Lall, P.; Hande, M.; Bhat, C.; Lee, J., Prognostics Health Monitoring (PHM) for Prior Damage Assessment in Electronics Equipment Under ThermoMechanical Loads, IEEE Transactions on Components, Packaging and Manufacturing Technology, Volume: 1, Issue: 11, Page(s): 1774 - 1789, 2011

- Lall, P., Vaidya, R., More, V., Goebel, K., Assessment of Accrued ThermoMechanical Damage in Leadfree Parts During Field-Exposure to Multiple Environments, SMTA Journal, Vol. 23(2), pp. 11-24, 2010.
- Lall, P., Hande, M., Bhat, C., More, V., Vaidya, R., Prognostication of system-state in lead-free electronics equipment under cyclic and steady-state thermo-mechanical loads,” Microelectronics Reliability, Vol. 49(8), pp. 825- 838, 2009.
- Thermo-mechanical Reliability Management Models for Area-Array Packages on Cu-Core and No-Core Assemblies, Lall, P., Shah, M., Drake, L., Moore, T., Suhling, J., SMTA Journal, Vol. 21, No. 3, pp. 20-35, 2008.
- Lall, P., M. Kasturi, J. Suhling, and D. Locker, Stress Strain Analysis on Stitch Bond of Cu-Al Wirebonds Using X-ray Micro-CT Technique, in Proceedings of the IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, Las Vegas, NV, pp. 841-846, May 28-31, 2019.
- Lall, P., N. Kothari, S. Deshpande, and L. Nguyen, Study of the Effect of Solder-Joint Voiding using X-ray MicroCT Data-based FE Models with Experimental Validation, in Proceedings of the Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, Las Vegas, NV, pp. 1160-1167, May 28-31, 2019.
- Lall, P., K. Goyal, B. Leever and J. Marsh, Thermo-mechanical Deformation in Flexible-board Assemblies during Reflow and Post-

assembly Usage, in Proceedings of IThERM, San Diego, CA, US, pp. 26-32, May 29-June 1, 2018.

- Lall, P., Harsha, M., Goebel, K., Jones, J., KEYNOTE PRESENTATION: Interrogation of Thermo-Mechanical Damage in Field-Deployed Electronics, IEEE EuroSIME Conference, Cascais, Portugal, pp. 1-16, April 15-18, 2012.
- Lall, P., P., Harsha, M., Suhling, J., Goebel, K., Jones, J., Accrued Damage and Remaining Useful Life in Field Extracted Assemblies Under Sequential Thermo-mechanical Loads, ASME International Congress and Exposition (IMECE), Paper IMECE2011-65834, pp. 1-16, Denver, CO, November 11- 17, 2011.
- Lall, P., Harsha, M., Goebel, K., Jones, J., Prognostication of Remaining Useful Life and Prior Thermo-mechanical Damage in Field-Deployed Electronics, SMTAI Conference, pp. 301-316, Ft. Worth, TX, Oct 16-20, 2011.
- Reliability of BGA and CSP on Metal-Backed Printed Circuit Boards in Harsh Environments, Lall, P., Islam, N, Evans, J., Suhling, J., ASME Journal of Electronic Packaging, Volume 129, pp. 382-290, December 2007.
- Reliability of BGA and CSP on Metal-Backed Printed Circuit Boards in Harsh Environments, Lall, P., Islam, N, Evans, J., Suhling, J., ASME Journal of Electronic Packaging, Volume 129, pp. 382-290, December 2007.

- Damage Mechanics of Electronics on Metal-Backed Substrates in Harsh Environments, Lall, P., Islam, M. N., Suhling, J., IEEE Transactions on Components and Packaging Technologies, Volume 29, Number 1, pp. 204- 212, March 2006.
- Lall, P., Islam, S., Suhling, J., Tian, G., Nano-Underfills for SnPb and SnAgCu Flip-Chip Applications in Extreme Environments, Proceedings of the ITherm 2006, 10th Intersociety Conference on Thermal and Thermomechanical Phenomena, San Diego, California, May 30-June 2, 2006.
- Lall, P., Shah, M., Drake, L., Moore, T., Suhling, J., Thermo-Mechanical Reliability Management Models For Area-Array Packages On Cu-Core And No-Core Assemblies, Proceedings of the Surface Mount Technology International (SMTAI), Orlando, Florida, pp. 582-596, October 7-11, 2007.
- Lall, P., G. Hariharan, A. Shirgaokar, J. Suhling, M. Strickland, J. Blanche, Thermo-Mechanical Reliability Based Part Selection Models for Addressing Part Obsolescence in CBGA, CCGA, FLEXBGA, and Flip-Chip Packages, ASME InterPACK Conference, Vancouver, British Columbia, Canada, IPACK2007-33832, pp. 1-18, July 8-12, 2007.
- Rudrapati, S., Lall, P., Thermo-Mechanical Reliability Of Flip-Chip Devices On metal Backed Flex Circuits, Proceedings of the Surface Mount Technology (SMTA) International, Chicago, Illinois, pp. 487-

494, September 24-28, 2006. o Lall, P., Islam, S., Suhling, J., Tian, G., Nano-Underfills for SnPb and SnAgCu Flip-Chip Applications in Extreme Environments, Paper to Appear in Proceedings of the ITHERM 2006, 10th Intersociety Conference on Thermal and Thermo-mechanical Phenomena, San Diego, California, May 30-June 2, 2006.

- Models for Thermo-Mechanical Reliability Trade-offs for Lead and Lead-Free Flip-Chip Electronics in Extreme Environments, Lall, P., Singh, N., Strickland, M., Blanche, J., Suhling, J., Proceedings of the Surface Mount Technology (SMTA) International, Chicago, Illinois, pp. 500-511, September 25-29, 2005.
- Damage Mechanics of Electronics on Metal-Backed Substrates in Harsh Environments, Lall, P., Islam, N., Shete, T., Evans, J., Suhling, J., Gale, S., Proceedings of the 54th IEEE Electronic Components and Technology Conference, Las Vegas, Nevada, pp. 704-711, June 1 - 4, 2004.
- Model for BGA and CSP in Automotive Underhood Environments, Lall, P., Islam, N., Suhling, J., Darveaux, R., Proceedings of the 53rd Electronic Components and Technology Conference, New Orleans, Louisiana, pp. 189- 196, May 27-30, 2003
- Assembly-Level Reliability of Flex-Substrate BGA, Elastomer-on-Flex Packages, and 0.5 mm Pitch Partial Array Packages, Lall, P., Banerji, K, Microelectronics Reliability Journal, Volume 40, pp. 1081-1095, 2000.

- Reliability Characterization of the SLICC Package, Pradeep Lall, Glenn Gold, Barry Miles, Kingshuk Banerji, Pat Thompson, Corey Koehler, Indira Adhihetty, Proceedings of the Electronics Components and Technology Conference (ECTC), Orlando, Florida, pp. 1202-1210, May 28-31, 1996.

13. I am the recipient of SMTA Founder's Award in 2024 for exceptional contributions to Electronics Manufacturing, SEMI R&D Achievements Award for landmark contributions to Additive Manufactured Electronics in 2023, ASME Avram Bar-Cohen Memorial Medal in 2022, IEEE Biedenbach Outstanding Engineering Educator Award in 2020, IEEE Electronic Packaging Society's 2018 Outstanding Sustained Technical Contribution Award, and a recipient of the Auburn University's 2018 Research Advisory Board's Advancement of Research and Scholarship Achievement Award. I received the National Science Foundation Alex Schwarzkopf Prize for Technology Innovation in 2016, Alabama Academy of Science Wright A, Gardner Award in 2016, IEEE Exceptional Technical Achievement Award in 2014, ASME-EPPD Applied Mechanics Award in 2013, SMTA's Member of Technical Distinction Award in 2013, Auburn University's Creative Research and Scholarship Award in 2013, SEC Faculty Achievement Award in 2013, Samuel Ginn College of Engineering Senior Faculty Research Award in 2007 and 2016. In total, my research in the field of electronics has been

recognized by over 40-awards. In addition, my publications have received over 50 best-paper awards at national and international conferences. A more complete list of my awards and honors can be found in my CV.

14. In 2026, I was elected for a third term on the IEEE Electronic Packaging Society Board-of-Governors. I am a named a Fellow of the NextFlex National Manufacturing Institute on Flexible Electronics. In addition, I am a fellow of the ASME, IEEE, and the Alabama Academy of Science.

15. I have also served on numerous technical committees, including as a member of National Academies Committee on Electronic Vehicle Controls, a Member of the IEEE Reliability Society AdCom, the IEEE Electronics Packaging Society Representative on the Artificial Intelligence Policy Committee, the IEEE Reliability Society Representative on the IEEE-USA Government Relations Council for R&D Policy, the Chair of Congress Steering Committee for the ASME Congress, a Member of the technical committee of the European Simulation Conference EuroSIME, Associate Editor for the IEEE Access Journal, and Associate Editor for the IEEE Transactions on Components and Packaging Technologies.

16. I have extensive experience in the fields of semiconductor packaging and testing, semiconductor chip interconnects, materials used in packaging, and testing hardware and software.

17. I am qualified to reach the opinions and conclusions stated in this Declaration. My opinions address the thermal aspects of the challenged combinations, including heat transfer across the thermal interposer, cold-plate cooling, thermal-interface materials, and the motivation and expectation of success in achieving uniform, zone-selective thermal control, drawing on my research and expertise in electronics thermal management and reliability.

18. In forming my opinions, I rely on my knowledge and experience in the fields relevant to this Declaration. I further rely on documents and information referenced in this Declaration.

19. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae attached to this Declaration.

III. Materials Reviewed

20. The opinions contained in this Declaration are based on the documents I have reviewed, my professional judgment, and my education, experience, and knowledge relating to power control and related fields. In forming my opinions, I have reviewed all materials referenced by the Petition and all materials listed in the List of Exhibits provided above (as well as any other materials and information I reference in this Declaration).

21. My opinions contained in this Declaration are based on the documents I have reviewed and considered, as well as my knowledge and professional judgment. My opinions have been guided by my appreciation of how a person of ordinary skill in the art (“POSITA”) would have understood the state of the art, the prior art, and the claims and the specification of the ’841 Patent at the time of the alleged invention.

22. The time of the alleged invention of the ’841 Patent encompasses the time frames near and including November 19, 2020. I understand the application for the ’841 Patent claims priority to a provisional application (provisional application No. 63/115,813), which was filed on November 19, 2020. My opinions reflect how a POSITA (which I describe below) would have understood the ’841 Patent, the prior art to the ’841 Patent, and the state of the art at the time of the alleged invention:

IV. Understanding of Legal Principles

23. I am not a lawyer, and I will not provide legal opinions. I have been advised that certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and validity of patent claims. The legal principles listed in Sections IV, V, VI, VII, VIII, and IX have been used for the purpose of my analysis.

24. I understand that a patent claim is invalid if it is anticipated or rendered obvious over the prior art and that a claim can be unpatentable even if all requirements of the claim cannot be found in a single prior art reference. I further understand that invalidating a claim requires that the claim be anticipated or rendered obvious from the perspective of a POSITA at the time the invention was made.

25. In forming my analysis, opinions, and conclusions expressed in this Declaration, I have applied the legal principles set forth below, which were provided to me by counsel.

V. Types of Claims

26. I understand that there are two types of U.S. patent claims: 1) independent claims, and 2) dependent claims. I understand that independent claims only include the aspects stated in the independent claim. I further understand that dependent claims include the aspects stated in the independent claim, and any other aspects stated in any claim from which that dependent claim depends, as well as any limitations required by the dependent claim.

VI. Anticipation

27. I understand that a claim in an issued patent can be invalid if it is anticipated. In this case, “anticipation” means there is a single prior art reference that discloses every element of the claim, arranged in the way required by the claim, either expressly or inherently.

28. I understand that anticipation of a claim requires that every element of a claim is disclosed expressly or inherently in the single prior art reference. I understand that “inherent” disclosure means that the claim element, although not expressly described by the prior art reference, must necessarily be present based on the disclosure. I understand that a mere probability that the element is present is not sufficient to qualify as “inherent disclosure.”

VII. Obviousness

29. I understand that a claim in an issued patent can be rendered invalid if it is obvious. Unlike anticipation, obviousness does not require that every element of the claim be in a single prior art reference. Instead, it is possible for claim elements to be described in different prior art references or that a claim element in a prior art reference might be modified, so long as there is motivation or sufficient reasoning to combine the references or make the modification and a reasonable expectation of success of doing so.

30. I understand that a claim is invalid for obviousness if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious from the perspective of a person of ordinary skill in the relevant art at the time the invention was made. I also understand that, when evaluating obviousness, one must consider obviousness of the claim “as a

whole.” This must be from the perspective of the person of ordinary skill in the relevant art at the time the invention was made.

31. I further understand that exemplary rationales that may support a conclusion of obviousness include:

- a) combining prior art elements according to known methods to yield predictable results;
- b) simple substitution of one known element for another to obtain predictable results;
- c) use of known technique(s) to improve similar devices (methods or products) in the same way;
- d) applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- e) “obvious to try” - choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- f) known work in one field of endeavor may prompt variations of the work for use in either the same field or a different field based on design incentives or other market forces if the variations are predictable to a POSITA; and

g) some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

32. In analyzing obviousness, I understand that it is important to understand the scope of the claims, the level of skill in the relevant art, the scope and content of the prior art, the differences between the prior art and the claims, and any “secondary considerations” (described below). I also understand that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Although I understand that it is not required, there may also be a specific “teaching, suggestion or motivation” to combine any first prior art reference with a second prior art reference. Such a “teaching, suggestion, or motivation” to combine the first prior art reference with the second prior art reference can be explicit or implicit and may provide further evidence of obviousness.

33. I understand that secondary (or objective) considerations are relevant to the determination of whether a claim is obvious. Such secondary (or objective) considerations can include evidence of commercial success caused by an invention, evidence of a long-felt need that was solved by an invention, evidence that others

copied an invention, or evidence that an invention achieved a surprising or unexpected result, among others. I understand that such evidence must have a nexus, or causal relationship to the elements of a claim, to be relevant to a determination of obviousness of the claim.

34. I also understand that, at least in IPR proceedings, admissions in the patent or in the prosecution file history of the patent (Applicant Admitted Prior Art or “AAPA”) can be used to establish background knowledge possessed by a POSITA, to furnish a motivation to combine, to assess whether a patent’s claims would have been obvious, and/or to supply a missing limitation.

VIII. Claim Construction

35. I understand that, for purposes of my analysis, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning” at the time the alleged invention was made. In determining the ordinary and customary meaning, the words of a claim are given the plain meaning that those words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to assist in the construction of a claim term. Additionally, treatises and dictionaries may be used, in limited circumstances, to determine the meaning attributed by a POSITA to a claim term at

the time of filing as long as such extrinsic input is consistent with the claim term as used in the claim.

36. For all claim terms considered in this Declaration, I have applied the ordinary and customary meaning of those terms as they would have been understood by a POSITA at the time the alleged invention was made. To the extent the Patent Owner proposes any constructions, or the Board construes any claims, I reserve the right to address such proposals or constructions. Under any reasonable construction of the claims, it is my opinion that the prior art discloses and/or suggest all the limitations recited in challenged claims of the '841 Patent.

IX. Person of Ordinary Skill in the Art

37. I understand that my assessment and determination of invalidity must be undertaken from the perspective of what would have been known or understood by a POSITA at the time of the earliest patent application supporting the '841 Patent.

38. I have been informed and understand that the POSITA is not a real person, but rather a legal construct - a hypothetical person. This person is presumed to have known the relevant art at the time of the invention. I have been informed by counsel that relevant factors in determining the level of ordinary skill include (1) the educational level of the inventor, (2) the type of problems encountered in the art, (3) prior art solutions to those problems, (4) the rapidity with which innovations are

made, (5) sophistication of the technology, and (6) the educational level of active workers in the field. I further understand that the person of “ordinary skill” is not a person of extraordinary skill in the art. In other words, this person of ordinary skill is not necessarily an expert in the field.

39. As of the alleged November 19, 2020 priority date, a POSITA would have held at least a bachelor’s degree in electrical engineering, mechanical engineering, or a related field, together with approximately two to three years of experience in semiconductor test equipment or thermal management of electronic devices. Additional education could substitute for experience, and vice versa.

40. At the time of the alleged invention, I was a person of at least ordinary skill in the art, and I have applied the perspective of the POSITA in forming and expressing my opinions below.

X. Technical Background and the Prior Art

41. Wafer-level electrical testing is used to characterize semiconductor devices before a wafer is diced and packaged. A probe assembly establishes electrical contact with multiple integrated-circuit sites, while a supporting chuck holds the wafer and establishes the test environment.

42. Figure 1 shows a semiconductor wafer prober with test head, probe card, cover panels, and other accessories removed. Internal parts are shown; the linear motor and platen, chuck, stage, and material handling elements are shown.

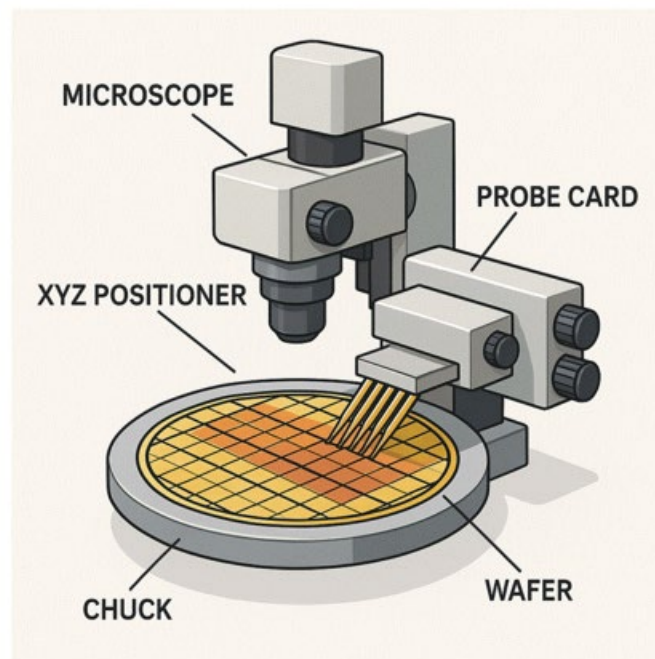


Figure 1: Schematic of Wafer Prober Parts (<https://anysilicon.com/wafer-probe/>)

43. The chuck or vacuum stage securely hold the wafer and provide temperature control over a broad range, typically from $-60\text{ }^{\circ}\text{C}$ to $300\text{ }^{\circ}\text{C}$, for stress testing. The optical microscope provides high-resolution imaging, motorized zoom, and autofocus for precise alignment. The XYZ θ positioners use motorized micrometer stages to enable nanometer-scale movement of the wafer along the X, Y, Z, and theta axes relative to the probes. The probe-card pins interface with the

test system and the die bond pads, establishing electrical contact while maintaining a consistent contact force, typically 3–5 g per needle.

44. Figure 2 and Figure 3 shows an actual wafer on a test stage with probes. The chuck for holding the wafer is also shown in Figure 3.

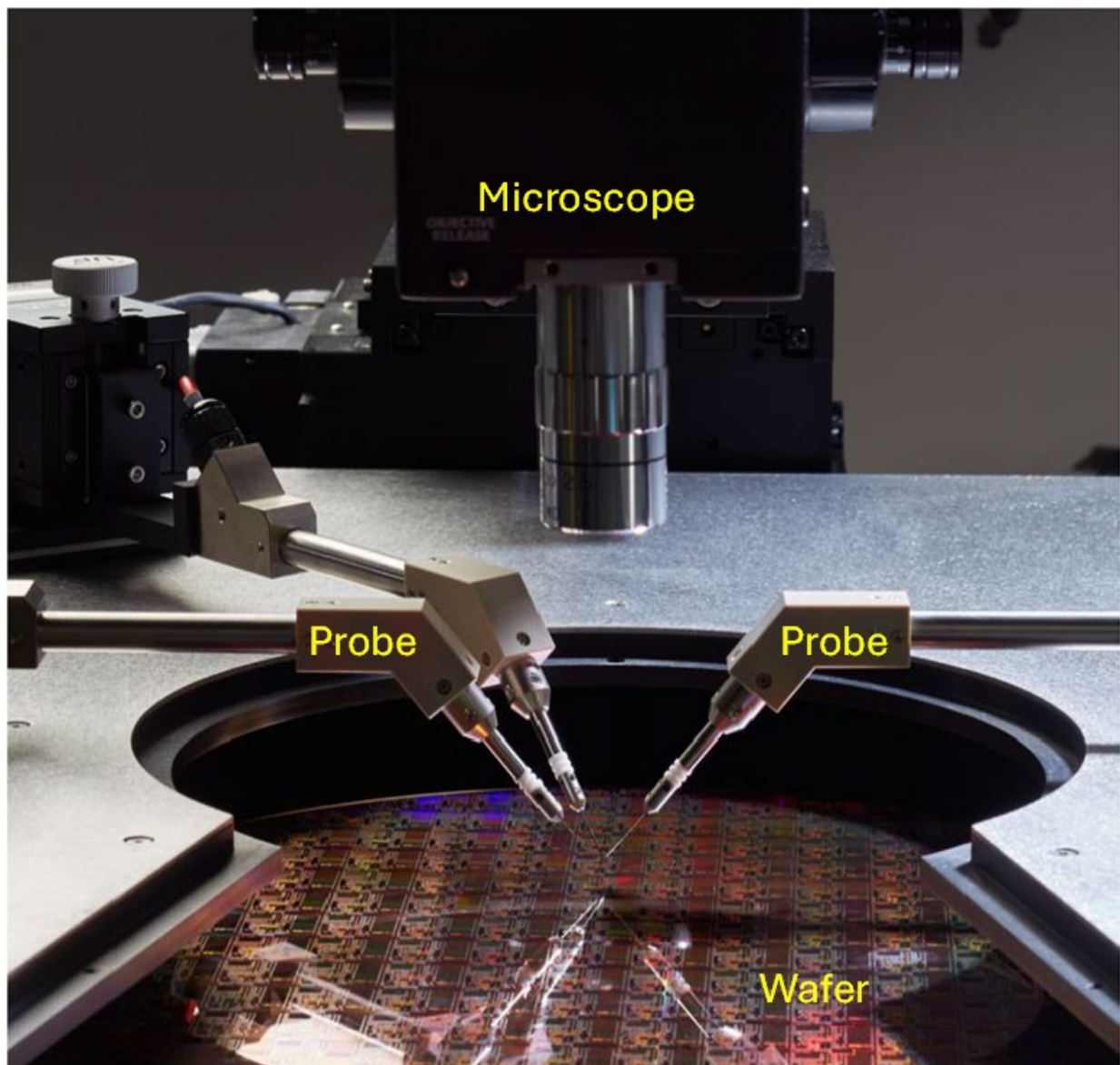


Figure 2: Actual Wafer on Probe Station with Microscope and Probes (Annotation Added) (<https://www.inseto.com/wp-content/uploads/2018/12/SemiProbe-Corporate-Capabilities.pdf>)

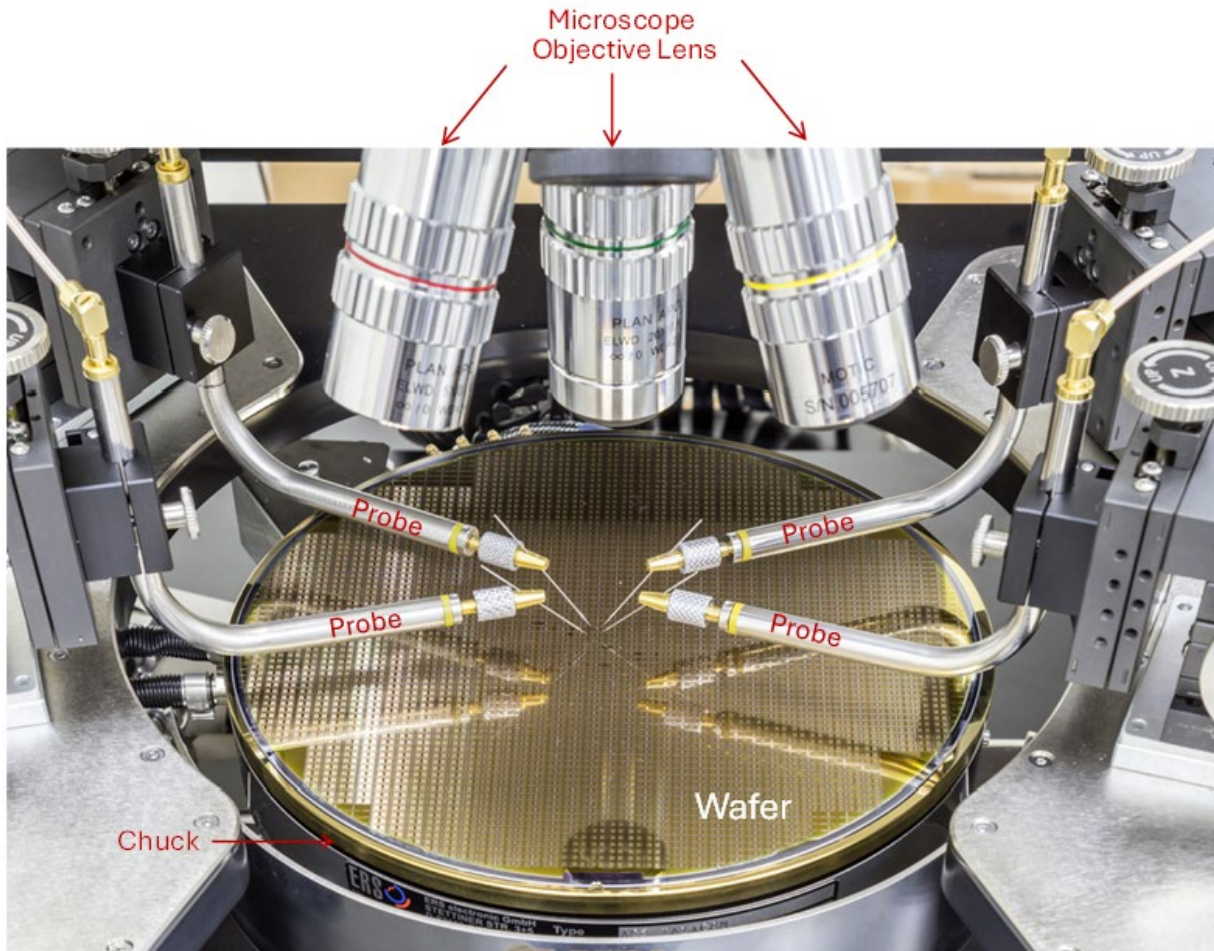


Figure 3: Actual Wafer on Probe Station with Microscope, Chuck and Probes (Annotation Added) (<https://www.integra-tech.com/testing-qualification/electrical-test/wafer-probe>)

45. In high-volume environments, an additional test system & handler are used to automate the wafer handling and integrate with ATE (Automatic Test Equipment) to sequence test wafers. In such applications, the microscope may be

replaced with machine vision. In addition, single probes may be replaced with a probe card.

46. A standard prober can accommodate a limited number of probe positions, typically around 8 to 12, and manual manipulators around the platen opening. Each probe tip must also be positioned manually by the operator, a labor-intensive task that requires substantial time and experience. For devices with more than 12 pins, probe cards therefore become essential.

47. A probe card includes a wafer prober, whose probes serve as connectors between the chip contact pads on the wafer and a tester, which serves as a measuring machine. The probe card needles contact the chip contact pads to perform electrical testing for the go/no-go test. The wafer test process is highly important and highly dependent on the reliability of probe cards. Figure 4 shows a probe card with integrated probes that swivels onto the wafer for electrically testing the chips on the wafer. In alternate configurations, the probe card may contact the wafer by descending vertically on the wafer that is mounted on the chuck.

Wafer Test System

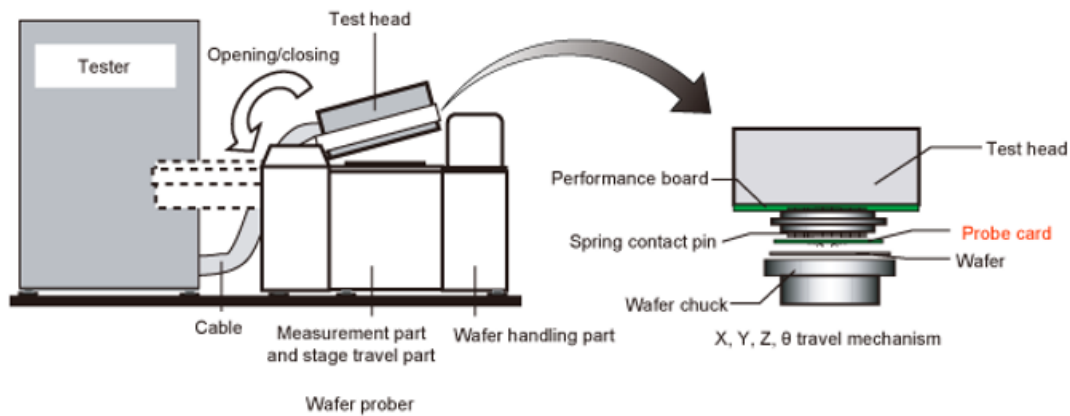


Figure 4: Swivel Probe Card (https://www.twmjc.com.tw/en/technical_column-detail/55/)

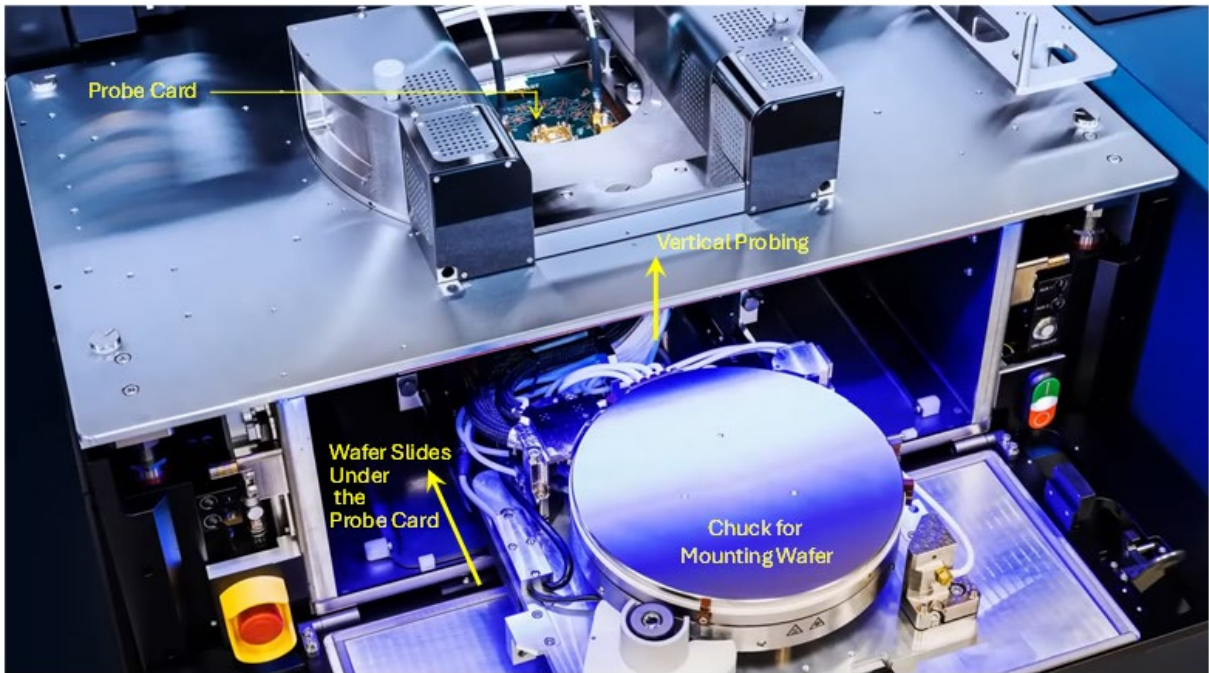


Figure 5: Vertical Probe Card on SUMMIT200 Probe Station for 200mm Wafers
(Still Taken from Video; Annotations Added)
(<https://www.youtube.com/watch?v=Otf1ZO6-IfA>)

48. The dynamic motorized Z-chuck is used to hold the wafer in place. In order to make electrical contact or step between different dies, the automated system moves this chuck vertically up and down along the Z-axis to contact the vertical probes for the purpose of chip test.

49. The chuck is typically an electrostatic chuck (ESC), which holds down a wafer securely using electrostatic attraction generated by an applied electrical voltage (Figure 6). A high DC voltage is applied to the internal electrodes buried in a thin ceramic or insulating dielectric layer inside the chuck. The electric field induces an opposite electrical charge on the back side of the wafer resting on top. The attraction between the opposing positive and negative charges creates a strong electrostatic clamping force that pulls and holds the wafer flat against the chuck surface.

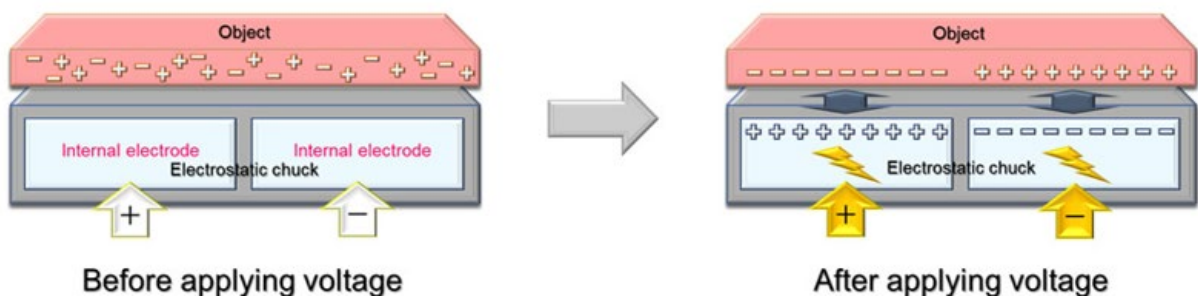


Figure 6: Electrostatic Chuck for Holding Down Wafers
(<https://creative-technology.co.jp/esc-e/>)

50. Alternatively, the wafer may be held down with mechanical vacuum or atmospheric pressure differential. The chuck in this case is called a dry interface chuck owing to the reliance on the physical contact to facilitate extreme heat dissipation without leaving a wet, residue on the wafer back side.

51. Probe-Testing is typically done to identify defective chips earlier in the process, prior to packaging, and to prevent incurring additional cost associated with packaging defective chips.

52. Temperature is a critical test variable because device performance, leakage current, timing behavior, and failure mechanisms can vary substantially with on-chip junction temperature.

53. In addition, devices are exposed to temperature fluctuations due to power dissipation, power cycling, ambient temperature cycling, and the differing thermal conductivities of the packaging materials surrounding the chip.

54. Owing to various parts of the semiconductor chip performing different functions, the heat dissipation is often not uniform. Thus, some parts of the chip are hotter than others in normal operation.

55. Accurate characterization during semiconductor probe testing, therefore, depends not only on setting a nominal wafer temperature but also on

maintaining each powered device near its intended temperature throughout the test interval.

56. If the testing is done at the wafer level instead of the chip level, individual dies can dissipate different amounts of electrical power because of variation in deposited materials, variations in the interfaces, process drift, or chip performance. These differences are used to precipitate the defective part of the wafer population.

57. During the test, it is therefore critical to replicate the operating conditions, exposing the chips to varying temperatures during the chip test. The operating conditions are replicated in the test by application of external temperatures.

58. The resulting heating during test is used to identify the areas of high defect or performance drift under simulated conditions experienced in operation when the chip is packaged with surrounding chips or passives that also dissipate heat and create thermal gradients.

59. The temperatures may be imposed uniformly in a thermal chamber or non-uniformly by an external source capable of imposing gradients. Both approaches address the same underlying engineering problem, i.e., one of identifying the propensity of temperature-activated failure mechanisms that are triggered early

in device life by sustained temperature exposure, temperature swings, spatial thermal gradients, and time-dependent temperature changes.

60. For example, in the U.S. Patent 5,001,423 dated March 19, 1991, temperature variation is used to create a controlled and repeatable thermal condition under which the chip's electrical performance can be tested reliably. The wafer chuck is divided into several temperature-sensor (Element 3) and cooling-element domains corresponding to the chip regions of the overlying undiced wafer. In this patent, the wafer prober electrically energizes one chip on the undiced wafer. That chip dissipates power and becomes the localized heat source. Temperature sensors (Element 3) distributed across the chuck are scanned to identify the thermal domain beneath the energized chip. The selected sensor supplies feedback to a closed-loop controller. The controller adjusts cooling using thermoelectric modules (Element 4) to keep the active chip's junction temperature near the prescribed test temperature, described as approximately 25 °C. The semiconductor tester then applies electrical test patterns and determines whether the chip meets its functional or parametric requirements.

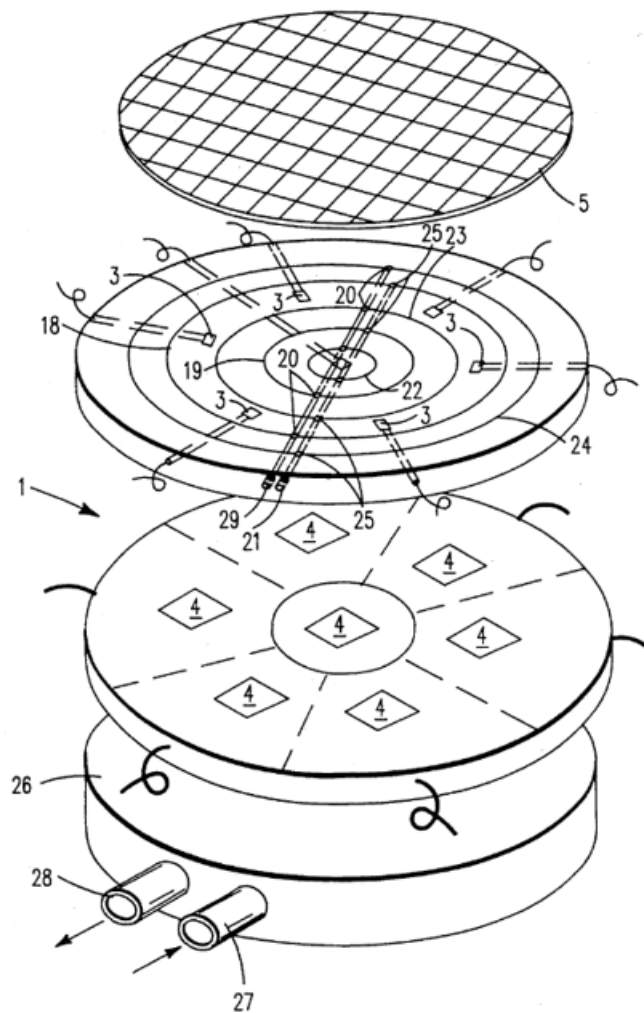


FIG. 2

Figure 7: Temperature Controlled Chuck (U.S. Patent 5,001,423 dated March 19, 1991) with thermocouple sensors (Element 3) and thermoelectric modules (Element 4) for temperature control.

61. The role of temperature in detection of subsurface defects in wafers has long been known. In A. N. Danilewsky et al., “Crack Propagation and Fracture in Silicon Wafers Under Thermal Stress,” Journal of Applied Crystallography, vol. 46, pp. 849–855, 2013; A silicon wafer containing edge microcracks was heated under

an imposed temperature gradient to generate thermal stress. In-situ X-ray diffraction imaging was used to distinguish cracks that became active under the applied gradient. The authors state that potentially dangerous cracks could be identified from the strain-related contrast around the crack tip (Figure 8).

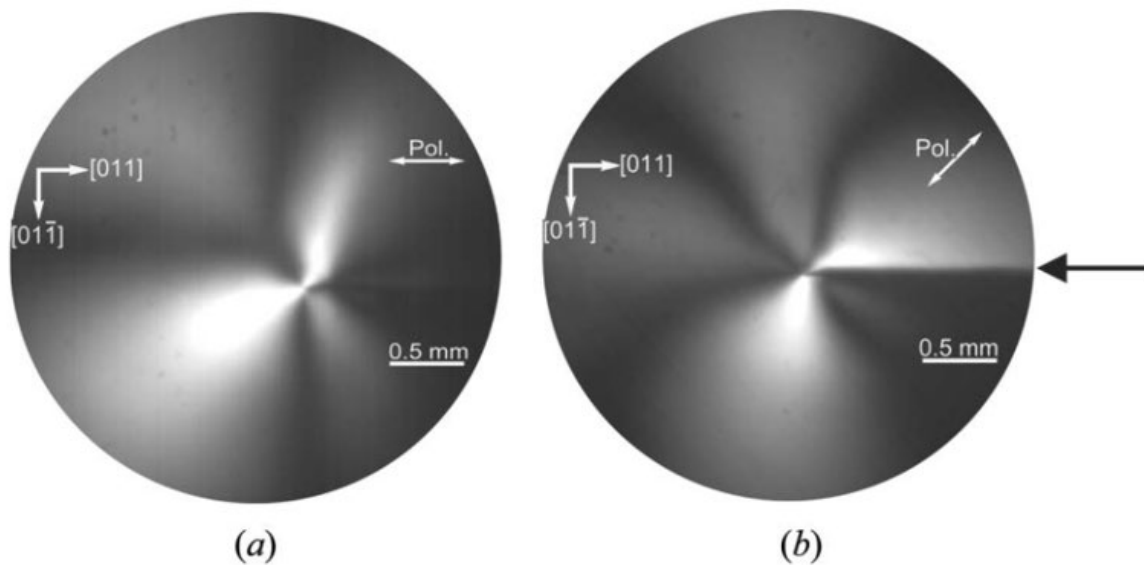


Figure 5

Polarized infrared images showing the strain around the tip of crack C3 after the second heating (black arrow indicates crack position). The asymmetric lobes indicate the inclined 60° dislocations to be the origin of the strain. (a) Polars parallel and perpendicular to crack direction. (b) Polars at 45° to crack direction.

Figure 8: Crack Detection Under Thermal Gradients (A. N. Danilewsky et al., “Crack Propagation and Fracture in Silicon Wafers Under Thermal Stress,” Journal of Applied Crystallography, vol. 46, pp. 849–855, 2013)

62. In J. Wang, G. Udupa, and B. K. A. Ngoi, “High-Speed Imaging for Evaluation of Silicon Wafer Defects,” Proceedings of SPIE, vol. 5852, 2005; the

wafer was subjected to externally applied dynamic thermal loading. The applied heating generated a transient, spatially varying thermal-strain field. Subsurface impurities and voids disturbed that field, and the disturbances were detected using speckle-shearing interferometry. The method has been used to identify good wafers from defective wafers in thermal stressing. Figure 9 shows regular fringes representing a good wafer, indicating a uniform and homogenous deformation distribution over the wafer. Figure 10 shows fringe irregularities that reveal subsurface defects localized in a suspicious region of the wafer.

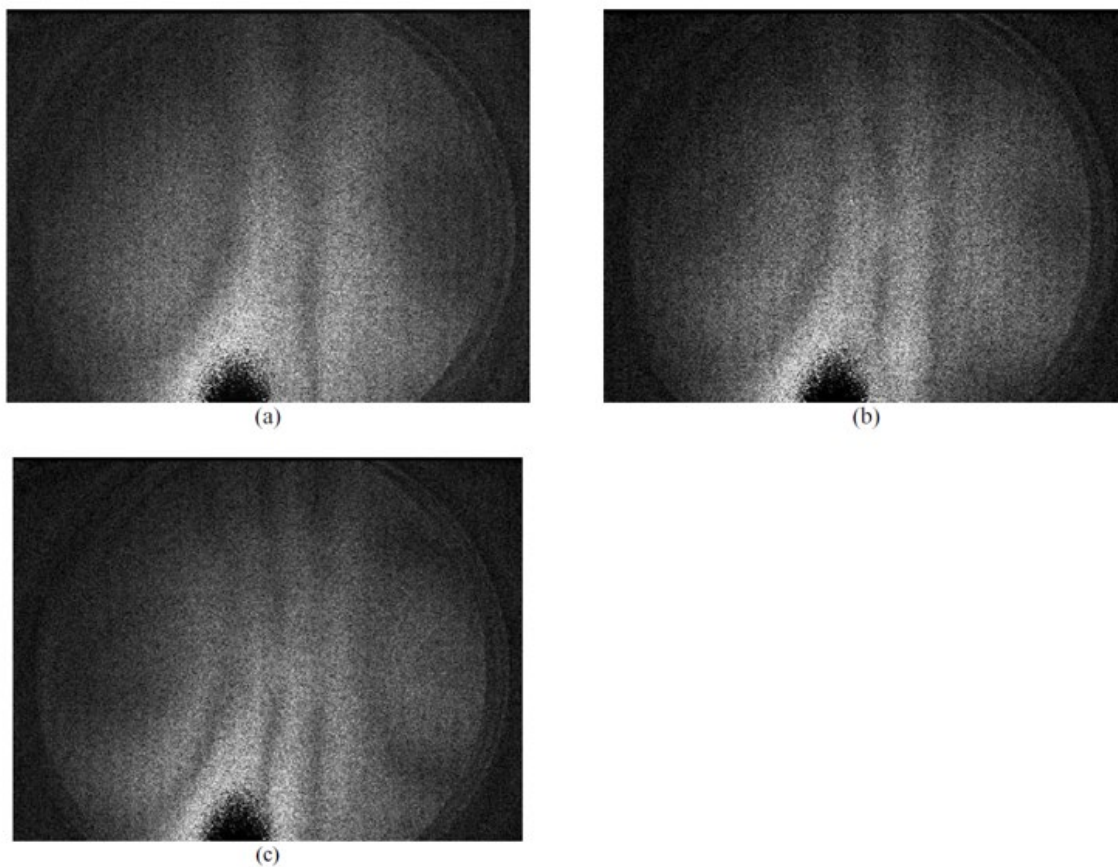


Fig. 5 A sequence of speckle correlograms representing a good wafer subject to a continuous thermal stressing. The images are captured at (a) 0.4s, (b) 0.6s, and (c) 0.8s after lighting.

Figure 9: Identification of Good Wafer in Thermal Stressing.

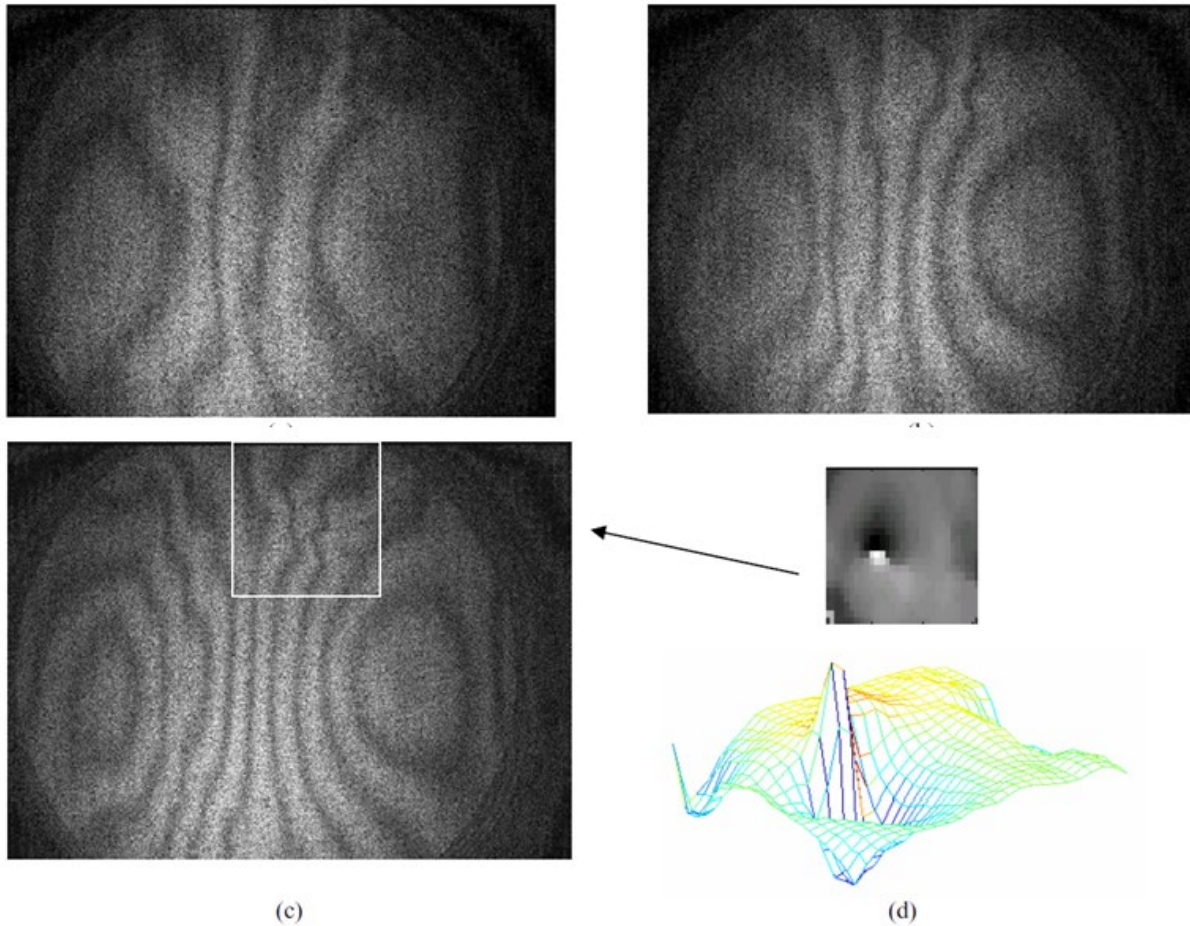


Fig. 6 Speckle correlograms captured at (a) 0.4s, (b) 0.6s, and (c) 0.8s after heating, representing a defective wafer. (d) is the phase change during the deformation time from 0.8s to 0.4s in a suspicious region of (c).

Figure 10: Identification of Defective Wafer in Thermal Stressing.

XI. The '841 Patent

63. The '841 Patent addresses temperature variations that can arise during wafer-level electrical testing when individual circuits dissipate different amounts of power. The patent explains that conventional systems applying a substantially uniform temperature across a wafer may not adequately compensate for localized heating associated with particular circuits or regions.

64. The '841 Patent discloses a wafer-scale active thermal-interposer layer positioned against a second surface of the wafer, opposite the surface contacted by the wafer probe. The thermal-interposer layer is configured to selectively heat areas of the wafer rather than applying heat uniformly across the entire wafer.

65. The disclosed system further includes a cold plate disposed beneath the wafer thermal-interposer layer and a thermal controller that coordinates cooling by the cold plate with selective heating by the thermal-interposer layer. In this manner, the system can maintain selected wafer areas at desired temperatures during testing.

66. In the disclosed test stack, a wafer probe contacts a first surface of the wafer to probe individual circuits, while the wafer thermal-interposer layer contacts the opposing surface, and the cold plate is positioned beneath that layer. This arrangement permits electrical testing and spatially selective thermal conditioning to occur in the same system.

67. The '841 Patent describes using this architecture to compensate for nonuniform device heating during wafer testing. By controlling temperature on a regional basis, the system is intended to support testing of multiple circuits while providing more localized temperature control than systems that heat or cool the wafer as a whole.

68. In one disclosed embodiment, the test system includes a tester system, a wafer probe, a wafer thermal-interposer layer, a cold plate, and a thermal controller. The tester system generates signals for input to the wafer circuits and processes output signals from those circuits, while the remaining components provide probing and thermal control during testing.

69. The wafer thermal-interposer layer may include a plurality of resistive traces arranged to define separately controllable thermal zones. The thermal controller selectively energizes the traces so that heat can be applied to corresponding areas of the wafer as required during testing.

70. The thermal controller is configured to maintain temperatures in selected wafer areas by controlling operation of the cold plate and the selective heating performed by the wafer thermal-interposer layer. The patent thus employs coordinated heating and cooling rather than relying on either function alone.

71. The disclosed embodiments position the wafer probe at a first surface of the wafer and the wafer thermal-interposer layer at the opposing surface. This configuration allows the probe to contact circuits from one side while thermal conditioning is applied from the other side.

72. The '841 Patent further describes controlling the separately controllable thermal zones in response to temperature information associated with the wafer or

the test stack. This control permits the energy supplied to selected resistive traces to be adjusted to maintain the desired temperature conditions during testing.

73. The '841 Patent also discloses methods in which multiple circuits of a wafer are electrically tested while corresponding wafer areas are selectively heated, and the wafer is cooled. The thermal controller coordinates these operations to maintain the temperatures of the selected areas during the testing process.

XII. Summary of Prior Art

U.S. Pat. No. 6,549,026 (DiBattista)

74. DiBattista et al. (US 6,549,026) describes an apparatus and method for controlling the temperature of integrated-circuit devices while the devices are tested on a semiconductor wafer.

75. The system uses a wafer chuck to locate and support the devices during testing, with multiple temperature-control devices positioned to correspond to the arrangement of the individual IC devices on the wafer.

76. Overall wafer temperature can be regulated by heating or cooling the chuck, including by circulating a temperature-controlled fluid through the chuck.

77. Localized temperature control is provided by associating a temperature-control device, such as a heating element, with each IC device being tested, allowing

heat to be supplied where it is needed rather than controlling only the wafer as a whole.

78. In an alternative configuration, each temperature-control device and its corresponding IC device can be associated with a separate heat sink, enabling localized removal of heat during testing.

79. The DiBattista patent addresses the difficulty of maintaining selected device temperatures when individual IC devices generate different amounts of heat during electrical operation and test. Conventional chuck-level heating or cooling alone may not compensate adequately for these localized thermal differences.

80. The DiBattista invention combines global chuck heating or cooling with temperature-control components aligned to individual devices, thereby improving control of the thermal conditions experienced by each IC device across the wafer.

81. The patent design is intended to improve temperature uniformity and test repeatability, reduce device-to-device thermal variation, and enable more reliable electrical characterization of wafer-level IC devices under controlled temperature conditions.

FIG. 2A

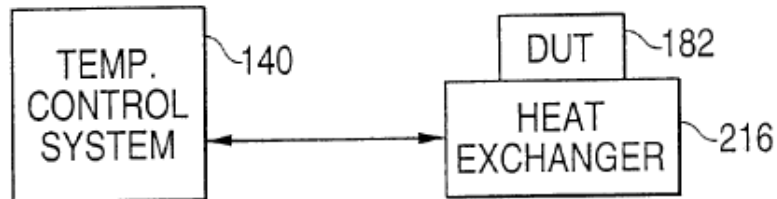


FIG. 2B

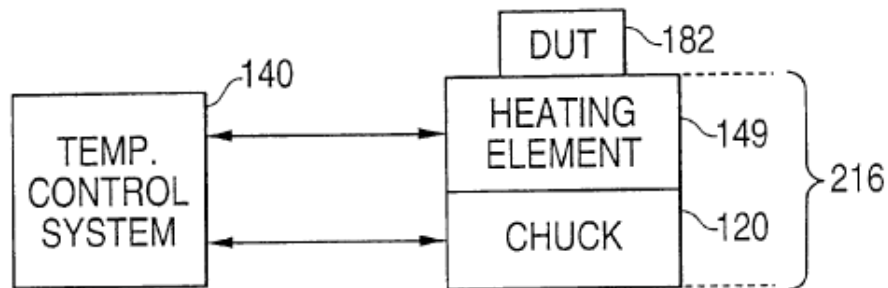


FIG. 2C

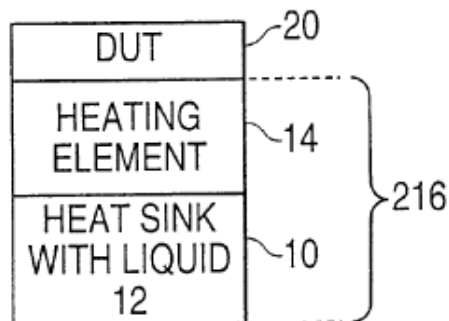


Figure 11: Wafer-level arrangement of temperature-control devices corresponding to individual IC devices.

Overall thermal-control system

- **140** — Temperature-control system that controls the heat exchanger **216**
- **216** — Heat exchanger thermally coupled to the device under test
- **182** — Device under test (**DUT**), preferably in physical contact with a surface of heat exchanger **216**

Figure 2B implementation

- **120** — Chuck forming part of heat exchanger **216**
- **149** — Heating element associated with chuck **120** and in thermal contact with DUT **182**

Figure 2C implementation

- **14** — Heating element forming part of heat exchanger **216**
- **10** — Heat sink associated with heating element **14**
- **12** — Temperature-regulated liquid used to control the temperature of heat sink **10**

Functional relationships

- In **FIG. 2A**, temperature-control system **140** regulates heat exchanger **216**, which controls the temperature of DUT **182**.
- In **FIG. 2B**, heat exchanger **216** is implemented as chuck **120** with heating element **149**.
- In **FIG. 2C**, heat exchanger **216** includes heating element **14** and liquid-regulated heat sink **10**, with liquid **12** providing temperature control.
- Although one DUT **182** is illustrated, the disclosed system is intended to provide individual thermal control for multiple integrated-circuit devices during simultaneous wafer-level testing.

FIG. 3

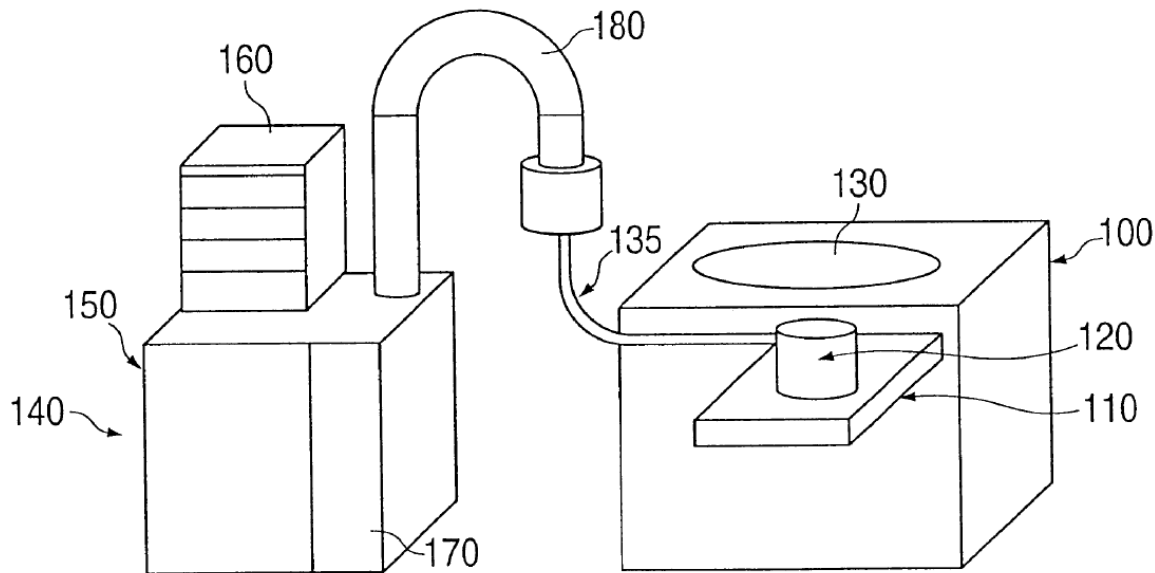


Figure 12: Relationship among the wafer, chuck, heating or cooling components, and localized temperature-control arrangement.

Wafer-prober assembly

- **100** — Wafer prober used to test semiconductor integrated-circuit devices formed on a wafer
- **110** — Stage of the wafer prober
- **120** — Chuck carried by stage **110**; supports the wafer containing the semiconductor devices

Electrical-test interface

- **130** — Test-head interface that provides electrical connections to the power and input/output pads of the devices on the wafer
 - The connections may be needles or another suitable form of electrical contact

Connections to the temperature-control system

- **135** — Housing containing the fluid-supply lines and control cables that connect chuck **120** to temperature-control system **140**

Temperature-control equipment

- **140** — Temperature-control system that regulates the temperature of the device under test at or near a selected set-point temperature, including compensation for device self-heating
- **150** — Thermal-control chassis containing the principal temperature-control components
- **160** — System controller with an operator interface
- **170** — Liquid-cooling and recirculation system
- **180** — Boom arm supporting the fluid-supply lines and control cables

Functional relationship

- Wafer prober **100** positions the wafer on the chuck **120**.
- Test-head interface **130** electrically contacts the devices.
- Temperature-control system **140** communicates with chuck **120** through the lines and cables in housing **135**.
- Chassis **150**, controller **160**, cooling and recirculation system **170**, and boom arm **180** work together to maintain the test device near the desired temperature despite self-heating.

U.S. Pat. Pub. No. 2002/0017916 (Costello)

82. Costello (US 2002/0017916 A1) describes a temperature-controlled semiconductor wafer chuck for a probe-test station. The chuck supports and vacuum-holds a wafer while directly heating or cooling it during manufacturing, testing, characterization, and failure analysis.

83. An independent temperature control is enabled through a primary heater near the chuck's top surface and a secondary heater near its bottom surface allow the two regions to be controlled separately, helping establish and maintain the desired wafer-side temperature.

84. Heat removal is achieved through an integrated heat sink that removes thermal energy from the chuck, supporting operation across both elevated and reduced test temperatures.

85. Reduced thermal distortion is achieved through multiple layers above the heat sink that are joined in a way that accommodates differential thermal expansion and contraction, minimizing warpage or loss of flatness as temperature changes.

86. Improved mechanical stiffness using an integrated heat-sink and layer structure that stiffens the chuck so it better resists deformation caused by probe-pin forces during electrical testing.

87. The Costello Patent uses wafer chucks that holds a wafer accurately while subjecting it to hot and cold test conditions. Temperature gradients and mismatched material expansion can distort the chuck, while probe forces can further deflect it, compromising contact consistency and measurement accuracy.

88. Costello combines active heating, cooling, independent top-and-bottom temperature regulation, expansion-tolerant layer connections, and structural reinforcement in one chuck system.

89. Costello's design is intended to provide more uniform thermal conditions, preserve chuck flatness and rigidity, and improve repeatability when

semiconductor wafers or related components are evaluated over a range of temperatures.

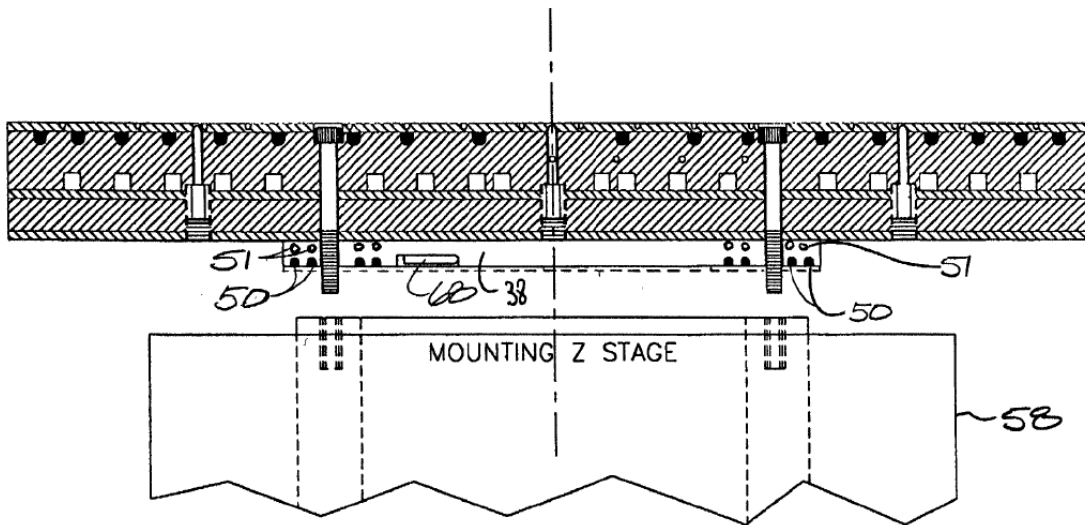


FIG. 4

Figure 13: Layered chuck construction, including the wafer-supporting region, heater structure, heat sink, and thermal interfaces.

- **38** Thermal insulator or insulation layer
- **50** Secondary heater fitted into thermal insulator **38**
- **51** Air- or liquid-cooling channels in thermal insulator **38**; cool the insulator and provide additional control of the chuck-base temperature
- **58** Prober stage
- **68** Secondary temperature sensor, or an array of sensors, located in thermal insulator **38** near its bottom. Directly senses temperature near the prober stage

Functional Relationship

Secondary heater **50**, cooling channels **51**, and secondary temperature sensor **68** regulate the lower portion of chuck **14**. This helps minimize temperature-induced distortion of prober stage **58**. The dual-secondary-heater embodiment also permits lower temperatures at chuck top surface without excessively cooling prober stage **58**.

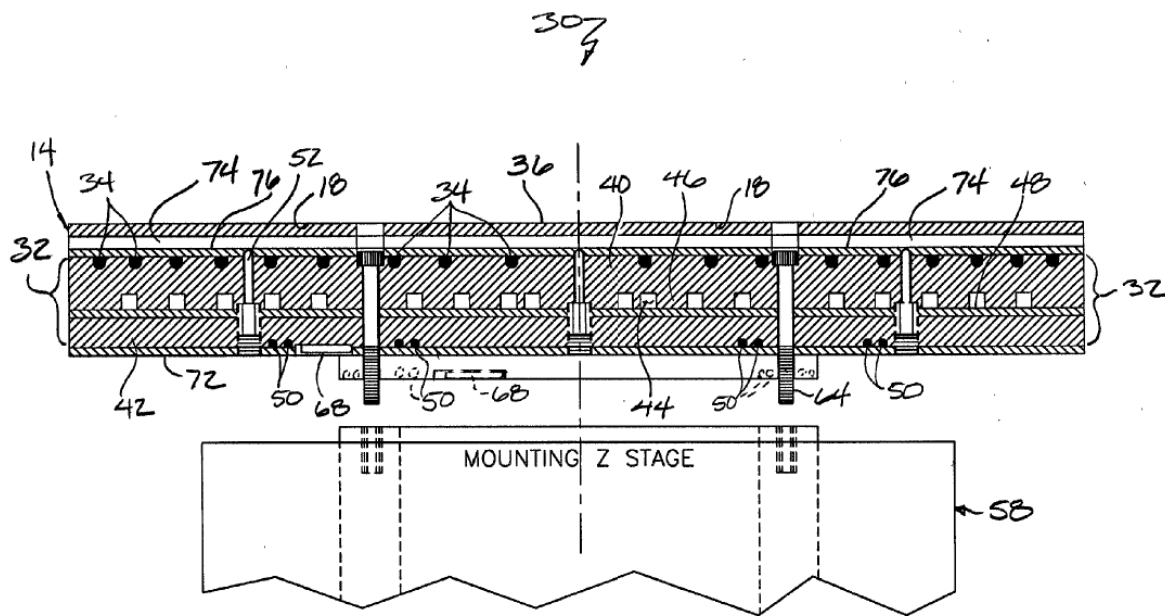


FIG. 5

Figure 14: Relationship between the chuck layers and the upper and lower temperature-control components.

- **14** — Temperature-controlled chuck
- **18** — Chuck top surface
 - Supports the test wafer
 - Electrically isolated to reduce leakage current and electrical noise
 - May be biased to a selected voltage for sensitive measurements
- **32** — Heat-sink assembly
- **34** — Primary heater

- **36** — Chuck top plate defining the chuck top surface **18**
- **40** — Heat-sink core layer
 - Contains the cooling-fluid channels **44** and pillars **46**
 - Provides cooling performance and structural stiffness
- **44** — Cooling-fluid channels formed in heat-sink core layer **40**
 - Circulate coolant through the heat sink
 - Are positioned near the middle of the layered heat-sink assembly for increased strength
- **46** — Pillars formed within heat-sink core layer **40**
 - Provide heat-transfer surface area between the chuck and coolant
 - Reinforce the heat sink against probing forces applied normal to chuck top surface **18**
- **50** — Secondary heater
- **58** — Prober stage
- **72** — Chuck bottom plate
 - Also functions as the **secondary-heater cover plate**
 - Is brazed to the heat-sink structure and helps increase structural rigidity and thermal transfer
- **74** — Electrical-isolation layer positioned between chuck top plate **36** and the heater/heat-sink structure
 - Maintains electrical isolation of chuck top **18**
 - May be retained by vacuum, ceramic bolts, or other electrically isolating means
- **76** — Primary-heater cover plate
 - Positioned above primary heater **34** and heat-sink core layer **40**
 - Brazed to the heat-sink assembly to improve rigidity and thermal coupling

Functional Relationship

Chuck top plate **36**, isolation layer **74**, and primary-heater cover plate **76** are arranged above heat-sink assembly **32**. The layers can move laterally and vertically relative to one another during heating and cooling, reducing bowing or warping caused by different thermal-expansion rates.

Within the heat-sink core layer **40**, cooling channels **44** provide coolant circulation while pillars **46** improve both heat transfer and mechanical stiffness. Chuck bottom plate **72** closes and reinforces the lower portion of the assembly and serves as a cover plate for secondary heater **50**.

U.S.2 Pat. Pub. No. 2011/0000426 (Herchen-1)

90. Herchen (US 2011/0000426 A1) describes a substrate-processing apparatus for controlling the temperature of semiconductor substrates, particularly wafers undergoing photolithography-related heating processes.

91. The apparatus includes top and bottom planar members with a heater layer positioned between them. The heater layer is retained by evacuating the region between the planar members, allowing vacuum force to secure the layered assembly without relying solely on permanent bonding.

92. The heater layer is formed from alternating electrically insulating and conducting layers, with resistive heater elements patterned in the conducting layers to produce controlled heating across the substrate-support surface.

93. The patterned heater elements can be arranged in separately controllable zones, enabling different regions of the apparatus to receive different amounts of heat and supporting improved temperature uniformity across the wafer.

94. The assembly can be thermally coupled to a cooling plate, with a compliant thermal-interface pad between the heater-bearing member and the cooling structure to improve heat transfer and accommodate surface or dimensional variations.

95. Herchen-1 addresses temperature nonuniformity and assembly difficulties in substrate-heating equipment. Conventional bonded heater stacks can be difficult to manufacture, repair, or keep in uniform thermal contact when their layers expand differently during repeated heating and cooling.

96. Herchen-1 combines patterned zoned heaters, insulating layers, vacuum retention, regulated vacuum interfaces, and a cooling-plate structure. These features relate to the later claim analysis by supplying independently controlled heater zones, multilayer heater construction, thermal-interface material, and vacuum-assisted attachment and release functions.

97. Herchen-1 is intended to provide uniform and responsive wafer heating, reliable thermal contact between replaceable layers, simplified assembly and servicing, and improved temperature control during semiconductor substrate processing.

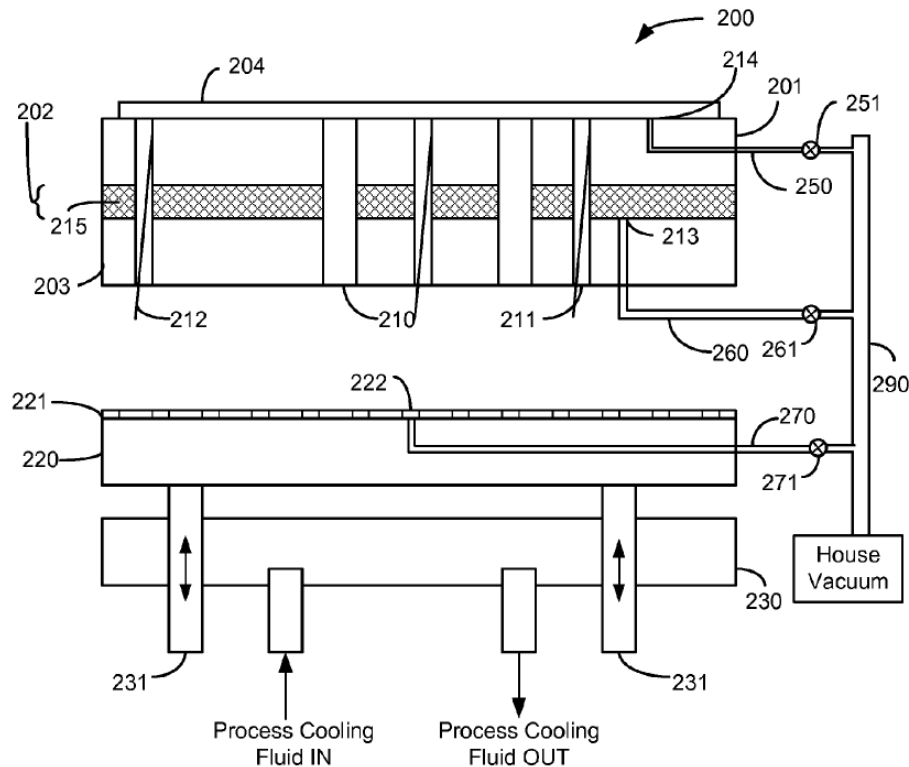


FIG. 2

Figure 15: Overall layered apparatus and vacuum-held heater arrangement.

Main assembly

- **200** — Substrate-processing apparatus; in some embodiments, a bake plate
- **201** — Top planar member that supports the substrate
- **202** — Evacuatable region between the top and bottom planar members; contains the heater layer
- **203** — Bottom planar member
- **204** — Substrate, such as a silicon, quartz, glass, or gallium-arsenide wafer
- **215** — Heater layer positioned in region **202** and trapped between planar members **201** and **203** when the region is evacuated

Substrate support and vacuum retention

- **214** — Vacuum ports used to hold the substrate against proximity pins on top planar member **201**
- **250** — Exhaust line connecting vacuum ports **214** to the house vacuum system

- **251** — Regulator for exhaust line **250**
- **290** — House vacuum system

Heater-layer vacuum system

- **213** — Vacuum port for evacuating region **202**
- **260** — Exhaust line connecting vacuum port **213** to house vacuum system **290**
- **261** — Regulator for exhaust line **260**

Lift and temperature-sensing components

- **210** — Lift-pin holes extending through the planar-member assembly
- **211** — Sensor through-holes
- **212** — Temperature sensors installed in sensor through-holes **211**; may be RTDs, thermocouples, or thermistors

Movable upper cooling assembly

- **220** — Movable top cooling plate positioned below bottom planar member **203**
- **221** — Thermal material or thermal pad on the upper surface of cooling plate **220**
- **222** — Vacuum ports embedded in thermal material **221** to establish and maintain the thermal gap
- **231** — Air cylinders that move top cooling plate **220** vertically
- **270** — Exhaust line connecting vacuum ports **222** to house vacuum system **290**
- **271** — Regulator for exhaust line **270**

Lower cooling assembly

- **230** — Stationary bottom cooling plate having fluid channels for active cooling; it removes heat from top cooling plate **220** when the plates are brought together

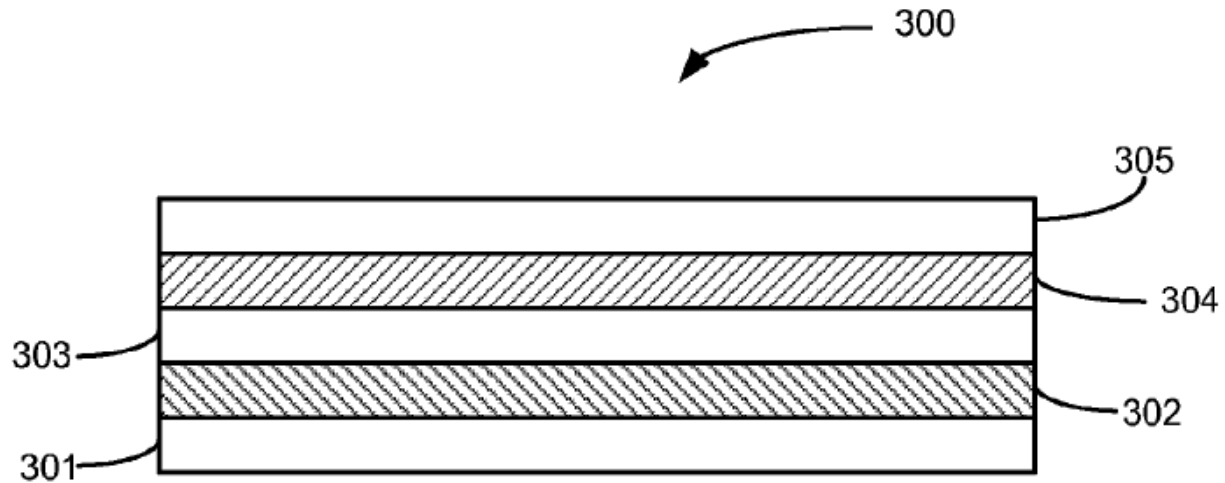


FIG. 3

Figure 16: Patterned heater layer and separately controllable heating regions.

- Insulating layers **301, 303, and 305** electrically isolate conducting layers **302 and 304** from one another.
- The complete layered stack—**301/302/303/304/305**—may be laminated or lapped into a single heater structure.
- Heater elements may be **etched, screen printed, or bonded** onto the conducting layers.

- **300** — Heater assembly
- **301** — First insulating layer
- **302** — First conducting layer disposed over and thermally coupled to insulating layer **301**
 - May include one or more heater elements arranged in a predetermined pattern
 - In one embodiment, provides **single-zone heating** for the substrate
- **303** — Intermediate or second insulating layer disposed over conducting layer **302**
- **304** — Second conducting layer disposed over insulating layer **303**
 - May include patterned heater elements
 - May form multiple independently controlled heating zones

- One disclosed example has **six independent heating zones**, each provided with a separate temperature sensor
- **305** — Final or upper insulating layer disposed over conducting layer **304**

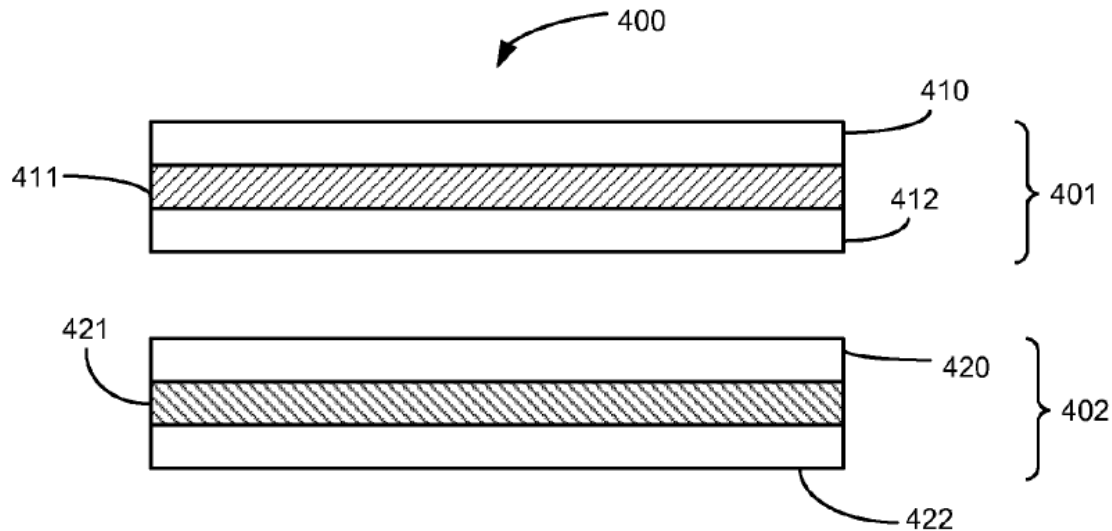


FIG. 4

Figure 17: The cooling plate, thermal-interface structure, and vacuum connections.

Overall heater

- **400** — Heater assembly in the alternate embodiment; formed from two separate heater stacks

First heater stack

- **401** — First heater stack; may provide multiple independently controlled heating zones
- **410** — Insulating layer of first heater stack **401**
- **411** — Conducting layer of first heater stack **401**
 - Located between insulating layers **410** and **412**
 - May contain heater elements arranged in multiple independently controlled heating zones
 - May have a zone pattern similar to conducting layer **304** in Figure 3
- **412** — Second insulating layer of first heater stack **401**

Second heater stack

- **402** — Second heater stack; separate from stack **401**
- **420** — Insulating layer of second heater stack **402**

- **421** — Conducting layer of second heater stack **402**
 - Located between insulating layers **420** and **422**
 - May have characteristics similar to conducting layer **302** in Figure 3
- **422** — Second insulating layer of second heater stack **402**

Associated apparatus feature

- **202** — Evacuatable region of the substrate-processing apparatus in which heater stacks **401** and **402** may be positioned and held together by vacuum

U.S. Pat. Pub. No. 2008/0160462A1 (Herchen-2)

98. Herchen et al. (US 2008/0160462 A1) describe a method and system for controlling heat transfer between a bake plate and a semiconductor substrate in a thermal-processing module of a track lithography tool.

99. The apparatus includes a bake plate having a process surface and an opposing lower surface, together with proximity pins that support the substrate at a controlled spacing above the process surface.

100. Multiple electrodes coupled to the bake plate receive drive signals and produce response signals that can be processed as capacitance measurements, allowing the system to determine the local gap between different portions of the substrate and the bake plate.

101. A chill plate is coupled beneath the bake plate through flexible members and defines multiple independently addressable chambers. Fluid channels connect the chambers to one or more pressurized-fluid sources.

102. Based on the measured substrate-to-plate gaps, the controller can vary pressure in selected chambers to locally deflect or position the bake plate and thereby compensate for substrate bow, warpage, or other shape variations.

103. Herchen-2 advances the state of the art by addressing nonuniform heat transfer caused by spatial variations in the gap between a wafer and a bake plate. Such variations can produce different heating rates and temperatures across the substrate during photolithographic processing.

104. The invention combines distributed capacitive gap sensing, chamber-specific pneumatic actuation, compliant mechanical coupling, and chill-plate support so that the thermal interface can be adjusted locally rather than treating the substrate and bake plate as uniformly spaced rigid bodies.

105. The design is intended to improve substrate-temperature uniformity, compensate dynamically for wafer shape, and increase the repeatability of bake and cure processes. In the later claim analysis, Herchen-2 provides additional support for a controlled thermal-interface structure and material choices used to improve conformity and heat transfer between adjacent thermal components.

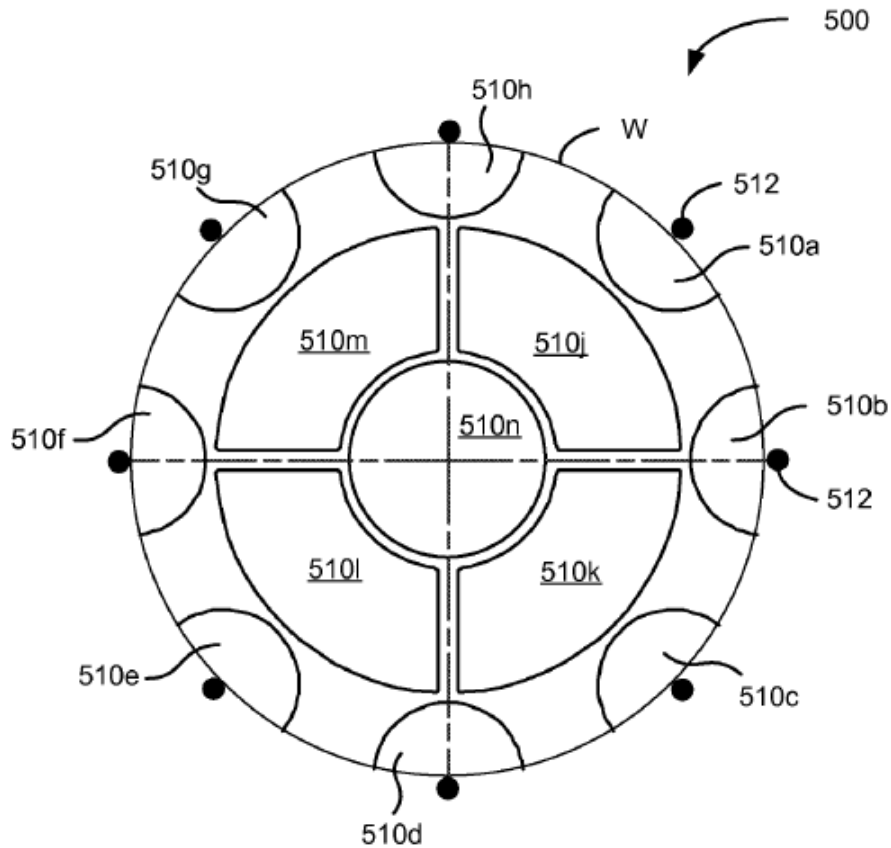


Figure 18: Electrodes 510 is positioned to provide capacitive coupling data for internal and peripheral positions of the substrate

500 — bake plates with integrated capacitive sensors
510 / 510a–510h — peripheral electrodes
510j–510n — interior electrodes
512 — mechanical stops or bosses defining the wafer pocket
W — wafer

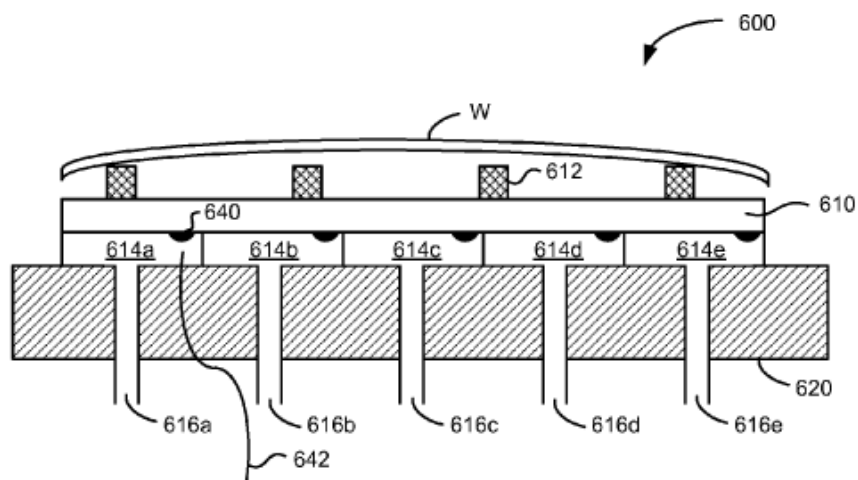


FIG. 6A

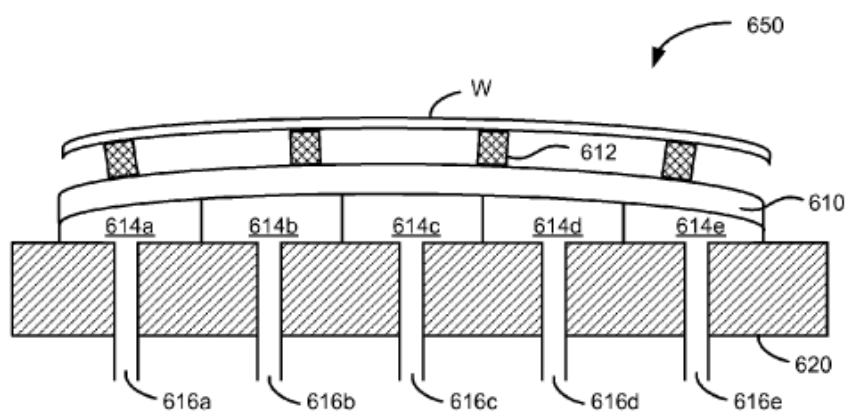


FIG. 6B

Figure 19: Proximity Pins (612) on Bake Plate (610) and Pressure Chambers (614) on Chill Plate (620)

W — bowed wafer
610 — bake plate
612 — proximity pins

614 / 614a–614e — independently controlled sealed pressure chambers 616 / 616a–616e — corresponding fluid ducts 620 — chill plate

COMPARISON OF HERCHEN-1 AND HERCHEN-2

106. Both patents seek improved wafer-temperature uniformity in semiconductor processing. Herchen-1 controls the heat source itself through patterned, independently controlled resistive-heater zones. Herchen-2 controls the heat-transfer path by sensing and modifying the local gap between the wafer and bake plate. Herchen-1 uses vacuum primarily to hold layers together while Herchen-2 uses fluid pressure primarily to mechanically adjust the bake plate.

107. The references are complementary: Herchen-1 supplies the zoned heater and layered thermal-stack architecture, while Herchen-2 supplies active gap sensing and localized mechanical compensation.

Aspect	Herchen-1 — US 2011/0000426 A1	Herchen-2 — US 2008/0160462 A1
Primary objective	Produce uniform, controllable wafer heating using a multilayer heater assembly.	Produce uniform wafer heating by correcting variations in the gap between the wafer and bake plate.
Main structure	Top and bottom planar members enclosing a patterned heater layer.	Bake plate positioned above a chambered chill plate and supporting the wafer on proximity pins.

Aspect	Herchen-1 — US 2011/0000426 A1	Herchen-2 — US 2008/0160462 A1
Control mechanism	Separately controllable resistive-heater zones directly vary local heat generation.	Capacitive electrodes measure local wafer-to-plate gaps; chamber pressure is adjusted to locally deform or position the bake plate.
Vacuum or pressure function	Vacuum retains the heater layer between the planar members and maintains thermal contact between layers.	Pressurized fluid independently actuates chambers beneath the bake plate to compensate for wafer bow or warpage.
Cooling arrangement	A cooling plate is thermally coupled to the heater-bearing assembly through a compliant thermal-interface pad.	A chill plate provides cooling and also contains the independently controlled pressure chambers.
Problem addressed	Temperature nonuniformity, differential thermal expansion, and manufacturing or servicing difficulties associated with bonded multilayer heater assemblies.	Temperature nonuniformity caused by spatial variations in the physical gap between a bowed or warped wafer and the bake plate.
Principal advancement	A vacuum-retained, replaceable multilayer heater stack with independently controlled heating zones and an adjoining cooling structure.	Closed-loop measurement and mechanical correction of the wafer-to-bake-plate gap using distributed capacitance sensing and pneumatic actuation.
Nature of control	Primarily thermal and electrical : local heater	Primarily geometric and mechanical : local spacing is measured and

Aspect	Herchen-1 — US 2011/0000426 A1	Herchen-2 — US 2008/0160462 A1
	power is adjusted by zone.	corrected to improve heat transfer.
Relevance to the claim analysis	Stronger support for independently controlled heater zones, multilayer heater construction, vacuum interfaces, cooling-plate structure, and compliant thermal-interface layers.	More supplementary support for controlled thermal interfaces, conformity between adjacent components, localized adjustment, and graphite or

U.S. Pat. Pub. No. 2013/0220989 – (Pease)

108. Pease et al. (US 2013/0220989 A1) describes a multiplexed heater array for controlling the temperature of a semiconductor substrate in a plasma-processing apparatus.

109. The heating plate contains multiple independently controllable planar heater zones distributed laterally across an electrically insulating layer, allowing the system to tune the spatial temperature profile of the supported substrate.

110. The heater zones are arranged in a scalable multiplexing layout using branch transmission lines, common transmission lines, diodes, and electrical interconnections so that many zones can be addressed without requiring a separate pair of external power conductors for every heater.

111. The heating plate can be manufactured by bonding ceramic or polymer sheets that carry the planar heater zones, transmission lines, and vias, producing a thin multilayer structure suitable for incorporation into a substrate-support assembly.

112. The substrate-support assembly can include an electrostatic clamping electrode and a temperature-controlled base plate, thereby combining localized surface heating with substrate retention and bulk cooling or temperature regulation.

113. The heater array may be powered with alternating current or phase-alternating direct-current drive. The spatial arrangement and alternating drive reduce net magnetic fields above the support assembly and help limit plasma nonuniformity associated with heater-current-generated electromagnetic fields.

114. Pease advances the state of the art by addressing the need for fine-grained temperature correction across semiconductor substrates while limiting wiring complexity, conductor count, magnetic-field effects, and the difficulty of scaling independently controlled heater zones to larger arrays.

115. Pease shows scalable die-sized planar heater zones, thin-film or etched-foil heater construction, selective zone energization, multiplexed or pulse-based power control, integration with a cooling plate, and substrate lift or handling features. The design is intended to improve temperature uniformity and process repeatability across the wafer.

Fig.1

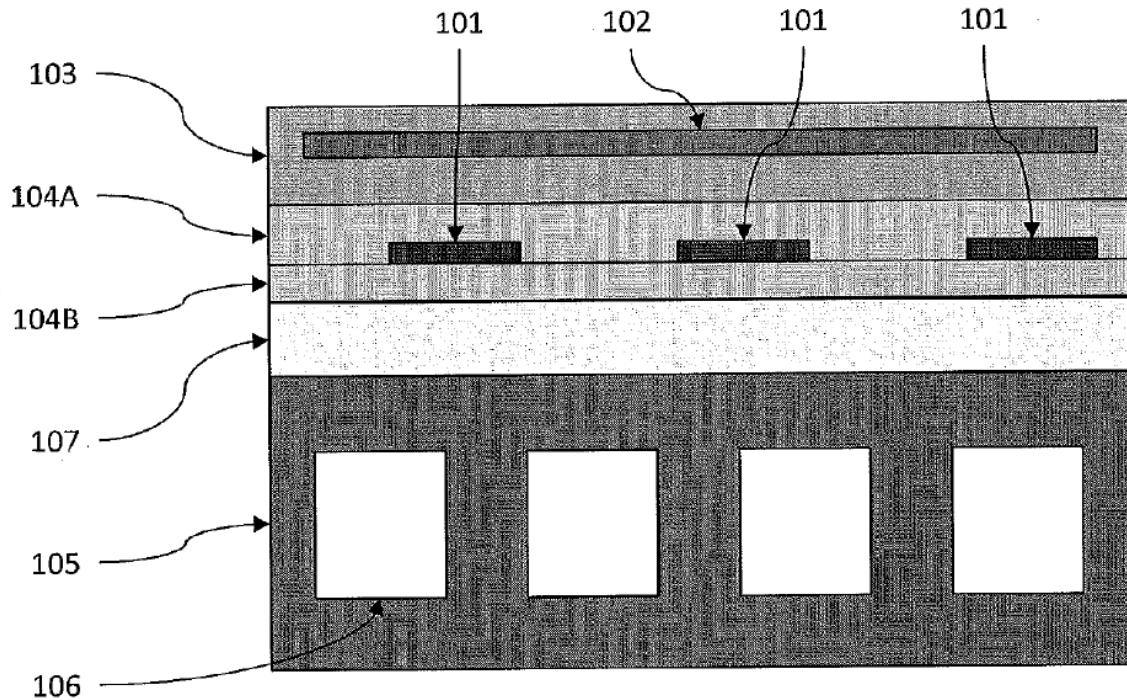


Figure 20: Cross-sectional substrate-support assembly, including the substrate, electrostatic chuck/clamping electrode, multiplexed heating plate, and temperature-controlled base plate.

- **101** — Array of planar heater zones incorporated between electrically insulating layers **104A** and **104B**
- **102** — Electrostatic-clamping electrode embedded in ceramic layer **103**
 - May be a monopolar or bipolar electrode
 - Uses a DC voltage to electrostatically clamp the substrate
- **103** — Ceramic electrostatic-clamping layer forming part of the electrostatic chuck
- **104A** — First electrically insulating layer surrounding the planar heater zones **101**
- **104B** — Second electrically insulating layer surrounding the planar heater zones **101**

- Layers **104A** and **104B** may comprise a polymer, an inorganic material, silicon oxide, alumina, yttria, aluminum nitride, or another suitable electrically insulating material
- **105** — Cooling plate
- **106** — Coolant-flow channels contained within cooling plate **105**
- **107** — Thermal-barrier layer positioned between the heated and cooled portions of the substrate-support assembly

Functional Arrangement

The planar heater zones **101** are positioned between insulating layers **104A** and **104B** to provide localized substrate heating. Above the heater array, electrode **102** is embedded in ceramic layer **103** to electrostatically clamp the substrate. Below the heater array, thermal-barrier layer **107** controls heat transfer to cooling plate **105**, while coolant flowing through channels **106** provides bulk cooling or temperature regulation.

Fig. 2

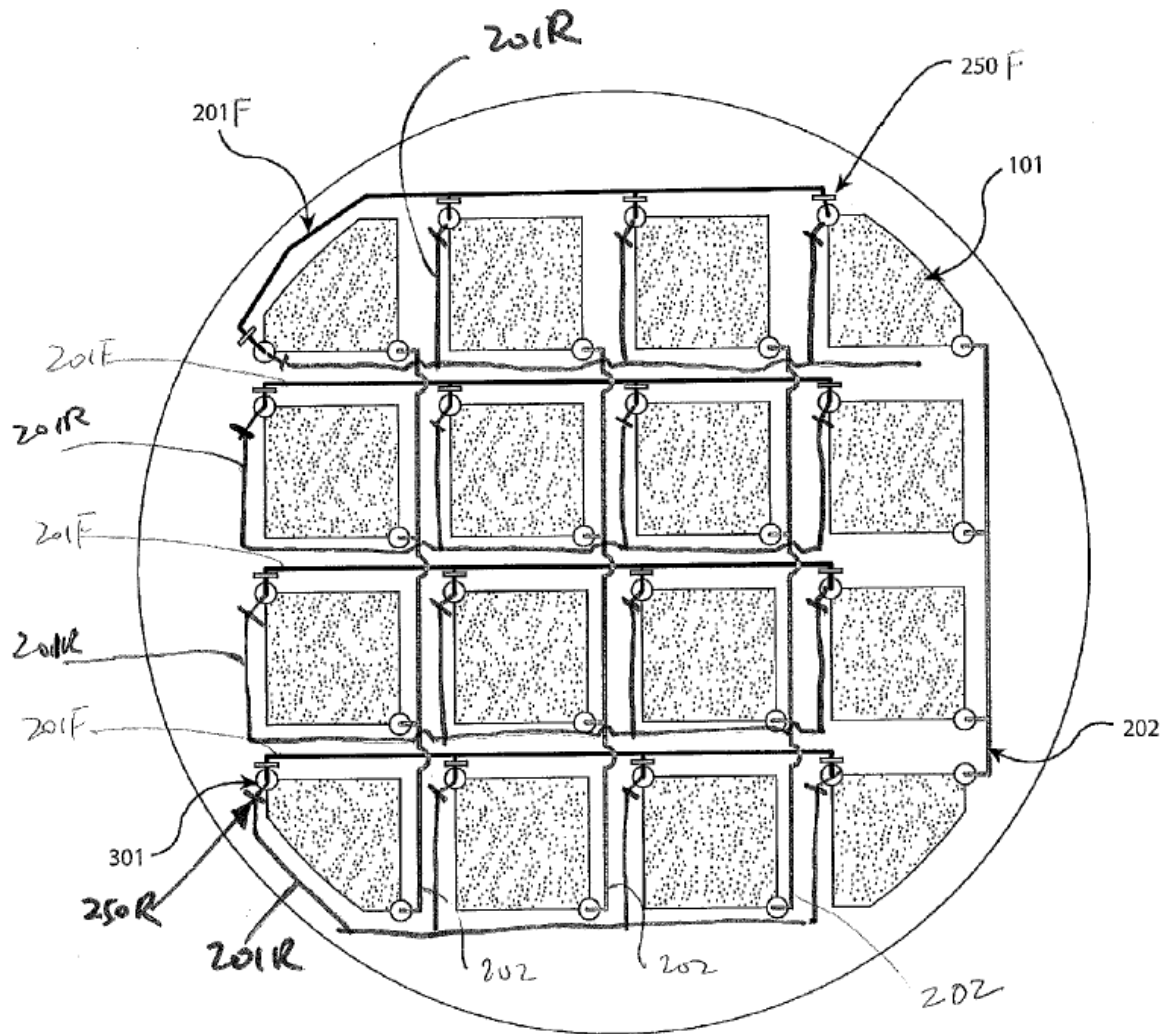


Figure 21: Laterally distributed array of independently controllable planar heater zones across the heating plate.

- **101** — Independently controllable planar heater zone
 - Each heater zone can be selectively energized.
 - Its time-averaged heating power can be individually adjusted using time-domain multiplexing.
- **201F** — Forward branch transmission line

- Connects a planar heater zone **101** to the multiplexed power-delivery network.
 - A selected pairing of forward branch line **201F** and common line **202** energizes only the heater zone associated with that pair.
- **201R** — Reverse branch transmission line corresponding to forward branch transmission line **201F**
 - Provides the reverse-current connection for planar heater zone **101**.
 - A selected pairing of reverse branch line **201R** and common line **202** energizes only the associated heater zone.
- **202** — Common transmission line
 - Used with a selected forward branch line **201F** or reverse branch line **201R** to address an individual heater zone **101**.
 - No two heater zones share the same branch-line/common-line pairing.
- **250F** — Forward diode
 - Connected in series between planar heater zone **101** and forward branch transmission line **201F**.
 - Prevents current from flowing from heater zone **101** toward forward branch line **201F**.
- **250R** — Reverse diode
 - Connected in series between planar heater zone **101** and reverse branch transmission line **201R**.
 - Prevents current from flowing from reverse branch line **201R** toward heater zone **101**.

Functional arrangement

- A switching arrangement connects a selected **201F–202** or **201R–202** line pair to a power supply, turning on only the corresponding heater zone **101**.
- The zones are individually regulated by **time-domain multiplexing**, which controls their time-averaged heating power.
- The heater zones **101**, transmission lines **201F**, **201R**, and **202**, and diodes **250F** and **250R** may occupy different electrically insulated planes within the heating plate.
- **Vertically extending vias** provide electrical connections between those planes.
- The heater zones are preferably positioned closest to the upper surface of the substrate-support assembly.

Fig.3

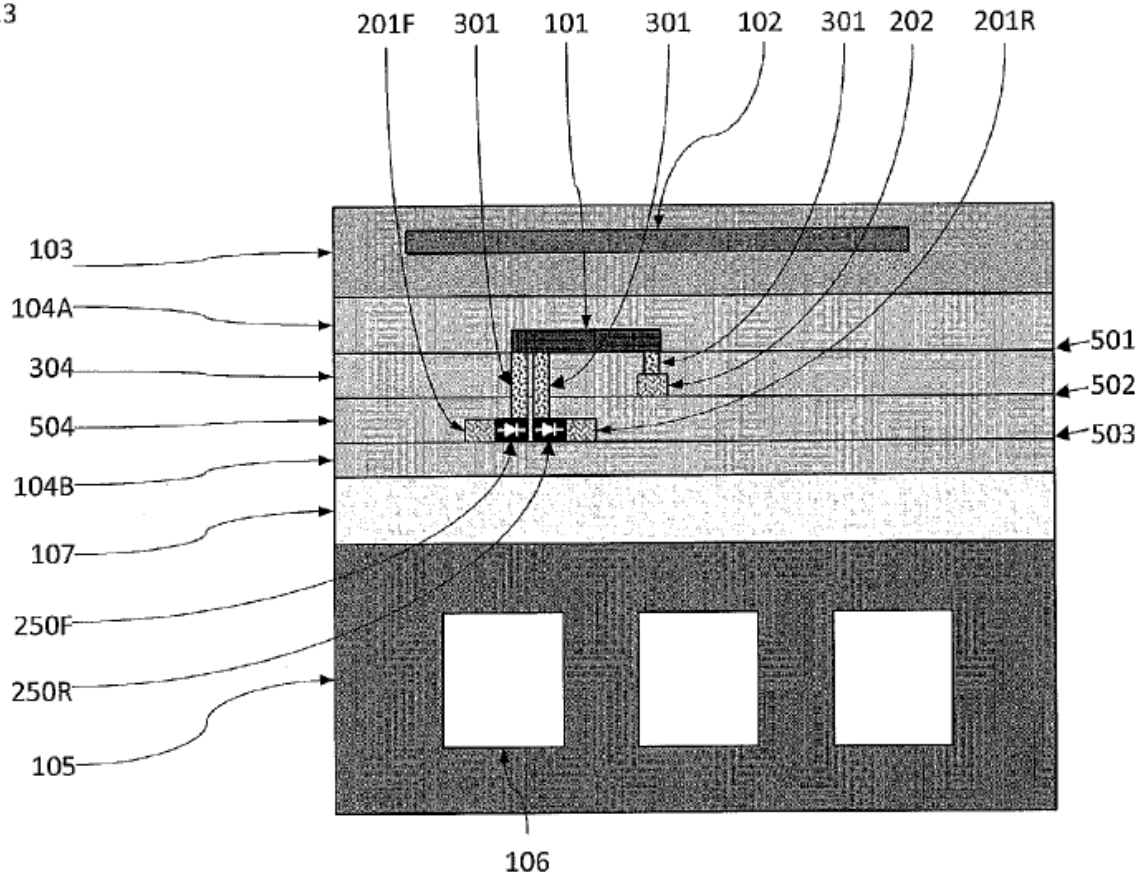


Figure 22: Planar heater zones connected through branch transmission lines, common transmission lines, switching components/diodes, and shared electrical conductors.

- **101** — Planar heater zone
 - Only one heater zone is shown in the cross-sectional view.
 - Located in first plane **501**.
- **201F** — Forward branch transmission line
 - Located in third plane **503**.
 - Connected to planar heater zone **101** through forward diode **250F** and via **301**.
- **201R** — Reverse branch transmission line
 - Located in third plane **503**.

- Connected to planar heater zone **101** through reverse diode **250R** and via **301**.
- **202** — Common transmission line
 - Located in second plane **502**.
 - Connected to planar heater zone **101** through via **301**.
- **250F** — Forward diode
 - Located in third plane **503** between forward branch transmission line **201F** and heater zone **101**.
 - Prevents current from flowing from planar heater zone **101** toward forward branch transmission line **201F**.
- **250R** — Reverse diode
 - Located in third plane **503** between reverse branch transmission line **201R** and heater zone **101**.
 - Prevents current from flowing from reverse branch transmission line **201R** toward planar heater zone **101**.
- **301** — Electrically conductive via
 - Provides vertical electrical connections between components located in different planes.
 - Connects the branch transmission lines **201F** and **201R**, and common transmission line **202**, to planar heater zone **101**.
- **304** — Electrically insulating layer
 - Separates adjacent electrical planes within the multilayer heating plate.
- **501** — First plane
 - Contains planar heater zones **101**.
- **502** — Second plane
 - Contains common transmission lines **202**.
- **503** — Third plane
 - Contains forward branch transmission lines **201F**, reverse branch transmission lines **201R**, and diodes **250F** and **250R**.
- **504** — Electrically insulating layer
 - Cooperates with insulating layer **304** to separate first plane **501**, second plane **502**, and third plane **503** electrically.

Functional Arrangement

The heater zone **101**, common line **202**, and branch lines **201F/201R** are distributed among three electrically isolated planes **501–503**. Conductive vias **301** connect the components vertically through insulating layers **504** and **304**. Diodes

250F and 250R control current direction, enabling selective bidirectional energization of the heater zone while preventing unintended reverse-current paths.
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U.S. Pat. Pub. No. 2004/0227536 – (Sugiyama)

116. Sugiyama et al. (US 2004/0227536 A1) describe a prober and probe-testing method for electrically testing multiple objects, such as semiconductor devices arranged on a wafer-like substrate, while controlling their temperature.

117. The prober includes a chamber, stage base, vertically movable Z stage, frame-type X–Y stage, substrate-fixing mechanism, probe card, and a probing stage positioned so that its axis is aligned with the probe center of the probe card.

118. The probing stage supports the substrate from below and includes an elevating mechanism that brings the objects under test into electrical contact with the probe card while maintaining the desired testing position.

119. Localized temperature control is provided by dividing the substrate-supporting region into cells or zones associated with one object or a selected group of objects under test. Each cell can include a heater or heat exchanger and a local temperature sensor.

120. A controller receives temperature information from the sensors and independently regulates heating or cooling in the respective cells, permitting different regions of the wafer to be maintained near selected temperatures during probe testing.

121. The substrate may be secured by vacuum during testing, and the localized thermal components may be separated by partitions or thermal-isolation structure to reduce heat transfer between adjacent cells.

122. Sugiyama shows combining accurate probe alignment and vertical probing motion with cell-based thermal control, thereby addressing temperature differences among devices and reducing unnecessary heating or cooling of the wafer as a whole.

123. The design is intended to improve temperature uniformity, test accuracy, and throughput by allowing independently controlled thermal zones to correspond to one die, multiple dice, or subdivisions of a die, and by permitting staged thermal preconditioning during wafer-level testing.

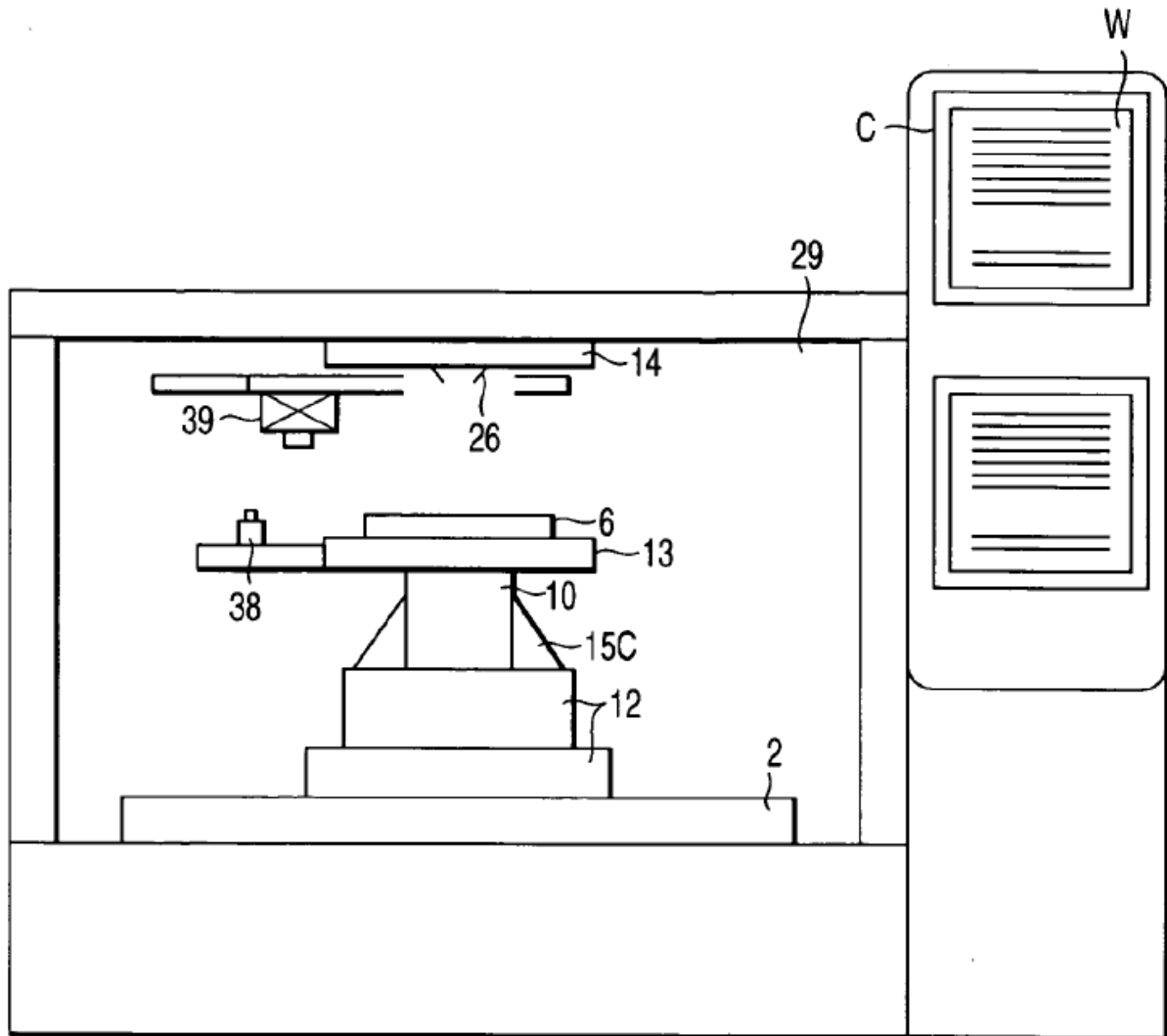


FIG. 1

Figure 23: Prober chamber, stage base, Z stage, frame-type X-Y stage, substrate-fixing mechanism, probe card, and probing stage.

- **100** — Prober according to the first embodiment
- **29** — Prober chamber housing the principal probing components
- **2** — Stage base arranged in the lower portion of prober chamber **29**
- **12** — X-Y stage
 - Moves in the X and Y directions

- May use separate X- and Y-motion structures or a single structure capable of movement in both directions
- **10** — Z stage that provides positioning in the vertical direction
- **6** — Main chuck
 - Supports the object to be tested
 - Positioned below and opposite probe card **14**
- **14** — Probe card arranged in the upper portion of prober chamber **29**
- **26** — Plurality of probes carried by probe card **14**
 - Used to test the electrical characteristics of the object placed on main chuck **6**

Functional Relationships

- Stage base **2** supports X–Y stage **12**, Z stage **10**, and main chuck **6**, which are arranged in the vertical or Z direction within prober chamber **29**.
- X–Y stage **12** positions the object laterally in the X and Y directions relative to probes **26**.
- Z stage **10** controls vertical positioning so the object supported on main chuck **6** can be brought into contact with probes **26**.
- Probe card **14** is positioned opposite main chuck **6**, aligning its probes **26** with the object under test.
- Probes **26** establish electrical contact with the object on main chuck **6**, enabling measurement of its electrical characteristics.



Figure 24: The probing stage is positioned within the X–Y stage, supports the wafer from below, and moves vertically to establish probe contact.

- **100** — Prober according to the second embodiment
- **9** — Heater cell structures provided in the main chuck
 - Each cell structure may contain a heater, temperature sensor, and heat exchanger
 - The cells permit localized and separate temperature control
- **18** — Heaters associated with the respective cell structures **9**
- **19** — Temperature sensors associated with the respective cell structures **9**
 - Detect the temperature of each cell
 - Supply temperature-detection results to temperature controller **27**
- **20** — Heat exchangers associated with the respective cell structures **9**
 - Provide localized heat removal or cooling

- **15** – Z-guide
- **18** — Heaters associated with the respective cell structures **9**
- **19** – Temperature Sensors
- **20** — Heat exchangers associated with the respective cell structures **9**
 - Provide localized heat removal or cooling
- **24** — Probing-stage elevating mechanism
- **24a** — Motor located in the Z stage
- **24b** — Ball-screw member fixed to and rotated by motor **24a**
- **24c** — Nut member fixed to probing stage **3** and threadedly engaged with ball screw **24b**
- **26** - Probes
- **27** — Temperature controller connected to heaters **18**, temperature sensors **19**, and heat exchangers **20**
- **31** – Z-Stage Elevating Mechanism

Functional relationship: Motor **24a** rotates ball screw **24b**. Because ball screw **24b** engages nut **24c**, which is fixed to probing stage **3**, that rotation moves probing stage **3** vertically.

U.S. Pat. Pub. No. 2016/0111315 – (Parkhe)

124. Parkhe (US 2016/0111315 A1) describes an electrostatic chuck assembly for supporting and electrostatically securing a semiconductor substrate during high-temperature processes such as physical vapor deposition, etching, and chemical vapor deposition.

125. The assembly includes a puck coupled to a cooling plate. The puck has an electrically insulative upper puck plate containing one or more heating elements and one or more electrostatic-clamping electrodes, together with a lower puck plate bonded to the upper puck plate by a metal bond.

126. The upper puck plate can generate heat and an electrostatic clamping field near the wafer-support surface, while the cooling plate removes heat from the puck to regulate the assembly over a wide operating-temperature range.

127. The lower puck plate includes multiple distributed fastening features located at different radial distances from its center. Fasteners engaging these features couple the cooling plate to the puck and apply approximately equal fastening forces across the interface.

128. A controlled thermal interface is formed between the puck and cooling plate. The interface may include a thermal-interface material, and its thermal conductance can be selected or spatially varied to manage radial or zonal heat transfer.

129. Different portions of the chuck can operate as thermal zones, with heating elements, cooling, interface conductance, and thermal-isolation features cooperating to reduce unwanted heat flow between regions and to improve substrate-temperature uniformity.

130. Parkhe advances the state of the art by addressing the large temperature gradients and differential thermal expansion that occur in high-temperature electrostatic chucks, where a heated ceramic puck is mechanically joined to a cooler metal cooling plate.

131. The design combines high-temperature electrostatic clamping, embedded heating, controlled cooling, distributed approximately equal fastening forces, compliant or tailored thermal interfaces, and a lift or loading structure to improve thermal contact, mechanical reliability, wafer handling, and repeatable temperature control.

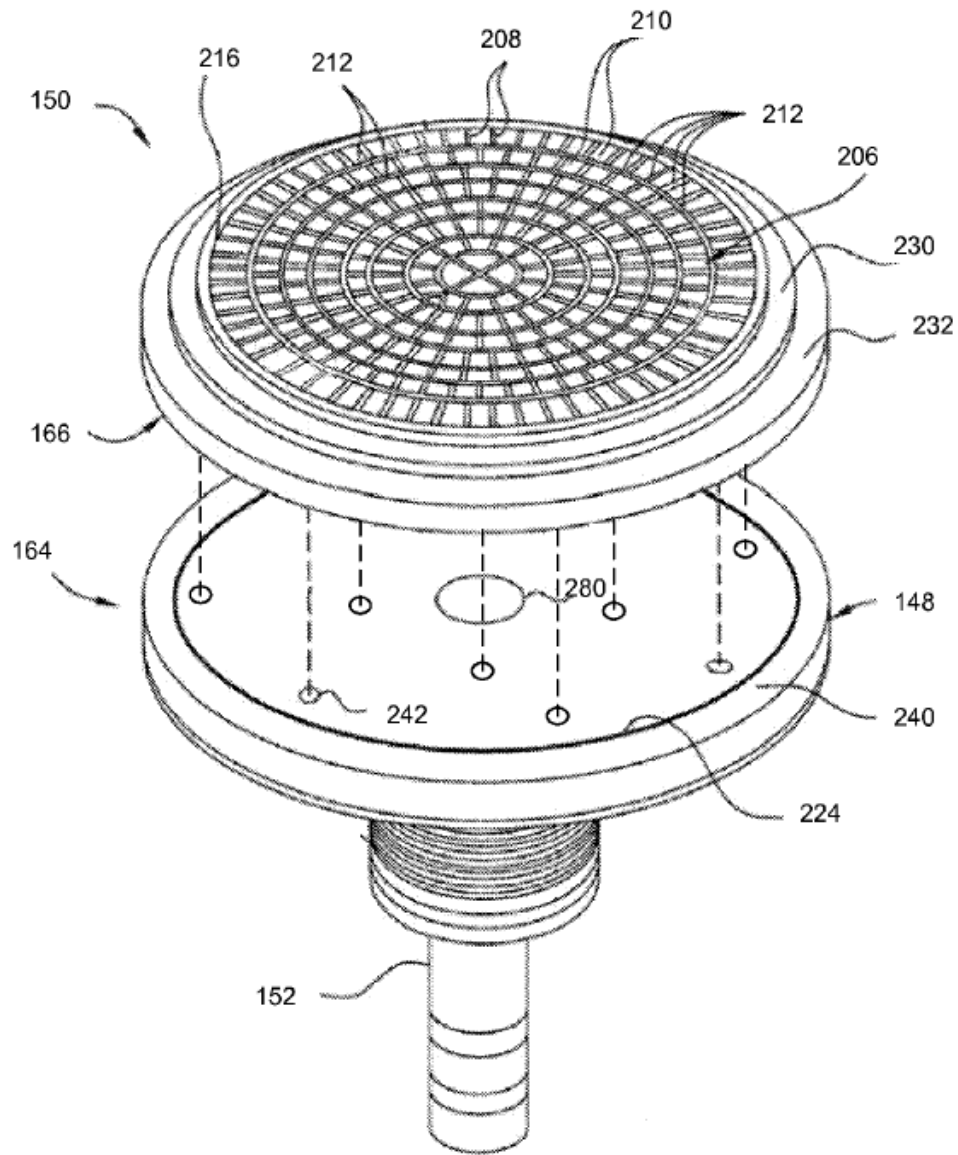


FIG. 2

Figure 26: Layered relationship among the substrate, upper puck plate, embedded heating and chucking components, lower puck plate, thermal interface, cooling plate, and fastening structure.

- **148** — Cooling plate assembly
- **150** — Electrostatic chuck assembly

- **152** — Support shaft or stem coupled to the cooling plate
- **164** — Lower surface of the puck
- **166** — Puck
- **206** — Lower puck plate
- **208** — Distributed fastening features formed in the lower puck plate
- **210** — Concentric annular ribs or raised contact regions
- **212** — Radial ribs or raised contact regions intersecting the annular ribs
- **216** — Metal bond joining the upper and lower puck plates
- **224** — Alignment or indexing feature at the cooling-plate perimeter
- **230** — Upper puck plate
- **232** — Outer peripheral surface of the puck
- **240** — Upper surface of the cooling plate
- **242** — Fastener-receiving openings in the cooling plate
- **280** — Central opening or passage through the cooling plate

Functional Relationships

- Upper puck plate **230** and lower puck plate **206** form puck **166** and are joined by metal bond **216**.
- Annular and radial raised regions **210** and **212** define distributed puck-to-cooling-plate contact regions and intervening interface spaces.
- Fastening features **208** align with fastener-receiving openings **242** so puck **166** can be secured to cooling plate **148** at multiple radial and circumferential locations.
- The distributed fastening arrangement applies the clamping load across the puck-to-cooling-plate interface rather than concentrating it at only the perimeter.
- Cooling plate upper surface **240** faces puck lower surface **164**, forming the controlled thermal interface.
- Support shaft **152** supports the cooling plate and provides a route for electrical, thermal-control, or fluid connections.
- Central passage **280** provides access through the cooling plate for an associated central connection or assembly feature.

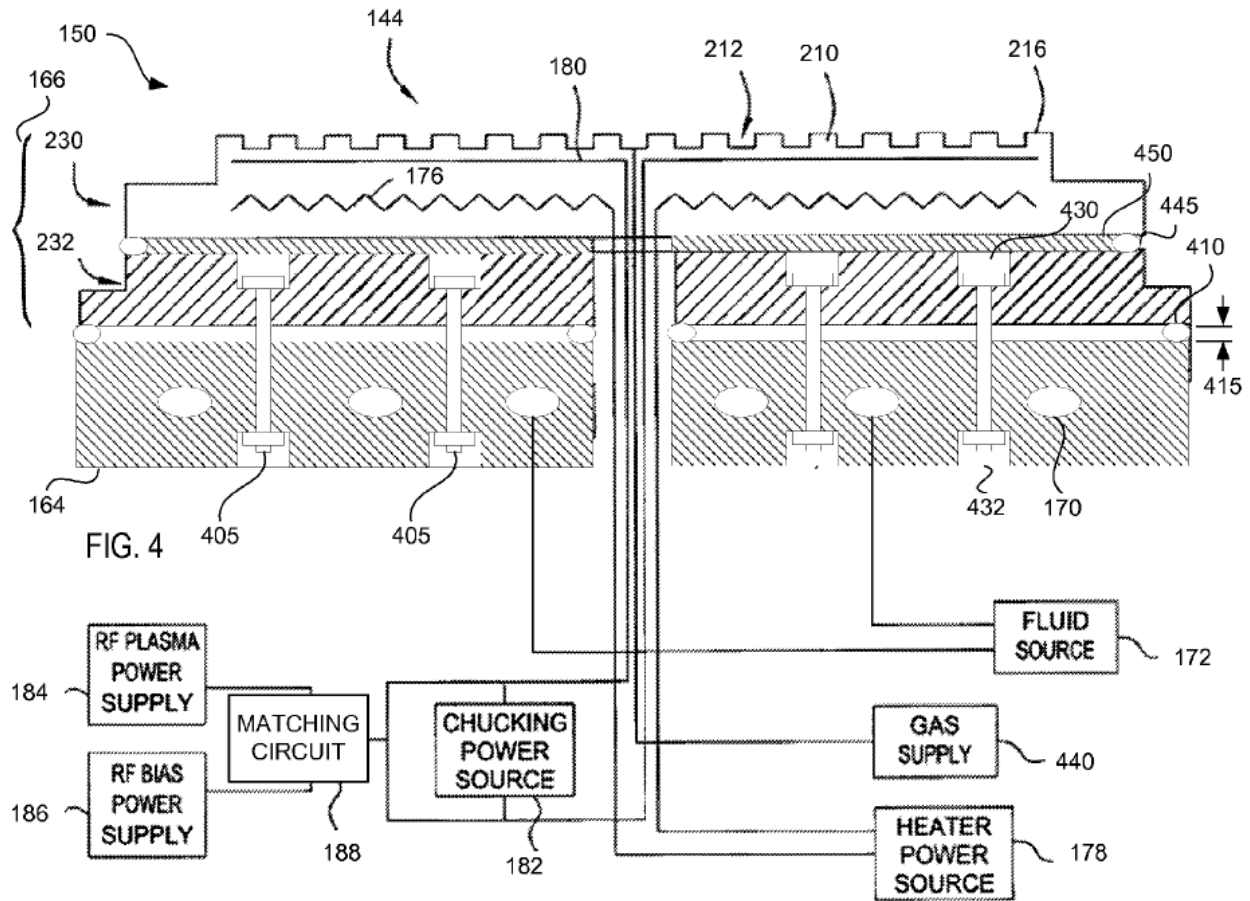


Figure 27: Puck, cooling plate, fasteners, and sealing or compliant interface components work together when the assembly is coupled.

- **144 — Substrate**, such as a semiconductor wafer, supported on the electrostatic chuck
- **150 — Electrostatic chuck assembly**
- **164 — Cooling plate** positioned beneath the puck
- **166 — Puck**, including the upper and lower puck plates
- **170 — Coolant channels** formed in cooling plate 164
- **172 — Fluid source** that circulates temperature-controlled fluid through coolant channels 170
- **176 — Heating element** embedded in the puck
- **178 — Heater power source** connected to heating element 176
- **180 — Electrostatic-clamping electrode** embedded in the puck
- **182 — Chucking power source** connected to electrode 180

- **184 — RF plasma power supply**
- **186 — RF bias power supply**
- **188 — Matching circuit** coupling RF power supplies **184** and **186** to the chuck assembly
- **210 — Raised substrate-support features or mesas** on the upper surface of the puck
- **212 — Gas-distribution grooves or channels** between the raised support features
- **216 — Backside-gas opening or port** communicating with the substrate-support surface
- **230 — Upper puck plate**
- **232 — Lower puck plate**
- **405 — Fastening members** coupling puck **166** to cooling plate **164**
- **410 — Outer sealing member**, such as an O-ring, at the puck-to-cooling-plate interface
- **415 — Controlled interface gap or spacing** between puck **166** and cooling plate **164**
- **430 — Thermal-interface layer or gasket** positioned between the puck and cooling plate
- **432 — Fastener head or retaining portion** engaging cooling plate **164**
- **440 — Gas supply** providing backside heat-transfer gas
- **445 — Inner sealing member**, such as an O-ring
- **450 — Upper interface or sealing layer** beneath the puck

Functional Relationships

- Substrate **144** rests on raised features **210**, while gas supplied by gas source **440** flows through port **216** and channels **212** to improve heat transfer between the substrate and puck.
- Chucking power source **182** energizes electrode **180**, electrostatically securing substrate **144** to puck **166**.
- Heater power source **178** energizes heating element **176** to heat the puck and substrate.
- Fluid source **172** circulates coolant through channels **170** in cooling plate **164**, removing heat from the puck.
- Fasteners **405**, including retaining portions **432**, couple puck **166** to cooling plate **164** while allowing the fastening load to be distributed across the assembly.
- Thermal-interface layer **430** bridges the controlled gap **415** and promotes heat transfer between puck **166** and cooling plate **164**.

- Sealing members **410** and **445** confine the interface or backside gas and prevent leakage.
- RF plasma power supply **184** and RF bias power supply **186** operate through matching circuit **188** to provide RF energy for plasma processing and substrate biasing.

XIII. SUMMARY OF CLAIM ELEMENTS AND PRIOR-ART RELIANCE

132. Appended below is a summary of the grounds under which 841-Patent has been assessed with respect to the prior art.

Ground	Claim(s) / claim element	Prior-art reference(s) relied on	Reliance for Specific Elements
Ground 1 DiBattista + Herchen-1 + Herchen-2 + Pease	Claim 1—wafer-test architecture; die-mapped, independently controlled heating zones; cold plate; thermal controller	DiBattista; Herchen-1; Pease	DiBattista supplies the wafer-test architecture, independently controlled heater traces/elements mapped to device positions, fluid-cooled chuck, and heating/cooling control. Herchen-1 supplies etched resistive traces arranged in independently controlled zones and cooling-plate structure. Pease supplies scalable die-sized planar heater zones, thin-film/etched-foil heaters, PWM control, cooling plate, and lift pins.
	Claim 5—first and second TIM layers comprise indium foil	Herchen-1; knowledge of a POSITA	Herchen-1 discloses a thermal-interface pad; indium foil is relied on as a known compliant TIM and

Ground	Claim(s) / claim element	Prior-art reference(s) relied on	Reliance for Specific Elements
			an obvious material choice.
	Claim 6—first and second TIM layers comprise graphite	Herchen-1; Herchen-2; knowledge of a POSITA	Herchen-1 discloses the thermal-interface pad; graphite is relied on as a known compliant TIM, with additional support cited to Herchen-2.
	Claim 8—two blow-off valves and common air source	Herchen-1; knowledge of a POSITA	Herchen-1 supplies regulated vacuum lines at both interfaces and release/separation functionality; positive-pressure blow-off is asserted to be a conventional complement.
	Claim 14—grounded shield layer protecting against PWM-generated EMI	Herchen-1; knowledge of a POSITA	Herchen-1 supplies the multilayer heater stack and insulating layers; adding a grounded shield is asserted to have been obvious for EMI protection.
	Claims 20, 21, 25, and 26—staged preconditioning of a next zone or set of zones during testing	DiBattista; knowledge of a POSITA	DiBattista supplies independent zone control, high-speed testing, and system-controller execution; programming staged preconditioning is asserted to have been obvious for testing expediency.
	Claim 22—TIM layer between cold plate and wafer TI layer comprising indium foil or graphite	Herchen-1; Herchen-2; knowledge of a POSITA	Herchen-1 supplies thermal material between the heater-bearing member and cooling plate; indium or graphite is supplied by known TIM choices, with

Ground	Claim(s) / claim element	Prior-art reference(s) relied on	Reliance for Specific Elements
			additional Herchen-2 support.
	Claim 27—resistive traces selectively energized during testing	DiBattista; Herchen-1	DiBattista supplies heater traces selectively powered under feedback control during testing; Herchen-1 confirms etched heater elements arranged in individually controlled zones.
Ground 2 DiBattista + Costello + knowledge of a POSITA	Claim 1—per-device thermal control, fluid-cooled chuck, rigid dual-sided thermal management, sensors, and control	DiBattista; Costello	DiBattista supplies per-DUT heaters and feedback control on a fluid-cooled chuck. Costello supplies rigid chuck construction, top/bottom thermal control, sensor arrays, hotspot-control strategies, and noise/leakage mitigation.
	Claim 4—TIM layers at both cold-plate/wafer-TI and wafer-TI/wafer interfaces	DiBattista; Costello; knowledge of a POSITA	Costello is relied on for conductive-layer and thermal/planarity teachings; adding TIM layers at both interfaces is asserted to improve heat transfer and mechanical conformity.
	Claims 5 and 6—TIM layers comprise indium foil or graphite	DiBattista; knowledge of a POSITA	Indium foil and graphite are relied on as known compliant TIMs and obvious choices among a limited number of materials.
	Claim 8—two blow-off valves and common air source	DiBattista; Costello; knowledge of a POSITA	Costello's vacuum-related disclosure is combined with the asserted conventional use of positive-pressure

Ground	Claim(s) / claim element	Prior-art reference(s) relied on	Reliance for Specific Elements
			blow-off for release.
	Claim 11—multiple thermal zones corresponding to each die	DiBattista; Costello	DiBattista supplies per-die independently controlled heater arrays; Costello supplies layered thermal paths and localized sensing/control, relied on for finer-granularity control within a die location.
	Claim 12—pin-lift mechanism and aligned pass-through channels	DiBattista; Costello; knowledge of a POSITA	Costello is cited for loading structure; loading pins are asserted to have been a known and common wafer load/unload mechanism.
	Claim 13—power supply controlled by PWM signals for selective heating	DiBattista; Costello; knowledge of a POSITA	The references supply heater power paths, thermal feedback, and independently controlled heating regions; PWM is relied on as a routine way to modulate average heater power per zone.
	Claim 14—grounded shield layer for PWM-related EMI	DiBattista; Costello	Costello is cited for electrical-noise, conductive-layer, and related chuck teachings, combined with the Ground 1 discussion.
	Claims 20, 21, 25, and 26—staged preconditioning during testing	DiBattista; knowledge of a POSITA	DiBattista supplies independent heater control and high-speed testing; staged preconditioning of a next zone or set is asserted to have been obvious.
	Claim 22—TIM layer comprising	Same reliance as Ground 2	The highlighted text incorporates the indium-foil

Ground	Claim(s) / claim element	Prior-art reference(s) relied on	Reliance for Specific Elements
	indium foil or graphite	claims 5 and 6	and graphite TIM analysis for claims 5 and 6.
Ground 3 Sugiyama + Parkhe + knowledge of a POSITA	Claim 1—localized wafer-test zones, sensors, heaters/heat exchangers, controller, and cooled high-temperature chuck architecture	Sugiyama; Parkhe	Sugiyama supplies localized cell-based wafer-test heating/cooling with sensors and a controller. Parkhe supplies the high-temperature ESC puck, heating elements, cooling plate, controlled thermal interface, zones, and thermal isolation.
	Claim 3—chiller and controller-operated coolant-flow valve	Sugiyama; Parkhe; knowledge of a POSITA	Sugiyama and Parkhe supply controlled liquid cooling; flow-control valves are asserted to be obvious for differential coolant regulation.
	Claim 4—TIM layers at both interfaces	Sugiyama; Parkhe; knowledge of a POSITA	Parkhe supplies thermal-interface teachings; adding conductive TIM layers at the two junctions is asserted to improve wafer temperature control and thermal transitions.
	Claims 5, 6, and 22—TIM comprises indium foil or graphite	Parkhe; knowledge of a POSITA	Indium foil and graphite are relied on as known compliant TIM choices; Parkhe is cited for the underlying interface structure.
	Claim 8—two blow-off valves and common air source	Sugiyama	Sugiyama supplies vacuum-secured wafer structure; vacuum release and associated valving are

Ground	Claim(s) / claim element	Prior-art reference(s) relied on	Reliance for Specific Elements
			asserted to be obvious.
	Claims 9 and 17— one thermal zone per die	Sugiyama; knowledge of a POSITA	Sugiyama supplies heaters/cells sized to an individual object under test, local sensors, heat exchange, and partitions; selecting one die per zone is asserted to be obvious.
	Claims 10 and 16— one thermal zone corresponding to multiple dice	Sugiyama; knowledge of a POSITA	Sugiyama supplies cells sized to a group of objects; expanding a zone to multiple dice is asserted to be an obvious throughput choice.
	Claims 11 and 18— multiple thermal zones per die	Sugiyama; knowledge of a POSITA	Sugiyama's cell-based architecture is relied on, with subdivision into multiple zones per die asserted to be an obvious option for finer control.
	Claim 12—pin-lift mechanism and aligned pass-through channels	Parkhe; knowledge of a POSITA	Parkhe is cited for lift/loading structure; use of loading pins is asserted to have been known and common in wafer handling.
	Claims 13 and 14— PWM heater control and grounded EMI shield	Sugiyama; Parkhe; knowledge of a POSITA	The references supply multi-zone resistive heaters, sensors, and closed-loop control; PWM is asserted to be a routine per-zone power-control method, and a grounded shield an obvious EMI-protection measure.
	Claims 20, 21, 25,	Sugiyama;	Sugiyama supplies

Ground	Claim(s) / claim element	Prior-art reference(s) relied on	Reliance for Specific Elements
	and 26—staged preconditioning during testing	knowledge of a POSITA	independently controlled heating elements and wafer-test sequencing; preconditioning the next zone or set during testing is asserted to have been obvious for expediency.

XIV. GROUND 1: Claims 1-27 are Rendered Obvious Over DiBattista in View of Herchen-1, Herchen-2, Pease, and Natsuhara

133. Claims 1-27 of the '841 Patent are unpatentable under 35 U.S.C. § 103 as obvious over DiBattista (U.S. Patent No. 6,549,026) in view of Herchen-1 (U.S. Patent Application Publication No. 2011/0000426), Herchen-2 (U.S. Patent Application Publication No. 2008/0160462) and Pease (U.S. Patent Application Publication No. 2013/0220989). These references are analogous prior art-being from the same field as the claimed invention, as being directed to the spatially resolved, zone-level temperature control of a wafer-scale substrate supported over a fluid-cooled plate, and their disclosures are complementary.

A. OVERVIEW OF GROUND 1

134. A comparison of the basic concept, thermal control structure, heating, and cooling approach is shown in Table 1.

Table 1: Comparison of DiBattista with 841-patent.

Aspect	US 6,549,026 B1 — DiBattista	US 12,320,841 B2 — Advantest
Basic concept	Multiple temperature-control devices arranged on or with the wafer chuck to correspond to individual IC devices	A wafer-scale active thermal-interposer layer containing patterned resistive traces that form independently heated zones
Thermal-control structure	Broadly describes localized heaters or heat sinks associated with respective devices	Requires a more specific stack: wafer probe, backside thermal interposer, cold plate, thermal controller, and test computer
Heating approach	A separate heater may be associated with each die or device location	Resistive traces traverse the interposer and selectively heat defined wafer zones
Cooling approach	The chuck may be heated or cooled using temperature-controlled fluid; separate local heat sinks are also disclosed	A cold plate adjacent to the interposer provides wafer cooling while the interposer supplies localized heating

135. To the extent the Patent Owner contends that DiBattista’s array of trace-based heating elements does not, standing alone, satisfy the requirement of “a plurality of resistive traces traversing said wafer TI layer” arranged to selectively heat “a plurality of zones” corresponding to areas of the wafer, Herchen-1 expressly discloses that limitation. Herchen-1 discloses a heater layer in which a conducting layer 304 carries heater elements arranged in a predetermined pattern, etched onto

the conducting layer and arranged to form six independent heating zones, each individually controlled and each having a separate temperature sensor. Herchen-1 at [0051], [0054], FIG. 5. Herchen-1 further discloses a movable top cooling plate 220 and a fluid-channel bottom cooling plate 230 positioned below the heater-bearing planar members, together with lift-pin holes 210 extending through the plate stack. Herchen-1 at [0048]-[0050].

136. DiBattista discloses the wafer-test architecture recited in claim 1, including an array 129 of independently controlled resistive heating elements 149 disposed on a fluid-cooled chuck in correspondence with the integrated-circuit devices under test, each element implemented with a “heater trace” that “provides the heat energy,” each “controlled independently of the others,” and a temperature control system 140 that maintains each device at a set-point temperature. DiBattista at 6:7-16, 6:21-37, 6:38-42, 7:59-8:2. Pease supplies the added features of the dependent claims addressed in this Ground. Pease discloses “multiple independently controllable planar heater zones in the substrate support assembly to enable the apparatus to actively create and maintain the desired spatial and temporal temperature profile,” Pease at [0014], in which each zone is “of similar size to or smaller than a single device die or group of device dies on the substrate so that the substrate temperature . . . can be controlled for each device die position to maximize

the yield of devices from the substrate.” Pease at [0030]. Pease’s “scalable architecture” accommodates “die-by-die substrate temperature control (typically more than 100 dies on a substrate of 300-mm diameter),” Pease at [0030], with a heating plate that “can have at least 10, at least 100 and up to 1000 heater zones.” Pease at [0049]. The heater elements “may be thin film resistive heaters” and “may be screen printed, wire wound or etched foil heaters.” Pease at [0017]. Pease further discloses a controller 1000 that includes “logic (hardware or software) to control at least one power supply,” Pease at [0041], digital power control in which “control is then effected by time division multiplexing and Pulse Width Modulation (PWM) techniques,” Pease at [0050], “a cooling plate 105 containing channels 106 for coolant flow,” Pease at [0018], and “lift pins for lifting the substrate.” Pease at [0030].

137. The DiBattista and Pease Patents address the same problem—spatially resolved, zone-level heating of a wafer-scale substrate supported over a fluid-cooled plate—and their teachings are complementary. Implementing DiBattista’s per-die wafer-test heater array with Pease’s scalable, multiplexed array of independently controllable planar heater zones sized to the device dies, together with Pease’s PWM power control and lift-pin arrangement, amounts to no more than combining prior-art elements according to known methods, and applying a known technique to a

known device ready for improvement, to yield the predictable result of finer zone-selective heating mapped to the die layout. From a thermal-engineering perspective, DiBattista establishes the need to counteract unequal self-heating among devices being tested simultaneously by independently adding heat at corresponding device locations, while the fluid-cooled chuck removes heat globally. Pease provides a implementation that increases the spatial resolution and scalability of that same control strategy: small planar heater zones can be selectively energized and their time-averaged power adjusted so that local heat input offsets die-to-die power differences and transient thermal disturbances without requiring the entire wafer or chuck to change temperature. A POSITA would have understood that this combination preserves a stable bulk thermal boundary condition at the cooled plate while superimposing controlled local heat flux at selected die positions, thereby reducing lateral temperature gradients, thermal cross-talk, and temperature lag as testing proceeds across the wafer. Pease's multiplexed addressing also permits many die-scale zones to be controlled with fewer external conductors, making DiBattista's individualized temperature regulation practical for wafers having large die counts without materially increasing the thermal mass of the heater layer. Because both systems rely on resistive heating, temperature feedback, and a cooled support structure, the thermal interfaces, control variables, and expected heat-flow paths are

compatible; any implementation would involve routine selection of zone dimensions, heater power, duty cycle, and controller timing based on the wafer's thermal resistance and capacitance. The resulting system would predictably improve temperature uniformity at each active device, respond more rapidly to localized self-heating, and maintain repeatable test temperatures while neighboring zones are inactive or being preconditioned. A person of ordinary skill in the art, therefore, would have had a reasonable expectation of success in combining DiBattista with Pease based on these established thermal-control principles.

138. A person of ordinary skill in the art would have been motivated to combine DiBattista and Herchen-1. Both references address the same problem - spatially controlled, zone-selective heating of a wafer-scale substrate using a patterned resistive heater layer over a liquid-cooled plate. Implementing DiBattista's per-die heater array with Herchen-1's etched, patterned resistive heater traces arranged in individually controlled zones traversing the heater layer amounts to no more than applying a known heater-trace construction to a known wafer-test chuck ready for improvement, combining prior-art elements according to known methods to yield the entirely predictable result of zone-selective heating mapped to the die layout. A skilled artisan would have had a reasonable expectation of success in doing so.

139. From a thermal-engineering perspective, DiBattista identifies the need to compensate for unequal device self-heating during simultaneous wafer-level testing while the fluid-cooled chuck establishes a common bulk-temperature boundary condition. Herchen-1 provides a compatible means of supplying that compensating heat through thin patterned resistive elements distributed in separately controlled zones, with an associated temperature sensor for each zone. A POSITA would have understood that positioning Herchen-1's zoned heater layer in DiBattista's chuck would permit the controller to add heat only where needed, thereby correcting local departures from the test set point without forcing the entire chuck and wafer to undergo a slower global temperature change. The combination would also reduce lateral temperature gradients and thermal cross-talk because the patterned traces concentrate heat generation near the selected die locations while the underlying cooling plate continuously removes excess heat and stabilizes the remainder of the wafer. Herchen-1's multilayer construction electrically isolates the conducting heater traces while maintaining a short thermal path to the substrate, and its compliant thermal material at the cooling interface improves conformity and reduces contact resistance caused by surface tolerances or differential thermal expansion. Vacuum retention of the heater layer between planar members would further promote repeatable thermal contact without a permanently bonded stack that

could bow or accumulate stress during repeated heating and cooling cycles. These features are thermally compatible with DiBattista's controlled chuck because both systems use resistive heat generation, local temperature sensing, and heat rejection to a liquid-cooled support; integration would require only routine selection of trace geometry, zone dimensions, heater power, sensor placement, and controller gains based on the wafer's thermal resistance and capacitance. The resulting assembly would predictably provide faster local response, improved temperature uniformity at active devices, reduced overshoot and lag during changes in device power, and more repeatable junction-temperature conditions during probing. A skilled artisan would therefore have had a reasonable expectation of success in combining DiBattista with Herchen-1 based on these established thermal-control principle.

140. Further, a person of ordinary skill in the art would have been motivated to combine DiBattista with Herchen-2. DiBattista addresses localized temperature differences produced by unequal device self-heating during simultaneous wafer-level testing and teaches independently controlled thermal elements associated with respective die locations on a fluid-cooled chuck. Herchen-2 addresses a complementary source of temperature nonuniformity: spatial variation in the thermal coupling between a wafer and its supporting plate caused by wafer bow, warpage, and nonuniform wafer-to-plate gaps. Herchen-2 uses distributed capacitive

measurements to determine those local gaps and independently controlled pressure chambers beneath a flexibly supported plate to adjust its local position or shape. From a thermal-engineering perspective, a POSITA would have understood that DiBattista's local heater control can accurately regulate heat generation only if the thermal resistance between each wafer region and the temperature-controlled support is sufficiently known and repeatable. An uncontrolled gap introduces an additional, spatially varying thermal resistance, causing nominally identical heater commands to produce different junction temperatures, heating rates, and steady-state errors at different die locations. Incorporating Herchen-2's distributed gap sensing and localized plate-shape adjustment into DiBattista's wafer-test chuck would reduce those variations by making the conductive and gap-mediated heat-transfer paths more uniform across the wafer. The resulting system would permit DiBattista's controller to distinguish temperature deviations caused by device power dissipation from deviations caused by poor local thermal contact, thereby improving the accuracy and stability of per-die temperature regulation. A POSITA also would have recognized that correcting wafer bow improves contact pressure and reduces local interfacial thermal resistance without requiring excessive global clamping force, which could otherwise distort the wafer or chuck and interfere with probe alignment. Herchen-2's chamber-specific actuation would allow local conformity to be adjusted

while the underlying chill plate continues to provide a stable heat sink, preserving DiBattista's global cooling function while enhancing the uniformity of heat removal from individual die regions. The combination would predictably reduce hot spots, lateral temperature gradients, thermal lag, and die-to-die differences in transient response, particularly during changes in device power or staged testing across the wafer. Because both references employ a wafer-support plate, active thermal control, sensing, and a cooled base, their thermal functions and control objectives are compatible; implementation would require only routine calibration of gap measurements, chamber pressures, heater power, and feedback gains to account for the wafer's thermal resistance and capacitance. Accordingly, combining DiBattista's independently controlled per-device heating with Herchen-2's measured and locally adjustable thermal interface would have yielded the predictable result of more uniform, repeatable, and responsive wafer-level temperature control, and a POSITA would have had a reasonable expectation of success in making the combination.

141. Herchen-2 teaches that gap non-uniformity arising from wafer bow degrades heating uniformity because local spacing changes the effective thermal resistance and heat-transfer coefficient between the wafer and the plate. Herchen-2 therefore proposes active plate-shape control through independently regulated chamber pressures informed by distributed capacitive measurements. Herchen-1, in

turn, teaches vacuum-retained multilayer heater assemblies that avoid the differential-thermal-expansion stresses and warpage associated with permanently bonded heater stacks while permitting heater replacement or reconfiguration and reducing cost of ownership. A POSITA would have recognized that integrating Herchen-1's vacuum-retained multilayer heater with Herchen-2's sensed, deformable, pressure-actuated bake plate addresses two coupled contributors to wafer-temperature nonuniformity: spatial variation in generated heat and spatial variation in the thermal path by which that heat reaches the wafer. The zoned heater could provide differential local heat flux, while the capacitive sensors and pressure chambers could reduce local gap variations so that commanded heater power produces a more consistent temperature response across the wafer. This combination would reduce variations in thermal contact resistance, heating rate, steady-state temperature, and time constant among wafer regions, thereby limiting hot spots, cold spots, lateral temperature gradients, overshoot, and thermal lag. The pressure-actuated plate could also maintain conformity without imposing excessive global clamping force, while vacuum retention of the heater stack would preserve repeatable interlayer contact and accommodate differential expansion during repeated heat-up and cool-down cycles. Because the heater layer, plate-shape actuator, gap sensors, and chill structure perform distinct but complementary

functions, integrating them would not require a change in their basic operating principles; it would require only routine calibration of heater-zone power, chamber pressure, sensed gap, and feedback gains based on the thermal resistance and capacitance of the assembled stack. A POSITA, therefore, would have expected the combined thermal module to provide more uniform and repeatable wafer temperatures, faster settling times following changes in set point or wafer loading, improved robustness to wafer bow and assembly tolerances, and easier maintenance through replacement of the vacuum-held heater layer.

142. Further, Herchen-2 contemplates heater elements embedded in or forming electrodes on a thin bake plate surface, and multi-zone heating is conventional in this context. Herchen-1 provides a known multilayer heater architecture with single- and multi-zone patterns that is designed to be sandwiched between planar members and held by vacuum. Substituting Herchen-1's multilayer, vacuum-held heater for the heater implementation in Herchen-2's bake plate is a like-for-like swap of heater technology in an established bake plate assembly to achieve predictable heating functionality with improved serviceability.

143. From a thermal perspective, the thin, distributed heater layer would shorten the conduction path between the resistive elements and the wafer-supporting surface, reducing thermal lag and allowing each zone to respond more rapidly to

changes in set point or localized heat loss. Vacuum retention would promote repeatable contact across the planar interfaces, reducing interfacial voids and spatial variations in contact resistance that otherwise could create hot spots, cold spots, or different thermal time constants among zones. The multilayer construction would also electrically isolate the heater traces while permitting the trace geometry and power density to be selected for the local thermal load. In combination with Herchen-2's distributed gap sensing and pressure-actuated plate-shape control, the zoned heater could compensate for residual differences in heat transfer caused by wafer bow, local spacing, edge losses, and process-dependent heat flux. The cooling structure would continue to establish a stable bulk-temperature boundary condition and remove excess heat, while the heater zones would superimpose controlled local heat input to correct smaller spatial and transient deviations. A POSITA would have understood that the resulting thermal behavior could be tuned through routine selection of zone size, trace resistance, heater duty cycle, sensor placement, interface pressure, and controller gains based on the assembled stack's thermal resistance and capacitance. Because the substituted heater performs the same basic function using established resistive-heating and feedback-control principles, the combination would predictably improve temperature uniformity, reduce overshoot and settling time, limit lateral thermal cross-talk, accommodate differential thermal expansion,

and preserve the ability to replace or reconfigure the heater layer without redesigning the surrounding bake-plate assembly.

B. DEPENDENT CLAIM 4: The system as described in claim 2 further comprising: a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and a second TIM layer disposed between said wafer TI layer and said wafer

144. Herchen-1 discloses a thermal interface material between the heater-bearing planar member and the cooling plate: cooling plate 220 “may include thermal material 221 disposed on its upper surface,” a “thermal pad” that “aid[s] in efficient removal of heat from the lower planar member.” Herchen-1 at [0049]. It would have been obvious to provide such a TIM layer both between the cold plate and the wafer TI layer and between the wafer TI layer and the wafer of the DiBattista-Herchen-1 system, as the mere duplication of a known thermal-interface layer to improve heat transfer at each interface yields a predictable result. From a thermal-engineering standpoint, a POSITA would have understood that each physical junction in the heat-transfer path—here, the cold-plate-to-wafer-TI-layer interface and the wafer-TI-layer-to-wafer interface—introduces a contact (interfacial) thermal resistance arising from microscopic surface roughness and the insulating air voids trapped between the mating surfaces, and that interposing a compliant, thermally conductive material at each junction conforms to those surfaces, displaces the trapped air, and lowers the interfacial resistance, thereby improving

conductive heat transfer across the stack. Herchen-1 confirms this very function, teaching not only that its thermal pad aids in the “efficient removal of heat from the lower planar member,” but also that maintaining intimate, uniform thermal contact across the interface is what allows heat to be “effectively and rapidly” removed so as to “reduce the time required to achieve a stable temperature.” Herchen-1 at [0049]. DiBattista reflects the same principle, teaching that the thermal performance of its wafer-test system depends on the thermal resistance of the medium in the heat-transfer path: its $K\theta$ term is expressly “derived from . . . the thermal resistance of the medium (or media . . .) between the electronic device and the heat exchanger,” such that reducing the resistance at each interface in that path directly improves the speed and accuracy with which each device is driven to and held at its set-point temperature. DiBattista at 9:46-10:10. A POSITA would therefore have recognized that placing a TIM at both the cold-plate/wafer-TI-layer interface and the wafer-TI-layer/wafer interface reduces the series thermal resistance of the overall stack, promotes more uniform temperature across the wafer, and yields faster, more accurate zone-level thermal control during testing. Because the two interfaces are thermally analogous and each benefits in the same way from reduced contact resistance, adding a compliant TIM at each is nothing more than the application of a known thermal technique to each interface of the combined system to improve it in the predictable

manner for which such materials are used, and a POSITA would have had a reasonable expectation of success in doing so.

C. DEPENDENT CLAIM 5: The system as described in claim 4 wherein said first and second TIM layers comprise indium foil.

145. Herchen-1 discloses a thermal-interface pad (Kapton® thermal material 221) at the cooling interface. Herchen-1 at [0049]. Indium foil is a well-known compliant thermal-interface material (TIM). See <https://indiumfoils.com/blog/what-is-the-use-of-indium-foil-2> (“Initially, indium was primarily utilized in the production of semiconductors and alloys. By the mid-20th century, its unique properties, such as excellent thermal and electrical conductivity, began to attract broader industrial interest”). Indium would have been an obvious choice among a limited number of known TIMs. For example, Cola (U.S. Pat. Pub. No. 2017/0347492), discloses carbon-nanotube-based thermal-interface materials placed between a heat source and a heat sink or heat spreader—including for use during ‘burn-in’ testing of electrical components such as chips—and teaches that the thermal-interface material’s inert metal support or foil may be formed from indium, among other metals. Cola at [0019], [0086].

D. DEPENDENT CLAIM 6: The system as described in claim 4 wherein said first and second TIM layers comprise graphite material

146. As with claim 5, Herchen-1 discloses a thermal-interface pad at the cooling interface, Herchen-1 at [0049]. Graphite is a well-known compliant TIM.

Graphite would have been an obvious choice among a limited number of known thermal-interface materials. *See also* Herchen-2 at [0042], [0044], [0052]. This is consistent with Cola, which identifies pyrolytic graphite as a state-of-the-art commercial thermal-interface material and evaluates its compressibility and rebound as a compliant TIM. Cola at [0167], [0171].

E. DEPENDENT CLAIM 20: The test system as described in claim 15 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone

147. DiBattista and Pease together disclose or render obvious the preconditioning sequence recited in dependent claim 20. DiBattista discloses an array of heating elements corresponding to respective integrated-circuit devices on the wafer, with each heating element “controlled independently of the others,” DiBattista at 6:38-42, and further teaches high-speed wafer testing in which the temperature of each device is “controlled independently of the other devices on the wafer during a test,” DiBattista at 12:26-31. DiBattista’s system controller 160 executes the temperature-control functions, DiBattista at 7:59-8:2. Thus, DiBattista

supplies the claimed test environment, the controller-operated plurality of discretely controllable thermal zones, the correspondence between a thermal zone and one or more die, and the ability to bring selected zones to and maintain them at a testing temperature independently while testing proceeds elsewhere on the wafer. Pease reinforces and supplies the spatial and temporal control capability. Pease discloses multiple independently controllable planar heater zones that actively create and maintain a desired “spatial and temporal temperature profile” across the substrate, Pease at [0014], with zones sized similarly to or smaller than a single die or group of dies so that temperature can be controlled at each die position, Pease at [0030]. Pease further teaches controller logic for controlling the heater power supply, Pease at [0041], and time-division multiplexing and pulse-width modulation to adjust the time-averaged power delivered to selected zones, Pease at [0050]. Those disclosures permit one selected zone to be held at the testing temperature while a different, independently addressable zone is energized and brought to that temperature before the tester reaches the corresponding die. In the claimed sequence, DiBattista’s controller would first bring the zone corresponding to the die under test to the prescribed testing temperature and maintain that zone during electrical testing. Because the remaining heater zones are independently controllable, the controller can simultaneously command the zone corresponding to the next die to begin

heating. Pease's spatial-and-temporal power control provides the control mechanism for assigning power to that second zone during the first die's test interval and regulating its approach to the same or another prescribed testing temperature. The second zone is therefore thermally preconditioned in advance rather than being heated only after probing of the first zone is complete. A POSITA would have been motivated to use this overlapping sequence in DiBattista's wafer-testing system because otherwise the tester would remain idle after each die or group of die while the next zone traversed its thermal time constant and settled at the test set point. Preheating the next independently controlled zone during the existing electrical-test interval uses time that would otherwise be unavailable for thermal settling, thereby reducing inter-site delay and increasing throughput without altering the electrical test performed at the first zone. The operation would also have been predictable: DiBattista already provides independent per-location thermal control under a system controller, and Pease provides die-scale heater zones and programmable spatial-and-temporal power allocation. The controller need only schedule the second zone's heating command early enough, using routine heater power, duty-cycle, temperature-feedback, and settling-time parameters, for that zone to reach the testing temperature before its corresponding die is probed. Simultaneously heating the second zone would not prevent maintenance of the first zone because the zones are

separately addressable and their power can be independently regulated. Accordingly, the combined disclosures cover each step of claim 20—bringing a first thermal zone to a testing temperature, testing one or more corresponding die, simultaneously bringing a second thermal zone to a testing temperature, and doing so in advance of testing the die corresponding to the second zone—and a POSITA would have had a reasonable expectation of success in implementing that staged preconditioning as a routine controller-programming and scheduling function.

148. DiBattista discloses independent control of each heating element, DiBattista at 6:38-42, and testing “at high speed” with the temperature of each device “controlled independently of the other devices on the wafer during a test,” DiBattista at 12:26-31, executed by a system controller 160, DiBattista at 7:59-8:2. Staged preconditioning follows from DiBattista’s independent zone control and high-speed testing. Programming the controller to precondition a next zone during testing would have been obvious to ensure expediency of testing moving from one die to the next. Pease reinforces this, disclosing multiple independently controllable planar heater zones that actively create and maintain a desired spatial and temporal temperature profile across the substrate, which enables a zone to be brought to temperature in advance of testing. Pease at [0014], [0030]. The thermal architecture of both references makes this preconditioning predictable. DiBattista holds its circulating

coolant “at a constant temperature that is sufficiently below the set point temperature” and uses each independently controlled heating element to “bring the temperature of the contact surface to the desired set point temperature,” so that the compact, per-zone heaters allow the local surface temperature “to be changed rapidly to compensate for variations in an IC device’s instantaneous power dissipation.” DiBattista at 5:62-6:16. Because the cold plate continuously maintains the sub-set-point baseline while each zone’s heater independently supplies only the additional power needed to reach that zone’s set point, a POSITA would have understood that one zone can be ramped toward its testing temperature while an adjacent zone is simultaneously held at temperature and tested, without the heating of the advancing zone defeating temperature control of the zone under test. Pease supplies the same capability in its multiplexed array, teaching that “[t]he time-averaged heating power of each planar heater zone can be individually tuned by time-domain multiplexing,” Pease at [0019], so that the power delivered to a second zone can be increased to precondition it while the first zone is maintained at its test temperature. The “temporal” dimension of Pease’s expressly disclosed “spatial and temporal temperature profile,” Pease at [0014], is precisely this time-sequenced, in-advance heating of selected zones. A POSITA would have recognized the thermal benefit of doing so: because bringing a zone from its idle temperature to its testing

temperature requires a finite thermal settling time, preconditioning the next zone or set of zones concurrently with testing of the current zone overlaps that ramp (dead) time with productive test time, reducing the aggregate time-to-temperature across the wafer and improving throughput—a predictable thermal result achieved through each reference’s independent, rapid, per-zone thermal control, and one a POSITA would have had a reasonable expectation of achieving.

F. DEPENDENT CLAIM 21: The test system as described in claim 15 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones

149. For the reasons given for claim 20, the recited preconditioning of a second set of zones while a first set’s die is tested would have been obvious to a POSITA and follows from DiBattista’s independent zone control and high-speed testing. DiBattista at 6:38-42, 12:26-31. Claim 21, however, applies that sequence to sets of thermal zones corresponding to respective die rather than to one zone at a time. A POSITA would have understood that multiple zones associated with a single die may have different thermal loads and time constants due to local device self-

heating, edge losses, lateral conduction, and differences in the thermal path to the fluid-cooled chuck. The controller could therefore bring the first set to a die-specific testing-temperature profile and maintain its constituent zones during testing by independently adjusting their heater power, while simultaneously applying separately selected power commands to the zones of the second set. Beginning that second-set conditioning during the first die's test interval would allow zones with slower responses to start earlier and zones with faster responses to receive lower power or later commands so that the entire second set converges to the prescribed profile before testing of the second die begins. The relevant control objective would not merely be that every zone reaches the same nominal temperature at the same instant. Rather, the controller could establish zone-specific set points selected to produce the desired temperature distribution across the second die, accounting for expected differences in local power dissipation during the upcoming electrical test. Temperature feedback from sensors associated with the constituent zones, together with stored calibration data correlating heater power to die temperature, would permit the controller to determine whether the second set had reached an acceptable thermal-ready condition—such as each zone being within a specified tolerance and the spatial gradient across the die being below a selected limit—before advancing the probe sequence. The controller could also compensate for thermal coupling

among zones by reducing power to a zone as heat arrives laterally from an adjacent zone, rather than treating each zone as thermally isolated. Because the first and second sets share the same wafer and cooled chuck, a POSITA would further have recognized the desirability of coordinating their aggregate heat input. The controller could enforce a total-power limit, prioritize maintenance power for the first set during active testing, and allocate the remaining power among the second-set zones according to their measured errors and thermal time constants. It could stagger initial energization, ramp duty cycles, or temporarily reduce power in zones nearest the first set to avoid disturbing the first die through lateral conduction or a transient rise in chuck temperature. As the second set approaches its prescribed profile, the controller could transition from higher preheating power to lower maintenance power, thereby reducing overshoot when testing moves to the second die and its own self-heating begins. This set-wise coordination would provide a technical benefit beyond the single-zone sequence of claim 20: the second die would enter testing with both its average temperature and its intra-die temperature distribution already controlled, reducing the risk that one portion of the die is thermally ready while another remains outside tolerance. Implementing the sequence would require only routine grouping of zone addresses by die, characterization of zone-to-zone thermal coupling, storage of set points and tolerance criteria, and scheduling of heater

commands using known feedback signals, power limits, anticipated test duration, and measured settling times. A POSITA therefore would have expected the claimed operation to reduce inter-die delay, limit thermal overshoot and cross-talk, and improve sub-die temperature uniformity and measurement repeatability at the start of testing, with a reasonable expectation of success.

G. DEPENDENT CLAIM 22: The test system as described in claim 15 further comprising: a thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer and wherein said TIM layer comprises one of: indium foil; and graphite material

150. Herchen-1 discloses a TIM layer between the heater-bearing planar member and the cooling plate-thermal material 221 disposed on the upper surface of cooling plate 220 to aid heat removal. Herchen-1 at [0049]. *See* discussion in Claims 5 and 6 regarding obviousness of this element. *See also* Herchen-2 at [0042], [0044], [0052].

H. DEPENDENT CLAIM 25: The method as described in claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises: bringing a first thermal zone of said plurality of separately controllable thermal zones to a testing temperature; and while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of separately controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone

151. Dependent claim 25 recites the method counterpart to the staged thermal preconditioning sequence addressed in claim 20. DiBattista and Pease

together disclose or render obvious each recited step. DiBattista discloses a wafer-testing method employing an array of heating elements associated with respective integrated-circuit devices, with each heating element “controlled independently of the others,” DiBattista at 6:38-42, and further teaches high-speed testing in which the temperature of each device is “controlled independently of the other devices on the wafer during a test,” DiBattista at 12:26-31. DiBattista’s system controller 160 performs the temperature-control functions, DiBattista at 7:59-8:2. Accordingly, DiBattista supplies selectively heating and maintaining temperatures of multiple wafer areas using a thermal controller, separately controllable thermal zones corresponding to die locations, bringing a selected first zone to a testing temperature, and maintaining that zone while the corresponding die is electrically tested. Pease supplies additional support for the claimed simultaneous and advance conditioning. Pease discloses multiple independently controllable planar heater zones that actively create and maintain a desired “spatial and temporal temperature profile” across a substrate, Pease at [0014], including zones sized similarly to or smaller than a single die or group of dies so that temperature can be controlled at each die position (Pease at [0030]). Pease further discloses controller logic for the heater power supply, (Pease at [0041]), and time-division multiplexing and pulse-width modulation for adjusting the time-averaged power delivered to selected zones (Pease at [0050]).

Those teachings permit the controller, as part of the claimed method, to continue regulating the first zone at its testing temperature while independently energizing a second zone and driving it toward its testing temperature before testing begins at the die or dies corresponding to that second zone. In operation, the first thermal zone would be brought to its prescribed set point and held there while the test computer applies and evaluates electrical test signals for the corresponding die or dies. During that same test interval, the controller would address the second zone, apply a selected heater-power or duty-cycle command, and use temperature feedback to regulate its approach to the required testing temperature. Because the zones are separately addressable, thermal conditioning of the second zone can occur without interrupting maintenance of the first zone or the electrical test underway there. This overlapping sequence directly implements the claim's requirement that the second zone be brought to temperature "simultaneously" with testing at the first zone and "in advance of" testing at the second zone. A POSITA would have been motivated to use this sequence in DiBattista's high-speed wafer-testing method because sequentially waiting until completion of the first test before initiating thermal conditioning of the next die location would introduce avoidable dead time while the second zone traverses its thermal time constant and settles at the test set point. Beginning that transition during the first die's electrical-test interval uses otherwise

unavailable settling time, shortens the interval between probe sites, and increases wafer-test throughput while preserving the prescribed thermal condition for each tested die. Pease's spatial-and-temporal control and multiplexed power delivery provide an implementation for scheduling this concurrent operation and allocating power among zones. A POSITA would have expected success because the method requires only routine controller programming using known zone addresses, heater power, duty cycle, temperature feedback, anticipated test duration, and measured settling time. The controller could initiate second-zone heating sufficiently early for that zone to reach and stabilize near the testing temperature before probe contact or test execution at the corresponding die, while independently trimming power to the first zone to offset device self-heating and heat removal through the cooled support. Thus, the combined teachings cover bringing a first thermal zone to a testing temperature, testing one or more corresponding die, simultaneously bringing a second thermal zone to a testing temperature, and completing that preconditioning before testing one or more die corresponding to the second zone. The resulting staged method would predictably reduce inter-site delay, improve temperature repeatability at the beginning of each die test, and increase throughput without changing the basic operating principles of DiBattista's independently controlled

wafer-test heaters or Pease's programmable zone-control architecture. *See* discussion in Ground 1, claim 20 regarding obviousness of this element.

I. DEPENDENT CLAIM 26: The method as described in claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises: bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones

152. Claim 26 adds a distinct method-level requirement not fully addressed by the separate analyses of claims 21 and 25: the controller must coordinate *sets* of separately controllable thermal zones with individual die in a sequenced wafer-testing operation. Unlike claim 21, which recites controller instructions in the test-system context, claim 26 requires performance of the heating-and-maintaining method itself. Unlike claim 25, which preconditions one zone for one or more die, claim 26 requires coordinated control of multiple zones associated with each die—bringing a first set of zones to the testing temperature for a first die and, during testing of that die, simultaneously bringing a second set of zones to temperature for a second die. DiBattista's independently controlled heater elements and system controller permit multiple heater locations to be grouped and commanded concurrently, while Pease's scalable die-sized or sub-die-sized heater array, spatial-

and-temporal control, multiplexed addressing, and PWM power allocation permit several zones associated with one die to receive independently selected power during the same control interval. A POSITA would have grouped zones according to the thermal footprint of each die—such as zones beneath regions having different self-heating, or thermal coupling—and would have scheduled the second die's group to begin conditioning while the first die's group is maintained at temperature and electrically tested. This set-wise overlap provides a predictable advantage beyond single-zone preconditioning: it allows the controller to establish a die-specific spatial temperature profile across multiple zones before probing the next die, rather than merely achieving a nominal temperature at one location. The controller could account for different thermal time constants within the set by initiating or modulating the constituent zones separately so that the second set converges to the prescribed profile when testing advances, while feedback control continues to hold the first set against disturbances from device self-heating. Implementing that sequence would require only routine assignment of zone addresses to die, storage of set-point and timing parameters, and scheduling of multiplexed heater commands. Accordingly, the combined teachings would have rendered obvious the claimed method of maintaining a first multi-zone set during testing of a first die while concurrently preconditioning a second multi-zone set in advance of testing a second die, with a

reasonable expectation of improved temperature uniformity at test initiation, reduced inter-die settling delay, and increased throughput. DiBattista at 6:38-42, 7:59-8:2, 12:26-31; Pease at [0014], [0030], [0041], [0050].

J. DEPENDENT CLAIM 27: The method of claim 24 wherein said plurality of separately controlled thermal zones comprise a plurality of resistive traces and wherein further said selectively heating and maintaining temperatures of said plurality of separately controllable thermal zones comprises said thermal controller selectively energizing said plurality of resistive traces during said testing.

153. Dependent claim 27 further narrows the method of claim 24 by requiring both a particular heater structure—a plurality of resistive traces forming the separately controlled thermal zones—and a particular operation during testing—the thermal controller selectively energizing those traces while the wafer die are being tested. DiBattista discloses both aspects in the wafer-test context. Its chuck includes an array of heating elements associated with respective integrated-circuit devices, and each element is implemented with a “heater trace” that “provides the heat energy.” DiBattista at 6:7-16. Those heater elements are independently controllable, so the temperature-control system can direct electrical power to selected traces rather than energizing the array uniformly. DiBattista at 6:38-42. DiBattista further explains that heater power is supplied under feedback control to maintain the selected device at or near its temperature set point during electrical testing, including as device self-heating changes the local thermal load. DiBattista

at 9:16-22, 12:20-25. Thus, the traces are not merely passive structures or heaters operated only before a test; they are selectively powered as part of the ongoing test method to add localized heat where the controller determines it is required. Herchen-1 supplies additional express support for implementing the separately controllable zones as patterned resistive traces. Herchen-1 discloses conducting layers carrying heater elements formed in predetermined patterns, including etched heater elements arranged as multiple independently controlled heating zones, with separate temperature sensing for the zones. Herchen-1 at [0051], [0054], FIG. 5. A POSITA would have understood an etched or otherwise patterned resistive element to operate by Joule heating: current through the trace produces heat in an amount governed by the trace resistance and applied electrical power. Selecting which trace receives current therefore selects which corresponding thermal zone is heated, while varying the applied power or duty cycle controls the heat delivered to that zone. Combining Herchen-1's patterned, independently addressable resistive-trace construction with DiBattista's per-device wafer-test controller would have been a straightforward implementation of DiBattista's disclosed heater traces. The references perform the same thermal function using compatible electrical and thermal principles: resistive elements generate local heat, temperature sensors indicate the response, and a controller adjusts power while a cooled support removes excess heat. No change to

the basic operating principle of either system would have been required. The controller would map each trace or group of traces to a corresponding wafer area, compare the sensed temperature with the applicable test set point, and selectively energize only the trace or traces requiring additional heat. During testing, it could increase power to offset heat loss to the cold plate, reduce or interrupt power as device self-heating increases, and leave nonselected traces unpowered or at a lower duty cycle to limit thermal cross-talk. A POSITA would have been motivated to use that selective operation because continuously energizing every trace at the same level would defeat the purpose of independently controlled zones, waste power, and create unnecessary heating in wafer regions not then requiring correction. Selective energization instead permits the controller to maintain the prescribed temperature at the die under test, compensate for die-to-die differences in power dissipation and local heat transfer, and establish or preserve the spatial temperature profile needed for repeatable measurements. Implementation would have required only routine choices concerning trace geometry and resistance, zone-to-trace addressing, sensor placement, power level or duty cycle, and feedback-control parameters. A POSITA would therefore have had a reasonable expectation that DiBattista's controller, using Herchen-1's patterned resistive traces, could selectively energize a plurality of traces during testing to heat and maintain the corresponding separately controllable thermal

zones. The combined teachings accordingly disclose or render obvious each additional limitation of claim 27. DiBattista at 6:7-16, 6:38-42, 9:16-22, 12:20-25; Herchen-1 at [0051], [0054], FIG. 5.

154. Further, DiBattista's zones comprise resistive heater traces (each element implemented with a "heater trace" that "provides the heat energy"), and the temperature control system selectively energizes those elements during testing by supplying heater power under feedback control. DiBattista at 6:7-16, 9:16-22, 12:20-25. Herchen-1 confirms the resistive-trace construction with its etched heater elements arranged in individually controlled zones. Herchen-1 at [0051]. The combination therefore energizes a plurality of resistive traces to selectively heat the separately controllable zones during testing.

155. Selectively energizing the resistive traces is itself the mechanism of localized, zone-specific heating. Passing current through a resistive trace dissipates electrical power as heat in the immediate vicinity of that trace, so energizing the traces of one zone deposits heat into that zone's area of the wafer while leaving unselected zones unheated, giving spatial control of the thermal profile through the choice of which traces are energized. DiBattista confirms this thermal operation: its individual heating elements "are resistive heaters" implemented with a "heater trace [that] provides the heat energy" and a co-located RTD trace that "provides

temperature information,” the two being “electrically isolated while being at essentially the same thermal position,” so that the heat generated by energizing a given trace is sensed and regulated in closed loop at that same location. DiBattista at 7:5-25. Herchen-1 likewise discloses etched resistive traces “arranged to form six independent heating zones with a separate temperature sensor for each zone,” Herchen-1 at [0051], confirming that selective energization of the traces of a given zone produces spatially resolved heating that is independently sensed and controlled, and Herchen-1 further teaches keeping the heater elements short to reduce “warping of the planar members due to differential thermal expansion coefficients,” Herchen-1 at [0054], so that the energized traces heat their zones without distorting the surface that must stay in intimate thermal contact with the wafer. A POSITA would therefore have understood that selectively energizing the resistive traces of the separately controllable zones during testing delivers responsive, spatially resolved heat mapped to the die layout—precisely the thermal function the claim recites—and would have expected it to operate predictably, because it is no more than the ordinary resistive-heating operation of the heater traces that both references disclose, carried out under the per-zone temperature feedback each reference provides.

XV. GROUND 2: Claims 1-27 are Rendered Obvious Over DiBattista in View of Costello, Herchen-1, and Criminale

156. Claims 1-27 of the '841 Patent are unpatentable under 35 U.S.C. § 103 as obvious over DiBattista (U.S. Patent No. 6,549,026) in view of Costello (U.S. Patent Application Publication No. 2002/0017916). Both references are analogous prior art directed to the spatially controlled heating of a wafer-scale substrate supported over a liquid-cooled plate, are from the same field as the claimed invention, being directed to the spatially resolved, zone-level temperature control of a wafer-scale substrate supported over a fluid-cooled plate, and their disclosures are complementary.

A. OVERVIEW OF GROUND 2

157. *See* description of DiBattista contained in Ground 1.

158. A person of ordinary skill would have been motivated to combine DiBattista's per-device, feedback-controlled thermal regulation at wafer level with Costello's mechanically rigid, dual-sided thermally managed chuck architecture and noise/leakage mitigation to achieve improved probe-test performance, with a reasonable expectation of success. DiBattista teaches an apparatus with a heat exchanger/chuck having a surface divided into regions corresponding to IC devices, where each device's temperature is individually controlled during testing. It further teaches embodiments with multiple heating elements on a fluid-cooled chuck acting as a heat sink, and alternative separate heat exchanger bodies, enabling rapid

compensation for device self-heating and per-DUT control. Costello identifies the problem of insufficient rigidity in temperature-controlled chucks subjected to high probe-pin loads and teaches a heat sink with internal pillars that both carry coolant and transmit compressive forces to prevent deformation. Costello teaches independently controlling the temperatures of the top and bottom (prober-facing) sides of the chuck using a primary heater near the wafer side, a secondary heater near the stage side, and a cooler, to maintain wafer temperature while protecting the prober stage from thermal drift.

159. From a thermal-engineering perspective, the references address complementary portions of the same heat-flow problem. DiBattista supplies spatially localized heat input and feedback control at individual device locations to counter unequal die self-heating, while Costello supplies a stiff, actively cooled bulk heat-removal path and separate control of the wafer-facing and stage-facing portions of the chuck. A POSITA would have understood that adding Costello's dual-sided thermal management to DiBattista's per-device heater array would establish a more stable lower-temperature boundary condition beneath the localized heaters, allowing heat added at a selected die location to be removed predictably through the chuck rather than spreading laterally or accumulating in the stage. This would reduce die-to-die thermal cross-talk, through-thickness gradients, and drift in the nominal chuck

temperature while preserving DiBattista's ability to trim local heat flux for each DUT. Costello's secondary heater and lower temperature sensing would also permit the stage-facing side to be held near a controlled temperature even as the wafer-facing side is heated or cooled, thereby limiting differential thermal expansion, chuck bow, and probe-to-pad misalignment during temperature transitions. Its pillar-reinforced coolant structure would maintain thermal contact and flatness under probe loading while increasing heat-transfer area to the coolant, improving repeatability of the thermal resistance between each DUT region and the heat sink. The combined system would therefore provide both fast local correction and stable bulk heat rejection: DiBattista's heaters could respond to transient device-power changes, while Costello's primary and secondary thermal loops suppress slower changes in chuck and stage temperature. Because both references use resistive heaters, temperature sensors, controller-regulated power, and fluid cooling in wafer-probe chucks, their thermal functions and heat-flow paths are compatible. Integration would require only routine selection of heater power, coolant temperature and flow, sensor placement, set points, and feedback gains based on the chuck's thermal resistance and capacitance. A POSITA would accordingly have expected the combination to provide improved local temperature accuracy, reduced thermal lag and overshoot, lower lateral and through-thickness gradients, preserved chuck

flatness, and more repeatable electrical measurements, without changing the basic operating principle of either reference.

160. A POSITA would also have been motivated to combine DiBattista and Costello because DiBattista targets per-DUT temperature accuracy through independently controlled thermal elements, while Costello provides distributed temperature sensing and control strategies for detecting and correcting localized non-uniformities and hotspots across a temperature-controlled chuck. These teachings address complementary parts of the same closed-loop control problem. DiBattista supplies the localized actuators and per-device set-point regulation needed to add or remove thermal energy at selected die locations; Costello supplies additional spatial information concerning the actual temperature field within the chuck and control techniques, including use of multiple sensors, averaging, and emphasis on the highest-temperature region, for selecting an appropriate control response. A POSITA would have recognized that reliance on a single sensor or inferred device power can leave uncertainty between the sensed temperature and the actual temperature at the active die, particularly where coolant flow, edge losses, probe loading, material interfaces, or neighboring powered devices create spatial gradients. Incorporating Costello's sensor array into DiBattista's per-DUT architecture would provide measurements at multiple locations, allowing the

controller to identify whether a deviation is local to the die under test, shared by a group of adjacent die, or attributable to drift of the chuck as a whole. The controller could then direct DiBattista's independently controlled heater associated with the affected DUT while avoiding unnecessary changes to heaters serving regions already at their set points. Costello's averaging strategy would support regulation of the overall wafer-contact temperature without overreacting to noise at one sensor, while its hotspot-focused strategy would enable the controller to limit the maximum local temperature that could otherwise distort electrical measurements or damage temperature-sensitive structures. Using both control modes would allow a POSITA to select or transition between a uniformity objective and a peak-temperature objective depending on the test condition and device power. The combination would also improve transient control: when a DUT begins dissipating power, nearby sensors could detect the developing thermal disturbance before it propagates through the bulk chuck, and DiBattista's local actuator could reduce or interrupt heater power at that location while Costello's bulk cooling and opposite-side thermal control continue to stabilize the remainder of the assembly. Conversely, when an inactive or low-power DUT falls below the prescribed temperature, the corresponding local heater could be increased without raising the entire chuck temperature. Because both references employ temperature sensors, controller-regulated heaters, and a fluid-

cooled wafer-probe chuck, combining their sensing and actuation functions would not change their respective operating principles. Implementation would require only routine mapping of sensor locations to DUT heater zones, calibration of sensor offsets and thermal response times, and selection of known control parameters such as averaging weights, hotspot thresholds, set points, and feedback gains. A POSITA would therefore have expected the combination to reduce sensor-to-die temperature error, detect hotspots more reliably, suppress spatial gradients and overshoot, and maintain tighter and more repeatable per-DUT temperatures during probing, with a reasonable expectation of success.

161. A person of ordinary skill would view Costello's sensor arrays and control strategies as directly complementary to DiBattista's per-DUT loops, improving spatial resolution and dynamic response to device self-heating and local hotspots that DiBattista seeks to counteract. DiBattista's multiple heaters with a fluid-cooled heat sink enable rapid compensation for device self-heating. Deploying Costello's multi-sensor feedback with DiBattista's power-following control would increase robustness against local thermal anomalies, yielding tighter per-DUT temperature regulation during probing. DiBattista's control electronics use embedded sensors and device power monitoring and Costello motivates noise

reduction by gradual, continuous power changes to avoid measurement noise from electromagnetic fluctuations.

B. DEPENDENT CLAIM 4: The system as described in claim 2 further comprising: a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and a second TIM layer disposed between said wafer TI layer and said wafer

162. *See* discussion of DiBattista for this claim in Ground 1.

163. Costello also discloses or renders obvious this claim in light of knowledge of a POSITA. Costello at [0072], [0075-76], claims 13 and 29. A POSITA working from Costello would have been motivated to add TIM layers at the two relevant mechanical/thermal junctions - (i) between the cold plate (*i.e.*, Costello's cooled heat sink/thermal base) and an intermediate wafer thermal-interface ("wafer TI") layer, and (ii) between that wafer TI layer and the wafer - because Costello not only discloses adding an electrically conductive layer, but is expressly concerned with achieving uniform temperature control at the wafer during probing and maintaining planarity/flatness and minimizing distortion under substantial probe-pin loading, while still enabling heating/cooling transitions. A thermally conductive layer accomplishes these goals more effectively. From a thermal standpoint, a POSITA would have recognized that interposing a compliant, thermally conductive TIM at each of these interfaces directly advances Costello's stated thermal objectives in three related ways. First, it lowers the contact (interfacial)

thermal resistance in the heat-transfer path that runs from Costello's cooled heat sink, through the layered chuck structure, to the wafer, thereby improving conductive heat transfer and the uniform wafer temperature that Costello seeks; this complements Costello's own heat-sink design, in which pillars are arranged to "conduct chuck heat to the coolant." Costello at [0077]. Second, because Costello teaches that the chuck must accommodate differential expansion and contraction among dissimilar layers—using joints and vacuum retention that hold the layers together "while allowing relative movement due to differential thermal expansion," Costello at [0022]—a compliant TIM at each interface conforms to the mating surfaces as the stack heats and cools, filling the microscopic gaps that would otherwise open at the joints and preserving intimate thermal contact across the temperature range. Third, that same compliance maintains conductive contact under the substantial probe-pin loads Costello's rigid pillar heat sink is built to bear, so heat continues to cross each joint efficiently even as the surfaces are loaded and deflected. These benefits track Costello's express teaching that the chuck has good thermal performance and is designed to "minimize changes in height, flatness and planarity over the temperature range of the chuck." Costello at [0023]. A POSITA would therefore have found it obvious, and would have had a reasonable expectation of success, in placing a compliant thermally conductive TIM at both the cold-plate/wafer-TI-layer and

wafer-TI-layer/wafer interfaces to reduce interfacial thermal resistance, improve temperature uniformity, and preserve flatness and thermal contact across heating and cooling transitions and under probe loading.

C. DEPENDENT CLAIM 5: The system as described in claim 4 wherein said first and second TIM layers comprise indium foil.

164. *See* discussion of DiBattista for this claim in Ground 1.

165. Indium foil is a well-known compliant TIM. Indium would have been an obvious choice among a limited number of known thermal-interface materials. This is further confirmed by Cola, which discloses carbon-nanotube-based thermal-interface materials placed between a heat source and a heat sink or heat spreader—including for use during ‘burn-in’ testing of electrical components such as chips—and teaches that the thermal-interface material’s inert metal support or foil may be formed from indium, among other metals. Cola at [0019], [0086].

D. DEPENDENT CLAIM 6: The system as described in claim 4 wherein said first and second TIM layers comprise graphite material

166. *See* discussion of DiBattista for this claim in Ground 1.

167. Graphite is a well-known compliant TIM. Graphite would have been an obvious choice among a limited number of known thermal-interface materials.

E. DEPENDENT CLAIM 11: The system as described in claim 2 wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.

168. Costello and DiBattista render this claim obvious. DiBattista targets per-die thermal control by matching an independently controlled heater array to the wafer die layout, expressly to overcome whole-wafer chuck limitations and to handle localized power dissipation during wafer probing (e.g., Figs. 8A, 10A-10B; discussion of individualized control).

169. A POSITA would have understood that a die is not necessarily an isothermal heat source: functional blocks, power-delivery regions, memory arrays, and peripheral circuitry can dissipate different amounts of power during the same test pattern. Dividing the thermal footprint of each die among multiple respective zones would permit the controller to apply different local heat fluxes within that footprint, compensating for sub-die hot and cold regions rather than regulating only a single average die temperature. This finer spatial resolution would reduce in-plane temperature gradients across the active die and improve correlation between the prescribed test temperature and the temperatures of the particular circuit regions being measured.

170. Costello focuses on maintaining uniform, stable wafer-contact temperatures under load and changing conditions by independently controlling top and bottom thermal influencers and by using local sensor arrays to address hot spots. Thermally, Costello's primary heater, cooled heat-sink structure, secondary heater,

and upper and lower temperature sensing provide information and control authority across the chuck thickness, not merely at one surface. A POSITA would have recognized that this arrangement can hold the wafer-facing region near its selected condition while limiting heat leakage into, or thermal drift of, the prober-facing region. Applied to multiple zones corresponding to one die, those teachings would provide a stable bulk boundary condition beneath the die while the individual upper zones correct local temperature departures. The result would be less through-thickness gradient, reduced chuck bow from differential expansion, and more repeatable thermal resistance between the die footprint and the coolant path during successive probe contacts.

171. A POSITA seeking improved temperature uniformity and faster, localized response for high-power or non-uniform dies would have been motivated to combine DiBattista's per-die, independently controlled heater array with Costello's layered, independently controlled thermal paths and localized sensing/control. The combination would create complementary control loops at different spatial and temporal scales: Costello's cooled, dual-sided chuck would regulate the slower bulk temperature of the support, while multiple DiBattista-type zones within each die footprint would respond more rapidly to localized changes in device power. When one portion of a die begins self-heating during a test vector, the

controller could reduce heater power in the corresponding zone without disturbing adjacent zones serving cooler portions of the same die; when power shifts to another circuit block, the zone commands could be redistributed accordingly. This localized transient response would reduce overshoot and thermal lag, preserve a more uniform junction-temperature profile during changing test patterns, and avoid the delay and measurement disturbance associated with changing the temperature of the entire chuck.

172. Both references operate in wafer-probing contexts, and integration would have involved routine thermal engineering: partitioning each die footprint into multiple addressable zones, associating sensor signals with those zones, and selecting heater power and feedback gains based on the known thermal resistance and capacitance of the wafer-chuck stack. Zone boundaries could be selected to follow expected power-density regions or to provide edge-versus-center correction, while the cooled structure supplies a common heat-rejection path. A POSITA would also have accounted for lateral conduction between neighboring zones by calibrating the control matrix or limiting simultaneous power changes, thereby reducing thermal cross-talk without requiring perfect physical isolation. Costello's rigid, pillar-supported heat sink would maintain contact pressure and heat-transfer area under probe loading, helping each zone retain a predictable response after repeated

indexing of the wafer. Nothing in either reference suggests thermal incompatibility; both employ resistive heating, sensing, feedback control, and fluid-assisted heat removal. A POSITA therefore would have reasonably expected multiple respective zones per die to provide predictable gains in sub-die uniformity, hotspot suppression, settling time, and repeatability, while preserving wafer flatness and probe alignment.

F. DEPENDENT CLAIM 20: The test system as described in claim 15 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone

173. *See* discussion in Ground 1, claim 20.

174. DiBattista discloses independent control of each heating element, DiBattista at 6:38-42, and testing “at high speed” with the temperature of each device “controlled independently of the other devices on the wafer during a test,” DiBattista at 12:26-31, executed by a system controller 160, DiBattista at 7:59-8:2. Staged preconditioning follows from DiBattista’s independent zone control and high-speed testing. Programming the controller to precondition a next zone during testing would have been obvious to ensure expediency of testing.

175. From a thermal perspective, each wafer region has a finite time constant determined by the local thermal mass, heater power, thermal resistance to the fluid-cooled chuck, and heat generated by nearby devices. If heating of the next zone began only after testing of the current die was complete, the tester would have to wait while that zone approached and settled at the prescribed testing temperature. A POSITA would therefore have been motivated to use DiBattista's independently controlled heaters to begin conditioning the second zone during the electrical-test interval for the first zone, thereby overlapping thermal settling with useful test time. The controller could maintain the first zone by adjusting its heater power in response to the device's self-heating, while separately applying power to the second zone based on its anticipated heating rate and the remaining test duration. Because the cooled chuck supplies a common heat-removal path, the controller could also limit second-zone power or begin conditioning sufficiently early to reduce overshoot, lateral thermal spreading, and disturbance of the zone being tested. Implementing that sequence would require only routine scheduling of independently addressable heater commands using known set points, feedback signals, heater power, and measured settling times. Programming the controller to precondition the next zone during testing therefore would have predictably reduced inter-site delay, improved

the repeatability of the second zone's temperature at the start of testing, and increased throughput, with a reasonable expectation of success.

G. DEPENDENT CLAIM 21: The test system as described in claim 15 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones

176. For the reasons given for claim 20, the recited preconditioning of a second set of zones while a first set's die is tested would have been obvious to a POSITA and follows from DiBattista's independent zone control and high-speed testing. DiBattista at 6:38-42, 12:26-31.

177. Claim 21, however, applies that sequence to sets of thermal zones corresponding to respective die rather than to one zone at a time. A POSITA would have understood that multiple zones associated with a single die may have different thermal loads and time constants due to local device self-heating, edge losses, lateral conduction, and differences in the thermal path to the fluid-cooled chuck. The controller could therefore bring the first set to a die-specific testing-temperature profile and maintain its constituent zones during testing by independently adjusting

their heater power, while simultaneously applying separately selected power commands to the zones of the second set. Beginning that second-set conditioning during the first die's test interval would allow zones with slower responses to start earlier and zones with faster responses to receive lower power or later commands so that the entire second set converges to the prescribed profile before testing of the second die begins. The relevant control objective would not merely be that every zone reaches the same nominal temperature at the same instant. Rather, the controller could establish zone-specific set points selected to produce the desired temperature distribution across the second die, accounting for expected differences in local power dissipation during the upcoming electrical test. Temperature feedback from sensors associated with the constituent zones, together with stored calibration data correlating heater power to die temperature, would permit the controller to determine whether the second set had reached an acceptable thermal-ready condition—such as each zone being within a specified tolerance and the spatial gradient across the die being below a selected limit—before advancing the probe sequence. The controller could also compensate for thermal coupling among zones by reducing power to a zone as heat arrives laterally from an adjacent zone, rather than treating each zone as thermally isolated.

178. Because the first and second sets share the same wafer and cooled chuck, a POSITA would further have recognized the desirability of coordinating their aggregate heat input. The controller could enforce a total-power limit, prioritize maintenance power for the first set during active testing, and allocate the remaining power among the second-set zones according to their measured errors and thermal time constants. It could stagger initial energization, ramp duty cycles, or temporarily reduce power in zones nearest the first set to avoid disturbing the first die through lateral conduction or a transient rise in chuck temperature. As the second set approaches its prescribed profile, the controller could transition from higher preheating power to lower maintenance power, thereby reducing overshoot when testing moves to the second die and its own self-heating begins.

179. This set-wise coordination would provide a technical benefit beyond the single-zone sequence of claim 20: the second die would enter testing with both its average temperature and its intra-die temperature distribution already controlled, reducing the risk that one portion of the die is thermally ready while another remains outside tolerance. Implementing the sequence would require only routine grouping of zones by die, characterization of zone-to-zone thermal coupling, storage of set points and tolerance criteria, and scheduling of heater commands using known feedback signals, power limits, anticipated test duration, and measured settling

times. A POSITA, therefore, would have expected the claimed operation to reduce inter-die delay, limit thermal overshoot and cross-talk, and improve sub-die temperature uniformity and measurement repeatability at the start of testing, with a reasonable expectation of success.

H. DEPENDENT CLAIM 22: The test system as described in claim 15 further comprising: a thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer and wherein said TIM layer comprises one of: indium foil; and graphite material

180. *See discussion of claims 5 and 6, above.*

I. DEPENDENT CLAIM 25: The method as described in claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises: bringing a first thermal zone of said plurality of separately controllable thermal zones to a testing temperature; and while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of separately controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone

181. *See discussion of claim 20, above.*

J. DEPENDENT CLAIM 26: The method as described in claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises: bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones

182. *See discussion of claim 21, above.*

XVI. GROUND 3: Claims 1-27 are Rendered Obvious Over Sugiyama in View of Parkhe, Natsuhara, Criminale, and knowledge of a POSITA

183. Claims 1-27 of the '841 Patent is unpatentable under 35 U.S.C. § 103 as obvious over Sugiyama (U.S. Patent Pub. No. 2004/0227536) in view of Parkhe (U.S. Patent Pub. No. 2016/0111315). These references are analogous prior art directed to the spatially controlled heating of a wafer-scale substrate supported over a liquid-cooled plate, and their disclosures are complementary.

A. OVERVIEW OF GROUND 3

184. Sugiyama discloses probers and probe testing methods enabling accurate, efficient temperature control of wafer-level test sites while preventing chuck tilt under probe load. A first aspect provides a prober with a main chuck on a Z stage, X-Y positioning, a probe card above, and multiple heaters sized to individual devices or device groups, each with temperature sensors and a heat exchanger controlled by a temperature controller. These heaters can be organized as cell structures aligned to die locations or die groups, each cell optionally including its own heater, sensor, and heat exchanger, with heat insulators between cells to reduce thermal cross-talk.

185. Operation includes placing and fixing a wafer, aligning in X, Y, and theta, contacting probes by raising the Z stage, overdriving, and testing after bringing the selected site to a set temperature. A second aspect reconfigures mechanics so the

X-Y stage has a central frame opening and carries a frame-structured substrate fixing mechanism with a continuous central opening. A probing stage with an upper flat surface smaller than the frame openings is fixed on the Z stage via a probing stage elevating mechanism, and is coaxial with the probe-card centerline.

186. This structure prevents main chuck tilt from probe needle pressure, particularly at wafer peripheries, improving stable contact. The probing stage can incorporate a heater, temperature sensor, and heat exchanger sized to the single site or multi-site region contacted by the probes, allowing rapid, low-energy thermal control of only the tested region. The probing stage is preferably aluminum, detachably mounted for exchange to match site size, and its compact mass reduces thermal inertia for faster heating and cooling. Alternative embodiments position the Z stage elevating mechanism on the stage base, use one or multiple Z drives, and implement the X-Y drive with linear motors and air bearings for smooth motion. Wafer fixing options include vacuum grooves or ports, hinged retainers, and a vertically actuated ring with support columns, and the chuck plate can be detachable. A method is claimed that sequences placement, X-Y-theta alignment, raising the probing stage to support the wafer, bringing probes into contact, overdriving, temperature conditioning to a target, electrical testing, and separation, repeated across sites.

187. Parkhe is directed to electrostatic chuck (ESC) assemblies usable for high-temperature semiconductor processing, addressing failures above about 120°C by providing a puck with an electrically insulative upper plate (with heating elements and electrodes) metal-bonded to a lower plate, fastener-coupled to a cooling plate with controlled force distribution and optional thermal choke features to achieve uniform heat transfer and high-temperature operation.

188. Further, Sugiyama teaches that heating/cooling large chuck areas is inefficient and slow, and advocates localized, cell-matched heaters/heat exchangers with sensors to reduce energy use and time to temperature. Parkhe seeks high-temperature ESC operation with uniform heat transfer and controlled thermal choke between puck and cooling plate. Combining Sugiyama's localized control with Parkhe's robust high-temperature ESC predictably improves spatial uniformity, transient response, and energy efficiency - recognized goals in wafer processing and testing.

189. A person of ordinary skill in the art would have been motivated to combine Sugiyama and Parkhe because their teachings address complementary parts of the same wafer-probe thermal-management problem. Sugiyama supplies the wafer-probe-specific control architecture: independently controlled local cells equipped with heaters, temperature sensors, and heat exchangers permit closed-loop

adjustment of temperature in localized regions of the supported wafer. Parkhe supplies a compatible mechanical and thermal foundation for that architecture: a heated puck and cooling-plate stack having a controlled thermal interface, distributed fastening, thermal-isolation features, and a stable heat-rejection path. Mounting or implementing Sugiyama's local control cells on Parkhe's mechanically stable, actively cooled support would allow each cell to add or remove heat locally while the puck/cooling-plate assembly establishes a repeatable boundary condition and carries rejected heat away. The combination would therefore reduce thermal cross-talk between neighboring regions, reduce variation in thermal-interface resistance, reduce radial and through-thickness temperature gradients, reduce thermally induced warpage and resulting probe-to-pad misalignment, while improving transient response and run-to-run repeatability. The references are technically compatible because both regulate temperature through conductive thermal paths using heaters, sensors, heat exchangers or cooling structures, and mechanically joined support components; neither requires an operating principle that would defeat the other. Selecting cell dimensions and placement, heater and sensor ratings, interface materials and thicknesses, fastener number and torque, isolation geometry, and coolant flow would have been routine implementation choices within the ordinary skill in thermal-fixture and wafer-prober design. Those choices would

predictably provide finer local correction superimposed on a stable cooled baseline, rather than produce an unexpected interaction. Accordingly, a skilled artisan would have had a reasonable expectation of successfully obtaining localized closed-loop thermal control on a mechanically stable cooled support, with the predictable benefits of lower gradients and distortion, faster settling, more accurate probe alignment, and improved measurement repeatability.

190. Further, Sugiyama teaches that heating/cooling large chuck areas is inefficient and slow, and advocates localized, cell-matched heaters/heat exchangers with sensors to reduce energy use and time to temperature. Parkhe seeks high-temperature ESC operation with uniform heat transfer and controlled thermal choke between puck and cooling plate. Combining Sugiyama's localized control with Parkhe's robust high-temperature ESC predictably improves spatial uniformity, transient response, and energy efficiency - recognized goals in wafer processing and testing.

191. It would have been obvious to substitute one known element for another. Sugiyama explicitly discloses temperature control elements comprising heaters with associated heat exchangers and sensors arranged as cells and controlled by a temperature controller. Parkhe's ESC already integrates heaters, sensors, and cooling channels/conduits and even references multiple heating zones and thermal

isolators to shape lateral profiles. Replacing or augmenting Parkhe's broader zones with Sugiyama's finer cell architecture is a straightforward substitution of known temperature-control topologies, expected to yield predictable improvements.

B. DEPENDENT CLAIM 3: The test system as described in claim 2 further comprising: a chiller for cooling liquid; and a valve for controlling an amount of said liquid flowing to said cold plate, wherein said valve is controlled by said thermal controller

192. Sugiyama discloses this element. Sugiyama at [0068-70].

193. To the extent Sugiyama does not disclose this element, Parkhe does; and it would have been obvious to supplement Sugiyama's disclosure with Parkhe for the reasons stated above. Parkhe at [0029], [0051], [0065-66].

194. Per-cell heat exchangers under per-cell temperature control mean the controller must differentially regulate cooling among cells. Such coolant-flow valves may be placed in the respective branch lines serving the per-cell heat exchangers and operated by the controller, in response to cell-temperature feedback, either proportionally or on an on/off basis to balance flow among cells. Differential regulation of a circulating coolant, at the granularity of each cell's exchanger, necessarily occurs by controlling coolant flow or capacity to each cell. In a fluid circuit, that modulation is performed by flow-control elements - *i.e.*, valves - actuated under the controller's commands to increase/decrease coolant flow to a given cell to meet its setpoint. As an example, this is consistent with Lutz (U.S. Pat.

Pub. No. 2003/0155939), which discloses a device-under-test temperature controller that regulates cooling of the heat-spreader plate by controlling the chiller, together with an external chiller that circulates coolant to the heat-exchanger, confirming that controller-regulated delivery of coolant to the plate was conventional. Lutz, claims 12, 14, and 16.

195. Sugiyama and Parkhe independently confirm the obviousness of a controller-actuated valve regulating coolant flow to the cold plate as a matter of thermal operation. Sugiyama cools each test site with a heat exchanger 20 that “includes a fluid supply/drain channel 20a and fluid supply unit 20b” through which “[a] fluid having high thermal conductivity is circulated,” Sugiyama at [0068], and its temperature controller “control[s] the temperatures of the cells separately on the basis of the detection results of the temperature sensors,” Sugiyama at [0070]. Because separate, per-cell cooling requires delivering different amounts of circulated coolant to different cells’ heat exchangers in order to hold each cell at its own set-point temperature, a POSITA would have understood that the controller necessarily modulates the coolant flow reaching each cell—and in a circulating-fluid circuit that flow modulation is accomplished by controller-actuated flow-control valves. Parkhe likewise circulates a “temperature regulating fluid” from a fluid source 172 through conduits in the cooling plate to heat and/or cool the puck under

controller control, Parkhe at [0029], and teaches that “the heat flux flowing from the puck 166 to the cooling plate 164 may be controlled” by adjusting the factors that affect heat transfer, Parkhe at [0053]-[0054]. Regulating the flow of the circulated coolant delivered to the cold plate with a controller-operated valve is the conventional and predictable means of controlling that cooling heat flux so as to drive and hold the cold plate, and thus the wafer, at the desired temperature. A POSITA combining Sugiyama’s per-cell circulated-fluid cooling with Parkhe’s controller-regulated coolant circulation would therefore have found it obvious, and would have had a reasonable expectation of success, to include a valve controlled by the thermal controller to regulate the amount of cooling liquid flowing to the cold plate, as the claim recites, achieving the predictable thermal result of faster, more accurate, and spatially differentiated cooling during testing.

C. DEPENDENT CLAIM 4: The system as described in claim 2 further comprising: a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and a second TIM layer disposed between said wafer TI layer and said wafer

196. This element would have been obvious in light of Sugiyama and Parkhe. *See* Parkhe at [0055-56], [0071]. A POSITA working from Sugiyama would have been motivated to add TIM layers at the two relevant mechanical/thermal junctions - (i) between a cold plate and an intermediate wafer thermal-interface (“wafer TI”) layer, and (ii) between that wafer TI layer and the wafer - because

Sugiyama is concerned with achieving temperature control at the wafer during probing, while still enabling heating/cooling transitions. A thermally conductive layer accomplishes these goals more effectively. Cola confirms the benefit, disclosing that a thermal-interface material placed between a heat source and a heat sink or spreader improves the transfer of heat, including for chips and dies. Cola at [0019].

197. The thermal rationale for adding a TIM at each interface follows directly from Parkhe's and Sugiyama's own teachings about how heat crosses these junctions. Parkhe teaches that heat transfer across the mechanical interface between the puck and the cooling plate is governed by the condition of that interface: the surface roughness, surface features, and material at the interface "affect heat transfer properties between the electrostatic puck . . . and the heat sink," Parkhe at [0066]; the fasteners are tightened to make the interface separation uniform so as to "ensure that the heat transfer properties between the cooling plate 164 and the puck 166 are uniform," and a conductive medium may be introduced into the interface "to improve heat transfer between the puck 166 and the cooling plate 164," Parkhe at [0052]; and "the heat flux flowing from the puck 166 to the cooling plate 164 may be controlled" by adjusting the factors that affect heat transfer across that interface, Parkhe at [0053]-[0054]. A POSITA would have recognized that a compliant,

thermally conductive TIM is exactly such an interface medium: interposed at the cold-plate/wafer-TI-layer and wafer-TI-layer/wafer junctions, it conforms to the mating surfaces, fills the microscopic air gaps that would otherwise raise interfacial thermal resistance, and makes heat transfer across each joint both more efficient and more uniform—furthering Parkhe’s express aim of uniform, controllable heat transfer across the interface while the puck and cooling plate remain “free to expand or contract independently during thermal cycling,” Parkhe at [0053]. The same reasoning applies to Sugiyama, which cools each test site by circulating “[a] fluid having high thermal conductivity” through its heat exchanger, Sugiyama at [0068], and forms its temperature-controlled probing stage from “a metal having high thermal conductivity such as aluminum,” Sugiyama at [0087], to achieve the accurate, efficient per-site temperature control it seeks; interposing a conductive TIM at the interfaces in the heat path from that cooled structure to the wafer predictably reduces interfacial thermal resistance and improves the speed and uniformity of that temperature control. Adding a conductive TIM at each interface is therefore the application of a known thermal-interface technique to improve heat transfer across the joints of the combined system in the manner for which such materials are conventionally used, and a POSITA would have had a reasonable expectation of success in doing so.

D. DEPENDENT CLAIM 5: The system as described in claim 4 wherein said first and second TIM layers comprise indium foil.

198. Indium foil is a well-known compliant TIM. Indium would have been an obvious choice among a limited number of known thermal-interface materials, obvious for the reasons set forth in claim 4, above. This is further confirmed by Cola, which discloses carbon-nanotube-based thermal-interface materials placed between a heat source and a heat sink or heat spreader—including for use during ‘burn-in’ testing of electrical components such as chips—and teaches that the thermal-interface material’s inert metal support or foil may be formed from indium, among other metals. Cola at [0019], [0086].

E. DEPENDENT CLAIM 6: The system as described in claim 4 wherein said first and second TIM layers comprise graphite material

199. Graphite is a well-known compliant TIM. Graphite would have been an obvious choice among a limited number of known thermal-interface materials. It would have been obvious to supplement Sugiyama’s disclosure with Parkhe for the reasons stated above. Parkhe at [0055-56], [0071]. As discussed above, Cola identifies pyrolytic graphite as a known, state-of-the-art compliant thermal-interface material, evaluated for its compressibility and rebound. Cola at [0167], [0171].

F. DEPENDENT CLAIM 20: The test system as described in claim 15 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first thermal zone of said plurality of discretely controllable

thermal zones to a testing temperature; and while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone

200. Temperature-sensor feedback can regulate the selected or preconditioned zone, with heater power ramped according to the zone's thermal time constant until a defined settling tolerance is reached; limiting or staggering power can reduce overshoot and thermal cross-talk through adjacent zones and the cooled support. These routine controls would improve starting-temperature repeatability and support a reasonable expectation of success. Sugiyama discloses independent control of each heating element, Sugiyama at [0020-22]. As noted above, Sugiyama discloses a controller for controlling independent heating elements. Staged preconditioning follows from Sugiyama's independent zone control and wafer testing system based on knowledge of a POSITA. Sugiyama at [0062-67]. Programming the controller to precondition a next zone during testing would have been obvious to ensure expediency of testing. Pease reinforces this, disclosing independently controllable heater zones that actively create and maintain a desired spatial and temporal temperature profile, which enables a next zone to be brought to temperature during testing. Pease at [0014], [0030].

201. The thermal design of both Sugiyama and Parkhe makes this concurrent preconditioning predictable. Sugiyama's heaters are organized as cell structures, each with its own heater, temperature sensor, and heat exchanger, and its temperature controller "control[s] the temperatures of the cells separately," Sugiyama at [0070]; the cells are further separated by "heat insulators 40 to partition themselves from each other," so that each object "can be controlled to a predetermined temperature in an environment that is not easily influenced by the temperature of an adjacent cell," Sugiyama at [0071]. A POSITA would have understood that this inter-cell thermal isolation is precisely what allows one cell to be ramped toward its testing temperature while an adjacent cell is simultaneously held at temperature and tested, without the preconditioning of the next cell disturbing temperature control of the cell under test. Sugiyama also teaches sizing each heated region to the object so that "the time required for increasing the temperature of the object to be tested can be shortened," Sugiyama at [0086], and so that, owing to low thermal inertia, "the object to be tested can be heated quickly," Sugiyama at [0089]—a fast per-zone thermal ramp that both enables and motivates preconditioning the next zone during testing in order to overlap that ramp time with productive test time. Parkhe supplies the same capability in its zoned architecture, disclosing that "the puck 166 includes two separate heating zones that can maintain

distinct temperatures,” Parkhe at [0029], with embedded thermal isolators between the cooling conduits to shape the lateral temperature profile, and teaching a thermal-choke design in which, “[t]o provide efficient heating of the substrate, it is desirable to limit the amount of heat conducted away from the upper puck plate,” Parkhe at [0054]—efficient, independently held zone temperatures that likewise permit one zone to be brought to temperature in advance while another is maintained at its test temperature. A POSITA would therefore have found it obvious, with a reasonable expectation of success, to program the controller to precondition a next zone to its testing temperature while testing the current zone, achieving the predictable thermal benefit of reduced aggregate time-to-temperature and improved throughput across the wafer.

G. DEPENDENT CLAIM 21: The test system as described in claim 15 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones

202. For the reasons given for claim 20, the recited preconditioning of a second set of zones while a first set’s die is tested would have been obvious to a

POSITA and follows from Sugiyama's independent zone control and wafer testing system.

H. DEPENDENT CLAIM 22: The test system as described in claim 15 further comprising: a thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer and wherein said TIM layer comprises one of: indium foil; and graphite material

203. *See discussion of claims 5 and 6, above.*

I. DEPENDENT CLAIM 25: The method as described in claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises: bringing a first thermal zone of said plurality of separately controllable thermal zones to a testing temperature; and while said test computer system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of separately controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone

204. *See discussion of claim 20, above.*

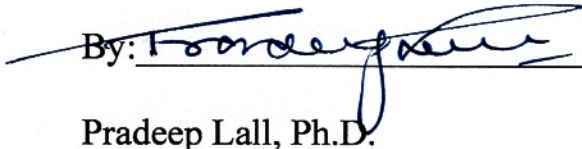
J. DEPENDENT CLAIM 26: The method as described in claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises: bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and while said test computer system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones

205. *See discussion of claim 21, above.*

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Dated:

Oct 4, 2026

By: 

Pradeep Lall, Ph.D.