Doc Code: TRACK1.REQ
Document Description: TrackOne Request

PTO/AIA/424 (04-14)

CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION UNDER 37 CFR 1.102(e) (Page 1 of 1)

First Named Inventor:	Samer Kabbani	Nonprovisional Application Number (if known):	
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i)(1) and the prioritized examination fee set forth in 37 CFR 1.17(c) have been filed with the request. The publication fee requirement is met because that fee, set forth in 37 CFR 1.18(d), is currently $0. The basic filing fee, search fee, and examination fee are filed with the request or have been already been paid. I understand that any required excess claims fees or application size fee must be paid for the application.

2. I understand that the application may not contain, or be amended to contain, more than four independent claims, more than thirty total claims, or any multiple dependent claims, and that any request for an extension of time will cause an outstanding Track I request to be dismissed.

3. The applicable box is checked below:

I. ☑ Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)

i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.

---OR---

(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.

ii. An executed inventor's oath or declaration under 37 CFR 1.63 or 37 CFR 1.64 for each inventor, **or** the application data sheet meeting the conditions specified in 37 CFR 1.53(f)(3)(i) is filed with the application.

II. ☐ Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)

i. A request for continued examination has been filed with, or prior to, this form.
ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature /Anthony C. Murabito/	Date 4-20-2022
Name (Print/Typed) Anthony C. Murabito	Practitioner Registration Number 35295

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required.**

☐ *Total of 1 forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	AATS-0107-02C01US
	Application Number	
Title of Invention	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Samer		Kabbani	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Laguna Niguel	CA	US

Mailing Address of Inventor:

Address 1	13 O Hill Ridge
Address 2	
City	Laguna Niguel
State/Province	CA
Postal Code	92677
Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Paul		Ferrari	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Mission Viejo	CA	US

Mailing Address of Inventor:

Address 1	27082 Segovia Circle
Address 2	
City	Mission Viejo
State/Province	CA
Postal Code	92691
Country	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Ikeda		Hiroki	

Residence Information (Select One) ◯ US Residency ● Non US Residency Active US Military Service

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	AATS-0107-02C01US
	Application Number	
Title of Invention	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING	

City	Kukishi Saitama	Country of Residence [i]	JP

Mailing Address of Inventor:

Address 1	12-15-20 Minami-Kurihashi		
Address 2			
City	Kukishi Saitama	State/Province	
Postal Code	349-1117	Country [i]	JP

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Kiyokawa		Toshiyuki	

Residence Information (Select One) ○ US Residency ◉ Non US Residency Active US Military Service

City	Kukishi Saitama	Country of Residence [i]	JP

Mailing Address of Inventor:

Address 1	781-7 Nokuki		
Address 2			
City	Kukishi Saitama	State/Province	
Postal Code	346-0002	Country [i]	JP

Inventor 5 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Gregory		Cruzan	

Residence Information (Select One) ◉ US Residency ○ Non US Residency Active US Military Service

City	Anaheim	State/Province	CA	Country of Residence [i]	US

Mailing Address of Inventor:

Address 1	189 South Peralta Hills Dr.		
Address 2			
City	Anaheim	State/Province	CA
Postal Code	92807	Country [i]	US

Inventor 6 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Karthik		Ranganathan	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	AATS-0107-02C01US
	Application Number	
Title of Invention	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING	

Residence Information (Select One) ◉ US Residency ○ Non US Residency Active US Military Service

City	Foothill Ranch	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	17 Beaulieu Lane		
Address 2			
City	Foothill Ranch	State/Province	CA
Postal Code	92610	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	109838		
Email Address	officeaction@mhbpatents.com	Add Email	Remove Email

Application Information:

Title of the Invention	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING		
Attorney Docket Number	AATS-0107-02C01US	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	9	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	AATS-0107-02C01US
	Application Number	
Title of Invention	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING	

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	**Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	109838		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	17528002	2021-11-16
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
17528002	Claims benefit of provisional	63115813	2020-11-19
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.			Add

Foreign Priority Information:

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	AATS-0107-02C01US
	Application Number	
Title of Invention	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING	

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	AATS-0107-02C01US
	Application Number	
Title of Invention	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	AATS-0107-02C01US
	Application Number	
Title of Invention	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Advantest Test Solutions, Inc.		
Mailing Address Information For Applicant:			
Address 1	3061 Zanker Rd.		
Address 2			
City	San Jose	**State/Province**	CA
Country	US	Postal Code	95134
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	AATS-0107-02C01US
	Application Number	
Title of Invention	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Anthony C. Murabito/			Date (YYYY-MM-DD)	2022-04-20
First Name	Anthony	Last Name	Murabito	Registration Number	35295

Additional Signature may be generated within this form by selecting the Add button. Add

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	AATS-0107-02C01US
	Application Number	
Title of Invention	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

RELATED APPLICATION(S)

[0001] This application is a Continuation of and claims priority to U.S. Serial No. 17/528,002, attorney docket AATS-0107-01U00US, entitled "Wafer Scale Active Thermal Interposer for Device Testing," to Kabbani et al., filed 11/16/2021, which in turn claims priority to U.S. Provisional Application No. 63/115,813, attorney docket AATS-0107-00.00US, filed 11/19/2020, entitled "Wafer Scale Active Thermal Interposer." This application is related to U.S. Patent No. 9,291,667 entitled "Adaptive Thermal Control." All such applications are hereby incorporated herein by reference in their entireties.

FIELD OF INVENTION

[0002] Embodiments of the present invention relate to the field of integrated circuit manufacturing and test. More specifically, embodiments of the present invention relate to systems and methods for testing integrated circuit devices in wafer embodiments.

BACKGROUND

[0003] It is common to subject integrated circuits, either packaged or unpackaged, to environmental testing as an operation in a manufacturing processes. Typically in such testing, the integrated circuit devices are subject

to electrical testing, e.g., "test patterns," to confirm functionality while being subjected to environmental stress. For example, an integrated circuit is heated and/or cooled to its specification limits while being electrically tested. In some cases, e.g., for qualification testing, an integrated circuit may be stressed beyond its specifications, for example, to determine failure points and/or establish "guard band" on its environmental specifications.

[0004] Traditionally, such testing has included placing one or more integrated circuits and their associated test interface(s) and support hardware into an environmental chamber. The environmental chamber would heat and/or cool the integrated circuit(s) under test, known as or referred to as a device under test, or "DUT," as well as the test interface and support hardware, to the desired test temperature. Unfortunately, use of such test chambers has numerous drawbacks. For example, the limits and/or accuracy of such testing may be degraded due to environmental limits of the test interface circuits and/or devices. In addition, due to the large volumes of air and mass of mounting structures and interface devices required within an environmental test chamber, the environment inside such a test chamber may not be changed rapidly, limiting a rate of testing. Further, placing and removing DUTs and testing apparatus into and out of such test chambers further limits rates of testing, and requires complex and expensive mechanisms to perform such insertions and removals.

[0005] Recently, environmental test systems have be created that heat and/or cool a DUT directly, without placing the DUT and test apparatus into an environmental chamber. Such "chamber-less" test systems overcome many of the limitations of chamber-based testing. Unfortunately, chamber-less test systems introduce testing difficulties, particularly related to cooling integrated circuits under test.

[0006] Cooling of integrated circuits under test is typically performed by thermally coupling a cooling structure, e.g., metal, to the device under test. A cooling fluid, e.g., comprising glycol, is circulated through a portion of the cooling structure. To adjust the temperature of the cooling structure, the temperature of the cooling fluid may be adjusted. The flow of the cooling fluid may also be adjusted, e.g., increased, reduced, started, and/or stopped.

[0007] It is desirable to perform environmental testing at a wafer level, for example, comprising tens to potentially thousands of dice, beneficially increasing manufacturing throughput. In addition, testing at a wafer level may identify defective or sub-standard die at the wafer level, avoiding the expense of additional manufacturing and test operations for such devices.

[0008] Unfortunately, precise heating and/or cooling of an individual die within a wafer is not available under the conventional art, rendering wafer-level testing under environmental conditions unavailable.

SUMMARY OF THE INVENTION

[0009] Therefore, what is needed are systems and methods for wafer scale active thermal interposer devices. What is additionally needed are systems and methods for wafer scale active thermal interposer devices operable to control different portions of a wafer to different temperatures. There is a further need for systems and methods for wafer scale active thermal interposer devices that are compatible and complementary with existing systems and methods of testing integrated circuits.

[0010] In accordance with embodiments of the present invention, a system for testing circuits of an integrated circuit semiconductor wafer includes a tester system for generating signals for input to the circuits and for processing output signals from the circuits for testing the wafer and a test stack coupled to the tester system. The test stack includes a wafer probe for contacting a first surface of the wafer and for probing individual circuits of the circuits of the wafer, a wafer thermal interposer (TI) layer operable to contact a second surface of the wafer and operable to selectively heat areas of the wafer, and a cold plate disposed under the wafer TI layer and operable to cool the wafer. The system further includes a thermal controller for selectively heating and maintaining temperatures of the areas of the wafer by controlling cooling of the cold plate and by controlling selective heating of the wafer TI layer.

[0011] In accordance with another embodiment of the present invention, a system for testing circuits of an integrated circuit semiconductor wafer includes a tester system for generating signals for input to the circuits and for processing output signals from the circuits for testing the wafer and a test stack coupled to the tester system. The test stack includes a wafer probe for contacting a top surface of the wafer and for probing individual circuits of the circuits of the wafer, a wafer thermal interposer (TI) layer operable to contact a bottom surface of the wafer and including a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of the wafer, and a cold plate disposed under the wafer TI layer and operable to cool the wafer. The system further includes a thermal controller for selectively heating and maintaining temperatures of areas of the wafer by controlling cooling of the cold plate and by controlling heating of the plurality of discretely controllable thermal zones of the wafer TI layer.

[0012] In accordance with a method embodiment of the present invention, a method for testing circuits of an integrated circuit semiconductor wafer includes testing the circuits of the wafer by using a tester system to generate signals for input to the circuits and to process output signals from the circuits, and in conjunction with the testing, selectively heating and maintaining temperatures of a plurality of areas of the wafer by using a thermal controller controlling a thermal interposer layer and a cold plate,

both disposed in proximity of the wafer and wherein the thermal interposer includes a plurality of separately controllable thermal zones wherein each thermal zone is operable to be selectively heated and temperature maintained by the thermal controller.

[0013] Embodiments include a system for testing circuits of an integrated circuit semiconductor wafer device under test (DUT), the system comprising: a tester system for generating signals for input to said circuits and for processing output signals from said circuits for testing said wafer DUT; a test stack coupled to said tester system, said test stack comprising: a wafer probe for contacting a top surface of said wafer DUT and for probing individual circuits of said circuits of said wafer DUT; a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer DUT and operable to selectively heat areas of said wafer DUT; and a cold plate disposed under said wafer TI layer and operable to cool said wafer DUT, said cold plate being disposed within a thermal array; and a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer DUT by controlling cooling of said cold plate and by controlling heating of said wafer TI layer.

[0014] Embodiments include the above and further comprising a power supply coupled to provide power to said wafer TI layer and controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said

heating of said wafer TI layer is based on said PWM signals. Embodiments include the above and further comprising: a chiller for cooling liquid; a valve for controlling an amount of said liquid flowing to said cold plate, wherein said valve is controlled by said thermal controller. Embodiments include the above and further comprising: a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and a second TIM layer disposed between said wafer TI layer and said wafer DUT.

[0015] Embodiments include the above and wherein said first and second TIM layers comprise indium foil. Embodiments include the above and further comprising: a first vacuum valve for establishing suction for securing said wafer DUT to said wafer TI layer; a second vacuum valve for establishing suction for securing said wafer TI layer to said cold plate; and a vacuum pump coupled to both said first and second vacuum valves. Embodiments include the above and further comprising: a first blow-off valve for controlling air to release said wafer DUT from said wafer TI layer; a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and a source of air coupled to both said first and second blow-off valves.

[0016] Embodiments include the above and wherein said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and wherein said plurality of traces are operable to selectively heat a plurality of zones of said wafer TI layer under control of said thermal controller and wherein

further said plurality of zones correspond to said areas of said wafer DUT. Embodiments include the above and wherein said plurality of zones of said wafer TI layer correspond to a die layout of said wafer DUT and wherein further said wafer TI layer is customized for said wafer DUT. Embodiments include the above and wherein each zone of said plurality of zones corresponds to a respective single die of said die layout of said wafer DUT. Embodiments include the above and wherein each zone of said plurality of zones corresponds to a respective plurality of die of said die layout of said wafer DUT. Embodiments include the above and wherein each die of said die layout of said wafer DUT corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.

[0017] Embodiments include the above and further comprising a pin lift mechanism for displacing pins for lifting said wafer DUT away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical pass through channels which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer DUT. Embodiments include the above and wherein: said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and operable to selectively heat a plurality of zones of said wafer TI layer responsive to said PWM signals; and said wafer TI layer comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said

grounded shield layer operable for protecting said wafer DUT from EMI radiation resultant from said PWM signals applied to said plurality of traces.

[0018] Embodiments are also drawn to a system for testing circuits of an integrated circuit semiconductor wafer device under test (DUT), the system comprising: a tester system for generating signals for input to said circuits and for processing output signals from said circuits for testing said wafer DUT; a test stack coupled to said tester system, said test stack comprising: a wafer probe for contacting a top surface of said wafer DUT and for probing individual circuits of said circuits of said wafer DUT; a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer DUT and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer DUT; and a cold plate disposed under said wafer TI layer and operable to cool said wafer DUT; and a thermal controller for selectively heating and maintaining temperatures of areas of said wafer DUT by controlling cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer.

[0019] Embodiments include the above and wherein said wafer DUT comprises a die layout comprising a plurality of die and wherein further said plurality of discretely controllable thermal zones is customized to said die

layout of said wafer DUT. Embodiments include the above and wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to multiple die of said die layout of said wafer DUT. Embodiments include the above and wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to a single die of said die layout of said wafer DUT. Embodiments include the above and wherein each die of said die layout of said wafer DUT corresponds to multiple thermal zones of said plurality of discretely controllable thermal zones of said wafer TI layer.

[0020] Embodiments include the above and wherein said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and operable to selectively heat and maintain temperatures of said plurality of discretely controllable thermal zones of said wafer TI layer responsive to said thermal controller. Embodiments include the above and wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and while said tester system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones

to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

[0021] Embodiments include the above and wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and while said tester system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

[0022] Embodiments are drawn to a method for testing circuits of an integrated circuit semiconductor wafer device under test (DUT), the method comprising: testing said circuits of said wafer DUT by using a tester system to generate signals for input to said circuits and to process output signals from said circuits; and in conjunction with said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer DUT by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of said wafer DUT and wherein said

thermal interposer device comprises a plurality of separately controllable thermal zones wherein each thermal zone is operable to be selectively heated and temperature maintained by said thermal controller.

[0023] Embodiments include the above and wherein said wafer DUT comprises a die layout and wherein further said plurality of separately controllable thermal zones of said thermal interposer device layer is customized to said die layout. Embodiments include the above and wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer DUT by using a thermal controller comprises: bringing a first thermal zone of said plurality of separately controllable thermal zones to a testing temperature; and while said tester system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of separately controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

[0024] Embodiments include the above and wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer DUT by using a thermal controller comprises: bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and while said tester system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously

bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. Unless otherwise noted, the drawings may not be drawn to scale.

[0026] Figure 1 illustrates an exemplary block diagram of elements of an automated test system environment that may serve as a platform for embodiments in accordance with the present invention.

[0027] Figure 2 illustrates an exemplary block diagram cross sectional view of a novel wafer scale active thermal interposer device, in accordance with embodiments of the present invention.

[0028] Figure 3 illustrates an exemplary block diagram of elements of an automated test system environment including a wafer scale active thermal interposer device, in accordance with embodiments of with the present invention.

[0029] Figure 4 illustrates an exemplary plan view of an exemplary layout 400 of controllable regions of a wafer scale active thermal interposer device

and an associated exemplary wafer, in accordance with embodiments of the present invention.

[0030] Figure 5 illustrates an exemplary plan view layout of controllable regions of a wafer scale active thermal interposer device and an associated wafer 520, in accordance with embodiments of the present invention.

[0031] Figure 6 illustrates an exemplary plan view layout of controllable regions of a wafer scale active thermal interposer device and an associated wafer, in accordance with embodiments of the present invention.

[0032] Figure 7A illustrates an exemplary computer controller process for testing circuits of an integrated circuit semiconductor wafer comprising multiple integrated circuit dice using a wafer scale active thermal interposer device, in accordance with embodiments of the present invention.

[0033] Figure 7B illustrates an exemplary computer controlled method for testing circuits of an integrated circuit semiconductor wafer using a wafer scale active thermal interposer device, in accordance with embodiments of the present invention.

[0034] Figure 8 illustrates a block diagram of an exemplary electronic system, which may be used as a platform to implement and/or as a control system for

embodiments of the present invention.

DETAILED DESCRIPTION

[0035] Reference will now be made in detail to various embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with these embodiments, it is understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the invention, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be recognized by one of ordinary skill in the art that the invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the invention.

[0036] Some portions of the detailed descriptions which follow (e.g., process 700) are presented in terms of procedures, steps, logic blocks, processing, and other symbolic representations of operations on data bits that may be performed on computer memory. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. A procedure, computer executed step, logic block, process, etc., is here, and generally,

conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, data, or the like.

[0037] It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present invention, discussions utilizing terms such as "testing" or "heating" or "maintaining temperature" or "bringing" or "capturing" or "storing" or "reading" or "analyzing" or "generating" or "resolving" or "accepting" or "selecting" or "determining" or "displaying" or "presenting" or "computing" or "sending" or "receiving" or "reducing" or "detecting" or "setting" or "accessing" or "placing" or "testing" or "forming" or "mounting" or "removing" or "ceasing" or "stopping" or "coating" or "processing" or "performing" or "generating" or "adjusting" or "creating" or "executing" or "continuing" or "indexing" or "translating" or "calculating" or "measuring" or "gathering" or "running" or the like, refer to the action and

processes of, or under the control of, a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

[0038] The meaning of "non-transitory computer-readable medium" should be construed to exclude only those types of transitory computer-readable media which were found to fall outside the scope of patentable subject matter under 35 U.S.C. § 101 in *In re Nuijten*, 500 F.3d 1346, 1356-57 (Fed. Cir. 1007). The use of this term is to be understood to remove only propagating transitory signals *per se* from the claim scope and does not relinquish rights to all standard computer-readable media that are not only propagating transitory signals *per se*.

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

[0039] Figure 1 illustrates an exemplary block diagram of elements of an automated test system environment 100, which utilizes a wafer scale active thermal interposer device, that may serve as a platform for embodiments in accordance with the present invention. Test system 100 receives and tests a

semiconductor wafer 120, for example comprising a plurality of integrated circuit devices or dice. A wafer probe card 110 is coupled to wafer 120, e.g., utilizing test pads formed on the wafer 120, to send and receive test signals and power to integrated circuit devices embodied within or on wafer 120. Wafer probe card 110 is typically electronically coupled to, and tests, a single die of wafer 120 at a time, although that is not required.

[0040] In accordance with embodiments of the present invention, a novel wafer scale active thermal interposer device 130 is coupled to the backside of wafer 120. Wafer scale active thermal interposer device 130 may be customized for a specific design of wafer 120, in some embodiments. In some embodiments, there may be a thermal interface material (not shown, see Figure 3) disposed between wafer scale active thermal interposer device 130 and wafer 120. Such a thermal interface material, if present, is designed to improve thermal coupling between wafer scale active thermal interposer device 130 and wafer 120.

[0041] In some embodiments, wafer scale active thermal interposer device 130 may comprise a base layer of aluminum nitride (AlN) with tungsten and/or molybdenum traces. A high temperature co-fired ceramic (HTCC) process may be utilized. Such embodiments may be suitable for testing comparatively higher power devices. In some embodiments, a low temperature co-fired ceramic (LTCC) process, e.g., comprising aluminum

oxide (Al_20_3) may be utilized. Such embodiments may be suitable for testing comparatively lower power devices.

[0042] Wafer scale active thermal interposer device 130 is further coupled to a cold plate 140. In some embodiments, there may be a thermal interface material (not shown) disposed between wafer scale active thermal interposer device 130 and cold plate 140. Such a thermal interface material, if present, is designed to improve thermal coupling between wafer scale active thermal interposer device 130 and cold plate 140.

[0043] In an embodiment, a cooling fluid, e.g., comprising glycol, although other fluids, including air, may be used, is generally circulated through cold plate 140. To adjust the temperature of the cold plate 140, the temperature of the cooling fluid may be adjusted, in some embodiments. In some embodiments, as illustrated in Figure 1, the flow rate of the cooling fluid may also be adjusted, e.g., increased, reduced, started, and/or stopped. For example, a speed of a pump and/or fan may be adjusted. In an embodiment, chiller 160 cools the cooling fluid, e.g., to -60 degrees C. The cooling fluid flows through 161 to valve 150. Valve 150, under the control of thermal controller 180, regulates the flow 151 of cooling fluid to cold plate 140. After cycling through cold plate 140, the cooling fluid is returned 141 to the chiller 160. In this manner, thermal controller 180 may cool wafer 120 during testing via cooling action from chiller 160 and the cold plate 140.

[0044] In accordance with embodiments of the present invention, thermal controller 180 may implement some or all of the control processes described in U.S. Patent No. 9,291,667 entitled "Adaptive Thermal Control," incorporated herein by reference in its entirety.

[0045] In some embodiments, cold plate 140 may comprise an evaporator and/or phase change cooling system. In such embodiments, chiller 160 may comprise a compressor and/or radiator, for example.

[0046] Wafer scale active thermal interposer device 130 functions to apply heat energy to one or more temperature regions of wafer 120. There temperature regions may correspond, in location and shape, with the dice on the wafer 120. To accomplish such heating, wafer scale active thermal interposer device 130 comprises one or more heating elements, as further described below. The heating elements of wafer scale active thermal interposer device 130 correspond to the temperature regions of wafer 120. In some embodiments, the heating elements comprise resistive traces on a ceramic substrate. In some embodiments, the heating elements may be Peltier devices, capable of cooling as well. However, any suitable heating and/or cooling technology is well suited to embodiments in accordance with the present invention. Wafer scale active thermal interposer device 130 also functions to couple heat energy from wafer 120 to cold plate 140 for cooling.

[0047] Wafer scale active thermal interposer device 130 further comprises a plurality of temperature measurement devices, e.g., thermocouples. The plurality of temperature measurement devices are configured to measure temperatures of regions of wafer 120. The plurality of temperature measurement devices may be located within or in close proximity to the heating elements of wafer scale active thermal interposer device 130. In some embodiments, wafer scale active thermal interposer device 130 may comprise temperature measurement devices characterized as not within or in close proximity to the heating elements of wafer scale active thermal interposer device 130. Each of the plurality of temperature measurement devices sends a temperature signal 131 to thermal controller 180. Wafer probe card 110, wafer 120, wafer scale active thermal interposer device 130, and cold plate 140 may be collectively known as or referred to as a test stack or test head when coupled together as illustrated in Figure 1.

[0048] Test system 100 further comprises a thermal controller 180. Thermal controller 180 is an intelligent device and sends control signals 182 to power supply 170 to supply electrical power 171 to one or more heating elements of wafer scale active thermal interposer device 130. Each heating element of wafer scale active thermal interposer device 130 may be individually controlled. Accordingly, there are typically more power signals 171 than illustrated. There may be more than one power supply, in some

embodiments. Based on temperature feedback 131 from one or more of the plurality of temperature measurement devices, thermal controller 180 may control power supply 170 to change the power supplied to a heating element. Power supply 170 may change a voltage level and/or pulse width modulate a voltage supplied to a heating element to control heating of the heating element, in some embodiments. Thermal controller 180 also controls the amount of heat energy extracted 141 from cold plate 140. For example, thermal controller 180 controls the temperature of cold plate 140. Thermal controller 180 controls valve 150 based on temperature feedback 131.

[0049] It is to be appreciated that cold plate 140 extracts heat, through wafer scale active thermal interposer device 130, from substantially all of wafer 120. In addition, cold plate 140 typically has a large thermal mass, and does not change temperature quickly. Accordingly, heating elements of wafer scale active thermal interposer device 130 may often be required to overcome the cooling effect of cold plate 140. In some embodiments, different regions of a wafer 120 may be heated and/or cooled to different temperatures based on the selective heating capability of the heaters of the wafer scale active thermal interposer device 10 and the cooling function of cold plate 140. For example, one region of wafer 120 may be heated to 100 degrees C, e.g., via a heater element within wafer scale active thermal interposer device 130, while another region of wafer 120 may be allowed to cool toward the temperature of cold plate 140 with no heat applied to such region by wafer scale active

thermal interposer device 130. Such differential heating and/or cooling of different regions of wafer 120 may produce a thermal gradient across or between regions of wafer 120, in some embodiments.

[0050] Figure 2 illustrates an exemplary block diagram cross sectional view of a novel wafer scale active thermal interposer device 200, in accordance with embodiments of the present invention. Wafer scale active thermal interposer device 200 comprises a heating element layer 250. Heating element layer 250 comprises a plurality of discrete and separately controllable heating elements configured to apply heat energy to a wafer (not shown). The heating elements may comprise resistive traces or other suitable types of heaters. The plurality of heating elements are coupled to a plurality of electrical signals 255, for providing controlled power to the heating elements such that the elements are separately controllable. Heating element layer 250 may include low resistance traces, e.g., from electrical signals 255 to the actual heating elements, in some embodiments. Heating element layer 250 also comprises a plurality of temperature measurement devices, e.g., thermocouples, (not shown), which are coupled to control elements via temperature a plurality of sense signals 252.

[0051] In accordance with embodiments of the present invention, wafer scale active thermal interposer device 200 may comprise a novel electromagnetic interference (EMI) shield layer 220 to address signal interference caused by

the heater elements. Each of the plurality of heating elements in layer 250 may utilize currents of many tens of amperes. In embodiments of the present invention that utilize switching such currents to control temperature, e.g., pulse width modulation, such switching may induce unwanted electromagnetic noise signals that are deleterious to the operation and/or test of integrated circuits on a wafer, e.g., wafer 120 of Figure 1, coupled to the wafer scale active thermal interposer device 200. In some embodiments, EMI shield layer 220 comprises a solid layer of conductor, e.g., conductive traces similar to those utilized in heating element layer 250. In some embodiments, EMI shield layer 220 comprises a grid of conductive elements. The grid may be sized to attenuate desired wavelength(s) of electromagnetic interference. EMI shield layer 220 may have an electrical connection 225, e.g., to ground, in some embodiments.

[0052] Wafer scale active thermal interposer device 200 comprises a top thermal layer 240. Thermal layer 240 functions to couple heat energy from heating element layer 250 to a wafer under test and vice versa. Thermal layer 240 is non conductive, in some embodiments. Thermal layer 240 should have a high degree of co-planarity in order to facilitate good thermal conduction to a wafer and to promote good vacuum hold down of the wafer, in some embodiments.

[0053] Wafer scale active thermal interposer device 200 is compatible and complementary with conventional elements of wafer scale test equipment. Accordingly, in some embodiments, wafer scale active thermal interposer device 200 may comprise one or more wafer vacuum line passthrough ports 215. Wafer vacuum line passthrough ports 215 couple to one or more conventional vacuum lines, as is typically used to hold down a wafer in place during testing. For example, wafer vacuum line passthrough port 215 mates with a vacuum port of a conventional cold plate, e.g., cold plate 140 of Figure 1. There may be a plurality of wafer vacuum line passthrough ports 215 in an instance of wafer scale active thermal interposer device 200, for example three arranged in an equilateral triangle, in some embodiments. A wafer vacuum line passthrough port 215 typically extends through wafer scale active thermal interposer device 200.

[0054] In some embodiments, wafer scale active thermal interposer device 200 may comprise one or more wafer blowoff line passthrough ports 221. Wafer blowoff line passthrough port 221 couples to a conventional wafer blowoff line, as is typically used to break a vacuum seal of a wafer, prior to removing the wafer from the test system. For example, wafer blowoff line passthrough port 221 mates with a wafer blowoff line port of a conventional cold plate, e.g., cold plate 140 of Figure 1. There may be a plurality of wafer blowoff line passthrough ports 221 in an instance of wafer scale active thermal interposer device 200, for example three arranged in an equilateral triangle, in some

embodiments. A wafer blowoff line passthrough port 221 typically extends through wafer scale active thermal interposer device 200.

[0055] Wafer scale active thermal interposer device 200 may also comprise a wafer pin lift port 230, in some embodiments. Wafer pin lift port 230 may be aligned with a similar port or channel in a cold plate, e.g., cold plate 140 of Figure 1. Wafer pin lift port 230 enables a wafer lift pin 235 to raise a wafer above the top of the wafer scale active thermal interposer device 200. For example, wafer handling equipment typically needs a gap under a wafer in order to lift the wafer and move the wafer to another station in a wafer manufacturing and test process. The wafer lift pin 235 typically extends from or through a cold plate, e.g., cold plate 140 of Figure 1, and/or from a chuck mechanism (not shown). In accordance with some embodiments of the present invention, the wafer lift pin 235 may be lengthened, in contrast to a conventional lift pin, to account for the thickness of wafer scale active thermal interposer device 200. There may be a plurality of wafer pin lift ports 230 in an instance of wafer scale active thermal interposer device 200, for example three arranged in an equilateral triangle, in some embodiments. A wafer pin lift port 230 typically extends through wafer scale active thermal interposer device 200.

[0056] With respect to the wafer scale active thermal interposer device 200, wafer vacuum line passthrough ports 215, wafer blowoff line passthrough

ports 221 and/or wafer pin lift ports 230 may be combined in any suitable combination, in accordance with embodiments of the present invention. For example, a wafer vacuum line passthrough ports 215 may be combined with a wafer blowoff line passthrough port 221.

[0057] Figure 3 illustrates an exemplary block diagram of elements of an automated test system environment 300 including a wafer scale active thermal interposer device, in accordance with embodiments of with the present invention. Figure 3 illustrates functional components of a wafer vacuum hold down and blowoff systems in combination with wafer scale active thermal interposer device 130.

[0058] Test system environment 300 comprises a vacuum pump 330 coupled to wafer vacuum valve 310 and wafer scale active thermal interposer (ATI) vacuum valve 320. Wafer vacuum valve 310 is coupled to wafer vacuum/blowoff line passthrough port 315 of wafer scale active thermal interposer device 130. In the illustrated embodiment, the vacuum passthrough and blowoff passthrough ports are combined, although this is not required and such ports may be separate. To hold down a wafer 120 prior to and during test, wafer vacuum valve 310 is opened, enabling a pressure differential between ambient atmosphere and vacuum to hold down the wafer 120 to the wafer scale active thermal interposer device 130.

[0059] ATI vacuum valve 320 is coupled to ATI vacuum/blowoff line passthrough port 316 of cold plate 140. To hold down ATI 130 prior to and during test, ATI vacuum valve 320 is opened, enabling a pressure differential between ambient atmosphere and/or ATI 130 and vacuum to hold down the ATI 130 to the cold plate 140.

[0060] Compressed dry air source (CDA) 360 is coupled to wafer CDA blowoff valve 340 and to ATI CDA blowoff valve 350. To blow the wafer off of the ATI 130, the wafer vacuum valve 310 is closed and the wafer CDA blowoff valve 340 is opened, coupling compressed dry air through the vacuum/blowoff line passthrough port 315 to break the prior vacuum seal. To remove the wafer scale active thermal interposer device 130 from the cold plate 140, for example, to change to a different wafer scale thermal interposer, the ATI vacuum valve 320 is closed and the ATI CDA blowoff valve 350 is opened, coupling compressed dry air through the ATI vacuum/blowoff line passthrough port 316 to break the prior vacuum seal.

[0061] In accordance with embodiments of the present invention, test system 300 may comprise a thermal interface material (TIM) 370 disposed at the ATI/wafer interface and/or a thermal interface material 380 disposed at the ATI/cold plate interface. The thermal interface material is operable to provide thermal coupling, e.g., has a high thermal conductance, and provides mechanical compliance to compensate for irregularities in the adjoining

surfaces. The thermal interface material may be considered to be separate from the wafer scale active thermal interposer device 130, in some embodiments. For example, a thermal interface material 370 may be applied to the wafer scale active thermal interposer device 130 after the wafer scale active thermal interposer device 130 is placed in the test system 300. Any suitable thermal interface material may be used, including those comprising indium foil and/or carbon nanotubes, in accordance with embodiments of the present invention. Thermal interface material 370 may differ from thermal interface material 380 in composition and/or thickness, in some embodiments.

[0062] Figure 4 illustrates an exemplary plan view layout of an exemplary layout 400 of controllable regions of a wafer scale active thermal interposer device 430 and an associated exemplary wafer 420, in accordance with embodiments of the present invention. The wafer scale active thermal interposer device 430 generally corresponds to wafer scale active thermal interposer device 130 as previously described in Figures 1, 2, and 3. The wafer scale active thermal interposer device 430 is configured to be used in testing of wafer 420.

[0063] Wafer 420 comprises a plurality of discrete dice 410. Dice 410 may be characterized as relatively small and/or designed to operate at relatively low power levels. Examples of such integrated circuits may include

microcontrollers, dynamic RAMs, application-specific integrated circuits, and the like. Due to their small size and/or low power operational characteristics, such integrated circuits may not require application of large amounts of heat energy to achieve desired test temperatures. In addition, small integrated circuit die may be physically smaller than a desired minimum size of a heating element as used in wafer scale active thermal interposer device 430.

[0064] Wafer scale active thermal interposer device 430 comprises a plurality of selective heatable regions 441, 442, 443, 444, 445, 446, 447, 448 and 449. The number of heatable regions and their layout is exemplary, and may be customized to the die layout of the wafer 420. Wafer scale active thermal interposer device 430 is configured to heat and/or cool portions of wafer 420 corresponding to one or more of the selective heatable regions 441, 442, 443, 444, 445, 446, 447, 448 and 449. In accordance with embodiments of the present invention, each heatable region of wafer scale active thermal interposer device 430 corresponds to more than one die of wafer 420. For example, heatable region 449 of wafer scale active thermal interposer device 430 is configured to selectively apply heat energy to approximately nine dice of wafer 420 when coupled to wafer 420 in a test system.

[0065] Figure 5 illustrates an exemplary plan view layout 500 of controllable regions of an exemplary wafer scale active thermal interposer device 530 and an associated exemplary wafer 520, in accordance with embodiments of the

present invention. The wafer scale active thermal interposer device 530 generally corresponds to wafer scale active thermal interposer device 130 as previously described in Figures 1, 2, and 3. The wafer scale active thermal interposer device 530 is configured to be used in testing of wafer 520.

[0066] Wafer 520 comprises a plurality of dice 510. Dice 510 may be characterized as relatively large and/or designed to operate at relatively high power levels. Examples of such integrated circuits may include central processing units (CPUs), graphics processing units (GPUs), Network Processing Units (NPUs), multi-core processing units, power semiconductors, and the like. Due to their large size and/or high power operational characteristics, such integrated circuits may require application of large amounts of heat energy to achieve desired test temperatures.

[0067] Wafer scale active thermal interposer device 530 comprises a plurality of selectable heatable regions 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, and 543. The number of heatable regions and their layout is exemplary. Wafer scale active thermal interposer device 530 is configured to heat and/or cool portions of wafer 520 corresponding to one or more of the heatable regions 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, and 543. In accordance with embodiments of the present invention, each heatable region of wafer scale active thermal interposer device 530 corresponds to one die of wafer 520 in location and shape. For example,

heatable region 542 of wafer scale active thermal interposer device 530 is configured to selectively apply heat energy to die 512 of wafer 520 when coupled to wafer 520 in a test system. In this novel manner, wafer scale active thermal interposer device 530 may selectively apply sufficient heat energy to large and/or high-power die to achieve desired test temperatures while in wafer form. The discrete dice of the wafer 520 may be selectively heated during testing by the discrete and separately controller heating elements of the wafer scale active thermal interposer device 530.

[0068] Figure 6 illustrates an exemplary plan view layout 600 of controllable regions of a wafer scale active thermal interposer device 630 and an associated wafer 620, in accordance with embodiments of the present invention. The wafer scale active thermal interposer device 630 generally corresponds to wafer scale active thermal interposer device 130 as previously described in Figures 1, 2, and 3. The wafer scale active thermal interposer device 630 is configured to be used in testing of wafer 620.

[0069] Wafer 620 comprises a plurality of dice 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, and 613. Dice 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, and 613 may be characterized as relatively large and/or designed to operate at relatively high power levels. Examples of such integrated circuits may include central processing units (CPUs), graphics processing units (GPUs), Network Processing Units (NPUs), multi-core

processing units, power semiconductors, and the like. Due to their large size and/or high power operational characteristics, such integrated circuits may require application of large amounts of heat energy to achieve desired test temperatures.

[0070] Large and complex integrated circuits frequently comprise a plurality of functional units, e.g., multiple processing cores, which are physically distinct. It may be desirable to test such functional units in whole or in partial isolation from other function units of a die. For example, a GPU comprising multiple floating point units may be designed to utilize a single floating point unit at times during operation, and turn off other floating point units, e.g., those that are not currently required, in order to reduce power consumption. It may be desirable to test the GPU under similar thermal conditions. For example, it may be desirable to run functional tests on a portion of the GPU corresponding to an operational floating point unit at a high temperature, while other portions of the GPU are at a different, e.g., lower, temperature, simulating non-operation.

[0071] In addition, the heat energy required to achieve a desirable test temperature for large and/or high powered die may exceed the capacity of a single heating element of a wafer scale thermal interposer. For example, conductive traces of a wafer scale thermal interposer may have current capacity limitations. Further, other components of a single heating element

and/or a wafer scale thermal interposer may limit an amount of heat energy generated to be less that required to supply sufficient heat energy to achieve a desired temperature of a die under test.

[0072] Wafer scale active thermal interposer device 630 comprises a plurality of heatable regions, e.g., heatable regions 641, 642, 643, and 644. The number of heatable regions and their layout is exemplary. Wafer scale active thermal interposer device 630 is configured to selectively heat and/or cool portions of wafer 620 corresponding to one or more of the heatable regions 641, 642, 643, and 644. In accordance with embodiments of the present invention, each heatable region of wafer scale active thermal interposer device 630 corresponds to a portion of one die of wafer 620. For example, heatable region 642 of wafer scale active thermal interposer device 630 is configured to selectively apply heat energy to the right upper quadrant of die 612 of wafer 620 when coupled to wafer 620 in a test system. In this novel manner, wafer scale active thermal interposer device 630 may selectively apply sufficient heat energy to portions of large and/or high-power die to achieve desired test temperatures, including different temperatures within a single die, while in wafer form.

[0073] In accordance with embodiments of the present invention, areas of a wafer, e.g., wafer 620 of Figure 6, which are not under test may nevertheless be opportunistically preconditioned to a desirable temperature. For example,

while testing die 612 (Figure 6) at a desired testing temperature, embodiments in accordance with the present invention may bring die 609 to a desired test temperature while die 609 is not being tested, e.g., prior to testing die 609. It is appreciated that semiconductor die have a thermal mass, and do not change temperature instantaneously. In this novel manner, a plurality of die may be opportunistically preconditioned to a desirable temperature, e.g., in advance of their testing, to increase testing throughput. Such opportunistic temperature preconditioning may beneficially increase a rate of testing of multiple dice, for example, by eliminating a time delay between testing of a first and a second die required to bring the second die, or portion thereof, to a desirable test temperature.

[0074] Figure 7A illustrates an exemplary computer controller process 700 for testing circuits of an integrated circuit semiconductor wafer comprising multiple integrated circuit dice using a wafer scale active thermal interposer device, in accordance with embodiments of the present invention. In 705, a wafer comprising multiple dice for testing is received for testing, e.g., within an automated test equipment, for example, automated test environment 100 of Figure 1.

[0075] In 710, a wafer, e.g., wafer 120 of Figure 1, is placed in contact with a wafer scale active thermal interposer device, e.g., wafer scale active thermal interposer device 130 (Figure 1). In 715, circuit testing is performed on the

wafer by electrically contacting dice of the wafer to apply testing signals thereto and to receive test output signals from the dice.

[0076] In 720, while performing the circuit testing, the temperature of dice under test is controlled by: 1) selectively controlling the heating of a plurality of heater elements within the wafer scale active thermal interposer device, wherein the plurality of heater elements correspond to a plurality of dice within the wafer under test; and 2) selectively controlling cooling of the cold plate. In optional 725, the results of the circuit testing are recorded.

[0077] Figure 7B illustrates an exemplary computer controlled method 750 for testing circuits of an integrated circuit semiconductor wafer using a wafer scale active thermal interposer device, in accordance with embodiments of the present invention. In 755, the circuits of a wafer are tested by using a tester system to generate signals for input to the circuits and to process output signals from the circuits.

[0078] In 760, in conjunction with the testing, a plurality of areas of the wafer are selectively heated and have their temperatures maintained by using a thermal controller selectively controlling discrete heater elements of a thermal interposer layer and a cold plate, both disposed in proximity of the wafer. The thermal interposer comprises a plurality of separately controllable thermal zones wherein each thermal zone is operable to be

selectively heated and temperature maintained by the thermal controller. The thermal zones may correspond in location and shape to dice on the wafer being tested. The selective heating may include bringing a first set of thermal zones of the plurality of separately controllable thermal zones to a testing temperature while the tester system is testing a first die of the die layout corresponding to the first set of thermal zones, simultaneously and opportunistically bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of the die layout corresponding to the second set of thermal zones.

[0079] In optional 765, a first thermal zone of the plurality of separately controllable thermal zones is brought to a testing temperature. In optional 770, a second thermal zone of the plurality of separately controllable thermal zones to is simultaneously brought to a testing temperature in advance of testing one or more die of the die layout corresponding to the second thermal zone, while the tester system is testing one or more die of the die layout corresponding to the first thermal zone. In optional 775, one or more die of the die layout corresponding to the second thermal zone are tested.

[0080] Figure 8 illustrates a block diagram of an exemplary electronic system 800, which may be used as a platform to implement and/or as a control system for embodiments of the present invention. Electronic system 800 may

be a "server" computer system, in some embodiments. Electronic system 800 includes an address/data bus 850 for communicating information, a central processor complex 805 functionally coupled with the bus for processing information and instructions. Bus 850 may comprise, for example, a Peripheral Component Interconnect Express (PCIe) computer expansion bus, industry standard architecture (ISA), extended ISA (EISA), MicroChannel, Multibus, IEEE 796, IEEE 1196, IEEE 1496, PCI, Computer Automated Measurement and Control (CAMAC), MBus, Runway bus, Compute Express Link (CXL), and the like.

[0081] Central processor complex 805 may comprise a single processor or multiple processors, e.g., a multi-core processor, or multiple separate processors, in some embodiments. Central processor complex 805 may comprise various types of well known processors in any combination, including, for example, digital signal processors (DSP), graphics processors (GPU), complex instruction set (CISC) processors, reduced instruction set (RISC) processors, and/or very long word instruction set (VLIW) processors. Electronic system 800 may also includes a volatile memory 815 (e.g., random access memory RAM) coupled with the bus 850 for storing information and instructions for the central processor complex 805, and a non-volatile memory 810 (e.g., read only memory ROM) coupled with the bus 850 for storing static information and instructions for the processor complex 805. Electronic system 800 also optionally includes a changeable, non-volatile memory 820

(e.g., NOR flash) for storing information and instructions for the central processor complex 805 which can be updated after the manufacture of system 800. In some embodiments, only one of ROM 810 or Flash 820 may be present.

[0082] Also included in electronic system 800 of Figure 8 is an optional input device 830. Device 830 can communicate information and command selections to the central processor 800. Input device 830 may be any suitable device for communicating information and/or commands to the electronic system 800. For example, input device 830 may take the form of a keyboard, buttons, a joystick, a track ball, an audio transducer, e.g., a microphone, a touch sensitive digitizer panel, eyeball scanner, and/or the like.

[0083] Electronic system 800 may comprise a display unit 825. Display unit 825 may comprise a liquid crystal display (LCD) device, cathode ray tube (CRT), field emission device (FED, also called flat panel CRT), light emitting diode (LED), plasma display device, electro-luminescent display, electronic paper, electronic ink (e-ink) or other display device suitable for creating graphic images and/or alphanumeric characters recognizable to the user. Display unit 825 may have an associated lighting device, in some embodiments.

[0084] Electronic system 800 also optionally includes an expansion interface 835 coupled with the bus 850. Expansion interface 835 can implement many well known standard expansion interfaces, including without limitation the Secure Digital Card interface, universal serial bus (USB) interface, Compact Flash, Personal Computer (PC) Card interface, CardBus, Peripheral Component Interconnect (PCI) interface, Peripheral Component Interconnect Express(PCI Express), mini-PCI interface, IEEE 8394, Small Computer System Interface (SCSI), Personal Computer Memory Card International Association (PCMCIA) interface, Industry Standard Architecture (ISA) interface, RS-232 interface, and/or the like. In some embodiments of the present invention, expansion interface 835 may comprise signals substantially compliant with the signals of bus 850.

[0085] A wide variety of well-known devices may be attached to electronic system 800 via the bus 850 and/or expansion interface 835. Examples of such devices include without limitation rotating magnetic memory devices, flash memory devices, digital cameras, wireless communication modules, digital audio players, and Global Positioning System (GPS) devices.

[0086] System 800 also optionally includes a communication port 840. Communication port 840 may be implemented as part of expansion interface 835. When implemented as a separate interface, communication port 840 may typically be used to exchange information with other devices via

communication-oriented data transfer protocols. Examples of communication ports include without limitation RS-232 ports, universal asynchronous receiver transmitters (UARTs), USB ports, infrared light transceivers, ethernet ports, IEEE 8394, and synchronous ports.

[0087] System 800 optionally includes a network interface 860, which may implement a wired or wireless network interface. Electronic system 800 may comprise additional software and/or hardware features (not shown) in some embodiments.

[0088] Various modules of system 800 may access computer readable media, and the term is known or understood to include removable media, for example, Secure Digital ("SD") cards, CD and/or DVD ROMs, diskettes and the like, as well as non-removable or internal media, for example, hard drives, solid state drive s (SSD), RAM, ROM, flash, and the like.

[0089] Embodiments in accordance with the present invention provide systems and methods for wafer scale active thermal interposer devices. In addition, embodiments in accordance with the present invention provide systems and methods for wafer scale active thermal interposer devices operable to control different portions of a wafer to different temperatures. Further, embodiments in accordance with the present invention provide systems and methods for wafer scale active thermal interposer devices that

are compatible and complementary with existing systems and methods of testing integrated circuits.

[0090] Various embodiments of the invention are thus described. While the present invention has been described in particular embodiments, it should be appreciated that the invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

CLAIMS

We Claim:

1. A system for testing circuits of an integrated circuit semiconductor wafer, the system comprising:

a tester system for generating signals for input to said circuits and for processing output signals from said circuits for testing said wafer;

a test stack coupled to said tester system, said test stack comprising:

a wafer probe for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer;

a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer; and

a cold plate disposed under said wafer TI layer and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer by controlling cooling of said cold plate and by controlling selective heating of said wafer TI layer.

2. The system as described in Claim 1 further comprising a power supply coupled to provide power to said wafer TI layer and controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said sekective heating of said wafer TI layer is based on said PWM signals.

3. The system as described in Claim 2 further comprising:

a chiller for cooling liquid;

a valve for controlling an amount of said liquid flowing to said cold plate, wherein said valve is controlled by said thermal controller.

4. The system as described in Claim 1 further comprising:

a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and

a second TIM layer disposed between said wafer TI layer and said wafer.

5. The system as described in Claim 4 wherein said first and second TIM layers comprise indium foil.

6. The system as described in Claim 4 further comprising:

a first vacuum valve for establishing suction for securing said wafer to said wafer TI layer;

a second vacuum valve for establishing suction for securing said wafer TI layer to said cold plate; and

a vacuum pump coupled to both said first and second vacuum valves.

7. The system as described in Claim 6 further comprising:

a first blow-off valve for controlling air to release said wafer from said wafer TI layer;

a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and

a source of air coupled to both said first and second blow-off valves.

8. The system as described in Claim 1 wherein said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and wherein said plurality of traces are operable to selectively heat a plurality of zones of said wafer TI layer under control of said thermal controller and wherein further said plurality of zones correspond to said areas of said wafer.

9. The system as described in Claim 8 wherein positions of said plurality of zones of said wafer TI layer correspond to a die layout of said wafer and wherein further said wafer TI layer is customized for said wafer.

10. The system as described in Claim 9 wherein each zone of said plurality of zones corresponds to a respective single die of said die layout of said wafer.

11. The system as described in Claim 9 wherein each zone of said plurality of zones corresponds to a respective plurality of dice of said die layout of said wafer.

12. The system as described in Claim 9 wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.

13. The system as described in Claim 1 further comprising a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical pass through channels which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer.

14. The system as described in Claim 2 wherein:

said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and operable to selectively heat a plurality of zones of said wafer TI layer responsive to said PWM signals; and

said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from said PWM signals applied to said plurality of traces.

15. A system for testing circuits of an integrated circuit semiconductor wafer, the system comprising:

a tester system for generating signals for input to said circuits and for processing output signals from said circuits for testing said wafer;

a test stack coupled to said tester system, said test stack comprising:

a wafer probe for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer;

a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer; and

a cold plate disposed under said wafer TI layer and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of areas of said wafer by controlling cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer.

16. A system as described in Claim 15 wherein said wafer comprises a die layout comprising a plurality of dice and wherein further positions and shapes of said plurality of discretely controllable thermal zones are customized to said die layout of said wafer.

17. A system as described in Claim 16 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to multiple dice of said die layout of said wafer.

18. A system as described in Claim 16 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to a single die of said die layout of said wafer.

19. A system as described in Claim 16 wherein each die of said die layout of said wafer corresponds to multiple thermal zones of said plurality of discretely controllable thermal zones of said wafer TI layer.

20. The system as described in Claim 16 wherein said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and operable to selectively heat and maintain temperatures of said plurality of discretely controllable thermal zones of said wafer TI layer responsive to said thermal controller.

21. The system as described in Claim 16 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and

while said tester system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

22. The system as described in Claim 16 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and

while said tester system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

23. A method for testing circuits of an integrated circuit semiconductor wafer, the method comprising:

testing said circuits of said wafer by using a tester system to generate signals for input to said circuits and to process output signals from said circuits; and

in conjunction with performing said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of said wafer and wherein said thermal interposer comprises a plurality of separately controllable thermal zones wherein each thermal zone is operable to be selectively heated and temperature maintained by said thermal controller.

24. A method as described in Claim 23 wherein said wafer comprises a die layout and wherein further positions and shapes of said plurality of separately controllable thermal zones of said thermal interposer layer are customized to said die layout.

25. The method as described in Claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises:

bringing a first thermal zone of said plurality of separately controllable thermal zones to a testing temperature; and

while said tester system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second

thermal zone of said plurality of separately controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

26. The method as described in Claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises:

bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and

while said tester system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

ABSTRACT OF THE DISCLOSURE

A system for testing circuits of an integrated circuit semiconductor wafer includes a tester system for generating signals for input to the circuits and for processing output signals from the circuits for testing the wafer and a test stack coupled to the tester system. The test stack includes a wafer probe for contacting a first surface of the wafer and for probing individual circuits of the circuits of the wafer, a wafer thermal interposer (TI) layer operable to contact a second surface of the wafer and operable to selectively heat areas of the wafer, and a cold plate disposed under the wafer TI layer and operable to cool the wafer. The system further includes a thermal controller for selectively heating and maintaining temperatures of the areas of the wafer by controlling cooling of the cold plate and by controlling selective heating of the wafer TI layer.

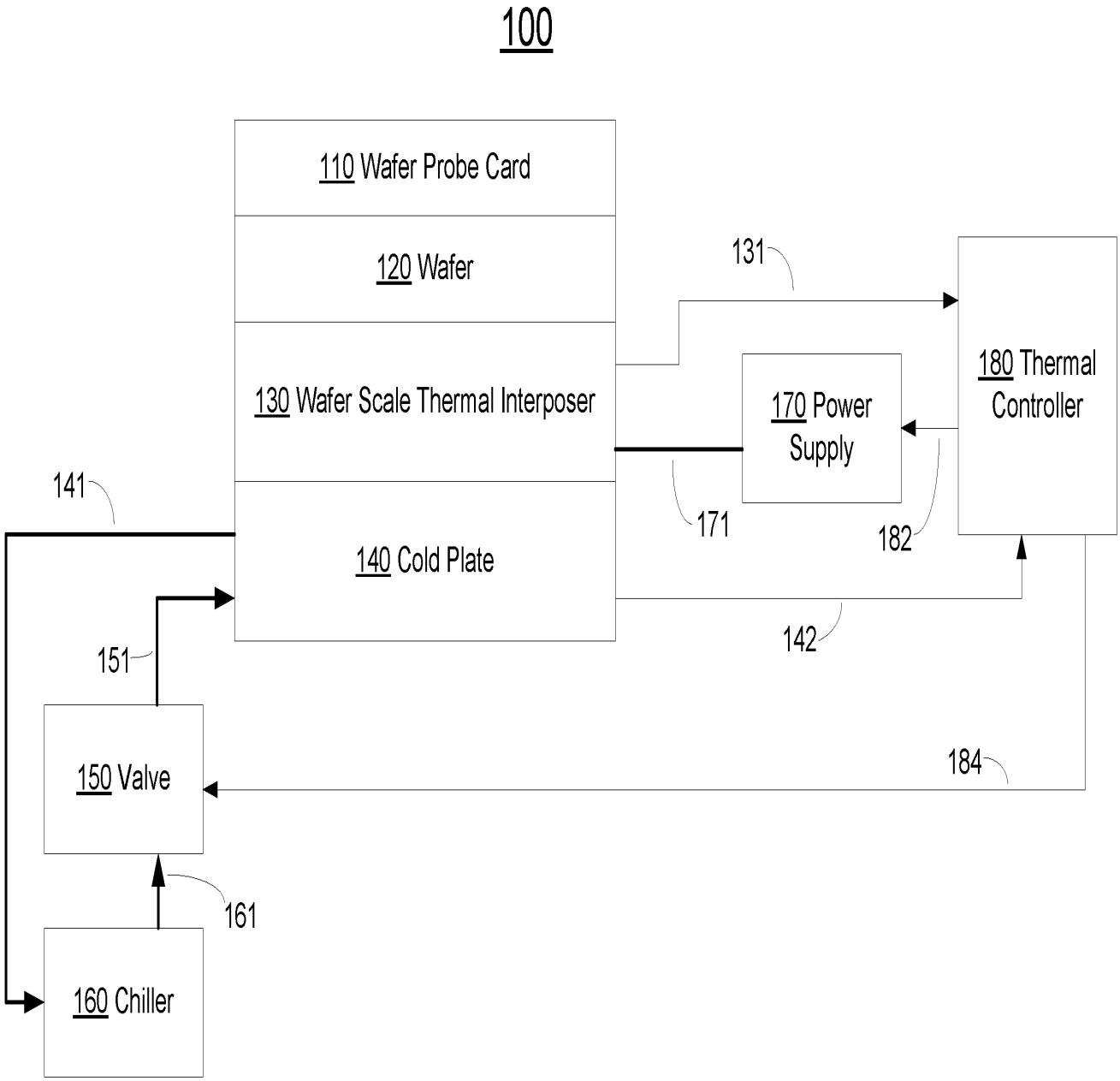

100
110 Wafer Probe Card
120 Wafer
130 Wafer Scale Thermal Interposer
140 Cold Plate
131
170 Power Supply
180 Thermal Controller
171
182
141
142
151
150 Valve
184
161
160 Chiller

Fig. 1

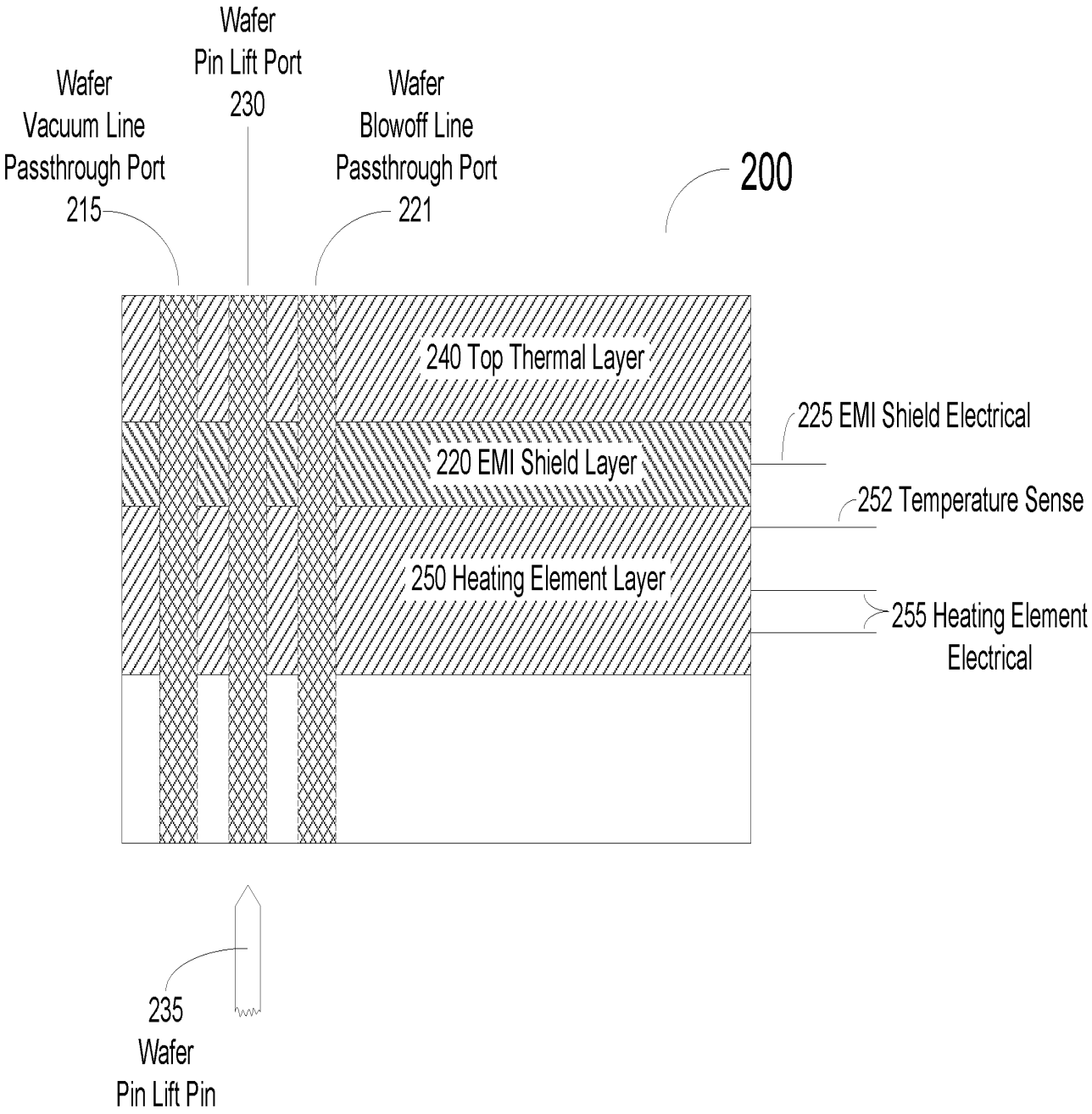

Wafer
Pin Lift Port
230
Wafer
Vacuum Line
Passthrough Port
215
Wafer
Blowoff Line
Passthrough Port
221
200
240 Top Thermal Layer
225 EMI Shield Electrical
220 EMI Shield Layer
252 Temperature Sense
250 Heating Element Layer
255 Heating Element
Electrical
235
Wafer
Pin Lift Pin

Fig. 2

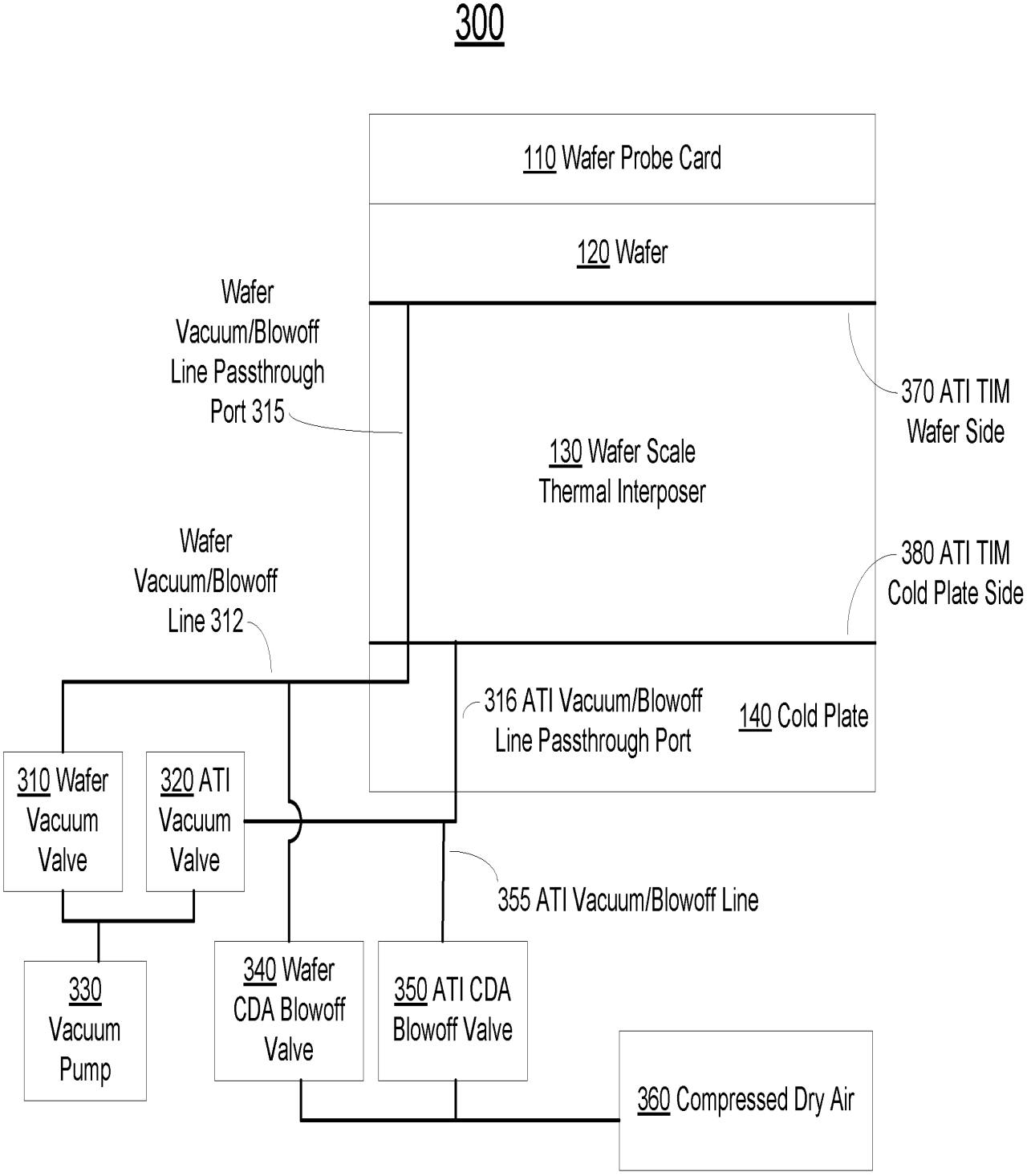

300
110 Wafer Probe Card
120 Wafer
Wafer Vacuum/Blowoff Line Passthrough Port 315
370 ATI TIM Wafer Side
130 Wafer Scale Thermal Interposer
Wafer Vacuum/Blowoff Line 312
380 ATI TIM Cold Plate Side
316 ATI Vacuum/Blowoff Line Passthrough Port
140 Cold Plate
310 Wafer Vacuum Valve
320 ATI Vacuum Valve
355 ATI Vacuum/Blowoff Line
330 Vacuum Pump
340 Wafer CDA Blowoff Valve
350 ATI CDA Blowoff Valve
360 Compressed Dry Air

Fig. 3

400

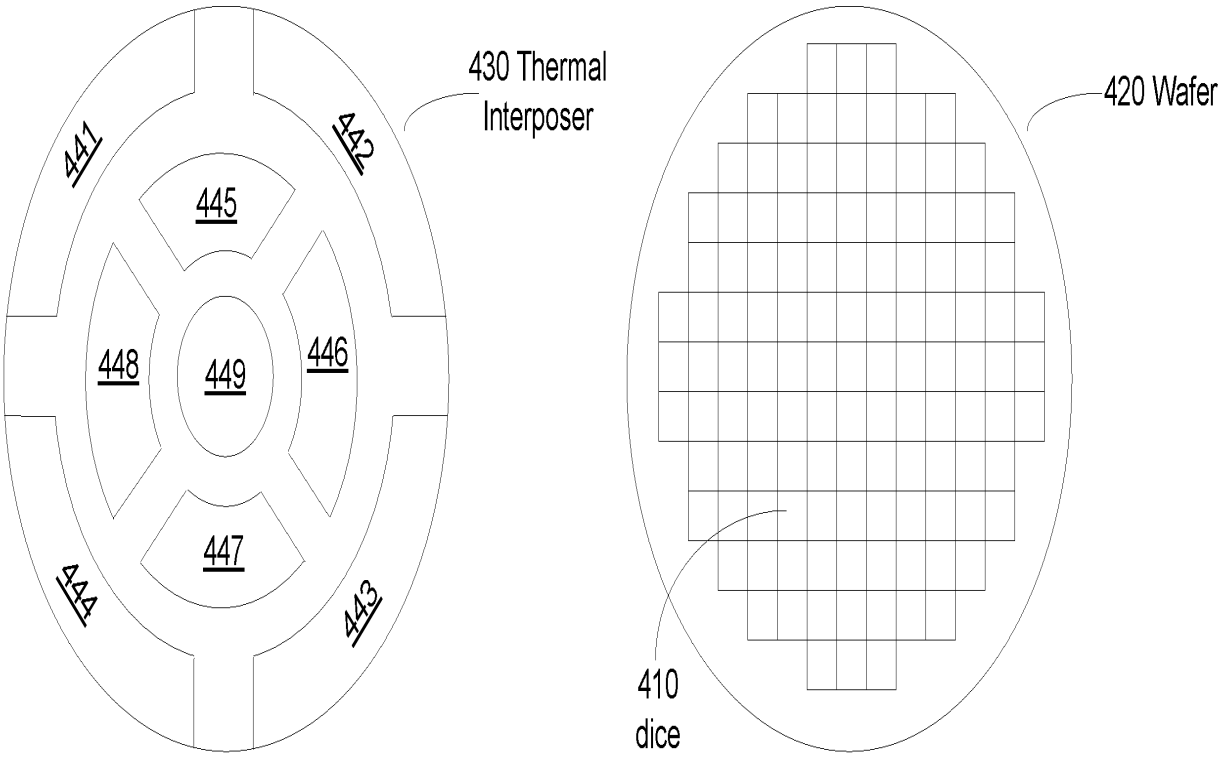

430 Thermal Interposer
420 Wafer
441
442
443
444
445
446
447
448
449
410 dice

Fig. 4

500

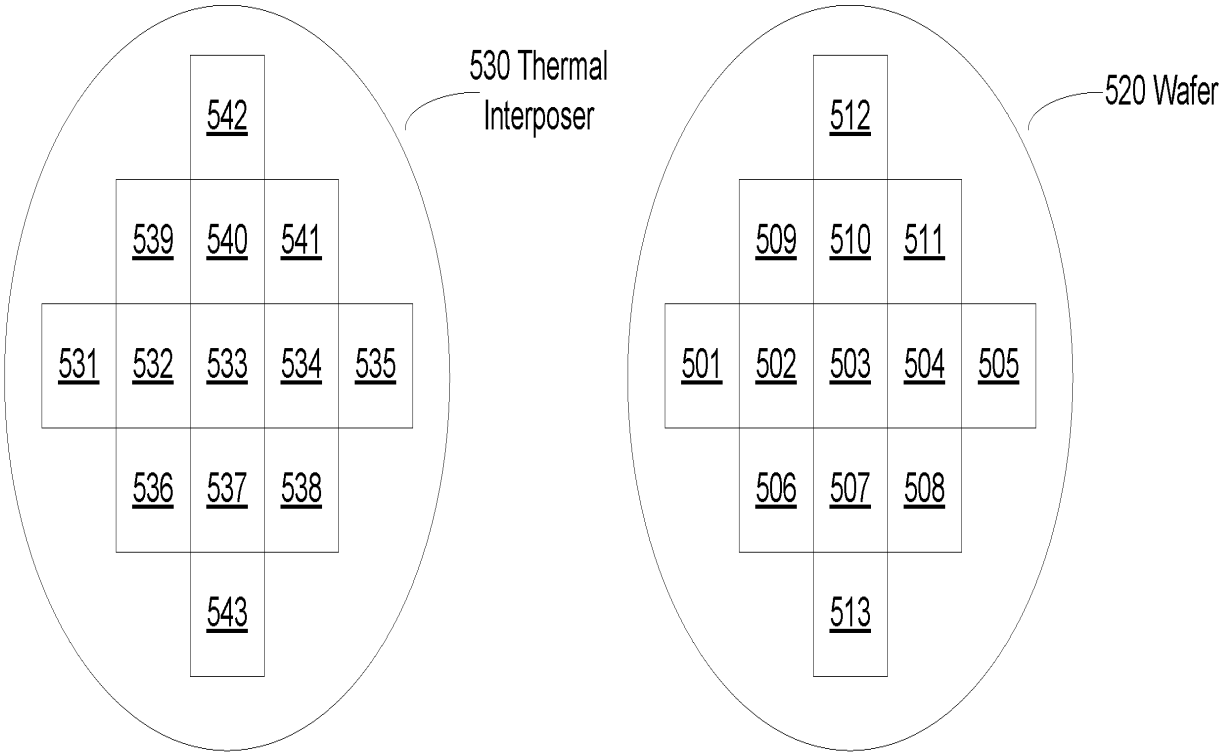

530 Thermal Interposer
542
539
540
541
531
532
533
534
535
536
537
538
543
520 Wafer
512
509
510
511
501
502
503
504
505
506
507
508
513

Fig. 5

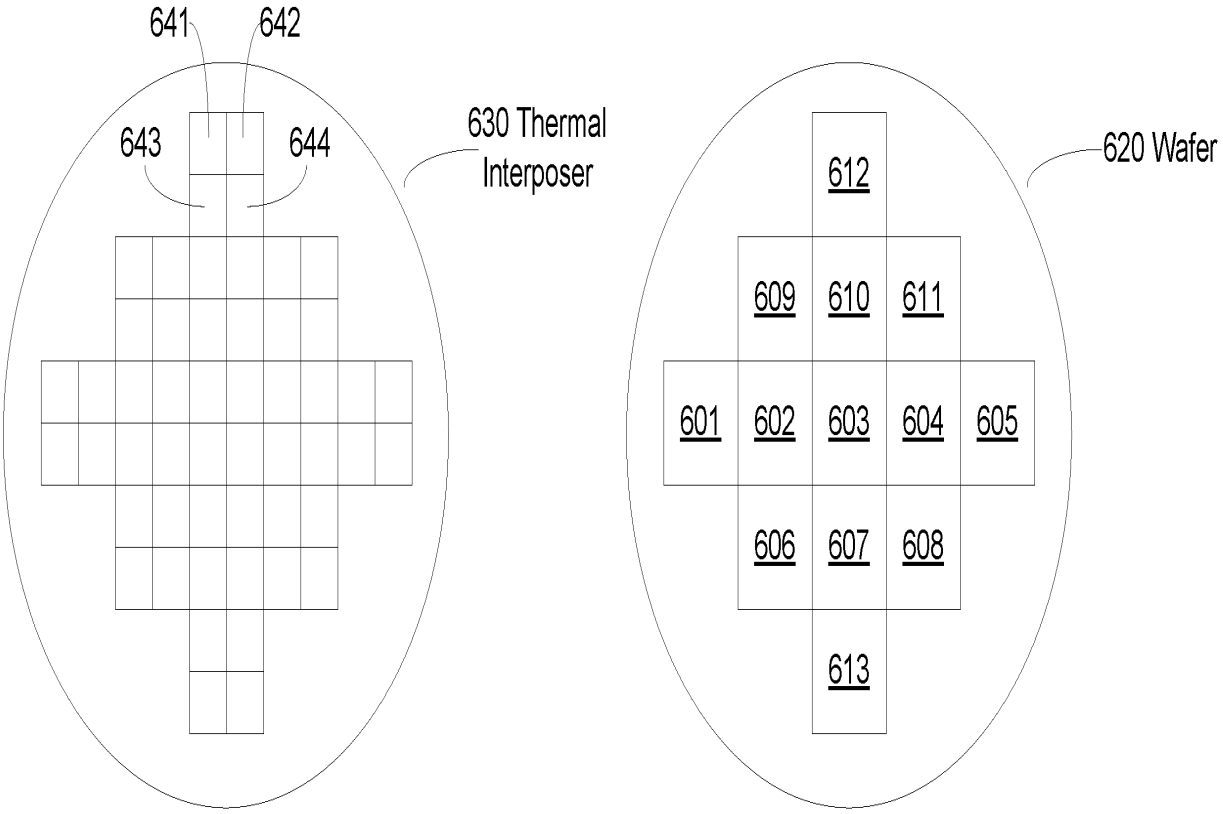

600
641
642
643
644
630 Thermal Interposer
620 Wafer
612
609
610
611
601
602
603
604
605
606
607
608
613

Fig. 6

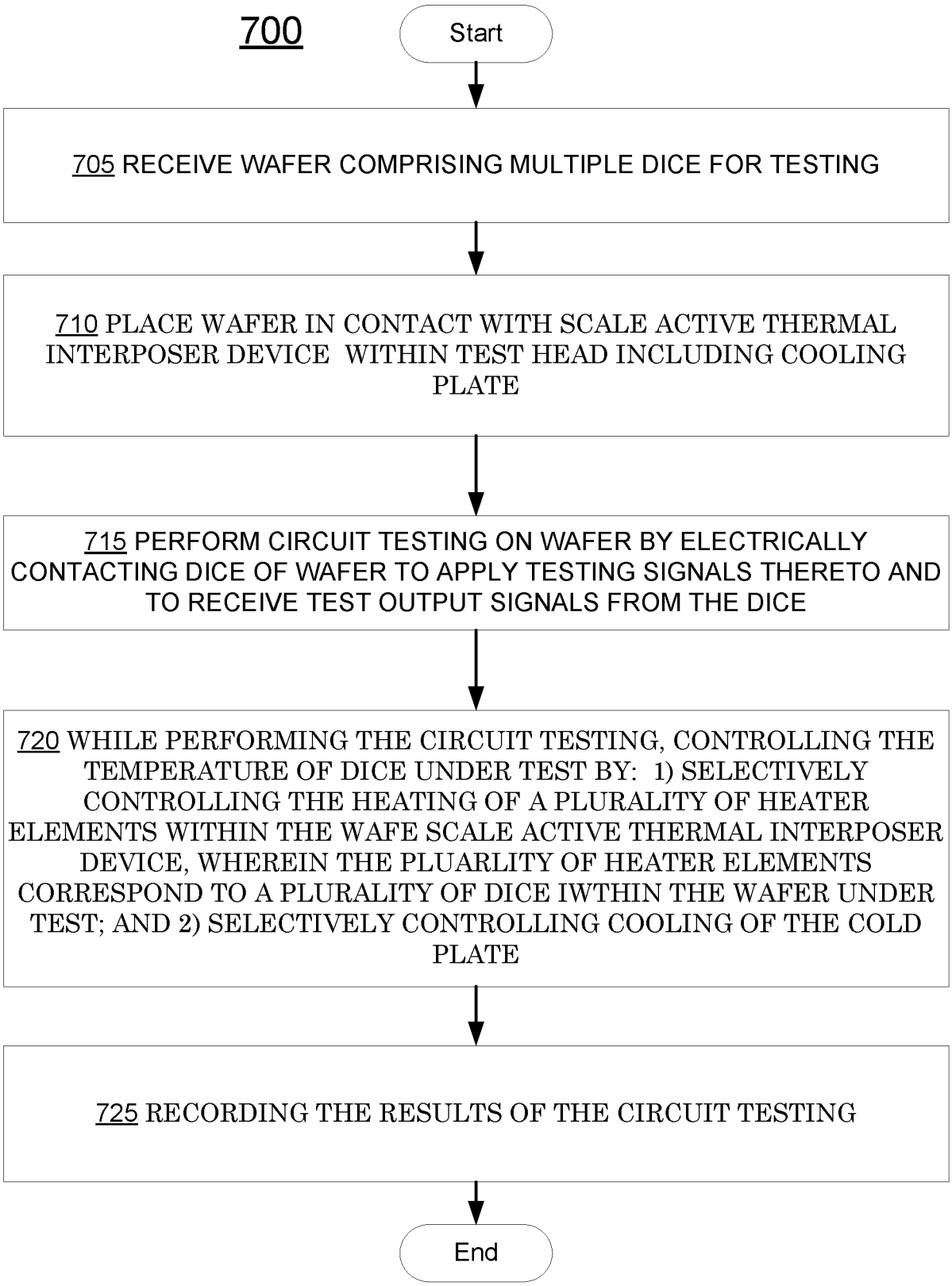

700
Start
705 RECEIVE WAFER COMPRISING MULTIPLE DICE FOR TESTING
710 PLACE WAFER IN CONTACT WITH SCALE ACTIVE THERMAL INTERPOSER DEVICE WITHIN TEST HEAD INCLUDING COOLING PLATE
715 PERFORM CIRCUIT TESTING ON WAFER BY ELECTRICALLY CONTACTING DICE OF WAFER TO APPLY TESTING SIGNALS THERETO AND TO RECEIVE TEST OUTPUT SIGNALS FROM THE DICE
720 WHILE PERFORMING THE CIRCUIT TESTING, CONTROLLING THE TEMPERATURE OF DICE UNDER TEST BY: 1) SELECTIVELY CONTROLLING THE HEATING OF A PLURALITY OF HEATER ELEMENTS WITHIN THE WAFE SCALE ACTIVE THERMAL INTERPOSER DEVICE, WHEREIN THE PLUARLITY OF HEATER ELEMENTS CORRESPOND TO A PLURALITY OF DICE IWTHIN THE WAFER UNDER TEST; AND 2) SELECTIVELY CONTROLLING COOLING OF THE COLD PLATE
725 RECORDING THE RESULTS OF THE CIRCUIT TESTING
End

Fig. 7A

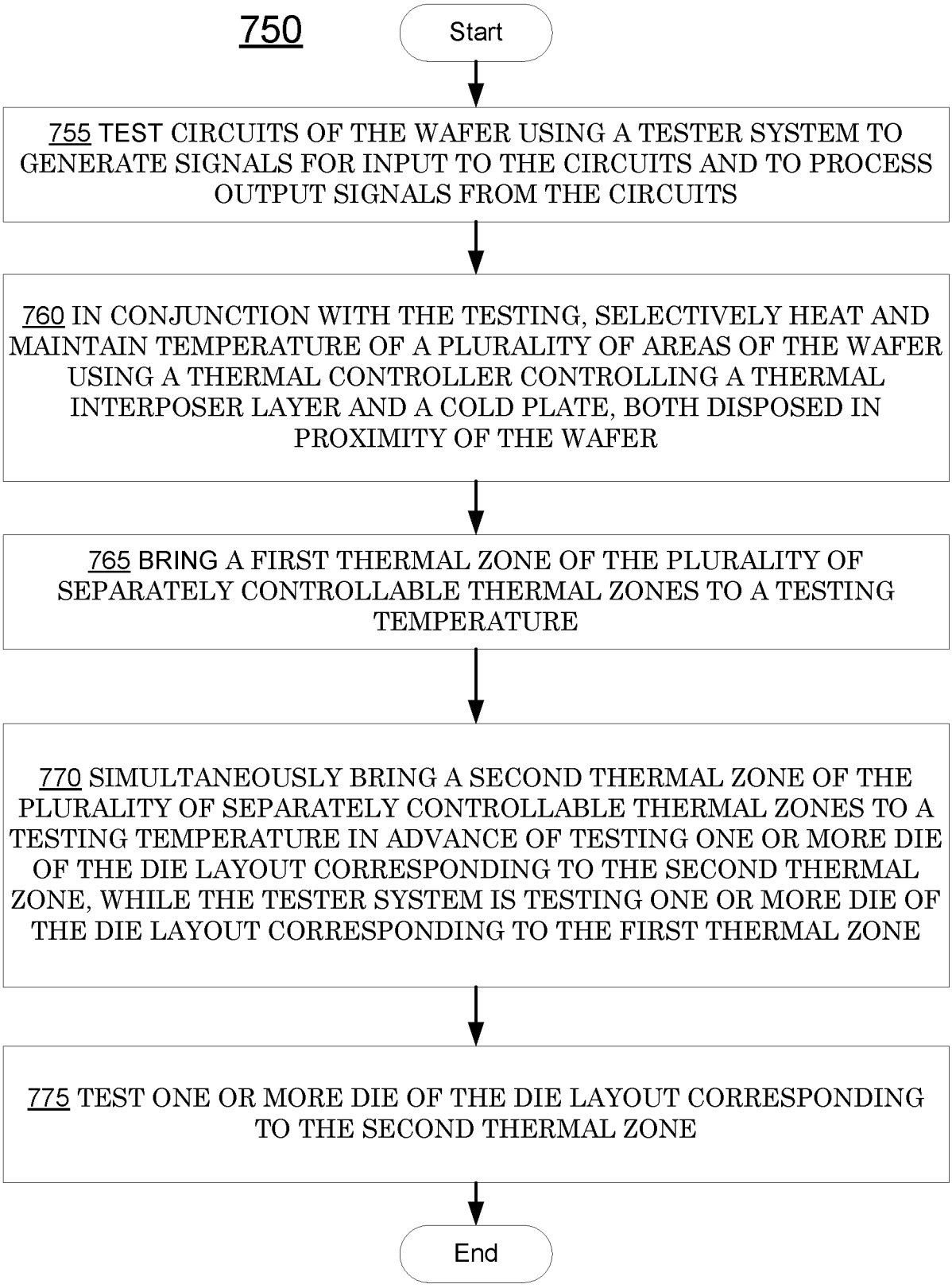

750
Start
755 TEST CIRCUITS OF THE WAFER USING A TESTER SYSTEM TO GENERATE SIGNALS FOR INPUT TO THE CIRCUITS AND TO PROCESS OUTPUT SIGNALS FROM THE CIRCUITS
760 IN CONJUNCTION WITH THE TESTING, SELECTIVELY HEAT AND MAINTAIN TEMPERATURE OF A PLURALITY OF AREAS OF THE WAFER USING A THERMAL CONTROLLER CONTROLLING A THERMAL INTERPOSER LAYER AND A COLD PLATE, BOTH DISPOSED IN PROXIMITY OF THE WAFER
765 BRING A FIRST THERMAL ZONE OF THE PLURALITY OF SEPARATELY CONTROLLABLE THERMAL ZONES TO A TESTING TEMPERATURE
770 SIMULTANEOUSLY BRING A SECOND THERMAL ZONE OF THE PLURALITY OF SEPARATELY CONTROLLABLE THERMAL ZONES TO A TESTING TEMPERATURE IN ADVANCE OF TESTING ONE OR MORE DIE OF THE DIE LAYOUT CORRESPONDING TO THE SECOND THERMAL ZONE, WHILE THE TESTER SYSTEM IS TESTING ONE OR MORE DIE OF THE DIE LAYOUT CORRESPONDING TO THE FIRST THERMAL ZONE
775 TEST ONE OR MORE DIE OF THE DIE LAYOUT CORRESPONDING TO THE SECOND THERMAL ZONE
End

Fig. 7B

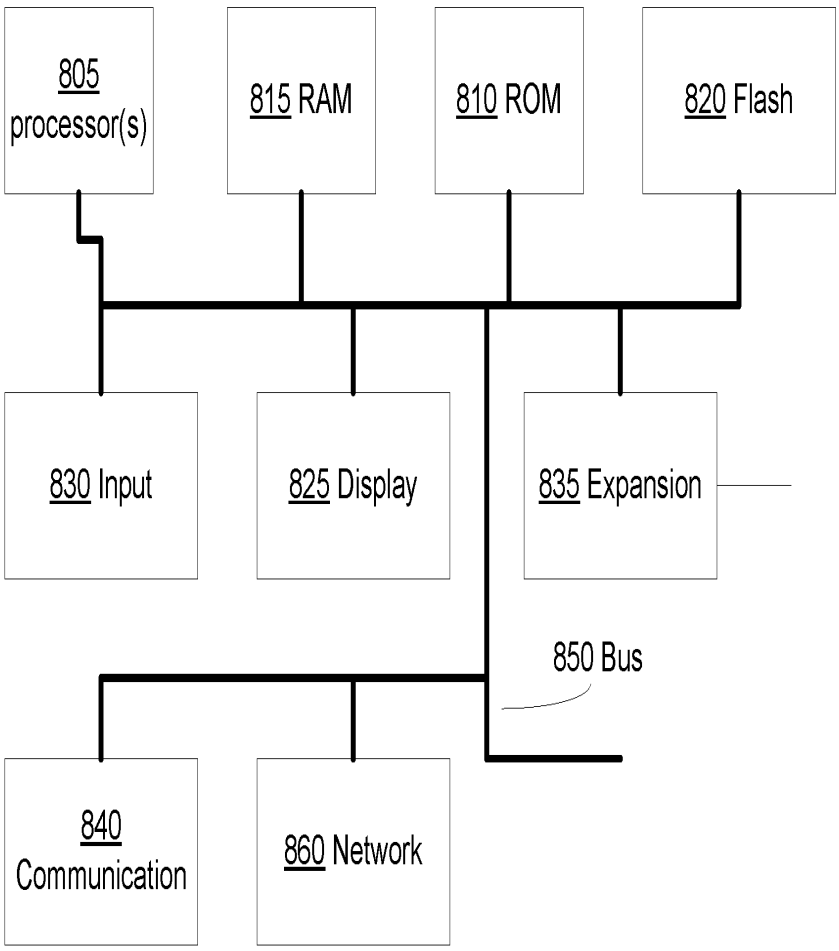

800
805 processor(s)
815 RAM
810 ROM
820 Flash
830 Input
825 Display
835 Expansion
850 Bus
840 Communication
860 Network

Fig. 8

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Filer:	Anthony C. Murabito/Mina Oliveri
Attorney Docket Number:	AATS-0107-02C01US

Filed as Large Entity

Filing Fees for Track I Prioritized Examination - Nonprovisional Application under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
REQUEST FOR PRIORITIZED EXAMINATION	1817	1	4200	4200
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	6	100	600
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
PROCESSING FEE, EXCEPT PROV. APPLS.	1830	1	140	140
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**6760**

Electronic Acknowledgement Receipt

EFS ID:	45521150
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Mina Oliveri
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	20-APR-2022
Filing Date:	
Time Stamp:	16:42:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	EFT
Payment was successfully received in RAM	$6760
RAM confirmation Number	E20224JG43250580
Deposit Account	504160
Authorized User	Mina Oliveri

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Track One Request	AATS-0107-02C01US_TRACKONE_REQUEST_4-20-2022.pdf	150189 3317ce8b483fff195c48eb5e5fac5bd17204c38a	no	2
Warnings:					
Information:					
2	Application Data Sheet	AATS-0107-02C01US_ADS_4-20-2022.pdf	1226817 909e99fd4227086c613c54d1c9ed4a311c406edb	no	10
Warnings:					
Information:					
3		AATS-0107-02C01US_20P075US03_Track1_Con_Filing.pdf	161147 c6943bb21b45c8b7f2325070d74cdafd264b69d7	yes	54

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	44
Claims	45	53
Abstract	54	54

Warnings:					
Information:					
4	Drawings-only black and white line drawings	AATS-0107-02C01US_20P075US03_Figures_4-20-2022.pdf	74719 fbe9eec582ff8068ec962d1ebc605998d717314f	no	9
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	53252 10567c86795611bfb9733b79b264ded3fc47e7f9	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	1666124

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/725,164	04/20/2022	2858	2420	AATS-0107-02C01US	26	3

CONFIRMATION NO. 5389

FILING RECEIPT

109838
Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

OC000000133380600

Date Mailed: 04/26/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Samer Kabbani, Laguna Niguel, CA;
Paul Ferrari, Mission Viejo, CA;
Ikeda Hiroki, Kukishi Saitama, JAPAN;
Kiyokawa Toshiyuki, Kukishi Saitama, JAPAN;
Gregory Cruzan, Anaheim, CA;
Karthik Ranganathan, Foothill Ranch, CA;

Applicant(s)

Advantest Test Solutions, Inc., San Jose, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 17/528,002 11/16/2021
which claims benefit of 63/115,813 11/19/2020

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/22/2022
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/725,164**
Projected Publication Date: 08/04/2022
Non-Publication Request: No
Early Publication Request: No
Title

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Preliminary Class

324

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/725,164	04/20/2022	Samer Kabbani	AATS-0107-02C01US

CONFIRMATION NO. 5389

109838
Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

FORMALITIES LETTER

OC000000133380601

Date Mailed: 04/26/2022

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing.

Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **160** surcharge.
- $(**0**) previous unapplied payment amount.
- $ **160** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

• A properly executed inventor's oath or declaration has not been received for the following inventor(s):
Samer Kabbani
Paul Ferrari
Ikeda Hiroki
Kiyokawa Toshiyuki
Gregory Cruzan
Karthik Ranganathan

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/mabebe/

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/725,164

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	26 minus 20 =	* 6			OR	x 100 =	600
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2420

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/725,164	04/20/2022	Samer Kabbani	AATS-0107-02C01US

CONFIRMATION NO. 5389

109838
Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

FORMALITIES LETTER

OC000000133380601

Date Mailed: 04/26/2022

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing.

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- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

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- $ **160** surcharge.
- $(**0**) previous unapplied payment amount.
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- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Samer Kabbani
  Paul Ferrari
  Ikeda Hiroki
  Kiyokawa Toshiyuki
  Gregory Cruzan
  Karthik Ranganathan

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

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Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

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For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/mabebe/

Electronic Patent Application Fee Transmittal

Application Number:	17725164
Filing Date:	20-Apr-2022
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Filer:	Anthony C. Murabito/Mina Oliveri
Attorney Docket Number:	AATS-0107-02C01US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Electronic Acknowledgement Receipt

EFS ID:	45759834
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Mina Oliveri
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	19-MAY-2022
Filing Date:	20-APR-2022
Time Stamp:	19:28:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	EFT
Payment was successfully received in RAM	$160
RAM confirmation Number	E20225IJ29000625
Deposit Account	504160
Authorized User	Mina Oliveri

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	NOTICE_AATS-0107-02C01US.pdf	81657 221dbc29103671afa6a0e75448e3edff21339bad	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37944 a3a2de39141e1333a9420ea73ddc3e190692d07e	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	119601		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/725,164	04/20/2022	Samer Kabbani	AATS-0107-02C01US

CONFIRMATION NO. 5389

109838
Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

INFORMAL NOTICE

OC000000133996545

Date Mailed: 05/23/2022

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Samer Kabbani
  Paul Ferrari
  Ikeda Hiroki
  Kiyokawa Toshiyuki
  Gregory Cruzan
  Karthik Ranganathan

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/nton/

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/725,164

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	26 minus 20 =	* 6			OR	x 100 =	600
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2420

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/725,164	04/20/2022	2858	2580	AATS-0107-02C01US	26	3

CONFIRMATION NO. 5389

UPDATED FILING RECEIPT

109838
Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

OC000000133996544

Date Mailed: 05/23/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Samer Kabbani, Laguna Niguel, CA;
Paul Ferrari, Mission Viejo, CA;
Ikeda Hiroki, Kukishi Saitama, JAPAN;
Kiyokawa Toshiyuki, Kukishi Saitama, JAPAN;
Gregory Cruzan, Anaheim, CA;
Karthik Ranganathan, Foothill Ranch, CA;

Applicant(s)

Advantest Test Solutions, Inc., San Jose, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 17/528,002 11/16/2021
which claims benefit of 63/115,813 11/19/2020

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/22/2022
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/725,164**
Projected Publication Date: 09/01/2022
Non-Publication Request: No
Early Publication Request: No
Title

WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Preliminary Class

324

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	OPAP
Examiner Name	CENTRAL, DOCKET
Attorney Docket Number	AATS-0107-02C01US

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	9841772	B2	2017-12-12	BUCHER	
	2	9080820	B2	2015-07-14	BOLTON	
	3	7411792	B2	2008-08-12	RICHARDS; ET AL	
	4	9310145	B2	2016-04-12	COLONGO; ET AL	
	5	7755899	B2	2010-07-13	STENMARK	
	6	10354785	B2	2019-07-16	YAMAGUCHI; ET AL	
	7	6184504	B1	2001-02-06	CARDELLA	
	8	9414526	B1	2016-08-09	MANN; ET AL	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	Samer Kabbani
	Art Unit	OPAP
	Examiner Name	CENTRAL, DOCKET
	Attorney Docket Number	AATS-0107-02C01US

	9	6668570		2003-12-30	WALL; et al	
	10	10908207		2021-02-02	BARABI; et al	
	11	7042240		2006-05-09	LOPEZ; et al	
	12	7830164		2010-11-09	EARLE; et al	
	13	6359264		2002-03-19	SCHAPER; ET AL	
	14	7626407		2009-12-01	KABBANI	
	15	9766287		2017-09-19	NARASAKI; ET AL	
	16	9494353		2016-11-15	YU; ET AL	
	17	7436059		2008-10-14	OUYANG	
	18	5821505		1998-10-13	TUSTANIWSKYJ; ET AL	
	19	9291667		2016-03-22	ARMSTRONG; ET AL	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Art Unit	OPAP
	Examiner Name	CENTRAL, DOCKET
	Attorney Docket Number	AATS-0107-02C01US

	20	7519880		2009-04-14	JOHNSON; ET AL	
	21	8558540		2013-10-15	WU; ET AL	
	22	10656200		2020-05-19	CRUZAN; ET AL	
	23	7151388		2006-12-19	GOPAL; ET AL	
	24	7848106		2010-12-07	MERROW	
	25	10656200		2020-05-19	CRUZAN; ET AL	
	26	10775408		2020-09-15	CARVALHO; ET AL	
	27	11143697		2021-10-12	WOLFF	
	28	5239093		1993-08-24	CHENG	
	29	7355428		2008-04-08	KABBANI; ET AL	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
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	Attorney Docket Number	AATS-0107-02C01US

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20090218087	A1	2009-09-03	OSHIMA	
	2	20210071917	A1	2021-03-11	PEI; ET AL	
	3	20030155939	A1	2003-08-21	LUTZ; ET AL	
	4	20180218926	A1	2018-08-02	STUCKEY; ET AL	
	5	20200371155	A1	2020-11-26	WALCZYK; ET AL	
	6	20050086948	A1	2005-04-28	MILKE-ROJO; ETAL	
	7	20130285686	A1	2013-10-31	MALIK; et al	
	8	20020118032	A1	2002-08-29	NORRIS; ET AL	
	9	20140251214	A1	2014-09-11	CUVALC; ET AL	
	10	20050151553	A1	2005-07-14	KABBANI; ET AL	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	Samer Kabbani
	Art Unit	OPAP
	Examiner Name	CENTRAL, DOCKET
	Attorney Docket Number	AATS-0107-02C01US

	11	20200363104	A1	2020-11-19	MacDonald; et al	
	12	20060290370	A1	2006-12-28	LOPEZ	
	13	20190346482	A1	2019-11-14	KIYOKAWA; ET AL	
	14	20100042355	A1	2010-02-18	AUBE; ET AL	
	15	20050026476	A1	2005-02-03	MOK; ET AL	
	16	20050103034	A1	2005-05-19	HAMILTON; ET AL	
	17	20220082587	A1	2022-03-17	GOPAL; ET AL	
	18	20150226794	A1	2015-08-13	CHEN	
	19	20160084880	A1	2016-03-24	LoCicero; ET AL	
	20	20170102409	A1	2017-04-13	SARHAD; ET AL	
	21	20190310314	A1	2019-10-10	LIU; ET AL	

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	First Named Inventor	Samer Kabbani
	Art Unit	OPAP
	Examiner Name	CENTRAL, DOCKET
	Attorney Docket Number	AATS-0107-02C01US

	22	20150028912	A1	2015-01-29	CHO; ET AL	
	23	20160351526	A1	2016-12-01	BOYD; ET AL	
	24	20210396801	A1	2021-12-23	RANGANATHAN; ET AL	
	25	20220137129	A1	2022-05-05	RANGANATHAN; ET AL	
	26	20110074080	A1	2011-03-31	DiStefano; ET AL	
	27	20180024188	A1	2018-01-25	CRUZAN; ET AL	
	28	20190064254	A1	2019-02-28	BOWYER; ET AL	
	29	20220044084	A1	2022-02-10	CARDY	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2005156172	JP	A	2005-06-16	NIPPON ENG KK ADVANTEST CORP	(with Machine Translation)	×

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
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	Examiner Name	CENTRAL, DOCKET
	Attorney Docket Number	AATS-0107-02C01US

	2	201636618	TW	A	2014-12-24	QUALITAU INC		☐
	3	201504647	TW	A	2013-07-24	ADVANTEST CORP		☐
	4	3270261	EP	A1	2018-01-17	ASETEK A/S		☐
	5	2008275512	JP	A	2008-11-13	ESPEC CORP		☐
	6	2016122039	WO	A1	2016-08-04	UNIQUEST CO LTD.		☐
	7	2017112076	WO	A1	2017-06-29	INTEL CORP.		☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1		

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	OPAP
	Examiner Name	CENTRAL, DOCKET
	Attorney Docket Number	AATS-0107-02C01US

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	OPAP
	Examiner Name	CENTRAL, DOCKET
	Attorney Docket Number	AATS-0107-02C01US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2022-06-08
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	45908560
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Missy Isaac
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	08-JUN-2022
Filing Date:	20-APR-2022
Time Stamp:	16:22:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	AATS-0107-02C01US_IDS.pdf	614272 08c0fa4186eb1f6e88995b9c1702ec508660 4d12	no	10

Warnings:

Information:					
2	Foreign Reference	TW201636618A.pdf	5454933 c46c93e133f05f610d58edc89dedf18c2ca37173	no	52
Warnings:					
Information:					
3	Foreign Reference	TW201504647A.pdf	6697504 d4da59a942108ba4a1ca23f620326ed423e4e90f	no	51
Warnings:					
Information:					
4	Foreign Reference	WO2017112076A1.pdf	4903394 26f667ce27bf610190ba2f3139135c910dc44a94	no	35
Warnings:					
Information:					
5	Foreign Reference	WO2016122039A1_.pdf	19970747 fce259c452a99e1ac05d0675964bc604e1244e71	no	25
Warnings:					
Information:					
6	Foreign Reference	EP3270261A1_.pdf	16335815 bd78d9a20146c389aba2999280e6e40bca5c51d1	no	14
Warnings:					
Information:					
7	Foreign Reference	JP2005156172A_.pdf	8988184 e40b71b8c04a214f91accf709a0df2df0a899a7b	no	15
Warnings:					
Information:					
8	Foreign Reference	JP2008275512A_.pdf	7454222 8664d8e363d572c4b8f4342892087fef21ca028a	no	13
Warnings:					
Information:					
		Total Files Size (in bytes):	70419071		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/725,164	04/20/2022	Samer Kabbani	AATS-0107-02C01US	5389

109838 7590 06/15/2022

Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

EXAMINER	
CENTRAL, DOCKET	

ART UNIT	PAPER NUMBER
OPAP	

NOTIFICATION DATE	DELIVERY MODE
06/15/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

acmadmin@mhbpatents.com
officeaction@mhbpatents.com

Decision Granting Request for Prioritized Examination (Track I)	**Application No.** 17/725,164	**Applicant(s)** Kabbani et al.	
	Examiner Kristen Matter	**Art Unit** OPET	**AIA (FITF) Status** Yes

1. THE REQUEST FILED 20 April 2022 IS **GRANTED** .

The above-identified application has met the requirements for prioritized examination

A. ☑ for an original nonprovisional application (Track I).
B. ☐ for an application undergoing continued examination (RCE).

2. **The above-identified application will undergo prioritized examination**. The application will be accorded special status throughout its entire course of prosecution until one of the following occurs:

A. filing a **petition for extension of time** to extend the time period for filing a reply;

B. filing an **amendment to amend the application to contain more than four independent claims, more than thirty total claims** , or a multiple dependent claim;

C. filing a **request for continued examination** ;

D. filing a notice of appeal;

E. filing a request for suspension of action;

F. mailing of a notice of allowance;

G. mailing of a final Office action;

H. completion of examination as defined in 37 CFR 41.102; or

I. abandonment of the application.

Telephone inquiries with regard to this decision should be directed to Kristen Matter at (571)272-5270. In his/her absence, calls may be directed to Petition Help Desk at (571) 272-3282.

/CHERYL GIBSON BAYLOR/ Paralegal Specialist, OPET	

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	3763
Examiner Name	LING, FOR K.
Attorney Docket Number	AATS-0107-02C01US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5126656		1992-06-30	Jones	
	2	5164661		1992-11-17	Jones	
	3	5315240		1994-05-24	Jones	
	4	5239093		1994-07-12	Okano	
	5	5420521		1995-05-30	Jones	
	6	6389225		2002-05-14	Malinoski , et al.	
	7	6498899		2002-12-24	Malinoski , et al.	
	8	6711904		2004-03-30	Law , et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Examiner Name	LING, FOR K.
	Attorney Docket Number	AATS-0107-02C01US

	9	6825681		2004-11-30	Feder , et al.	
	10	6862405		2005-03-01	Malinoski , et al.	
	11	6985000		2006-01-10	Feder , et al.	
	12	7311782		2007-12-25	Strang , et al.	
	13	7659738		2010-02-09	Hong	
	14	7726145		2010-06-01	Nakamura	
	15	8343280		2013-01-01	Iimuro	
	16	8772682		2014-07-08	Ambal , et al.	
	17	8927907		2015-01-06	Fink , et al.	
	18	9307578		2016-04-05	Pease	
	19	10056225		2018-08-21	Gaff , et al.	

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	Examiner Name	LING, FOR K.
	Attorney Docket Number	AATS-0107-02C01US

	20	10163668		2018-12-25	Steinhauser	
	21	10955466		2021-03-23	Tsai , et al.	
	22	10983145		2021-04-20	Akers , et al.	
	23	7830164		2010-11-09	Earle , et al.	

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020026258	A1	2002-02-28	Suzuki, Tetsuya ; et al.	
	2	20040017185	A1	2004-01-29	Song, Jae Myeong ; et al.	
	3	20130181576	A1	2013-07-18	SHIOZAWA; Masakuni ; et al.	
	4	20180189159	A1	2018-07-05	Carmichael; Richard ; et al.	
	5	20190162777	A1	2019-05-30	Chiang; Sheung Ming John ; et al.	

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	First Named Inventor	Samer Kabbani
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	Examiner Name	LING, FOR K.
	Attorney Docket Number	AATS-0107-02C01US

	6	20220137092	A1	2022-05-05	Ranganathan; Karthik ; et al.	

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	101073016	CN	A	2007-11-14	ADVANTEST CORP		
	2	103038751	CN	A	2013-04-10	ADVANTEST CORP		
	3	105144114	CN	A	2015-12-09	ADVANTEST CORP		
	4	110618903	CN	A	2019-12-27	BEIJING MEMBLAZE TECH CO LTD		
	5	200535440	TW	A	2005-11-01	AGILENT TECHNOLOGIES INC		
	6	201840996	TW	A	2018-11-16	A T E SOLUTIONS INC		
	7	2017015052	WO	A1	2017-01-26	DELTA DESIGN INC		
	8	2017039936	WO	A1	2017-03-09	TERADYNE INC		

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
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	First Named Inventor	Samer Kabbani
	Art Unit	3763
	Examiner Name	LING, FOR K.
	Attorney Docket Number	AATS-0107-02C01US

	9	2020159954	WO	A1	2020-08-06	KES SYSTEMS INC		
	10	2008275512	JP	A	2008-11-13	ESPEC CORP		

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	RANGANATHAN et al. D517: Shielded Socket and Carrier for High-Volume Test of Semiconductor Devices; Powerpoint; 12 pp. 09-30-2021	

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	3763
	Examiner Name	LING, FOR K.
	Attorney Docket Number	AATS-0107-02C01US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2022-07-08
Name/Print	Anthony C. Murabito	Registration Number	35295

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EFS ID:	46146488
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Missy Isaac
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	08-JUL-2022
Filing Date:	20-APR-2022
Time Stamp:	14:34:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	AATS-0107-02C01US_IDS_07-08-2022.pdf	613644 d46bf5cf601913876be694d16b29651eb345780b	no	7

Warnings:

Information:					
2	Non Patent Literature	NPL_1.pdf	2879933 20fb4b64a6dd603e0a23343b89786621c783ffc8	no	12
Warnings:					
Information:					
3	Foreign Reference	CN101073016A.pdf	1984724 3ba0fa9e51c64cc62e726d4e6dfda9e10bcfe318	no	46
Warnings:					
Information:					
4	Foreign Reference	CN103038751A.pdf	3354281 5c19ef79287ebec5dedf7a154b690af4b7b8ee7c	no	29
Warnings:					
Information:					
5	Foreign Reference	CN105144114A.pdf	1977997 3c16b8093b45dd4fe1101581f25891472ff399c4	no	27
Warnings:					
Information:					
6	Foreign Reference	CN110618903A.pdf	1203545 8e8cfb32cb43e0706c3ac90d7b9b0e4c0592d2a0	no	18
Warnings:					
Information:					
7	Foreign Reference	TW200535440A.pdf	5721922 7a628ac416e9ca85d161e4cf1472cbaebeb34111	no	67
Warnings:					
Information:					
8	Foreign Reference	TW201840996A.pdf	1211162 4ab1e2eb299dcd3a349976002a462126e43a41c5	no	35
Warnings:					
Information:					

9	Foreign Reference	JP2008275512A.pdf	472696 e333a13278754f268bc23a60056ee28c18c1392e	no	13
Warnings:					
Information:					
10	Foreign Reference	WO2017015052A1.pdf	1097401 0eb8af74dd2462c5b1483033e9c5908f9ad88b3d	no	34
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Information:					
11	Foreign Reference	WO2017039936A1.pdf	2258291 c393833af4d70f0dc65e05fe13453a0bd148e185	no	48
Warnings:					
Information:					
12	Foreign Reference	WO20201599954A1.pdf	1404556 3547b048e29b78e2dc8eef4f9bcf4f16e0087da1	no	33
Warnings:					
Information:					
		Total Files Size (in bytes):	24180152		

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Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	3763
Examiner Name	TBD
Attorney Docket Number	AATS-0107-02C01US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5239093		1993-08-24	CHENG	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	3763
	Examiner Name	TBD
	Attorney Docket Number	AATS-0107-02C01US

	1	RANGANATHAN et al. D517: Shielded Socket and Carrier for High-Volume Test of Semiconductor Devices; Powerpoint; 12 pp. 09-30-2021

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	3763
	Examiner Name	TBD
	Attorney Docket Number	AATS-0107-02C01US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2022-07-12
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	46172755
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Missy Isaac
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	12-JUL-2022
Filing Date:	20-APR-2022
Time Stamp:	17:27:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	AATS-0107-02C01US_IDS_07-12-2022.pdf	612139 5480c8f081401d877ff11f6e91714fb1cc78a482	no	4

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Information:	
Total Files Size (in bytes):	612139

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/725,164	04/20/2022	Samer Kabbani	AATS-0107-02C01US

CONFIRMATION NO. 5389

109838
Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

PUBLICATION NOTICE



Title:WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

Publication No.US-2022-0276301-A1
Publication Date:09/01/2022

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

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In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2868
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	202043787	TW	A	2020-12-01	CELERINT LLC		

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	2868
	Examiner Name	SHAH, NEEL D
	Attorney Docket Number	AATS-0107-02C01US

	1	

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	Attorney Docket Number	AATS-0107-02C01US

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

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Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2022-09-22
Name/Print	Anthony C. Murabito	Registration Number	35295

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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Electronic Acknowledgement Receipt

EFS ID:	46672962
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Missy Isaac
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	22-SEP-2022
Filing Date:	20-APR-2022
Time Stamp:	14:34:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	AATS-0107-02C01US_IDS_09-22-2022.pdf	612099 3e9fc8ce0acba672edab9a0892dbac3b70aea085	no	4

Warnings:

Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	Foreign Reference	TW202043787A__.pdf	7634114 1c1b6d9a23133bfcc88a10de8257fe05ceb6efa2	no	51
Warnings:					
Information:					
			Total Files Size (in bytes):	8246213	

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/725,164	04/20/2022	Samer Kabbani	AATS-0107-02C01US	5389

109838 7590 09/23/2022

Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

EXAMINER	
SHAH, NEEL D	

ART UNIT	PAPER NUMBER
2868	

NOTIFICATION DATE	DELIVERY MODE
09/23/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

acmadmin@mhbpatents.com
officeaction@mhbpatents.com

Office Action Summary	Application No. 17/725,164	Applicant(s) Kabbani et al.	
	Examiner NEEL D SHAH	Art Unit 2868	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 04/20/22.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-26 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-4,8-12,15-20 and 23-24 is/are rejected.

8) ☑ Claim(s) 5-7,13-14,21-22 and 25-26 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 04/20/22 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 06/08/22, 07/08/22, 07/12/22.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 06/08/22, 07/08/22, 07/12/22 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

Claim Objections

3. Claim 2 is objected to because of the following informalities: the term "selective" misspelled. Appropriate correction is required.

Note: Claim 1 is rejected twice below.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

4. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

5. **Claims 1-4, 8-12, 15-20, 23-24 are rejected** under 35 U.S.C. 103 as being unpatentable over Feder et al. (US 6,825,681) in view of Ando et al. (US 8,653,843). ("Feder" and "Ando").

6. Regarding claim 1, Feder teaches A system for testing circuits of an integrated circuit semiconductor wafer [Figures 1-12, a system for testing circuits of an integrated circuit semiconductor wafer is taught], the system comprising: a tester system for generating signals for input to said circuits and for processing output signals from said circuits for testing said wafer [Figures 1-12, a tester system 53, 55 for generating signals for input and output is shown]; a test stack coupled to said tester system [Figures 1-12, a test stack 1, 47 combined is shown], said test stack comprising: a wafer probe for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer [Figures 1-12, a wafer probe 51 for contacting wafer 49 and for probing circuits is shown; see Column 8, lines 50-67]; a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer [Figures 1-12, a wafer thermal interposer layer 1 is shown for heating (using thermal elements 5)]; and a cold plate disposed under said wafer TI layer and operable to cool said wafer [Figures 1-12, thermal chuck 47 acts as a cold plate under wafer TI layer 1 to cool wafer 49]; and a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer (by controlling cooling of said cold plate and) by controlling selective heating of said wafer TI layer [Figures 1-12, Column 9, lines 24-35, a thermal controller is taught for selectively controlling heating].

Feder does not explicitly teach controlling cooling of said plate.

However, Ando teaches controlling cooling of said plate [Figures 1-4, controlling cooler 113 to adjust temperature is taught].

It would have been obvious to one skilled in the art before the effective filing date of the invention to modify Feder with Ando. Doing so would allow Feder to comprise controller to

control coolant which would help improve temperature control and hence help improve testing in a controlled environment.

7. Regarding claim 2, Feder teaches further comprising a power supply coupled to provide power to said wafer TI layer and controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said selective heating of said wafer TI layer is based on said PWM signals [Figures 1-12, Column 7, lines36-41 and Column 11, lines 47-54 teaches a power supply coupled to provide power to wafer TI layer 1 and controlled by thermal controller via PWM signals].

8. Regarding claim 3, Feder teaches further comprising: a chiller for cooling liquid; a valve for controlling an amount of said liquid flowing to said cold plate, wherein said valve is controlled by said thermal controller [Figures 1-12, a chiller/coolant for cooling liquid is taught and coolant hoses, pipes is taught].

9. Regarding claim 4, Feder teaches further comprising: a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and a second TIM layer disposed between said wafer TI layer and said wafer [Figures 1-12, a first thermal interface material is disposed, see Figure 2].

10. Regarding claim 8, Feder teaches wherein said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and wherein said plurality of traces are operable to selectively heat a plurality of zones of said wafer TI layer under control of said thermal controller and wherein further said plurality of zones correspond to said areas of said wafer [Figures 1-4, a plurality of traces of TI layer 1 is shown, see thermal zones 5].

11. Regarding claim 9, Feder teaches wherein positions of said plurality of zones of said wafer TI layer correspond to a die layout of said wafer and wherein further said wafer TI layer is

customized for said wafer [Figures 1-4, the positions of thermal zones correspond to a die layer of wafer].

12. Regarding claim 10, Feder teaches wherein each zone of said plurality of zones corresponds to a respective single die of said die layout of said wafer [Figures 1-4, each zone correspond to single die].

13. Regarding claim 11, Feder teaches wherein each zone of said plurality of zones corresponds to a respective plurality of dice of said die layout of said wafer [Figures 1-4, each zone correspond to plurality of dice].

14. Regarding claim 12, Feder teaches wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer [Figures 1-4, each die correspond to multiple respective zones].

15. Regarding claim 15, Feder teaches A system for testing circuits of an integrated circuit semiconductor wafer [Figures 1-12, a system for testing circuits of an IC semiconductor wafer is taught], the system comprising: a tester system for generating signals for input to said circuits and for processing output signals from said circuits for testing said wafer [Figures 1-12, a tester system 55 for generating signals for input to circuits and for processing output signals from circuit for testing wafer 49 is shown]; a test stack coupled to said tester system [Figures 1-12, a test stack 47, 1 combined is shown], said test stack comprising: a wafer probe for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer [Figures 1-12, a wafer probe 45 for contacting a top surface of wafer 49 is shown for probing individual circuits/dice]; a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer and comprising a plurality of discretely controllable thermal zones, wherein

each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer [Figures 1-4, a wafer thermal interposer 1 to contact a bottom surface of wafer 49 is shown comprising thermal zones 5]; and a cold plate disposed under said wafer TI layer and operable to cool said wafer [Figures 1-4, thermal reservoir 47 for cooling acts as a cold plate]; and a thermal controller for selectively heating and maintaining temperatures of areas of said wafer (by controlling cooling of said cold plate) and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer [Figures 1-12, a thermal controller for selectively heating and maintaining temperatures by controlling head of thermal zones 5 is taught].

Feder does not explicitly teach controlling cooling of said cold plate.

However, Ando teaches controlling cooling of said cold plate [Figures 1-5, controlling cooling of cold plate is taught].

It would have been obvious to one skilled in the art before the effective filing date of the invention to modify Feder with Ando. Doing so would allow Feder to comprise capability of controlling cooling of said cold plate which will help improve system by obtaining preferred environment.

16. Regarding claim 16, Feder teaches wherein said wafer comprises a die layout comprising a plurality of dice and wherein further positions and shapes of said plurality of discretely controllable thermal zones are customized to said die layout of said wafer [Figures 1-4, a die layout comprising plurality of dice is taught].

17. Regarding claim 17, Feder teaches wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to multiple dice of said die layout of said wafer [Figures 1-4, each thermal zone 5 are controlled].

18. Regarding claim 18, Feder teaches wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to a single die of said die layout of said wafer [Figures 1-4, each thermal zone corresponds to a single die].

19. Regarding claim 19, Feder teaches wherein each die of said die layout of said wafer corresponds to multiple thermal zones of said plurality of discretely controllable thermal zones of said wafer TI layer [Figures 1-4, each zone correspond to plurality of dice].

20. Regarding claim 20, Feder teaches wherein said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and operable to selectively heat and maintain temperatures of said plurality of discretely controllable thermal zones of said wafer TI layer responsive to said thermal controller [Figures 1-4, a plurality of traces of TI layer 1 is shown, see thermal zones 5].

21. Regarding claim 23, Feder teaches A method for testing circuits of an integrated circuit semiconductor wafer [Figures 1-12, a method for testing circuits of an IC semiconductor wafer is shown], the method comprising:51CONFIDENTIAL testing said circuits of said wafer by using a tester system to generate signals for input to said circuits and to process output signals from said circuits [Figures 1-12, testing circuits of wafer 49 by using a tester system to generate signals for input and to process output signals (via tester cable 55) is taught]; and in conjunction with performing said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller controlling a thermal interposer layer (and a cold plate) [Figures 1-12, in conjunction with testing, selectively heating and maintaining temperatures of areas of wafer 49 by using a thermal controller controlling a thermal interposer layer 1 is taught], both disposed in proximity of said wafer and wherein said thermal interposer comprises a plurality of separately controllable thermal zones wherein each thermal zone is

operable to be selectively heated and temperature maintained by said thermal controller [Figures 1-12, controlling thermal zones 5 of thermal interposer 1 is taught].

Feder does not explicitly teach controlling a cold plate.

However, Ando teaches controlling a cold plate [Figures 1-5, controlling cooling of cold plate is taught].

It would have been obvious to one skilled in the art before the effective filing date of the invention to modify Feder with Ando. Doing so would allow Feder to comprise capability of controlling cooling of said cold plate which will help improve system by obtaining preferred environment.

22. Regarding claim 24, Feder teaches wherein said wafer comprises a die layout and wherein further positions and shapes of said plurality of separately controllable thermal zones of said thermal interposer layer are customized to said die layout [Figures 1-4, a die layout comprising plurality of dice is taught].

23. **Claim 1 is rejected** under 35 U.S.C. 103 as being unpatentable over Johnson et al. (US 9,400,291) in view of Feder (US 6,825,681). ("Johnson").

24. Regarding claim 1, Johnson teaches A system for testing circuits of an integrated circuit semiconductor wafer [Figures 1-4, A system for testing circuits of an IC semiconductor wafer is taught], the system comprising: a tester system for generating signals for input to said circuits and for processing output signals from said circuits for testing said wafer [Figures 1-4, a tester system 110 for generating signals for input and for processing output signals is shown]; a test stack coupled to said tester system, said test stack comprising: a wafer probe for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer

[Figures 1-4, a DUT 130 and thermal actuator 140 forms a test stack, a wafer probe 110 for contacting individual circuits of wafer DUT 130 is shown]; a wafer thermal interposer (TI) layer (operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer) [Figures 1-4, a thermal interposer layer see heating is shown]; and a cold plate (disposed under said wafer TI layer and operable to cool said wafer) [Figures 1-4, a cold plate seeing cooling is shown]; and a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer by controlling cooling of said cold plate and by controlling selective heating of said wafer TI layer [Figures 1-4, a thermal controller 150/250 for heating and cooling is shown].

Johnson does not explicitly teach a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer; and a cold plate disposed under said wafer TI layer and operable to cool said wafer.

However, Feder teaches a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer; and a cold plate disposed under said wafer TI layer and operable to cool said wafer [Figures 1-12, a thermal interposer layer 1 and a cooling plate 47 is shown].

It would have been obvious to one skilled in the art before the effective filing date of the invention to modify Johnson with Feder. Doing so would allow Johnson to comprise a thermal actuator with a thermal interposer layer for heating and a cooling plate for cooling in a specific arrangement which would effectively help carry out testing in a controlled environment.

Allowable Subject Matter

25. Claims 5-7, 13-14, 21-22, 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims are stated below:

5. The system as described in Claim 4 wherein said first and second TIM layers comprise indium foil.
6. The system as described in Claim 4 further comprising: a first vacuum valve for establishing suction for securing said wafer to said wafer TI layer; a second vacuum valve for establishing suction for securing said wafer TI layer to said cold plate; and a vacuum pump coupled to both said first and second vacuum valves.
7. The system as described in Claim 6 further comprising: a first blow-off valve for controlling air to release said wafer from said wafer TI layer; a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and a source of air coupled to both said first and second blow-off valves.
13. The system as described in Claim 1 further comprising a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical pass through channels which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer.
14. The system as described in Claim 2 wherein: said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and operable to selectively heat a plurality of zones of said wafer TI layer responsive to said PWM signals; and said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from said PWM signals applied to said plurality of traces.
21. The system as described in Claim 16 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising: bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and while said tester system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.
22. The system as described in Claim 16 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal

zones of said wafer TI layer, said preconditioning method comprising: bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and while said tester system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

25. The method as described in Claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises: bringing a first thermal zone of said plurality of separately controllable thermal zones to a testing temperature; and while said tester system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of separately controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

26. The method as described in Claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises: bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and while said tester system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NEEL D SHAH whose telephone number is (571)270-3766. The examiner can normally be reached M-F: 9AM-5:30PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Judy Nguyen can be reached on 571-272-2258. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NEEL D SHAH/
Primary Examiner, Art Unit 2868

Notice of References Cited	Application/Control No. 17/725,164	Applicant(s)/Patent Under Reexamination Kabbani et al.	
	Examiner NEEL D SHAH	Art Unit 2868	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
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*	B	US-8653843-B2	02-2014	Ando; Masakazu	G01R31/2874	324/750.04
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	D					
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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/725,164	Kabbani et al.
	Examiner	Art Unit
	NEEL D SHAH	2868

CPC - Searched*		
Symbol	Date	Examiner
(G01R31/00,20,26,28,31,3185 G01R1/04,067,073,44).cpc.	09/19/2022	NS

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST search attached	09/19/2022	NS
IDS checked, ip.com searched, DP checked, inventor-assignee name search done	09/19/2022	NS

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/NEEL D SHAH/ Primary Examiner, Art Unit 2868	

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	OPAP
Examiner Name	CENTRAL, DOCKET
Attorney Docket Number	AATS-0107-02C01US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

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Attorney Docket Number	AATS-0107-02C01US

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	OPAP
	Examiner Name	CENTRAL, DOCKET
	Attorney Docket Number	AATS-0107-02C01US

	2	201636618	TW	A	2014-12-24	QUALITAU INC		☐
	3	201504647	TW	A	2013-07-24	ADVANTEST CORP		☐
	4	3270261	EP	A1	2018-01-17	ASETEK A/S		☐
	5	2008275512	JP	A	2008-11-13	ESPEC CORP		☐
	6	2016122039	WO	A1	2016-08-04	UNIQUEST CO LTD.		☐
	7	2017112076	WO	A1	2017-06-29	INTEL CORP.		☐

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EXAMINER SIGNATURE

Examiner Signature	/NEEL D SHAH/	Date Considered	09/19/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2022-06-08
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

Bibliographic Data

Application No: 17/725,164

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /NEEL D SHAH/ Examiner's Signature | Initials

Title: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
04/20/2022	324	2868	AATS-0107-02C01US
RULE			

APPLICANTS

Advantest Test Solutions, Inc., San Jose, CA, UNITED STATES

INVENTORS

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Ikeda Hiroki, Kukishi Saitama, JAPAN

Kiyokawa Toshiyuki, Kukishi Saitama, JAPAN

Gregory Cruzan, Anaheim, CA, UNITED STATES

Karthik Ranganathan, Foothill Ranch, CA, UNITED STATES

CONTINUING DATA

This application is a CON of 17528002 11/16/2021

17528002 has PRO of 63115813 11/19/2020

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

04/22/2022

STATE OR COUNTRY

UNITED STATES

ADDRESS

Advantest c/o Murabito Hao & Barnes LLP

111 North Market Street

Suite 700

San Jose, CA 95113

UNITED STATES

FILING FEE RECEIVED

$6,760

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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First Named Inventor	Samer Kabbani
Art Unit	3763
Examiner Name	TBD
Attorney Docket Number	AATS-0107-02C01US

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	1	5239093		1993-08-24	CHENG	

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Attorney Docket Number	AATS-0107-02C01US

	1	RANGANATHAN et al. D517: Shielded Socket and Carrier for High-Volume Test of Semiconductor Devices; Powerpoint; 12 pp. 09-30-2021

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EXAMINER SIGNATURE

Examiner Signature	/NEEL D SHAH/	Date Considered	/NEEL D SHAH/

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Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2022-07-12
Name/Print	Anthony C. Murabito	Registration Number	35295

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	6	"17725164"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DK, EA, EE, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/14 11:57 AM
L2	0	("2022/0276301").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/09/14 12:05 PM
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L4	1	(Advantest NEAR2 (Test Solutions)).as.	(US-PGPUB; USPAT)	OR	ON	ON	2022/09/14 12:06 PM
L5	10	(Advantest NEAR2 (Test Solutions)).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DK, EA, EE,	OR	ON	ON	2022/09/14 12:06 PM

			ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L6	1908	((Kabbani NEAR2 Samer) (Ferrari NEAR2 Paul) (Hiroki NEAR2 Ikeda) (Toshiyuki NEAR2 Kiyokawa) (Cruzan NEAR2 Gregory) (Ranganathan NEAR2 Karthik)).inv.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DK, EA, EE, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/14 12:09 PM
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L10	84	8 9	(US-PGPUB; USPAT)	OR	ON	ON	2022/09/14 12:11 PM

L11	58	("3700857" | "3836751" | "4126824" | "4357526" | "4374316" | "4624137" | "4684783" | "4744246" | "4777434" | "4808009" | "4909078" | "4956793" | "5059770" | "5126656" | "5164661" | "5315240" | "5352870" | "5420520" | "5420521" | "5539186" | "5550482" | "5605612" | "5643483" | "5669419" | "5672980" | "5740016" | "5751015" | "5821505" | "5911897" | "5940110" | "5977785" | "5982013" | "6389225" | "20020033391").pn. OR ("6825681").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/09/15 09:54 AM
L12	43	(Artificial Intelligence) Similar to: 17/725,164 with 0 CPC Selections and 0 Text Selections Text: (JP-2021141143-A OR US-20210278456-A1 OR CN-113341239-A OR KR-20210111681-A OR US-10955466-B2 OR CN-114113970-A OR US-20060279319-A1 OR US-20080061814-A1 OR TW-I288240-B OR CN-114113969-A OR JP-5352135-B2 OR TW-200643439-A OR JP-2009031271-A OR US-7663390-B2 OR US-20090009203-A1 OR US-20100123474-A1 OR US-8040146-B2 OR JP-6441252-B2 OR JP-2017167006-A OR US-10359468-B2 OR TW-202104918-A OR TW-I701450-B OR US-20170269154-A1 OR US-9933478-B2 OR US-7621761-B2 OR US-20210018560-A1 OR US-20050026476-A1 OR JP-2016191563-A OR FR-2959018-B1	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DK, EA, EE, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO))	OR	ON	ON	2022/09/15 10:14 AM

		OR EP-1153431-A1 OR WO-0039851-A1 OR EP-1153431-B1 OR US-6140141-A OR EP-3825705-A1 OR KR-20220000822-A OR US-6885203-B1 OR US-20210156891-A1 OR US-20080090429-A1 OR CN-113851416-A OR US-20210407829-A1 OR EP-3929603-A1 OR ES-2545008-T3 OR KR-20100057118-A OR TW-202206819-A OR CN-103038654-A OR US-7247035-B2 OR TW-202132780-A OR US-11002760-B1 OR US-20060240690-A9 OR JP-2022007724-A).did.					
L13	32	(Artificial Intelligence) More like doc: US-20220276301-A1 Text: (US-20220155364-A1 OR KR-20220068939-A OR US-20220187361-A1 OR US-20220268831-A1 OR US-20220178991-A1 OR TW-202234082-A OR KR-20220079467-A OR KR-20220079465-A OR US-20220206061-A1 OR KR-20220097269-A OR KR-20210157893-A OR DE-102019128942-A1 OR KR-20220044430-A OR US-20220107360-A1 OR US-20210183668-A1 OR TW-202224048-A OR EP-0227926-A1 OR US-11313898-B1 OR KR-102438150-B1 OR US-20220196728-A1).did.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 10:15 AM
L14	0	12 AND 13	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB,	OR	ON	ON	2022/09/15 10:15 AM

			HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L15	117	12 13	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 10:16 AM
L16	58	("3700857" | "3836751" | "4126824" | "4357526" | "4374316" | "4624137" | "4684783" | "4744246" | "4777434" | "4808009" | "4909078" | "4956793" | "5059770" | "5126656" | "5164661" | "5315240" | "5352870" | "5420520" | "5420521" | "5539186" | "5550482" | "5605612" | "5643483" | "5669419" | "5672980" | "5740016" | "5751015" | "5821505" | "5911897" | "5940110" | "5977785" | "5982013" | "6389225" | "20020033391").pn. OR ("6825681").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/09/15 10:24 AM
L17	50	("20220155364" "20220187361" "20220268831" "20220178991" "20220206061" "20100052714" "20050206397" "7863915" "7579847" "6891385" "20030122567"	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/09/15 10:36 AM

		"20210396801" "6825681" "6985000" "20050007136" "20040012404" "6094059" "20220107360" "6094060" "5949246" "6549026" "20160131702" "20020047702" "6744270" "20020171133" "20080090429" "6791171" "7330041" "7621761" "20210183668" "8025097" "20020075023" "7138818" "20050017750" "20050026476" "20060240690" "7247035" "20070267188" "6525555" "20040174181" "11035898" "20070057684" "7688090" "6867611" "7772860" "20080297186" "6064213" "7396236" "20030107394" "6812718").pn.					
L18	38	"7436059"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 10:38 AM
L19	164	"5821505"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS,	OR	ON	ON	2022/09/15 10:39 AM

			IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L20	66	"5821505"	(US-PGPUB; USPAT)	OR	ON	ON	2022/09/15 10:39 AM
L21	10	((US-8653843-B2 OR US-7436059-B1 OR US-6825681-B2 OR US-5821505-A OR US-10955466-B2).did. AND USPT.dbnm.) OR ((US-20220206061-A1 OR US-20220187361-A1 OR US-20220178991-A1 OR US-20220155364-A1).did. AND DWPI.dbnm.) OR ((US-20210156891-A1).did. AND PGPB.dbnm.)	(USPAT; US-PGPUB; FPRS; USOCR; IBM_TDB; EPO; JPO; DERWENT; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN))	OR	ON	ON	2022/09/15 02:06 PM
L22	22592	((test$3 inspect$3 monitor$3) WITH (IC (integrated ADJ circuit) DUT (device ADJ under ADJ test) dice chip wafer)) AND ((thermal heat$3) WITH (wafer DUT (device ADJ under ADJ test))) AND (cool$3 WITH (wafer DUT (device ADJ under ADJ test))) AND ((control$3 adjust$3) WITH (thermal heat$3 cool$3 temperature))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:10 PM
L23	1097	((test$3 inspect$3 monitor$3) WITH (IC (integrated ADJ circuit) DUT (device ADJ under ADJ test) dice chip wafer)).ti,ab,clm. AND ((thermal heat$3) WITH (wafer DUT (device ADJ under ADJ test))).ab,clm. AND (cool$3 WITH (wafer DUT (device ADJ under ADJ test))).ab,clm. AND ((control$3 adjust$3)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO;	OR	ON	ON	2022/09/15 02:11 PM

		WITH (thermal heat$3 cool$3 temperature)).ab,clm.	JPO; DERWENT; IBM_TDB)				
L24	76144	(G01R31/00,20,26,28,31,3185 G01R1/04,067,073,44). cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:12 PM
L25	61	23 AND 24	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:12 PM
L26	1981	(thermal ADJ actuator) SAME (heat$3) SAME (cool$3)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:21 PM
L27	4	24 AND 26	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB,	OR	ON	ON	2022/09/15 02:21 PM

			HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L28	15	22 AND 26	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:22 PM
L29	69	(thermal ADJ actuator) SAME (heat$3) SAME (cool$3) SAME wafer	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:23 PM
L30	2	26 AND 324/$.ccls.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2022/09/15 02:26 PM

			IBM_TDB)				
L31	77	(thermal ADJ actuator) SAME (heat$3) SAME (cool$3) SAME (wafer DUT probe)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:27 PM
L32	22	(thermal ADJ actuator) SAME (heat$3 ADJ2 (plate layer arm)) SAME (cool$3 ADJ2 (plate layer arm))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:34 PM
L33	49	("5021630" | "5104480" | "5194710" | "5255022" | "5420521" | "5525300" | "5541524" | "5570032").pn. OR ("5821505").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/09/15 02:43 PM
L34	14	((US-9400291-B2 OR US-8653843-B2 OR US-7436059-B1 OR US-6914446-B1 OR US-6825681-B2 OR US-5821505-A OR US-10955466-B2).did. AND USPT.dbnm.) OR ((US-20220206061-A1 OR US-20220187361-A1 OR US-20220178991-A1 OR US-20220155364-A1 OR US-20140062513-A1).did. AND DWPI.dbnm.) OR ((US-	(USPAT; US-PGPUB; FPRS; USOCR; IBM_TDB; EPO; JPO; DERWENT; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN))	OR	ON	ON	2022/09/15 02:46 PM

		20210350061-A1 OR US-20210156891-A1).did. AND PGPB.dbnm.)					
L35	1	34 AND (PWM (pulse ADJ width ADJ modulation) (pulse$1width ADJ modulation))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:46 PM
L36	9	34 AND (Control$4 WITH cool$3)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/16 05:15 PM
L37	0	34 AND ((indium ADJ foil) OR (carbon ADJ nanotube))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DK, EA, EE, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 11:13 AM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	3763
Examiner Name	LING, FOR K.
Attorney Docket Number	AATS-0107-02C01US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5126656		1992-06-30	Jones	
	2	5164661		1992-11-17	Jones	
	3	5315240		1994-05-24	Jones	
	4	5239093		1994-07-12	Okano	
	5	5420521		1995-05-30	Jones	
	6	6389225		2002-05-14	Malinoski , et al.	
	7	6498899		2002-12-24	Malinoski , et al.	
	8	6711904		2004-03-30	Law , et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	3763
	Examiner Name	LING, FOR K.
	Attorney Docket Number	AATS-0107-02C01US

	9	6825681		2004-11-30	Feder , et al.	
	10	6862405		2005-03-01	Malinoski , et al.	
	11	6985000		2006-01-10	Feder , et al.	
	12	7311782		2007-12-25	Strang , et al.	
	13	7659738		2010-02-09	Hong	
	14	7726145		2010-06-01	Nakamura	
	15	8343280		2013-01-01	Iimuro	
	16	8772682		2014-07-08	Ambal , et al.	
	17	8927907		2015-01-06	Fink , et al.	
	18	9307578		2016-04-05	Pease	
	19	10056225		2018-08-21	Gaff , et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	3763
	Examiner Name	LING, FOR K.
	Attorney Docket Number	AATS-0107-02C01US

	20	10163668		2018-12-25	Steinhauser	
	21	10955466		2021-03-23	Tsai , et al.	
	22	10983145		2021-04-20	Akers , et al.	
	23	7830164		2010-11-09	Earle , et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020026258	A1	2002-02-28	Suzuki, Tetsuya ; et al.	
	2	20040017185	A1	2004-01-29	Song, Jae Myeong ; et al.	
	3	20130181576	A1	2013-07-18	SHIOZAWA; Masakuni ; et al.	
	4	20180189159	A1	2018-07-05	Carmichael; Richard ; et al.	
	5	20190162777	A1	2019-05-30	Chiang; Sheung Ming John ; et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	3763
	Examiner Name	LING, FOR K.
	Attorney Docket Number	AATS-0107-02C01US

	6	20220137092	A1	2022-05-05	Ranganathan; Karthik ; et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	101073016	CN	A	2007-11-14	ADVANTEST CORP		
	2	103038751	CN	A	2013-04-10	ADVANTEST CORP		
	3	105144114	CN	A	2015-12-09	ADVANTEST CORP		
	4	110618903	CN	A	2019-12-27	BEIJING MEMBLAZE TECH CO LTD		
	5	200535440	TW	A	2005-11-01	AGILENT TECHNOLOGIES INC		
	6	201840996	TW	A	2018-11-16	A T E SOLUTIONS INC		
	7	2017015052	WO	A1	2017-01-26	DELTA DESIGN INC		
	8	2017039936	WO	A1	2017-03-09	TERADYNE INC		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	3763
	Examiner Name	LING, FOR K.
	Attorney Docket Number	AATS-0107-02C01US

	9	2020159954	WO	A1	2020-08-06	KES SYSTEMS INC		
	10	2008275512	JP	A	2008-11-13	ESPEC CORP		

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	RANGANATHAN et al. D517: Shielded Socket and Carrier for High-Volume Test of Semiconductor Devices; Powerpoint; 12 pp. 09-30-2021	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/NEEL D SHAH/	Date Considered	09/19/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	3763
Examiner Name	LING, FOR K.
Attorney Docket Number	AATS-0107-02C01US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2022-07-08
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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UNITED STATES PATENT AND TRADEMARK OFFICE

USPTO Automated Interview Request (AIR)

Nov 3 2022

This paper requesting to schedule and/or conduct an interview is appropriate because:

This submission is requested to be accepted as an authorization for this interview to communicate via the internet. Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned concerning scheduling of the interview via video conference, instant messaging, or electronic mail, and to conduct the interview in accordance with office practice including video conferencing.

Name(s):
Anthony C. Murabito

S-signature:
/Anthony C Murabito/

Registration Number:
35295

U.S. Application Number:
17725164

Confirmation Number:
5389

E-mail Address:
amurabito@mhbpatents.com

Phone Number:
+1 4089389080 ext 110

Proposed Time of Interview:
11-9-2022 1:30 PM ET

Alternative Proposed Time(s) of Interview:
11-9-2022 4:00 PM ET

Alternative Proposed Time(s) of Interview:
11-10-2022 1:30 PM ET

Prefered Interview Type:
Telephonic

I am the applicant or applicant's representative for this application.

Topic for Discussion:
9/23/22 Rejection; Claims 1, 3, 4; allowable matter in Claims 14, 21, 22, 25, 26

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6515470		2003-02-04	SUZUKI; ET AL	
	2	7138811		2006-11-21	MAHONEY; ET AL	
	3	7781883		2010-08-24	SRI-JAYANTHA; ET AL	
	4	8970244		2015-03-03	DI STEFANO; ET AL	
	5	9594113		2017-03-14	DAVIS; ET AL	
	6	10126356		2018-11-13	BARABI; ET AL	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	2858
	Examiner Name	SHAH, NEEL D
	Attorney Docket Number	AATS-0107-02C01US

	1	20060158207		2006-07-20	REITINGER	
	2	20090160472		2009-06-25	SEGAWA; ET AL	
	3	20110050268		2011-03-03	CO; ET AL	
	4	20140035715		2014-02-06	TAKAHASHI; ET AL	
	5	20150137842		2015-05-21	MURAKAMI; ET AL	
	6	20160247552		2016-08-25	KIM; ET AL	
	7	20190271719		2019-09-05	STERZBACH	
	8	20200041564		2020-02-06	COJOCNEANU; ET AL	
	9	20210183668		2021-06-17	CAGLE; ET AL	
	10	20210293495		2021-09-23	BARAKO; ET AL	
	11	20220206061		2022-06-30	RANGANATHAN; ET AL	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	109716513	CN		2019-05-03	ROGERS CORP		
	2	110214270	CN		2019-09-06	TOYOTA MOTOR CO LTD		
	3	446682	TW		2001-07-21	SPEEDLINE TECHNOLOGIES INC		
	4	200620596	TW		2006-06-16	ULTRATECH INC		
	5	200628818	TW		2006-08-16	REITINGER ERICH		
	6	201226579	TW		2012-07-01	IND TECH RES INST		
	7	201229535	TW		2012-07-16	NIHON MICRONICS KK		
	8	201323883	TW		2013-06-16	CELADON SYSTEMS INC		
	9	201447325	TW		2014-12-16	SEIKO EPSON CORP		

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	Examiner Name	SHAH, NEEL D
	Attorney Docket Number	AATS-0107-02C01US

	10	201608254	TW		2016-03-01	R&D CIRCUITS INC		
	11	201712459	TW		2017-04-01	DELTA DESIGN INC		
	12	201834134	TW		2018-09-16	SEMES CO LTD		
	13	202043787	TW		2020-12-01	CELERINT LLC		
	14	202004980	TW		2020-01-16	APPLIED MATERIALS INC		

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
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Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2022-12-07
Name/Print	Anthony C. Murabito	Registration Number	35295

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Electronic Patent Application Fee Transmittal

Application Number:	17725164
Filing Date:	20-Apr-2022
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Filer:	Anthony C. Murabito/Missy Isaac
Attorney Docket Number:	AATS-0107-02C01US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

Electronic Acknowledgement Receipt

EFS ID:	47165259
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Missy Isaac
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	07-DEC-2022
Filing Date:	20-APR-2022
Time Stamp:	19:13:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	EFT
Payment was successfully received in RAM	$260
RAM confirmation Number	E2022B7J13482297
Deposit Account	504160
Authorized User	Missy Isaac

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	AATS-0107-02C01US_IDS_12-07-2022.pdf	613414 14db87fe9977ea222d88eddedad727b364277344	no	6
Warnings:					
Information:					
2	Foreign Reference	TW201447325A.pdf	2183741 3138062381d384c545eba1415804476afce0572d	no	55
Warnings:					
Information:					
3	Foreign Reference	TW201712459A.pdf	1291345 5c807c3c3e10af03e6b87cbfc980a1141a38581c	no	34
Warnings:					
Information:					
4	Foreign Reference	TW201226579A.pdf	4270461 62f407030e3749210704f5abb631d9f6486d9e99	no	29
Warnings:					
Information:					
5	Foreign Reference	CN109716513A.pdf	5893162 641c0ac17b374bbd98664133d9e404dd7467dc42	no	26
Warnings:					
Information:					
6	Foreign Reference	CN110214270A.pdf	8501664 045f8f8fcf1875b292ab8bd2c2bcd813a6427e55	no	41
Warnings:					
Information:					

7	Foreign Reference	TW446682B_.pdf	23884731 1699605b374f7e6b6f81b1ac0e7e58e5b099af8e	no	31
Warnings:					
Information:					
8	Foreign Reference	TW202004980A.pdf	2017561 9b7fabe93322174dfcbaa587cfae5d39c155007e	no	40
Warnings:					
Information:					
9	Foreign Reference	TW201834134A.pdf	1174869 d07402495eb7891f738a7d7908235ce675a0df9b	no	28
Warnings:					
Information:					
10	Foreign Reference	TW201229535A.pdf	1105865 0bfef89df8abcf9b1c1deee127cb44742fda155e	no	34
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Information:					
11	Foreign Reference	TW200628818A.pdf	1419060 7c57efa78f72bfb6e7e16cb94dfe912500000b4e	no	20
Warnings:					
Information:					
12	Foreign Reference	TW200620596A.pdf	4763726 fc2ab50b19210df356193962a33dc8eeb613f3a7	no	67
Warnings:					
Information:					
13	Foreign Reference	TW202043787A.pdf	7171252 b95291ff3315f9663b2f40fc100cd66c5d697c27	no	51
Warnings:					
Information:					

14	Foreign Reference	TW201636618A.pdf	1512929 0a087d926e7eb2bbbd7c83c79ca1b2c787b27a13	no	52
Warnings:					
Information:					
15	Foreign Reference	TW201323883A.pdf	1801539 83a201ca41660dc2173c4ac7a9c3b6a684624ef0	no	47
Warnings:					
Information:					
16	Foreign Reference	TW201608254A.pdf	1788225 45fd6f852804f626331a7378935651fa32fb9bed	no	37
Warnings:					
Information:					
17	Fee Worksheet (SB06)	fee-info.pdf	38245 c7f766c77e8f235d57cca460f54f39b4bd6d451d	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	69431789	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/725,164	Filing Date 04/20/2022	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	12/20/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 26	Minus	** 26	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	SLIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/STEPHEN TYLER HOLLAND/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kabbani et al.

Serial:	17/725,164	Confirmation No.	5389
Filed:	4/20/2022	Group Art Unit:	2868
Examiner:	Shah, Neel D.		
For:	Wafer Scale Active Thermal Interposer for Device Testing		

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

AMENDMENT and RESPONSE

Dear Examiner Shah:

In response to the Official Action mailed 9/23/2022, please enter the following amendments and remarks for filing in the above captioned patent application.

AEM Americas, Inc. - 1002
Page 203

In the Claims:

1. (currently amended) A system for testing circuits of an integrated circuit semiconductor wafer, the system comprising:

a tester system for generating signals for input to said circuits and for processing output signals from said circuits for testing said wafer;

a test stack coupled to said tester system, said test stack comprising:

a wafer probe for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer;

a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer; and

a cold plate disposed under said wafer TI layer and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer by controlling cooling of said cold plate and by controlling selective heating of said wafer TI layer,

wherein said wafer TI layer comprises one or more alignment holes for aligning said wafer TI layer with structures of said test stack external to said wafer TI layer.

2. (currently amended) The system as described in Claim 1 further comprising a power supply coupled to provide power to said wafer TI layer and

AEM Americas, Inc. - 1002
Page 204

controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said ~~ekective~~selective heating of said wafer TI layer is based on said PWM signals.

3. (original) The system as described in Claim 2 further comprising:

a chiller for cooling liquid;

a valve for controlling an amount of said liquid flowing to said cold plate, wherein said valve is controlled by said thermal controller.

4. (original) The system as described in Claim 1 further comprising:

a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and

a second TIM layer disposed between said wafer TI layer and said wafer.

5. (original) The system as described in Claim 4 wherein said first and second TIM layers comprise indium foil.

6. (original) The system as described in Claim 4 further comprising:

a first vacuum valve for establishing suction for securing said wafer to said wafer TI layer;

a second vacuum valve for establishing suction for securing said wafer TI layer to said cold plate; and

a vacuum pump coupled to both said first and second vacuum valves.

7. (original) The system as described in Claim 6 further comprising:

a first blow-off valve for controlling air to release said wafer from said wafer TI layer;

a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and

a source of air coupled to both said first and second blow-off valves.

8. (original) The system as described in Claim 1 wherein said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and wherein said plurality of traces are operable to selectively heat a plurality of zones of said wafer TI layer under control of said thermal controller and wherein further said plurality of zones correspond to said areas of said wafer.

9. (original) The system as described in Claim 8 wherein positions of said plurality of zones of said wafer TI layer correspond to a die layout of said wafer and wherein further said wafer TI layer is customized for said wafer.

10. (original)The system as described in Claim 9 wherein each zone of said plurality of zones corresponds to a respective single die of said die layout of said wafer.

11. (original)The system as described in Claim 9 wherein each zone of said plurality of zones corresponds to a respective plurality of dice of said die layout of said wafer.

12. (original)The system as described in Claim 9 wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.

13. (original)The system as described in Claim 1 further comprising a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical pass through channels which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer.

14. (original)The system as described in Claim 2 wherein:

said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and operable to selectively heat a plurality of zones of said wafer TI layer responsive to said PWM signals; and

said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for

AEM Americas, Inc. - 1002
Page 207

protecting said wafer from EMI radiation resultant from said PWM signals applied to said plurality of traces.

15. (currently amended) A system for testing circuits of an integrated circuit semiconductor wafer, the system comprising:

a tester system for generating signals for input to said circuits and for processing output signals from said circuits for testing said wafer;

a test stack coupled to said tester system, said test stack comprising:

a wafer probe for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer;

a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer,

wherein said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from activation of signals of said wafer TI layer; and

a cold plate disposed under said wafer TI layer and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of areas of said wafer by controlling cooling of said cold plate and

AEM Americas, Inc. - 1002

by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer.

16. (original)A system as described in Claim 15 wherein said wafer comprises a die layout comprising a plurality of dice and wherein further positions and shapes of said plurality of discretely controllable thermal zones are customized to said die layout of said wafer.

17. (original)A system as described in Claim 16 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to multiple dice of said die layout of said wafer.

18. (original)A system as described in Claim 16 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to a single die of said die layout of said wafer.

19. (original)A system as described in Claim 16 wherein each die of said die layout of said wafer corresponds to multiple thermal zones of said plurality of discretely controllable thermal zones of said wafer TI layer.

20. (original)The system as described in Claim 16 wherein said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and operable to

AEM Americas, Inc. - 1002
Page 209

selectively heat and maintain temperatures of said plurality of discretely controllable thermal zones of said wafer TI layer responsive to said thermal controller.

21. (original)The system as described in Claim 16 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and

while said tester system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

22. (original) The system as described in Claim 16 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and

AEM Americas, Inc. - 1002
Page 210

while said tester system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

23. (currently amended) A method for testing circuits of an integrated circuit semiconductor wafer, the method comprising:

testing said circuits of said wafer by using a tester system to generate signals for input to said circuits and to process output signals from said circuits; and

in conjunction with performing said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of said wafer and wherein said thermal interposer comprises a plurality of separately controllable thermal zones wherein each thermal zone is operable to be selectively heated and temperature maintained by said thermal controller; and

while said tester system is testing a first die of said wafer corresponding to a first thermal zone, simultaneously bringing a second thermal zone of said plurality of separately controllable thermal zones to a testing temperature in

AEM Americas, Inc. - 1002
Page 211

advance of testing a second die of said wafer corresponding to said second thermal zone.

24. (original)A method as described in Claim 23 wherein said wafer comprises a die layout and wherein further positions and shapes of said plurality of separately controllable thermal zones of said thermal interposer layer are customized to said die layout.

25. (canceled)

26. (original)The method as described in Claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises:

bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and

while said tester system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

AEM Americas, Inc. - 1002
Page 212

27. (new) The system of Claim 1 wherein said thermal controller is further configured to precondition a first area of said wafer to achieve a desired test temperature in advance of testing said first area, while testing and controlling a temperature of a second area of said wafer.

AEM Americas, Inc. - 1002
Page 213

REMARKS

Claims 1-24, 26, and 27 are pending in the present application. Claim 25 is canceled herein. Claims 1, 2, 15, and 23 are amended. Claim 27 is newly presented. No new matter is added. Applicants respectfully request reconsideration of the present application in view of the indicated amendments and the following remarks.

The amendments presented herein incorporate indicated-allowable matter, and are believed to place the present application in condition for allowance. The present amendments are further believed to require no additional search or examination.

Claim Amendments

Claim 1 is amended to include material from originally presented and indicated-allowable Claim 13. Further, these claimed limitations find support at least in the embodiments disclosed in Figure 2, items 215, 221, and/or 230, and in the Specification at paragraphs [0017] and [0055], *inter alia.*

Claim 15 is amended to include material from originally presented and indicated-allowable Claim 14. Further, these claimed limitations find support

AEM Americas, Inc. - 1002
Page 214

at least in the embodiments disclosed in Figure 2, item 225, and in the Specification at paragraphs [0017] and [0051], *et seq., inter alia.*

Claim 23 is amended to include material from originally presented and indicated-allowable Claim 25. Further, these claimed limitations find support at least in the embodiments disclosed in the Figure 7B, item 770, in the Specification at paragraphs [0020-1], [0073], and [0079], and in originally presented Claims 21, 22, 25, and/or 26, *et seq., inter alia.*

Newly presented Claim 27 finds support at least in the embodiments disclosed in the Figure 7B, item 770, in the Specification at paragraphs [0020-1], [0073], and [0079], and in originally presented and indicated-allowable Claims 21, 22, 25, and/or 26, *et seq., inter alia.*

Allowable Matter

The Official Action indicates that `Claims 5-7, 13-14, 21-22, 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.`

AEM Americas, Inc. - 1002
Page 215

Applicants thank the Examiner for indicating allowable matter.

Claim Objections

Claim 2 is objected to because of the following informalities: the term "selective" misspelled. Amendments to Claim 2 presented herein correct these cited informalities.

35 U.S.C. § 103

Claims 1-4, 8-12, 15-20, 23-24 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Feder et al. (U.S. Patent 6,825,681, "Feder") in view of Ando et al. (U.S. Patent 8,653,843, ""Ando"). Applicants respectfully assert that embodiments in accordance with the present invention are patentable over the cited art for at least the following reasons.

Claim 1 is amended to incorporate material from indicated-allowable Claim 13. Applicants believe such amendments place Claim 1 in condition for allowance.

Dependent Claims 2-14 and 27, including presently rejected Claims 2-4, and 8-12, overcome the rejections of record at least by virtue of their dependence from Claim 1, and are patentable over the cited art.

Independent Claim 15 is amended to incorporate material from indicated-allowable Claim 14. Applicants believe such amendments place Claim 15 in condition for allowance.

Dependent Claims 16-22, including presently rejected Claims 16-20, overcome the rejections of record at least by virtue of their dependence from Claim 15, and are patentable over the cited art.

Independent Claim 23 is amended to incorporate material from indicated-allowable Claim 25. Applicants believe such amendments place Claim 23 in condition for allowance.

Dependent Claims 24 and 26, including presently rejected Claim 24, overcome the rejections of record at least by virtue of their dependence from Claim 15, and are patentable over the cited art.

Claims 1-4, 8-12, 15-20, 23-24 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Johnson et al. (U.S. Patent 9,400,291,

AEM Americas, Inc. - 1002
Page 217

"Johnson") in view of Feder. Applicants respectfully assert that embodiments in accordance with the present invention are patentable over the cited art for at least the following reasons.

Claim 1 is amended to incorporate material from indicated-allowable Claim 13. Applicants believe such amendments place Claim 1 in condition for allowance.

AEM Americas, Inc. - 1002
Page 218

CONCLUSION

Claims 1-24, 26, and 27 are pending in the present application. All Claims are understood to incorporate indicated allowable material, and allowance of such claims is earnestly sought.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 504160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Date: December 20, 2022

/Anthony C. Murabito/
Anthony C. Murabito
Reg. No. 35,295

111 North Market Street
Suite 700
San Jose, California 95113
(408) 938-9060

AEM Americas, Inc. - 1002
Page 219

Electronic Acknowledgement Receipt

EFS ID:	47242692
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Mina Oliveri
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	20-DEC-2022
Filing Date:	20-APR-2022
Time Stamp:	13:21:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		AATS-0107-02C01US_AMDT_12-20-2022_.pdf	86907 c76ea6a23e96d51cee2c856db379caa438ed8149	yes	17

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Request for Reconsideration-After Non-Final Rejection	1	1
	Claims	2	11
	Applicant Arguments/Remarks Made in an Amendment	12	17
Warnings:			
Information:			
	Total Files Size (in bytes):	86907	

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New International Application Filed with the USPTO as a Receiving Office

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

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	1	651540	TW	B	2019-02-21	TERADYNE INC		
	2	201333497	TW	A	2013-08-16	ADVANTEST CORP		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	2858
	Examiner Name	SHAH, NEEL D
	Attorney Docket Number	AATS-0107-02C01US

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	2858
	Examiner Name	SHAH, NEEL D
	Attorney Docket Number	AATS-0107-02C01US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2023-01-03
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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EFS ID:	47311155
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Missy Isaac
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	03-JAN-2023
Filing Date:	20-APR-2022
Time Stamp:	19:56:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	AATS-0107-02C01US_IDS_01-03-23.pdf	612167 4dc81d79690eb42b0df32aa73b54dd83cc77af2f	no	4

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2	Foreign Reference	TWI651540B_.pdf	1687176 00dce058f4b60e64229aa5a73604ea5eabda9be5	no	37
Warnings:					
Information:					
3	Foreign Reference	TW201333497A_.pdf	2023999 5f7aafbdbe7fd8758b46422890d0d3bba8cfc31b	no	61
Warnings:					
Information:					
			Total Files Size (in bytes):	4323342	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kabbani et al.

Serial:	17/725,164	Confirmation No.	5389
Filed:	4/20/2022	Group Art Unit:	2868
Examiner:	Shah, Neel D.		
For:	Wafer Scale Active Thermal Interposer for Device Testing		

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL AMENDMENT

Dear Examiner Shah:

In response to the Official Action mailed 9/23/2022 and Applicants' Response of 12/20/2022, please enter the indicated amendments and the following remarks for filing in the above captioned patent application.

AEM Americas, Inc. - 1002
Page 228

In the Claims:

1. (currently amended) A system for testing circuits of an integrated circuit semiconductor wafer, the system comprising:

a tester system for generating signals for input to said circuits and for processing output signals from said circuits for testing said wafer;

a test stack coupled to said tester system, said test stack comprising:

a wafer probe for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer;

a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer; and

a cold plate disposed under said wafer TI layer and operable to cool said wafer; ~~and~~

a thermal controller for selectively heating and maintaining temperatures of said areas of said wafer by controlling cooling of said cold plate and by controlling selective heating of said wafer TI layer[[,]]; and

~~wherein said wafer TI layer comprises one or more alignment holes for aligning said wafer TI layer with structures of said test stack external to said wafer TI layer~~

a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical alignment holes which are aligned with said pins for allowing

AEM Americas, Inc. - 1002
Page 229

said pins to pass through said cold plate and said wafer TI layer to lift said wafer.

2. (previously presented) The system as described in Claim 1 further comprising a power supply coupled to provide power to said wafer TI layer and controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said selective heating of said wafer TI layer is based on said PWM signals.

3. (original) The system as described in Claim 2 further comprising:

a chiller for cooling liquid;

a valve for controlling an amount of said liquid flowing to said cold plate, wherein said valve is controlled by said thermal controller.

4. (original) The system as described in Claim 1 further comprising:

a first thermal interface material (TIM) layer disposed between said cold plate and said wafer TI layer; and

a second TIM layer disposed between said wafer TI layer and said wafer.

5. (original) The system as described in Claim 4 wherein said first and second TIM layers comprise indium foil.

6. (original) The system as described in Claim 4 further comprising:

a first vacuum valve for establishing suction for securing said wafer to said wafer TI layer;

a second vacuum valve for establishing suction for securing said wafer TI layer to said cold plate; and

a vacuum pump coupled to both said first and second vacuum valves.

7. (original) The system as described in Claim 6 further comprising:

a first blow-off valve for controlling air to release said wafer from said wafer TI layer;

a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and

a source of air coupled to both said first and second blow-off valves.

8. (original) The system as described in Claim 1 wherein said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and wherein said plurality of traces are operable to selectively heat a plurality of zones of said wafer TI layer under control of said thermal controller and wherein further said plurality of zones correspond to said areas of said wafer.

9. (original) The system as described in Claim 8 wherein positions of said plurality of zones of said wafer TI layer correspond to a die layout of said wafer and wherein further said wafer TI layer is customized for said wafer.

10. (original)The system as described in Claim 9 wherein each zone of said plurality of zones corresponds to a respective single die of said die layout of said wafer.

11. (original)The system as described in Claim 9 wherein each zone of said plurality of zones corresponds to a respective plurality of dice of said die layout of said wafer.

12. (original)The system as described in Claim 9 wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.

13. (canceled)

14. (original)The system as described in Claim 2 wherein:

said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and operable to selectively heat a plurality of zones of said wafer TI layer responsive to said PWM signals; and

AEM Americas, Inc. - 1002
Page 232

said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from said PWM signals applied to said plurality of traces.

15. (previously presented)A system for testing circuits of an integrated circuit semiconductor wafer, the system comprising:

a tester system for generating signals for input to said circuits and for processing output signals from said circuits for testing said wafer;

a test stack coupled to said tester system, said test stack comprising:

a wafer probe for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer;

a wafer thermal interposer (TI) layer operable to contact a bottom surface of said wafer and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone is operable to be discretely and selectively heated to selectively heat a respective area of said wafer,

wherein said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from activation of signals of said wafer TI layer; and

a cold plate disposed under said wafer TI layer and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of areas of said wafer by controlling cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said wafer TI layer.

16. (original)A system as described in Claim 15 wherein said wafer comprises a die layout comprising a plurality of dice and wherein further positions and shapes of said plurality of discretely controllable thermal zones are customized to said die layout of said wafer.

17. (original)A system as described in Claim 16 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to multiple dice of said die layout of said wafer.

18. (original)A system as described in Claim 16 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to a single die of said die layout of said wafer.

19. (original)A system as described in Claim 16 wherein each die of said die layout of said wafer corresponds to multiple thermal zones of said plurality of discretely controllable thermal zones of said wafer TI layer.

20. (original)The system as described in Claim 16 wherein said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and operable to selectively heat and maintain temperatures of said plurality of discretely controllable thermal zones of said wafer TI layer responsive to said thermal controller.

21. (original)The system as described in Claim 16 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

bringing a first thermal zone of said plurality of discretely controllable thermal zones to a testing temperature; and

while said tester system is testing one or more die of said die layout corresponding to said first thermal zone, simultaneously bringing a second thermal zone of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing one or more die of said die layout corresponding to said second thermal zone.

22. (original) The system as described in Claim 16 wherein said thermal controller comprises instructions for implementing a preconditioning method of said plurality of discretely controllable thermal zones of said wafer TI layer, said preconditioning method comprising:

AEM Americas, Inc. - 1002
Page 235

bringing a first set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature; and

while said tester system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of said plurality of discretely controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

23. (previously presented)A method for testing circuits of an integrated circuit semiconductor wafer, the method comprising:

testing said circuits of said wafer by using a tester system to generate signals for input to said circuits and to process output signals from said circuits; and

in conjunction with performing said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller controlling a thermal interposer layer and a cold plate, both disposed in proximity of said wafer and wherein said thermal interposer comprises a plurality of separately controllable thermal zones wherein each thermal zone is operable to be selectively heated and temperature maintained by said thermal controller; and

while said tester system is testing a first die of said wafer corresponding to a first thermal zone, simultaneously bringing a second thermal zone of said

AEM Americas, Inc. - 1002
Page 236

plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said wafer corresponding to said second thermal zone.

24. (original)A method as described in Claim 23 wherein said wafer comprises a die layout and wherein further positions and shapes of said plurality of separately controllable thermal zones of said thermal interposer layer are customized to said die layout.

25. (canceled)

26. (original)The method as described in Claim 24 wherein said selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller comprises:

bringing a first set of thermal zones of said plurality of separately controllable thermal zones to a testing temperature; and

while said tester system is testing a first die of said die layout corresponding to said first set of thermal zones, simultaneously bringing a second set of thermal zones of plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said die layout corresponding to said second set of thermal zones.

27. (previously presented)The system of Claim 1 wherein said thermal controller is further configured to precondition a first area of said wafer to achieve a desired test temperature in advance of testing said first area, while testing and controlling a temperature of a second area of said wafer.

AEM Americas, Inc. - 1002
Page 238

REMARKS

Claims 1-12, 14-24, 26, and 27 are pending in the present application. Claim 13 is canceled herein. Claim1 is amended. No new matter is added. Applicants respectfully request reconsideration of the present application in view of the indicated amendments and the following remarks.

The amendments presented herein incorporate indicated-allowable matter, and are believed to place the present application in condition for allowance. The present amendments are further believed to require no additional search or examination.

Claim Amendments

Claim 1 is amended to include material from originally presented and indicated-allowable Claim 13. Further, these claimed limitations find support at least in the embodiments disclosed in Figure 2, items 215, 221, and/or 230, and in the Specification at paragraphs [0017] and [0055], *inter alia*.

Examiner Interview Summary

Applicants' representatives and Examiner Shah conducted a series of Examiner Interviews. The amendments to Claim 1, presented herein, were discussed. The Examiner indicated that this amendment should place the application under condition for allowance.

Applicants thank the Examiner for the Interviews.

AEM Americas, Inc. - 1002
Page 240

CONCLUSION

Claims 1-12, 14-24, 26, and 27 are pending in the present application. All Claims are understood to incorporate indicated allowable material, and allowance of such claims is earnestly sought.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 504160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Date: January 4, 2023

/Anthony C. Murabito/
Anthony C. Murabito
Reg. No. 35,295

111 North Market Street
Suite 700
San Jose, California 95113
(408) 938-9060

Electronic Acknowledgement Receipt

EFS ID:	47316160
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Mina Oliveri
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	04-JAN-2023
Filing Date:	20-APR-2022
Time Stamp:	14:59:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		AATS-0107-02C01US_17-725164_Supplemental_Amendment_1-04-2023.pdf	66978 a9dfb42b3d351f5b55a2c43bc648687c634c104d	yes	14

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Supplemental Response or Supplemental Amendment	1	1
	Claims	2	11
	Applicant Arguments/Remarks Made in an Amendment	12	14
Warnings:			
Information:			
	Total Files Size (in bytes):	66978	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

109838 7590 01/18/2023

Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

EXAMINER	
SHAH, NEEL D	
ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 01/18/2023

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/725,164	04/20/2022	Samer Kabbani	AATS-0107-02C01US	5389

TITLE OF INVENTION: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	04/18/2023

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

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By fax, send to: (571)-273-2885

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(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/725,164	04/20/2022	Samer Kabbani	AATS-0107-02C01US	5389

TITLE OF INVENTION: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	04/18/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
SHAH, NEEL D	2858	324-754070

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

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❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
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NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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Page 245

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/725,164	04/20/2022	Samer Kabbani	AATS-0107-02C01US	5389

109838 7590 01/18/2023

Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

EXAMINER	
SHAH, NEEL D	

ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 01/18/2023

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice Requiring Inventor's Oath or Declaration	Application No. 17/725,164	Applicant(s) Samer Kabbani	
	Examiner SHAH, NEEL D	Art Unit 2858	

This notice is an attachment to the Notice of Allowability (PTOL-37), or the Notice of Allowability For A Design Application (PTOL-37D).

An inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 executed by or with respect to each inventor has not yet been submitted.

An oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each inventor (for any inventor for which a compliant oath, declaration, or substitute statement has not yet been submitted) MUST be filed no later than the date on which the issue fee is paid. See 35 U.S.C. 115(f). Failure to timely comply will result in ABANDONMENT of this application.

A properly executed inventor's oath to declaration has not been received for the following inventor(s):

If applicant previously filed one or more oaths, declarations, or substitute statements, applicant may have received an informational notice regarding deficiencies therein.

The following deficiencies are noted:

INFORMAL ACTION PROBLEMS

- A properly executed inventor's oath or declaration has not been received for the following inventor(s): **Samer Kabbani**, **Paul Ferrari**, **Ikeda Hiroki**, **Kiyokawa Toshiyuki**, **Gregory Cruzan**, and **Karthik Ranganathan**. Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

Questions relating to this Notice should be directed to the Application Assistance Unit at 571-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/725,164	Applicant(s) Kabbani et al.	
	Examiner NEEL D SHAH	Art Unit 2858	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 01/04/23.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-12,14-24 and 26-27 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 9/22/22, 12/07/22, 01/03/23.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☑ Interview Summary (PTO-413), Paper No./Mail Date. 01/03/23.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NEEL D SHAH/
Primary Examiner, Art Unit 2858

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 09/22/22, 12/07/22, 01/03/23 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

Response to Arguments

3. Applicant's arguments in light of claim amendment, see Remarks, filed 12/20/22 and 01/04/23, with respect to Non-Final Rejection have been fully considered and are persuasive. The rejection has been withdrawn.

Claim Status

4. Claims 1-12, 14-24, 26-27 are pending in the application. Claims 13 and 25 are cancelled.

Allowable Subject Matter

5. **Claims 1-12, 14-24, 26-27 are allowed**.

6. The following is an examiner's statement of reasons for allowance:

7. Regarding claim 1, the prior art of record taken alone or in combination fails to teach or suggest the limitation of "a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical alignment holes which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer" in combination with other limitations of the claim.

8. Claims 2-12, 14 and 27 are also allowed as they further limit claim 1.

9. Regarding claim 15, the prior art of record taken alone or in combination fails to teach or suggest the limitation of "wherein said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from activation of signals of said wafer TI layer" in combination with other limitations of the claim.

10. Claims 16-22 are also allowed as they further limit claim 1.

11. Regarding claim 23, the prior art of record taken alone or in combination fails to teach or suggest the limitation of "while said tester system is testing a first die of said wafer corresponding to a first thermal zone, simultaneously bringing a second thermal zone of said plurality of separately controllable thermal zones to a testing temperature in advance of testing a second die of said wafer corresponding to said second thermal zone" in combination with other limitations of the claim.

12. Claims 24 and 26 are also allowed as they further limit claim 23.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NEEL D SHAH whose telephone number is (571)270-3766. The examiner can normally be reached M-F: 9AM-5:30PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Judy Nguyen** can be reached on **571-272-2258**. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NEEL D SHAH/
Primary Examiner, Art Unit 2858

Examiner-Initiated Interview Summary	**Application No.** 17/725,164	**Applicant(s)** Kabbani et al.		
	Examiner NEEL D SHAH	**Art Unit** 2858	**AIA (First Inventor to File) Status** Yes	**Page** 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
NEEL D SHAH	Primary Examiner	Telephonic
Neal Osborn	Attorney	

Date of Interview: 03 January 2023

Issues Discussed:

Proposed Amendment(s)

Claim 1 was briefly discussed. Examiner stated that the currently amended claim 1 was not sufficient to overcome rejection. Amending claim 1 with dependent claim 13 was discussed. Supplemental amendment was filed on 01/04/23 to reflect this. See office action. -NS

/NEEL D SHAH/ Primary Examiner, Art Unit 2858	

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/725,164	Kabbani et al.
	Examiner	**Art Unit**
	NEEL D SHAH	2858

CPC								
Symbol							**Type**	**Version**
G01R	/	31	/	2887			F	2013-01-01
H01L	/	23	/	473			I	2013-01-01
G01R	/	31	/	318511			I	2013-01-01
F28F	/	2260	/	02			A	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	25	
/NEEL D SHAH/ Primary Examiner, Art Unit 2858	06 January 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20230106

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/725,164	Kabbani et al.
	Examiner	**Art Unit**
	NEEL D SHAH	2858

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G01R	/	31	/	20
G01R	/	31	/	26
G01R	/	31	/	28
G01R	/	1	/	04
G01R	/	1	/	067
G01R	/	1	/	073
G01R	/	1	/	44

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	25	
/NEEL D SHAH/ Primary Examiner, Art Unit 2858	06 January 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office

Part of Paper No.: 20230106

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/725,164	Kabbani et al.
	Examiner	**Art Unit**
	NEEL D SHAH	2858

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	11	10	19	19										
2	2	12	11	20	20										
3	3	13	12	21	21										
5	4		13	22	22										
6	5	4	14	23	23										
7	6	15	15	24	24										
8	7	16	16		25										
9	8	17	17	25	26										
10	9	18	18	14	27										

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	25	
/NEEL D SHAH/ Primary Examiner, Art Unit 2858	06 January 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office

Part of Paper No.: 20230106

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/725,164	Kabbani et al.
	Examiner	Art Unit
	NEEL D SHAH	2858

CPC - Searched*		
Symbol	Date	Examiner
(G01R31/00,20,26,28,31,3185 G01R1/04,067,073,44).cpc.	09/19/2022	NS
(G01R31/00,20,26,28,31,3185 G01R1/04,067,073,44).cpc.	01/06/2023	NS

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST search attached	09/19/2022	NS
IDS checked, ip.com searched, DP checked, inventor-assignee name search done	09/19/2022	NS
EAST search updated	01/06/2023	NS

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
G01R	31/00,20,26,28,31,3185 ;1/04,067,073,44	01/06/2023	NS

/NEEL D SHAH/ Primary Examiner, Art Unit 2868	

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2868
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	202043787	TW	A	2020-12-01	CELERINT LLC		

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2868
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

	1	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/NEEL D SHAH/	Date Considered	01/06/2023

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2868
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2022-09-22
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

Bibliographic Data

Application No: 17/725,164

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /NEEL D SHAH/ Examiner's Signature | Initials

Title: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
04/20/2022	324	2858	AATS-0107-02C01US
RULE			

APPLICANTS

Advantest Test Solutions, Inc., San Jose, CA, UNITED STATES

INVENTORS

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Kiyokawa Toshiyuki, Kukishi Saitama, JAPAN

Gregory Cruzan, Anaheim, CA, UNITED STATES

Karthik Ranganathan, Foothill Ranch, CA, UNITED STATES

CONTINUING DATA

This application is a CON of 17528002 11/16/2021

17528002 has PRO of 63115813 11/19/2020

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

04/22/2022

STATE OR COUNTRY

UNITED STATES

ADDRESS

Advantest c/o Murabito Hao & Barnes LLP

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San Jose, CA 95113

UNITED STATES

FILING FEE RECEIVED

$6,760

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6515470		2003-02-04	SUZUKI; ET AL	
	2	7138811		2006-11-21	MAHONEY; ET AL	
	3	7781883		2010-08-24	SRI-JAYANTHA; ET AL	
	4	8970244		2015-03-03	DI STEFANO; ET AL	
	5	9594113		2017-03-14	DAVIS; ET AL	
	6	10126356		2018-11-13	BARABI; ET AL	

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First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

	1	20060158207		2006-07-20	REITINGER	
	2	20090160472		2009-06-25	SEGAWA; ET AL	
	3	20110050268		2011-03-03	CO; ET AL	
	4	20140035715		2014-02-06	TAKAHASHI; ET AL	
	5	20150137842		2015-05-21	MURAKAMI; ET AL	
	6	20160247552		2016-08-25	KIM; ET AL	
	7	20190271719		2019-09-05	STERZBACH	
	8	20200041564		2020-02-06	COJOCNEANU; ET AL	
	9	20210183668		2021-06-17	CAGLE; ET AL	
	10	20210293495		2021-09-23	BARAKO; ET AL	
	11	20220206061		2022-06-30	RANGANATHAN; ET AL	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	2858
	Examiner Name	SHAH, NEEL D
	Attorney Docket Number	AATS-0107-02C01US

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	109716513	CN		2019-05-03	ROGERS CORP		
	2	110214270	CN		2019-09-06	TOYOTA MOTOR CO LTD		
	3	446682	TW		2001-07-21	SPEEDLINE TECHNOLOGIES INC		
	4	200620596	TW		2006-06-16	ULTRATECH INC		
	5	200628818	TW		2006-08-16	REITINGER ERICH		
	6	201226579	TW		2012-07-01	IND TECH RES INST		
	7	201229535	TW		2012-07-16	NIHON MICRONICS KK		
	8	201323883	TW		2013-06-16	CELADON SYSTEMS INC		
	9	201447325	TW		2014-12-16	SEIKO EPSON CORP		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	2858
	Examiner Name	SHAH, NEEL D
	Attorney Docket Number	AATS-0107-02C01US

	10	201608254	TW		2016-03-01	R&D CIRCUITS INC		
	11	201712459	TW		2017-04-01	DELTA DESIGN INC		
	12	201834134	TW		2018-09-16	SEMES CO LTD		
	13	202043787	TW		2020-12-01	CELERINT LLC		
	14	202004980	TW		2020-01-16	APPLIED MATERIALS INC		

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		

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EXAMINER SIGNATURE

Examiner Signature	/NEEL D SHAH/	Date Considered	01/06/2023

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2022-12-07
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	6	"17725164"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DK, EA, EE, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/14 11:57 AM
L2	0	("2022/0276301").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/09/14 12:05 PM
L3	84	("5239093" OR "10056225" OR "10163668" OR "10955466" OR "10983145" OR "20020026258" OR "20040017185" OR "20130181576" OR "20180189159" OR "20190162777" OR "20220137092" OR "5126656" OR "5164661" OR "5315240" OR "5420521" OR "6389225" OR "6498899" OR "6711904" OR "6825681" OR "6862405" OR "6985000" OR "7311782" OR "7659738" OR "7726145" OR "7830164" OR "8343280" OR "8772682" OR "8927907" OR "9307578" OR "10354785" OR "10656200" OR "10775408" OR "10908207" OR "11143697" OR	(US-PGPUB; USPAT)	OR	ON	ON	2022/09/14 12:06 PM

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L5	10	(Advantest NEAR2 (Test Solutions)).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DK, EA, EE,	OR	ON	ON	2022/09/14 12:06 PM

			ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L6	1908	((Kabbani NEAR2 Samer) (Ferrari NEAR2 Paul) (Hiroki NEAR2 Ikeda) (Toshiyuki NEAR2 Kiyokawa) (Cruzan NEAR2 Gregory) (Ranganathan NEAR2 Karthik)).inv.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DK, EA, EE, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/14 12:09 PM
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L15	117	12 13	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 10:16 AM
L16	58	("3700857" | "3836751" | "4126824" | "4357526" | "4374316" | "4624137" | "4684783" | "4744246" | "4777434" | "4808009" | "4909078" | "4956793" | "5059770" | "5126656" | "5164661" | "5315240" | "5352870" | "5420520" | "5420521" | "5539186" | "5550482" | "5605612" | "5643483" | "5669419" | "5672980" | "5740016" | "5751015" | "5821505" | "5911897" | "5940110" | "5977785" | "5982013" | "6389225" | "20020033391").pn. OR ("6825681").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/09/15 10:24 AM
L17	50	("20220155364" "20220187361" "20220268831" "20220178991" "20220206061" "20100052714" "20050206397" "7863915" "7579847" "6891385" "20030122567"	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/09/15 10:36 AM

		"20210396801" "6825681" "6985000" "20050007136" "20040012404" "6094059" "20220107360" "6094060" "5949246" "6549026" "20160131702" "20020047702" "6744270" "20020171133" "20080090429" "6791171" "7330041" "7621761" "20210183668" "8025097" "20020075023" "7138818" "20050017750" "20050026476" "20060240690" "7247035" "20070267188" "6525555" "20040174181" "11035898" "20070057684" "7688090" "6867611" "7772860" "20080297186" "6064213" "7396236" "20030107394" "6812718").pn.					
L18	38	"7436059"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 10:38 AM
L19	164	"5821505"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS,	OR	ON	ON	2022/09/15 10:39 AM

			IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L20	66	"5821505"	(US-PGPUB; USPAT)	OR	ON	ON	2022/09/15 10:39 AM
L21	10	((US-8653843-B2 OR US-7436059-B1 OR US-6825681-B2 OR US-5821505-A OR US-10955466-B2).did. AND USPT.dbnm.) OR ((US-20220206061-A1 OR US-20220187361-A1 OR US-20220178991-A1 OR US-20220155364-A1).did. AND DWPI.dbnm.) OR ((US-20210156891-A1).did. AND PGPB.dbnm.)	(USPAT; US-PGPUB; FPRS; USOCR; IBM_TDB; EPO; JPO; DERWENT; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN))	OR	ON	ON	2022/09/15 02:06 PM
L22	22592	((test$3 inspect$3 monitor$3) WITH (IC (integrated ADJ circuit) DUT (device ADJ under ADJ test) dice chip wafer)) AND ((thermal heat$3) WITH (wafer DUT (device ADJ under ADJ test))) AND (cool$3 WITH (wafer DUT (device ADJ under ADJ test))) AND ((control$3 adjust$3) WITH (thermal heat$3 cool$3 temperature))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:10 PM
L23	1097	((test$3 inspect$3 monitor$3) WITH (IC (integrated ADJ circuit) DUT (device ADJ under ADJ test) dice chip wafer)).ti,ab,clm. AND ((thermal heat$3) WITH (wafer DUT (device ADJ under ADJ test))).ab,clm. AND (cool$3 WITH (wafer DUT (device ADJ under ADJ test))).ab,clm. AND ((control$3 adjust$3)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO;	OR	ON	ON	2022/09/15 02:11 PM

		WITH (thermal heat$3 cool$3 temperature)).ab,clm.	JPO; DERWENT; IBM_TDB)				
L24	76144	(G01R31/00,20,26,28,31,3185 G01R1/04,067,073,44).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:12 PM
L25	61	23 AND 24	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:12 PM
L26	1981	(thermal ADJ actuator) SAME (heat$3) SAME (cool$3)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:21 PM
L27	4	24 AND 26	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB,	OR	ON	ON	2022/09/15 02:21 PM

			HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L28	15	22 AND 26	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:22 PM
L29	69	(thermal ADJ actuator) SAME (heat$3) SAME (cool$3) SAME wafer	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:23 PM
L30	2	26 AND 324/$.ccls.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2022/09/15 02:26 PM

			IBM_TDB)				
L31	77	(thermal ADJ actuator) SAME (heat$3) SAME (cool$3) SAME (wafer DUT probe)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:27 PM
L32	22	(thermal ADJ actuator) SAME (heat$3 ADJ2 (plate layer arm)) SAME (cool$3 ADJ2 (plate layer arm))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:34 PM
L33	49	("5021630" | "5104480" | "5194710" | "5255022" | "5420521" | "5525300" | "5541524" | "5570032").pn. OR ("5821505").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/09/15 02:43 PM
L34	14	((US-9400291-B2 OR US-8653843-B2 OR US-7436059-B1 OR US-6914446-B1 OR US-6825681-B2 OR US-5821505-A OR US-10955466-B2).did. AND USPT.dbnm.) OR ((US-20220206061-A1 OR US-20220187361-A1 OR US-20220178991-A1 OR US-20220155364-A1 OR US-20140062513-A1).did. AND DWPI.dbnm.) OR ((US-	(USPAT; US-PGPUB; FPRS; USOCR; IBM_TDB; EPO; JPO; DERWENT; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN))	OR	ON	ON	2022/09/15 02:46 PM

		20210350061-A1 OR US-20210156891-A1).did. AND PGPB.dbnm.)					
L35	1	34 AND (PWM (pulse ADJ width ADJ modulation) (pulse$1width ADJ modulation))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/15 02:46 PM
L36	9	34 AND (Control$4 WITH cool$3)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/16 05:15 PM
L37	0	34 AND ((indium ADJ foil) OR (carbon ADJ nanotube))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DK, EA, EE, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/19 11:13 AM
L38	14	((US-20220206061-A1 OR US-20220187361-A1 OR US-20220178991-A1 OR US-20220155364-A1 OR US-20140062513-	(USPAT; US-PGPUB; FPRS; USOCR; IBM_TDB; EPO; JPO; DERWENT; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS,	OR	ON	ON	2022/12/27 11:15 AM

		A1).did. AND DWPI.dbnm.) OR ((US-10955466-B2 OR US-6825681-B2 OR US-8653843-B2 OR US-7436059-B1 OR US-5821505-A OR US-9400291-B2 OR US-6914446-B1).did. AND USPT.dbnm.) OR ((US-20210156891-A1 OR US-20210350061-A1).did. AND PGPB.dbnm.)	CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN))				
L39	0	38 AND (align$4 NEAR4 (hole open$3) WITH (thermal interposer layer))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/12/27 11:20 AM
L40	236	((thermal ADJ2 actuator) SAME (heat$3) SAME (cool$3)) AND (align$4 NEAR3 (hole open$3))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/12/27 11:21 AM
L41	160	((thermal ADJ2 actuator) SAME (heat$3) SAME (cool$3)) AND (align$4 NEAR3 (hole open$3))	(US-PGPUB; USPAT)	OR	ON	ON	2022/12/27 11:21 AM
L42	10	((thermal ADJ2 actuator) SAME (heat$3 cool$3)) AND (align$4 NEAR3 (hole open$3) WITH (thermal interposer))	(US-PGPUB; USPAT)	OR	ON	ON	2022/12/27 11:23 AM

L43	17	("10126356" OR "20060158207" OR "20090160472" OR "20110050268" OR "20140035715" OR "20150137842" OR "20160247552" OR "20190271719" OR "20200041564" OR "20210183668" OR "20210293495" OR "20220206061" OR "6515470" OR "7138811" OR "7781883" OR "8970244" OR "9594113").pn.	(US-PGPUB; USPAT)	OR	ON	ON	2022/12/27 11:36 AM
L44	1	43 AND (align$4 NEAR4 (hole open$3) WITH (thermal interposer layer))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/12/27 11:40 AM
L45	68	38 43	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/12/27 11:42 AM
L46	0	45 AND ((ground shield$3 protect$3) WITH (wafer DUT (device ADJ under ADJ test) die) WITH ((electromagnetic ADJ2 interferance) EMI radiation))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV,	OR	ON	ON	2022/12/27 11:43 AM

			MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L47	0	26 AND ((ground shield$3 protect$3) WITH (wafer DUT (device ADJ under ADJ test) die) WITH ((electromagnetic ADJ2 interferance) EMI radiation))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/12/27 11:44 AM
L48	0	45 AND ((simultaneous$2 concurrent$2) WITH (thermal heat$3) WITH control$4)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/12/27 11:45 AM
L49	5	45 AND ((simultaneous$2 concurrent$2) WITH (thermal heat$3))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/12/27 11:45 AM
L50	15	((US-9400291-B2 OR	(USPAT; US-PGPUB;	OR	ON	ON	2022/12/30

		US-8653843-B2 OR US-7436059-B1 OR US-7138811-B1 OR US-6914446-B1 OR US-6825681-B2 OR US-5821505-A OR US-10955466-B2).did. AND USPT.dbnm.) OR ((US-20220206061-A1 OR US-20220187361-A1 OR US-20220178991-A1 OR US-20220155364-A1 OR US-20140062513-A1).did. AND DWPI.dbnm.) OR ((US-20210350061-A1 OR US-20210156891-A1).did. AND PGPB.dbnm.)	FPRS; USOCR; IBM_TDB; EPO; JPO; DERWENT; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN))				09:50 AM
L51	1	50 AND ((wafer thermal interposer layer) WITH (hole channel) WITH align$4)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DK, EA, EE, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/12/30 09:57 AM
L52	18	("651540" "201333497").pn.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DK, EA, EE, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/01/05 01:07 PM
L53	15	("5205132" | "6788084" | "6956390" | "7483769" | "7792597" | "7822586" | "20020014894" | "20030001605" | "20050224492" | "20050267645" |	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2023/01/05 01:21 PM

		"20070267188" | "20080161978" | "20130285686").pn. OR ("9400291").urpn. AND (PGPB | USPT | USOC).dbnm.					

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	0	((thermal ADJ2 (interposer actuator)) SAME (heat$3 cool$3)).clm. AND (align$4 NEAR3 (hole open$3) WITH (thermal interposer actuator)).clm. AND ((cold cool$3) NEAR4 (plate wafer)).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2023/01/05 01:11 PM
N2	9	((thermal ADJ2 (actuator interposer)) SAME (heat$3) SAME (cool$3) SAME (wafer DUT (device ADJ under ADJ test))).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2023/01/05 01:11 PM
N3	5	((thermal ADJ2 (actuator interposer)) SAME (heat$3 cool$3 cold) SAME (wafer DUT (device ADJ under ADJ test))).clm. AND ((ground shield$3 protect$3) WITH (wafer DUT (device ADJ under ADJ test) die) WITH ((electromagnetic ADJ2 interferance) EMI radiation)).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2023/01/05 01:24 PM
N4	4726	(G01R31/00,20,26,28,31,3185 G01R1/04,067,073,44).cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2023/01/05 01:26 PM
N5	0	(((test$3 inspect$3) WITH (IC wafer DUT (integrated ADJ circuit) (device ADJ under ADJ test))) SAME probe SAME ((thermal heat$3) NEAR3 (interposer actuator)) SAME ((cool$3 cold) NEAR3 (plate wafer))).clm. AND ((pin probe) WITH (hole	(US-PGPUB; USPAT)	OR	ON	ON	2023/01/05 01:30 PM

		through$1hole)).clm.					
N6	2	(((test$3 inspect$3) WITH (IC wafer DUT (integrated ADJ circuit) (device ADJ under ADJ test))) SAME probe SAME ((thermal heat$3) NEAR3 (interposer actuator)) SAME ((cool$3 cold) NEAR3 (plate wafer))).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2023/01/05 01:31 PM
N7	0	N4 AND (((test$3 inspect$3) WITH (IC wafer DUT (integrated ADJ circuit) (device ADJ under ADJ test))) SAME probe SAME ((thermal heat$3) NEAR3 (interposer actuator)) SAME (cool$3 cold)).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2023/01/05 01:31 PM
N8	0	N4 AND (((test$3 inspect$3) WITH (IC wafer DUT (integrated ADJ circuit) (device ADJ under ADJ test))) SAME probe).clm. AND ((control$4 adjust$4) WITH (heat$3 cool$3)).clm. AND (((thermal heat$3) NEAR4 (interposer actuator)) SAME (ground$3 NEAR2 shield$3)).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2023/01/05 01:33 PM
N9	0	(((test$3 inspect$3) WITH (IC wafer DUT (integrated ADJ circuit) (device ADJ under ADJ test))) SAME probe).clm. AND ((control$4 adjust$4) WITH (heat$3 cool$3)).clm. AND (((thermal heat$3) NEAR4 (interposer actuator)) SAME (ground$3 NEAR2 shield$3)).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2023/01/05 01:33 PM

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	651540	TW	B	2019-02-21	TERADYNE INC		
	2	201333497	TW	A	2013-08-16	ADVANTEST CORP		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
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EXAMINER SIGNATURE

Examiner Signature	/NEEL D SHAH/	Date Considered	01/06/2023

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2023-01-03
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	17725164
Filing Date	04/20/2022
First Named Inventor	Samer Kabbani
Title	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	AATS-0107-02C01US

SIGNATURE of Applicant or Patent Practitioner

Signature	/Anthony C. Murabito/	Date (Optional)	
Name	Anthony C. Murabito	Registration Number	35,295
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 109838

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

ADVANTEST TEST SOLUTIONS, INC.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	H. Kobayashi	Date (Optional)	Oct. 14, 2015
Name	Hiroshi Kobayashi		
Title	IP Department Manager		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	47389405
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Missy Isaac
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	18-JAN-2023
Filing Date:	20-APR-2022
Time Stamp:	14:44:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	AATS-0107-02C01US_POA_01-18-2023.pdf	750343 10364222bec00175089dd846ea814a5001bcaf66	no	2

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/725,164	04/20/2022	Samer Kabbani	AATS-0107-02C01US

CONFIRMATION NO. 5389

109838
Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

POA ACCEPTANCE LETTER

OC000000137239427

Date Mailed: 01/25/2023

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/18/2023.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/rnegga/

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(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8653843		2014-02-18	ANDO; ET AL	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	2858
	Examiner Name	SHAH, NEEL D
	Attorney Docket Number	AATS-0107-02C01US

	1	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17725164
	Filing Date	2022-04-20
	First Named Inventor	Samer Kabbani
	Art Unit	2858
	Examiner Name	SHAH, NEEL D
	Attorney Docket Number	AATS-0107-02C01US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2023-04-17
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	17725164
Filing Date:	20-Apr-2022
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Filer:	Anthony C. Murabito/Missy Isaac
Attorney Docket Number:	AATS-0107-02C01US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

Electronic Acknowledgement Receipt

EFS ID:	47855447
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Missy Isaac
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	17-APR-2023
Filing Date:	20-APR-2022
Time Stamp:	17:52:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	EFT
Payment was successfully received in RAM	$260
RAM confirmation Number	E20234GH54545426
Deposit Account	504160
Authorized User	Missy Isaac

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	AATS-0107-02C01US_IDS.pdf	612055 37fd83871f32a74c307b9ffecfcbb2dde4bcc6a5	no	4
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	38245 ca805b3f0faaa1c701a1cda22864e986532485a9	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	650300		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 17/528,002

filed on 11-16-2021.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: Samer Kabbani Date (Optional): 6/10/2022

DocuSigned by:
Signature: Samer Kabbani
C5F560F8A7464DB...

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Paul Ferrari Date (Optional): 7/27/22

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Ikeda Hiroki Date (Optional): 19Jan2023

Signature: Ikeda.Hiroki 池田浩樹

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Kiyokawa Toshiyuki Date (Optional): _____

Signature: T. Kiyokawa

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LEGAL NAME OF INVENTOR

Inventor: Gregory Cruzan Date (Optional): _____

Signature: Gregory Cruzan

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Karthik Ranganathan Date (Optional): 4/14/2022

Signature: [signature]

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This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	47863008
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Missy Isaac
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	18-APR-2023
Filing Date:	20-APR-2022
Time Stamp:	17:17:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	AATS-0107-02C01US_DECLARATIONS.pdf	850191 5fb6cee2409596c9f08f7905df2a1425b7859946	no	7

Warnings:

Information:	
Total Files Size (in bytes):	850191

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B – FEE(S) TRANSMITTAL

Complete and send this form, together with the applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By fax, send to: (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Advantest c/o Murabito, Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Mina Oliveri	(Typed or printed name)
/Mina Oliveri/	(Signature)
4-18-2023	(Date)

APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
17/725,164	04/20/2022	Samer Kabbani	AATS-0107-02C01US	5389

TITLE OF INVENTION: WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	04/18/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363)

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1.

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2. 3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Advantest Test Solutions, Inc.

(B) RESIDENCE: (CITY and STATE or COUNTRY): San Jose, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. Fees Submitted: ☑ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment (*Please first reapply any previously paid fee shown above*):

☑ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 504160

5. Change of Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29. NOTE: Absent a valid Certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27. NOTE: If the application was previously under micro entity status, checking this box will be taken as a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status. NOTE: Checking this box will be taken as a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Anthony C. Murabito/ Date 04-18-2023

Typed or printed name Anthony C. Murabito Registration No. 35,295

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	17725164
Filing Date:	20-Apr-2022
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Filer:	Anthony C. Murabito/Mina Oliveri
Attorney Docket Number:	AATS-0107-02C01US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1200**

Electronic Acknowledgement Receipt

EFS ID:	47863423
Application Number:	17725164
International Application Number:	
Confirmation Number:	5389
Title of Invention:	WAFER SCALE ACTIVE THERMAL INTERPOSER FOR DEVICE TESTING
First Named Inventor/Applicant Name:	Samer Kabbani
Customer Number:	109838
Filer:	Anthony C. Murabito/Mina Oliveri
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	AATS-0107-02C01US
Receipt Date:	18-APR-2023
Filing Date:	20-APR-2022
Time Stamp:	18:07:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	EFT
Payment was successfully received in RAM	$1200
RAM confirmation Number	E20234HI09009106
Deposit Account	504160
Authorized User	Mina Oliveri

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	AATS-0107-02C01US_Issue_Fee_Tran_4-18-2023.pdf	301718 1e118837c7381ac6c00dd8c9a9f0dfba198f7986	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37935 3025521a1bb303f61c03f2c0e8643e08dd7a935d	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	339653		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/725,164	04/20/2022	Samer Kabbani	AATS-0107-02C01US	5389

109838 7590 05/04/2023

Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

EXAMINER	
SHAH, NEEL D	

ART UNIT	PAPER NUMBER
2858	

NOTIFICATION DATE	DELIVERY MODE
05/04/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

acmadmin@mhbpatents.com
officeaction@mhbpatents.com

Notice of Allowability	Application No. 17/725,164	Applicant(s) Kabbani et al.	
	Examiner NEEL D SHAH	Art Unit 2858	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 04/20/23.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-12,14-24 and 26-27 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 04/17/2023.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NEEL D SHAH/
Primary Examiner, Art Unit 2858

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8653843		2014-02-18	ANDO; ET AL	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

	1	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/NEEL D SHAH/	Date Considered	05/01/2023

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	2858
Examiner Name	SHAH, NEEL D
Attorney Docket Number	AATS-0107-02C01US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Anthony C. Murabito/	Date (YYYY-MM-DD)	2023-04-17
Name/Print	Anthony C. Murabito	Registration Number	35295

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.S/

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17725164
Filing Date	2022-04-20
First Named Inventor	Samer Kabbani
Art Unit	3763
Examiner Name	LING, FOR K.
Attorney Docket Number	AATS-0107-02C01US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5126656		1992-06-30	Jones	
	2	5164661		1992-11-17	Jones	
	3	5315240		1994-05-24	Jones	
Change(s) applied to document, /S.D./ 1/19/2023	4	5239093		~~1994-07-12~~ 08/1993	~~Okano~~ Cheng	
	5	5420521		1995-05-30	Jones	
	6	6389225		2002-05-14	Malinoski , et al.	
	7	6498899		2002-12-24	Malinoski , et al.	
	8	6711904		2004-03-30	Law , et al.	

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UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/725,164	06/13/2023	11674999	AATS-0107-02C01US	5389

109838 7590 05/24/2023

Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street
Suite 700
San Jose, CA 95113

ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at https://patentcenter.uspto.gov/. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

The USPTO is implementing electronic patent issuance with a transition period, during which period the USPTO will mail a ceremonial paper copy of the electronic patent grant to the correspondence address of record. Additional copies of the patent (i.e., certified and presentation copies) may be ordered for a fee from the USPTO's Certified Copy Center at https://certifiedcopycenter.uspto.gov/index.html. The Certified Copy Center may be reached at (800)972-6382.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site http://pair.uspto.gov for additional inventors):

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Paul Ferrari, Mission Viejo, CA;
Ikeda Hiroki, Kukishi Saitama, JAPAN;
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Gregory Cruzan, Anaheim, CA;

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Advantest Test Solutions, Inc., San Jose, CA;

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United States Patent and Trademark Office
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Alexandria, VA 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.
17/725,164	13-JUN-23	11674999

Advantest c/o Murabito Hao & Barnes LLP
111 North Market Street Suite 700
San Jose, CA 95113

EGRANT NOTIFICATION

Your electronic patent grant (eGrant) is now available, which can be accessed via Patent Center at https://patentcenter.uspto.gov

The electronic patent grant is the official patent grant under 35 U.S.C. 153. For more information, please visit https://www.uspto.gov/electronicgrants

To:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313−1450	**REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK**

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Southern District of California on the following: _X_ Patents or ___ Trademarks:

DOCKET NO. 3:25−cv−02604−JES−BJW	**DATE FILED** 10/1/25	**US District Court** Southern District of California San Diego, CA
PLAINTIFF Advantest Test Solutions, Inc.		DEFENDANT AEM Holdings Ltd. , et al.
PATENT OR TRADEMARK NO.	**PATENT OR TRADEMARK NO.**	**PATENT OR TRADEMARK NO.**
1. 11,674,999	**6.** 12,259,428	**11.**
2. 12,320,841	**7.**	**12.**
3. 12,013,432	**8.**	**13.**
4. 12,085,609	**9.**	**14.**
5. 12,000,885	**10.**	**15.**

In the above−entitled case, the following patents(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY __ Amendment __ Answer __ Cross Bill __ Other Pleading	
PATENT OR TRADEMARK NO.	**PATENT OR TRADEMARK NO.**	**PATENT OR TRADEMARK NO.**
1.	**6.**	**11.**
2.	**7.**	**12.**
3.	**8.**	**13.**
4.	**9.**	**14.**
5.	**10.**	**15.**

In the above−entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGMENT

CLERK John Morrill	(BY) DEPUTY CLERK	DATE