UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AEM AMERICAS, INC.,

Petitioner

v.

ADVANTEST TEST SOLUTIONS, INC.,

Patent Owner

Case IPR2027-00006

U.S. Patent No. 11,674,999

DECLARATION OF JOSEPH C. MCALEXANDER III, P.E.

UNDER 37 C.F.R. § 1.68 IN SUPPORT OF PETITION

FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,674,999

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I. Introduction

1. I, Joseph C. McAlexander III declare as follows:

2. I have been retained as an expert consultant by Maier and Maier PLLC on behalf of AEM Americas, Inc. ("Petitioner") in this proceeding before the United States Patent and Trademark Office ("PTO") regarding U.S. Patent No. 11,674,999 ("the '999 Patent") (Ex 1001). I have been asked to provide my technical review, analysis, insights, and opinions regarding the references that form the basis for the alleged grounds of unpatentability set forth in the Petition. For this service, I am being compensated for my time, and I am reimbursed for actual expenses. I have no interest in the outcome of this proceeding, and my compensation is not dependent on the content of my opinions or the outcome of this proceeding.

II. Qualifications

3. I am an independent consultant. All opinions stated in this Declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience relating to the technology referenced in this Declaration.

4. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. A copy of my current curriculum vitae, which includes a more detailed summary of my education and professional and academic experience is provided as Appendix A to this Declaration.

The following provides an overview of some of my experience that is relevant to the matters set forth in this Declaration.

5. I am a Registered Professional Engineer (#79454) and the President of McAlexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 54 years and am a named inventor on 31 U.S. patents and a number of foreign patents.

6. I have extensive expertise in the subject matter area relevant to this matter, specifically the design, fabrication, and testing of integrated circuits, including that of thermal control and evaluation of said circuits. For example, I have over fourteen years of experience at Texas Instruments. There, I designed, developed, tested, and implemented circuits, processes, and procedures to assure product and process reliability. More specifically, I designed and managed the processing and productization of many types of integrated circuit devices, including, among others, dynamic and static storage devices, charge coupled devices (CCD) for imaging applications, electrically programmable and erasable non-volatile devices (EPROM / EEPROM) for instruction storage and access, logic devices, and controllers. I also was responsible for the design and use of many performance test

boards used in probe, final, and reliability testing and performance characterization of integrated circuits under varying temperature conditions as well as the creation and implementation of the testing programs used to evaluate the performance characteristics of the integrated circuits. Evaluations required precise thermal control for accurate testing.

7. Additionally, while at EPI for 5 years, I managed activities which included test and reliability board designs. Specifically, my experience in the industry and with engineers practicing in the industry informs my opinion as to the level of skill of individuals and the general state of the art.

8. Specifically, I have: designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both nonvolatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs; managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control; testing, analysis, and control involved use of mechanical

calibration and measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications; taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control; provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other), and products related to wireless tracking and geofencing; and designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

9. I am qualified to reach the opinions and conclusions stated in this Declaration. My opinions concerning the semiconductor wafer-test architecture (the tester, the wafer probe, the resistive-trace heater array, and the closed-loop thermal control) draw on my more than fifty years of hands-on experience designing, fabricating, and production-testing integrated circuits under controlled temperature.

10. In forming my opinions, I rely on my knowledge and experience in the fields relevant to this Declaration. I further rely on documents and information referenced in this Declaration.

11. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae attached to this Declaration.

III. Materials Reviewed

12. The opinions contained in this Declaration are based on the documents I have reviewed, my professional judgment, and my education, experience, and knowledge relating to wafer probe testing and related fields. In forming my opinions, I have reviewed all materials referenced by the Petition and all materials listed in the List of Exhibits provided in the Petition (as well as any other materials and information I reference in this Declaration).

13. My opinions contained in this Declaration are based on the documents I have reviewed and considered, as well as my knowledge and professional judgment. My opinions have been guided by my appreciation of how a person of ordinary skill in the art ("POSITA") would have understood the state of the art, the prior art, and the claims and the specification of the '999 Patent at the time of the alleged invention.

14. The time of the alleged invention of the ’999 Patent encompasses the time frames near and including November 19, 2020. I understand the application for the ’999 Patent claims priority to a provisional application (provisional application No. 63/115,813), which was filed on November 19, 2020. My opinions reflect how a POSITA (which I describe below) would have understood the ’999 Patent, the prior art to the ’999 Patent, and the state of the art at the time of the alleged invention.

IV. Understanding of Legal Principles

15. I am not a lawyer, and I will not provide legal opinions. Although I am not a lawyer, I have been advised that certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and validity of patent claims.

16. I understand that a patent claim is invalid if it is anticipated or rendered obvious over the prior art and that a claim can be unpatentable even if all requirements of the claim cannot be found in a single prior art reference. I further understand that invalidating a claim requires that the claim be anticipated or rendered obvious from the perspective of a POSITA at the time the invention was made.

17. In forming my analysis, opinions, and conclusions expressed in this Declaration, I have applied the legal principles set forth below, which were provided to me by counsel.

V. Types of Claims

18. I understand that there are two types of U.S. patent claims: 1) independent claims, and 2) dependent claims. I understand that independent claims only include the aspects stated in the independent claim. I further understand that dependent claims include the aspects stated in the independent claim, and any other aspects stated in any claim from which that dependent claim depends, as well as any limitations required by the dependent claim.

VI. Anticipation

19. I understand that a claim in an issued patent can be invalid if it is anticipated. In this case, "anticipation" means there is a single prior art reference that discloses every element of the claim, arranged in the way required by the claim, either expressly or inherently.

20. I understand that anticipation of a claim requires that every element of a claim is disclosed expressly or inherently in the single prior art reference. I understand that "inherent" disclosure means that the claim element, although not expressly described by the prior art reference, must necessarily be present based on the disclosure. I understand that a mere probability that the element is present is not sufficient to qualify as "inherent disclosure."

VII. Obviousness

21. I understand that a claim in an issued patent can be rendered invalid if it is obvious. Unlike anticipation, obviousness does not require that every element of the claim be in a single prior art reference. Instead, it is possible for claim elements to be described in different prior art references or that a claim element in a prior art reference might be modified, so long as there is motivation or sufficient reasoning to combine the references or make the modification and a reasonable expectation of success of doing so.

22. I understand that a claim is invalid for obviousness if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious from the perspective of a person of ordinary skill in the relevant art at the time the invention was made. I also understand that, when evaluating obviousness, one must consider obviousness of the claim "as a whole." This must be from the perspective of the person of ordinary skill in the relevant art at the time the invention was made.

23. I further understand that exemplary rationales that may support a conclusion of obviousness include:

a) combining prior art elements according to known methods to yield predictable results;

b) simple substitution of one known element for another to obtain predictable results;

c) use of known technique(s) to improve similar devices (methods or products) in the same way;

d) applying a known technique to a known device (method or product) ready for improvement to yield predictable results;

e) "obvious to try" - choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;

f) known work in one field of endeavor may prompt variations of the work for use in either the same field or a different field based on design incentives or other market forces if the variations are predictable to a POSITA; and

g) some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

24. In analyzing obviousness, I understand that it is important to understand the scope of the claims, the level of skill in the relevant art, the scope and content of the prior art, the differences between the prior art and the claims, and any "secondary considerations" (described below). I also understand that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve

similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Although I understand that it is not required, there may also be a specific "teaching, suggestion or motivation" to combine any first prior art reference with a second prior art reference. Such a "teaching, suggestion, or motivation" to combine the first prior art reference with the second prior art reference can be explicit or implicit and may provide further evidence of obviousness.

25. I understand that secondary (or objective) considerations are relevant to the determination of whether a claim is obvious. Such secondary (or objective) considerations can include evidence of commercial success caused by an invention, evidence of a long-felt need that was solved by an invention, evidence that others copied an invention, or evidence that an invention achieved a surprising or unexpected result, among others. I understand that such evidence must have a nexus or causal relationship to the elements of a claim to be relevant to a determination of obviousness of the claim.

26. I also understand that, at least in IPR proceedings, admissions in the patent or in the prosecution file history of the patent (Applicant Admitted Prior Art or "AAPA") can be used to establish background knowledge possessed by a

POSITA, to furnish a motivation to combine, to assess whether a patent's claims would have been obvious, and/or to supply a missing limitation.

VIII. Claim Construction

27. I understand that, for purposes of my analysis, the terms appearing in the patent claims should be interpreted according to their "ordinary and customary meaning" at the time the alleged invention was made. In determining the ordinary and customary meaning, the words of a claim are given the plain meaning that those words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to assist in the construction of a claim term. Additionally, treatises and dictionaries may be used, in limited circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of filing as long as such extrinsic input is consistent with the claim term as used in the claim.

28. For all claim terms considered in this Declaration, I have applied the ordinary and customary meaning of those terms as they would have been understood by a POSITA at the time the alleged invention was made. To the extent the Patent Owner proposes any constructions, or the Board construes any claims, I reserve the right to address such proposals or constructions. Under any reasonable construction

of the claims, it is my opinion that the prior art discloses and/or suggests all the limitations recited in challenged claims of the ’999 Patent.

IX. Person of Ordinary Skill in the Art

29. I understand that my assessment and determination of invalidity must be undertaken from the perspective of what would have been known or understood by a POSITA at the time of the earliest patent application supporting the ’999 Patent.

30. I have been informed and understand that the POSITA is not a real person, but rather a legal construct - a hypothetical person. This person is presumed to have known the relevant art at the time of the invention. I have been informed by counsel that relevant factors in determining the level of ordinary skill include (1) the educational level of the inventor, (2) the type of problems encountered in the art, (3) prior art solutions to those problems, (4) the rapidity with which innovations are made, (5) sophistication of the technology, and (6) the educational level of active workers in the field. I further understand that the person of “ordinary skill” is not a person of extraordinary skill in the art. In other words, this person of ordinary skill is not necessarily an expert in the field.

31. As of the alleged November 19, 2020 priority date, a POSITA would have held at least a bachelor’s degree in electrical engineering, mechanical engineering, or a related field, together with approximately two to three years of

experience in semiconductor test equipment or thermal management of electronic devices. Additional education could substitute for experience, and vice versa.

32. At the time of the alleged invention, I was a person of at least ordinary skill in the art, and I have applied the perspective of the POSITA in forming and expressing my opinions below.

X. Technical Background and the Prior Art

33. Wafer probing permits concurrent electrical testing of one or more individual, semiconductor integrated circuit dies while they remain part of the wafer, before singulation, by contacting the die bond pads with probe needles or a probe card connected to a test system. Because semiconductor device performance is temperature-dependent, wafer probers have long employed thermal chucks to heat or cool the wafer during testing.

34. By way of further background, semiconductors underlie virtually all modern electronics. Chips are fabricated as grid-like arrays of integrated circuits on silicon wafers (today most commonly 300mm in diameter), and ongoing miniaturization has steadily increased transistor density, operating performance, power requirements, and both the number and spacing of input/output (I/O) contact points. After fabrication, the wafer undergoes wafer test—also called wafer probe or sort—to separate good dies from bad before the wafer is diced and the good dies are

packaged, subjected to burn-in, and given a final test. A wafer test system typically comprises a tester (automatic test equipment or "ATE") that supplies power and test stimuli and captures responses, a test head that forms the electrical and mechanical interface to the probe card, and a prober and wafer handler that load the wafer, mount it on a wafer chuck, and raise each die into contact with the probe contact elements.

35. A probe card provides the temporary electrical interface between the test head and the die(s) under test, and generally comprises a probe head housing the contact elements, a space transformer (whether a discrete component or a fan-out of the contact elements), and a printed circuit board, sometimes with an interposer to aid planarization, within a rigid framework that minimizes deflection under contact forces. Probe cards, in use since at least the 1960s, fall into two families defined by the direction in which the contact elements meet the die I/Os: cantilever (needle) probes, which are typically limited to perimeter or linear bond-pad I/Os, and vertical probes—such as buckling-beam designs—which can contact I/Os anywhere on the die and can engage bond pads or solder bumps/columns.

36. Further, wafer testing of individual dies directly on the wafer can use precision probe needles brought into contact with the die bond pads before dicing and packaging, and explain that the wafer is ramped to a target test temperature (for example, on the order of -60°C to +150°C) and allowed to thermally stabilize before

probe contact, using a temperature-controlled chuck. *See* AnySilicon, Wafer Testing: Ultimate Guide (https://anysilicon.com/wafer-testing-ultimate-guide/). Electrical noise and crosstalk (producing fluctuating measurements and false parametric failures), wafer warpage and alignment drift (addressed with vacuum-backed chucks and backside fluid cooling), and low throughput and high test are recurring challenges in wafer testing, and they further note that excessive heat can degrade device functionality and lifespan, so that thermal testing is used to detect hotspots and thermal irregularities and to ensure adequate heat dissipation. AnySilicon, Wafer Testing: Ultimate Guide; Wafer World, The Depths of Wafer Testing and Quality Assurance in Semiconductor Production (Feb. 5, 2024) (https://www.waferworld.com/post/the-depths-of-wafer-testing-and-quality-assurance-in-semiconductor-production).

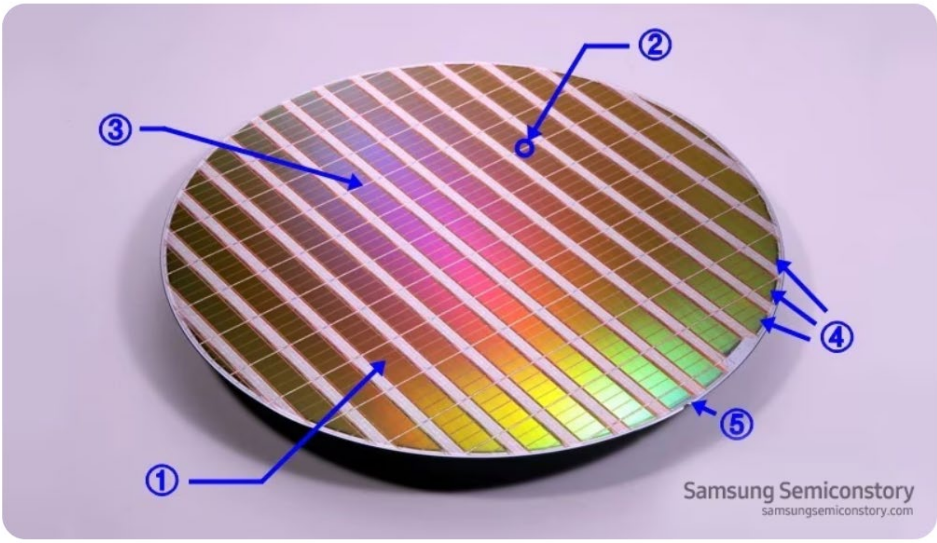
37. Early temperature-controlled chucks generally provided global heating or cooling of the entire wafer. Such systems used resistive heaters, chilled-liquid channels, heat sinks, and recirculating coolant to bring the wafer or chuck surface to a desired test temperature, together with temperature sensors such as resistance temperature detectors (RTDs) and a controller. As of the alleged priority date, wafer probe stations already incorporated temperature-controlled wafer chucks, probe pins connected to an electrical test system, heaters, chillers, cooling channels, sensors,

user interfaces, and controllers for maintaining the chuck at a desired test temperature.

38. As integrated circuits became more power-dense and wafer-level testing more demanding, global chuck control became insufficient. Individual dies could generate localized hot spots during testing, and different regions of the wafer could require independent thermal control. The art, therefore, progressed toward localized, die-specific thermal control—including arrays of resistive heating elements arranged to correspond to the IC devices on the wafer, each independently controlled and implementable using resistive heater traces—and subsequently toward more granular multi-zone heater structures, pulse-width-modulation (PWM) heater control, grounded electromagnetic-interference (EMI) shielding, and preconditioning of zones to reduce temperature-stabilization delay.

39. Each of these building blocks—wafer probing, fluid-cooled chucks or cold plates, die-corresponding heater arrays, resistive heater traces, independent zone control, PWM heater driving, grounded EMI shielding, and preconditioning to reduce temperature-stabilization delay—was separately known in the wafer-test and semiconductor thermal-control fields before the alleged invention.

40. An image of a wafer is below, showing the wafer itself with the individuals dies being tested.



① Chip: The thin and small piece on the wafer where the electrical circuits are embedded. The IC chip.
② Scribe Line: The border between the chip without any electrical circuits. Lines to separate each chip on the wafer.
③ TEG (Test Element Group): A chip to test whether it works or not.
④ Edge Die: The damaged part. A bigger wafer has less damage than a wafer with a smaller diameter, which also reduces the loss factor.
⑤ Flat Zone: The flat part to distinguish the round wafer structure.

41. *See* https://semiconductor.samsung.com/support/tools-resources/dictionary/semiconductor-glossary-wafer/.

XI. The '999 Patent

42. The '999 Patent is directed to a wafer-level test system that provides localized, zone-based thermal control of a wafer during active electrical probing. The Patent identifies the difficulty of maintaining accurate, localized wafer and die temperatures during wafer-level testing: conventional wafer probers and temperature-controlled chucks could heat or cool the wafer globally, but such systems struggled with localized thermal non-uniformity, die-specific hot spots,

temperature drift, and throughput loss caused by waiting for each die or wafer region to stabilize at the required test temperature. These problems are more acute for high-power or temperature-sensitive integrated circuits, whose dies may generate differing heat loads during testing.

43. To address these problems, the ’999 Patent describes a wafer-scale thermal interposer (“wafer TI”) layer positioned against the backside of the wafer. The wafer TI layer includes a plurality of zones arranged to selectively heat a plurality of thermal zones corresponding to areas of the wafer or its die layout. A cold plate provides a cooling baseline while the resistive traces provide localized heating above that baseline, and a thermal controller coordinates both the cooling of the cold plate and the selective heating of the resistive traces to bring and maintain selected wafer regions at target temperatures during electrical probing.

44. The challenged claims 1-25 recite this architecture and its variations, including per-die and multi-die zone correspondence, PWM-based heater control, a grounded shield layer for EMI protection, thermal-interface-material (TIM) layers, blow-off valves, a pin-lift mechanism, and zone-preconditioning methods, each of which I address in the Grounds below.

XII. Summary of Prior Art

45. The prior art relied upon in the Grounds below discloses each of the building blocks described above. I summarize each reference briefly here and apply it to the challenged claims in the Grounds that follow.

46. DiBattista (U.S. Patent No. 6,549,026) discloses a wafer-level test system having a fluid-cooled chuck (cold plate) and an array of independently controlled resistive heating elements arranged in correspondence with the integrated-circuit devices under test, such that each device aligns with a corresponding heater. A temperature control system coordinates the liquid cooling of the chuck and the selective heating of the individual elements to maintain each device at a set-point temperature during testing, and the heating elements may be implemented as resistive heater traces. DiBattista at 6:7-16, 6:21-37, 6:38-42, 7:59-8:2.

47. Herchen-1 (U.S. Patent Application Publication No. 2011/0000426) discloses a multilayer heater held by vacuum between top and bottom planar members, with heater elements arranged in a predetermined pattern forming independently controlled heating zones—for example, six zones, each with a separate temperature sensor—together with a movable top cooling plate, a fluid-channel bottom cooling plate, lift-pin holes extending through the plate stack, and a thermal-interface pad at the cooling interface. Herchen-1 at [0046]-[0054], FIG. 5.

48. Herchen-2 (U.S. Patent Application Publication No. 2008/0160462) discloses bake-plate heat-transfer control in a track lithography tool, using capacitive sensors to measure the gap between the substrate and a thin bake plate and chambered pressure control to deform the bake plate and compensate for wafer bow and non-uniform air gaps, thereby improving heat-transfer uniformity, with the bake plate coupled to a chill plate for rapid cooling. Herchen-2 at [0042], [0044], [0052].

49. Pease (U.S. Patent Application Publication No. 2013/0220989) discloses a substrate-support heating plate having multiple independently controllable planar heater zones in a scalable, multiplexed architecture, each zone sized to a single device die or a group of dies (at least 10, at least 100, and up to 1000 zones), with thin-film, screen-printed, wire-wound, or etched-foil heater elements, digital power control effected by time-division multiplexing and pulse-width modulation (PWM), a cooling plate containing channels for coolant flow, and lift pins. Pease at [0014], [0017], [0018], [0030], [0041], [0049], [0050].

50. Costello (U.S. Patent Application Publication No. 2002/0017916) discloses a temperature-controlled semiconductor wafer chuck for a probe test station, having a heat sink with internal cooling channels and structural pillars that resist deformation under probe-pin loads, a primary heater adjacent the wafer side and a secondary heater adjacent the stage side for independent dual-sided

temperature control, and temperature sensors (RTDs) with a controller that can use multiple sensors to detect and address localized hot spots—for example, by selecting the sensor nearest a die location or the sensor registering the highest temperature. Costello at [0019]-[0021], [0052]-[0053], [0066]-[0067], [0070]-[0076], [0080].

51. Sugiyama (U.S. Patent Application Publication No. 2004/0227536) discloses probers and probe-testing methods that provide accurate, localized temperature control of the tested wafer site while preventing chuck tilt under probe-needle pressure. Sugiyama teaches temperature-control cells sized to individual devices or groups of devices, each cell including a heater, a temperature sensor, and a heat exchanger governed by a temperature controller, with heat insulators between cells to reduce thermal cross-talk, and it teaches that heating or cooling large chuck areas is inefficient and slow, favoring localized, cell-matched thermal control. Sugiyama at [0020]-[0022], [0062]-[0070], [0077].

52. Parkhe (U.S. Patent Application Publication No. 2016/0111315) discloses an electrostatic chuck assembly for high-temperature substrate processing, having an electrically insulative upper puck plate with embedded heating elements and electrodes metal-bonded to a lower plate, which is fastener-coupled to a cooling plate with controlled force distribution and thermal-choke features to achieve uniform heat transfer, and which references multiple heating zones and thermal

isolators for shaping the lateral temperature profile. Parkhe at [0029], [0033], [0051], [0055]-[0056], [0065]-[0066], [0071].

XIII. GROUND 1: Claims 1-25 are Rendered Obvious Over DiBattista in View of Herchen-1, Herchen-2, Pease, and Natsuhara

53. Claims 1-25 of the '999 Patent are unpatentable under 35 U.S.C. § 103 as obvious over the below references.

A. OVERVIEW OF GROUND 1

54. DiBattista discloses a wafer-level test system in which an array 129 of independently controlled resistive heating elements 149 is disposed on a fluid-cooled chuck 122 in one-to-one correspondence with the integrated-circuit devices under test on the wafer, and in which a temperature control system 140 maintains each device at a set-point temperature by controlling both the liquid cooling of the chuck and the selective heating of the individual elements. DiBattista at 6:7-16, 6:21-37, 6:38-42, 7:37-44, 7:59-8:2, 8:50-57. DiBattista, therefore, supplies the test architecture, the zone-selective heating mapped to circuit positions, the cold plate, and the dual heating-and-cooling thermal controller recited in claim 1.

55. To the extent the Patent Owner contends that DiBattista's array of trace-based heating elements does not, standing alone, satisfy the requirement of "a plurality of resistive traces traversing said wafer TI layer" arranged to selectively heat "a plurality of zones" corresponding to areas of the wafer, Herchen-1 expressly

discloses that limitation. Herchen-1 discloses a heater layer in which a conducting layer 304 carries heater elements arranged in a predetermined pattern, etched onto the conducting layer and arranged to form six independent heating zones, each individually controlled and each having a separate temperature sensor. Herchen-1 at [0051], [0054], FIG. 5. Herchen-1 further discloses a movable top cooling plate 220 and a fluid-channel bottom cooling plate 230 positioned below the heater-bearing planar members, together with lift-pin holes 210 extending through the plate stack. Herchen-1 at [0048]-[0050].

56. DiBattista discloses the wafer-test architecture recited in claim 1, including an array 129 of independently controlled resistive heating elements 149 disposed on a fluid-cooled chuck in correspondence with the integrated-circuit devices under test, each element implemented with a "heater trace" that "provides the heat energy," each "controlled independently of the others," and a temperature control system 140 that maintains each device at a set-point temperature. DiBattista at 6:7-16, 6:21-37, 6:38-42, 7:59-8:2. Pease supplies the added features of the dependent claims addressed in this Ground. Pease discloses "multiple independently controllable planar heater zones in the substrate support assembly to enable the apparatus to actively create and maintain the desired spatial and temporal temperature profile" (Pease at [0014]), in which each zone is "of similar size to or

smaller than a single device die or group of device dies on the substrate so that the substrate temperature . . . can be controlled for each device die position to maximize the yield of devices from the substrate." Pease at [0030]. Pease's "scalable architecture" accommodates "die-by-die substrate temperature control (typically more than 100 dies on a substrate of 300-mm diameter)" (Pease at [0030]), with a heating plate that "can have at least 10, at least 100 and up to 1000 heater zones." Pease at [0049]. The heater elements "may be thin film resistive heaters" and "may be screen printed, wire wound or etched foil heaters." Pease at [0017]. Pease further discloses a controller 1000 that includes "logic (hardware or software) to control at least one power supply" (Pease at [0041]), digital power control in which "control is then effected by time division multiplexing and Pulse Width Modulation (PWM) techniques" (Pease at [0050]), "a cooling plate 105 containing channels 106 for coolant flow" (Pease at [0018]), and "lift pins for lifting the substrate." Pease at [0030].

57. The references address the same problem - spatially resolved, zone-level heating of a wafer-scale substrate supported over a fluid-cooled plate - and their teachings are complementary. Implementing DiBattista's per-die wafer-test heater array with Pease's scalable, multiplexed array of independently controllable planar heater zones sized to the device dies, together with Pease's PWM power

control and lift-pin arrangement, amounts to no more than combining prior-art elements according to known methods, and applying a known technique to a known device ready for improvement, to yield the predictable result of finer zone-selective heating mapped to the die layout. A person of ordinary skill in the art would have had a reasonable expectation of success in doing so, as confirmed by the following explanation.

58. The reasonable expectation of success follows from the references themselves. DiBattista already reduced the base architecture to practice. It discloses a working closed-loop thermal control system in which a liquid-cooled chuck is held below a set point and each resistive heating element is driven, through a dedicated thermal control board and power amplifier, to hold its corresponding device at the set-point temperature, with multiple thermal control boards enabling simultaneous, independent operation of a plurality of heating elements each thermally coupled to an individual device under test. DiBattista at 6:7-16, 7:59-8:2; *see* FIGS. 6-9. Because DiBattista demonstrates that per-element, feedback-controlled heating over a fluid-cooled heat sink actually works at the wafer level, a POSITA implementing the combination faced only the routine task of increasing the number and granularity of those elements. Pease confirms that this scaling was predictable and well within the ordinary level of skill: its scalable, multiplexed heater architecture "can readily

accommodate the number of planar heater zones required for die-by-die substrate temperature control (typically more than 100 dies on a substrate of 300-mm diameter),” with a heating plate having “at least 10, at least 100 and up to 1000 heater zones.” Pease at [0030], [0049]. Pease further teaches that the heater elements may be thin film resistive heaters and may be screen printed, wire wound or etched foil heaters - conventional, manufacturable constructions - and that power to the individual zones is controlled by established "time division multiplexing and Pulse Width Modulation (PWM) techniques, which Pease describes as simpler and more efficient. Pease at [0017], [0050]. These are mature techniques used for their ordinary purpose, and a POSITA would have expected them to perform as described when applied within DiBattista’s existing control architecture. The combination thus assembles known elements performing their known functions to yield no more than the predictable result of finer zone-selective heating mapped to the die layout, and a POSITA would have had a reasonable expectation of success in achieving it.

59. A person of ordinary skill in the art would have been motivated to combine DiBattista and Herchen-1. Both references address the same problem - spatially controlled, zone-selective heating of a wafer-scale substrate using a patterned resistive heater layer over a liquid-cooled plate. Implementing DiBattista’s per-die heater array with Herchen-1’s etched, patterned resistive heater traces

arranged in individually controlled zones traversing the heater layer amounts to no more than applying a known heater-trace construction to a known wafer-test chuck ready for improvement, combining prior-art elements according to known methods to yield the entirely predictable result of zone-selective heating mapped to the die layout. A skilled artisan would have had a reasonable expectation of success in doing so.

60. Further, not only are the teachings of the DiBattista and Herchen-1 references complementary, the combination of DiBattista and Herchen-1 would also be obvious to try with a reasonable expectation of success. Controlled heating in a zone as taught by Herchen-1 would assist in the transition to temperature for the die-under-test according to the teaching of DiBattista.

61. A POSITA's reasonable expectation of success in combining DiBattista with Herchen-1 is confirmed by the specific, compatible disclosures of the two references. Herchen-1 does not merely suggest patterned resistive heaters in the abstract; it discloses a concrete, buildable construction in which the heater elements are "etched onto" a conducting layer "arranged to form six independent heating zones with a separate temperature sensor for each zone," and it identifies screen printing and bonding as alternative known fabrication methods for the same structure. Herchen-1 at [0051]. Herchen-1 also supplies the cooperating cold-plate

structure - a fluid-channel bottom cooling plate 230 - of the same kind DiBattista already employs. Herchen-1 at [0050]. Implementing DiBattista's individually controlled heating elements as Herchen-1's etched, per-zone resistive traces is a like-for-like exchange of one known resistive-heater construction for another within the same wafer-scale, liquid-cooled thermal architecture. The underlying operating principle - passing current through a patterned resistive trace to heat a corresponding region under closed-loop sensor feedback - is identical in both references, and neither teaches away from, or suggests any incompatibility with, the other. A POSITA would accordingly have expected Herchen-1's etched, zoned heater to function in DiBattista's system exactly as it functions in Herchen-1's, and would have had a reasonable expectation of success.

62. Further, combining with Herchen-2 would have been obvious. Herchen-1 and Herchen-2 share an inventor. Both references are directed to thermal processing in track lithography tools used for photolithography sequences including bake and chill operations in multi-chamber systems. Herchen-2 addresses non-uniform heat transfer arising from wafer bow and varying wafer-to-plate air gaps, and provides methods to measure wafer shape and compensate by deforming a flexible bake plate using chambered pressure control. Herchen-1 addresses limitations of conventional heaters that are bonded or printed onto plates, including

Coefficient of Thermal Expansion (CTE) mismatch warping, maintenance cost, and inflexibility, by holding a multilayer heater between top and bottom planar members using vacuum in an evacuated region.

63. Herchen-2 teaches that gap non-uniformity from wafer bow degrades uniform heating and proposes active plate shape control via chamber pressures informed by capacitive measurements. Herchen-1 teaches vacuum-held heater layers to avoid CTE-induced warping from permanent bonds and to enable easy replacement or reconfiguration of heater elements, reducing Cost of Ownership (CoO). A POSITA would have recognized that integrating a vacuum-retained multilayer heater (Herchen-1) with a deformable, pressure-actuated bake plate with sensing (Herchen-2) addresses both heat-transfer uniformity and maintainability in the same thermal module.

64. Further, Herchen-2 contemplates heater elements embedded in or forming electrodes on a thin bake plate surface; and multi-zone heating is conventional in this context. Herchen-1 provides a known multilayer heater architecture with single- and multi-zone patterns that is designed to be sandwiched between planar members and held by vacuum. Substituting Herchen-1's multilayer, vacuum-held heater for the heater implementation in Herchen-2's bake plate is a

like-for-like swap of heater technology in an established bake plate assembly to achieve predictable heating functionality with improved serviceability.

65. The addition of Herchen-2 to the combination would also be obvious to try with a reasonable expectation of success. Controlled heating in a zone as taught by Herchen-1, assisted by a like-for-like swap of heater technology by Herchen-2 would further enhance in the transition to temperature for the die-under-test according to the teaching of DiBattista.

66. The reasonable expectation of success extends to the addition of Herchen-2. Herchen-1 and Herchen-2 share an inventor and address the same genre of thermal-processing module, and Herchen-2's contribution - measuring wafer-to-plate gap non-uniformity with capacitive sensors and compensating for it by deforming a flexible plate through chambered pressure control - operates independently of, and does not disturb, the resistive-heating function supplied by DiBattista and Herchen-1. Herchen-2 at [0042], [0044], [0052]. Integrating Herchen-2's gap sensing and plate-shape compensation with the vacuum-retained multilayer heater of Herchen-1 combines two separately disclosed, non-conflicting improvements within the same bake/chill thermal module, each performing its ordinary function. Because each reference supplies a mature, independently demonstrated capability, and because combining them requires no change to the

underlying operating principle of any one of them, a POSITA would have had a reasonable expectation that the combined system would achieve the predictable result of uniform, serviceable, zone-selective thermal control.

B. INDEPENDENT CLAIM 1

67. DiBattista in view of Herchen-1, Herchen-2, and Pease render obvious every limitation of claim 1, as described above. Below, I address the lift mechanism limitation of claim 1.

1. [1.g]: a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical alignment holes which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer.

68. DiBattista in view of Pease renders this element obvious. Pease discloses a lift-pin mechanism for the substrate support. Although the pins are not separately illustrated, Pease teaches that "the substrate support assembly can comprise features such as lift pins for lifting the substrate" (Pease at [0030]) and describes "a lifting pin arrangement for raising and lowering a substrate." Pease at [0055]. Pease further discloses routing conductors "through holes or conduits in the cooling plate" (Pease at [0040]), with "feedthroughs in the cooling plate" (Pease at [0030]), confirming that vertical pass-through features extending through the cooling plate were conventional. It would have been obvious to provide DiBattista's

fluid-cooled chuck with Pease's lift-pin arrangement and to align the pass-through channels through both the cold plate and the wafer TI layer, so that the pins pass through both the cold plate and the wafer TI layer to lift the wafer. A POSITA would have been motivated to add such a lift-pin mechanism to load and unload wafers from the heated surface without side access.

C. DEPENDENT CLAIM 4: The system as described in claim 2 wherein: said wafer TI layer comprises a plurality of traces traversing said wafer TI layer and operable to selectively heat a plurality of zones of said wafer TI layer responsive to said PWM signals; and said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from said PWM signals applied to said plurality of traces.

69. Herchen-1 discloses a multi-layer heater stack with insulating layers 301, 303, 305 isolating the conducting layers. Herchen-1 at [0051]-[0052]. Adding a grounded shield layer would have been obvious to a POSITA who would have known of the benefits to shield electrical components from electrical radiation. A POSITA would have drawn on Natsuhara (U.S. Pat. Pub. No. 2007/0205787), which teaches forming a grounded electrically conductive layer over the resistance heat generator in a wafer prober to shield the wafer from electromagnetic waves that would otherwise disturb the measurement of very low currents, and teaches that

connecting a grounding line to that conductive layer blocks almost all such electromagnetic waves. Natsuhara at [0012], [0024].

D. DEPENDENT CLAIM 8: The system as described in claim 7 further comprising: a first blow-off valve for controlling air to release said wafer from said wafer TI layer; a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and a source of air coupled to both said first and second blow-off valves.

70. Herchen-1 discloses regulated vacuum lines at both interfaces (ports 214 and 222, regulators 251, 271, house vacuum system 290) that are relieved to release the substrate and separate the plates during load/unload. Herchen-1 at [0046]-[0049]. It would have been obvious to a POSITA to use positive-pressure blow-off valves or an air source for releasing the wafer. Releasing a vacuum-secured substrate with a positive air pulse is a conventional complement to release vacuum. As noted below, Costello likewise discloses vacuum securing of the wafer at the chuck that is relieved during load and unload, confirming that controlling air and vacuum to release the wafer was conventional. Costello at [0052]-[0053].

E. DEPENDENT CLAIM 10: The system as described in claim 9 wherein positions of said plurality of zones of said wafer TI layer correspond to a die layout of said wafer and wherein further said wafer TI layer is customized for said wafer.

71. DiBattista in view of Herchen-1 renders claim 10 obvious. In DiBattista, "[e]ach heating element 149 in the array 129 has a size and shape corresponding to that of the associated IC device to be tested on the wafer and the

pattern of heating elements 149 matches that of the devices on the wafer." DiBattista at 6:21-37. The regions of the chuck "correspond to respective ones of the plurality of integrated circuit devices formed on the wafer," so the positions of the heating zones correspond to, and the layer is customized for, the die layout of the wafer. DiBattista at 3:15-20. Herchen-1's etched heater elements likewise are arranged in a predetermined pattern forming individually controlled zones. Herchen-1 at [0051].

F. DEPENDENT CLAIM 12: The system as described in claim 10 wherein each zone of said plurality of zones corresponds to a respective plurality of dice of said die layout of said wafer.

72. DiBattista teaches that each heating element has "a size and shape corresponding to that of the associated IC device," DiBattista at 6:21-37, and Herchen-1 teaches a conducting layer 304 whose heater elements form a limited number of individually controlled zones (e.g., six independent zones), Herchen-1 at [0051]. It would have been obvious to size the zones of the DiBattista-Herchen-1 heater layer so that each zone corresponds to a respective plurality of dice, as a matter of routine design choice in matching zone granularity to the die layout, yielding predictable temperature control of groups of dice.

G. DEPENDENT CLAIM 13: The system as described in claim 10 wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.

73. DiBattista in view of Pease renders claim 13 obvious. DiBattista discloses per-device heating elements each having "a size and shape corresponding to that of the associated IC device," each "controlled independently of the others." DiBattista at 6:21-37, 6:38-42. Pease discloses that the planar heater zones can be made finer than a die: "each planar heater zone of the heating plate is of similar size to or smaller than a single device die or group of device dies on the substrate so that the substrate temperature . . . can be controlled for each device die position to maximize the yield of devices from the substrate." Pease at [0030]. Pease's "scalable architecture" accommodates "die-by-die substrate temperature control (typically more than 100 dies on a substrate of 300-mm diameter)," Pease at [0030], and the heating plate "can have at least 10, at least 100 and up to 1000 heater zones." Pease at [0049]. Applying Pease's sub-die zone granularity to DiBattista's wafer-test chuck yields a wafer TI layer in which each die of the die layout corresponds to multiple respective zones, achieving the predictable benefit of finer intra-die thermal control.

H. DEPENDENT CLAIM 14: The system of claim 1 wherein said thermal controller is further configured to precondition a first area of said wafer to achieve a desired test temperature in advance of testing said first area, while testing and controlling a temperature of a second area of said wafer.

74. DiBattista discloses independent control of each heating element (DiBattista at 6:38-42), and testing "at high speed" with the temperature of each device "controlled independently of the other devices on the wafer during a test" (DiBattista at 12:26-31), executed by a system controller 160 (DiBattista at 7:59-8:2). Staged preconditioning follows from DiBattista's independent zone control and high-speed testing. Programming the controller to precondition a next zone during testing would have been obvious to ensure expediency of testing moving from one die to the next. Pease reinforces this, disclosing multiple independently controllable planar heater zones that actively create and maintain a desired spatial and temporal temperature profile across the substrate, which enables a zone to be brought to temperature in advance of testing. Pease at [0014], [0030].

XIV. GROUND 2: Claims 1-25 are Rendered Obvious Over DiBattista in View of Costello, Herchen-1, and Criminale

75. Claims 1-25 of the '999 Patent are unpatentable under 35 U.S.C. § 103 as obvious over the below references.

A. OVERVIEW OF GROUND 2

76. *See* description of DiBattista contained in Ground 1.

77. A person of ordinary skill would have been motivated to combine DiBattista's per-device, feedback-controlled thermal regulation at wafer level with Costello's mechanically rigid, dual-sided thermally managed chuck architecture and

noise/leakage mitigation to achieve improved probe-test performance, with a reasonable expectation of success. DiBattista teaches an apparatus with a heat exchanger/chuck having a surface divided into regions corresponding to IC devices, where each device's temperature is individually controlled during testing. DiBattista at Abstract, claim 1, FIGS. 10A-10B. It further teaches embodiments with multiple heating elements on a fluid-cooled chuck acting as a heat sink, and alternative separate heat exchanger bodies, enabling rapid compensation for device self-heating and per-DUT control. DiBattista at col. 5, col. 8, FIGS. 8A-8B, 10A-10B. Costello identifies the problem of insufficient rigidity in temperature-controlled chucks subjected to high probe-pin loads and teaches a heat sink with internal pillars that both carry coolant and transmit compressive forces to prevent deformation. Costello at [0008]-[0009], [0014], [0077]. Costello teaches independently controlling the temperatures of the top and bottom (prober-facing) sides of the chuck using a primary heater near the wafer side, a secondary heater near the stage side, and a cooler, to maintain wafer temperature while protecting the prober stage from thermal drift. Costello at [0013], [0018], [0051], [0059], [0064].

78. A POSITA would have been motivated to combine DiBattista and Costello as DiBattista targets per-DUT temperature accuracy and Costello provides arrays of sensors and controller algorithms to detect and address localized non-

uniformities and hotspots. DiBattista at claim 1, FIGS. 8A, 10A-10B; Costello at [0017], [0066]-[0067]. DiBattista provides per-device temperature control during test and Costello teaches multiple sensors and algorithms (e.g., averaging, hotspot-focused control) to handle local non-uniformities. Costello at [0062], [0066]-[0068].

79. A person of ordinary skill would view Costello's sensor arrays and control strategies as directly complementary to DiBattista's per-DUT loops, improving spatial resolution and dynamic response to device self-heating and local hotspots that DiBattista seeks to counteract. Costello at [0017], [0066]-[0067]; DiBattista at col. 5, FIGS. 8A-8B. DiBattista's multiple heaters with a fluid-cooled heat sink enable rapid compensation for device self-heating. DiBattista at col. 5, col. 8, FIGS. 8A-8B. Deploying Costello's multi-sensor feedback with DiBattista's power-following control would increase robustness against local thermal anomalies, yielding tighter per-DUT temperature regulation during probing. DiBattista at col. 9-10, FIG. 9; Costello at [0066]-[0067]. DiBattista's control electronics use embedded sensors and device power monitoring and Costello motivates noise reduction by gradual, continuous power changes to avoid measurement noise from electromagnetic fluctuations. DiBattista at col. 9, FIGS. 6-7; Costello at [0017], [0070]-[0071].

80. Further, not only are the teachings of the DiBattista and Costello references complementary, the combination of DiBattista and Costello would also be obvious to try with a reasonable expectation of success. The addition of multi-sensor feedback, as taught by Costello, would assist in temperature calibration and maintenance for the die-under-test according to the teaching of DiBattista. Costello at [0066]-[0068]; DiBattista at col. 11-12, FIG. 9.

81. A POSITA would have had a reasonable expectation of success in combining DiBattista and Costello because the two references share the same closed-loop, resistive-heater-over-fluid-cooled-chuck paradigm and because Costello's additions plug directly into DiBattista's existing control chain without altering its operating principle. DiBattista at col. 8, FIGS. 2C, 8B; Costello at [0006], [0016], [0055]. DiBattista already drives each heating element from a computed temperature-control signal through a power amplifier under RTD feedback. DiBattista at 7:59-8:2; *see* FIGS. 6-9. Costello teaches the same mode of control - feedback from the temperature sensors is used to adjust the temperature of the coolant, and the primary and secondary heaters - and supplies refinements that are simply additive to it: multiple RTDs with selectable averaging algorithms, and the ability to "control the chuck temperature top temperature based on the local temperature of the device under test" by selecting the sensor nearest a die or the

sensor registering the highest temperature to locate and counteract a hot spot. Costello at [0066]-[0067]. Costello also teaches a mechanically rigid heat sink whose internal pillars transmit force applied to the first side of the chuck through the heat sink so that the chuck resists deformation due to forces applied to a top surface, addressing probe-pin loads without changing the thermal control scheme. Costello at [0014], [0019]-[0021], [0077]. Because Costello's multi-sensor feedback, hot-spot logic, and structural rigidity each operate through, and are compatible with, the feedback-controlled heater architecture that DiBattista already discloses, a POSITA would have expected their combination to yield the predictable result of tighter, more robust per-die temperature regulation under probe load, with a reasonable expectation of success.

B. INDEPENDENT CLAIM 1

82. DiBattista in view Costello render obvious every limitation of claim 1, as set forth above. Below, I address the TI layer and lift mechanism limitations of claim 1.

1. [1.d]: a wafer thermal interposer (TI) layer operable to contact a second surface of said wafer and operable to selectively heat areas of said wafer; and

83. *See* discussion of DiBattista for this element in Ground 1.

84. In the DiBattista-Costello combination, DiBattista supplies the plurality of resistive-trace heating elements arranged in one-to-one correspondence with the

devices on the wafer, selectively heating a plurality of zones corresponding to areas of the wafer, as set forth for this element in Ground 1. Costello supplies the mechanically rigid, dual-sided temperature-controlled chuck and the array of temperature sensors that localize control of hot spots at each device under test. Costello at [0054-56], [0016], [0079], [0066]. Costello discloses a chuck top plate carrying a primary resistance-coil heater directly beneath the wafer, together with an array of temperature sensors enabling localized temperature control at the device under test. A POSITA would have implemented DiBattista's per-device resistive-trace zones on Costello's rigid, sensor-instrumented chuck, yielding a wafer TI layer whose resistive traces selectively heat a plurality of zones corresponding to areas of the wafer under closed-loop, localized control.

2. [1.g]: a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical alignment holes which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer.

85. *See* discussion of DiBattista for this claim in Ground 1.

86. Costello discloses this element. Costello at [0080]. It would have been obvious to a POSITA to use loading pins, as such were known and common method to load and unload wafers being tested. Herchen-1 and Pease confirm that pin-lift loading was conventional, with Herchen-1 disclosing lift-pin holes extending

through the plate stack and Pease disclosing lift pins for lifting the substrate. Herchen-1 at [0048]-[0050]; Pease at [0030].

C. DEPENDENT CLAIM 2: The system as described in claim 1 further comprising a power supply coupled to provide power to said wafer TI layer and controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said selective heating of said wafer TI layer is based on said PWM signals.

87. Costello and DiBattista render this claim obvious. Taken together, the references teach both elements the claim targets: (i) a power supply path that provides power to wafer-contact heating elements/thermal layer, and (ii) a controller that modulates heater power responsive to thermal feedback to achieve selective heating across independently controlled regions. Costello identifies DC resistance heaters on the chuck, a system controller and heater power source that vary heater power to achieve setpoints, and sensor feedback via resistance temperature detectors (RTDs) at the top and bottom surfaces; it also presents sensor arrays for localized temperature management and algorithms for selecting or averaging sensors. Costello at [0016], [0049], [0064], [0066]-[0067], [0070]-[0071]. DiBattista details a control chain in which a thermal control circuit computes a control signal from setpoint, sensed forcing temperature, and device power, and then drives a power amplifier stage that delivers heater current to each heating element, with multiple boards

enabling independent per-heater control for spatial selectivity. DiBattista at col. 9-12, FIGS. 6-9.

88. Given these teachings, implementing pulse-width modulation (PWM) signaling from the thermal controller to control the heater power supply for the wafer TI layer would have been an obvious design choice for a POSITA. The controller-to-power-stage interface in DiBattista already contemplates a control signal feeding a power amplifier that modulates heater current; replacing or complementing an analog/linear drive with PWM to achieve the commanded average power is a known, routine substitution within power electronics that yields predictable results - namely, regulation of average heater power while maintaining closed-loop temperature control using the existing RTD feedback path. DiBattista at col. 9, FIGS. 6-7.

89. Further, DiBattista's architecture places a computed temperature-control signal upstream of a heater power amplifier that supplies heater power to heating elements, which are arranged as independently controlled units on the chuck (DiBattista at col. 9, FIGS. 6, 8A); this control topology is naturally compatible with implementing PWM at the power stage to modulate delivered power per zone according to the controller's command. Costello expressly focuses on controlling heater current in a manner that minimizes electrical noise and describes adjusting heater power supply output smoothly to avoid rapid current changes (Costello at

[0070]-[0071]); a POSITA would recognize PWM as a selectable technique for controlling average power (via duty-cycle control) while meeting the same control objectives, particularly when combined with filtering or appropriate switching frequency selection to manage emitted noise.

90. Further, DiBattista emphasizes selective or zoned heating, which aligns with PWM's suitability to independently modulate power to multiple heater channels. DiBattista teaches arrays of heaters with independent control channels corresponding to device locations, enabling per-region temperature regulation atop a fluid-cooled heat sink. DiBattista at col. 7-8, FIGS. 8A, 10A-10B. In such multi-zone systems, PWM affords straightforward, scalable channelization: each zone's heater power can be duty-cycled under the thermal controller's loop using the already-disclosed feedback signals to achieve selective heating of the wafer TI layer.

D. DEPENDENT CLAIM 8: The system as described in claim 7 further comprising: a first blow-off valve for controlling air to release said wafer from said wafer TI layer; a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and a source of air coupled to both said first and second blow-off valves.

91. *See* discussion of DiBattista for this claim in Ground 1.

92. Costello discloses or renders obvious this claim in light of the knowledge of a POSITA. Costello at [0052-53]. It would have been obvious to a POSITA to use a positive-pressure blow-off valves or an air source for releasing the

wafer. Releasing a vacuum-secured substrate with a positive air pulse is a conventional complement to release vacuum. Costello secures the wafer on the chuck top surface by means of conventional vacuum line openings and grooves connected to a vacuum source, and likewise uses vacuum conduits to hold the chuck layers together. Costello at [0049], [0054], [0087]. Costello further provides an on-board compressed-air source and a controlled valving arrangement that selectively directs pressurized air through the chuck's conduits under system-controller control and vents it to the atmosphere. Costello at [0051]-[0052], [0055]. Given these teachings, a POSITA would have found it obvious, with a reasonable expectation of success, to release the vacuum-secured wafer by discontinuing the holding vacuum and applying a positive-pressure air pulse through the same grooves and conduits using Costello's existing air source and valving. Positive-pressure blow-off is the well-known, predictable complement to vacuum chucking and would require no change to Costello's underlying structure or operating principle.

E. DEPENDENT CLAIM 13: The system as described in claim 10 wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.

93. Costello and DiBattista render this claim obvious. DiBattista targets per-die thermal control by matching an independently controlled heater array to the wafer die layout, expressly to overcome whole-wafer chuck limitations and to handle

localized power dissipation during wafer probing (e.g., Figs. 8A, 10A-10B; discussion of individualized control).

94. Costello focuses on maintaining uniform, stable wafer-contact temperatures under load and changing conditions by independently controlling top and bottom thermal influencers and by using local sensor arrays to address hot spots.

95. A POSITA seeking improved temperature uniformity and faster, localized response for high-power or non-uniform dies would have been motivated to marry DiBattista's per-die, independently controlled heater array with Costello's layered, independently controlled thermal paths and localized sensing/control. Doing so predictably yields finer-granularity thermal management at the wafer-contact interface and layered control authority over each die location.

96. Both references operate in wafer probing contexts and integration is routine engineering: define multiple independently controllable thermal "zones" that influence each die area, leveraging known controls and sensor feedback to meet uniformity targets. Nothing in either reference suggests incompatibility.

F. DEPENDENT CLAIM 14: The system of claim 1 wherein said thermal controller is further configured to precondition a first area of said wafer to achieve a desired test temperature in advance of testing said first area, while testing and controlling a temperature of a second area of said wafer.

97. DiBattista discloses independent control of each heating element, DiBattista at 6:38-42, and testing "at high speed" with the temperature of each device "controlled independently of the other devices on the wafer during a test," DiBattista at 12:26-31, executed by a system controller 160, DiBattista at 7:59-8:2. Staged preconditioning follows from DiBattista's independent zone control and high-speed testing. Programming the controller to precondition a next zone during testing would have been obvious to ensure expediency of testing. DiBattista further teaches that multiple thermal control boards can be provided to allow simultaneous operation of a plurality of heating elements, each thermally coupled to an individual device and each having its own set of control inputs, monitoring circuit, and power amplifier, so that the several regions are driven to their respective set-point temperatures in parallel and independently. DiBattista at col. 9-10, FIGS. 6-8A. Because each region is independently and simultaneously controllable to its own set point, bringing one zone to a testing temperature while another zone is being tested is nothing more than a programmed use of DiBattista's existing parallel, per-region control. DiBattista also expressly identifies the problem that such preconditioning solves, namely the increased time to reach set point and the resulting lost utilization of expensive test equipment and personnel, which gives a POSITA a clear motivation to program the controller to bring the next zone to its testing temperature during testing of a current

zone. DiBattista at col. 1-2. A POSITA would thus have found the claimed preconditioning method obvious, with a reasonable expectation of success, yielding the predictable benefit of reduced test time and improved throughput.

XV. GROUND 3: Claims 1-25 are Rendered Obvious Over Sugiyama in View of Parkhe, Natsuhara, Criminale, and knowledge of a POSITA

98. Claims 1-25 of the '999 Patent are unpatentable under 35 U.S.C. § 103 as obvious over the below references.

A. OVERVIEW OF GROUND 3

99. Sugiyama discloses probers and probe testing methods enabling accurate, efficient temperature control of wafer-level test sites while preventing chuck tilt under probe load. Sugiyama at [0015]-[0017]. A first aspect provides a prober with a main chuck on a Z stage, X-Y positioning, a probe card above, and multiple heaters sized to individual devices or device groups, each with temperature sensors and a heat exchanger controlled by a temperature controller. Sugiyama at [0020], [0067]-[0069]. These heaters can be organized as cell structures aligned to die locations or die groups, each cell optionally including its own heater, sensor, and heat exchanger, with heat insulators between cells to reduce thermal cross-talk. Sugiyama at [0022]-[0023], [0070]-[0071].

100. Operation includes placing and fixing a wafer, aligning in X, Y, and theta, contacting probes by raising the Z stage, overdriving, and testing after bringing

the selected site to a set temperature. Sugiyama at [0039], [0072]-[0073]. A second aspect reconfigures mechanics so the X-Y stage has a central frame opening and carries a frame-structured substrate fixing mechanism with a continuous central opening. Sugiyama at [0025]-[0026], [0076]. A probing stage with an upper flat surface smaller than the frame openings is fixed on the Z stage via a probing stage elevating mechanism and is coaxial with the probe-card centerline. Sugiyama at [0026], [0080].

101. This structure prevents main chuck tilt from probe needle pressure, particularly at wafer peripheries, improving stable contact. Sugiyama at [0010], [0084]. The probing stage can incorporate a heater, temperature sensor, and heat exchanger sized to the single site or multi-site region contacted by the probes, allowing rapid, low-energy thermal control of only the tested region. Sugiyama at [0030]-[0031], [0085]-[0086]. The probing stage is preferably aluminum, detachably mounted for exchange to match site size; and its compact mass reduces thermal inertia for faster heating and cooling. Sugiyama at [0087], [0089]. Alternative embodiments position the Z stage elevating mechanism on the stage base, use one or multiple Z drives, and implement the X-Y drive with linear motors and air bearings for smooth motion. Sugiyama at [0074]-[0075]. Wafer fixing options include vacuum grooves or ports, hinged retainers, and a vertically actuated

ring with support columns; and the chuck plate can be detachable. Sugiyama at [0066], [0077]-[0079]. A method is claimed that sequences placement, X-Y-theta alignment, raising the probing stage to support the wafer, bringing probes into contact, overdriving, temperature conditioning to a target, electrical testing, and separation, repeated across sites. Sugiyama at [0039], [0082]-[0083].

102. Parkhe is directed to electrostatic chuck (ESC) assemblies usable for high-temperature semiconductor processing, addressing failures above about 120°C by providing a puck with an electrically insulative upper plate (with heating elements and electrodes) metal-bonded to a lower plate, fastener-coupled to a cooling plate with controlled force distribution and optional thermal choke features to achieve uniform heat transfer and high-temperature operation. Parkhe at [0016]-[0017], [0051]-[0053], [0072].

103. It would have been obvious to integrate Sugiyama's localized, cell-based temperature control paradigm into Parkhe's high-temperature ESC architecture by implementing multiple, spatially distributed heating/cooling control zones within or functionally coupled to the Parkhe puck/cooling-plate interface, each zone sized and positioned to correspond to regions of the substrate requiring differential thermal management (e.g., die clusters or annular/radial segments), and

governed by a controller using temperature sensor feedback. Sugiyama at [0069]-[0071]; Parkhe at [0017], [0051].

104. Further, Sugiyama teaches that heating/cooling large chuck areas is inefficient and slow, and advocates localized, cell-matched heaters/heat exchangers with sensors to reduce energy use and time to temperature. Sugiyama at [0009], [0086]. Parkhe seeks high-temperature ESC operation with uniform heat transfer and controlled thermal choke between puck and cooling plate. Parkhe at [0052]-[0053], [0072]. Combining Sugiyama's localized control with Parkhe's robust high-temperature ESC predictably improves spatial uniformity, transient response, and energy efficiency - recognized goals in wafer processing and testing.

105. It would have been obvious to substitute one known element for another. Sugiyama explicitly discloses temperature control elements comprising heaters with associated heat exchangers and sensors arranged as cells and controlled by a temperature controller. Sugiyama at [0022], [0069]-[0071]. Parkhe's ESC already integrates heaters, sensors, and cooling channels/conduits and even references multiple heating zones and thermal isolators to shape lateral profiles. Parkhe at [0028]-[0029], [0051]. Replacing or augmenting Parkhe's broader zones with Sugiyama's finer cell architecture is a straightforward substitution of known

temperature-control topologies and would be expected to yield predictable improvements.

106. Further, the teachings of the Sugiyama and Parkhe references are complementary. The integration of Sugiyama with Parkhe would also be obvious to try with a reasonable expectation of success. The addition of localized zone temperature control, as taught by Sugiyama, would assist in temperature control for the broader zones according to the teaching of Parkhe. Sugiyama at [0022]-[0023], [0070]-[0071], [0086]; Parkhe at [0028]-[0029].

107. A POSITA would have had a reasonable expectation of success in combining Sugiyama with Parkhe because both references already build their thermal control from the same, interchangeable set of components - resistive heaters, temperature sensors, fluid-based heat exchange, and a controller - and Sugiyama's finer, cell-based control is a known substitute for Parkhe's coarser zoning rather than a new mechanism. Sugiyama discloses cell structures in which a heater, temperature sensor, and heat exchanger can be arranged in each cell, separately controlled by a temperature controller on the basis of the detection results of the temperature sensors, with heat insulators partitioning the cells to reduce thermal cross-talk. Sugiyama at [0067]-[0071]. Parkhe's architecture already contains the same building blocks: embedded heating elements regulated by a heater power source, fluid

conduits for cooling, embedded thermal isolators to control a lateral temperature profile, and two separate heating zones or four different heating zones that can maintain distinct temperatures, monitored by multiple temperature sensors through a controller. Parkhe at [0028]-[0029]. Refining Parkhe's two- or four-zone puck into the finer, cell-matched zones taught by Sugiyama is therefore a substitution of one known temperature-control topology for another within an architecture already designed for independent, sensor-fed zone control. Sugiyama confirms the result is predictable and advantageous, teaching that confining heating to the tested region shortens the time required for increasing the temperature of the object to be tested and reduces energy consumption and loss. Sugiyama at [0086]. A POSITA would have expected the combined system to deliver finer-grained, more responsive thermal control without disturbing Parkhe's high-temperature operation, and thus would have had a reasonable expectation of success.

B. INDEPENDENT CLAIM 1

108. Sugiyama in view of Parkhe render obvious every limitation of claim 1, as set forth element-by-element below.

1. [1.g]: a pin lift mechanism for displacing pins for lifting said wafer away from said wafer TI layer and wherein said cold plate and said wafer TI layer both comprise vertical alignment holes which are aligned with said pins for allowing said pins to pass through said cold plate and said wafer TI layer to lift said wafer.

109. It would have been obvious to supplement Sugiyama's disclosure with Parkhe for the reasons stated above. Parkhe at [0033], [0051], [0078]. It would further have been obvious to a POSITA to use loading pins, as such were known and common method to load and unload wafers being tested, as noted above. Sugiyama at [0077]-[0078], [0080]-[0081], *see* discussion in Ground 1 regarding lift pins.

C. DEPENDENT CLAIM 2: The system as described in claim 1 further comprising a power supply coupled to provide power to said wafer TI layer and controlled by said thermal controller via pulse-width modulation (PWM) signals, wherein said selective heating of said wafer TI layer is based on said PWM signals.

110. This claim is obvious. *See* Sugiyama at [0066-70], [0085], [0090]. Both Sugiyama and Parkhe require independently maintaining distinct temperatures per zone using a controller that responds to multiple temperature sensors, which calls for per-zone modulation of heater power. Implementing the controller's outputs as PWM duty-cycle signals to a power stage per zone is a routine approach to achieve precise, decoupled average power in resistive heaters, yielding predictable success in holding setpoints. Both references' closed-loop, multi-zone resistive-heater architectures necessarily require adjustable heater power per zone, with which PWM is a standard, predictable technique to realize per-zone average power control with fine granularity, efficiency, and compatibility with digital controllers.

D. DEPENDENT CLAIM 4: The system as described in claim 2 wherein: said wafer TI layer comprises a plurality of traces

traversing said wafer TI layer and operable to selectively heat a plurality of zones of said wafer TI layer responsive to said PWM signals; and said wafer TI layer further comprises a grounded shield layer disposed on a top surface of said wafer TI layer, said grounded shield layer operable for protecting said wafer from EMI radiation resultant from said PWM signals applied to said plurality of traces.

111. Sugiyama in light of a knowledge of a POSITA renders this claim obvious. Adding a grounded shield layer would have been obvious due to known need to shield electrical components from electrical radiation. As in Ground 1, Natsuhara supports this, teaching a grounded electrically conductive layer over the resistance heat generator in a wafer prober that blocks electromagnetic waves interfering with the measurement of very low currents. Natsuhara at [0012], [0024].

E. DEPENDENT CLAIM 8: The system as described in claim 7 further comprising: a first blow-off valve for controlling air to release said wafer from said wafer TI layer; a second blow-off valve for controlling air to release said wafer TI layer from said cold plate; and a source of air coupled to both said first and second blow-off valves.

112. This claim is rendered obvious given Sugiyama's disclosure of a vacuum. *See* Sugiyama at Figs. 3, 10, 12, [0066], [0077]. It would have been obvious to a POSITA to release the vacuum-secured wafer and TI layer using a positive-pressure blow-off valve and air source. Releasing a vacuum-secured substrate with a positive air pulse is a conventional complement to vacuum securing, and applying that known technique to Sugiyama's vacuum-secured chuck yields the predictable

result of controlled wafer release. Costello similarly discloses vacuum securing of the wafer that is relieved during load and unload, confirming that using controlled air and vacuum to release the wafer was conventional. Costello at [0052]-[0053].

F. DEPENDENT CLAIM 11: The system as described in claim 10 wherein each zone of said plurality of zones corresponds to a respective single die of said die layout of said wafer.

113. Sugiyama in light of knowledge of a POSITA discloses or renders obvious this element. Sugiyama at [0022-23], [0067-68], [0071-72], [0080], [0091-92], claims 2-3.

114. Sugiyama teaches partitioning temperature-control functionality on the chuck into multiple independently controllable "cells" or zones whose sizes are selected to match either a single object-under-test (i.e., a single die on the wafer) or a small group of such objects, and to control each such cell based on local sensing. Sugiyama at [0067-68]. Because Sugiyama discloses (i) heaters sized to one object or a group, (ii) per-cell temperature sensors and heat exchange, (iii) heat-insulating partitions between cells, and (iv) the benefits of minimizing heated area to reduce thermal lag/energy while improving accuracy, a POSITA would be motivated to select the finest practical granularity - one die per zone - when die-level electrical probing is performed, thereby making each zone correspond to a respective single die layout position. Since electrical probe testing is conducted at the die (object)

level with a defined probe footprint, and Sugiyama provides cells/heaters "corresponding to" individual objects and sized to that region, a POSITA would configure each zone to the die footprint so that each probed die is temperature-controlled independently during its testing.

G. DEPENDENT CLAIM 12: The system as described in claim 10 wherein each zone of said plurality of zones corresponds to a respective plurality of dice of said die layout of said wafer.

115. Sugiyama in light of knowledge of a POSITA discloses or renders obvious this element. Sugiyama at [0022-23], [0071], [0080], [0091-92], claims 2-3. Further, it would be obvious to try, based on the desire to increase testing throughput, to adjust the heating zones to cover a plurality of dice.

H. DEPENDENT CLAIM 13: The system as described in claim 10 wherein each die of said die layout of said wafer corresponds to multiple respective zones of said plurality of zones of said wafer TI layer.

116. Sugiyama in light of knowledge of a POSITA discloses or renders obvious this element. Sugiyama at [0022-23], [0069], [0067-71], [0080], [0091-92], claims 2-3. Further, it would be obvious to try, based on the desire for more granular testing ability, to adjust the heating zones such that multiple zones covered a single die.

I. DEPENDENT CLAIM 14: The system of claim 1 wherein said thermal controller is further configured to precondition a first area of said wafer to achieve a desired test temperature in advance of testing said first area, while testing and controlling a temperature

of a second area of said wafer.

117. Sugiyama discloses independent control of each heating element, Sugiyama at [0020-22]. As noted above, Sugiyama discloses a controller for controlling independent heating elements. Staged preconditioning follows from Sugiyama's independent zone control and wafer testing system based on knowledge of a POSITA. Sugiyama at [0062-67]. Programming the controller to precondition a next zone during testing would have been obvious to ensure expediency of testing. Pease reinforces this, disclosing independently controllable heater zones that actively create and maintain a desired spatial and temporal temperature profile, which enables a next zone to be brought to temperature during testing. Pease at [0014], [0030].

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Dated: October 4, 2026

By: */s/Joseph C. McAlexander III*

Joseph C. McAlexander III, P.E.