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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/172,644	02/04/2014	Michael Miskin	LYN-091109CO01	7455

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EXAMINER
HAMMOND, CRYSTAL L

ART UNIT	PAPER NUMBER
2844	

NOTIFICATION DATE	DELIVERY MODE
10/08/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 14/172,644	Applicant(s) MISKIN ET AL.	
	Examiner CRYSTAL L. HAMMOND	Art Unit 2844	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02/04/2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-28 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-28 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 02/04/2014 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☒ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____. | 4) ☐ Other: ____. |

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-28 are rejected under pre-AIA 35 U.S.C. 102(a) as being anticipated by Miskin et al. (US 2007/0273299).

Figure 15 of Miskin discloses an LED lighting device comprising:

(1) regarding Claim 1:

at least two LED circuits (26 in Fig 15), each LED circuit having opposing ends and at least two LEDs (ends in Fig 15); at least four voltage input electrical contacts (4 contacts are coupled to LEDs in Fig 15), the at least four voltage input electrical contacts being configured so that each opposing end of each of the at least two circuits has one voltage input electrical contact connected thereto, wherein, each of the at least two LED circuits are electrically unconnected from each other (See Fig 15 and [0082]-each LED set is unconnected from the other sets and Fig 16).

(2) regarding Claim 2:

wherein each of the at least two LED circuits include at least two LEDs connected in series (Fig 16 and [0018]-parallel series strings).

(3) regarding Claim 3:

wherein each of the at least two LED circuits are arranged in a bridge circuit having at least one LED connected across the outputs (Diode bridge 230 in Fig 21).

(4) regarding Claim 4:

wherein the at least two LEDs in each of the at least two LED circuits are connected in an anti-parallel manner ([abstract text]).

(5) regarding Claim 5:

wherein the at least four voltage input electrical contacts are configured such that a first voltage input electrical contact is connected to an anode of one LED in a first of the at least two LED circuits; and a cathode of one LED in the first of the at least two LED circuits; a second voltage input electrical contact is connected to an anode of one LED in the first of the at least two LED circuits; and a cathode of one LED in the first of the at least two LED circuits; a third voltage input electrical contact is connected to an anode of one LED in a second of the at least two LED circuits; and a cathode of one LED in the second of the at least two LED circuits; a fourth voltage input electrical contact is connected to an anode of one LED in the second of the at least two LED circuits; and a cathode of one LED in the second of the at least two LED circuits, wherein the first voltage input electrical contact is connected to a different anode and a different

cathode than the second voltage input electrical contact, and the third voltage input electrical contact is connected to a different anode and a different cathode than the fourth voltage input electrical contact (See Fig 16 #178, 180 and 182 are different representations of LED and electrical contact connections).

(6) regarding Claim 6:

wherein the at least two circuits may be connected in a series relationship by connecting the first voltage input electrical contact to a first output of a power supply, connecting the third voltage input electrical contact to a second output of a power supply, and connecting the second voltage input electrical contact and the fourth voltage input electrical contact to each other; or a parallel relationship by connecting the first voltage input electrical contact and the third voltage input electrical contact to a first output of a power supply, and and the second voltage input electrical contact and the fourth voltage input electrical contact to a second output of a power supply (See Fig 16 [0083]).

(7) regarding Claim 7:

wherein the LED lighting device is an LED package (See Fig 16).

(8) regarding Claim 8:

wherein the at least two LED circuits are connected in series or parallel utilizing the at least four voltage electrical input contacts within the LED package (See Fig 16-[0011]).

(9) regarding Claim 9:

wherein the at least two LED circuits are integrated on a single chip ([0011]).

(10) regarding Claim 10:

wherein the at least two LED circuits are integrated on discrete chips so that each of the at least two LED circuits is on a separate chip ([0011]).

(11) regarding Claim 11:

wherein the at least two LEDs forming each of the at least two LED circuits are discrete die integrated on a substrate ([0011]).

(12) regarding Claim 12:

wherein the LED lighting device is an LED assembly of discretely packaged LEDs ([0011]).

(13) regarding Claim 13:

at least two LED circuits (178 in Fig 16); at least three voltage input electrical contacts, wherein a first voltage input electrical contact connected to both of the at least two LED circuits, a second voltage input electrical contact is connected to a first of the at least two LED circuits, and a third voltage input electrical contact is connected to a second of the at least two circuits (See electrical contacts coupled to ends of 178 in Fig 16).

(14) regarding Claim 14:

wherein each of the at least two LED circuits include plurality of LEDs and the at least three voltage input electrical contacts are arranged such that the first voltage input electrical contact is connected to a cathode of one of the plurality of

LEDs in both of the at least two LED circuits; the second voltage input electrical contact is connected to an anode of one of the plurality of LEDs in the first of the at least two LED circuits; the third voltage input electrical contact is connected to an anode of one of the plurality of LEDs in the second of the at least two LED circuits (See Fig 16).

(15) regarding Claim 15:

wherein at least a portion of the plurality of LEDs in each of the at least two LED circuits are connected in series (See 180 in Fig 16).

(16) regarding Claim 16:

wherein at least a portion of the plurality of LEDs in each of the at least two LED circuits are connected in an anti-parallel configuration ([abstract text]).

(17) regarding Claim 17:

wherein each of the at least two LED circuits includes a first portion of the plurality of LEDs connected in a first series string of LEDs, a second portion of the plurality of LEDs connected in a second series string of LEDs, the first portion of the plurality of LEDs and the second portion of LEDs connecting at a first branch junction and a second branch junction in an anti-parallel manner ([abstract text] and Fig 16).

(18) regarding Claim 18:

wherein the first voltage input electrical contact connects to the first branch junction of both of the at least two LED circuits; the second voltage input electrical contact connects to the second branch junction of the first of the at

least two LED circuits; and the third voltage input electrical contact connects to the second branch junction of the second of the at least two LED circuits (See Fig 16 and [0083]).

(19) regarding Claim 19:

wherein each of the at least two LED circuits include a bridge rectifier; and at least one LED connected across the output of the bridge rectifier (See Fig 21).

(20) regarding Claim 20:

wherein the at least three voltage input electrical contacts are arranged such that the first voltage input electrical contact is connected to a first input of a bridge rectifier in both of the at least two LED circuits; the second voltage input electrical contact is connected to a second input of the bridge rectifier in the first of the at least two LED circuits; and the third voltage input electrical contact is connected to a second input of the bridge rectifier in the second of the at least two LED circuits (See Fig 21).

(21) regarding Claim 21:

wherein the LED lighting device is an LED package (See Fig 16).

(22) regarding Claim 22:

wherein the at least two LED circuits are integrated on a single chip ([0011]).

(23) regarding Claim 23:

wherein the at least two LED circuits are integrated on discrete chips so that each of the at least two LED circuits is on a separate chip ([0011]).

(24) regarding Claim 24:

wherein the at least two LEDs forming each of the at least two LED circuits are discrete die integrated on a substrate ([0011]).

(25) regarding Claim 25:

wherein the LED lighting device is an LED assembly of discretely packaged LEDs ([0011]).

(26) regarding Claim 26:

at least two LED circuits (178 in Fig 16), each LED circuit having at least two LEDs, the at least two LEDs in each circuit being connected in an anti-parallel configuration ([abstract text]); at least four voltage input electrical contacts, the at least four voltage input electrical contacts being configured so that one voltage input electrical contact is electrically connected to each opposing end of each of the at least two LED circuits, wherein, each of the at least two LED circuits are electrically unconnected from each other (See Fig 16).

(27) regarding Claim 27:

at least two LED circuits (178 in Fig 16), each LED circuit having at least two LEDs, the at least two LED circuits each having opposing ends, and the at least two LEDs in each circuit being connected in an anti-parallel configuration ([abstract text]); at least four voltage input electrical contacts, the at least four voltage input electrical contacts being configured so that each opposing end of each of the at least two LED circuits has one voltage input electrical contact

electrically connected thereto, wherein, each of the at least two LED circuits are electrically unconnected from each other (See Fig 16).

(28) regarding Claim 28:

wherein each of the at least two LED circuits are formed on discrete chips ([0011]), the discrete chips each containing at least two voltage input electrical contacts, the at least two voltage input electrical contacts being configured so that each opposing ends of each LED circuit have one voltage input electrical contact on each chip electrically connected to each opposing end, and the at least two voltage input electrical contacts for each discrete chip are electrically connected to one of the at least four voltage input electrical contacts in the LED package (See Fig 16).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CRYSTAL L. HAMMOND whose telephone number is (571)270-1682. The examiner can normally be reached on Monday Thru Friday 7:30 AM-5:00 PM Alt Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Taningco can be reached on (571) 272-8048. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CRYSTAL L HAMMOND/
Primary Examiner, Art Unit 2844