QSFP-DD MSA

QSFP-DD Hardware Specification

for

QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER

Rev 3.0 September 19, 2017

Abstract: This specification defines: the electrical and optical connectors, electrical signals and power supplies, mechanical and thermal requirements of the pluggable QSFP Double Density (QSFP-DD) module, connector and cage system. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

POINTS OF CONTACT:

Tom Palkert	Mark Nowell	Scott Sommers
Technical Editor	Co-Chair	Co-Chair
Molex	Cisco	Molex
2222 Wellington Court	170 West Tasman Dr	2222 Wellington Court
Lisle, IL 60532-1682	San Jose, CA 95134	Lisle, IL 60532-1682
Ph: 952-200-8542	Ph: 613-254-3391	Ph: 630-527-4317
tom.palkert at molex.com	mnowell at cisco.com	scott.sommers at molex.com

www.qsfp-dd.com

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Foreword

The development work on this specification was done by the QSFP-DD MSA, an industry group. The membership of the committee since its formation in Feb 2016 has included a mix of companies which are leaders across the industry.

TABLE OF CONTENTS

1 Scope 7
1.1 Description of Sections *7*
2 References 7
2.1 Industry Documents *7*
2.2 Sources *8*
3 Introduction 8
3.1 Objectives *8*
3.2 Applications *9*
4 Electrical Specification 9
4.1 Electrical Connector *9*
4.1.1 Low Speed Electrical Hardware Signals 16
4.1.2 Low Speed Electrical Specification 17
4.1.3 Timing for soft control and status functions 18
4.1.4 High Speed Electrical Specification 20
4.2 Power Requirements *21*
4.2.1 Power Classes and Maximum Power Consumption 22
4.2.2 Host Board Power Supply Filtering 22
4.2.3 Module Power Supply Specification 23
4.2.4 Host Board Power Supply Noise Output 23
4.2.5 Module Power Supply Noise Output 24
4.2.6 Module Power Supply Noise Tolerance 24

4.3 ESD *26*

5 Mechanical and Board Definition 27

5.1 Introduction *27*

5.2 Datums, Dimensions and Component Alignment *28*

5.3 Module Mechanical Dimensions *31*

5.4 Module Flatness and Roughness *37*

5.5 Module paddle card dimensions *38*

5.6 Module Extraction and Retention Forces *41*

5.7 2x1 Electrical Connector Mechanical *42*

5.7.1 2x1 Connector and Cage host PCB layout 47

5.8 Surface Mount Electrical Connector Mechanical *50*

5.8.1 Surface mount connector and cage host PCB layout 56

5.9 Module Color Coding and Labeling *58*

5.10 Optical Interface *59*

5.10.1 MPO Optical Cable connections 60

5.10.2 Dual LC Optical Cable connection 62

5.10.3 Dual CS Optical Cable connection 62

5.10.4 Electrical data input/output to optical port mapping 63

6 Environmental and Thermal 63

6.1 Thermal Requirements *63*

6.1.1 External Case and Handle Touch Temperature 63

7 Management Interface 64

7.1 SCL, SDA and ModSEL Timing Specification *64*

7.1.1 Introduction 64

7.1.2 Management Interface Timing Specification 64

7.1.3 Serial Interface Protocol 65

Appendix A: Informative overall module length with elastomeric handle attached to module latches *68*

Table 1- Pad Function Definition..... 12
Table 2- Low Speed Control and Sense Signals..... 18
Table 3- Timing for QSFP-DD soft control and status functions..... 19
Table 4- I/O Timing for Squelch & Disable..... 20
Table 5- Power Classes..... 22
Table 6- Power Supply specifications, Instantaneous, sustained and steady state current limits..... 25
Table 7- Datums..... 29
Table 8- Module flatness specifications..... 37
Table 9- Insertion, Extraction and Retention Forces..... 41
Table 10- Electrical data input to Optical Port Mapping..... 63
Table 11- Temperature Range Class of operation..... 63
Table 12- Management Interface timing parameters..... 66

Figure 1: Application Reference Model..... 9
Figure 2: Module pad layout..... 11
Figure 3: Example QSFP-DD Host Board Schematic For Optical Modules..... 14
Figure 4: Example QSFP-DD Host Board Schematic for active copper cables..... 15
Figure 5: Example QSFP-DD Host Board Schematic for passive copper cables..... 16
Figure 6: Recommended Host Board Power Supply Filtering..... 22
Figure 7: Instantaneous and sustained peak currents for Icc Host (see Fig. 6)..... 23
Figure 8: 2x1 stacked cage and module..... 27
Figure 9: Press fit cage for surface mount (SMT) connector..... 27
Figure 10: Type 1 Pluggable module..... 28
Figure 11: Type 2 Pluggable module..... 28
Figure 12: 2X1 stacked connector/cage datum descriptions..... 30
Figure 13: Surface mount connector/cage datum descriptions..... 31
Figure 14: Type 1 Module..... 32
Figure 15: Type 2 Module..... 32
Figure 16: Drawing of module..... 34
Figure 17: Detailed dimension of module..... 36
Figure 18: Module paddle card dimensions..... 39
Figure 19: Module pad dimensions..... 40
Figure 20: Integrated connector in 2x1 stacked cage..... 42
Figure 21: 2x1 stacked cage..... 43
Figure 22: 2x1 stacked cage dimensions..... 44
Figure 23: Connector pins in 2x1 stacked cage as viewed from the front..... 45
Figure 24: 2x1 Bezel Opening..... 46
Figure 25: 2X1 host board connector contacts..... 47
Figure 26: 2X1 Host PCB Mechanical Layout..... 49
Figure 27: SMT connector in 1xn cage..... 50
Figure 28: SMT 1x1 Cage Design..... 52
Figure 29: SMT 1x1 Connector Design..... 54
Figure 30: SMT 1xn bezel opening..... 55
Figure 31: SMT Host PCB Mechanical Layout..... 56
Figure 32: SMT Connector and Host PCB Pin Numbers..... 57
Figure 33: Optical Media Dependent Interface port assignments..... 59
Figure 34: MPO-12 Single Row optical patch cord and module receptacle..... 60
Figure 35: MPO-16 Single Row optical patchcord and module receptacle..... 61
Figure 36: MPO-12 Two Row optical patchcord and module receptacle..... 61
Figure 37: Dual LC optical patchcord and module receptacle..... 62
Figure 38: Dual CS connector module receptacle (in support of breakout applications)... 62
Figure 39: QSFP-DD Timing Diagram..... 64
Figure 40: SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times... 67
Figure 41: Informative overall module length with handle for Type 1 module..... 68
Figure 42: Informative overall module length with handle for Type 2 module..... 68

QSFP-DD 8X Pluggable Transceiver

1 Scope

The scope of this specification is the definition of a high density 8-channel (8x) module, cage and connector system. QSFP-DD supports up to 400 Gb/s in aggregate over an 8 x 50 Gb/s electrical interface. The cage and connector design provides backwards compatibility to QSFP28 modules which can be inserted into a QSFP-DD port and connected to 4 of the 8 electrical channels.

1.1 Description of Sections

Section 1 Scope and Purpose

Section 2 Referenced and Related Standards and SFF Specifications

Section 3 Introduction

Section 4 Electrical specifications

Section 5 Mechanical specifications and printed circuit board recommendations

Section 6 Environmental and thermal considerations

Section 7 Management Interface

2 References

2.1 Industry Documents

The following interface standards and specifications are relevant to this Specification:

- GR-253-CORE
- IEEE Std 802.3
- IEEE Std 802.3by
- IEEE Std 802.3bs
- IEEE Std 802.3cd
- InfiniBand Architecture Specifications
- FC-PI-6p
- FC-PI-7
- ANSI/TIA-568.3
- TIA-604-5 (FOCIS 5)
- TIA-604-10 (FOCIS 10)
- TIA-604-18 (FOCIS 18)
- IEC 61754-7-1
- ANSI/ESDA/JDEC JS001
- EN6100-4-2
- QSFP-DD Management Interface Specification
- GR63 Section 4.1.7 (Touch Temperature Reference)
- UL 60950-1 Section 4.5.4 (Touch Temperature Reference)
- IEC 31300-3-35

SFF Specifications

- INF-8436 QSFP (Quad SFP) 4 Gbps 4X Transceiver
- SFF-8636 Shielded Cables Common Management Interface
- SFF-8472 Diagnostic Monitoring Interface for Optical Transceivers
- SFF-8661 QSFP+ 4X Pluggable Module
- SFF-8679 QSFP28 4X Base Electrical Specification

CS optical connector specification

- CS-01242017 Revision 1.0 (Can be found at www.QSFP-DD.com)

2.2 Sources

This document can be obtained via the www.QSFP-DD.com web site.

3 Introduction

This Specification covers the following items:

a) Electrical interfaces including pad assignments for data, control, status and power supplies and host PCB layout requirements.

b) Optical interfaces (including optical receptacles and mating fiber plugs for multimode and single-mode duplex and parallel fiber applications). Breakout cable applications are also specified. Optical signaling specifications are not included in this document but are defined in the applicable industry standards.

c) Mechanical specifications including dimensions and tolerances for the connector, cage and module system. Includes details of the requirements for correct mating of the module and host sides of the connector.

d) Thermal requirements

e) Electrostatic discharge (ESD) requirements by reference to industry standard limits and test methods.

This Specification does not cover the following items:

a) Electromagnetic interference (EMI) protection. EMI protection is the responsibility of the implementers of the cages and modules.

b) Memory map definition which can be found in the QSFP-DD Memory Map Specification.

3.1 Objectives

Electrical signal contact and channel assignments, electrical and power requirements defined in Section 4 and optical lane assignments defined in Section 5 ensure that the pluggable modules and cable assemblies are functionally interchangeable. Dimensions, mounting and insertion requirements defined in Section 5 for the bezel, optical module, cable plug, cage and connector system on a circuit board ensure that these products are mechanically interchangeable.

3.2 Applications

This specification defines a common solution for combined eight-channel ports that support Ethernet and/or InfiniBand and/or Fibre Channel requirements. The QSFP-DD interface can support pluggable modules or direct attach cables based on multimode fiber, single mode fiber or copper wires.
An application reference Model, shown in Figure 1, shows the high-speed data interface between an ASIC and the QSFP-DD module.

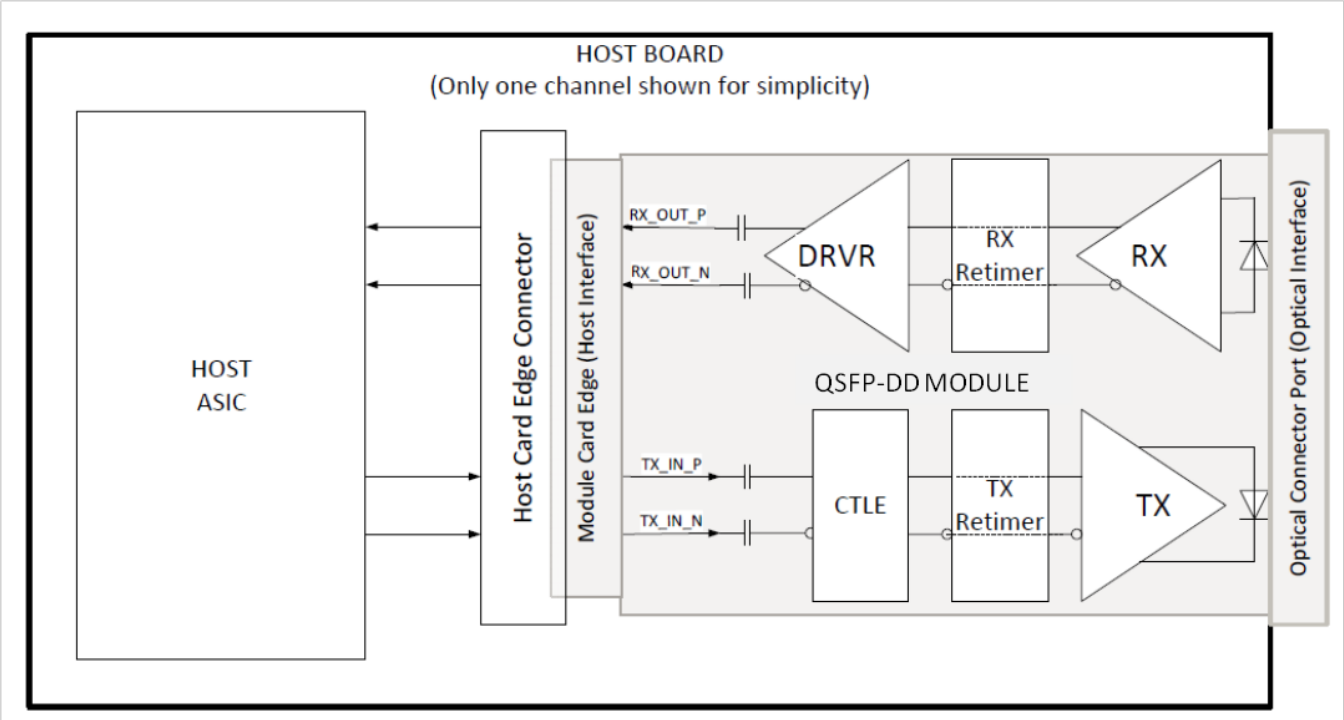


Figure 1: Application Reference Model

Note: For high speed electrical signals the compliance board methodology of IEEE and OIF should be used. Measurements taken with QSFP-DD compliance boards should be corrected for any difference between the loss of these compliance boards and the loss of the compliance boards specified in the standard.

4 Electrical Specification

This section contains signal definitions and requirements that are specific to the QSFP-DD module. High-speed signal requirements including compliance points for electrical measurements are defined in the applicable industry standard.

4.1 Electrical Connector

The QSFP-DD module edge connector consists of a single paddle card with 38 pads on the top and 38 pads on the bottom of the paddle card for a total of 76 pads. The pads are defined in such a manner so as to accommodate insertion of a QSFP module into a QSFP-DD receptacle. The legacy signal locations are deeper on the paddlecard, so that legacy QSFP module pads only connect to the longer row of connector pins, leaving the short row of connector pins unconnected in a QSFP application.

The pads are designed for a sequenced mating:

First mate – ground pads
Second mate – power pads
Third mate – signal pads

Because the QSFP-DD module has 2 rows of pads, the additional QSFP-DD pads will have an intermittent connection with the legacy QSFP pins in the connector during the module insertion and removal. The 'legacy' QSFP pads have a 'B' label shown in Table 1 to designate them as the second row of module pads to contact the QSFP-DD connector. The additional QSFP-DD pads have an 'A' label in Table 1 to designate them as the first row of module pads to contact the QSFP-DD connector. The additional QSFP-DD pads have first, second and third mate to the connector pins for both insertion and removal. Each of the first, second and third mate connections of the legacy QSFP pads and the respective additional QSFP-DD pads are simultaneous.

Figure 2 shows the signal symbols and pad numbering for the QSFP-DD module edge connector. The diagram shows the module PCB edge as a top and bottom view. There are 76 pads intended for high speed signals, low speed signals, power and ground connections. Table 1 provides more information about each of the 76 pads. Figure 18 and Figure 19 show pad dimensions . The connector can be integrated into a 2x1 stacked configuration with 2 ports as illustrated in Figure 8 or a surface mount configuration as shown in Figure 9.

For EMI protection the signals from the host connector should be shut off when the QSFP-DD module is not present. Standard board layout practices such as connections to Vcc and GND with vias, use of short and equal-length differential signal lines are recommended. The chassis ground (case common) of the QSFP-DD module should be isolated from the module’s circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

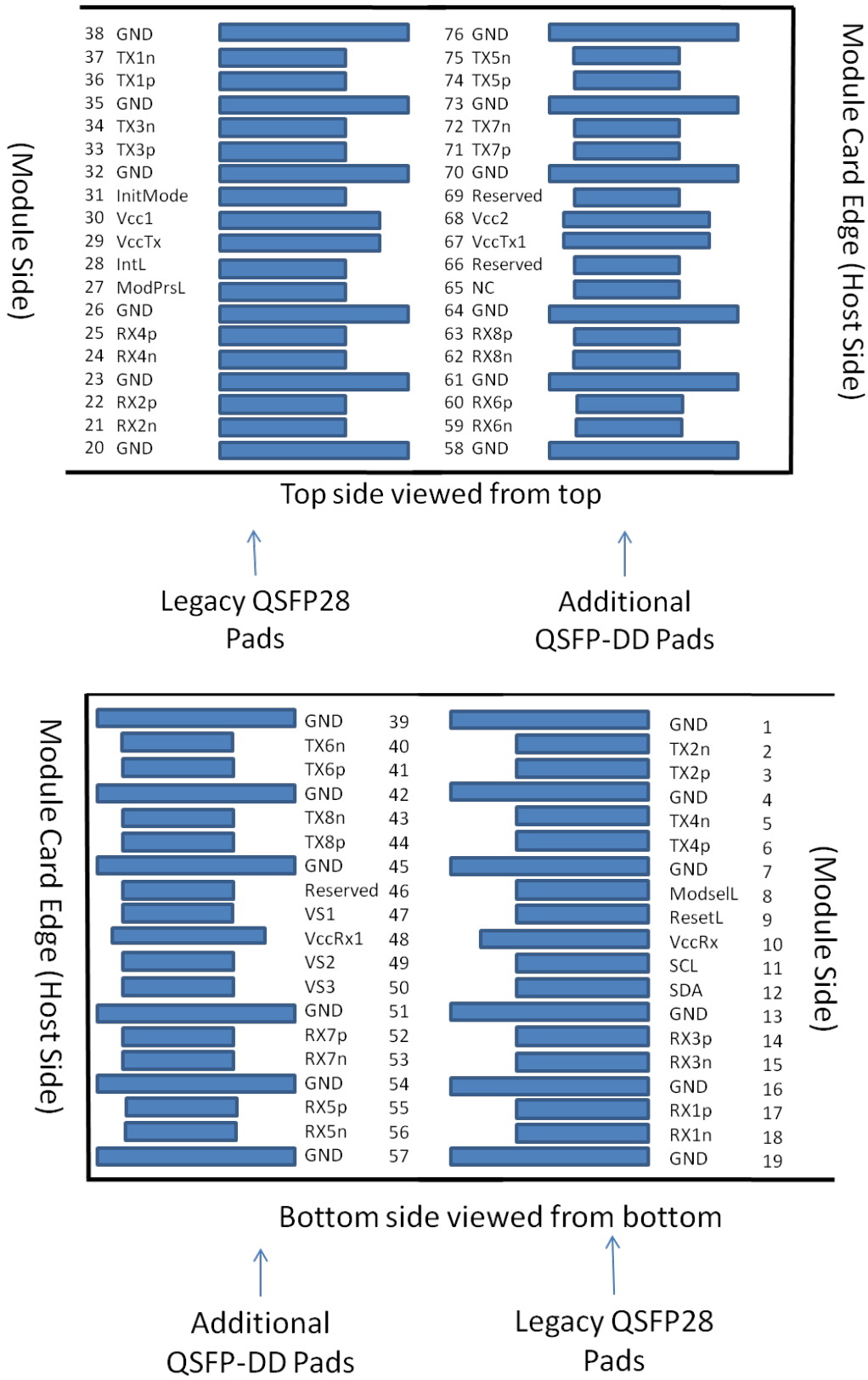


Figure 2: Module pad layout

Table 1- Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Figure 3, Figure 4 and Figure 5 show examples of QSFP-DD host PCB schematics with connections to CDR and control ICs. An 8 wide electrical/optical interface is shown. Note alternate electrical/optical interfaces are supported using optical multiplexing (WDM) or electrical multiplexing.

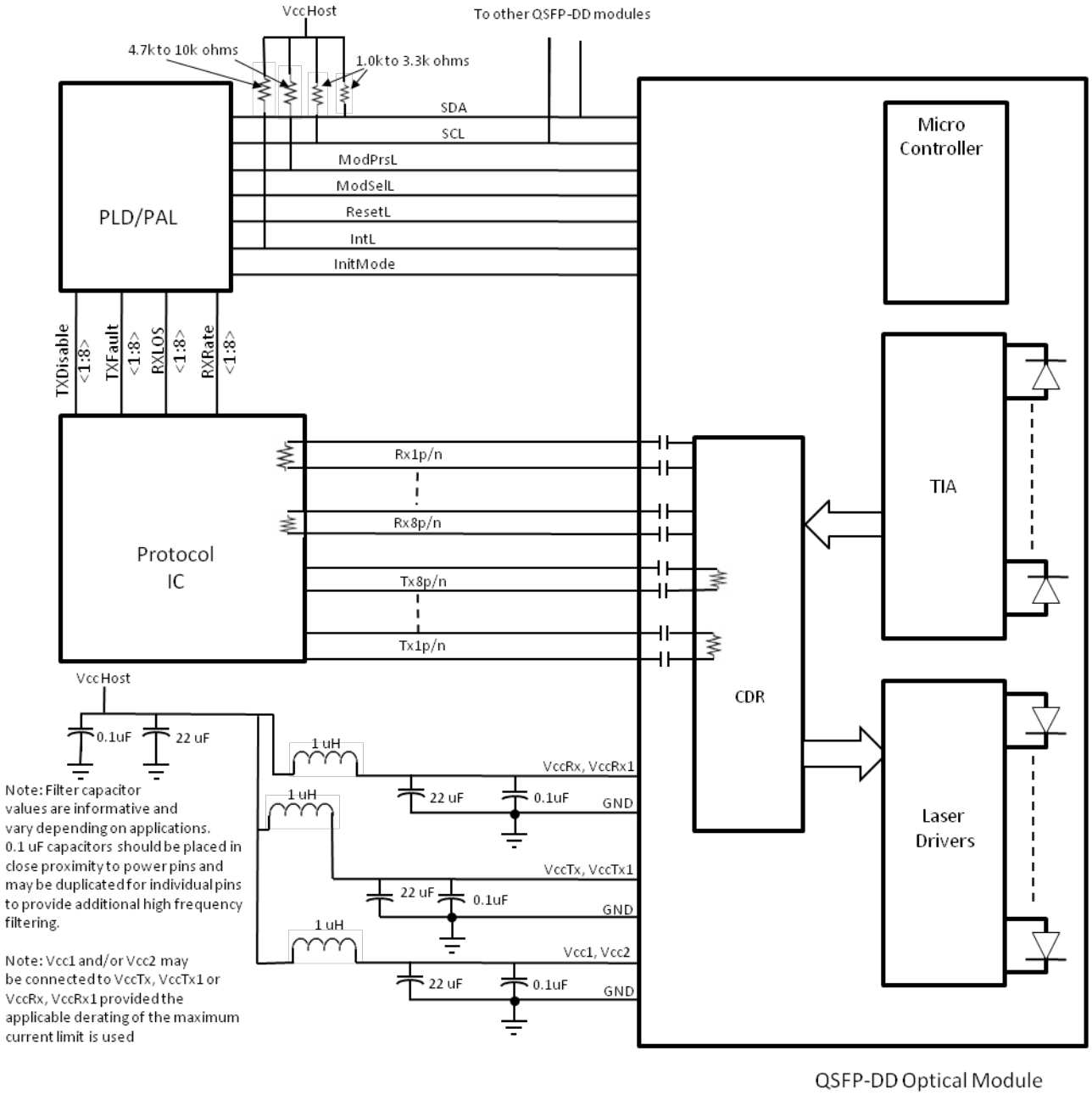


Figure 3: Example QSFP-DD Host Board Schematic For Optical Modules

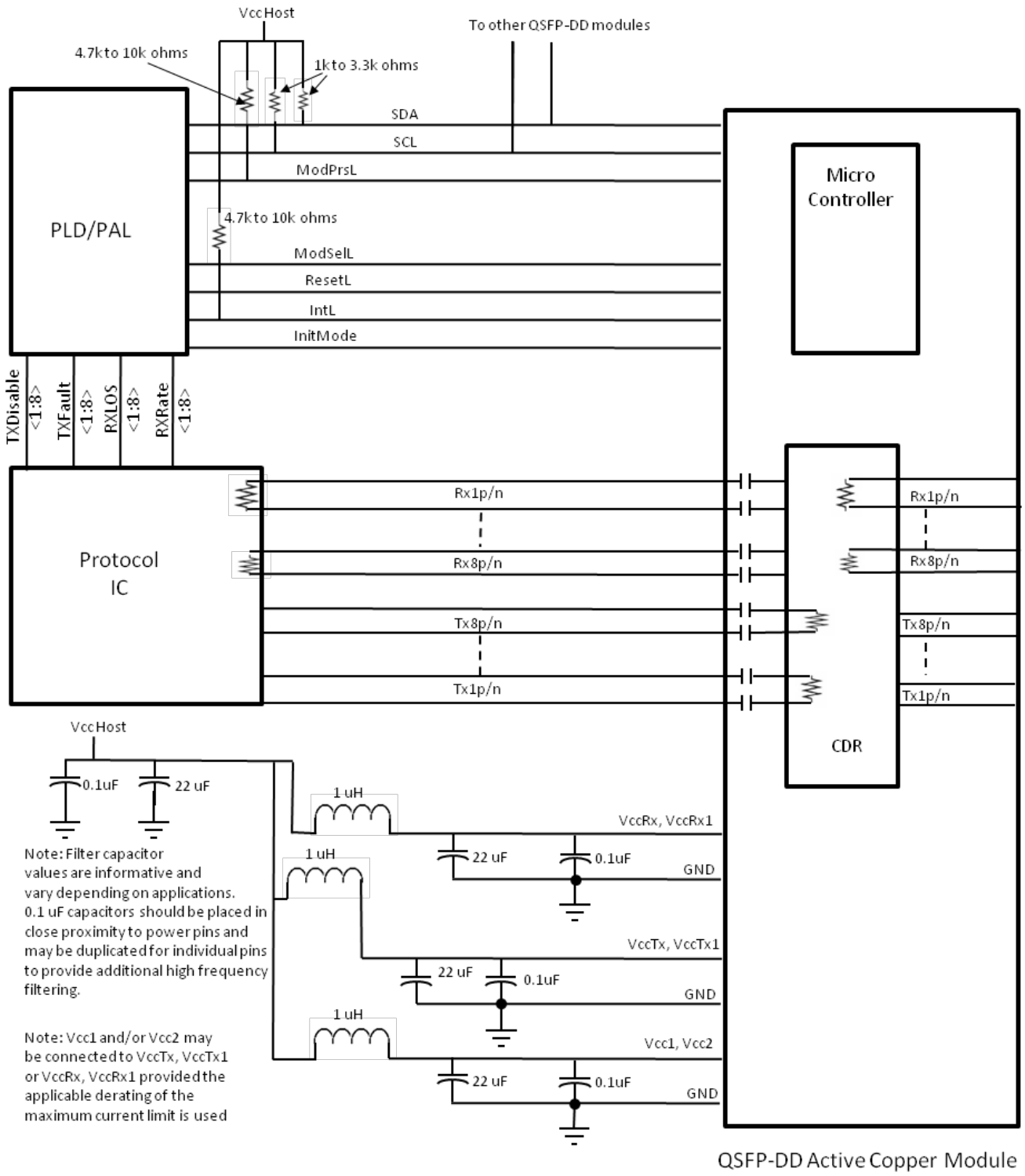


Figure 4: Example QSFP-DD Host Board Schematic for active copper cables

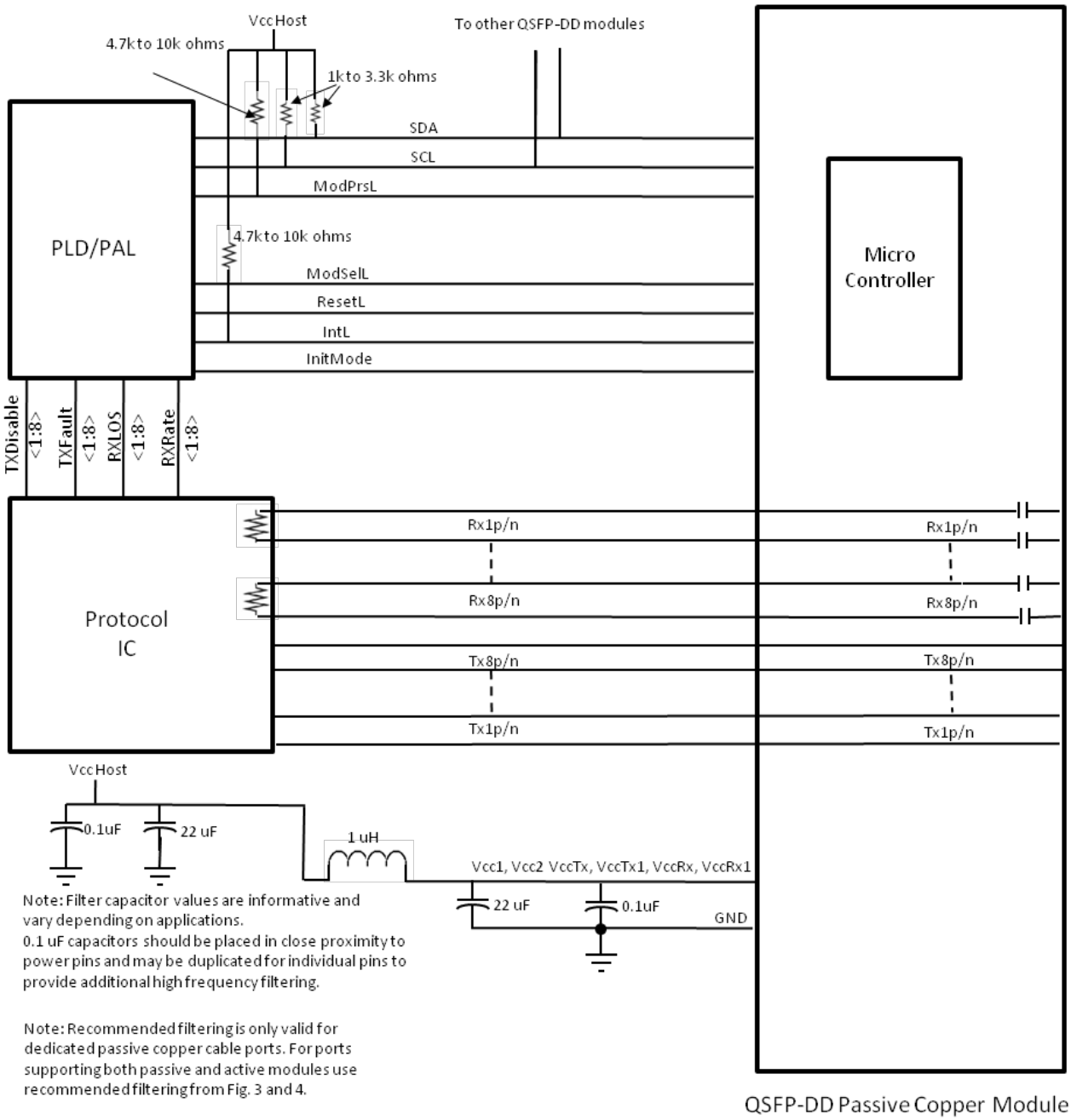


Figure 5: Example QSFP-DD Host Board Schematic for passive copper cables

4.1.1 Low Speed Electrical Hardware Signals

In addition to the 2-wire serial interface the module has the following low speed signals for control and status:

ModSelL
ResetL
InitMode
ModPrsL
IntL

4.1.1.1 ModSelL

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DD module (see Table 2). When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

4.1.1.2 ResetL

The ResetL signal shall be pulled to Vcc in the module (see Table 2). A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 3) initiates a complete module reset, returning all user module settings to their default state.

4.1.1.3 InitMode

InitMode is an input signal. The InitMode signal must be pulled up to Vcc in the QSFP-DD module (see Table 2). The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in the QSFP-DD Management Interface Specification. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for LPMode signal description.

4.1.1.4 ModPrsL

ModPrsL must be pulled up to Vcc Host on the host board and pulled low in the module (see Table 2). The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull up resistor on the host board.

4.1.1.5 IntL

IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board (see Table 2). When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

4.1.2 Low Speed Electrical Specification

Low speed signaling other than the SCL and SDA interface is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs (see Table 2). The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

Note: Timing diagrams for SCL and SDA are shown in Section 7.

The QSFP-DD low speed electrical specifications are given in Table 2. This specification ensures compatibility between host bus masters and the 2-wire interface.

Table 2- Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3mA for fast mode, 20ma for Fast-mode plus
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400kHz clock rate use 3.0 k Ohms Pullup resistor, max. For 1000kHz clock rate refer to Figure 40
			200	pF	For 400kHz clock rate use 1.6 k Ohms pullup resistor, max. For 1000kHz clock rate refer to Figure 40.
InitMode, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
	|Iin|		360	uA	0V<Vin<Vcc
IntL	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	10k ohms pull up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

4.1.3 Timing for soft control and status functions

Timing for QSFP-DD soft control and status functions are described in Table 3.

Table 3- Timing for QSFP-DD soft control and status functions

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[1] , hot plug or rising edge of reset until completion of the MgmtInit State
ResetL Assert Time	t_reset_init	10		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read[2] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Deassert Time (optional fast mode)	toff_losf		3	ms	Time from Rx LOS condition absent to negation of Rx LOS status bit.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)[3] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)[3] until associated IntL operation resumes
Application or Rate Select Change Time	t_ratesel		100	ms	Time from change of state of Application or Rate Select bit[3] until transmitter or receiver bandwidth is in conformance with appropriate specification
Note 1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 6.					
Note 2. Measured from the rising edge of SDA in the stop bit of the read transaction					
Note 3. Measured from the rising edge of SDA in the stop bit of the write transaction					
Note 4. Rx LOS condition is defined at the optical input by the relevant standard					

Squelch and disable timings are defined in Table 4.

Table 4- I/O Timing for Squelch & Disable

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached. See Subsection 4.1.4.1.
Rx Squelch Deassert Time	toff_Rxsq	15	ms	Time from resumption of Rx input signals until normal Rx output condition is reached. See subsection 4.1.4.1.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached. See subsection 4.1.4.2.
Tx Squelch Deassert Time	toff_Txsq	400	ms	Time from resumption of Tx input signals until normal Tx output condition is reached. See subsection 4.1.4.2.
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence [1] until optical output falls below 10% of nominal
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal
Tx Disable Deassert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled
Note 1: Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction				

4.1.4 High Speed Electrical Specification

For detailed electrical specifications see the appropriate specification, e.g. 802.3ba Annex 86A, 802.3bs Annex 120E or Annex 120C, FC-PI-6, FC-PI-7, OIF-CEI-28G-VSR, OIF-CEI-56G-VSR or the InfiniBand specification.
Partial or complete squelch specifications may be provided in the appropriate specification. Where squelch is not fully defined by the appropriate specification, the recommendations of the following subsections 4.1.4.1 and 4.1.4.2 may be used.

4.1.4.1 Rx(n)(p/n)

Rx(n)(p/n) are QSFP-DD module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the QSFP-DD module and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 900 mVpp or the relevant standard, whichever is less.

Output squelch for loss of optical input signal, hereafter RX Squelch, is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, then the receiver output(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output as shown in Section 5.10.4. In the squelched state output impedance levels are maintained while the differential voltage amplitude shall be less than 50 mVpp.

In normal operation the default case has RX Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface.

4.1.4.2 Tx(n)(p/n)

Tx(n)(p/n) are QSFP-DD module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the QSFP-DD optical module. The AC coupling is implemented inside the QSFP-DD optical module and not required on the Host board.

Output squelch for loss of electrical signal, hereafter Tx Squelch, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input channel becoming less than 70 mVpp, then the transmitter optical output associated with that electrical input channel shall be squelched and the associated TxLOS flag set. If multiple electrical input channels are associated with the same optical output channel, the loss of any of the incoming electrical input channels causes the optical output channel to be squelched.

For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch is an optional function. If TX squelch is implemented, the disable squelch must be provided.

4.2 Power Requirements

The power supply has six designated pins, VccTx, VccTx1, Vcc1, Vcc2, VccRx, VccRx1 in the connector. Vcc1 and Vcc2 are used to supplement VccTx, VccTx1, VccRx or VccRx1 at the discretion of the module vendor. Power is applied concurrently to these pins.

A host board together with the QSFP-DD module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All power supply requirements in Table 6 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

4.2.1 Power Classes and Maximum Power Consumption

There are two power modes; Low Power Mode and High Power Mode, and eight power classes, Class 1 - Class 8. Module power modes are defined in Table 6 and power classes are defined in Table 5.

Since a wide range of module power classes exist, to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to accommodate only low power consumption modules, it is recommended that the host implement the state machine defined in the QSFP-DD Management Interface Specification and identify the power class of the module before allowing the module to go into high power mode.

Table 5- Power Classes

Power Class	Max Power (W)
1	1.5
2	3.5
3	7.0
4	8.0
5	10
6	12
7	14
8	>14

In general, the higher power classification levels are associated with higher data rates and longer reaches. The system designer is responsible for ensuring that the maximum case temperature does not exceed the case temperature requirements.

4.2.2 Host Board Power Supply Filtering

The host board should use the power supply filtering equivalent to that shown in Figure 6.

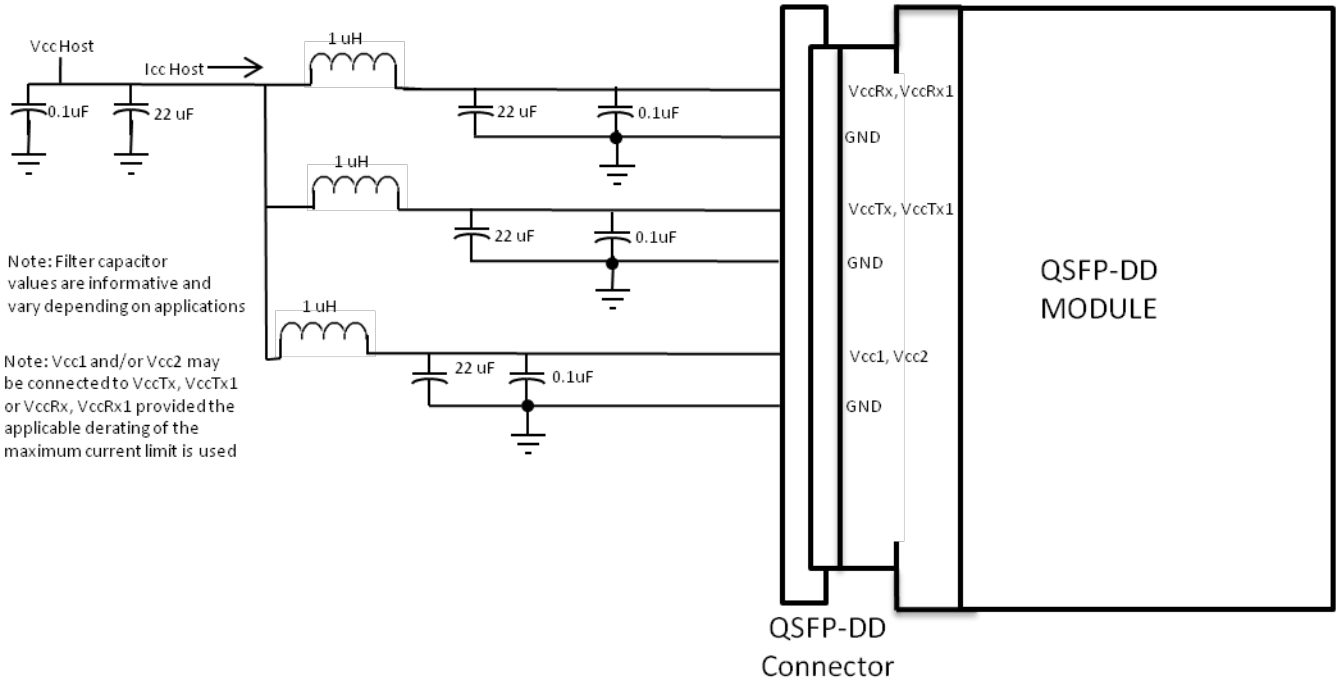


Figure 6: Recommended Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Card Edge Connector. It is recommended that the 22 uF capacitors each have an equivalent series resistance of 0.22 ohm.

The specifications for the power supply are shown in Table 6. The limits in Table 6 apply to the combined current that flows through all inductors in the power supply filter (represents ICC host in Figure 6). The test method for measuring inrush current can be found in Keysight Technologies application brief 5991-2778EN.pdf.

4.2.3 Module Power Supply Specification

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all QSFP-DD modules shall power up in Low Power Mode if InitMode is asserted. If InitMode is not asserted the module will proceed to High Power Mode without host intervention. Figure 7 shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes. Specification values for maximum instantaneous, sustained and steady state currents at each power class are given in Table 6.

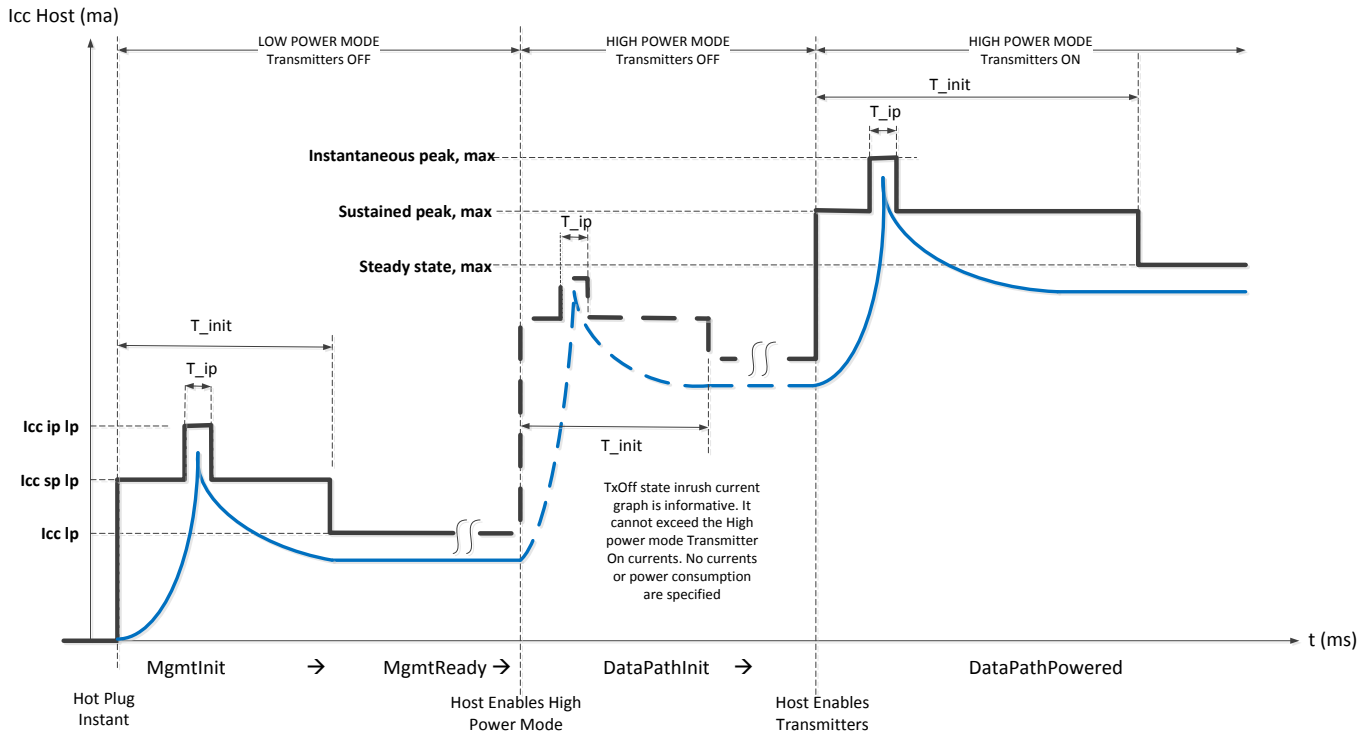


Figure 7: Instantaneous and sustained peak currents for Icc Host (see Fig. 6)

4.2.4 Host Board Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than the value in Table 6 when tested by the methods of SFF-8431, section D.17.1.

4.2.5 Module Power Supply Noise Output

The QSFP-DD module shall generate less than the value in Table 6 when tested by the methods of SFF-8431, section D.17.2. Note: The series resister specified in D.17 Figure 56 may need to be reduced for high power modules.

4.2.6 Module Power Supply Noise Tolerance

The QSFP-DD module shall meet all requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 6, swept from 10 Hz to 10 MHz according to the methods of SFF-8431, section D.17.3. This emulates the worst case noise output of the host.

Table 6- Power Supply specifications, Instantaneous, sustained and steady state current limits

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccTx, VccTx1, VccRx, VccRx1, Vcc1 & Vcc2 including ripple, droop and noise below 100kHz[1]		3.135	3.3	3.465	V
Host RMS noise output 10 Hz-10 MHz				25	mV
Module RMS noise output 10 Hz - 10 MHz				15	mV
Module power supply noise tolerance 10 Hz - 10 MHz (peak-to-peak)	$PSNR_{mod}$			66	mV
Module inrush - instantaneous peak duration	T_ip			50	µs
Module inrush - initialization time	T_init			500	ms
Low Power Mode					
Power Consumption	P_lp			1.5	W
Instantaneous peak current at hot plug	Icc_ip_lp	-	-	600	mA
Sustained peak current at hot plug	Icc_sp_lp	-	-	495	mA
Steady state current	Icc_lp	See Note 2			mA
High Power Mode Power Class 1 module					
Power Consumption	P_1			1.5	W
Instantaneous peak current	Icc_ip_1	-	-	600	mA
Sustained peak current	Icc_sp_1	-	-	495	mA
Steady state current	Icc_1	See Note 2			mA
High Power Mode Power Class 2 module					
Power Consumption	P_2			3.5	W
Instantaneous peak current	Icc_ip_2	-	-	1400	mA
Sustained peak current	Icc_sp_2	-	-	1155	mA
Steady state current	Icc_2	See Note 2			mA
High Power Mode Power Class 3 module					
Power Consumption	P_3			7	W
Instantaneous peak current	Icc_ip_3	-	-	2800	mA
Sustained peak current	Icc_sp_3	-	-	2310	mA
Steady state current	Icc_3	See Note 2			mA
High Power Mode Power Class 4 module					
Power Consumption	P_4			8	W
Instantaneous peak current	Icc_ip_4	-	-	3200	mA
Sustained peak current	Icc_sp_4	-	-	2640	mA
Steady state current	Icc_4	See Note 2			mA
High Power Mode Power Class 5 module					
Power Consumption	P_5			10	W
Instantaneous peak current	Icc_ip_5	-	-	4000	mA
Sustained peak current	Icc_sp_5	-	-	3300	mA
Steady state current	Icc_5	See Note 2			mA
High Power Mode Power Class 6 module					
Power Consumption	P_6			12	W
Instantaneous peak current	Icc_ip_6	-	-	4800	mA
Sustained peak current	Icc_sp_6	-	-	3960	mA
Steady state current	Icc_6	See Note 2			mA
High Power Mode Power Class 7 module					
Power Consumption	P_7			14	W
Instantaneous peak current	Icc_ip_7	-	-	5600	mA
Sustained peak current	Icc_sp_7	-	-	4620	mA
Steady state current	Icc_7	See Note 2			mA
High Power Mode Power Class 8 module					
Power Consumption	P_8[3]			>14	W
Instantaneous peak current	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current	Icc_sp_8	-	-	P_8/3.03	A
Steady state current	Icc_8	-	-	6	A

Note 1: Measured at VccTx, VccTx1, VccRx, VccRx1, Vcc1 and Vcc2
Note 2: The module must stay within its declared power class.
Note 3: User must read management register for maximum power consumption

4.3 ESD

Where ESD performance is not otherwise specified, e.g. in the InfiniBand specification, the QSFP-DD module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case. All the QSFP-DD module and host pins including high speed signal pins shall withstand 1000 V electrostatic discharge based on Human Body Model per ANSI/ESDA/JEDEC JS-001.

5 Mechanical and Board Definition

5.1 Introduction

The cages and modules defined in this section are illustrated in Figure 8 (2x1 stacked cage), Figure 9 (surface mount cage}, Figure 10 (Type 1 pluggable module) and Figure 11 (Type 2 pluggable module). All Pluggable modules and direct attach cable plugs (both Type 1 and Type 2) must mate to the connectors and cages defined in this specification. The Type 2 module allows an additional extension of the module outside of the cage to allow for flexibility in module design. Heat sink/clip thermal designs are application specific and not specifically defined by this specification. See Appendix A for informative recommendations on overall module length including handle.

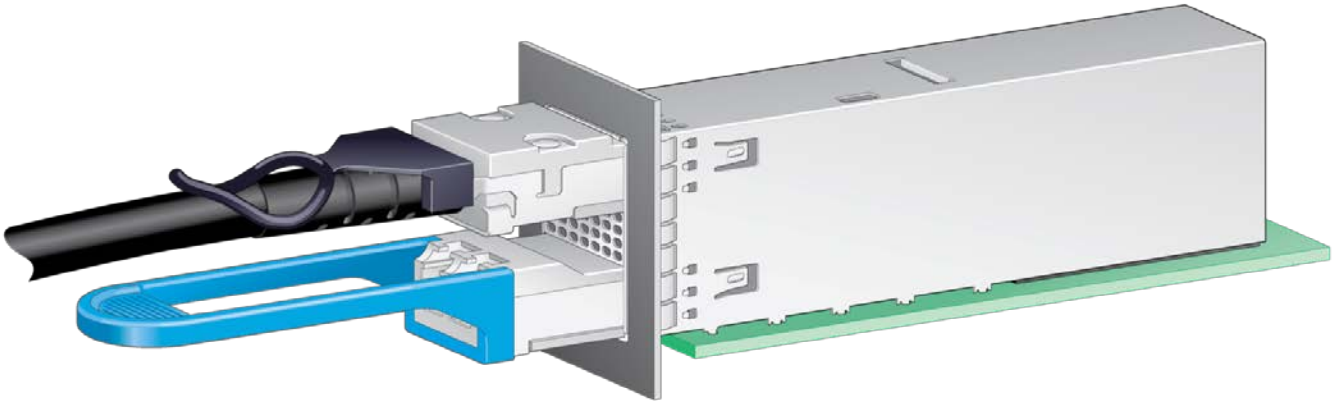


Figure 8: 2x1 stacked cage and module

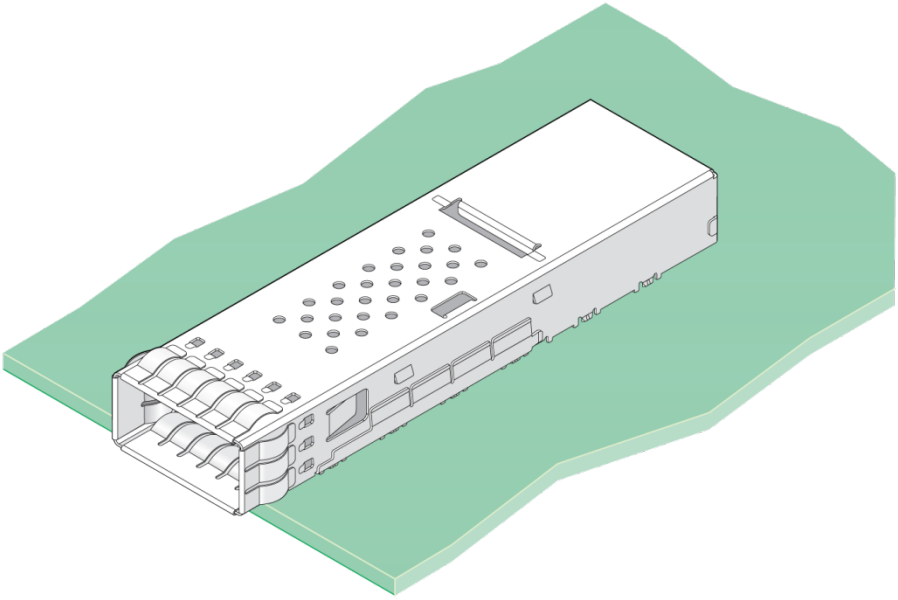


Figure 9: Press fit cage for surface mount (SMT) connector

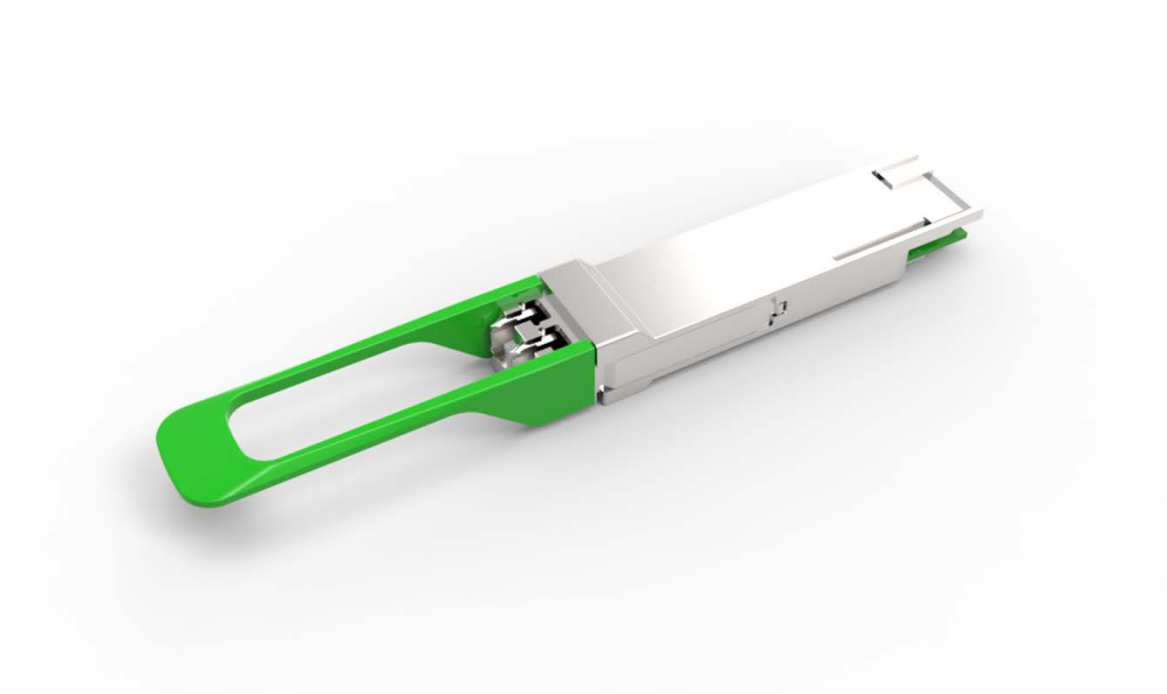


Figure 10: Type 1 Pluggable module

Figure 11: Type 2 Pluggable module

5.2 Datums, Dimensions and Component Alignment

A listing of the datums for the various components is contained in Table 7. The alignments of some of the datums are noted. In order to reduce the complexity of the drawings, all dimensions are considered centered unless otherwise specified. Dimensions and tolerancing conform to ASME Y14.5-2009. All dimensions are in millimeters.

Table 7- Datums

Datum	Description
A	Host Board Top Surface
B	Inside surface of bezel
C	**Distance between Connector terminal thru holes on host board
D	*Hard stop on module
E	**Width of module
F	Height of module housing
G	**Width of module pc board
H	Leading edge of signal contact pads on module pc board
J	Top surface of module pc board
K	*Host board thru hole #1 to accept connector guide post
L	*Host board thru hole #2 to accept connector guide post
M	**Width of bezel cut out
P	Vertical Center line of internal surface of cage
S	Seating plane of cage on host board
T	*Hard stop on cage
AA	**Connector slot width
BB	Seating plane of connector on host board
DD	Top surface of module housing
EE	Centerline of module opening to locate paddle card Datum H
FF	Centerline of upper port cage height
GG	Centerline of lower port cage height
EE	Primary Datum hole for 2x1 Host PCB
*Datums D and T are aligned when assembled (see Figure 12 and Figure 13) **Centerlines of datums AA, C, E, G, M are aligned on the same vertical plane	

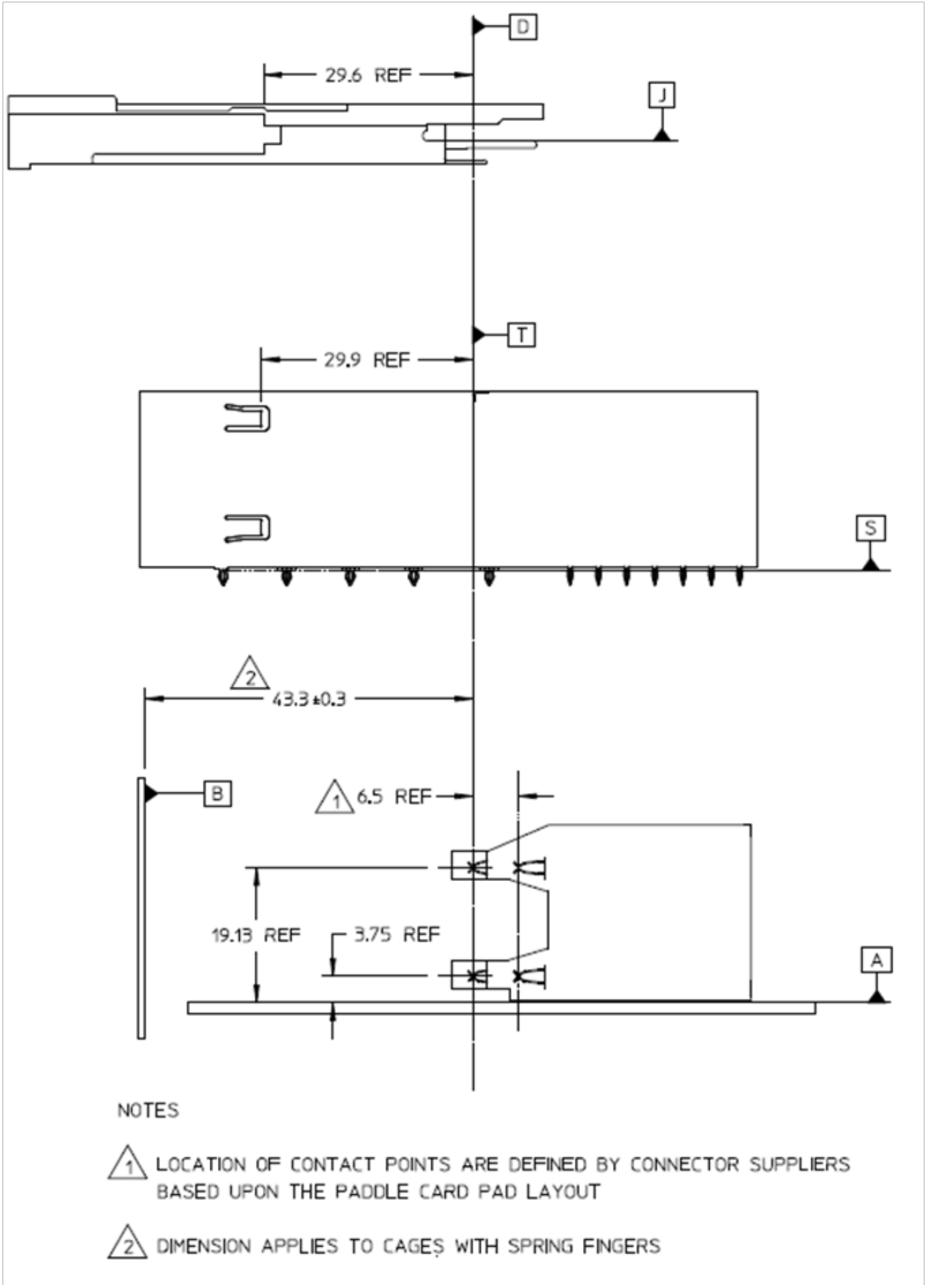


Figure 12: 2X1 stacked connector/cage datum descriptions

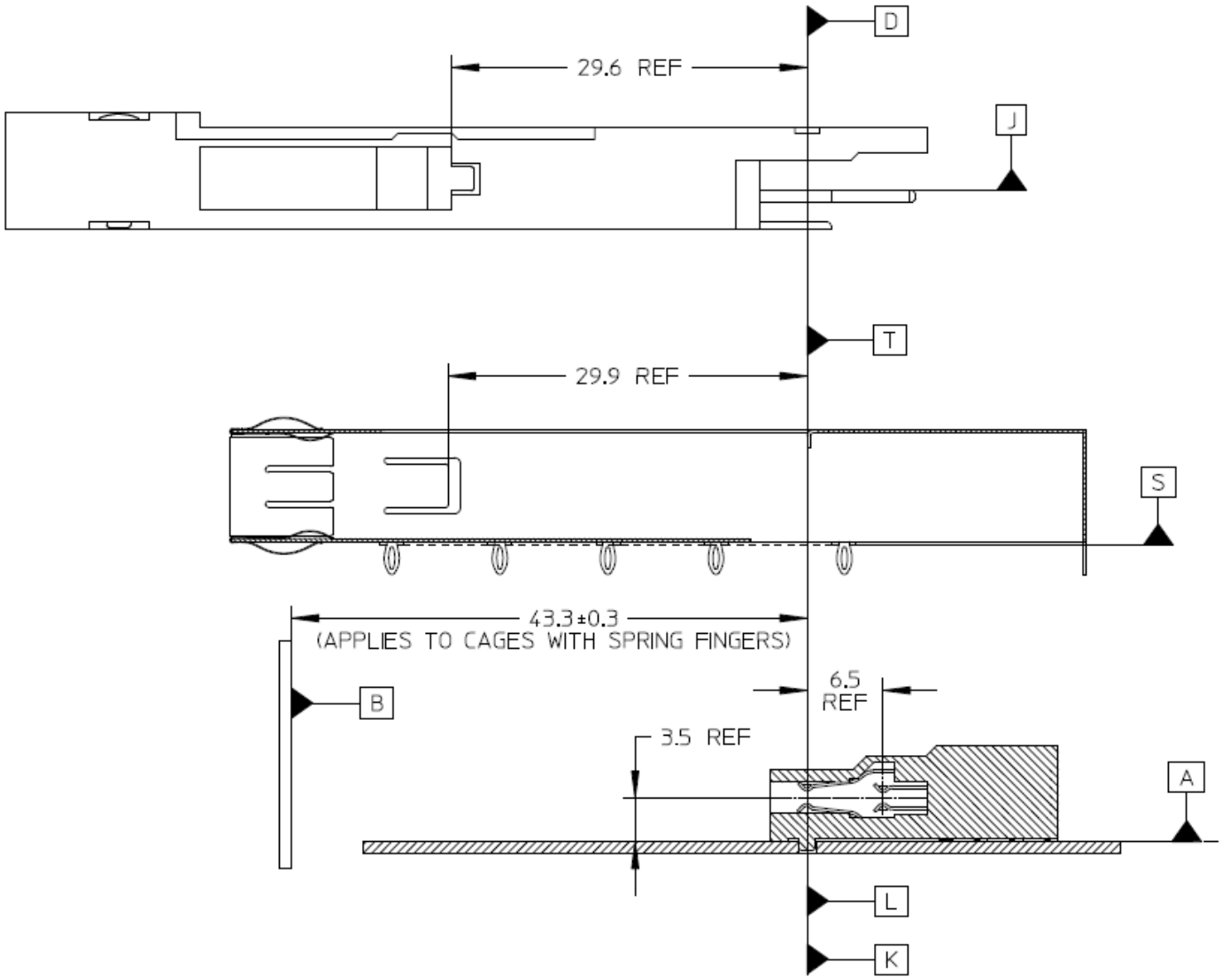


Figure 13: Surface mount connector/cage datum descriptions

5.3 Module Mechanical Dimensions

The mechanical outline for the Type 1 module is shown in Figure 14 and the Type 2 module is shown in Figure 15. The module shall provide a means to self-lock with either the 2x1 stacked cage or SMT cage upon insertion. The module package dimensions are defined in Figure 16 and Figure 17. The dimensions that control the size of the module that extends outside of the cage are listed as maximum dimensions per Note 4 in Figure 16. Note: All dimensions are in mm.

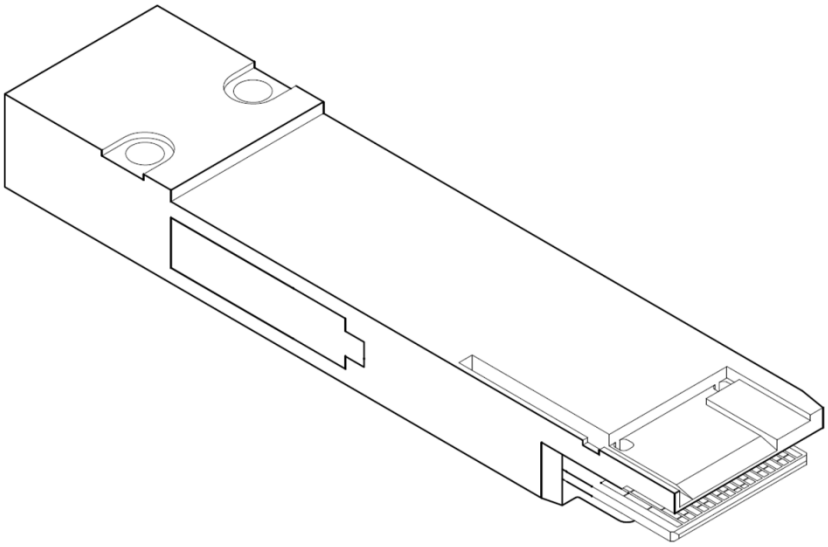


Figure 14: Type 1 Module

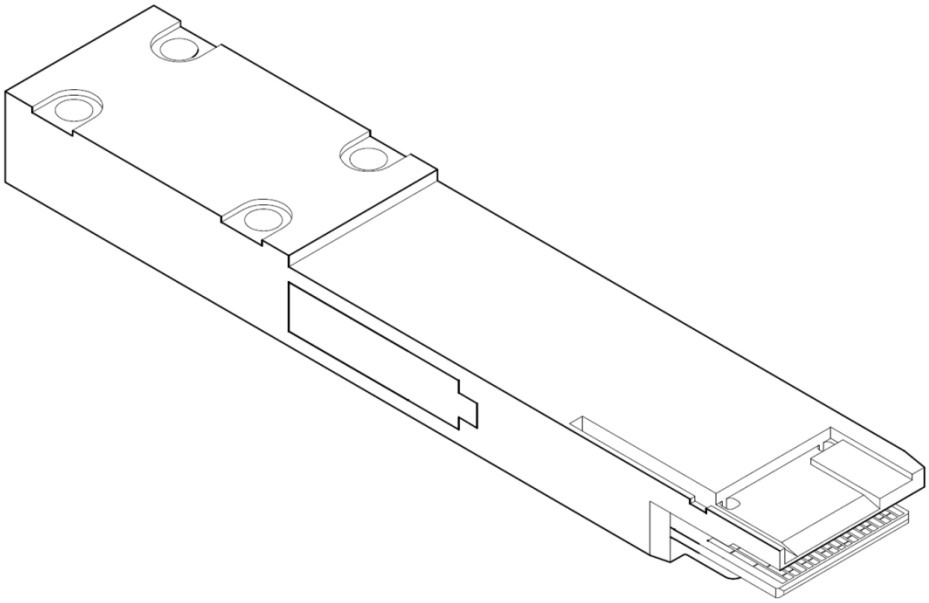


Figure 15: Type 2 Module

Notes for Module Drawings (Figures 16 and 17):

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. Sharp corners and edges are not allowed. Round off all edges and corners to a minimum radius of 0.10 mm.
4. Dimension defines enlarged section of transceiver that extends outside of cage to accommodate mating plug and actuator mechanism
5. Surfaces on all 4 sides of the 12.4 mm minimum dimension to be conductive for connection to chassis ground.
6. Dimension applies to latch mechanism
7. Dimension applies to the location of the edge of the module board pad. Datum H, contacts 21, 22, 36, and 37 are visible.
8. Dimension to include bail travel.
9. Dimensions apply to openings in the housing.
10. Optional feature to aid inspection of dimensions from Datum D.
11. Flatness and surface roughness (Ra) applies for indicated length and minimum width of 13 mm. Surface to be thermally conductive. See Section 5.4 Table 8 for flatness and roughness requirements
12. Higher wattage modules may require additional space for cooling.

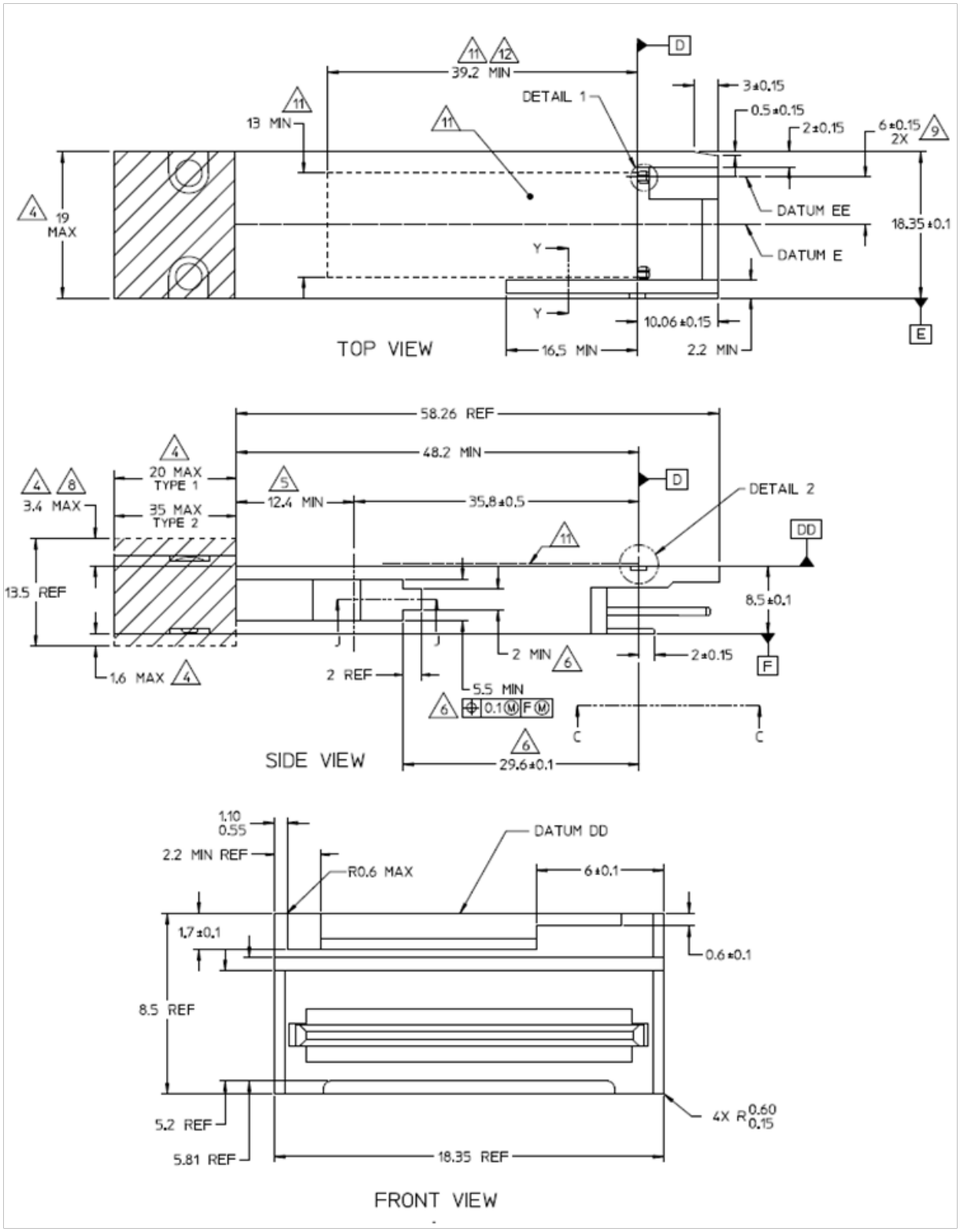
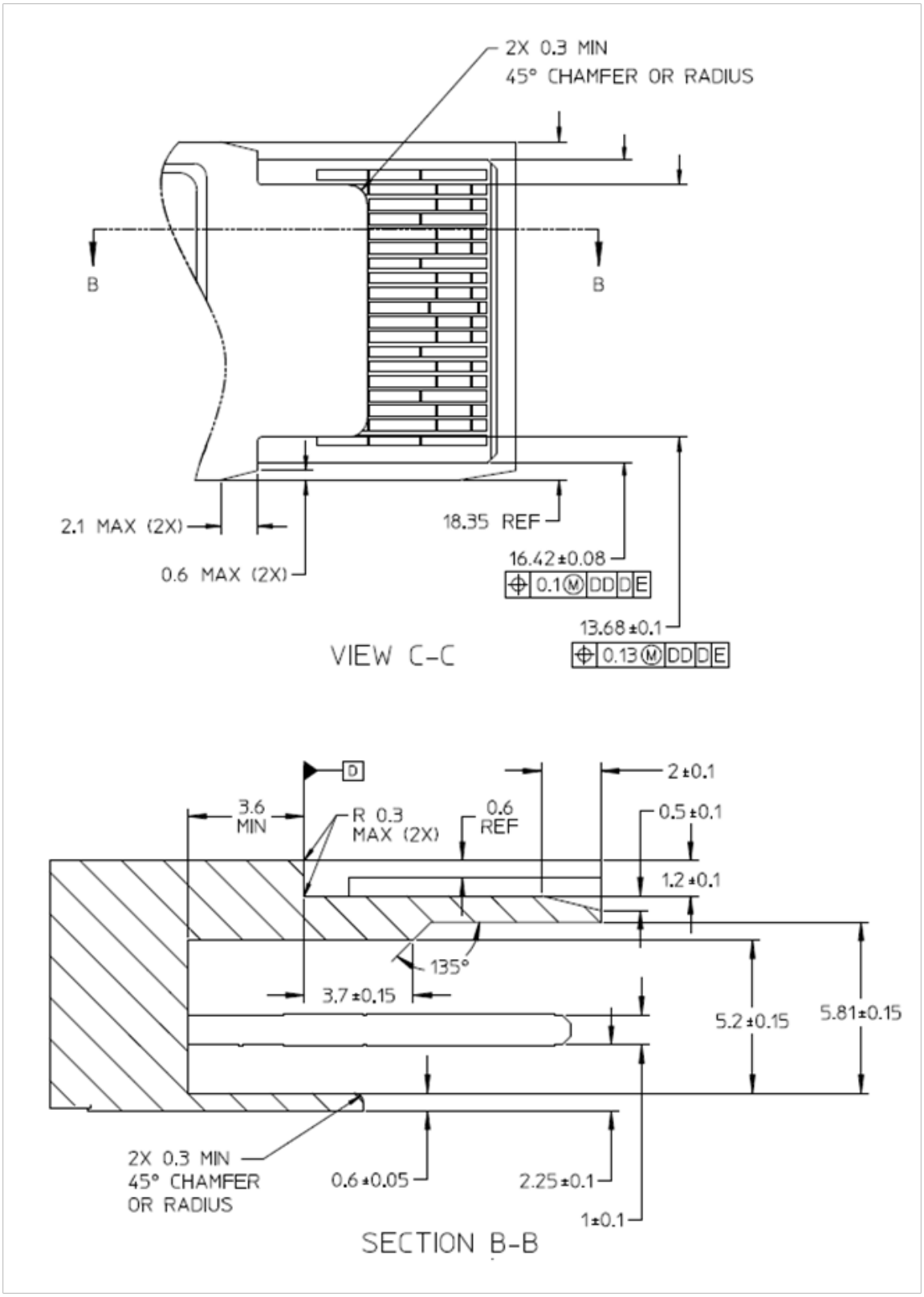


Figure 16: Drawing of module


2X 0.3 MIN
45° CHAMFER OR RADIUS
B
B
2.1 MAX (2X)
0.6 MAX (2X)
18.35 REF
16.42±0.08
0.1 M DD D E
13.68±0.1
0.13 M DD D E
VIEW C-C
D
3.6
MIN
R 0.3
MAX (2X)
0.6
REF
2±0.1
0.5±0.1
1.2±0.1
135°
3.7±0.15
5.2±0.15
5.81±0.15
2X 0.3 MIN
45° CHAMFER
OR RADIUS
0.6±0.05
2.25±0.1
1±0.1
SECTION B-B

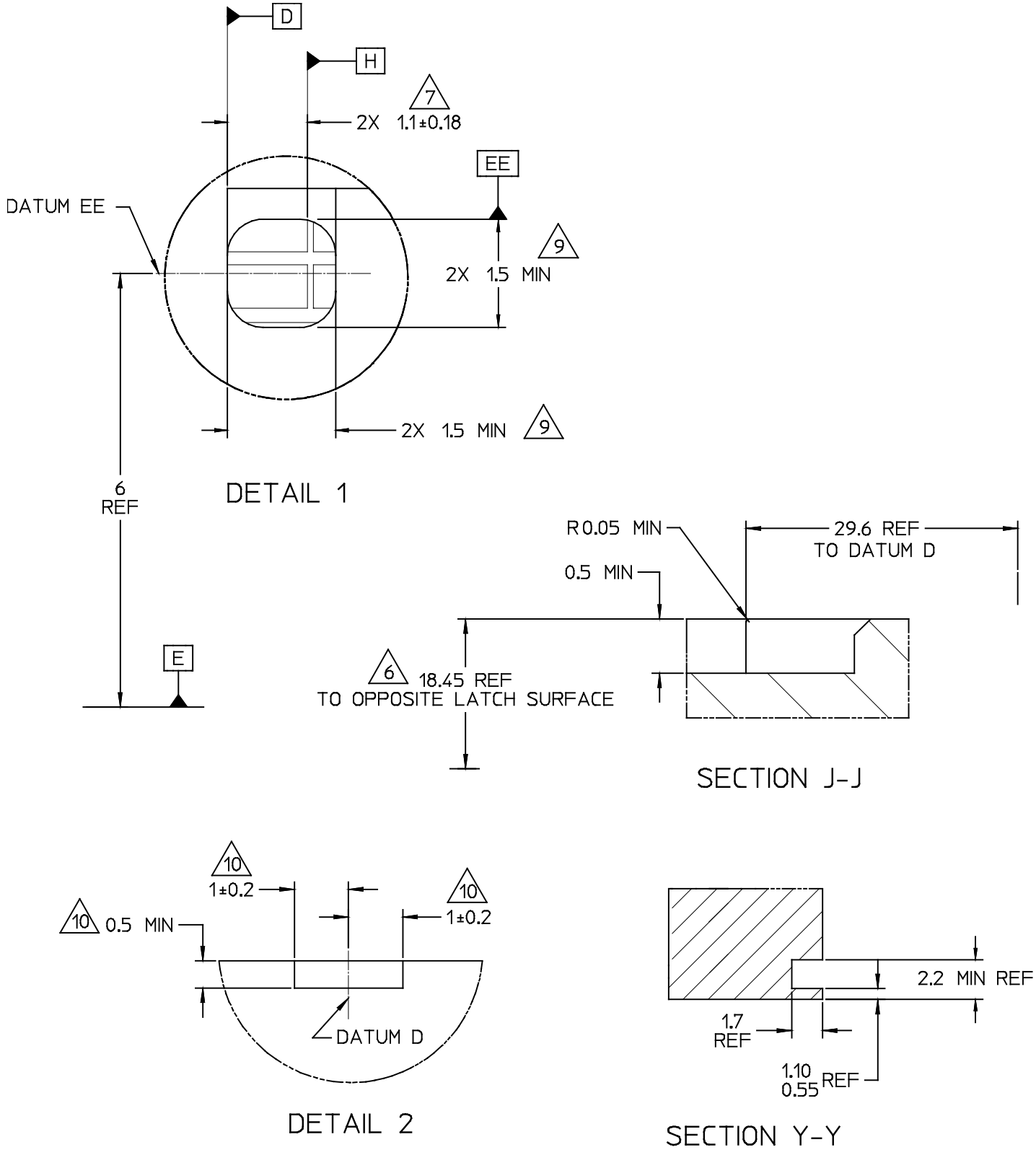


Figure 17: Detailed dimension of module

5.4 Module Flatness and Roughness

Module flatness and roughness are specified to improve module thermal characteristics when used with a riding heat sink. Relaxed specifications are used for lower power modules to reduce cost. The module flatness and roughness specifications apply to the specified heat sink contact area as specified in Figure 16. Specifications for Module flatness and surface roughness are shown in Table 8 (see Figure 16 note 11).

Table 8- Module flatness specifications

Power Class	Module Flatness (mm)	Surface Roughness (Ra,µm)
1	0.075	1.6
2	0.075	1.6
3	0.075	1.6
4	0.075	1.6
5	0.050	0.8
6	0.050	0.8
7	0.050	0.8
8	0.050	0.8

5.5 Module paddle card dimensions

Notes for Module Paddle Card Drawings (Figures 18 and 19):

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. No solder mask within 0.05 mm of all defined contact pad edges.
4. No solder mask between end contacts and the sides of the paddle card
5. Datum H is established with Datum Target points at the leading edge of the outer most signal contact pads to be re-established on each side
6. Dimension applies from the first set of signal pads to the second set of signal pads
7. Dimension and tolerance applies to all ground pads on both top and bottom side of paddle card
8. Dimension and tolerance applies to all power pads on both top and bottom side of paddle card
9. Dimension and tolerance applies to all signal pads on both top and bottom side of paddle card
10. A zero gap is allowed for a continuous pad option
11. Applies to all signal pad to pad spacing
12. Pre-wipe pads (shaded area) on module card host side are optional
13. Pre-wipe pads (unshaded area) are required except in continuous power or ground pad designs
14. Paddle card thickness is measured over pads. Vias must not be proud of the pad surface
15. Minimum dimension required for mating sequence between signal and ground pads
16. Minimum dimension required for mating sequence between signal and power pads
17. Component keep out area measured from Datum H
18. A single split in the pre-wipe signal pad is optional, and if implemented, the resulting 2 pads shall be separated with a gap of 0.13 +/- 0.05
19. Contact pad plating

    0.38 micrometers minimum gold over

    1.27 micrometers minimum nickel

    Alternate contact pad plating

    0.05 micrometers minimum gold over

    0.30 micrometers minimum palladium over

    1.27 micrometers minimum nickel

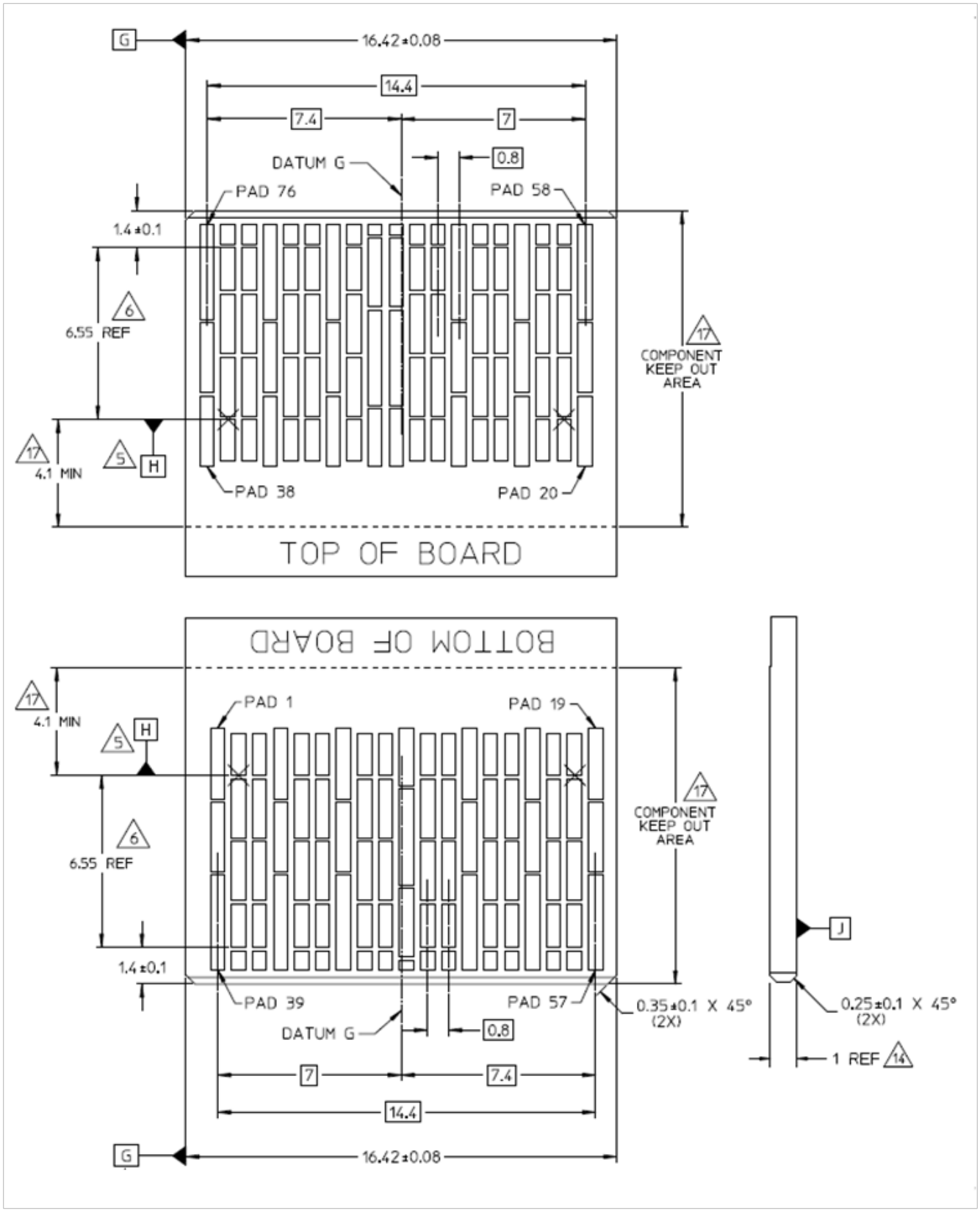


Figure 18: Module paddle card dimensions

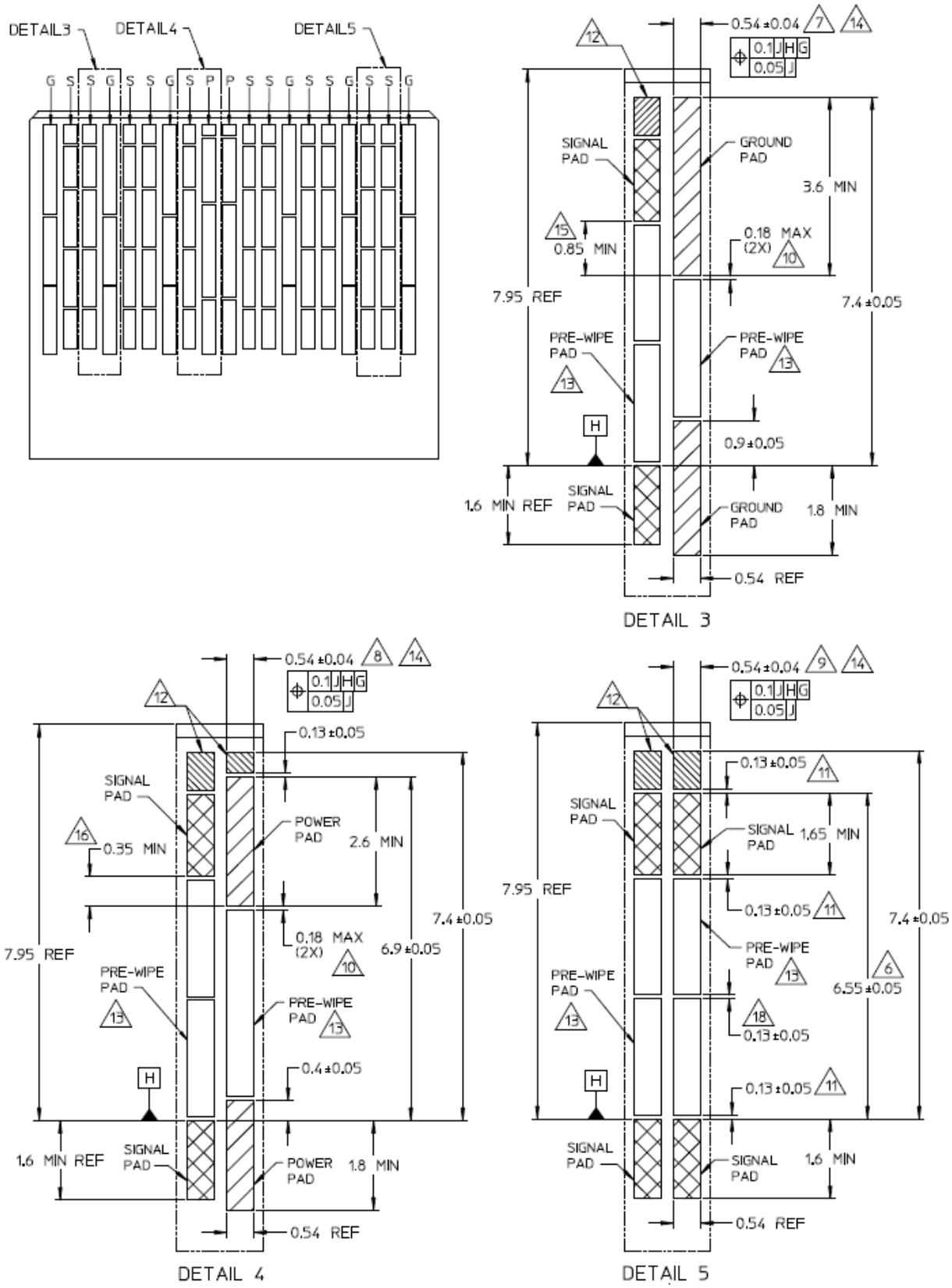


Figure 19: Module pad dimensions

5.6 Module Extraction and Retention Forces

The requirements for insertion forces, extraction forces and retention forces are specified in Table 9. The QSFP-DD cage and module are designed to ensure that excessive force applied to a cable does not damage the QSFP-DD cage or host connector. If any part is damaged by excessive force, it should be the cable or media module and not the cage or host connector which is part of the host system. The contact pad plating shall meet the requirements of Section 5.5.

Table 9- Insertion, Extraction and Retention Forces

Measurement	Min	Max	Units	Comments
QSFP module insertion	0	40	N	
QSFP-DD module insertion	0	90	N	
QSFP module extraction	0	30	N	
QSFP-DD module extraction	0	50	N	
QSFP module retention	90	N/A	N	No damage to module below 90N with latch engaged
QSFP-DD module retention	90	N/A	N	No damage to module below 90N with latch engaged
Cage retention (Latch strength)	125	N/A	N	No damage to latch below 125N
Cage retention in Host Board	114	N/A	N	Force to be applied in a vertical direction, no damage to cage
Insertion / removal cycles, connector / cage	100	N/A	Cycles	Number of cycles for the connector and cage with multiple modules.
Insertion / removal cycles, QSFP-DD module	50	N/A	Cycles	Number of cycles for an individual module.

5.7 2x1 Electrical Connector Mechanical

The QSFP-DD Connector is a 76-contact, right angle connector. The integrated connector in a 2x1 stacked cage is shown in Figure 20 with detailed drawings in Figure 21, Figure 22 and Figure 23. Recommendations for the 2x1 stacked cage bezel opening are shown in Figure 24.

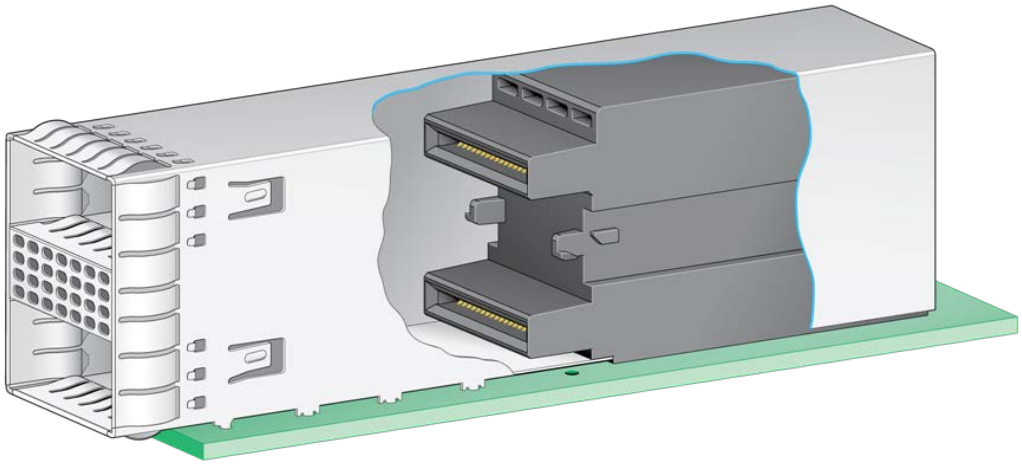


Figure 20: Integrated connector in 2x1 stacked cage

Notes for 2x1 stacked cage: (Figures 21 and 22):

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters.
3. Dimensions from inside surfaces of spring fingers when fully depressed.
4. Connector removed for drawing clarity.
5. Applies to all spring fingers on all sides.
6. External cage dimensions. Does not include folding tabs.
7. Length of cage and signal tails.
8. Press fit cage pins apply to right side of cage.
9. Press fit cage pins apply to left side of cage.
10. Press fit pin offset between right and left side of cage.
11. Dimensions includes backcover.
12. Size and position of cage and connector press fit pins shall be defined by each supplier based upon the PCB footprint layout.
13. Cavity for heat sink is optional.

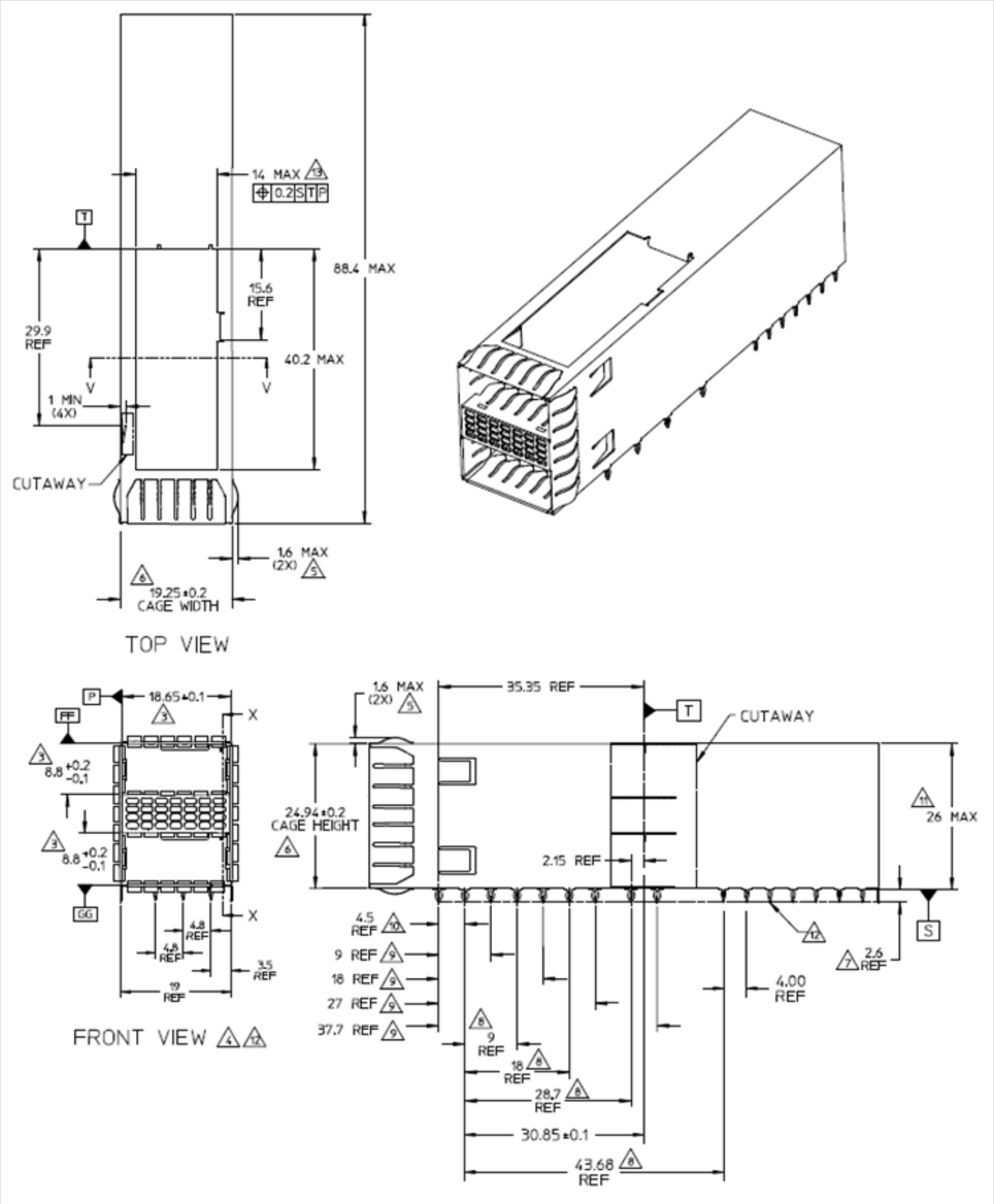


Figure 21: 2x1 stacked cage

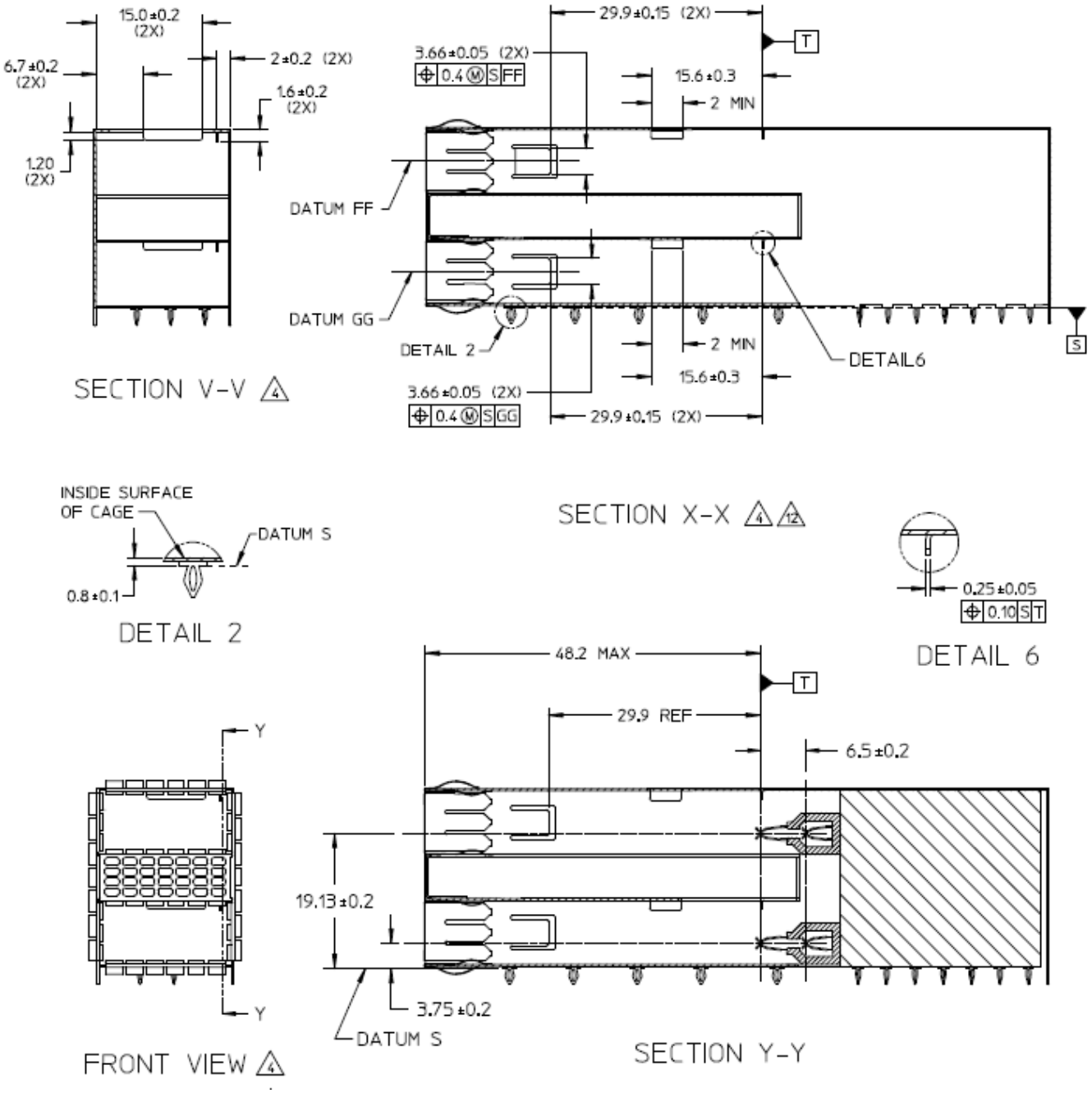


Figure 22: 2x1 stacked cage dimensions

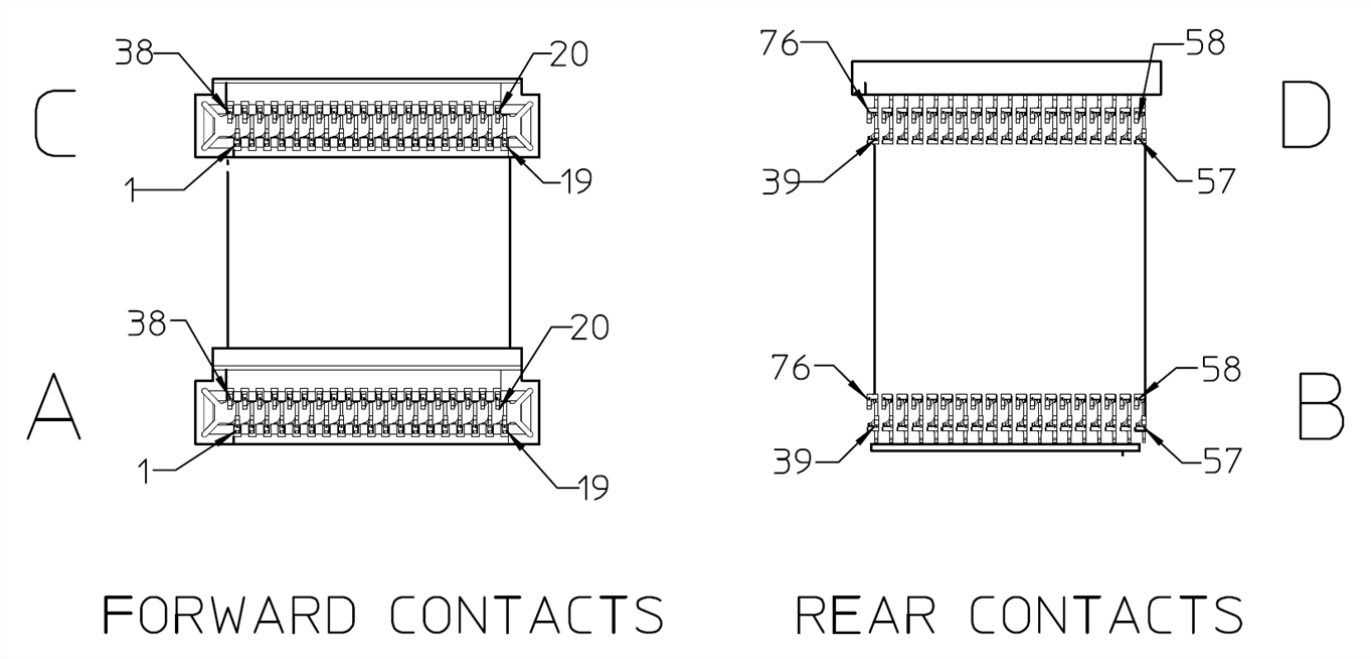


Figure 23: Connector pins in 2x1 stacked cage as viewed from the front

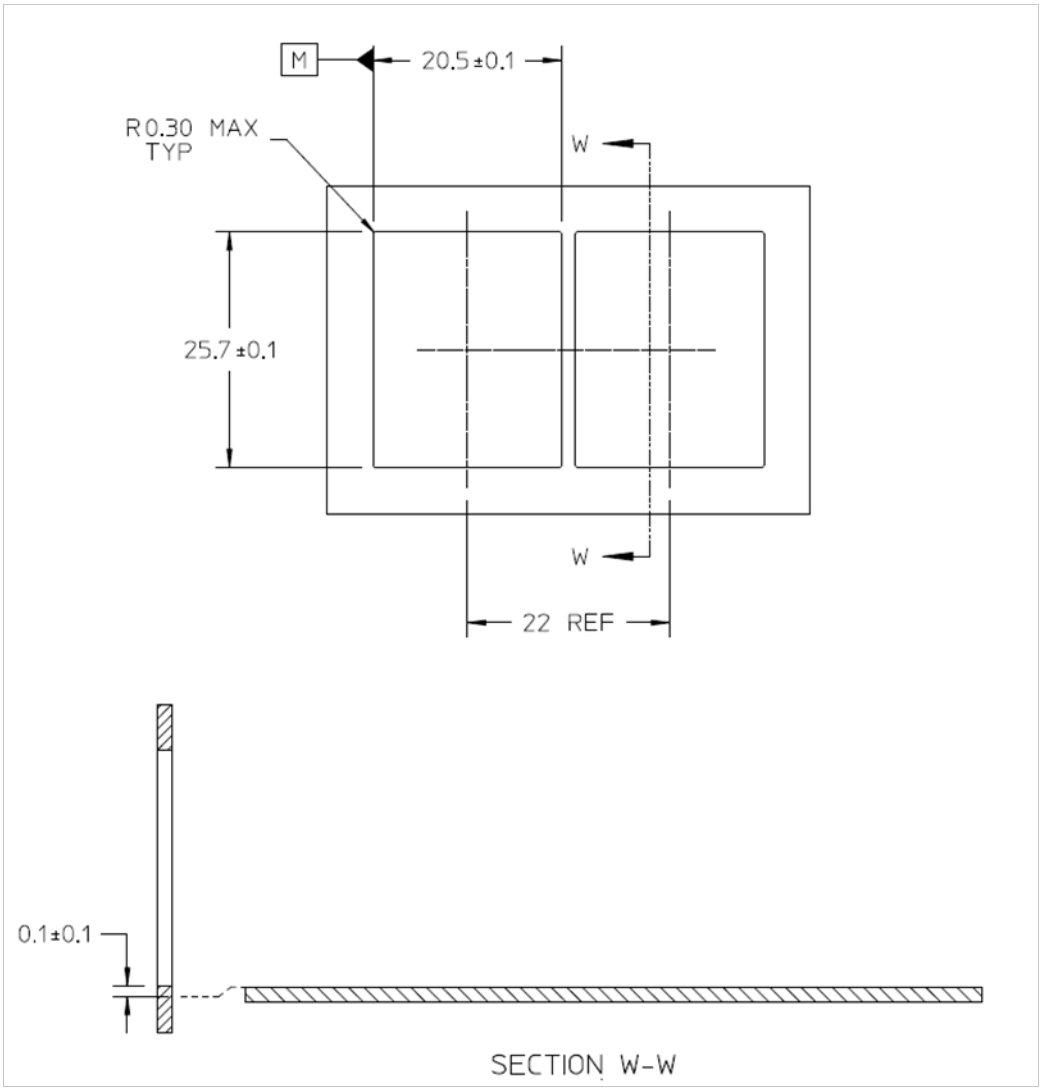


Figure 24: 2x1 Bezel Opening

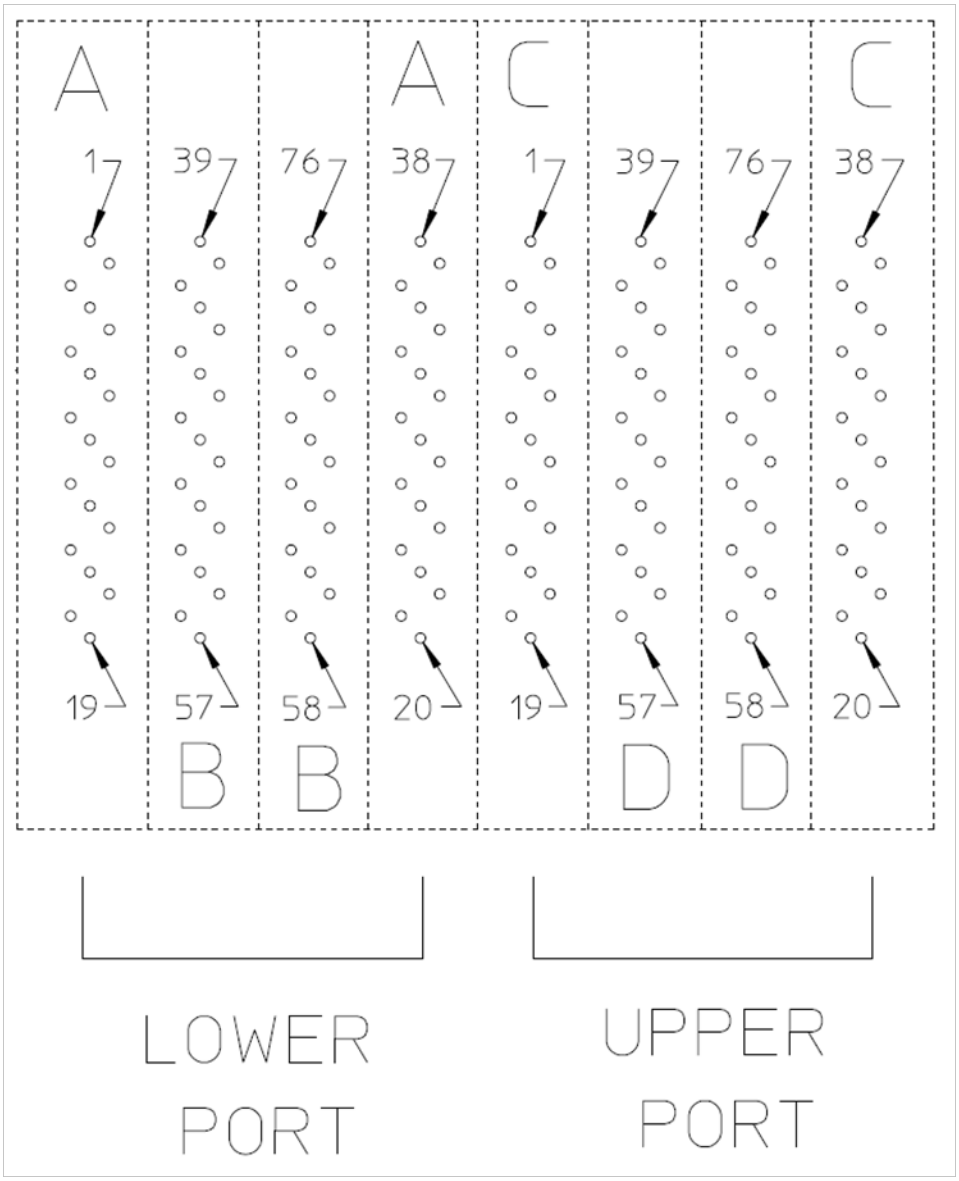


Figure 25: 2X1 host board connector contacts

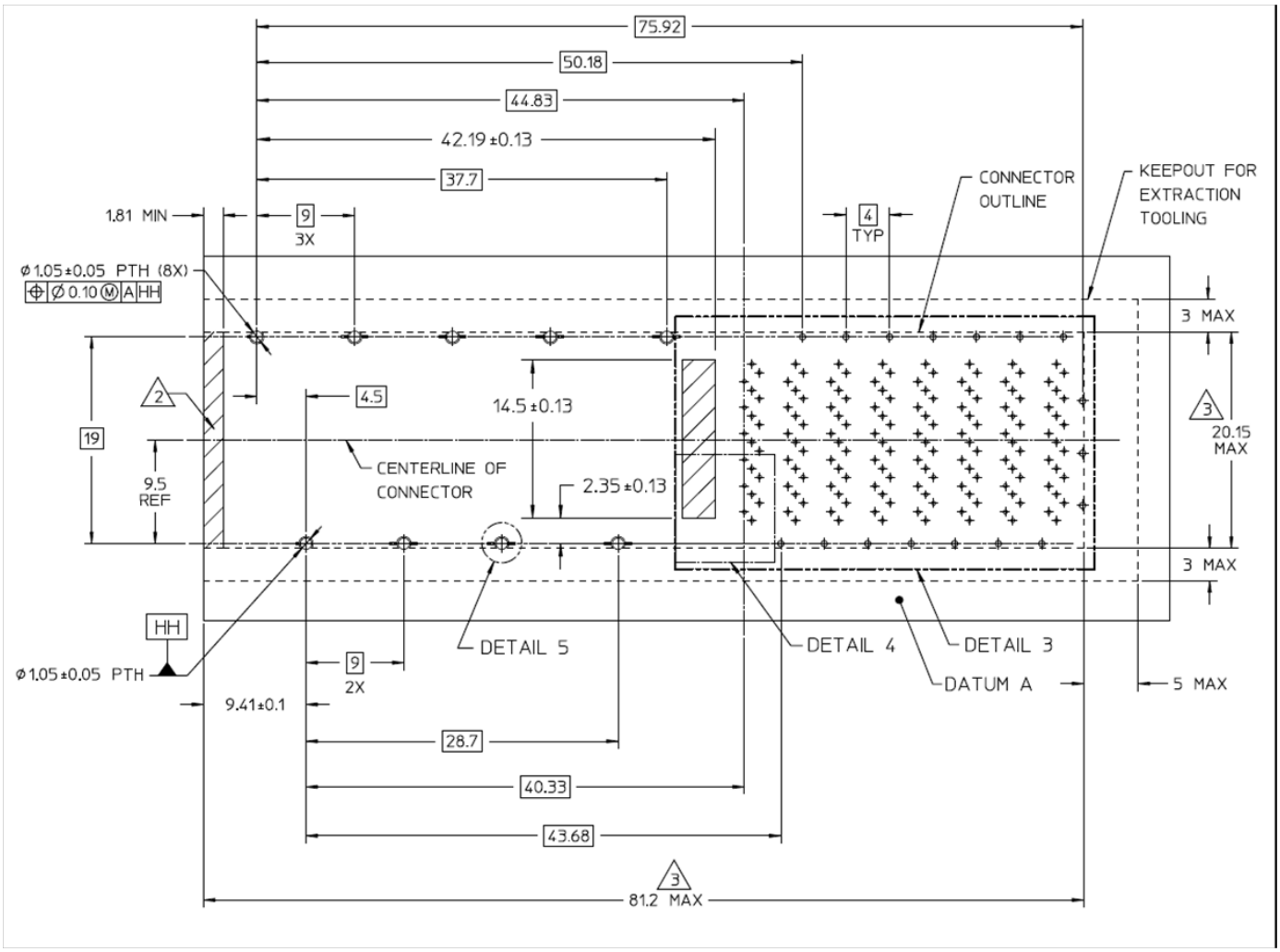
5.7.1 2x1 Connector and Cage host PCB layout

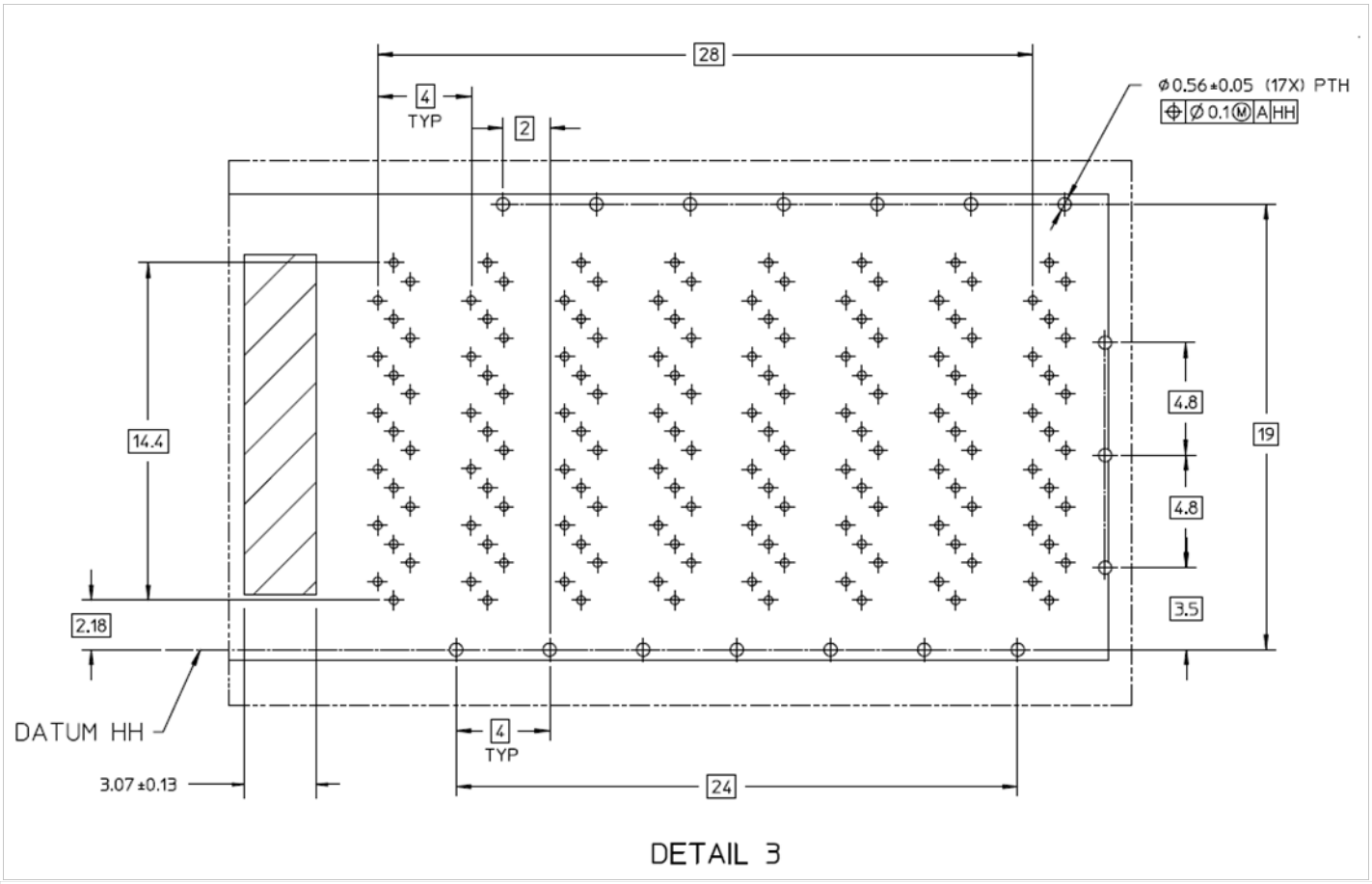
A typical host board mechanical layout for attaching the QSFP-DD 2x1 Connector and Cage System is shown in Figure 25 and Figure 26. Location of the pattern on the host board is application specific.

To achieve 25-50 Gbps performance pad dimensions and associated tolerances must be adhered to and attention paid to the host board layout.

Notes for Host PCB (Figure 26):

1. The entire area under the connector (outside dashed lines) is to be considered a keep out area for components
2. Hatched area represent zones on the PCB that come in contact with or are in close proximity to the plastic housing or the connector cage. Indicated areas to be considered trace free.
3. Dimension applies to connector outline





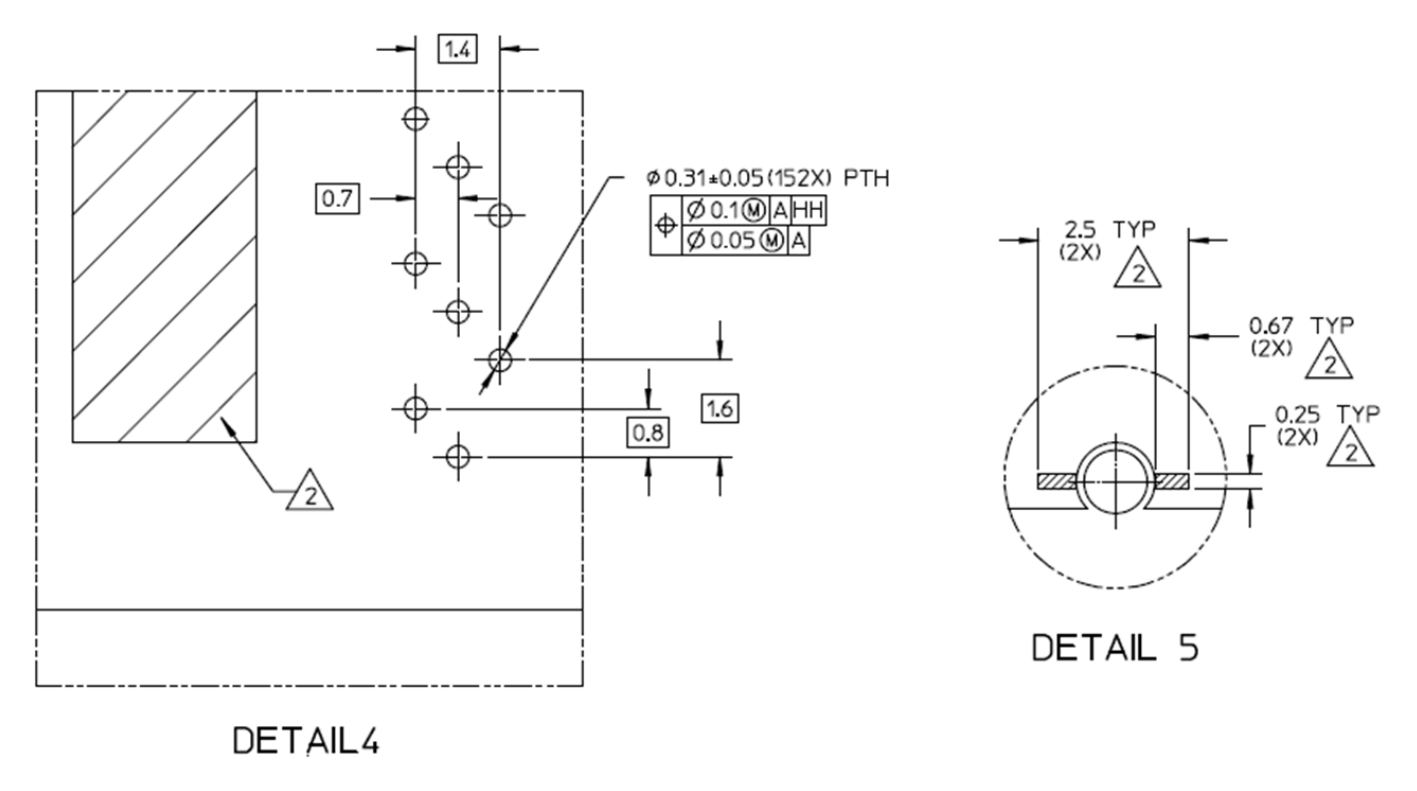


Figure 26: 2X1 Host PCB Mechanical Layout

5.8 Surface Mount Electrical Connector Mechanical

The QSFP-DD Connector is a 76-contact, right angle connector. The SMT connector in a 1xn cage is shown in Figure 27 with detailed drawings in Figure 28 and Figure 29. Recommendations for the SMT cage bezel opening are shown in Figure 30.

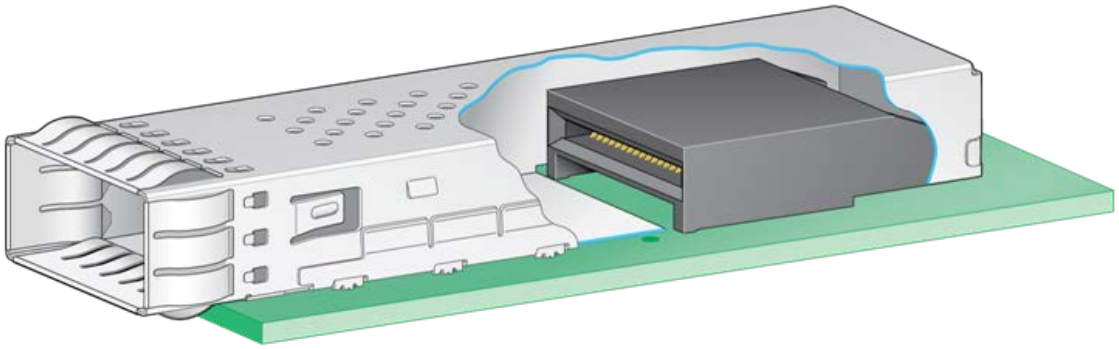
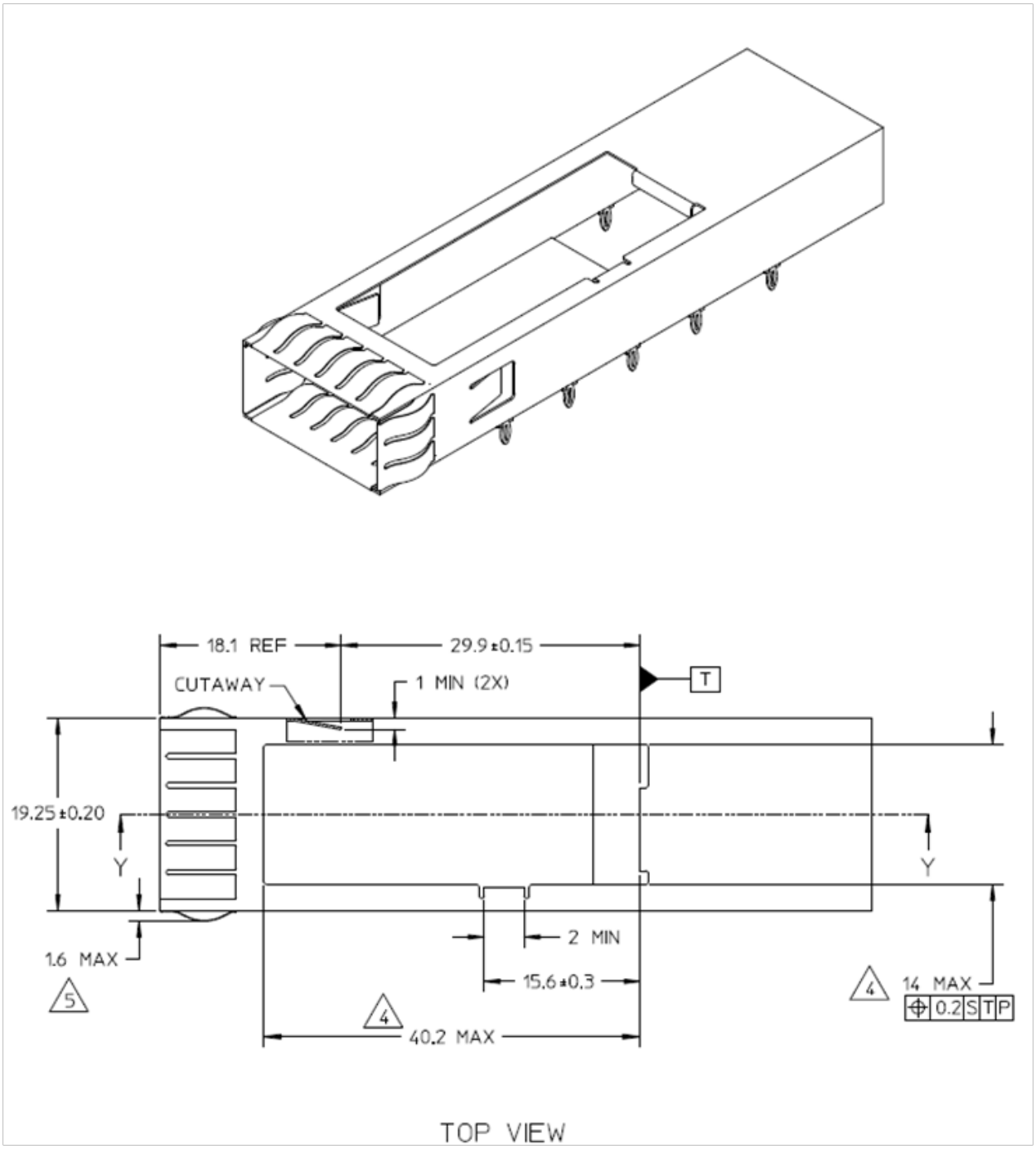


Figure 27: SMT connector in 1xn cage

Notes for SMT 1 x N Cage Drawings (Figure 28, 29, 30):

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. Dimensions from inside surfaces of spring fingers when fully depressed.
4. Cavity for heat sink is optional
5. Applies to all spring fingers on all sides
6. Datum S is defined by seating plane on host board
7. Size and position of cage press fit pins shall be defined by each supplier based upon the PCB footprint layout.


18.1 REF
29.9±0.15
CUTAWAY
1 MIN (2X)
T
19.25±0.20
Y
Y
1.6 MAX
5
2 MIN
15.6±0.3
4
40.2 MAX
4
14 MAX
0.2 S T P
TOP VIEW

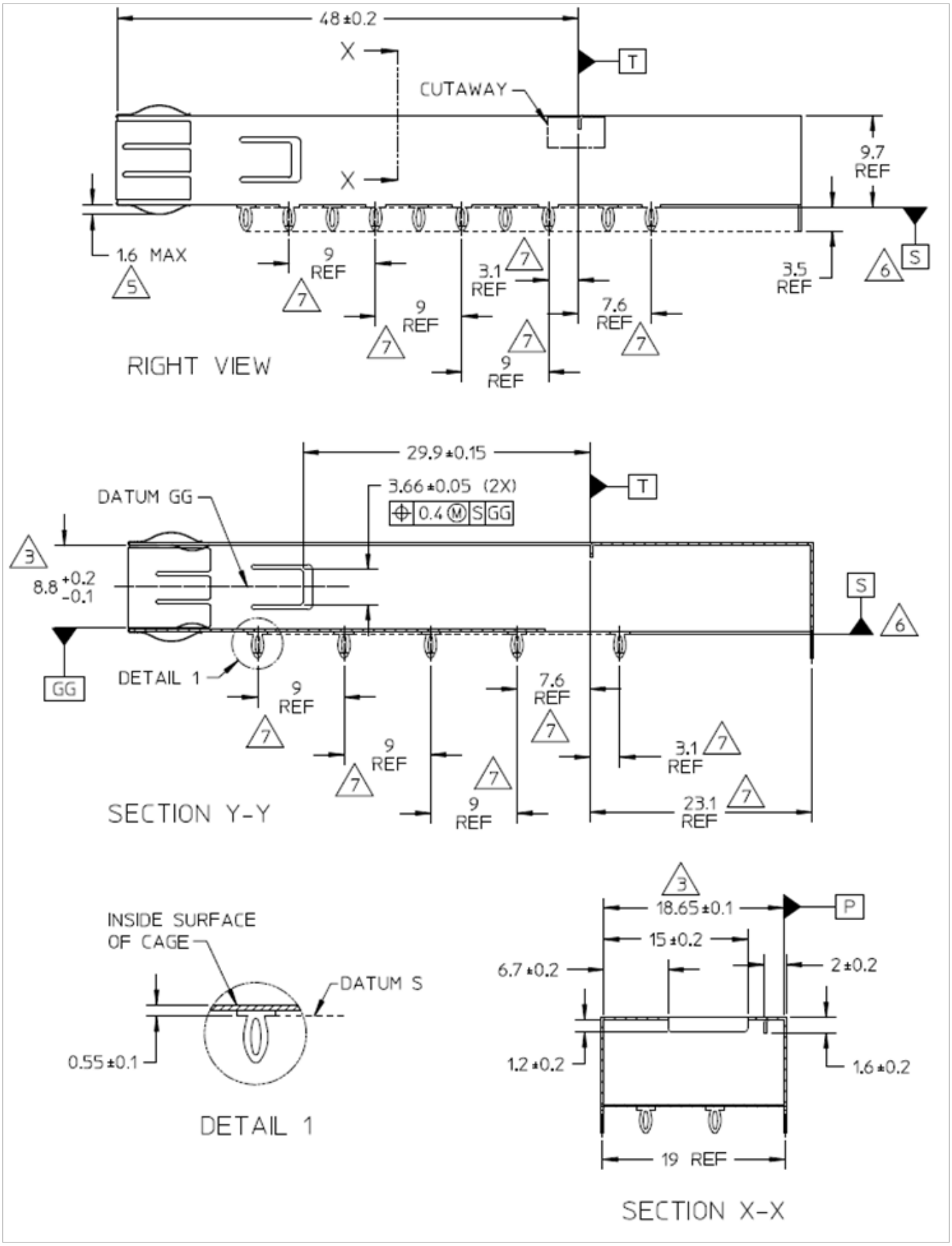
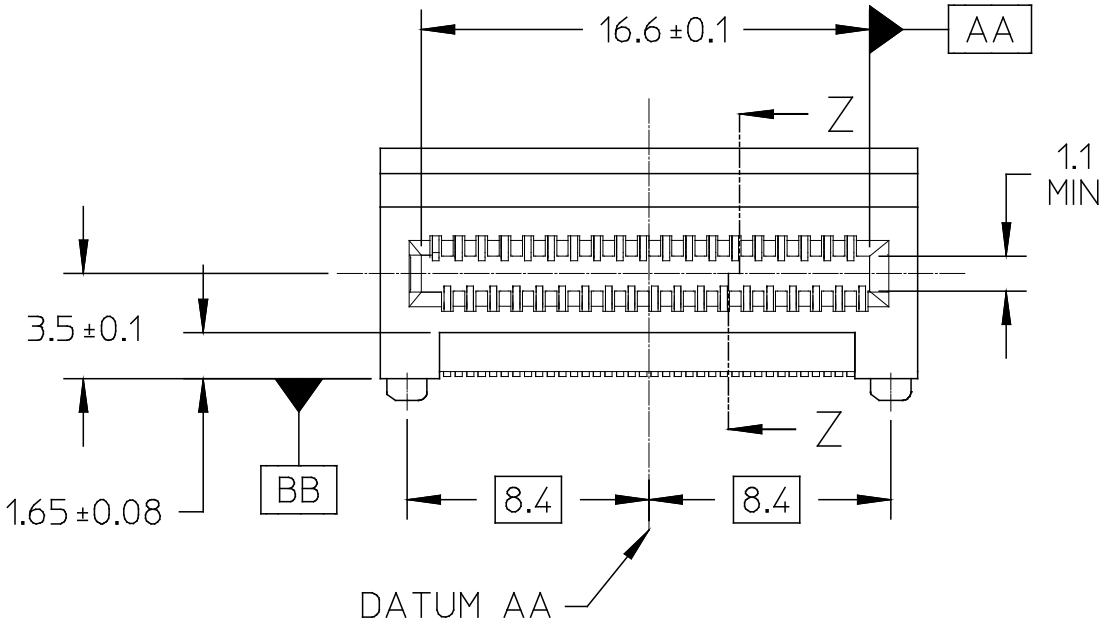
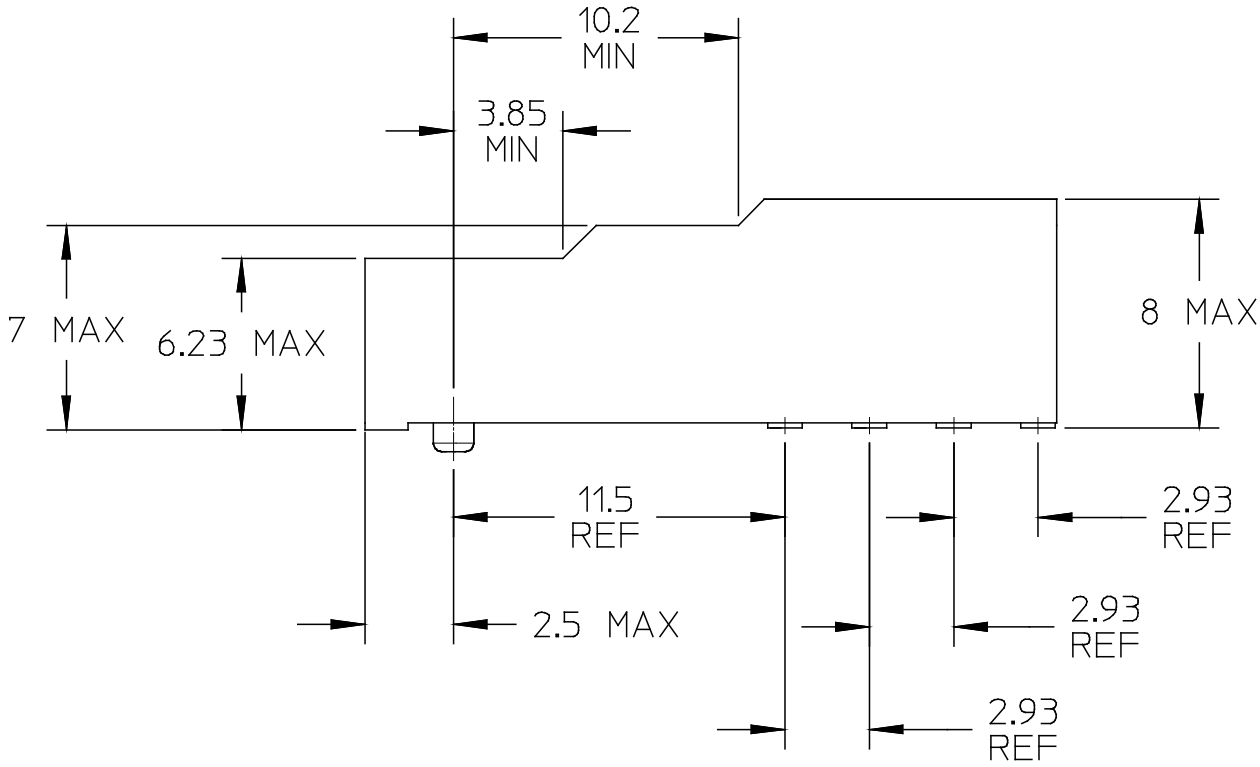


Figure 28: SMT 1x1 Cage Design



FRONT VIEW



SIDE VIEW

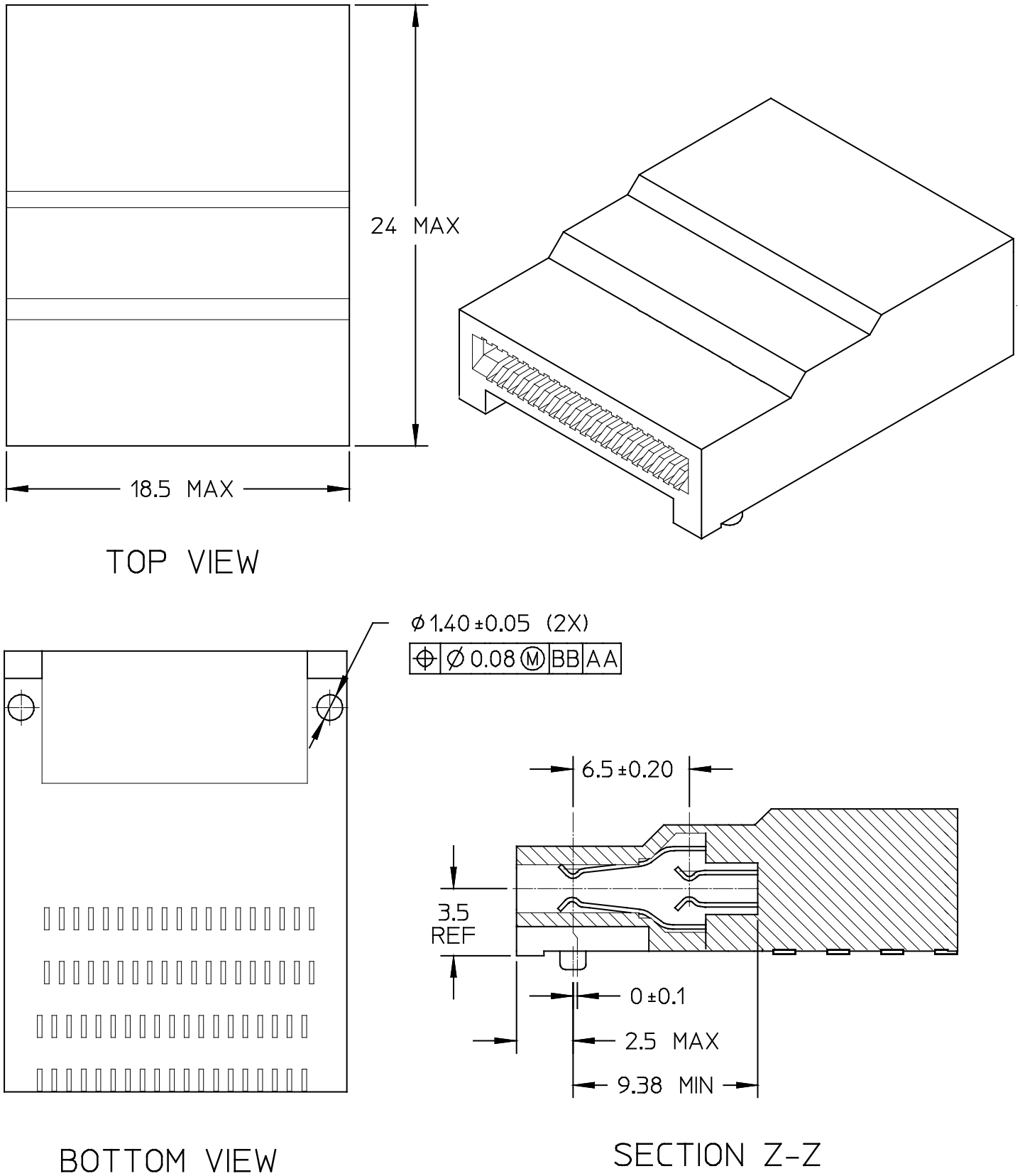


Figure 29: SMT 1x1 Connector Design

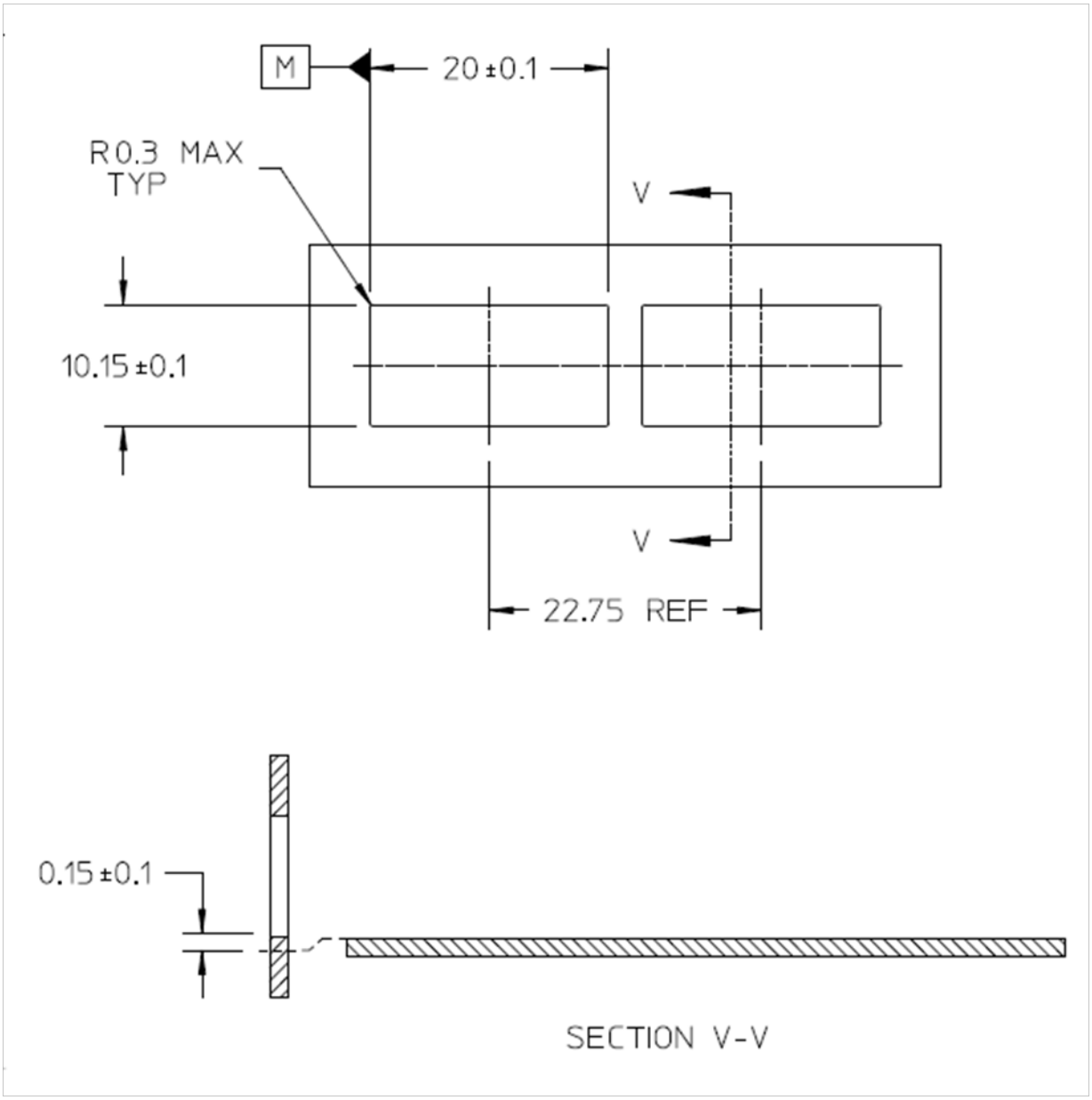


Figure 30: SMT 1xn bezel opening

5.8.1 Surface mount connector and cage host PCB layout

A typical host board mechanical layout for attaching the QSFP-DD surface mount Connector and Cage System is shown in Figure 31 and Figure 32. Location of the pattern on the host board is application specific.

To achieve 25-50 Gbps performance pad dimensions and associated tolerances must be adhered to and attention paid to the host board layout.

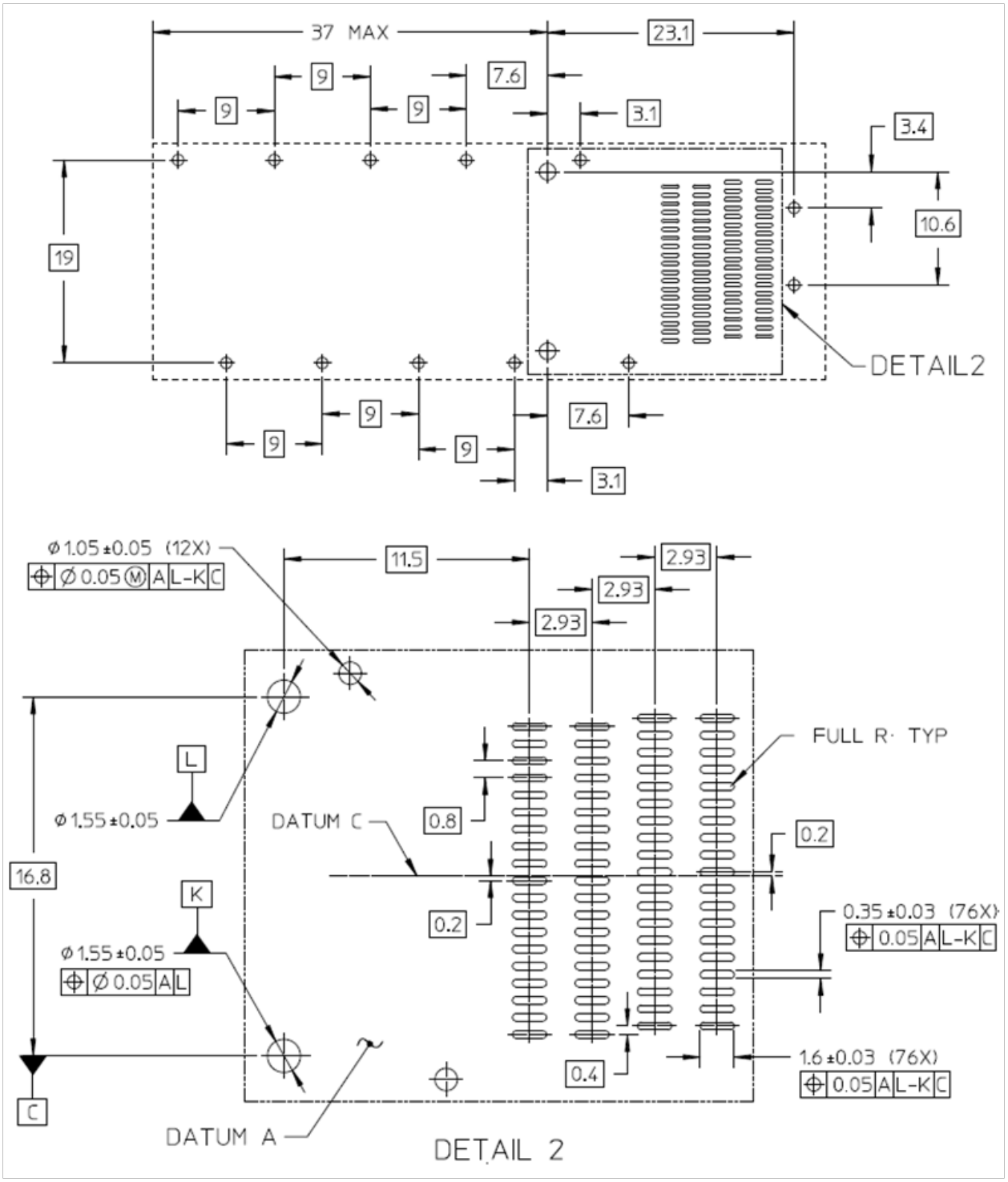


Figure 31: SMT Host PCB Mechanical Layout

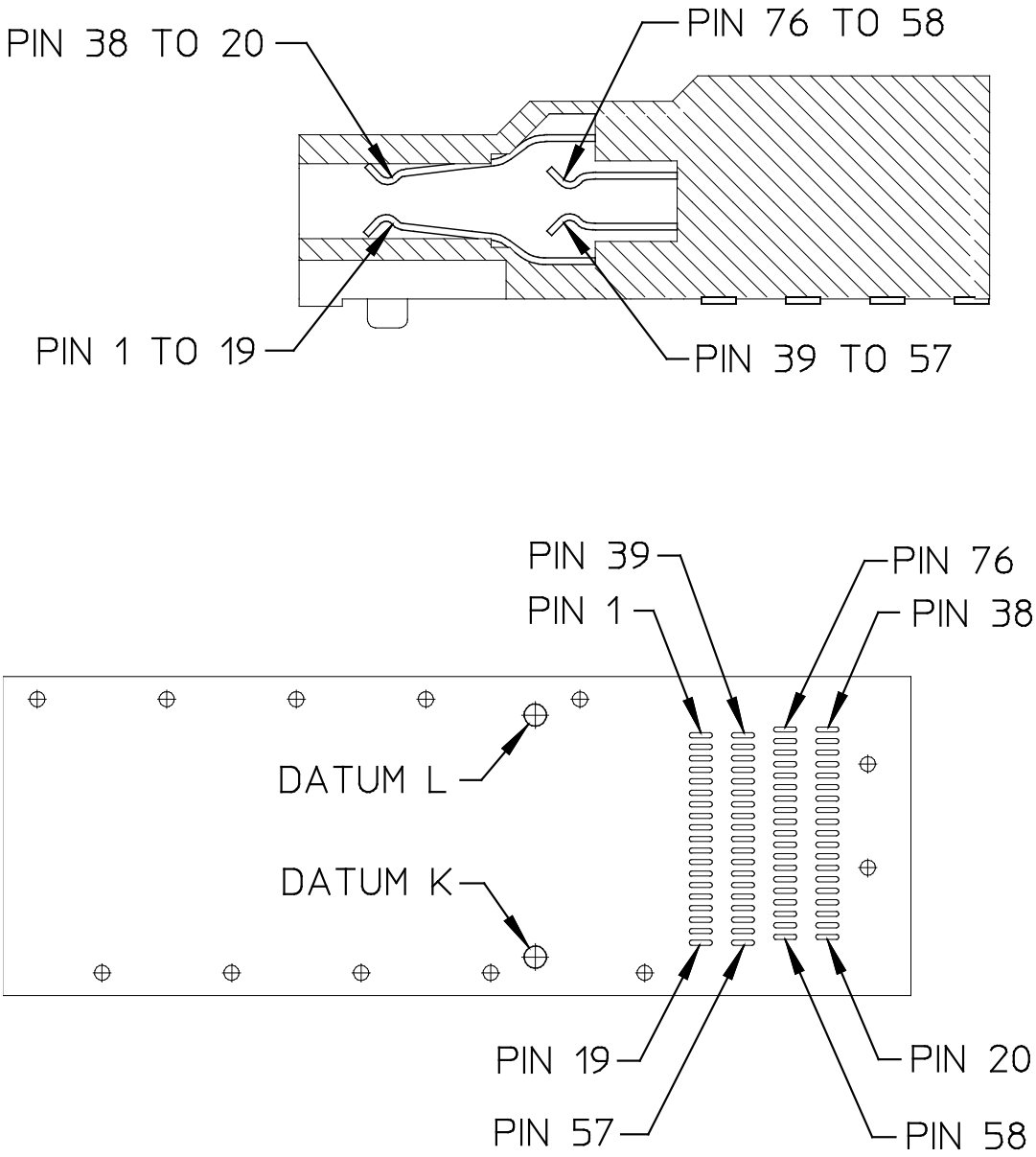


Figure 32: SMT Connector and Host PCB Pin Numbers

5.9 Module Color Coding and Labeling

An exposed feature of the QSFP-DD module (a feature or surface extending outside of the bezel) shall be color coded as follows:

Beige for 850nm
Blue for 1310nm
White for 1550nm

Each QSFP-DD module shall be clearly labeled. The complete labeling need not be visible when the QSFP-DD module is installed and the bottom of the device is the recommended location for the label. Labeling shall include:

Appropriate manufacturing and part number identification
Appropriate regulatory compliance labeling
A manufacturing traceability code

The label should also include clear specification of the external port characteristics such as:

Optical wavelength
Required fiber characteristics
Operating data rate
Interface standards supported
Link length supported
Connector Type

If required to comply with Section 6.1.1, a label must be applied to the top external surface of the module case, warning of high touch temperature.

The labeling shall not interfere with the mechanical, thermal or EMI features.

5.10 Optical Interface

The QSFP-DD optical interface port shall be either a male MPO receptacle (see Figure 34, Figure 35 and Figure 36), a dual LC (see Figure 37) or a CS connector (see Figure 38). The recommended location and numbering of the optical ports for each of the Media Dependent Interfaces is shown in Figure 33. The transmit and receive optical lanes shall occupy the positions depicted in Figure 33 when looking into the MDI receptacle with the connector keyway feature on top.

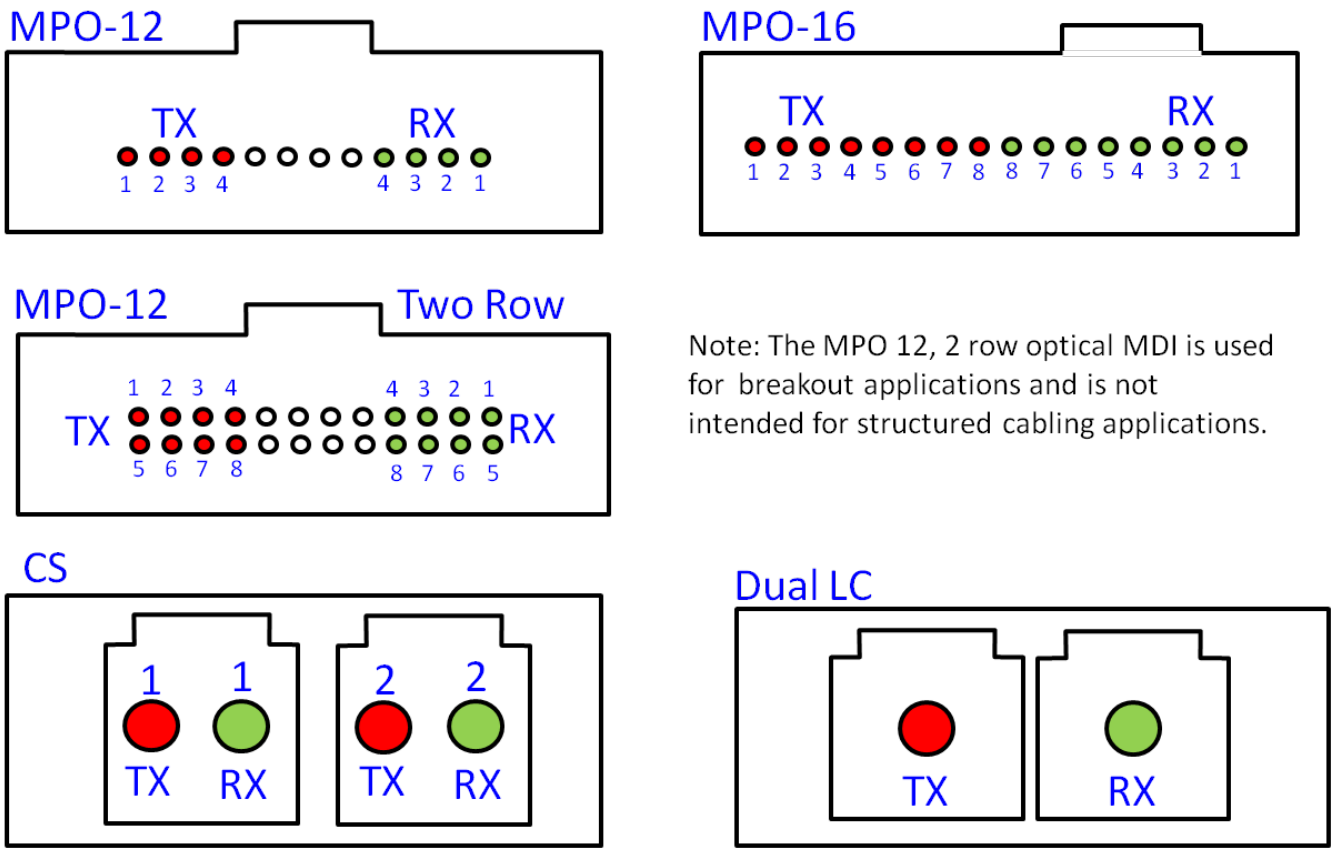


Figure 33: Optical Media Dependent Interface port assignments

5.10.1 MPO Optical Cable connections

The optical plug and receptacle for the MPO-12 connector is specified in TIA-604-5 and shown in Figure 34 (MPO-12 Single Row)and Figure 36 (MPO-12 Two Row). The optical plug and receptacle for the MPO-16 connector is specified in TIA-604-18 and shown in Figure 35 (MPO-16 Single Row). Note: This specification uses the terms MPO-12 in place of the TIA term MP0 and MPO-12 Two Row in place of the TIA term MPO Two Row.

Aligned keys are used to ensure alignment between the modules and the patchcords. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top. Note: Two alignment pins are present in each receptacle.

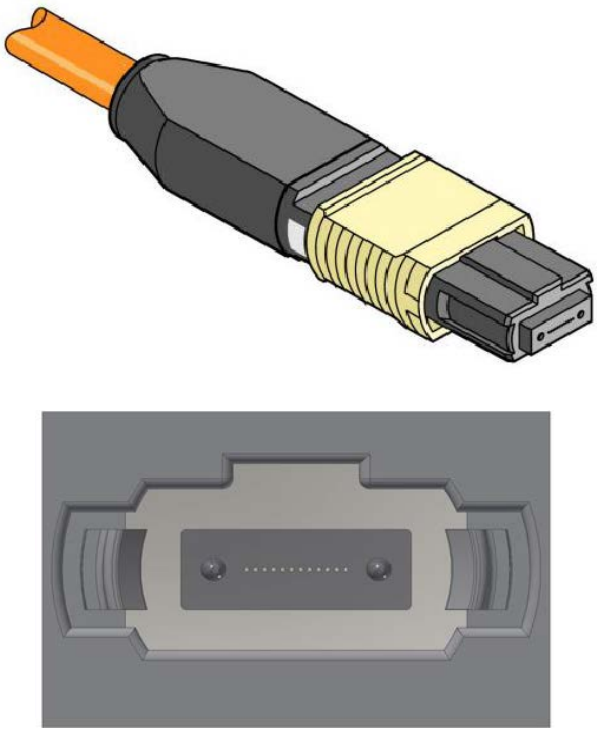


Figure 34: MPO-12 Single Row optical patch cord and module receptacle

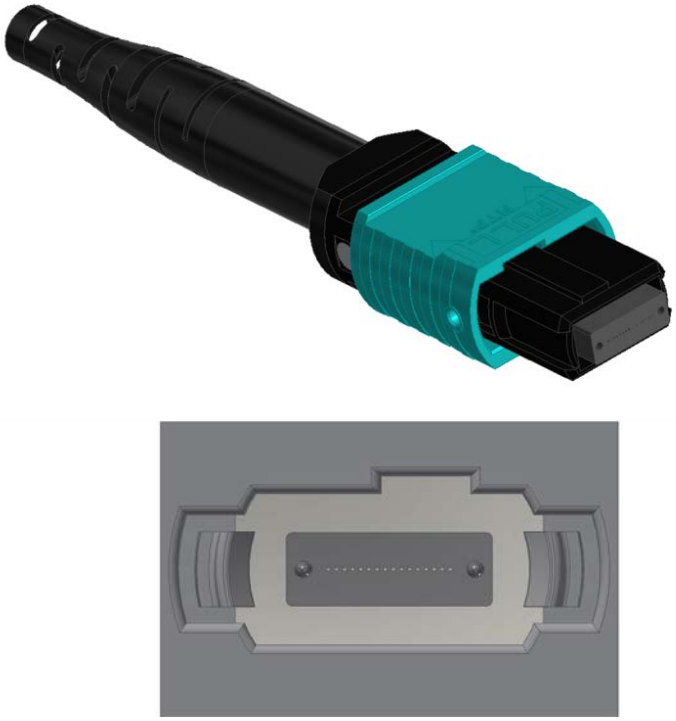


Figure 35: MPO-16 Single Row optical patchcord and module receptacle

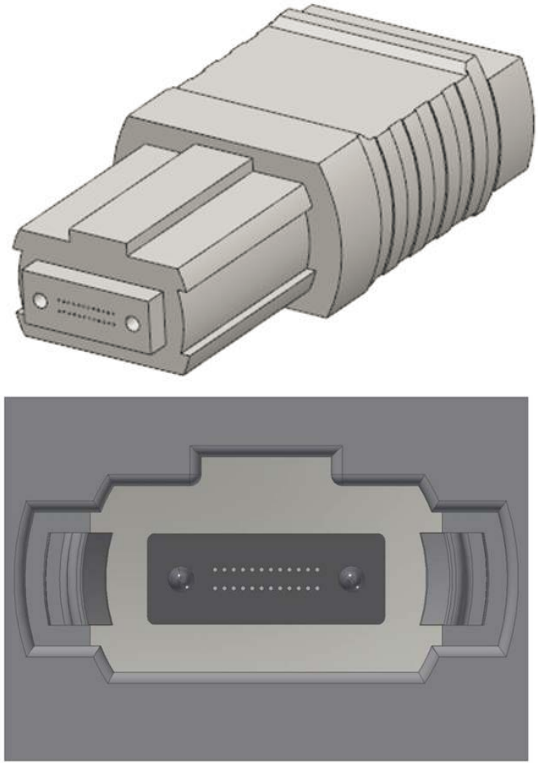


Figure 36: MPO-12 Two Row optical patchcord and module receptacle

5.10.2 Dual LC Optical Cable connection

The Dual LC optical patchcord and module receptacle is specified in TIA-604-10 and shown in Figure 37.

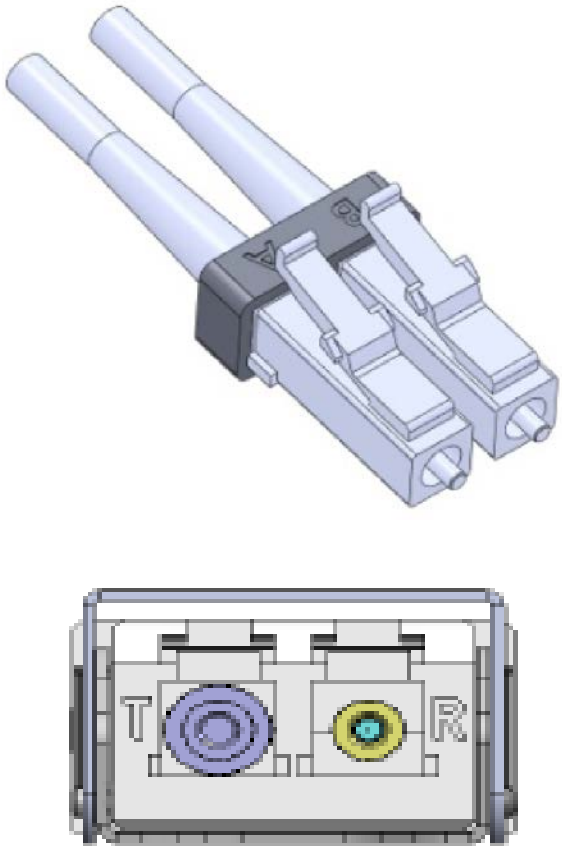


Figure 37: Dual LC optical patchcord and module receptacle

5.10.3 Dual CS Optical Cable connection

The Dual CS optical receptacle for a QSFP-DD module is specified in CS-01242017 (see Industry Documents) and shown in Figure 38.

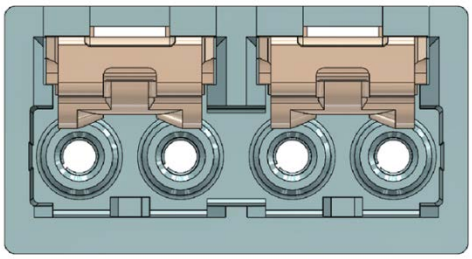


Figure 38: Dual CS connector module receptacle (in support of breakout applications)

5.10.4 Electrical data input/output to optical port mapping

Table 10 defines the mapping of electrical TX data inputs to optical ports. The mapping of the RX optical ports to electrical RX outputs is symmetric. Note that there is no defined mapping of electrical input/output to optical wavelengths for WDM applications.

Table 10- Electrical data input to Optical Port Mapping

Electrical Data Input Reference	Optical Port Type (see Figure 33)			
	LC	CS or MPO-12	MPO-12	MPO-12 (two row) MPO-16
	1 TX fiber[1]	2 Tx fibers[1]	4 Tx fibers[1]	8 Tx fibers[1]
Tx1	TX-1	TX-1	TX-1	TX-1
Tx2				TX-2
Tx3			TX-2	TX-3
Tx4				TX-4
Tx5		TX-2	TX-3	TX-5
Tx6				TX-6
Tx7			TX-4	TX-7
Tx8				TX-8
Note 1: Tx-n, where n is the optical port number as defined in Figure 33				

6 Environmental and Thermal

6.1 Thermal Requirements

The module shall operate within one or more of the case temperatures ranges defined in Table 11. The temperature ranges are applicable between 60m below sea level and 1800m above sea level, (Ref. NEBS GR-63) utilizing the host systems designed airflow.

Table 11- Temperature Range Class of operation

Class	**Case Temperature Range**
Standard	0°C through 70°C
Extended	-5°C through 85°C
Industrial	-40°C through 85°C

QSFP-DD is designed to allow for up to 36 modules; stacked, ganged and/or belly-to-belly in a 1U 19" rack, with the appropriate thermal design for cooling/airflow.

6.1.1 External Case and Handle Touch Temperature

For all power classes, all module case and handle surfaces outside of the cage must comply with applicable Touch Temperature requirements. If module case temperature will exceed applicable short-term touch temperature limits, a means must be provided to prevent contact with the case during unlatching and removal. See UL 60950-1 and NEBS GR63. Figure 10, Figure 11 and Appendix A: show typical handles used to unlatch and remove the module, thereby limiting contact with the module case. Handles are typically low thermal conductivity elastomer and allow a higher touch temperature.

7 Management Interface

A management interface, as already commonly used in other form factors like QSFP, SFP, and CDFP, is specified in order to enable flexible use of the module by the user. This QSFP-DD specification is based on SFF-8636 but with modifications to support an 8-channel module, and as such is not directly backwards compatible with SFF-8636. Some timing requirements are critical, especially for a multi-channel device, so the interface speed may optionally be increased. Byte 00 on the Lower Page or Address 128 Page 00 is used to indicate the use of the QSFP-DD memory map rather than the QSFP memory map. When a legacy QSFP28 module is inserted into a QSFP-DD port the legacy QSFP memory map (i.e. SFF-8636) must be used. This case is outside the scope of this document.

In some applications, muxing or demuxing may occur in the module. In this specification, all references to channel numbers are based on the electrical connector interface channels, unless otherwise indicated. In cases where a status or control aspect is applicable only to channels after muxing or demuxing has occurred, the status or control is intended to apply to all channels in the mux group, unless otherwise indicated.

7.1 SCL, SDA and ModSEL Timing Specification

7.1.1 Introduction

Low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to Vcc_host on the 2-wire interface SCL (clock) and SDA (Data) signals. Detailed electrical specifications are given in SFF-8679 Subsection 5.3. Nomenclature for all registers more than 1 bit long is MSB-LSB.

7.1.2 Management Interface Timing Specification

The timing requirements are shown in Figure 39 and specified in Table 12.
QSFP-DD is positioned to leverage 2-wire timing (Fast Mode devices) to align the use of related cores on host ASICs. The default clock rate is a maximum of 400 kHz with an option to support up to a maximum of 1 MHz. This subsection closely follows the QSFP SFF-8636 specification.

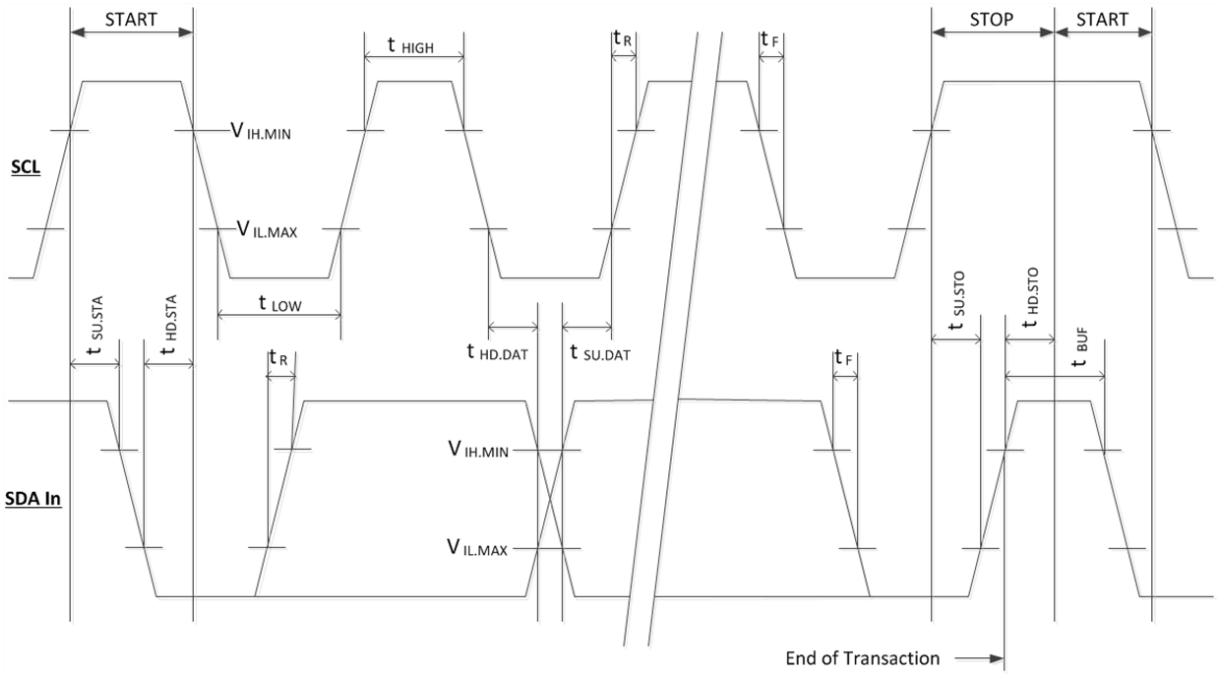


Figure 39: QSFP-DD Timing Diagram

The 2-wire serial interface address of the QSFP-DD module is 1010000X (A0h). In order to allow access to multiple QSFP-DD modules on the same 2-wire serial bus, the QSFP-DD includes a module select pad, ModSelL. This input (which is pulled high, deselected in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.
Before initiating a 2-wire serial bus communication, the host shall provide setup time on the ModSelL line of all modules on the 2-wire bus. The host shall not change the ModSelL line of any module until the 2-wire serial bus communication is complete and the hold time requirement is satisfied.

7.1.3 Serial Interface Protocol

7.1.3.1 Management Timing Parameters

The timing parameters for the 2-Wire interface to the QSFP-DD module and the QSFP-DD memory transaction timings are shown in Table 12. Tradeoffs between Pull up resistor values, bus capacitance and rise time are shown in Figure 40.

Table 12- Management Interface timing parameters

		Fast Mode (400 KHz)		Fast Mode Plus (1 MHz)			
Parameter	Symbol	Min	Max	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	0	1000	KHz	
Clock Pulse Width Low	tLOW	1.3		0.50		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		1		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	tR		300		120	ns	From (VIL,MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc)
Input Fall Time	tF		300		120	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.6		0.6		µs	
STOP Hold Time	tHD.STO	0.6		0.26		us	
Aborted sequence – bus release	Deselect _Abort	2		2		ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA
ModSelL Setup Time[1]	tSU.ModSelL	2		2		ms	ModSelL Setup Time is the setup time on the select lines before the start of a host initiated serial bus sequence.
ModSelL Hold Time[1]	tHD.ModSelL	2		2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module Select status.
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500		500	us	Maximum time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write	tWR		40		40	ms	Complete (up to) 4 Byte Write
Endurance (Write Cycles)		50K			50k	cycles	Module Case Temperature = 70^0 C

Note 1: When the host has determined that module is QSFP-DD, the management registers can be read to determine alternate supported ModSelL set up and hold times.

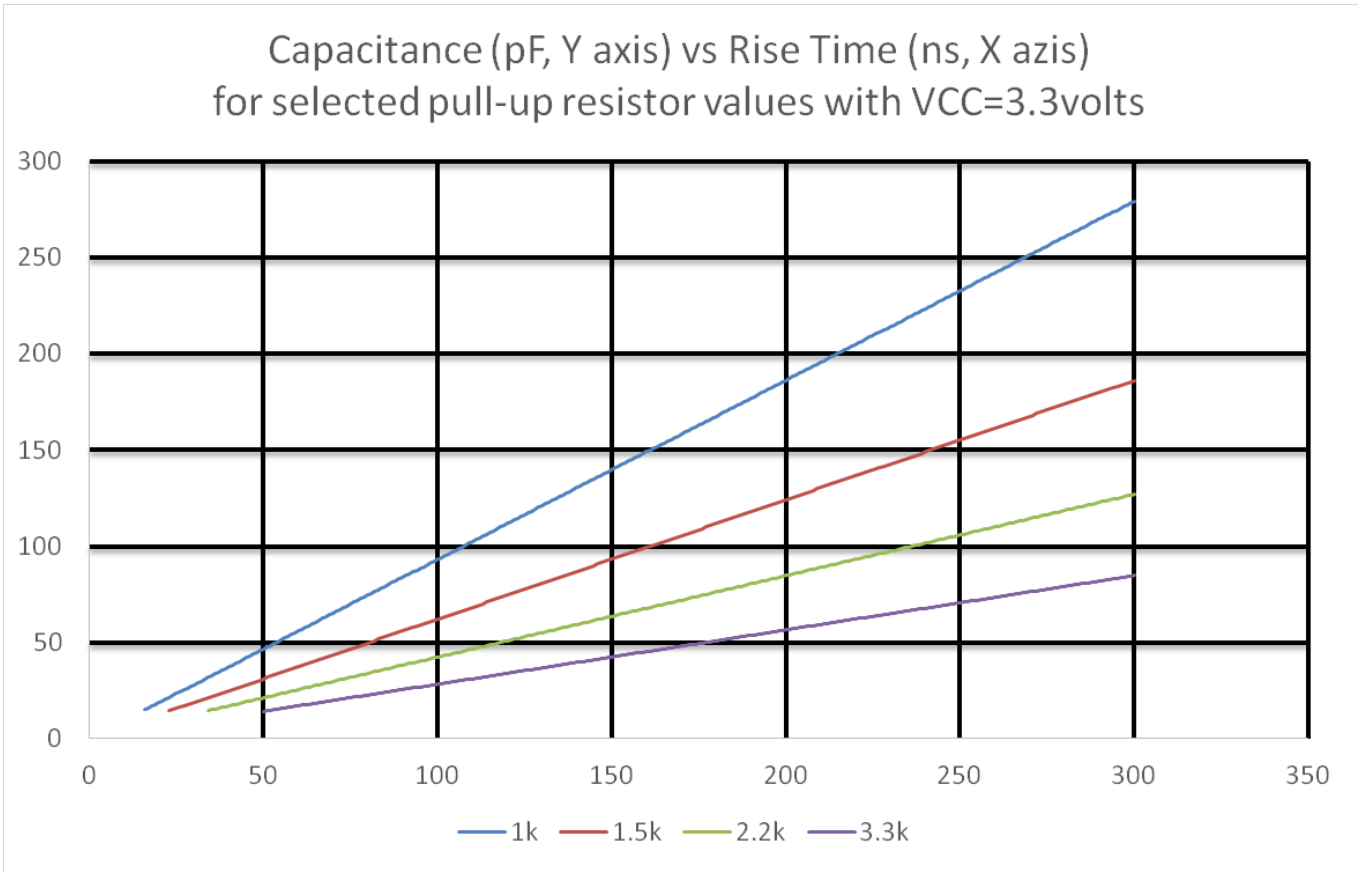


Figure 40: SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times

Appendix A: Informative overall module length with elastomeric handle attached to module latches

Figure 41 and Figure 42 show flexible elastomeric handles attached to the module latches. Handle ends for Types 1 and Type 2 modules should be aligned independent of module case extension. Type 1 modules should meet the overall length of 118mm maximum per Figure 41 with a handle length of approximately 50mm. Type 2 modules should comply with Figure 42 and have reduced handle length equal to the module case length extension

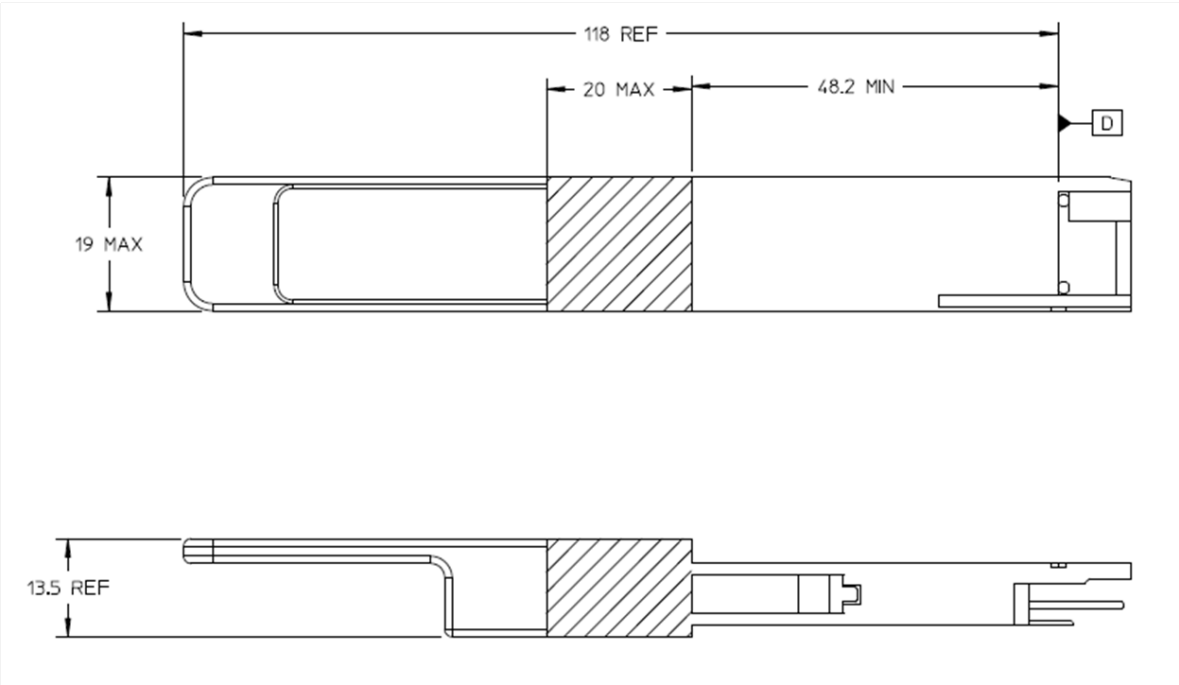


Figure 41: Informative overall module length with handle for Type 1 module

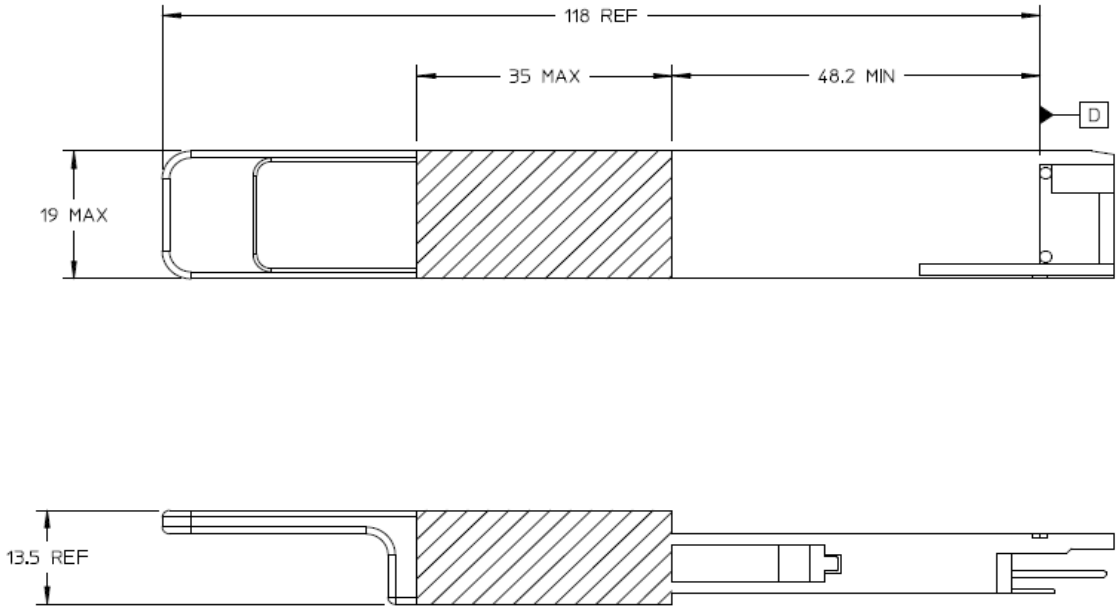


Figure 42: Informative overall module length with handle for Type 2 module

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