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PROVISIONAL APPLICATION FOR PATENT COVER SHEET – Page 1 of 2

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. _____

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
G. R. Mohan	Rao	Richardson, Texas

Additional inventors are being named on the _____ *separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max):

IMPROVED LIFETIME MIXED LEVEL NAND FLASH SYSTEM

Direct all correspondence to: CORRESPONDENCE ADDRESS

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ENCLOSED APPLICATION PARTS ***(check all that apply)***

☐ Application Data Sheet. See 37 CFR 1.76

☐ CD(s), Number of CDs _____

☒ Drawing(s) *Number of Sheets* 4

☐ Other (specify) _____

☒ Specification (e.g. description of the invention) *Number of Pages* 12

Fees Due: Filing Fee of $220 ($110 for small entity). If the specification and drawings exceed 100 sheets of paper, an application size fee is also due, which is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

METHOD OF PAYMENT OF THE FILING FEE AND APPLICATION SIZE FEE FOR THIS PROVISIONAL APPLICATION FOR PATENT

☒ Applicant claims small entity status. See 37 CFR 1.27.

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☐ Payment by credit card. Form PTO-2038 is attached

☒ The Director is hereby authorized to charge the filing fee and application size fee (if applicable) or credit any overpayment to Deposit Account Number: 50-4199.

110.00

TOTAL FEE AMOUNT ($)

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SIGNATURE /Konrad V. Sherinian/ Date July 19, 2011

TYPED or PRINTED NAME Konrad V. Sherinian REGISTRATION NO. 55,612 *(if appropriate)*

TELEPHONE 312-984-0144 Docket Number: 0299-0004

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IMPROVED LIFETIME MIXED LEVEL NAND FLASH SYSTEM

Inventor: G. R. Mohan Rao

CROSS REFERENCE TO RELATED APPLICATIONS

[001] This application incorporates by reference United States Patent Number 7,855,916 filed on October 22, 2008 by inventor G.R. Mohan Rao, and issued on December 21, 2010.

FIELD OF THE INVENTION

[002] The present invention relates to a system and method for providing reliable storage through the use of NAND FLASH, and more particularly to a system and method of increasing the reliability and lifetime of a NAND FLASH storage system, module, or chip through the use of a mixture of multi-level cell and single level cell NAND FLASH storage without substantially raising the cost of the NAND FLASH storage system. The memory in a total nonvolatile memory system may contain some DRAM (for buffering, caching, address table storage etc), NAND flash, and some HDD (hard disk drives) when storage of the order of terabytes is required.

DESCRIPTION OF THE PRIOR ART

[003] Non-volatile memories provide long-term storage of data. In the past, this has primarily been limited to storage of small programs, such as a computer BIOS, or to storage of small amounts of rarely changed data, such

as configuration information. However, process improvements now permit NAND FLASH to challenge the dominance of rotating magnetic media; i.e., hard disk drives. In particular, 4 Gbit (Billions-of-Bits) NAND FLASH chips are now common, with economical 16 Gbit and 32 Gbit chips quickly gaining market share. In fact, NAND FLASH is now used in a wide variety of applications, including portable storage, digital photography, cellular phones, and portable music players to name a few.

[004] NAND FLASH devices are generally fragmented into a number of identically sized blocks, each of which is further segmented into some number of pages. For example, a block may comprise 32 to 64 pages, each of which incorporates 2-4 KB of memory. In addition, the process of writing data to a NAND FLASH is complicated by the fact that, during normal operation, erased bits, which are usually all bits in a block with the value of '1', can only be changed to the opposite state, which is usually '0', once before the entire block must be erased. Blocks can only be erased in their entirety, and, when erased, are usually written to '1' bits.

[005] The vast majority of NAND FLASH in enterprise servers utilizes a single level cell (SLC) architecture. However, multi-level cell (MLC) FLASH is gaining in popularity. MLC allows a single cell to store multiple bits, and accordingly, to assume more than two values; i.e., '0' or '1'. Most MLC NAND FLASH architectures allow up to 4 values per cell; i.e., '00', '01', '10', or '11'. Generally, MLC NAND FLASH enjoys greater density than SLC NAND FLASH, at the cost of a decrease in access speed and lifetime. It should be noted, however, that even SLC NAND FLASH has a considerably lower lifetime than

rotating magnetic media, being able to withstand only between 50,000 and 100,000 writes, and MLC NAND FLASH has a much lower lifetime than SLC NAND FLASH, being able to withstand between 3,000 and 10,000 writes. As is well known in the art, a write or program, in NAND flash (floating gate) requires an erase before write.

[006] Despite its limitations, there are a number of applications that lend themselves to the use of MLC FLASH. Generally, applications where data is read many times but written few times and physical size is an issue are good candidates for the use of MLC FLASH. For example, FLASH cards for use in digital cameras would be a good application of MLC FLASH, as MLC can provide higher density memory at lower cost than SLC memory.

[007] Given the limited number of writes that individual blocks within FLASH devices can tolerate, wear leveling algorithms are used within the FLASH devices (sometimes as firmware commonly known as FTL, flash translation layer; and, in other times managed by a controller) to attempt to ensure that hot blocks; i.e., those that are frequently written, are not rendered unusable much faster than other blocks. This task is usually performed within a flash translation layer, which is a logical function embedded within a FLASH device that abstracts the complexity of accessing memory locations within the FLASH device. In particular, as a FLASH device does not support overwriting individual pages, an FTL maps individual pages of FLASH memory to a particular block, and performs the function of mapping logical pages to physical FLASH pages, and erase blocks.

OBJECTS OF THE INVENTION

[008] Accordingly, an objective of the invention is to provide a NAND FLASH storage system that provides long lifetime storage at low cost;

[009] Other advantages of the disclosed invention will be clear to a person of ordinary skill in the art. It should be understood, however, that a system, method, or apparatus could practice the disclosed invention while not achieving all of the enumerated advantages, and that the protected invention is defined by the claims.

SUMMARY OF THE INVENTION

[0010] A system for storing data comprises at least one MLC NAND FLASH module and at least one SLC NAND FLASH module, each of which comprises a plurality of individually erasable blocks. A controller controls both the at least one MLC NAND FLASH module and the at least one SLC NAND FLASH module. In particular, the controller maintains a table listing individual logical address ranges each of which maps to a similar range of physical addresses within either the at least one MLC NAND FLASH module or the at least one SLC NAND FLASH module. After each write to FLASH memory, the controller conducts a data integrity check to ensure that the data was written correctly. When the data is not written correctly, the controller modifies the table so that the range of addresses on which the write failed is remapped to the next available range of physical addresses within the at least one SLC NAND FLASH module.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Although the characteristic features of this invention will be particularly pointed out in the claims, the invention itself, and the manner in which it may be made and used, may be better understood by referring to the following description taken in connection with the accompanying drawings forming a part hereof, wherein like reference numerals refer to like parts throughout the several views and in which:

[0012] FIG. 1 is a block diagram of a computer system incorporating one aspect of the disclosed invention;

[0013] FIG. 2 is a drawing depicting an address map that implements an aspect of the disclosed invention;

[0014] FIGS. 3a and 3b are a flow chart illustrating a method for use in implementing an aspect of the disclosed invention; and

[0015] FIG. 4 is a block diagram depicting an embodiment of the invention for implementation within a NAND FLASH module.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

[0016] The present invention relates to the reliable storage of data in read and write memories, and, in particular, to the reliable storage of data in NAND FLASH. Generally, two separate banks of NAND FLASH are maintained by a controller. One bank contains economical MLC NAND FLASH, while a second bank contains high endurance SLC NAND FLASH. The controller conducts a data integrity test after every write. If a particular address range fails a data integrity test, the address range is remapped from an MLC NAND FLASH device to a SLC NAND FLASH device. As the SLC NAND FLASH is used to boost the lifetime of the storage system, it can be considerably lesser in

amount than the MLC NAND FLASH. For example, a system may set SLC NAND FLASH equal to 12.5% or 25% of MLC NAND FLASH.

[0017] Turning to the Figures, and to Figure 1 in particular, a computer system 10 depicting the disclosed invention is shown. A processor 12 is coupled to a device controller 14, such as a chipset, using a prior art link, such as a parallel bus or packet-based link. The device controller 14 provides interface functions to the processor 12, and may be included in the processor 12, or not present at all in certain computer systems. The device controller 14 provides a number of input / output ports 16,18, such as, for example, serial ports, such as USB ports and Firewire ports, and network ports, such as, for example, Ethernet ports and 802.11 ("Wi-Fi") ports. The device controller 14 also controls a bank of DRAM 20. In addition, the device controller 14 controls access to one or more disks 24, such as, for example, a rotating magnetic disk, or an optical disk, as well as two or more types of NAND FLASH memory. One type of NAND FLASH memory is a pool of MLC NAND FLASH memory 26. Another type of NAND FLASH memory is a pool of SLC NAND FLASH memory 28.

[0018] The device controller 14 maintains a translation table which may include address translations for all devices in the computer system. Nonetheless, we will limit our discussion to here to the pools of NAND FLASH memory. In particular, the controller maintains a translation table that maps logical computer system addresses to physical addresses in one of the pools of NAND FLASH memory. As MLC memory is less expensive than SLC memory, on a cost per bit basis, the translation table will initially map all logical NAND FLASH addresses to the MLC FLASH memory pool 26. The address ranges within the

translation table will assume some minimum quantum, such as, for example, one block, although a smaller size, such as a page could be used, if the NAND FLASH has the capability of erasing the smaller size.

[0019] A read-modify-write scheme is used to write data to the NAND FLASH. Data to be written to NAND FLASH is maintained in DRAM 20. After each write to an address within a particular address range, the controller will, as time permits, perform a read on the address range to ensure the integrity of the written data. If a data integrity test fails, the address range is remapped from the MLC FLASH memory pool 26 to the next available address range in the SLC FLASH memory pool 28.

[0020] Figure 2 illustrates one possible embodiment of this translation table. In Figure 2a, a list of logical address ranges is translated to physical addresses. As illustrated, all of the logical address ranges are translated to the MLC NAND FLASH pool. However, via a data integrity verification check, such as the one explained later, it is determined that address range R2 corresponds to a failed quanta of data stored in the MLC NAND FLASH pool. Figure 2b shows the quanta of data which failed a data integrity verification check remapped to the next available range of physical addresses within the SLC NAND FLASH pool.

[0021] Figures 3s and 3b are a flow chart illustrating a method for utilizing a NAND FLASH memory system incorporating an aspect of the disclosed invention. The method begins in a step 102, when a command to write a quantum of data stored in DRAM to a particular location in NAND FLASH memory is received. In step 104, the quantum of data is read from DRAM into memory within the device controller (which acts as the memory controller). In

step 106, the logical address range encompassing the NAND FLASH address range to be written is read into device controller memory. In step 108, the quantum of data to be written to NAND FLASH is combined with the present contents of the entire address range that the data will be written to. In step 109, the NAND FLASH address range to be written is erased. In step 110, the combined data is written to the appropriate NAND FLASH logical range.

[0022] In step 112 the NAND FLASH logical range that was written in step 110 is read into device controller memory. This is compared with the retained data representing the combination of the previous contents of the logical address range and the quantum of data to be written. If the retained data matches the newly stored data in the NAND FLASH memory, the write was a success, and the method exits in step 118. However, if the retained data does not match the newly stored data in the NAND FLASH memory, the method executes step 120, which identifies the next quantum of available SLC NAND FLASH memory addresses. In step 122, a check is made to determine if additional SLC NAND FLASH memory is available, and, if not, the NAND FLASH memory system is marked as failed, and an alert is raised. However, if additional SLC NAND FLASH memory is available, the next available quantum of SLC NAND FLASH memory is remapped to the logical address range that had been mapped to the failed NAND FLASH. Execution then returns to step 110, where the write is repeated.

[0023] Another use of this invention would be segregate hot blocks; i.e., those that are changed the most, to the pool of SLC NAND FLASH memory, while segregating cold blocks; i.e., those that are written rarely, to the pool of MLC

NAND FLASH memory. This could be accomplished within the device controller 14 described above, which could simply maintain a count of those blocks that are accessed to the most, and, on a periodic basis, such as, for example, 1000 writes, or 10,000 writes, transfer the contents of those blocks to SLC memory.

[0024] Figure 4 depicts an additional embodiment of the disclosed invention. The embodiment is entirely resident within NAND FLASH module 50. In particular, a standard NAND FLASH interface 52 is managed by flash translation layer logic 54. The flash translation layer 54 oversees two planes of NAND FLASH memory 56,58, each of which comprises a pool of MLC NAND FLASH memory 60a,60b and a pool of SLC FLASH memory 62a,62b.

[0025] This embodiment could function similarly to the system level embodiment discussed earlier, but the control functions, such as maintenance of the translation table, could be conducted within the flash translation layer 54 instead of in a device controller.

[0026] Many modifications and variations of the present invention are possible in light of the above teachings. Thus, it is to be understood that, within the scope of the appended claims, the invention may be practiced otherwise than is specifically described above. The foregoing description of the invention has been presented for purposes of illustration and description, and is not intended to be exhaustive or to limit the invention to the precise form disclosed. The description was selected to best explain the principles of the invention and practical application of these principles to enable others skilled in the art to best utilize the invention in various embodiments and various modifications as

are suited to the particular use contemplated. It is intended that the scope of the invention not be limited by the specification, but be defined by the claims set forth below.

Claims

What is claimed is:

[C1] 1. A system for storing data comprising:

i) at least one MLC NAND FLASH memory pool comprising a plurality of blocks;

ii) at least one SLC NAND FLASH memory pool comprising a plurality of blocks; and

iii) a controller coupled to said at least one MLC NAND FLASH memory pool and said at least one SLC NAND FLASH memory pool, said controller maintaining an address map of a pool of NAND FLASH MEMORY, said pool comprising a list of logical address ranges accessible by a computer system, said list of logical address ranges having a minimum quanta of addresses, wherein each entry in said list of logical address ranges maps to either said at least one SLC NAND FLASH memory pool or to said at least one MLC NAND FLASH memory pool;

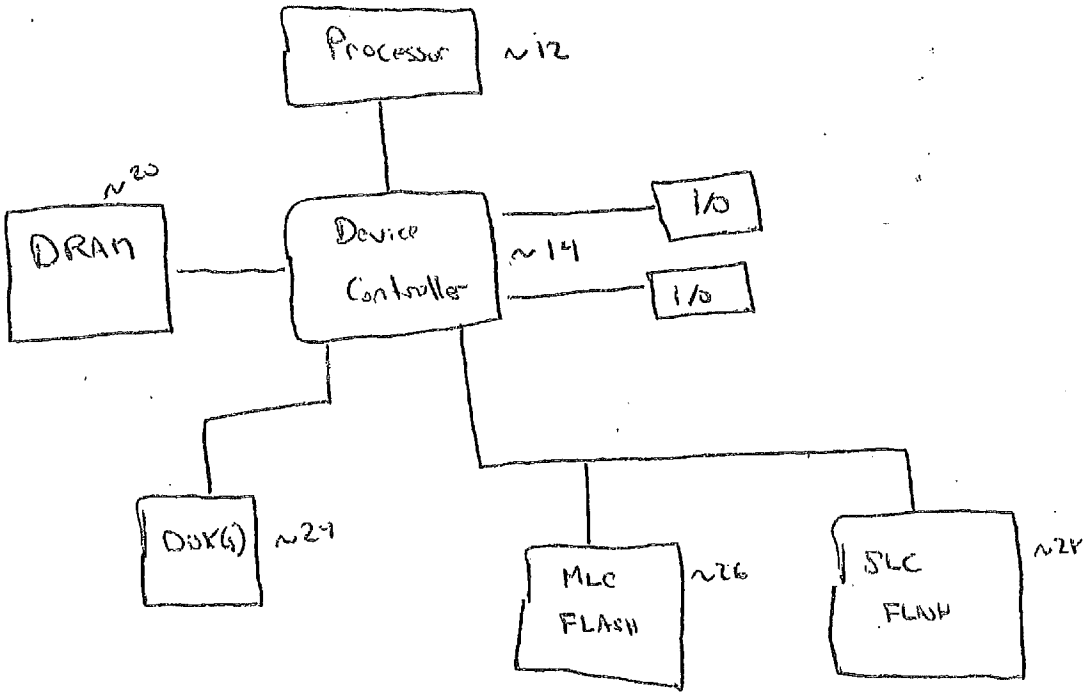
iv) wherein said controller is adapted to determine if a range of addresses listed by an entry and mapped to said at least one MLC NAND FLASH memory pool fails a data integrity test, and, in the event of such a failure, remaps said entry to an equivalent range of addresses of said at least one SLC NAND FLASH memory pool.

[C2] 2. The system of claim 1 wherein said minimal quanta of addresses is equal to one block.

ABSTRACT

[0027] A flash controller manages a pool of NAND FLASH memory including at least one MLC NAND FLASH module and at least one SLC NAND FLASH module. If a write to a logical address range mapped to physical addresses within an MLC NAND FLASH module fails, that range is remapped to physical addresses within an SLC NAND FLASH module.

FIG. 1



Logical Range	Physical Range
R0	MLC / Block 0
R1	MLC / Block 1
R2	MLC / Block 2
R3	MLC / Block 3
R4	MLC / Block 4
RN	MLC / Block N

Failed Data Integrity Test

Logical Range	Physical Range
R0	MLC / Block 0
R1	MLC / Block 1
R2	SLC / Block 0
R3	MLC / Block 3
R4	MLC / Block 4
RN	MLC / Block N

FIG. 2

FIG. 3a

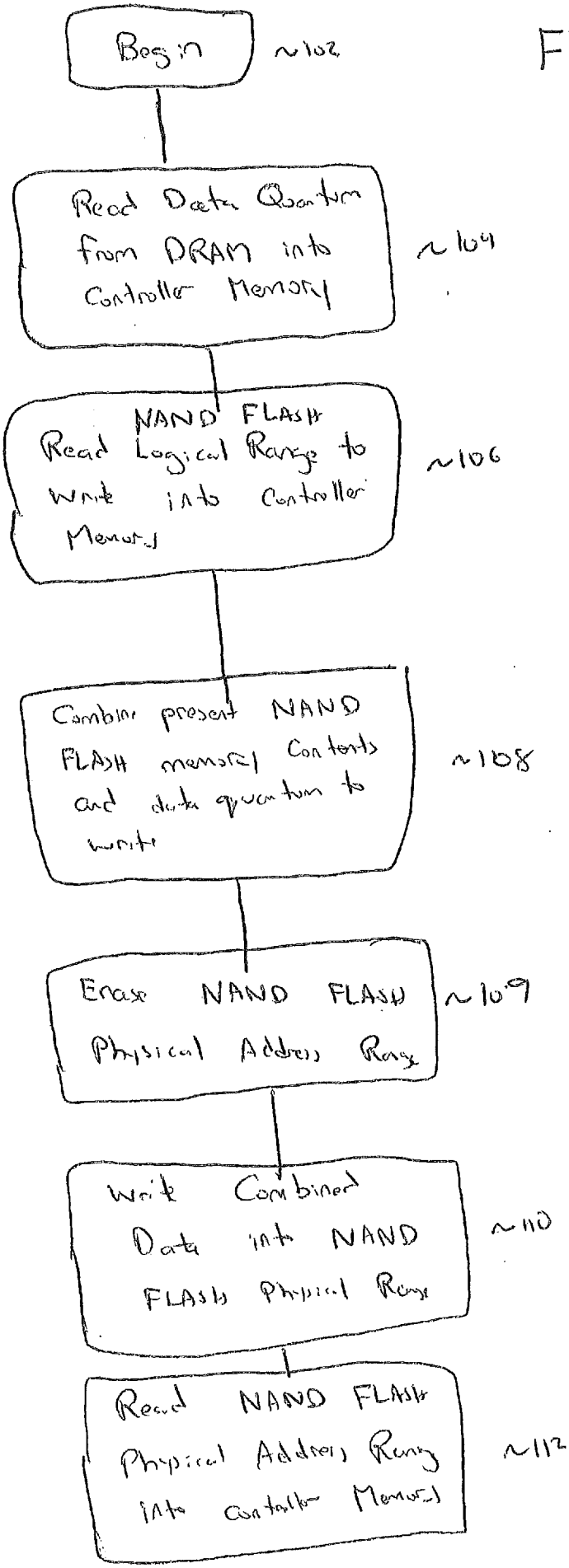
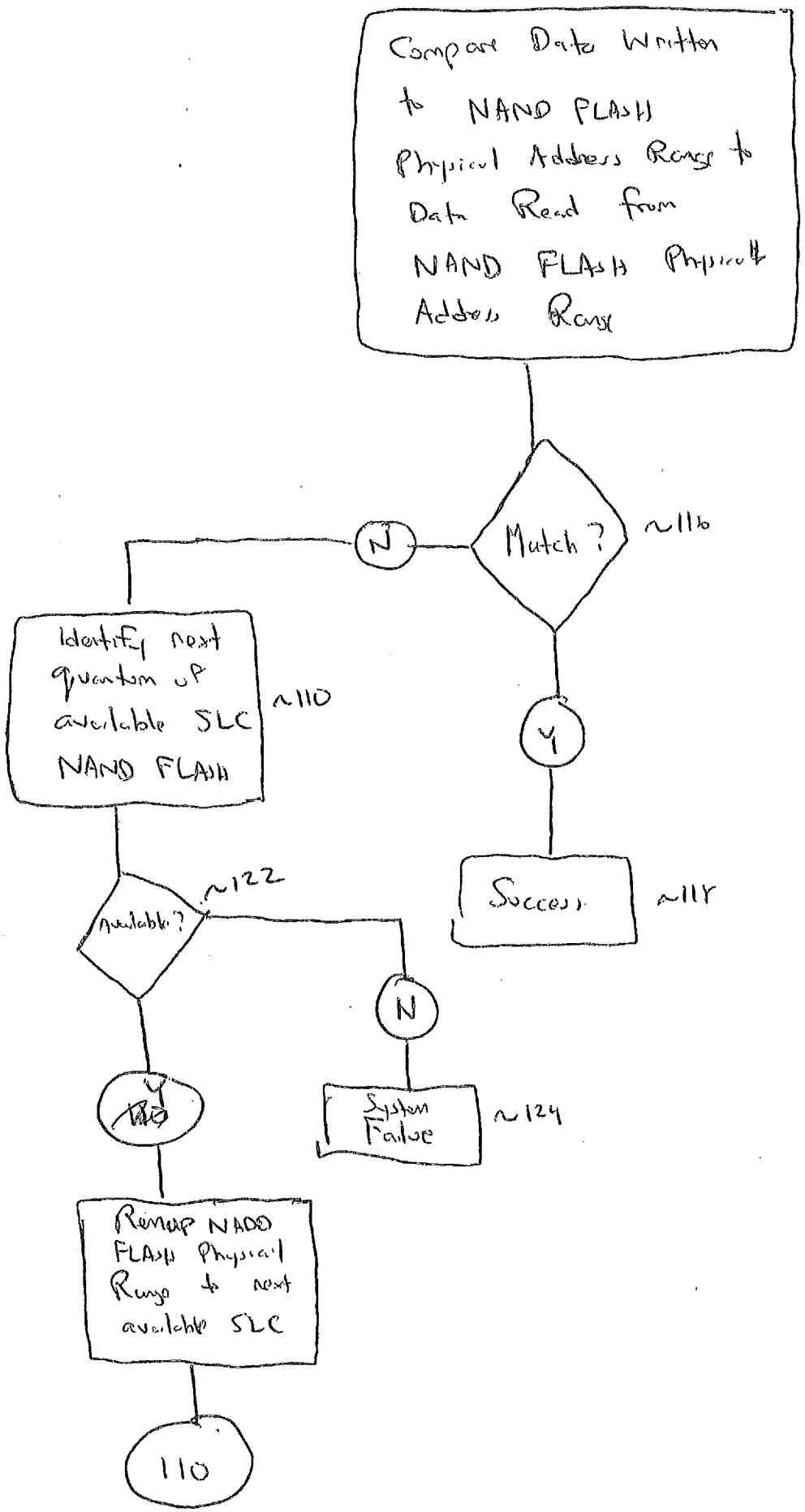
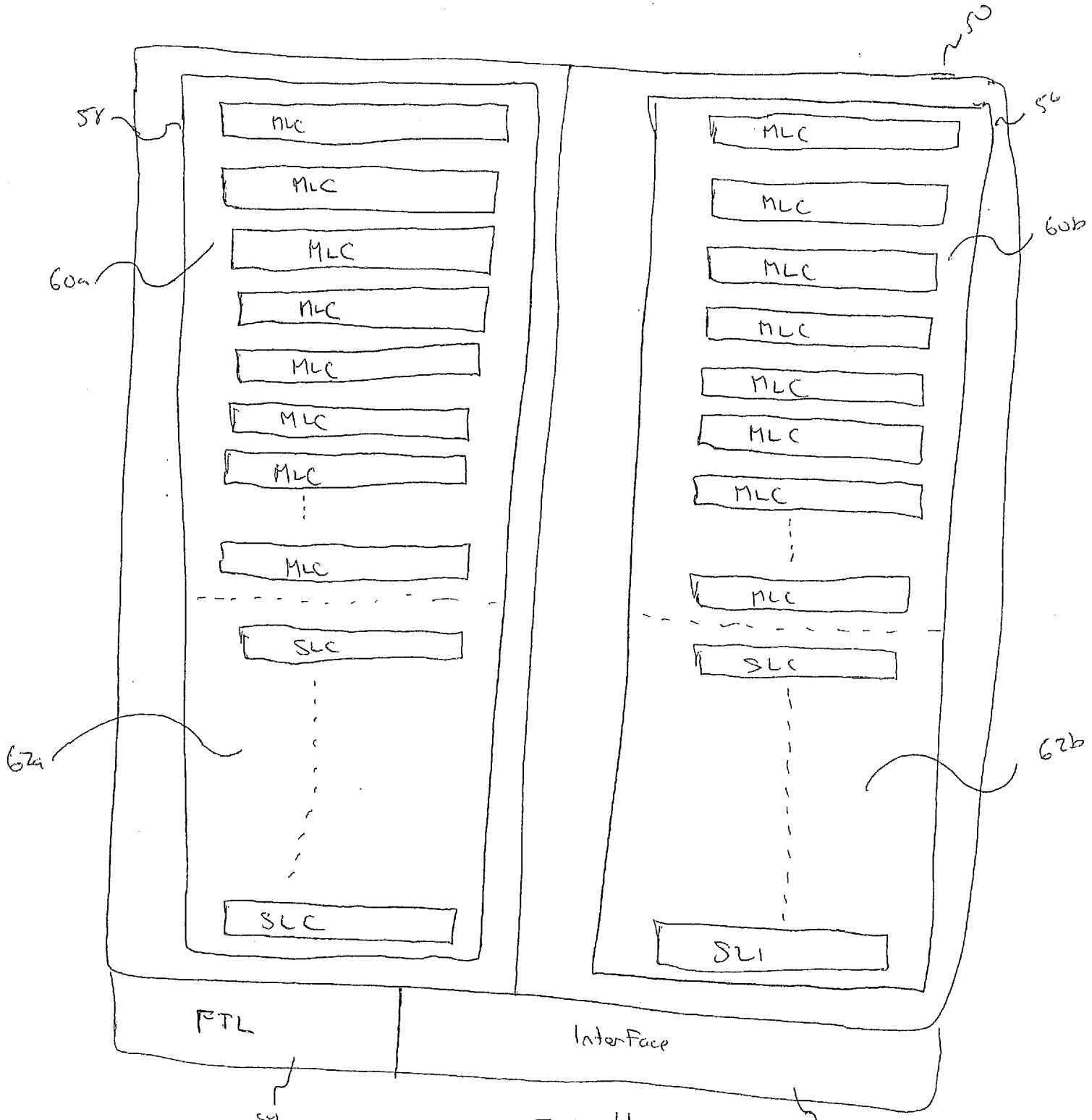

Begin
~102
Read Data Quantum from DRAM into Controller Memory
~104
Read NAND FLASH Logical Range to write into Controller Memory
~106
Combine present NAND FLASH memory contents and data quantum to write
~108
Erase NAND FLASH Physical Address Range
~109
Write Combined Data into NAND FLASH Physical Range
~110
Read NAND FLASH Physical Address Range into Controller Memory
~112

FIG. 3b


Compare Data Written to NAND FLASH Physical Address Range to Data Read from NAND FLASH Physical Address Range
~114
Match ?
~116
N
Y
Identify next quantum of available SLC NAND FLASH
~110
Success
~118
Available ?
~122
N
Y
System Failure
~124
Remap NAND FLASH Physical Range to next available SLC
110


50
58
56
MLC
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MLC
MLC
MLC
MLC
60a
60b
SLC
SLC
SLC
SLC
62a
62b
FTL
Interface
54
52

FIG. 4

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	IMPROVED LIFETIME MIXED LEVEL NAND FLASH SYSTEM
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Filer:	Konrad Val Sherinian/Francisca Hubbard
Attorney Docket Number:	0299-0004

Filed as Small Entity

Provisional Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
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Provisional Application filing fee	2005	1	110	110
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Claims:				
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Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**110**

Electronic Acknowledgement Receipt

EFS ID:	10550654
Application Number:	61509257
International Application Number:	
Confirmation Number:	3039
Title of Invention:	IMPROVED LIFETIME MIXED LEVEL NAND FLASH SYSTEM
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	70653
Filer:	Konrad Val Sherinian/Francisca Hubbard
Filer Authorized By:	Konrad Val Sherinian
Attorney Docket Number:	0299-0004
Receipt Date:	19-JUL-2011
Filing Date:	
Time Stamp:	14:45:11
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$110
RAM confirmation Number	1054
Deposit Account	504199
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Provisional Cover Sheet (SB16)	ProvCvrSht.pdf	317870 810da49f816c703eab25edca524e2e20e4194d5b	no	2
Warnings:					
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Information:					
2		Specification.pdf	1410808 fd9b0ab4a0c1bc5dc34aaa7f9c53cf96828847be	yes	12
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	10	
	Claims		11	11	
	Abstract		12	12	
Warnings:					
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3	Drawings-only black and white line drawings	Drawings.pdf	354255 080eb719f6d13e8b28ac1ba514dd79d106ab30c7	no	4
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	29592 e8d5656597675eca91aa3069022edc8353a74969	no	2
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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
61/509,257	07/19/2011		110	0299-0004		

CONFIRMATION NO. 3039

FILING RECEIPT

OC000000048999897

70653
LAW OFFICES OF EUGENE M. CUMMINGS, P.C.
ONE NORTH WACKER DRIVE
SUITE 4130
CHICAGO, IL 60606

Date Mailed: 07/29/2011

Receipt is acknowledged of this provisional patent application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

G.R. Mohan Rao, Richardson, TX;

Power of Attorney:
Konrad Sherinian--55612

If Required, Foreign Filing License Granted: 07/27/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/509,257**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

LIFETIME MIXED LEVEL NAND FLASH SYSTEM

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international

patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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