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Rao

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(54) **NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES**

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This patent is subject to a terminal disclaimer.

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Related U.S. Application Data

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(60) Provisional application No. 60/982,175, filed on Oct. 24, 2007.

(51) **Int. Cl.**

G11C 11/34	(2006.01)
G11C 16/04	(2006.01)
G06F 9/26	(2006.01)

(52) **U.S. Cl.** **365/185.08**; 365/185.11; 365/185.12; 365/185.17; 711/202

(58) **Field of Classification Search** 365/185.08, 365/185.11, 185.12, 185.17; 711/202

See application file for complete search history.

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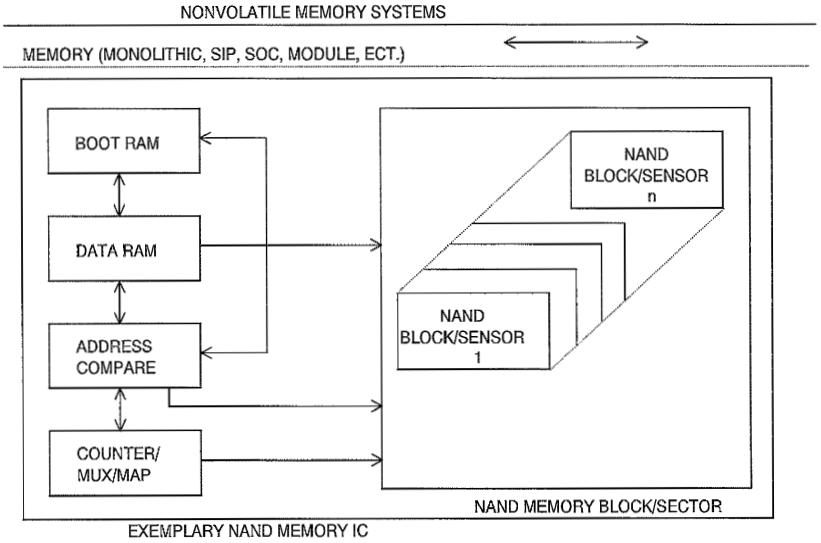
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(57) **ABSTRACT**

A nonvolatile memory system is described with novel architecture coupling nonvolatile storage memory with random access volatile memory. New commands are included to enhance the read and write performance of the memory system.

10 Claims, 12 Drawing Sheets



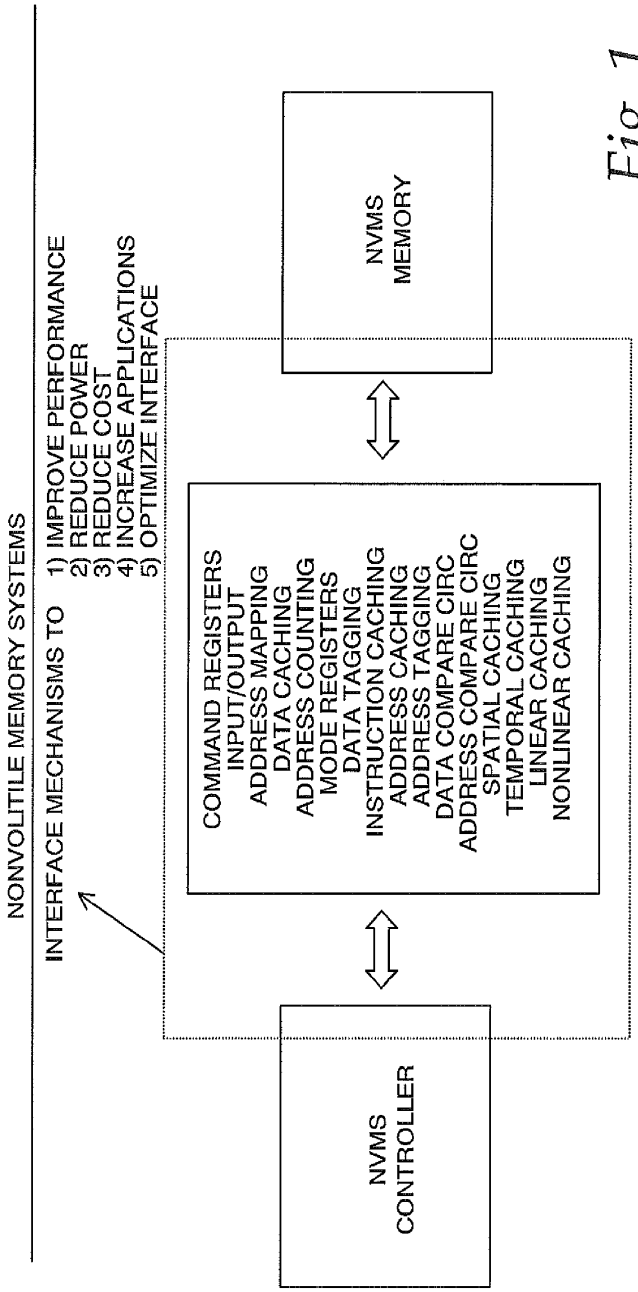
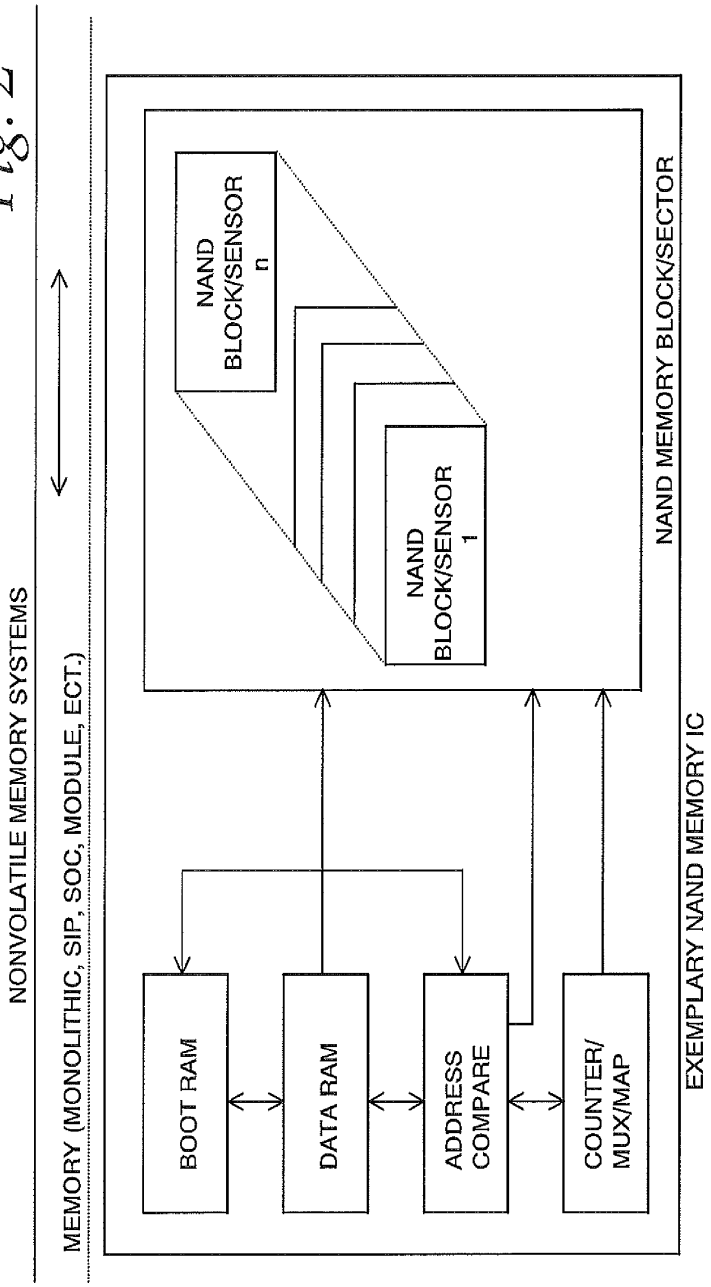

NONVOLITILE MEMORY SYSTEMS
INTERFACE MECHANISMS TO
1) IMPROVE PERFORMANCE
2) REDUCE POWER
3) REDUCE COST
4) INCREASE APPLICATIONS
5) OPTIMIZE INTERFACE
NVMS CONTROLLER
COMMAND REGISTERS
INPUT/OUTPUT
ADDRESS MAPPING
DATA CACHING
ADDRESS COUNTING
MODE REGISTERS
DATA TAGGING
INSTRUCTION CACHING
ADDRESS CACHING
ADDRESS TAGGING
DATA COMPARE CIRC
ADDRESS COMPARE CIRC
SPATIAL CACHING
TEMPORAL CACHING
LINEAR CACHING
NONLINEAR CACHING
NVMS MEMORY

Fig. 1

Fig. 2


NONVOLATILE MEMORY SYSTEMS
MEMORY (MONOLITHIC, SIP, SOC, MODULE, ECT.)
EXEMPLARY NAND MEMORY IC
NAND MEMORY BLOCK/SECTOR
NAND BLOCK/SENSOR n
NAND BLOCK/SENSOR 1
BOOT RAM
DATA RAM
ADDRESS COMPARE
COUNTER/ MUX/MAP

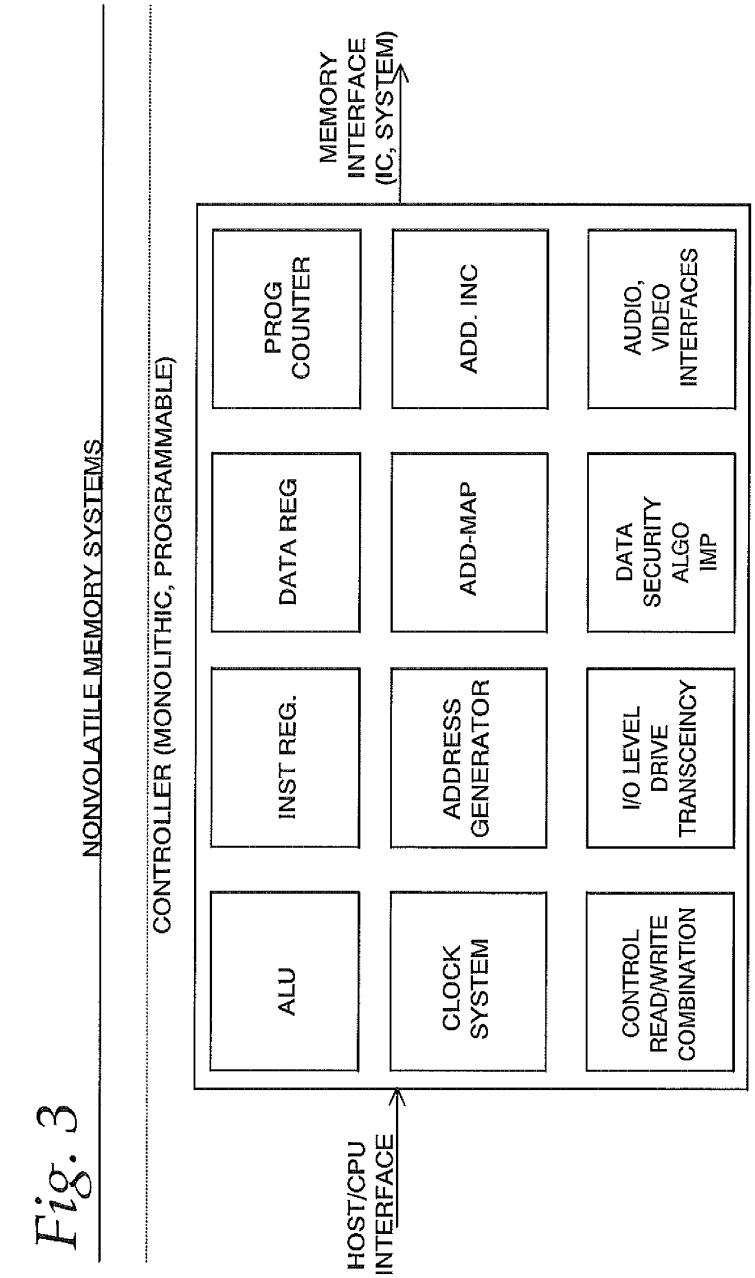

NONVOLATILE MEMORY SYSTEMS
CONTROLLER (MONOLITHIC, PROGRAMMABLE)
HOST/CPU INTERFACE
MEMORY INTERFACE (IC, SYSTEM)
ALU
INST REG.
DATA REG
PROG COUNTER
CLOCK SYSTEM
ADDRESS GENERATOR
ADD-MAP
ADD. INC
CONTROL READ/WRITE COMBINATION
I/O LEVEL DRIVE TRANSCEINCY
DATA SECURITY ALGO IMP
AUDIO, VIDEO INTERFACES

Fig. 3

Fig. 4

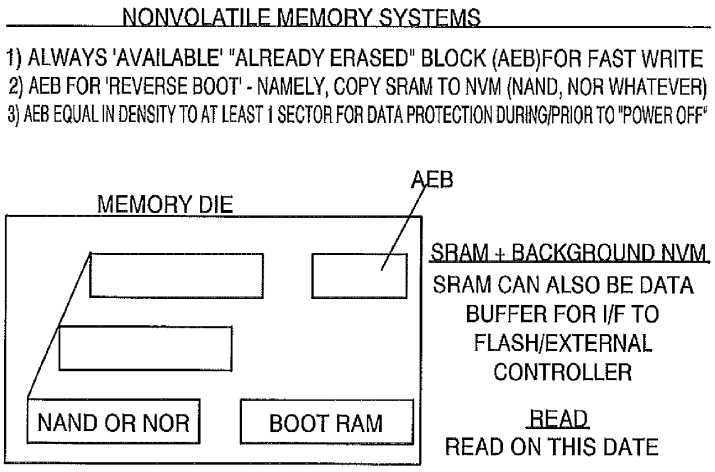
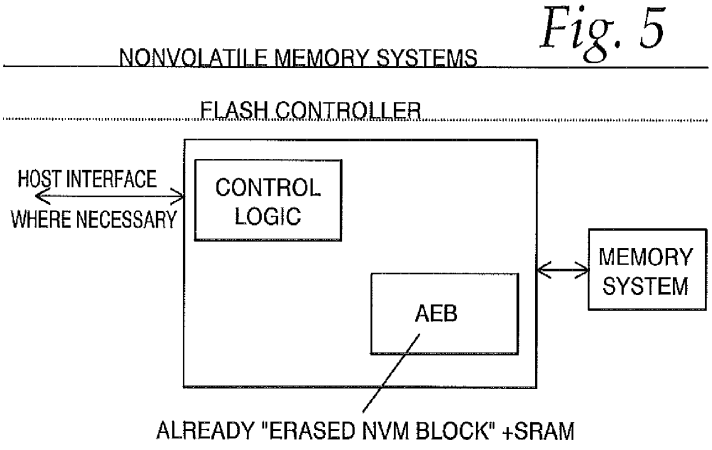

NONVOLATILE MEMORY SYSTEMS
1) ALWAYS 'AVAILABLE' "ALREADY ERASED" BLOCK (AEB)FOR FAST WRITE
2) AEB FOR 'REVERSE BOOT' - NAMELY, COPY SRAM TO NVM (NAND, NOR WHATEVER)
3) AEB EQUAL IN DENSITY TO AT LEAST 1 SECTOR FOR DATA PROTECTION DURING/PRIOR TO "POWER OFF"
AEB
MEMORY DIE
SRAM + BACKGROUND NVM
SRAM CAN ALSO BE DATA BUFFER FOR I/F TO FLASH/EXTERNAL CONTROLLER
NAND OR NOR
BOOT RAM
READ
READ ON THIS DATE

Fig. 5


NONVOLATILE MEMORY SYSTEMS
FLASH CONTROLLER
HOST INTERFACE
WHERE NECESSARY
CONTROL LOGIC
MEMORY SYSTEM
AEB
ALREADY "ERASED NVM BLOCK" +SRAM

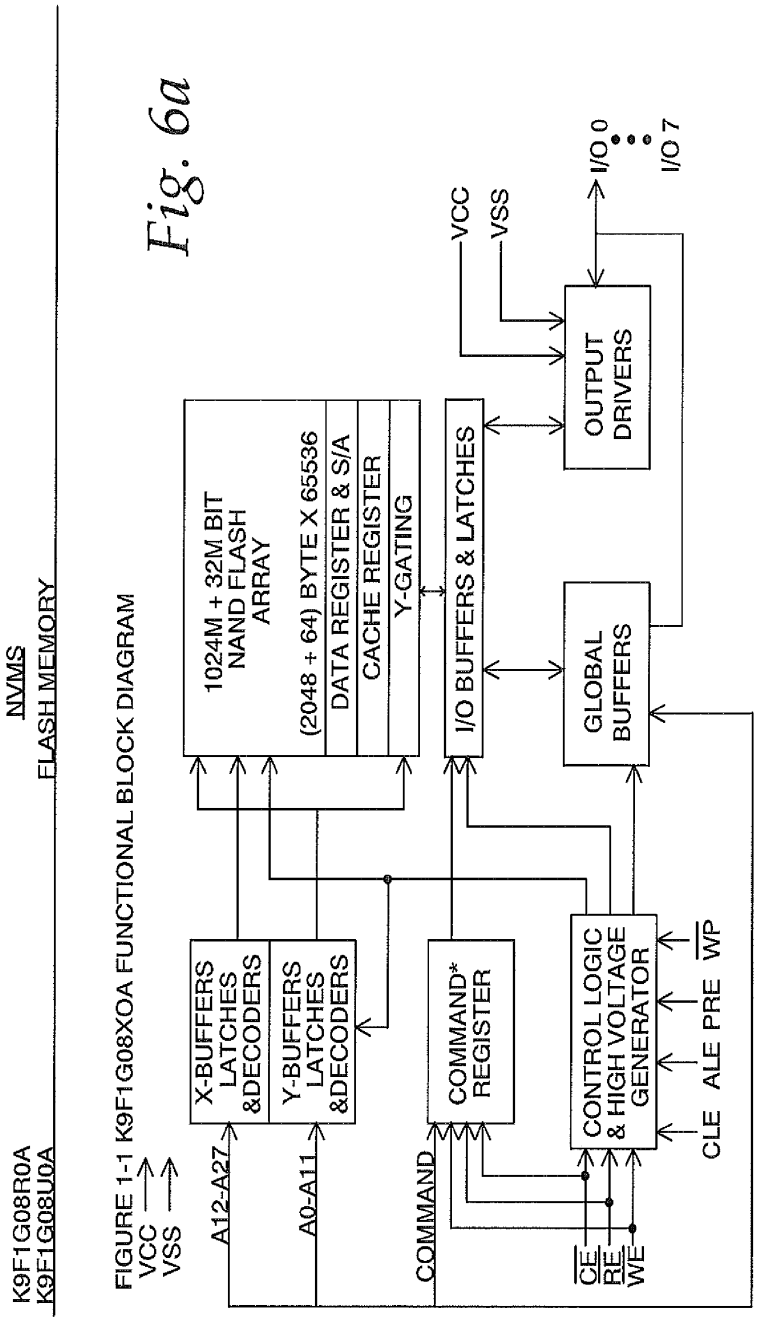
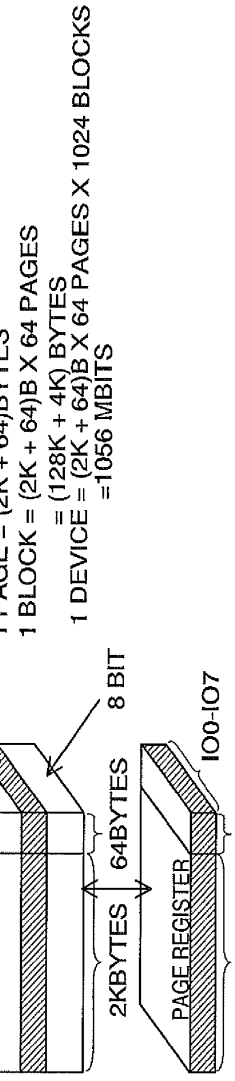

K9F1G08R0A
K9F1G08U0A
NVMS
FLASH MEMORY
FIGURE 1-1 K9F1G08XOA FUNCTIONAL BLOCK DIAGRAM
VCC
VSS
A12-A27
A0-A11
COMMAND
X-BUFFERS LATCHES &DECODERS
Y-BUFFERS LATCHES &DECODERS
COMMAND* REGISTER
1024M + 32M BIT NAND FLASH ARRAY
(2048 + 64) BYTE X 65536
DATA REGISTER & S/A
CACHE REGISTER
Y-GATING
I/O BUFFERS & LATCHES
CONTROL LOGIC & HIGH VOLTAGE GENERATOR
GLOBAL BUFFERS
OUTPUT DRIVERS
VCC
VSS
I/O 0
I/O 7
CE
RE
WE
CLE
ALE
PRE
WP

Fig. 6a

Fig. 6b

FIGURE 2-1. K9F1G08XOA (X8) ORGANIZATION



	I/0.0	I/0.1	I/0.2	I/0.3	I/0.4	I/0.5	I/0.6	I/0.7	
1ST CYCLE	A0	A1	A2	A3	A4	A5	A6	A7	COLUMN ADDRESS
2ND CYCLE	A8	A9	A10	A11	*L	*L	*L	*L	COLUMN ADDRESS
3RD CYCLE	A12	A13	A14	A15	A16	A17	A18	A19	ROW ADDRESS
4TH CYCLE	A20	A21	A22	A23	A24	A25	A26	A27	ROW ADDRESS

NOTE: COLUMN ADDRESS: STARTING ADDRESS OF THE REGISTER
*L MUST BE SET TO "LOW"
*THE DEVICE IGNORES ANY ADDITIONAL INPUT OF ADDRESS CYCLES THAN REQUIRED.

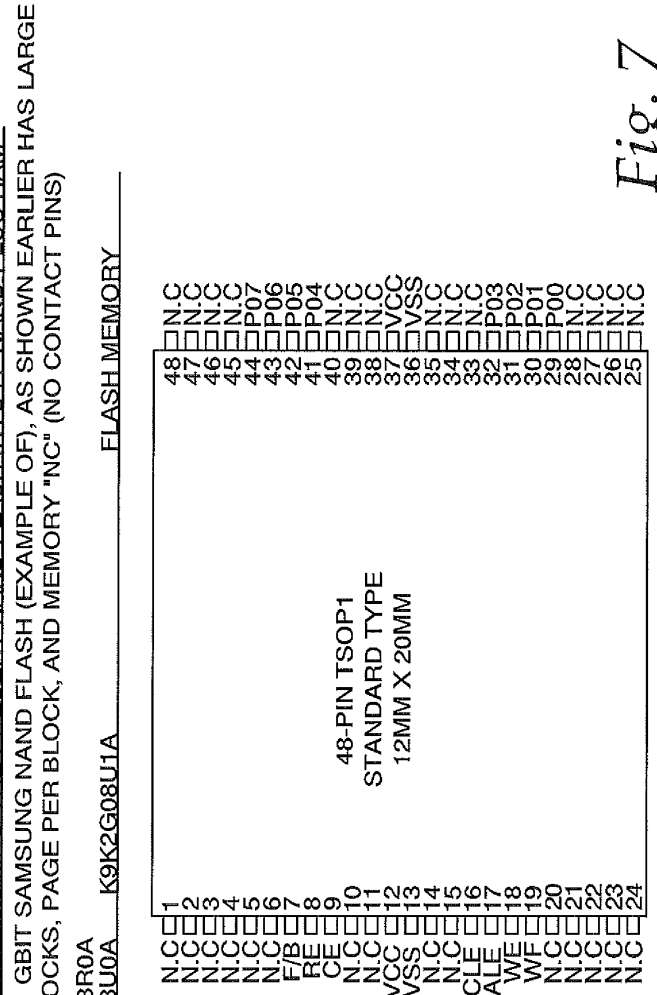

NVMS CONFIGURING THE PRESENT NAND FLASH INTO A "NAND PLUS RAM"
THE CURRENT 1 GBIT SAMSUNG NAND FLASH (EXAMPLE OF), AS SHOWN EARLIER HAS LARGE BLOCKS, PAGE PER BLOCK, AND MEMORY "NC" (NO CONTACT PINS)
K9F1G08R0A
K9F1G08U0A K9K2G08U1A FLASH MEMORY
48-PIN TSOP1
STANDARD TYPE
12MM X 20MM
1 N.C
2 N.C
3 N.C
4 N.C
5 N.C
6 F/B
7 RE
8 CE
9 N.C
10 N.C
11 VCC
12 VSS
13 N.C
14 N.C
15 CLE
16 ALE
17 WE
18 WP
19 N.C
20 N.C
21 N.C
22 N.C
23 N.C
24
48 N.C
47 N.C
46 N.C
45 N.C
44 P07
43 P06
42 P05
41 P04
40 N.C
39 N.C
38 N.C
37 VCC
36 VSS
35 N.C
34 N.C
33 N.C
32 P03
31 P02
30 P01
29 P00
28 N.C
27 N.C
26 N.C
25 N.C

Fig. 7

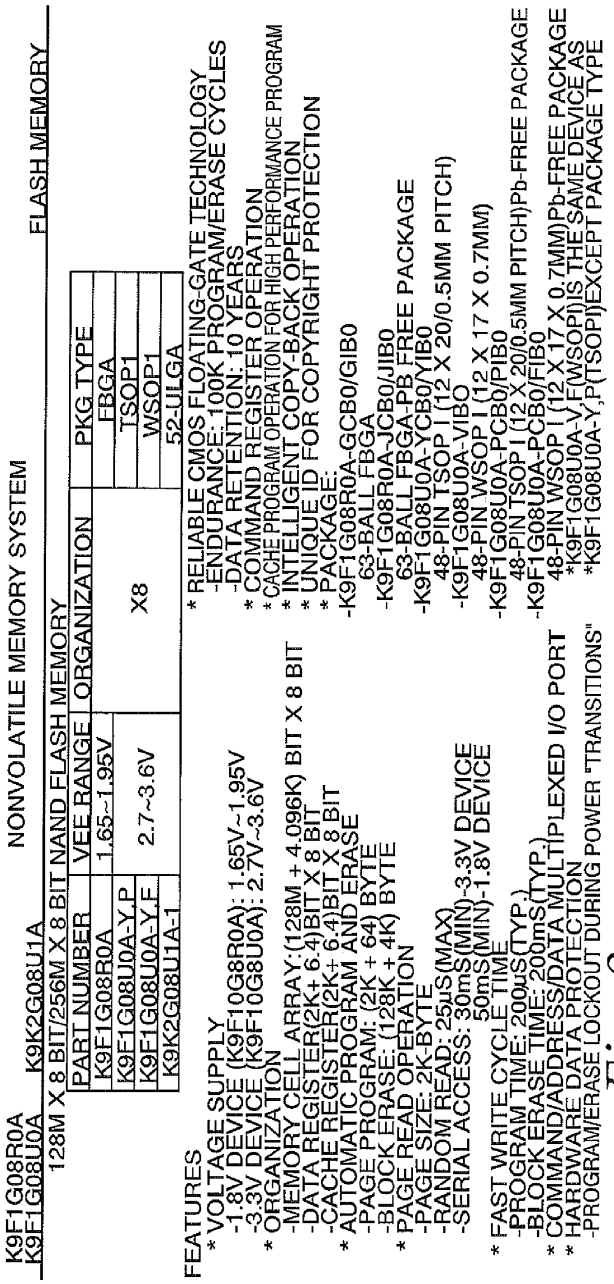

K9F1G08R0A
K9F1G08U0A
K9K2G08U1A
NONVOLATILE MEMORY SYSTEM
FLASH MEMORY
128M X 8 BIT/256M X 8 BIT NAND FLASH MEMORY
PART NUMBER
VEE RANGE
ORGANIZATION
PKG TYPE
K9F1G08R0A
1.65~1.95V
X8
FBGA
K9F1G08U0A-Y,P
TSOP1
K9F1G08U0A-Y,F
2.7~3.6V
WSOP1
K9K2G08U1A-1
52-ULGA
FEATURES
* VOLTAGE SUPPLY
-1.8V DEVICE (K9F10G8R0A): 1.65V~1.95V
-3.3V DEVICE (K9F10G8U0A): 2.7V~3.6V
* ORGANIZATION
-MEMORY CELL ARRAY: (128M + 4,096K) BIT X 8 BIT
-DATA REGISTER(2K+ 6.4)BIT X 8 BIT
-CACHE REGISTER(2K+ 6.4)BIT X 8 BIT
* AUTOMATIC PROGRAM AND ERASE
-PAGE PROGRAM: (2K + 64) BYTE
-BLOCK ERASE: (128K + 4K) BYTE
* PAGE READ OPERATION
-PAGE SIZE: 2K-BYTE
-RANDOM READ: 25μS(MAX)
-SERIAL ACCESS: 30mS(MIN)-3.3V DEVICE
50mS(MIN)-1.8V DEVICE
* FAST WRITE CYCLE TIME
-PROGRAM TIME: 200μS(TYP.)
-BLOCK ERASE TIME: 200mS(TYP.)
* COMMAND/ADDRESS/DATA MULTIPLEXED I/O PORT
* HARDWARE DATA PROTECTION
-PROGRAM/ERASE LOCKOUT DURING POWER "TRANSITIONS"
* RELIABLE CMOS FLOATING-GATE TECHNOLOGY
-ENDURANCE: 100K PROGRAM/ERASE CYCLES
-DATA RETENTION: 10 YEARS
* COMMAND REGISTER OPERATION
* CACHE PROGRAM OPERATION FOR HIGH PERFORMANCE PROGRAM
* INTELLIGENT COPY-BACK OPERATION
* UNIQUE ID FOR COPYRIGHT PROTECTION
* PACKAGE:
-K9F1G08R0A-GCB0/GIB0
63-BALL FBGA
-K9F1G08R0A-JCB0/JIB0
63-BALL FBGA-PB FREE PACKAGE
-K9F1G08U0A-YCB0/YIB0
48-PIN TSOP I (12 X 20/0.5MM PITCH)
-K9F1G08U0A-VIB0
48-PIN WSOP I (12 X 17 X 0.7MM)
-K9F1G08U0A-PCB0/PIB0
48-PIN TSOP I (12 X 20/0.5MM PITCH)Pb-FREE PACKAGE
-K9F1G08U0A-PCB0/FIB0
48-PIN WSOP I (12 X 17 X 0.7MM)Pb-FREE PACKAGE
*K9F1G08U0A-V,F(WSOP1)IS THE SAME DEVICE AS
*K9F1G08U0A-Y,P(TSOP1)EXCEPT PACKAGE TYPE
-K9K2G08U1A-ICB0/IIB0
52-ULGA (12 X 17X 0.65MM)

Fig. 8

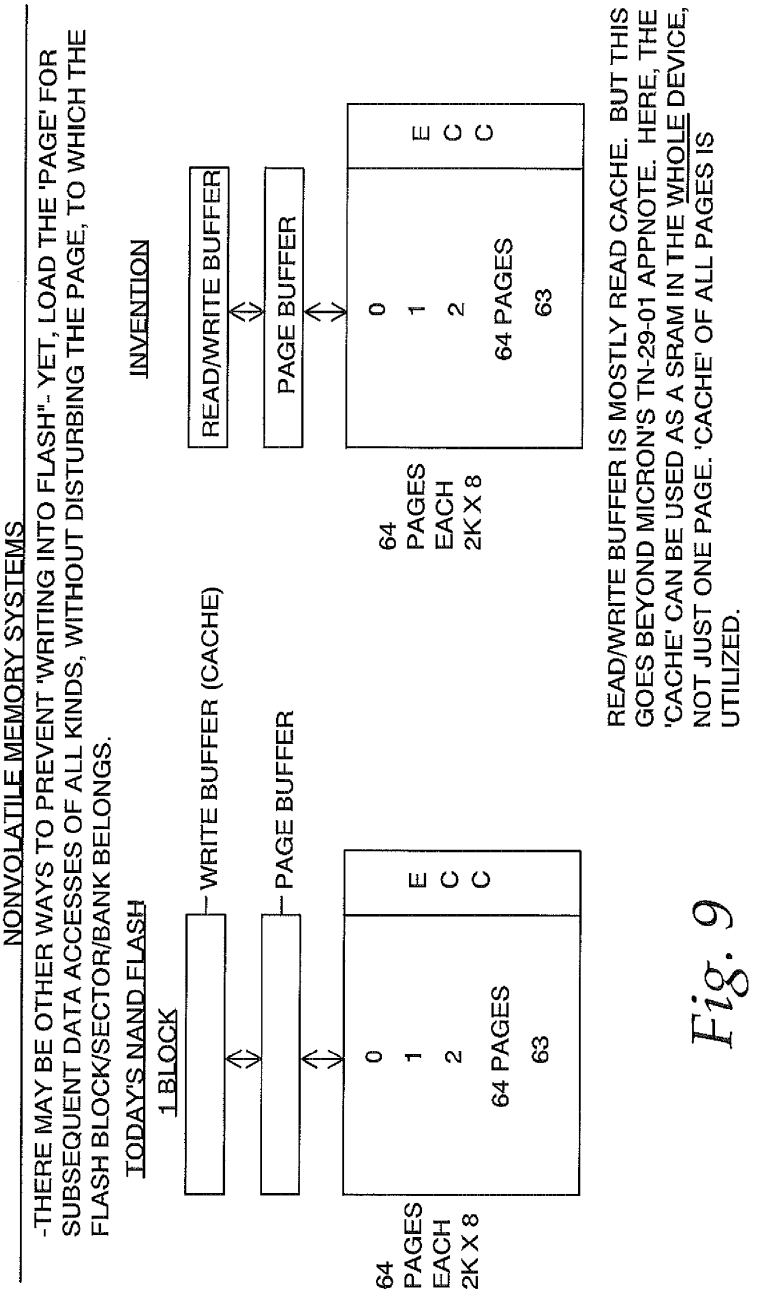

NONVOLATILE MEMORY SYSTEMS
-THERE MAY BE OTHER WAYS TO PREVENT 'WRITING INTO FLASH"- YET, LOAD THE 'PAGE' FOR SUBSEQUENT DATA ACCESSES OF ALL KINDS, WITHOUT DISTURBING THE PAGE, TO WHICH THE FLASH BLOCK/SECTOR/BANK BELONGS.
TODAY'S NAND FLASH
1 BLOCK
WRITE BUFFER (CACHE)
PAGE BUFFER
64 PAGES EACH 2K X 8
0
1
2
63
64 PAGES
E
C
C
INVENTION
READ/WRITE BUFFER
PAGE BUFFER
64 PAGES EACH 2K X 8
0
1
2
63
64 PAGES
E
C
C
READ/WRITE BUFFER IS MOSTLY READ CACHE. BUT THIS GOES BEYOND MICRON'S TN-29-01 APPNOTE. HERE, THE 'CACHE' CAN BE USED AS A SRAM IN THE WHOLE DEVICE, NOT JUST ONE PAGE. 'CACHE' OF ALL PAGES IS UTILIZED.

Fig. 9

NONVOLATILE MEMORY SYSTEMS
*BATTERY BACK UP SRAM/AND/OR DRAM WITH FLASH (OR SIMILAR NONVOLATILE MEMORY WITH SLOW WRITE TIME)
HAVE THE SRAM AND/OR DRAM STORE WRITE AND WRITE TO NV MEMORY ONLY IN "IDLE" OR "NO INTERRUPT WITH RAM" TIME
PROVIDE BATTERY BACK UP FOR RAM SO DATA IN RAM IS NOT LOST
DRAM AND /OR SRAM DENSITY CAN BE ABOUT 1/10TH (10%) OF NV DENSITY E.G., 256Mb OF RAM FOR 3 TO 4 GBITS OF NV(LIKE FLASH)
SPECIAL INTERFACE
DRAM/AND/OR SRAM (BATTERY BACK UP)
NONVOLATILE MEMORY
HOST OR NVM CONTROLLER
TRADITIONAL BUS FOR MEMORY
THIS GOES BEYOND THE "MULTI CHIP PACKAGE SOLUTIONS" OF PSRAM/FLASH OFFERED IN CELL PHONES TODAY
*INCLUDE NEW COMMANDS IN REGISTERS OF BOTH, RAM AND NV.

Fig. 10

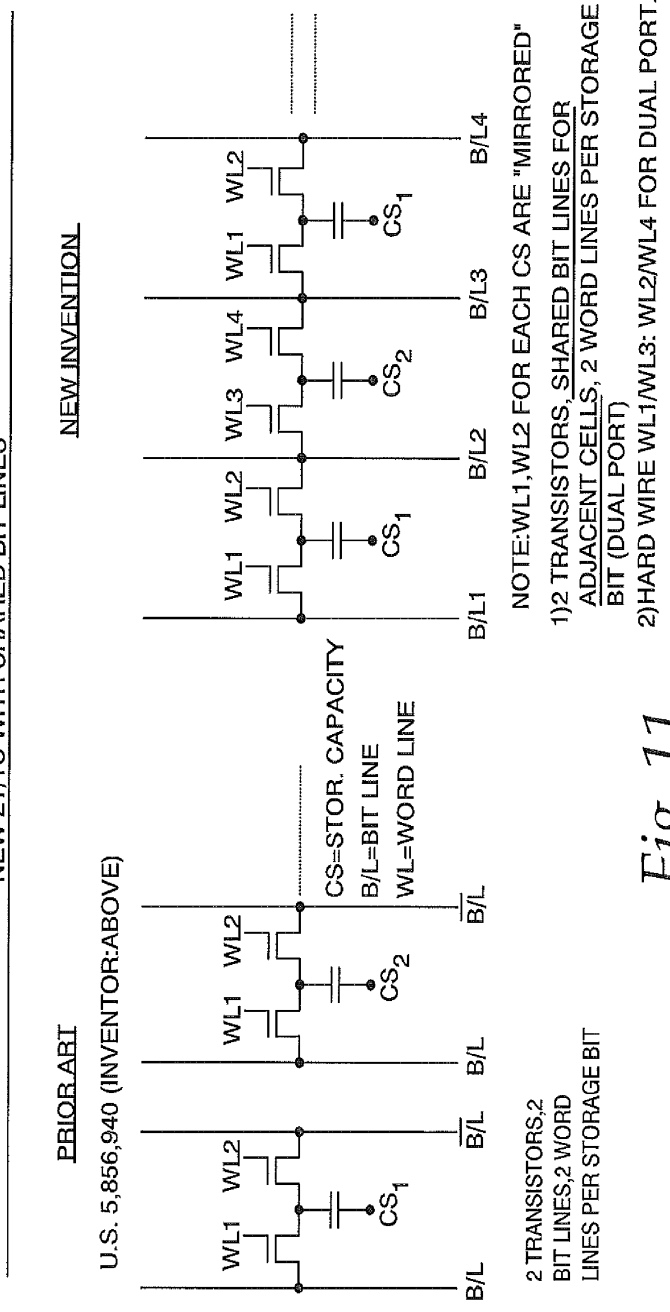
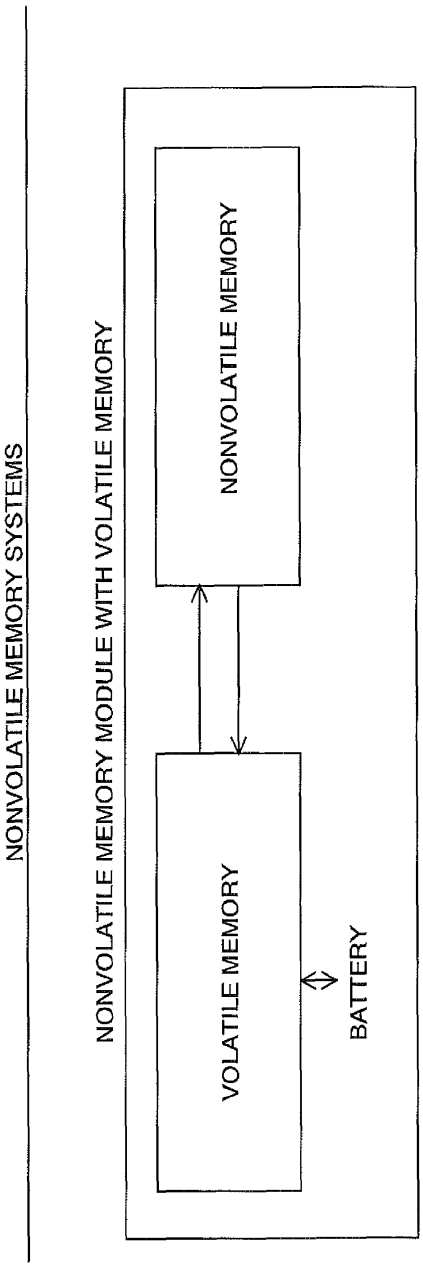

NEW 2T/1C WITH SHARED BIT LINES
PRIOR ART
U.S. 5,856,940 (INVENTOR:ABOVE)
NEW INVENTION
WL1
WL2
WL3
WL4
CS1
CS2
B/L
B/L1
B/L2
B/L3
B/L4
CS=STOR. CAPACITY
B/L=BIT LINE
WL=WORD LINE
2 TRANSISTORS,2 BIT LINES,2 WORD LINES PER STORAGE BIT
NOTE:WL1,WL2 FOR EACH CS ARE "MIRRORED"
1)2 TRANSISTORS, SHARED BIT LINES FOR ADJACENT CELLS, 2 WORD LINES PER STORAGE BIT (DUAL PORT)
2)HARD WIRE WL1/WL3: WL2/WL4 FOR DUAL PORT.

Fig. 11



*VOLATILE MEMORY CAN BE DRAM, SRAM OR COMBINATION
*NONVOLATILE MEMORY CAN BE ANY KIND OF FLASH, MAGRAM,FERAM,CNT ETC.
*READ/WRITE CAN BE THROUGH VM(VOLATILE MEMORY) WHICH ACTS AS A CACHE BUFFER (BOTH DATA AND ADDRESS, COULD BE COMMAND AS WELL)

Fig. 12

NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation application of U.S. patent application Ser. No. 12/256,362 filed Oct. 22, 2008 now U.S. Pat. No. 7,855,916 and entitled "NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES," and is hereby incorporated by reference in its entirety and which claims priority under 35 U.S.C. §119(e) to U.S. Provisional Patent Application Ser. No. 60/982,175 filed on Oct. 24, 2007 entitled "NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND RITE MEMORIES," and which is hereby incorporated by reference in its entirety.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable.

REFERENCE TO SEQUENCE LISTING, A TABLE, OR A COMPUTER PROGRAM LISTING COMPACT DISC APPENDIX

Not Applicable.

BACKGROUND OF THE INVENTION

Nonvolatile memory systems, subsystems and integrated circuits are used in multiple consumer, computer and communications applications. They can be a NAND flash memory IC or NOR flash memory. Part of the memory system may contain volatile memory like static random access memory (SRAM) or dynamic random access memory (DRAM). They can be many IC's mounted on a memory card or module. A subsystem may contain at least one such module and a memory controller. A system may contain several subsystems as well as multi core CPU's (Central Processing Unit). The memory integrated circuits used in such a system may be SLC (single level) or MLC (multi level) storage. The read/write access ports to the system may be single ported or multi ported.

Today's dominant memory is flash. In flash, the dominant architecture is NAND flash. In spite of the fact that the internal IC architecture of NAND (or for that matter other flash architectures like NOR, OneNAND™) has "page" architecture for read and write access, the performance (read time, program/write time) is slow compared to volatile memory systems built with SRAMs and DRAMs. The "page" architecture in NAND indeed has "static latches" that can temporarily store data as a buffer (one page per block), and sometimes have an additional "write cache buffer" for the whole IC. The page is 1 KB (1,024 bytes) to 2 KB (2,048 bytes). Each nonvolatile memory block of NAND flash memory cells, may have 64 to 128 pages (or, 128 KB to 256 KB). Still, the performance is relatively poor to mediocre at best from a randomly and independently accessible perspective per each byte of data. The "page buffered architecture" of today's NAND flash memory does not lend itself to true, fast, read and write memory access for SSD (solid state disk) and similar commercial applications in PCs and servers for data computation, storage and multimedia execution.

The invention described in this utility patent application focuses on ways to modify the already existing "buffers" in an optimal manner to enhance the random access performance of nonvolatile IC, subsystem and system. The volatile random access memory (RAM) in a preferred embodiment is a 6-transistor SRAM memory cell at the core, and complete peripheral address decoding circuitry for independent accessible access (read, write etc) at a fine grain level of a bit, or byte. In another embodiment, the volatile RAM in each block can be an 8-transistor dual-ported SRAM. In another embodiment, the nonvolatile memory can be a DRAM. The invention is applicable to other nonvolatile or pseudo non volatile memories like PCM (phase change memory), nano crystalline memory, charge trapped memory, ferroelectric memory, magnetic memory, plastic memory and similar embodiments.

BRIEF SUMMARY OF THE INVENTION

The preferred embodiment adds new commands to be executed in the Command Register of the NVM (nonvolatile memory). In other embodiments, these commands can be shared between the NVM IC and memory controller. Prior art NVM IC's have limited commands like (1) read page in flash; (2) erase block in flash; (3) program page in flash, etc. With this invention, new additional commands are executed: (4) read page in the SRAM of the block only; (5) read new page from the nonvolatile memory (NVM) block; (6) write page into SRAM of the block, but, not program into the NVM block until such a command is additionally given. This invention provides every page of each NVM block as an independently accessible random access memory to perform load/store applications, as well as a coupled memory to the assigned NVM block. Each NVM NAND flash may have 1,024 such blocks. Each block is typically 64 kilobytes in density. Page for each block is typically 1 to 2 kilobytes and each bit is independently addressable in a random manner, as well as accessed in a random manner. Error correction and detection to the memory on a page basis can be implemented as well either on the NVM IC or in the memory controller.

Another preferred embodiment selects any of the currently unused blocks and uses the SRAM pages in those blocks to perform other operations as necessary. Such data manipulating operations can be arithmetic and/or logic operations. In another preferred embodiment, the "volatile memory of a page" is a DRAM. That DRAM, again, is independently accessible and addressable in a random manner.

BRIEF DESCRIPTIONS OF THE DRAWINGS

FIG. **1** is a diagram showing a nonvolatile memory system with features as described for the present invention.

FIG. **2** shows an exemplary NAND memory integrated circuit as one element of the NVMS (nonvolatile memory system).

FIG. **3** shows various components of a controller for the nonvolatile memory system (NVMS) of this invention.

FIG. **4** shows a novel implementation of block erase per this invention.

FIG. **5** shows a flash memory controller with block erase feature.

FIG. **6** shows a current NAND flash chip architecture by Samsung.

FIG. **7** shows a pin out for a 1 Gb Samsung flash memory.

FIG. **8** shows some operational features of the above Samsung flash memory.

FIG. **9** shows how the invention of this patent distinguishes itself from today's nonvolatile memory.

FIG. **10** shows improved features of this invention compared to currently available (commercial) multichip NVMS solutions.

FIG. **11** shows how the "random access memory" of this invention can be implemented in dual port access for enhanced performance.

FIG. **12** shows a high level architecture of the NVMS of this invention which comprises both nonvolatile and volatile memory.

DETAILED DESCRIPTION OF THE INVENTION

Each NAND flash memory commercially available (in various pin outs/densities) today has a 512 B-1 KB-2 KByte page in a 64 Kb to 128K Byte block (a block contains at least one sector), 64 rows worth of data, 1 page/sector. To write one page takes about 200 μs. There are about 1,024 sectors in a 1 Gbit flash (NAND). So each NAND flash chip has 1 Mb SRAM (1 k pages). The invention requires each page to have "bit-to-bit" NVM back up (nonvolatile SRAM). So a page can be copied directly to the NVM as needed. This additional row can be in the sector itself. Address/control logic to accommodate this page can be easily done in the sector, if needed.

Page invention—Modify page as shown in Samsung K9F1G08R0A (1 Gbit NANDflash). In the Samsung device, Page is approximately 2 KByte+64 bits (for some kind of Ecc) in each 128 KByte block. There are 1 K blocks, each of 128 KBytes (inclusive of Page). The Page has no direct identity (namely, it is not a register or RAM with independent random address and command executions)—it is temporary storage buffer to help execute read/write to nonvolatile array. Since each block (sector) is addressable, one can have a "Tag address bit"—if enabled it can activate "page addressing."

Control Page—Nonvolatile array communication with a 'Switch' where volatile and nonvolatile memory can be accessed (unlike current art)—then page 2 Kbytes can be used as independent RAM for other useful purposes. One preferred embodiment—Select any of the currently unused blocks and use that/those pages as a modified SRAM; access that SRAM by currently used NC pins and rename them. Even with "concurrent Read/Write", "write cache buffering" and other features, most blocks among the (1,024 or more) many in a NAND flash chip are unused while one or two blocks are being accessed (read, write, erase). The associated "page buffers" are also unused and wasted. In this preferred embodiment, a page of the currently unused block's page (2 K Bytes×1 Kblocks is 2 MBytes of SRAM per chip—with a little overhead circuitry it can be 2 MBytes of SRAM with multiple port access as well) can be read and written (random page access, random access within a page, serial access from a page etc.). There are plenty of NC pins available in commercially available NAND flash ICs (one example is provided in FIG. **7**)—we can configure NC pins to be used as Address, DATA, Command, Control in a combination. In parallel, the NAND flash can concurrently operate.

The concepts of SRAM mode by using available pages can also be implemented in Samsung's one NAND™ flash (for example), NOR flash or even Serial EEPROM flash—The exact implementation, page/latch size, command set may vary. The concepts of SRAM mode by using available pages can also be implemented in traditional NOR flash, as well, with slight modifications (e.g., one row equivalent page in every block or sector, on chip cache, boot code, data buffers). The concepts of SRAM mode can also be implemented in other nonvolatile memory devices (and their controllers) e.g., FeRAM, MRAM, Phase change RAM/memory, CNT RAM, NROM (Saifun) and similar ones. All these concepts can configure the multiple functions of the device or combination there of by (1) control/command signals, (2) programmable registers, (3) mode registers, (4) command register, etc—they can reside in part or in whole in controller, memory, special control, command, interface chip or even CPU.

It should be made clear that the "pages" and "buffers" mentioned in these pages titled "NVMS" do not necessarily have to be (1) static latches (6 transistor latches) or (2) traditional SRAM's. They can be DRAM's as is known widely in the industry. They can be MRAM, FeRAM (ferroelectric) or other similar concepts (molecular RAM etc). The implementation of a nonvolatile memory system may contain these configurable NVMS chips as described here (one or more). Configurable NVMS can be combined with commodity NOR/NAND/One NAND, flash chips, controllers, PSRAM's, DRAM's, or other similar functions to offer a total "system-in-package" (SIP) or "system-on-chip" (SOC).

In order to conserve operating power, the unselected, yet available pages can be in a "stand by" mode—namely, reduced Vcc (power supply voltage), until the access to that page is required. Such a, 'cycle look ahead', can be built into the memory chip, or provided by controller (on chip or off chip). A battery back up for the SRAM part of the device can be a very attractive option for a very large density total nonvolatile static random access memory (NVSRAM) that can go into a broad range of applications in computer, consumer, communications etc. Maxim supplies NVSRAM's—no flash IC in NVSRAM. A "power triggered switch-off/on" (Similar to what Simtek's NVSRAM's do) is also possible, thus eliminating the "battery option".

Commands/Instructions are given as follows, in a preferred embodiment, which vary between NAND, One NAND, NOR, serial flash etc. Traditional flash: Read page in flash, Erase block in flash, Program page in flash, Etc. New commands with these inventions: Read page as SRAM/RAM, Write page as SRAM/RAM, Read/Modify/W Write page as SRAM/RAM, Read byte out of a page, etc; Write byte out of a page etc. Nibble mode/Serial access/double data rate are all possible.

The "address boundary" for a commercial NAND flash (especially in burst mode access e.g., burst READ) is different than a "2 K byte" NAND flash page. The address boundary does/should not deter by using the inventions mentioned here for a superior READ (intelligent caching) or WRITE performance. Most flash systems are weighted to MOSTLY READ and FEW ERASE/PROGRAM (WRITE) due to the obvious endurance limitations (write/erase cycles limit). Hence, any performance in READ—Speed, and available Storage space—is always beneficial to a stand alone die and/or card, module, subsystem, system. To write to a page or pseudo page, WRITE command and immediately PROGRAM SUSPEND to invalidate writing into NVM. The data should be in page/pseudo page. This is one example.

As described in earlier pages, the page latches are available for reading. The pages can be read a byte (8 bits) or 2 bytes (16 bits) at a time. The whole page 2 K bytes, can be sequentially accessed in 20-25 ns/byte. The subject invention uses the pages as a content addressable memory (CAM) and the NVM core as the stored data. The match lines (as used in CAM's—refer to U.S. Pat. Nos. 6,310,880 and 6,597,596 which use a DRAM storage) can be connected to the pages. The addresses in each block can be sequentially read, until the MATCH is found.

What is claimed is:

1. A non-volatile memory module comprising:

a pool of NAND flash arranged as a plurality of blocks wherein each block is comprised of a plurality of pages;

a pool of volatile memory;

a controller coupled to the pool of NAND flash and the pool of volatile memory;

an interface coupled to the controller;

wherein each page of NAND flash has a corresponding page of volatile memory; and

wherein each page of a block of the pool of NAND flash is adapted to be substituted on the fly for any other page of a different block of the pool of NAND flash through address mapping.

2. The non-volatile memory module of claim **1** wherein the volatile memory is static random access memory.

3. The non-volatile memory module of claim **1** wherein the volatile memory module is dynamic random access memory.

4. The non-volatile memory module of claim **1** wherein each page is at least 1 kilobyte of memory.

5. The non-volatile memory module of claim **1** wherein each page is 2 kilobyte of memory.

6. The non-volatile memory module of claim **1** wherein each block is at least 64 kilobyte of memory.

7. The non-volatile memory module of claim **2** further comprising a battery coupled to the volatile memory.

8. The non-volatile memory module of claim **3** further comprising a battery coupled to the volatile memory.

9. The non-volatile memory module of claim **1** wherein the NAND flash is comprised of single level memory cells.

10. The non-volatile memory module of claim **1** wherein the NAND flash is comprised of multi-level memory cells.

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