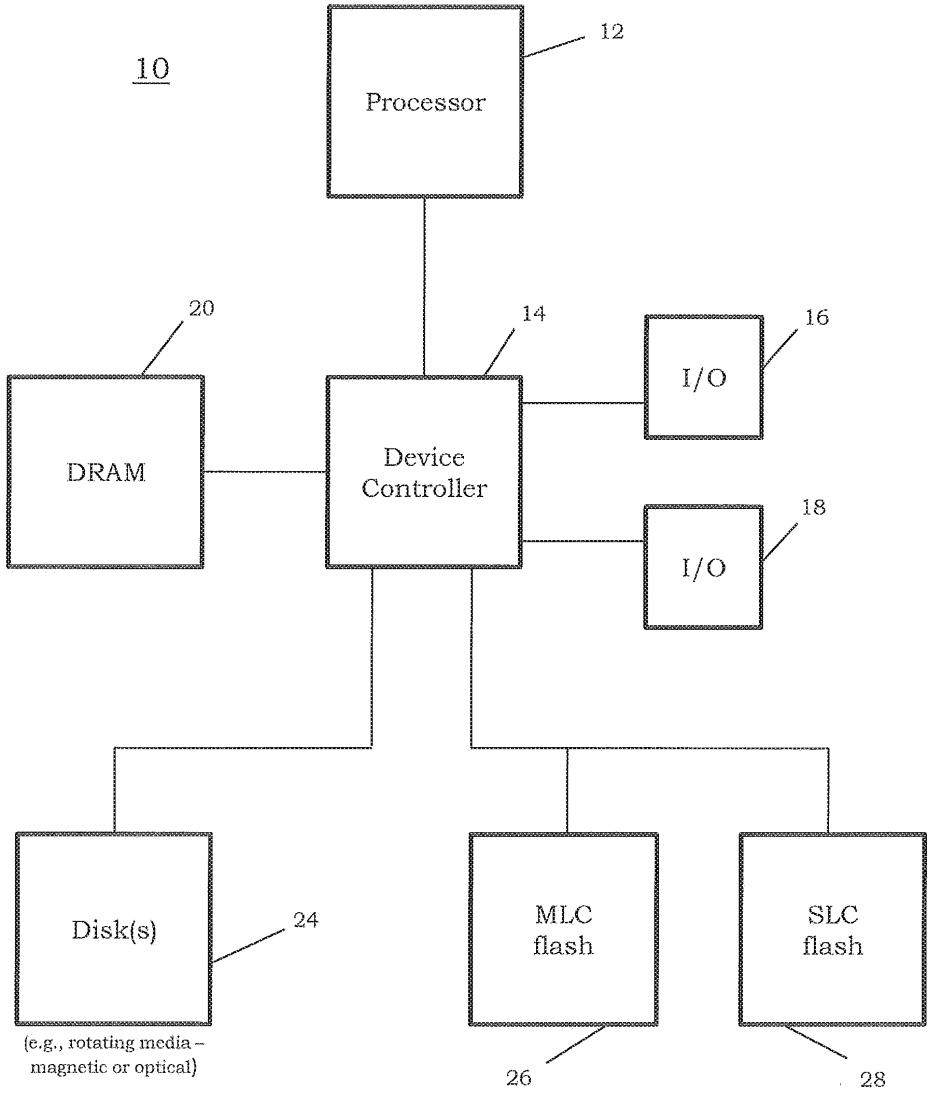

10
Processor
12
20
14
16
DRAM
Device Controller
I/O
18
I/O
Disk(s)
24
(e.g., rotating media – magnetic or optical)
MLC flash
SLC flash
26
28

FIG. 1

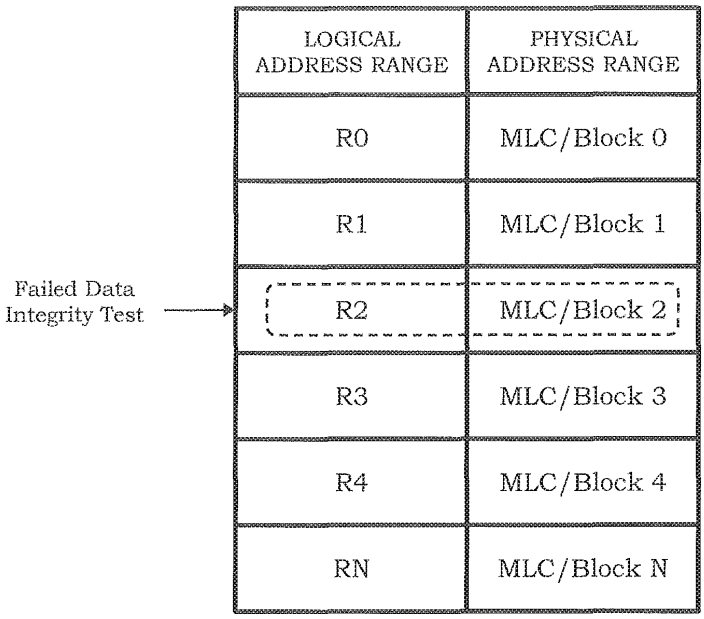

LOGICAL ADDRESS RANGE
PHYSICAL ADDRESS RANGE
R0
MLC/Block 0
R1
MLC/Block 1
Failed Data Integrity Test
R2
MLC/Block 2
R3
MLC/Block 3
R4
MLC/Block 4
RN
MLC/Block N

FIG. 2A

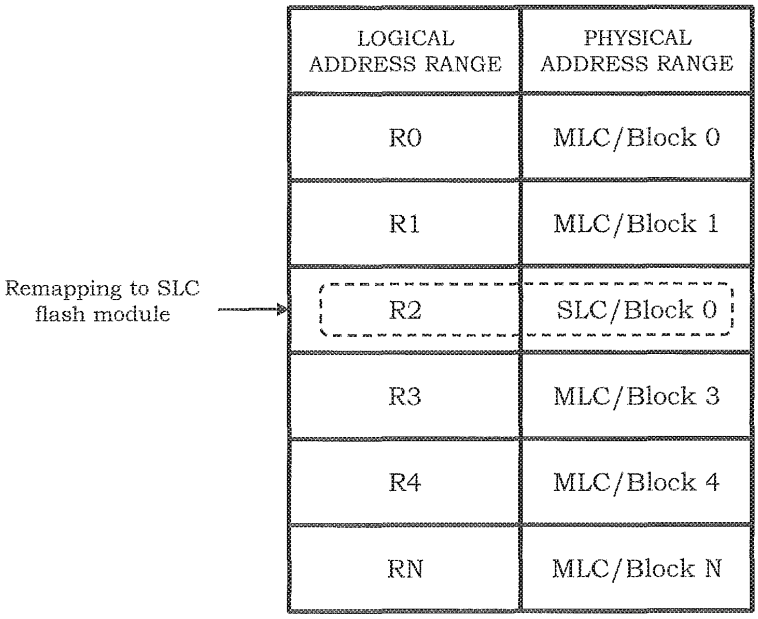

LOGICAL ADDRESS RANGE
PHYSICAL ADDRESS RANGE
R0
MLC/Block 0
R1
MLC/Block 1
Remapping to SLC flash module
R2
SLC/Block 0
R3
MLC/Block 3
R4
MLC/Block 4
RN
MLC/Block N

FIG. 2B

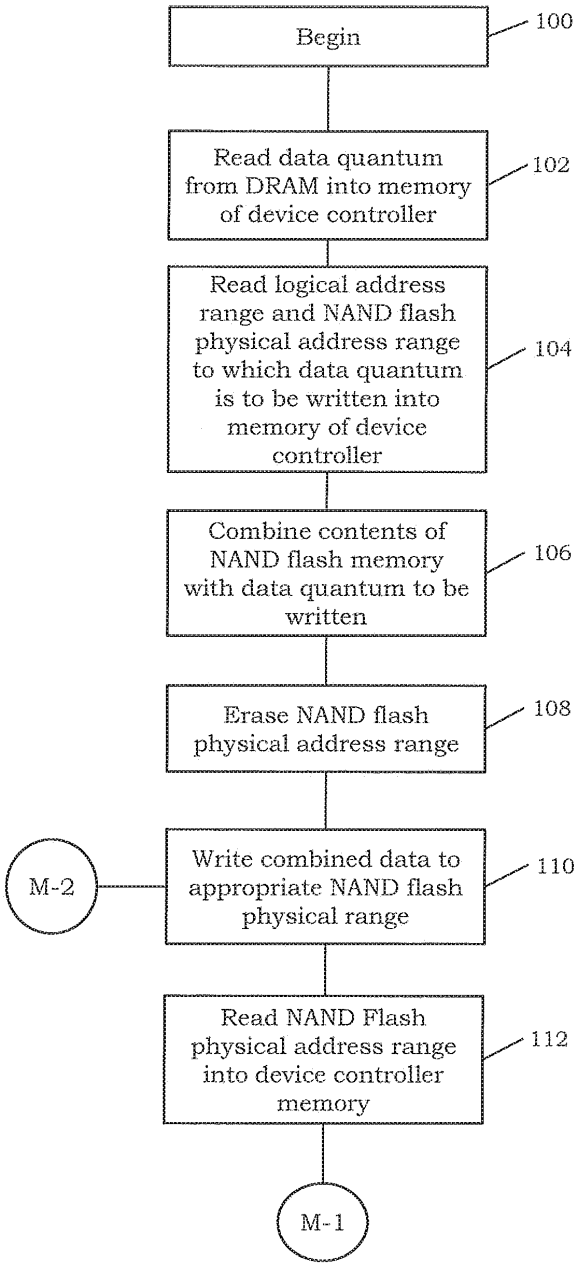

Begin
100
Read data quantum from DRAM into memory of device controller
102
Read logical address range and NAND flash physical address range to which data quantum is to be written into memory of device controller
104
Combine contents of NAND flash memory with data quantum to be written
106
Erase NAND flash physical address range
108
M-2
Write combined data to appropriate NAND flash physical range
110
Read NAND Flash physical address range into device controller memory
112
M-1

FIG. 3A

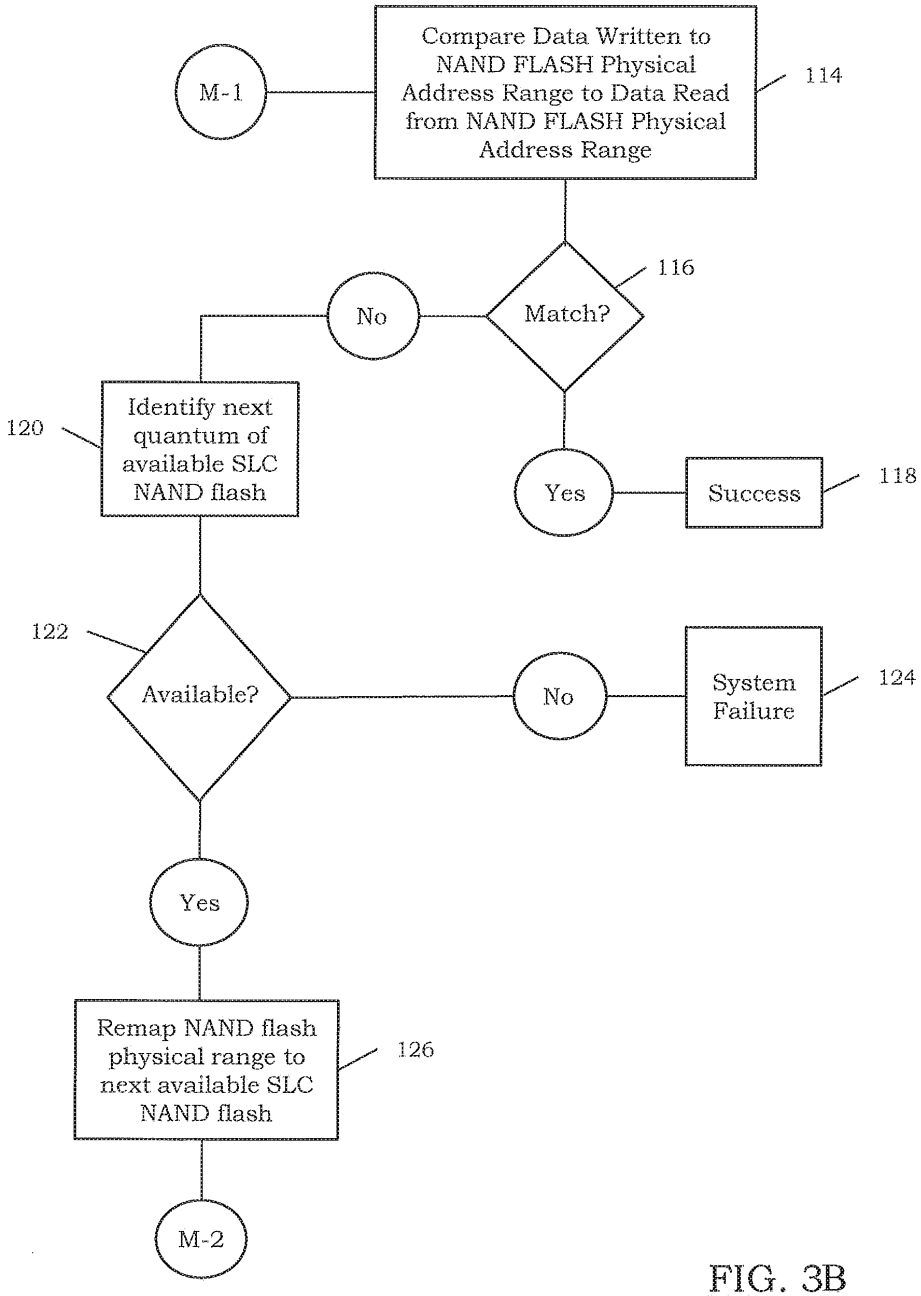

M-1
Compare Data Written to NAND FLASH Physical Address Range to Data Read from NAND FLASH Physical Address Range
114
Match?
116
No
Yes
Success
118
Identify next quantum of available SLC NAND flash
120
Available?
122
No
System Failure
124
Yes
Remap NAND flash physical range to next available SLC NAND flash
126
M-2

FIG. 3B

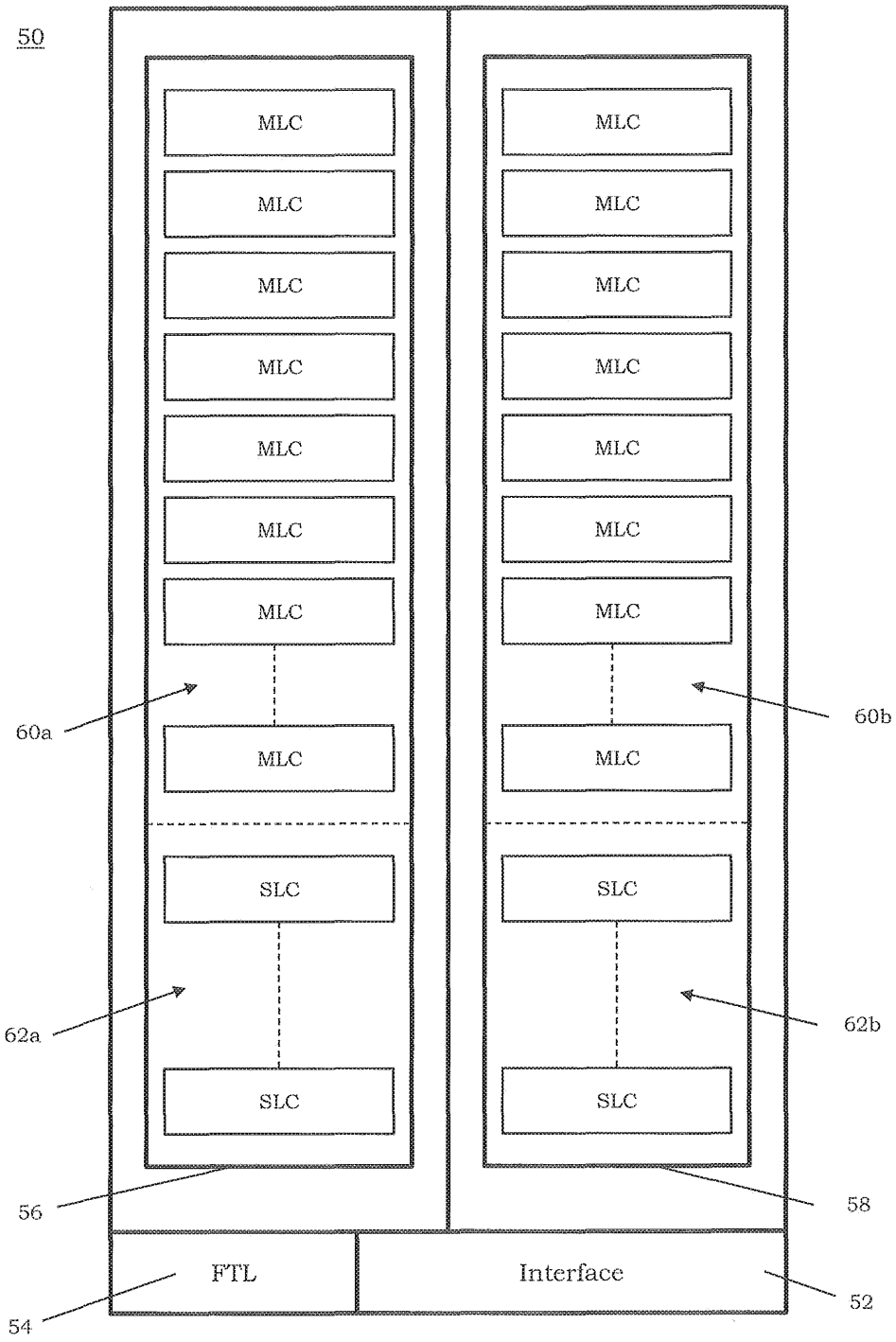

50
MLC
MLC
MLC
MLC
MLC
MLC
MLC
MLC
60a
60b
MLC
MLC
SLC
SLC
62a
62b
SLC
SLC
56
58
FTL
Interface
54
52

FIG. 4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR UNITED STATES PATENT

LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of U.S. Patent Application No. U.S. Application No. 14/950,553 filed on November 24, 2015, entitled LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM (Atty. Dkt. No. GRTD-32800), which published on June 2, 2016, as U.S. Application Publication No. 2016-0155496, now U.S. Patent No. 9,997,240 issued June 12, 2018, which is incorporated by reference in its entirety. U.S. Application No. 14/950,553 is a Continuation of U.S. Patent Application No. 14/525,411, filed October 28, 2014, entitled LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM, which published on October 1, 2015, as U.S. Publication No. 2015-0278013, now U.S. Patent No. 9,196,385, issued on November 24, 2015, (Atty. Dkt. No. GRTD-32620). Application No. 14/525,411 is a Division of U.S. Patent Application No. 13/455,267, filed April 25, 2012, published on January 24, 2013, as U.S. Publication No. 2013-0021846, now U.S. Patent No. 8,891,298, issued on November 18, 2014, entitled LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM (Atty. Dkt. No. GRTD-32619). Application No. 13/455,267 claims the benefit of U.S. Provisional Application No. 61/509,257, filed July 19, 2011, entitled LIFETIME MIXED LEVEL NAND FLASH SYSTEM (Atty. Dkt. No. GRTD-32624). Patent Nos. 9,997,240; 9,196,385; and 8,891,298 and Patent Application Publication Nos. 2015-0278013 and 2013-0021846 are hereby incorporated by reference in their entirety. This application also incorporates by reference the complete disclosure of U.S. Patent Application No. 12/256,362, filed October 22, 2008, published on April 30, 2009, as U.S. Publication No. 2009-0109787, now U.S. Patent No. 7,855,916, issued on December 21, 2010, entitled NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES (Atty. Dkt. No.

GRTD-32614). This application also incorporates by reference the complete disclosure of U.S. Patent Application No. 12/915,177, filed October 29, 2010, published on March 10, 2011, as U.S. Publication No. 2011-0060870, now U.S. Patent No. 8,194,452, issued on June 5, 2012, entitled NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES (Atty. Dkt. No. 32615).

TECHNICAL FIELD

[0002] This application relates to a system and method for providing reliable storage through the use of non-volatile memories and, more particularly, to a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use of a combination of single-level cell (SLC) and multi-level cell (MLC) NAND flash storage without substantially raising the cost of the NAND flash storage system. The memory in a total non-volatile memory system may contain some SRAM (static random-access memory), DRAM (dynamic RAM), RRAM (resistive RAM), PCM (phase change memory), MAGRAM (magnetic random-access memory), NAND flash, and one or more HDDs (hard disk drives) when storage of the order of several terabytes is required. The SLC non-volatile memory can be flash, PCM, RRAM, MAGRAM or any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash, and it provides for data access speeds that are faster than that of MLC flash or rotating storage media (e.g., HDDs).

BACKGROUND

[0003] Non-volatile memories provide long-term storage of data. More particularly, non-volatile memories can retain the stored data even when not powered. Magnetic (rotating) hard disk drives (HDD) dominate this storage medium due to lower cost compared to solid state disks (SSD). Optical (rotating) disks, tape drives and others have a smaller role in long-term storage systems. SSDs are preferred for their superior performance (fast access time), mechanical reliability and ruggedness, and portability. Flash memory, more specifically NAND flash, is the dominant SSD medium today.

[0004] RRAM, PCM, MAGRAM and others, wi11likely play a larger role in the future, each of them having their own advantages and disadvantages. They may ultimately replace flash memories, initially for use as a "write buffer" and later to replace "SLC flash" and "MLC flash." MLC NAND flash is a flash memory technology using multiple levels per cell to allow more bits to be stored using the same number of transistors. In SLC NAND flash technology, each cell can exist in one of two states, storing one bit of information per cell. Most MLC NAND flash memory has four possible states per cell, so it can store two bits of information per cell.

[0005] These semiconductor technology driven "flash alternatives," i.e., RRAM, PCM, MAGRAM and others, have several advantages over any (SLC or MLC) flash because they: 1) allow data to be written over existing data (without prior erase of existing data), 2) allow for an erase of individual bytes or pages (instead of having to erase an entire block), and 3) possess superior endurance (1,000,000 write-erase cycles compared to typical 100,000 cycles for SLC flash and less than 10,000 cycles for MLC flash).

[0006] HDDs have several platters. Each platter contains 250-5,000 tracks (concentric circles). Each track contains 64 to 256 sectors. Each sector contains 512 bytes of data and has a unique "physical (memory) address." A plurality of sectors is typically combined to form a "logical block" having a unique "logical address." This logical address is the address at which the logical block of physical sectors appears to reside from the perspective of an executing application program. The size of each logical block and its logical address (and/or address ranges/boundaries) is optimized for the particular operating system (OS) and software

applications executed by the host processor. A computer OS organizes data as "files." Each file may be located (stored) in either a single logical block or a plurality of logical blocks, and therefore, the location of files typically traverses the boundaries of individual (physical) sectors. Sometimes, a plurality of files has to be combined and/ or modified, which poses an enormous challenge for the memory controller device of a non-volatile memory system.

[0007] SSDs are slowly encroaching on the HDD space and the vast majority of NAND flash in enterprise servers utilizes a SLC architecture, which further comprises a NAND flash controller and a flash translation layer (FTL). NAND flash devices are generally fragmented into a number of identically sized blocks, each of which is further segmented into some number of pages. It should be noted that asymmetrical block sizes, as well as page sizes, are also acceptable within a device or a module containing devices. For example, a block may comprise 32 to 64 pages, each of which incorporates 2 - 4 Kbit of memory. In addition, the process of writing data to a NAND flash memory device is complicated by the fact that, during normal operation of, for example, single-level storage (SLC) , erased bits (usually all bits in a block with the value of '1') can only be changed to the opposite state (usually '0') once before the entire block must be erased. Blocks can only be erased in their entirety, and, when erased, are usually written to '1' bits. However, if an erased block is already there, and if the addresses (block, page, etc.) are allowed, data can be written immediately; if not, a block has to be erased before it can be written to.

[0008] FTL is the driver that works in conjunction with an existing operating system (or, in some embedded applications, as the operating system) to make linear flash memory appear to the system like a disk drive, i.e., it emulates a HDD. This is achieved by creating "virtual" small blocks of data, or sectors, out of flash's large erase blocks and managing data on the flash so that it appears to be "write in place" when in fact it is being stored in different locations in the flash. FTL further manages the flash so that there are clean/ erased places to store data.

[0009] Given the limited number of writes that individual blocks within flash devices can tolerate, wear leveling algorithms are used within the flash devices (as firmware commonly known as FTL or managed by a controller) to attempt to ensure that "hot" blocks, i.e., blocks that are frequently written, are not rendered unusable much faster than other blocks. This task is

usually performed within a flash translation layer. In most cases, the controller maintains a lookup table to translate the memory array physical block address (PBA) to the logical block address (LBA) used by the host system. The controller's wear-leveling algorithm determines which physical block to use each time data is programmed, eliminating the relevance of the physical location of data and enabling data to be stored anywhere within the memory array and thus prolonging the service life of the flash memory. Depending on the wear-leveling method used, the controller typically either writes to the available erased block with the lowest erase count (dynamic wear leveling); or it selects an available target block with the lowest overall erase count, erases the block if necessary, writes new data to the block, and ensures that blocks of static data are moved when their block erase count is below a certain threshold (static wear leveling).

[0010] MLC NAND flash SSDs are slowly replacing and/ or coexisting with SLC NAND flash in newer SSD systems. MLC allows a single cell to store multiple bits, and accordingly, to assume more than two values; i.e., '0' or '1'. Most MLC NAND flash architectures allow up to four (4) values per cell; i.e., '00', '01', '10', or '11'. Generally, MLC NAND flash enjoys greater density than SLC NAND flash, at the cost of a decrease in access speed and lifetime (endurance). It should be noted, however, that even SLC NAND flash has a considerably lower lifetime (endurance) than rotating magnetic media (e.g., HDDs), being able to withstand only between 50,000 and 100,000 writes, and MLC NAND flash has a much lower lifetime (endurance) than SLC NAND flash, being able to withstand only between 3,000 and 10,000 writes. As is well known in the art, any "write" or "program" to a block in NAND flash (floating gate) requires an "erase" (of a block) before "write."

[0011] Despite its limitations, there are a number of applications that lend themselves to the use of MLC flash. Generally, MLC flash is used in applications where data is read many times (but written few times) and physical size is an issue. For example, flash memory cards for use in digital cameras would be a good application of MLC flash, as MLC can provide higher density memory at lower cost than SLC memory.

[0012] When a non-volatile storage system combines HDD, SLC and MLC (setting aside volatile memory for buffering, caching etc) in a single (hybrid) system, new improvements and

solutions are required to manage the methods of writing data optimally for improved life time (endurance) of flash memory. Accordingly, various embodiments of a NAND flash storage system that provides long lifetime (endurance) storage at low cost are described herein.

[0013] The following description is presented to enable one of ordinary skill in the art to make and use the disclosure and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present disclosure is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

SUMMARY

[0014] According to one embodiment of the present disclosure, there is provided a system for storing data which comprises at least one MLC nonvolatile memory module (hereinafter referred to as "MLC module") and at least one SLC non-volatile memory module (hereinafter referred to as "SLC module"), each module comprises a plurality of individually erasable blocks. The data storage system according to one embodiment of the present disclosure further comprises a controller for controlling both the at least one MLC module and the at least one SLC module. In particular, the controller maintains an address map comprising a list of individual logical address ranges each of which maps to a similar range of physical addresses within either the at least one MLC module or the at least one SLC module. After each write to (flash) memory, the controller conducts a data integrity check to ensure that the data was written correctly. When the data was not written correctly, the controller modifies the table so that the range of addresses on which the write failed is remapped to the next available range of physical addresses within the at least one SLC module. The SLC module can be (NAND) flash, PCM, RRAM, MAGRAM or any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash, and it provides for data access speeds that are faster than that of MLC flash or rotating storage media (e.g., HDDs).

[0015] According to another embodiment of the present disclosure, there is provided a system for storing data which comprises a controller that is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The present disclosure will be more fully understood by reference to the following detailed description of one or more preferred embodiments when read in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout the views and in which:

[0017] FIG. 1 is a block diagram of a computer system incorporating one embodiment of the present disclosure;

[0018] FIGS. 2A and 2B are drawings depicting a translation table/address map in accordance with one embodiment of the present disclosure;

[0019] FIGS. 3A and 3B are a flow chart illustrating an exemplary method for use in implementing one embodiment of the present disclosure; and

[0020] FIG. 4 is a block diagram depicting one embodiment of the present disclosure for implementation within a NAND flash module.

DETAILED DESCRIPTION

[0021] The present disclosure is directed to the reliable storage of data in read and write memory, and, in particular, to the reliable storage of data in non-volatile memory, such as, for example, NAND flash. Generally, and in particular regard to NAND flash memory, two separate banks of NAND flash are maintained by a controller. One bank contains economical MLC NAND flash, while a second bank contains high endurance SLC NAND flash. The controller conducts a data integrity test after every write. If a particular address range fails a data integrity test, the address range is remapped from MLC NAND flash to SLC NAND flash. As the SLC NAND flash is used to boost the lifetime (endurance) of the storage system, it can be considerably lesser in amount than the MLC NAND flash. For example, a system may set SLC NAND flash equal to 12.5% or 25% of MLC NAND flash (total non-volatile memory storage space=MLC+SLC).

[0022] Turning to the Figures and to FIG. 1 in particular, a computer system 10 depicting one embodiment of the present disclosure is shown. A processor 12 is coupled to a device controller 14, such as a chipset, using a data link well known in the art, such as a parallel bus or packet-based link. The device controller 14 provides interface functions to the processor 12. In some computer systems, the device controller 14 may be an integral part of the (host) processor 12. The device controller 14 provides a number of input/output ports 16 and 18, such as, for example, serial ports (e.g., USB ports and Firewire ports) and network ports (e.g., Ethernet ports and 802.11 "Wi-Fi" ports). The device controller 14 may also control a bank of, for example, DRAM 20. In addition, the device controller 14 controls access to one or more disks 24, such as, for example, a rotating magnetic disk, or an optical disk, as well as two or more types of NAND flash memory. One type of NAND flash memory is a MLC NAND flash memory module 26. Another type of NAND flash memory is a SLC NAND flash memory module 28.

[0023] The device controller 14 maintains a translation table/address map which may include address translations for all devices in the computer system. Nonetheless, the discussion in the present disclosure will be limited only to NAND flash memory modules. In particular, the device controller 14 maintains a translation table that maps logical computer system addresses to physical addresses in each one of the MLC- and SLC-NAND flash memory modules 26 and 28,

respectively. As MLC flash memory is less expensive than SLC flash memory, on a cost per bit basis, the translation table will initially map all logical NAND flash addresses to the MLC NAND flash memory module 26. The address ranges within the translation table will assume some minimum quantum, such as, for example, one block, although a smaller size, such as one page could be used, if the NAND flash has the capability of erasing the smaller size quantum.

[0024] A "read-modify-write" scheme is used to write data to the NAND flash. Data to be written to NAND flash is maintained in DRAM 20. After each write to an address within a particular address range, the device controller 14 will—as time permits—perform a read on the address range to ensure the integrity of the written data. If a data integrity test fails, the address range is remapped from the MLC NAND flash memory module 26 to the next available address range in the SLC NAND flash memory module 28.

[0025] FIGS. 2A and 2B illustrate one embodiment of a translation table/address map of the present disclosure. In Figure. 2A, a list of logical address ranges (R0-RN) is translated to physical address ranges. As illustrated, all of the logical address ranges are translated to blocks on the MLC NAND flash memory module 26. However, through the application of a data integrity verification check (explained in more detail below) it is determined that, for example, address range R2 corresponds to failed quanta of data stored in block 2 of the MLC NAND flash memory module 26. FIG. 2B shows the quanta of data which failed the data integrity verification check (see FIG. 2A) remapped to the next available range of physical addresses within the SLC NAND flash memory module 28, in this example, SLC/block 0.

[0026] FIGS. 3A and 3B are a flow chart illustrating a method for utilizing a NAND flash memory system incorporating one embodiment of the present disclosure. The method begins in a step 100, when a command to write a quantum of data stored in DRAM to a particular location in NAND flash memory is received. In step 102, the quantum of data is read from DRAM into memory within the device controller (which acts as the memory controller). In step 104, both the logical address range and the NAND flash physical address range to which the quantum of data is to be written, is read into memory of the device controller. In step 106, the quantum of data to be written is combined with the contents of the NAND flash memory. In step 108, the NAND flash physical address range to be written is erased. In step 110, the combined data is written to

the appropriate NAND flash physical address range. In step 112 the NAND flash physical address range that was written in step 110 is read into device controller memory.

[0027] The flowchart continues in FIG. 3B. In step 114 the NAND flash physical address range that was read into device controller memory is compared with the retained data representing the combination of the previous contents of the physical address range and the quantum of data to be written. In step 116, if the retained data matches the newly stored data in the NAND flash memory, the write was a success, and the method exits in step 118. However, if the retained data does not match the newly stored data in the NAND flash memory, the method executes step 120, which identifies the next quantum of available SLC NAND flash memory addresses. In step 122, a check is made to determine if additional SLC NAND flash memory is available, and, if not, the NAND flash memory system is marked as failed, prompting a system alert step 124. However, if additional SLC NAND flash memory is available, the failed NAND flash physical address range is remapped to the next available quantum of SLC NAND flash memory in step 126. Execution then returns to step 110, where the write is repeated.

[0028] Another application of one embodiment of the present disclosure, not depicted in any of the drawings, is to allocate "hot" blocks; i.e., those blocks that receive frequent writes, into the SLC NAND flash memory module 28, while allocating "cold" blocks; i.e., those blocks that only receive infrequent writes, into the MLC NAND flash memory module 26. This could be accomplished within the device controller 14 described above, which could simply maintain a count of those blocks that are accessed (written to) most frequently, and, on a periodic basis, such as, for example, every 1000 writes, or every 10,000 writes, transfer the contents of those blocks into the SLC NAND flash memory module 28.

[0029] FIG. 4 depicts another embodiment of the present disclosure. The embodiment is entirely resident within a NAND flash module 50. In particular, a standard NAND flash interface 52 is managed by flash translation layer (FTL) logic 54. The flash translation layer (FTL) 54 manages two NAND flash memory banks 56 and 58, whereby memory bank 56 comprises a plurality of MLC NAND flash memory modules 60a and a plurality of SLC NAND flash memory modules 62a. Memory bank 58 comprises a plurality of MLC NAND flash memory modules 60b and a plurality of SLC NAND flash memory modules 62b.

[0030] This embodiment of the present disclosure could function similarly to the system level embodiment discussed earlier with reference to FIGS 1-3B, but the control functions, such as maintenance of the translation table/address map (FIGS. 2A and 2B), could be conducted within the flash translation layer (FTL) 54 instead of in a device controller 14.

[0031] Embodiments of the present disclosure relate to a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use of a combination of multi-level cell (MLC) and single-level cell (SLC) NAND flash storage. The above description is presented to enable one of ordinary skill in the art to make and use the disclosure and is provided in the context of a patent application and its requirements. While this disclosure contains descriptions with reference to certain illustrative aspects, it will be understood that these descriptions shall not be construed in a limiting sense. Rather, various changes and modifications can be made to the illustrative embodiments without departing from the true spirit, central characteristics and scope of the disclosure, including those combinations of features that are individually disclosed or claimed herein. Furthermore, it will be appreciated that any such changes and modifications will be recognized by those skilled in the art as an equivalent to one or more elements of the following claims, and shall be covered by such claims to the fullest extent permitted by law.

WHAT IS CLAIMED IS:

1. A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element;

at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements; and

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories.

2. The system of Claim 1, wherein the memory elements are a module, standalone device, or multi-chip package.

3. The system of Claim 1, wherein at least one of the volatile or nonvolatile memories are embedded in the at least one controller.

4. The system of Claim 1, wherein the nonvolatile memory is flash memory.

5. The system of Claim 1, wherein the nonvolatile memory is phase-change memory.

6. The system of Claim 1, wherein the nonvolatile memory is magnetic random access memory.

7. The system of Claim 1, wherein the volatile memory is dynamic random access memory.

8. The system of Claim 1, wherein the volatile memory is static random access memory.

9. The system of Claim 1, wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD).

ABSTRACT

A flash controller for managing at least one MLC non-volatile memory module and at least one SLC non-volatile memory module. The flash controller is adapted to determine if a range of addresses listed by an entry and mapped to said at least one MLC non-volatile memory module fails a data integrity test. In the event of such a failure, the controller remaps said entry to an equivalent range of addresses of said at least one SLC non-volatile memory module. The flash controller is further adapted to determine which of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and allocating those blocks that receive frequent writes to the SLC non-volatile memory module and those blocks that receive infrequent writes to the MLC non-volatile memory module.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	G.R. Mohan Rao	§	Conf. No.	6732
Serial No:	16/006,299	§	Group Art Unit:	2824
Filed:	June 12, 2018	§	Examiner:	Reidlinger, Ronald Lance

For: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Via EFS-Web
Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

The Applicant submits the following amendments and remarks in response to the Office Action dated January 24, 2019. If any extension of time for this Response is required, the Applicant requests that this be considered a petition therefore.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks begin on page 6 of this paper.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element;

at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements; ~~and~~

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein;

the controller performing a data integrity test on stored data in a given one of the MLC and SLC nonvolatile memory elements after any access operation is performed thereon;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

2. (Currently Amended) The system of Claim 1, wherein the memory elements are a software module, a hardware module, a standalone device, or multi-chip package.

3. (Currently Amended) The system of Claim 1, wherein at least one of the volatile or nonvolatile memory elements ~~memories~~ are embedded in the at least one controller.

4. (Currently Amended) The system of Claim 1, wherein the MLC and SLC nonvolatile memory elements comprise [[is]] flash memory.

5. (Currently Amended) The system of Claim 1, wherein the memory in the SLC and MLC nonvolatile memory elements is phase-change memory.

6. (Currently Amended) The system of Claim 1, wherein the memory in the SLC and MLC nonvolatile memory elements is magnetic random access memory.

7. (Currently Amended) The system of Claim 1, wherein the random access volatile memory element is dynamic random access memory.

8. (Currently Amended) The system of Claim 1, wherein the random access volatile memory element is static random access memory.

9. (Original) The system of Claim 1, wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD).

10. (New) The system of Claim 1, wherein the controller, upon detection of a failure of the data integrity test, remaps the data to the other of the MLC and SLC nonvolatile memory elements.

11. (New) The system of Claim 10, wherein the given one of the MLC and SLC nonvolatile memory elements is the MLC nonvolatile memory element.

12. (New) The system of Claim 10, wherein the SLC memory element has a higher endurance than the MLC memory element.

13. (New) The system of Claim 1, wherein the access operation is a Read operation.

14. (New) The system of Claim 1, wherein the access operation is a Write operation.

15. (New) The system of Claim 1, wherein the MLC is a 1 bit cell.

16. (New) The system of Claim 1, wherein the MLC is a multilevel cell, wherein the multilevel cell stores n bits per cell, wherein n is any integer greater than 1.

17. (New) The system of Claim 16, wherein the multilevel cell is a 3 bit cell.

18. (New) The system of Claim 16, wherein the multilevel cell is a 4 bit cell.

19. (New) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element;

at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

at least one controller to maintain an address table in one or more of the memory elements;

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein;

the controller performing a data integrity test on stored data in a given one of the MLC and SLC nonvolatile memory elements after any access operation is performed thereon;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

20. (Currently Amended) The system of Claim 19, wherein the memory elements are a software module, a hardware module, a standalone device, or multi-chip package.

21. (Currently Amended) The system of Claim 19, wherein at least one of the volatile or nonvolatile memory elements are embedded in the at least one controller.

REMARKS

Applicant has carefully reviewed the Office Action dated January 24, 2019. Applicant has amended Claims 1-8 and added new Claims 10-21 to more clearly point out the present inventive concept. No new matter has been added. Reconsideration and favorable action are respectfully requested.

Claim 1 has been amended to add the limitation wherein the controller is operable to perform a data integrity check after an access operation and, upon a failure of the data integrity check, remap the physical memory address space. Support for this can be found at paragraphs [0014], [0021], [0024], and [0025]. This remapping is for the purpose of endurance and, as such, after remapping, endurance will be increased. Further, new claims 10 – 21 further define this remapping as remapping from the MLC to the SLC, wherein the SLC is a higher endurance memory.

Claims 1 – 4 and 7 – 9 stand rejected under 35 U.S.C. §103(a) as unpatentable over the combination of Gorobets in view of Goodson. This rejection is respectfully traversed with respect to the claims as currently presented.

The Gorobets reference does not disclose or suggest a remapping operation wherein the remapping operation is for the purpose of improving the endurance. Rather, all that the Gorobets reference does is remap for wearability in accordance with a wearability algorithm. There is no integrity check that is performed for this operation. Further, there is no indication that the remapping of the physical address space will be from a memory element having a relatively lower endurance to another memory element having a relatively higher endurance. The Goodson reference does not cure this deficiency. Therefore, Applicant respectfully requests withdrawal of the 35 U.S.C. §103 rejection with respect to Claims 1 – 4 and 7 – 9.

Claim 5 has been rejected under 35 U.S.C. §103(a) in view of the additional reference Kund and Claim 6 has been rejected in view of the additional reference Chen. Claims 5 and 6 depend from Claim 1 and, therefore, for the reasons stated hereinabove, are believed to be allowable for the reasons described with respect hereinabove to Claim 1 and, therefore, Applicant respectfully requests withdrawal of the 35 U.S.C. §103 rejection with respect to Claims 5 and 6.

CONCLUSION

Applicant has now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicant respectfully requests full allowance of the claims as amended.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at patents@naifeh.com.

Recognizing that Internet communications are not secure, Applicant hereby authorizes the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application by video conferencing, instant messaging, or electronic mail. Applicant understands that a copy of these communications will be made of record in the application file.

Respectfully submitted,

/Bill R. Naifeh, Reg No. 44,962/

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under 37 CFR 1.34

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	RAO, G.R. Mohan
Serial No.:	16/006,299
Confirmation No.:	6732
Filed:	June 12, 2018
Group:	2824
Examiner:	REIDLINGER, Ronald Lance
For:	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

AMENDMENT

This communication is responsive to the Examiner's Office Action dated April 28, 2020. Reconsideration is respectfully requested.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.

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In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element that can be mapped into the MLC memory space;

at least one SLC nonvolatile memory element that can be mapped into the SLC memory space;

at least one random access volatile memory ~~element~~;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory;

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory ~~elements~~ for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;

the controller performing a data integrity test on stored data in ~~a given one of~~ the MLC ~~and SLC~~ nonvolatile memory element ~~elements~~ after [[any]] at least a Write access operation [[is]] performed thereon by comparing the stored data to the retained data in the random access volatile memory;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

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wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

2. (Previously presented) The system of Claim 1, wherein the FTL flash translation layer is a software module, or a firmware module containing software updates.

3. (Currently Amended) The system of Claim 1, wherein at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller.

4. (Previously presented) The system of Claim 1, wherein the MLC and SLC nonvolatile memory elements comprise flash memory.

5. (Cancelled)

6. (Cancelled)

7. (Currently Amended) The system of Claim 1, wherein the random access volatile memory ~~element~~ is dynamic random access memory.

8. (Currently Amended) The system of Claim 1, wherein the random access volatile memory ~~element~~ is static random access memory.

9. (Cancelled)

10. (Currently Amended) The system of Claim 1, wherein the controller, upon detection of a failure of the data integrity test, remaps the data to the ~~other of the MLC and~~ SLC nonvolatile memory element ~~elements~~.

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11. (Cancelled)

12. (Previously presented) The system of Claim 10, wherein the SLC memory element has a higher endurance than the MLC memory element.

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Currently Amended) The system of Claim 1, wherein the MLC is a multilevel cell, wherein the multilevel cell stores [[n]] at least 2 bits per cell~~, wherein n is any integer greater than 1~~.

17. (Cancelled)

18. (Cancelled)

19. (Currently Amended) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space, and to maintain an address table in one or more of the memory elements;

at least one MLC nonvolatile memory element that can be mapped into the nonvolitile memory space;

at least one SLC nonvolatile memory element that can be mapped into the nonvolitile memory space;

at least one random access volatile memory ~~element~~;

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the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory ~~elements~~ for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;

the controller performing a data integrity test on stored data in ~~a given one of~~ the MLC ~~and SLC~~ nonvolatile memory element ~~elements~~ after [[any]] at least a Write access operation [[is]] performed thereon by comparing the stored data to the retained data in the random access volatile memory;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Currently Amended) The system of Claim 1, wherein the contents of frequently accessed ~~requests to~~ portions of the memory space ~~due to read or write, or read, modify, or write,~~

~~or data moves which contain frequent erases~~ are periodically moved from the MLC space to the SLC space.

26. (New) The system of Claim 1 wherein the MLC allows a single cell to store multiple bits.

REMARKS

Applicant has carefully reviewed the Office Action dated April 28, 2020. Applicant has amended claims 1, 3, 7, 8, 10, 16, 19, and 25. Claims 9, 13, 14, 17, 18, and 22-24 have been cancelled. New claim 26 has been added. Reconsideration and favorable action is respectfully requested.

I. Interview Summary

Applicant thanks the Examiner for the telephone interview conducted on October 7, 2020. Applicant was represented by Tim Bliss (#50,925), Greg Howison (#30,646), and inventor Mohan Rao. Amendments to claims 1 and 19 were discussed with respect to the prior art reference *Oribe*, as well as support for the amendments. No final conclusion was reached as to allowability of the amended claims, with the Examiner reserving the right for further search and consideration.

II. Rejections under 35 U.S.C. §112, first paragraph

All claims rejected under §112, first paragraph, have been cancelled except for Claim 25. Claim 25 has been amended to clarify the scope of the claim. Claim 25 is supported, for example, in paragraph [0028] of the specification. Accordingly, Applicant respectfully requests that the rejection of Claim 25 under §112, first paragraph, be withdrawn.

III. Rejections under 35 U.S.C. §112, second paragraph

All claims rejected under §112, second paragraph, have been cancelled except for Claim 25. Claim 25 has been amended to address the rejected elements. Accordingly, Applicant respectfully requests that the rejection of Claim 25 under §112, second paragraph, be withdrawn.

IV. Rejections under 35 U.S.C. §103

A. Claims 1-4, 7-10, 12-14, and 16-19

Claims 1-4, 7-10, 12-14, 16, 17, and 19 stand rejected under 35 USC §103(a) as being unpatentable over combinations of *Gorobets* in view of *Goodson* and *Oribe*. This rejection is respectfully traversed with respect to the claims as currently amended.

The Examiner has stated that the one element missing from the primary references, *Gorobets* in view of *Goodson,* is a lack of performing a data integrity check. The relies upon *Oribe* for the support of this element. In view of the newly added limitations to Claims 1 and 19, this rejection is respectfully traversed.

Claims 1 and 19, as amended, include the following limitation:

> *the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;*
>
> *the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory;*

This limitation requires that the nonvolatile memory element "retain" the stored data and then, during a data integrity test, the stored data for a Write access is "compared" to the stored data. Support for these amendments is found, for example, in paragraph [0027] and Fig. 3B.

This is to be contrasted with the refresh operation of *Oribe*, in which, in response to some determination that a bit error rate has exceeded a certain threshold, data will be remapped or moved from that block of memory to another block. There is no comparison operation, as that is

not required in order to determine the bit error rate of data. All that is required is to merely analyze the data and the error correction bits to determine the bit error rate.

In the currently amended claims, the actual data that is being written to the memory is retained in nonvolatile memory and then written to memory. This data is subsequently read from the memory and compared to the retained data. This operation is not some operation that can be carried out by a conventional cache, as that cache is typically only designed to handle one block of data. In the nonvolatile memory, in order to facilitate a compare operation, if an entire block is being written to with new data, that entire block has to be retained in one portion of the memory and then written to the memory, followed by a subsequent Read of the memory, requiring that block of data to be placed in an additional area of the nonvolatile memory, thus requiring at least two blocks of memory space in the nonvolatile memory. A refresh operation only requires one block of data cache.

Oribe does not disclose or suggest any type of compare operation as part of the data integrity operation. The refresh operation does not in any way "retain" data in any type of data cache for the purposes of a refresh operation.

Applicant submits that neither *Gorobets* nor *Oribe* can remap the address space to a different physical range of addresses "and transfer of data corresponding to the stored data to those remapped physical addresses." *Oribe* can only determine that a block of Flash memory has failed but, after such a determination, any data stored therein is lost. Since the operation of a Flash memory after accessing data therefrom requires an Erase operation, it is this Erase operation that provides the most stress on the Flash memory, thus causing a particular section to fail. Since neither *Gorobets* nor *Oribe* retain the data to be written for later comparison, neither suggests nor discloses such an operation, either singly or in combination. *Goodson* fails to remedy this deficiency.

Claims 2-4, 7, 8, 10, 12, 16, and 25 depend from and further limit claim 1, and therefore are allowable for at least the same reasons as claim 1.

B. New claim 26

Support for new claim 26 is found, for example, in paragraph [0010], second sentence. Claim 26 depends from and further limits claim 1, and therefore is allowable for at least the same reasons as claim 1.

V. Conclusion

For the reasons described above, Applicant submits that all pending claims are in condition for allowance. If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at tim@naifeh.com.

Recognizing that Internet communications are not secure, Applicant hereby authorizes the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application by video conferencing, instant messaging, or electronic mail. Applicant understands that a copy of these communications will be made of record in the application file.

Respectfully submitted,

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