

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PHISON ELECTRONICS CORPORATION,
Petitioner,

v.

VERVAIN, LLC,
Patent Owner.

PGR2024-00047
U.S. Patent No. 11,830,546

PATENT OWNER'S PRELIMINARY RESPONSE

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EXHIBIT LIST

Exhibit No.	Description
2001	Declaration of Dr. Sunil Khatri
2002	Chen et al., <i>Ultra MLC Technology Introduction</i> , Advantech Technical White Paper (Oct. 5, 2012) (“Chen”)
2003	Excerpts from Micheloni et al., <i>Inside NAND Flash Memories</i> (1 st ed. 2010) (“Micheloni”)
2004	<i>Vervain, LLC v. Phison Electronics Corporation</i> , No. 1:24-CV-259-ADA, Dkt. 37 (W.D. Tex. Nov. 27, 2024) (Joint Claim Construction Statement)
2005	Phison’s Exhibit E Claim Chart, served with its Preliminary Invalidity Contentions on August 16, 2024 in <i>Vervain, LLC v. Phison Electronics Corporation</i> , No. 1:24-CV-259-ADA (W.D. Tex.)
2006	<i>Vervain v. Western Digital Corp. et al.</i> , No. 6:21-cv-488-ADA, Dkt. 41 (W.D. Tex. Jan. 24, 2022) (Claim Construction Order)
2007	U.S. Patent App. No. 2007/0271609 assigned to Phison Electronics Corp.
2008	Patent Office Subject Matter Eligibility Guidance Examples 1-36
2009	U.S. Patent Application Pub. No. 2011/0099460 (“Dusija”)
2010	Highlighted Version of U.S. Patent No. 8,634,240 (“Gavens”), indicating which material from Gavens is also present in U.S. Patent Application Pub. No. 2011/0099460 (“Dusija”)
2011	<i>Micron Technology, Inc., v. Vervain, LLC</i> , IPR2021-01550, Ex. 1009 (P.T.A.B. Sept. 21, 2021) (expert declaration challenging the validity of U.S. Patent No. 10,950,300)
2012	U.S. Patent No. 8,194,452 to G. R. Mohan Rao (incorporated by reference by the 546 Patent)

Exhibit No.	Description
2013	Oxford Dictionary of Computing (Sixth Edition, 2008) (page 312, defining “memory element”)
2014	U.S. Patent App. No. 2010/0186084 currently assigned to Kingston Digital, Inc.
2015	Microsoft Computer Dictionary (5 th ed. 2002)
2016	Micron’s Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,950,300, IPR2021-01550, Sept. 21, 2021 (“300 petition”)
2017	“Maximize.” Merriam-Webster.com Thesaurus, Merriam-Webster, https://www.merriam-webster.com/thesaurus/maximize . Accessed 24 Nov. 2021.
2018	<i>Vervain, LLC v. Phison Electronics Corporation</i> , No. 1:24-CV-259-ADA, Dkt. 16 (W.D. Tex. Jul. 15, 2024) (agreed scheduling order)
2019	<i>Vervain, LLC v. Phison Electronics Corporation</i> , No. 1:24-CV-259-ADA, Dkt. 40 (W.D. Tex. Dec. 16, 2024) (Order Resetting Zoom Markman Hearing to January 9, 2025)
2020	Docket Sheet for <i>Vervain, LLC v. Phison Electronics Corporation</i> , No. 1:24-CV-259-ADA (W.D. Tex.)
2021	“Judge Albright Patent FAQ,” https://www.txwd.uscourts.gov/for-attorneys/judge-albright-courtroom-faq/ . Accessed December 18, 2024)
2022	Phison’s Preliminary Invalidity Contentions served on August 16, 2024 in <i>Vervain, LLC v. Phison Electronics Corporation</i> , No. 1:24-CV-259-ADA (W.D. Tex.)
2023	Judge Albright’s Standing Order Governing Proceedings (OGP) 4.4—Patent Cases, Filed January 23, 2024.
2024	Excerpts from the Prosecution History of U.S. Patent No. 11,830,546
2025	U.S. Patent App. Pub. No. 2011/0096601 to Gavens et al.

I. INTRODUCTION

Vervain, LLC (“PO” or “Vervain”) submits this Preliminary Response in accordance with 35 U.S.C. § 323 and 37 C.F.R. § 42.207, responding to the Petition for Post Grant Review (PGR) (Paper 2) of U.S. Patent No. 11,830,546 (“546 Patent” or “the Challenged Patent”) filed by Phison Electronics Corporation (“Phison” or “Petitioner”). The Petition includes four grounds of unpatentability challenging claims 1-7 (“Challenged Claims”). The first three grounds include cursory challenges under 35 U.S.C. §§ 101, 112(a), and 112(b). The fourth ground relies on single-reference obviousness based on U.S. Patent No. 8,634,240 (“Gavens”) (Ex. 1045). All of these grounds fall far short of the mark for the reasons below.

First, the Board should exercise its discretion and deny institution under 35 U.S.C. § 324(a). The parties are already litigating a parallel case in district court, which involves the Challenged Patent and seven others. The parallel case is well past its infancy. Before the institution decision is due in this PGR proceeding, the district court will have already held the *Markman* hearing, and the parties will be halfway through fact discovery. At the *Markman* hearing, the Court will rule on most of the indefiniteness challenges Petitioner makes again here. And trial in the district court case is scheduled for three months before the final written decision deadline here. Furthermore, Petitioner asserts overlapping grounds in district court,

but has not stipulated to any estoppel if the Petition is instituted. The advanced parallel proceeding should proceed, and this Petition should be denied.

Second, the Board should deny institution because Petitioner's grounds lack merit. All the grounds are cursory and lack adequate explanation and/or are internally inconsistent. Additionally, Petitioner's obviousness arguments have already been rejected by the Patent Office and should not be reconsidered now. *See* 35 U.S.C. § 325(d). Petitioner has not established that it is more likely than not that it will prevail on any ground. *See* 35 U.S.C. § 324(a).

Accordingly, PO requests that the Board deny institution of the Petition.

II. OVERVIEW OF THE CHALLENGED PATENT AND THE CHALLENGED CLAIMS

The Challenged Patent, entitled "Lifetime Mixed Level Non-Volatile Memory System" was filed on March 16, 2021 and has an effective filing date of July 19, 2011. Ex. 1001. Dr. G. R. Mohan Rao is the sole named inventor of the Challenged Patent.

At a high level, the Challenged Patent describes a reliable flash memory storage system combining both single-level cell (SLC) and multi-level cell (MLC)

non-volatile memories.¹ Ex. 1001, Abstract; Ex. 2001, ¶37. Prior to the Challenged Patent, Dr. Rao recognized that “MLC NAND flash SSDs are slowly replacing and/or coexisting with SLC NAND flash in newer SSD systems” because “MLC flash memory is less expensive than SLC flash memory[] on a cost per bit basis.” Ex. 1001, 3:27-28, 5:41-44. However, while “MLC NAND flash enjoys greater density than SLC NAND flash” it comes “at the cost of a decrease in access speed and lifetime (endurance).” *Id.*, 3:32-35. As a result, various hybrid systems combining SLC and MLC (among others) are taught in the Challenged Patent, to combine the benefits of both types of non-volatile flash storage at a low cost. *Id.*, 3:53-60.

The Challenged Patent addresses improvements and solutions for managing the writing of data optimally for improved reliability and lifetime (endurance) of such hybrid memory systems. *Id.*, 3:53-60. Specifically, the Challenged Claims are directed to specific techniques for efficiently using SLC and MLC flash to improve the overall performance of the memory. *Id.*, claim 1. For example, if data stored in the MLC fails a data integrity test, then it is transferred to higher-performance SLC

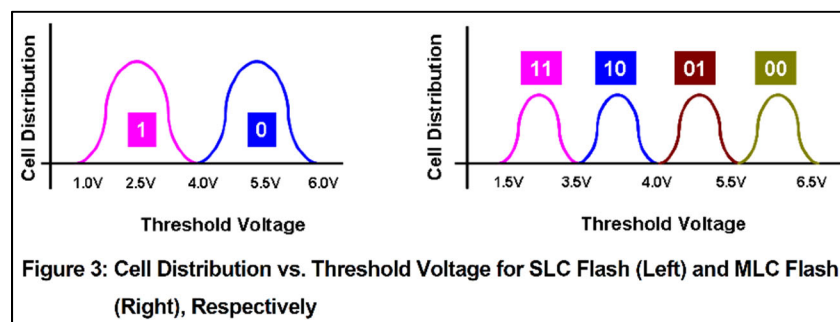
¹ Non-volatile memories can store information even after the system is powered off. Flash memory is a specific type of non-volatile memory, where data is stored in “blocks” of “pages.” Ex. 1001, 2:43-50; Ex. 2001, ¶27.

or less-used MLC. *Id.* By doing so, the number of errors is reduced, and overall endurance of the memory is increased. Ex. 1001, 3:58-60.

A. SLC and MLC Flash

SLC memory stores 1 bit per cell, and MLC memory stores more than 1 bit per cell. Ex. 1001, 2:5-11; Ex. 2001, ¶¶32-34. As noted above, there are pros and cons to SLC and MLC flash. In general, SLC is faster and less prone to errors, but requires more space and power to store a given amount of data. Ex. 1001, 1:48-53. The opposite is true of MLC. MLC flash is slower and more prone to errors, but stores data more densely with less power consumption. *Id.*, 3:32-35.

SLC and MLC flash memories both use the same type of transistor called a floating gate transistor. *Id.*, 3:41-44. They both store a charge in the floating gate of each transistor (cell), which changes the threshold voltage of the transistor. Ex. 2001, ¶32. The memory uses the threshold voltage to determine what bit, or bits, were stored in the transistor. The MLC cell in the figure below illustrates threshold voltages for a 2-bit MLC cell.



Ex. 2002, 3.

The primary difference between SLC and MLC is what data each threshold voltage represents. Ex. 2001, ¶33. With SLC flash, the transistor stores only a 1 or 0, so a wide range of threshold voltages can be allotted to a single bit. Ex. 1001, 3:29-30. This allows for faster and more reliable memory access. On the other hand, MLC flash must be slowly and carefully programmed to a narrower, more precise range of threshold voltages, with each threshold voltage range representing a specific pair of bits (*see* figure above, which shows four pairs of bits—11, 10, 01, and 00—corresponding to smaller ranges of threshold voltages compared to the SLC). Ex. 1001, 3:30-32.

B. Address Table

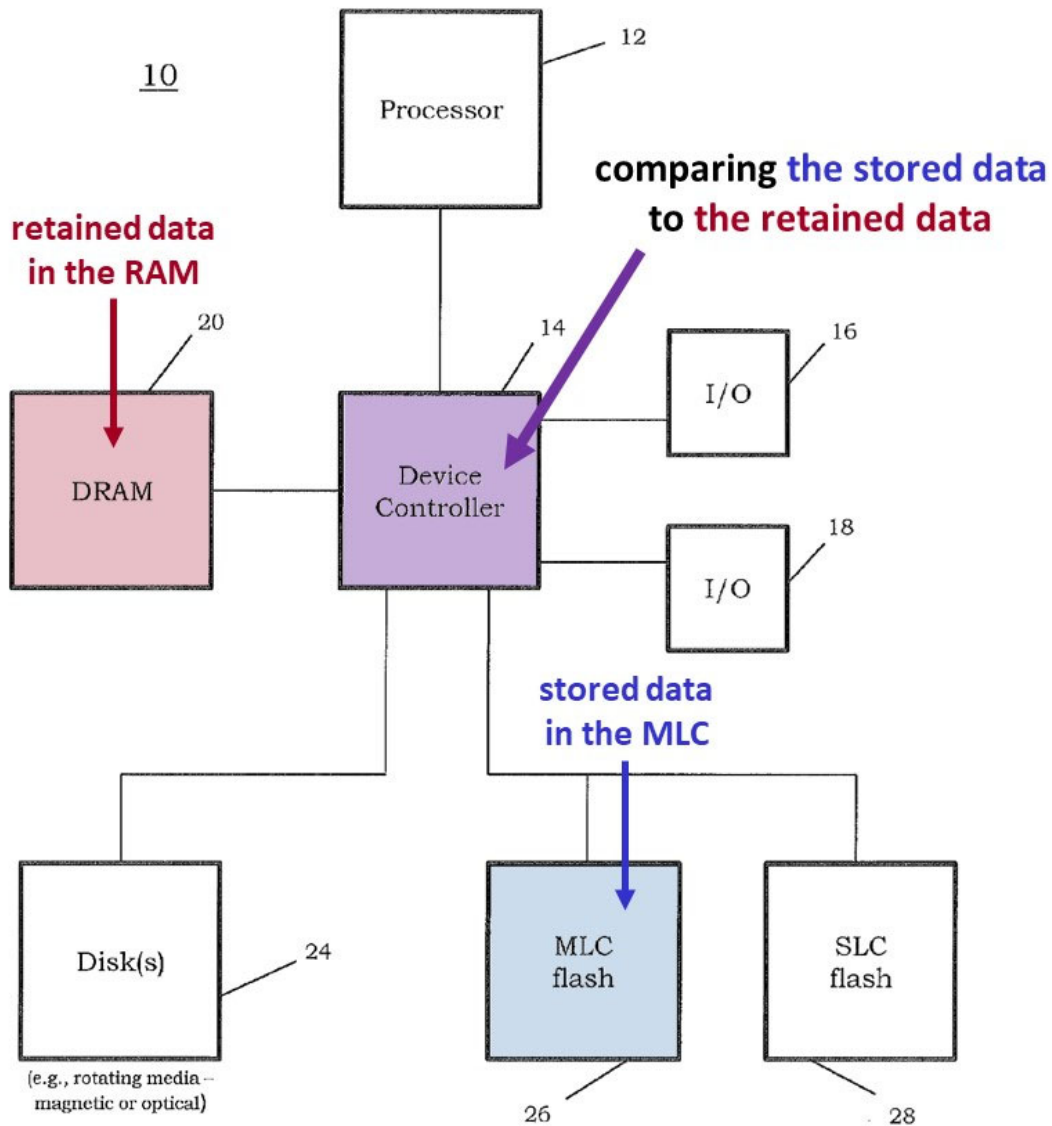
To provide wear leveling, garbage collection, and bad block management, a translation layer is used to map logical addresses to actual physical memory locations. Ex. 2003, 40-42; Ex. 1001, 2:61-3:26; *see also* Ex. 2001, ¶35. As part of this translation layer, “tables are widely used in order to map sectors and pages from logical to physical.” Ex. 2003, 40; Ex. 1001, 3:10-14. These tables map logical blocks to physical blocks. Ex. 2003, 40-42; Ex. 1001, 3:10-14. Using a “block” or similar granularity is important, since flash memory is arranged so that when erasing and rewriting data, a whole block is “erased together.” Ex. 2003, 22; Ex. 1001, 2:50-60. Dr. Rao explained that “[t]he address ranges within the translation table will assume some minimum quantum, such as, for example, one block....” Ex. 1001,

5:44-48. Dr. Rao further explained that memory is written and mapped on the granularity of a “quantum,” such as a block or page. *Id.*, 5:44-48; Figs. 3A-B.

C. Data Integrity Tests

As mentioned above, when data is stored in MLC memory, it is more prone to errors, and some data is more prone to errors than other data. Ex. 2001, ¶36. One reason for this is that the threshold voltage intervals for MLC memory are smaller than the intervals for SLC memory, and thus, errors can occur when writing or reading the data. *Id.*, ¶36. Errors can also be caused by the data stored in neighboring cells. *Id.* A data integrity test checks the integrity of the data (*i.e.*, whether errors have occurred). This test can be run immediately after data is written, or at a later time. If the test reveals a problem such as corrupt data, the data can be remapped to SLC (which is less error-prone), and the address table is modified accordingly. Ex. 1001, 4:20-26. Alternately, MLC data can be remapped to other MLC blocks, and the address table is then modified accordingly. *Id.*, 3:4-26.

The Challenged Patent claims a particular way of writing the data to the MLC and performing the data integrity test. Dr. Rao recognized that there were advantages in using a dynamic random access memory (DRAM) to assist with both the write access operation and data integrity test. As seen in Figure 1 below, the controller (purple) controls a DRAM (red).

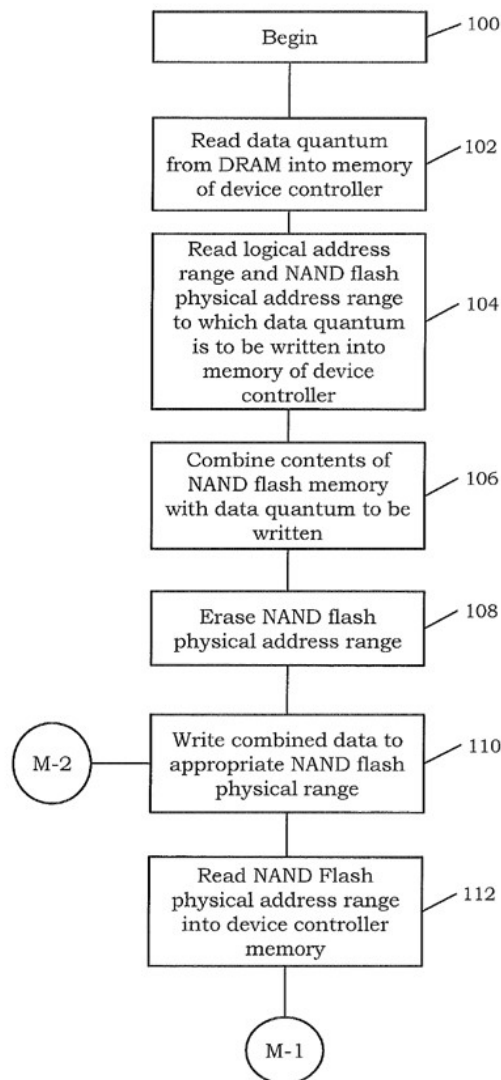


Ex. 1001, Fig. 1 (annotations added²), 5:24-25. The DRAM is used during a write access operation to the MLC flash (highlighted blue). The data to be written to the MLC flash is maintained (or retained) in the DRAM. Ex. 1001, 5:49-51. If time permits, the controller performs a data integrity test on the data that was stored in

² Unless otherwise noted, PO added coloring to Figures.

the MLC. *Id.*, 5:51-54. If the stored data fails the data integrity test, the address range for the stored data is remapped to a new location (*e.g.*, the SLC flash). *Id.*, 5:54-57.

Figures 3A and 3B show in more detail how the DRAM is used during the write access operation and data integrity test.



Id., Fig. 3A. The write access operation begins at step 100. *Id.*, 6:7-10. In step 102, the data to be written to the MLC is read from the DRAM into the controller memory.

Id., 6:10-12. In step 104, the controller obtains the logical and physical address ranges for the data to be written to the MLC. *Id.*, 6:12-15. In step 106, the controller combines the data from the DRAM with data from the MLC. *Id.*, 6:15-18. In step 108, the controller erases the physical address range where the data is being written. *Id.*, 6:18-19. Finally, in step 110, the combined data is written to the MLC flash. *Id.*, Fig. 3A (step 110), 6:19-21.

The data integrity test begins at the bottom of Figure 3A and continues to Figure 3B. In step 112, the data that was stored in the MLC (“the stored data”) is read into the controller memory. *Id.*, 6:21-23. In step 114, the stored data is compared to the data that was retained in the DRAM (“the retained data”). *Id.*, 6:24-29.

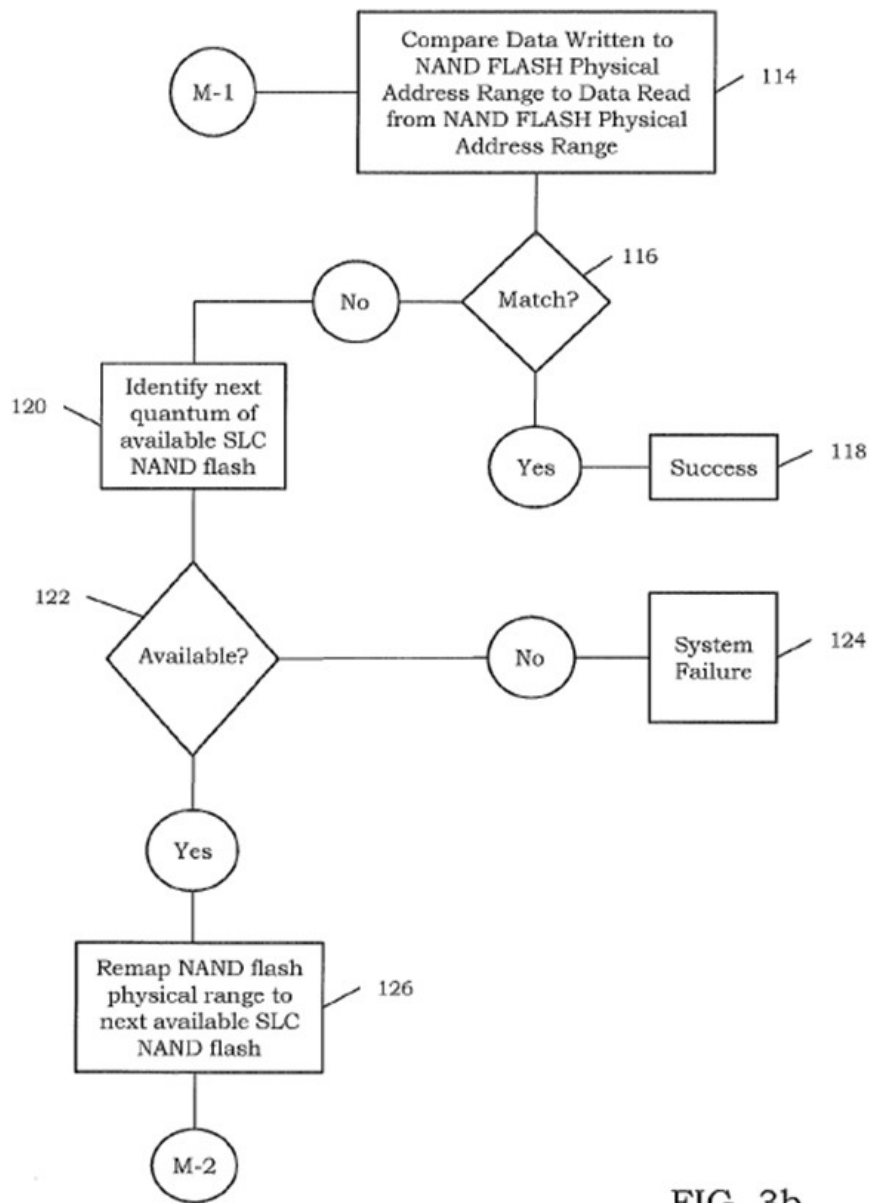


FIG. 3b

Id., Fig. 3B. If there is a match, the data was successfully stored in the MLC. *Id.*, 6:29-31. If not, the retained data is written to another location (*e.g.*, SLC). *Id.*, 6:31-35.

D. Claim 1

Claim 1 of the Challenged Patent requires a system for storing data comprising: (1) non-volatile MLC memory; (2) non-volatile SLC memory; (3) random access volatile memory (highlighted red); and (4) controller memory. The random access volatile memory is a key feature of the invention and it permeates most of the elements of the claim ([1a], [1d], [1f]-[1h]). As discussed above, the random access volatile memory is particularly important to the “Write access operation” in [1f] and the “data integrity test” in [1g].

Claim 1	
[1Pre]	A system for storing data comprising:
[1a]	[1a1] memory space containing volatile memory space and [1a2] nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space;
[1b]	at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements;
[1c]	a bank of nonvolatile memory, including: [1c1] a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and [1c2] at least one SLC memory module including at least one SLC nonvolatile memory element;

[1d]	at least one random access volatile memory element ;
[1e]	a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements;
[1f]	the controller [1f1] having associated controller memory for storing received data therein, the controller [1f2] controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored data, the controller, [1f3] in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, [1f4] operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data;
[1g]	the controller [1g1] performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by [1g2] reading the stored data to the controller memory and [1g3] comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that

	was associated with the stored data in the random access volatile memory by the controller during the Write access operation;
[1h]	wherein [1h1] the address table maps logical and physical addresses adaptable to the system, wherein [1h2] the mapping is performed as necessitated by the system to maximize lifetime, and wherein [1h3] the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and
[1i]	wherein a failure of the data integrity test performed on the stored data by the controller results in [1i1] a remapping of address space to a different physical range of addresses and [1i2] transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test.

In [1f1], the controller stores received data in the controller memory. In the Write access operation of [1f3-1f4], the data is transferred to two places: to the MLC non-volatile memory as “stored data” and to the random access volatile memory as “retained data.”

After data is written to the MLC in the Write access operation, the controller performs a data integrity test to determine whether the data has any errors ([1g]). To do so, the controller reads the “stored data” to the controller memory ([1g2]) and

compares this data to the “retained data” in the random access volatile memory ([1g3]).

III. PERSON OF ORDINARY SKILL IN THE ART

For purposes of this preliminary response only, PO adopts Petitioner’s definition of a person of ordinary skill in the art (POSA). Petition, 22-23; Ex. 2001, ¶¶22-26.³

IV. CLAIM CONSTRUCTION⁴

Petitioner proposed construction of three terms: “MLC memory modules,” “SLC memory modules,” and “comparing.” Petition, 23-28. PO disagrees with Petitioner’s proposed constructions, but construction of these terms is not necessary to resolve the parties’ dispute regarding whether institution should be granted. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). Accordingly, PO does not contest Petitioner’s proposed constructions for the limited purpose of this Preliminary Response.

Notably, for “SLC memory modules” and “MLC memory modules,” Petitioner Phison proposes a *different* construction here than it proposes in district

³ PO submits the declaration of Dr. Sunil Khatri, an expert in the field of the Challenged Patent. Ex. 2001, ¶¶4-26.

⁴ PO addresses the indefiniteness grounds separately in Section VIII below.

court. *Compare* Petition, 24 *with* Ex. 2004, 2-3. Yet neither of Phison’s constructions makes sense. The district court has already construed “SLC non-volatile memory” and “MLC non-volatile memory” in related litigation to refer to “nonvolatile memory that stores one bit bits of information per cell” and “nonvolatile memory that stores multiple bits of information per cell.” Ex. 2006 at 2. Phison’s proposals, which refer to the presence of certain circuitry rather than the number of bits stored per cell, are inconsistent with the court’s prior construction and should be rejected.

V. THE BOARD SHOULD EXERCISE ITS DISCRETION AND DENY INSTITUTION UNDER 35 U.S.C. § 324(a)

The Board should exercise its discretion and deny institution on all grounds because of the significant overlap with the parallel district court litigation, as well as prior litigation that has already rejected some of Petitioner’s indefiniteness arguments. *See* Exs. 2004, 2006.

The parties are engaged in parallel district court litigation that is significantly underway. Petitioner filed its Petition on August 27, 2024. Five months prior—on March 8, 2024—PO filed a complaint against Phison asserting infringement of the Challenged Patent, among related patents, in the United States District Court for the Western District of Texas. *See* Ex. 1060; *see also* Ex. 1062 (asserting eight patents, including the Challenged Patent) (hereinafter, the “Parallel Litigation”). In the Parallel Litigation, the parties completed *Markman* briefing, and the Court (with

Judge Albright presiding) scheduled a *Markman* hearing for January 9, 2025. *See* Ex. 2019. Fact discovery opened on December 9, 2024, and trial is scheduled to begin on December 15, 2025. *See* Ex. 2018.

As shown below, the *Fintiv* factors weigh in favor of denying institution on all grounds. *See NXP USA, Inc. v. Impinj, Inc.*, PGR2022-00005, Paper 18 at 7 (P.T.A.B. May 2, 2022) (weighing *Fintiv* factors and denying institution under 35 U.S.C. § 324(a)).

A. Factor 1: The Parallel Litigation Has Not Been Stayed And Is Unlikely To Be Stayed Even If This Petition Is Instituted

This factor weighs against institution because a stay of the Parallel Litigation is highly unlikely. Petitioner has not sought a stay, and the Board’s institution decision is expected by March 24, 2025. Given the timing and complexity of the Parallel Litigation, it is improbable that Judge Albright would grant a stay even if the Petition is instituted.

Particularly, March 2025 is months after the currently scheduled *Markman* hearing, and Judge Albright will likely have issued a *Markman* order by that time. *See* Ex. 2019. Fact discovery, which opened on December 9, 2024, will be significantly advanced. *See* Ex. 2018. Accordingly, the Court will have “expended significant resources,” and would be unlikely to grant a stay. *See, e.g., Sonrai Memory Ltd. v. LG Elecs. Inc.*, No. 6:21-CV-00168-ADA, 2022 WL 2307475, at *3

(W.D. Tex. June 27, 2022) (denying stay when *Markman* hearing was held two weeks before institution decision).

Further, in the Parallel Litigation, PO asserted *eight patents* against Phison. *See* Ex. 1062. Petitioner filed IPR and PGR petitions against *only six of those patents*—leaving two patents unchallenged, with no potential overlap with Board proceedings (should any be instituted). Additionally, the Board is unlikely to decide whether to institute four of these pending petitions, which have not yet been accorded filing dates, until at least June 2025. *See* IPR2025-00212, IPR2025-00213, IPR2025-00214, IPR2025-00215. This would be only weeks before the currently scheduled close of fact discovery on July 7, 2025. *See* Ex. 2018. Finally, the first final written decision (if any) across the various petitions (that of this Petition) would likely issue by March 24, 2026—months *after* the currently scheduled trial date of December 15, 2025. *See* Ex. 2018. In circumstances such as these, it is unlikely that the Court would grant a stay. *See Smart Mobile Techs. LLC v. Apple Inc.*, No. 6:21-CV-00603-ADA, 2023 WL 5051374, at *6 (W.D. Tex. Aug. 8, 2023) (denying stay based on instituted IPRs when institution was not granted on all asserted patents).

Thus, Factor 1 weighs against institution.

B. Factor 2: The Board Would Likely Issue A FWD More Than Three Months After Trial

This factor weighs against institution because trial is scheduled to begin more than three months before the projected final written decision. The Board is expected to decide whether to institute by March 24, 2025. Accordingly, the projected statutory deadline for a final written decision would be March 24, 2026—more than three months after the December 15, 2025 trial date. *See* Ex. 2018. Judge Albright is highly unlikely to move this trial date, as he has a practice of “not mov[ing] the trial date except in extreme situations.” Ex. 2021; *see also* *NXP USA*, PGR2022-00005, Paper 18 at 9 (weighing factor 2 in favor of discretionary denial when “the currently scheduled trial in the parallel proceeding is scheduled to begin over two months before our deadline to reach a final decision”).

C. Factor 3: The Court And Parties Have Invested Heavily In The Parallel Litigation

This factor weighs against institution because the parties and the Court have invested and will continue to invest significant resources in the Parallel Litigation. The Board weighs “the amount and type of work already completed in the parallel litigation by the court and the parties at the time of the institution decision.” *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 9 (P.T.A.B. Mar. 20, 2020) (“*Fintiv*”).

By the time the Board decides whether to institute this PGR in March 2025, the parties will have completed *Markman* briefing (Nov. 22, 2024); briefed a motion to dismiss (which the Court resolved on Dec. 2, 2024); held a *Markman* hearing (Jan. 9, 2025); and exchanged final infringement and invalidity contentions (Jan. 31, 2025). Exs. 2018, 2019, 2020. And given its practice of issuing *Markman* orders at or shortly after *Markman* hearings, the District Court will almost certainly have issued its *Markman* order well before March 2025, which will address most of the indefiniteness grounds raised by the Petitioner here. *See* Ex. 2004; *infra* Section V.D (explaining the overlap between the indefiniteness arguments in the Parallel Litigation and this proceeding).

Additionally, fact discovery began on December 9, 2024, and closes July 7, 2025. Ex. 2018. By March 2025, the estimated institution decision date, the parties will be halfway through fact discovery, will have exchanged numerous documents, and will have likely begun depositions.

Thus, the Court and the parties have invested and will continue to invest significant resources in the Parallel Litigation and, accordingly, this factor weighs against institution. *See NXP USA*, PGR2022-00005, Paper 18 at 9-10 (weighing factor 3 in favor of discretionary denial where the *Markman* hearing and the service of final infringement and invalidity contentions occurred before the Board's institution decision deadline).

D. Factor 4: There Is Significant Overlap Between Issues Raised In This Petition And In The Parallel Litigation

This factor weighs against institution given the significant overlap between the Petition and the Parallel Litigation. The Parallel Litigation involves the same 546 Patent as this proceeding, along with seven additional patents. The Parallel Litigation already involves or will likely involve each of the grounds raised in the Petition. For example, the indefiniteness grounds raised in Grounds 3.A through 3.E have all been raised in district court and are fully briefed, and will likely be ruled upon at the Court’s January 9, 2025 *Markman* hearing. Other grounds—such as patent eligibility, written description, and obviousness—have similarly been raised in Petitioner Phison’s invalidity contentions in district court.

Ground 1 § 101: Petitioner Phison’s preliminary invalidity contentions argue that the claims are ineligible under § 101 because they are allegedly directed to an abstract “memory space.” Ex. 2022 (Phison’s preliminary invalidity contentions), 27-28. Petitioner makes the same argument here in ground 1.

Ground 2 § 112(a): While Phison has only served its *preliminary* invalidity contentions, those contentions already identify the same § 112(a) challenges addressed below in grounds 2.A-2.E. *See* Ex. 2022, 9 (“memory space,” ground 2.A), 9-10 (“memory element,” ground 2.B), 13-14 (“mapping...” limitation, ground 2.C), 19-20 (“failed data,” ground 2.D), 26 (“single block,” ground 2.E).

Ground 3 § 112(b): Indefiniteness is an issue of claim construction. The parties already completed *Markman* briefing, and a *Markman* order is expected in January 2025. The Court will determine whether the terms identified in grounds 3.A-3.E are indefinite at that time. *See* Ex. 2004 (joint claim construction chart, identifying the claim terms being construed in the Parallel Litigation).

Additionally, while Petitioner’s ground 3.E is not addressed in the parties’ *Markman* briefing, this was Petitioner’s choice. Phison could have requested that the Court also consider whether this term is indefinite at the *Markman* hearing but chose not to do so. *See* Ex. 2023, 7 (permitting parties to seek “leave of Court” to request construction of additional terms). Even so, Phison still identified ground 3.E in its preliminary invalidity contentions (*see* Ex. 2022, 18-19) and could attempt to later raise this ground with the Court.

Ground 4 § 103: The Parallel Litigation involves the same Gavens reference that Petitioner relies on in ground 4. Gavens is the *only primary reference* identified for the 546 Patent in Phison’s Preliminary Invalidity Contentions. Ex. 2022, 6-7. And Phison charted Gavens to the claims. Ex. 2005 (charting Gavens to the 546 Patent, including the allegedly incorporated reference—Gorobets, Chen, Lee, and Paley—cited in Petitioner’s ground).

Despite this significant overlap, ***Petitioner has not filed a Sotera stipulation or any other stipulation*** to mitigate concerns of duplicative efforts between the

District Court and the Board, as well as any concerns regarding potentially conflicting decisions. *See Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 19 (P.T.A.B. Dec. 1, 2020). Notably, the District Court will already have decided most of the indefiniteness grounds in the Petition at the *Markman* hearing in January 2025—long before the final written decision of this PGR.

Thus, this factor weighs heavily against institution. *See NXP USA*, PGR2022-00005, Paper 18 at 11-12 (weighing factor 4 in favor of discretionary denial when the petitioner “d[id] not offer a stipulation” and “assert[ed] the same prior art in both proceedings”).

E. Factor 5: The Parties Are The Same In Both Proceedings

The Petitioner and the defendant in the Parallel Litigation “are the same party[.]”, so “this factor weighs in favor of discretionary denial.” *NXP USA*, PGR2022-00005, Paper 18 at 12.

F. Factor 6: The Merits Of The Petition Are Not Strong

As demonstrated below in Sections VI-IX, the merits of the Petition are weak. Thus, this factor weighs against institution.

G. Additional Considerations

Finally, Petitioner has filed six separate petitions (PGR2024-00047; PGR2024-00048; IPR2025-00212, IPR2025-00213; IPR2025-00214; IPR2025-00215) challenging six of the eight patents asserted in the Parallel Litigation. The

goal of discretionary denial under is to “allay[] concerns about inefficiency and duplication of efforts.” *Fintiv* at 6. Instituting six separate PGRs/IPRs to address only some of the issues currently being addressed in the single, mature district court case is inefficient and a considerable waste of resources.

Thus, all *Fintiv* factors weigh against institution, and the Board should exercise its discretion to deny institution under 35 U.S.C. § 324(a).

VI. GROUND 1: 35 U.S.C. § 101

Petitioner asserts that the claims are directed towards patent-ineligible subject matter. This challenge fails.

A. The Petition Does Not Establish Patent Ineligibility Under § 101

Petitioner’s § 101 analysis is wrong regarding both steps of the *Alice* test. Ex. 2001, ¶¶46-58. In determining whether a claim is directed to patent-ineligible subject matter under the *Alice* framework, both the Supreme Court and Federal Circuit warn against characterizing the claim at “a high level of abstraction and untethered from the language of the claims” as such a characterization “all but ensures that the exceptions to § 101 swallow the rule.” *Enfish, LLC v. Microsoft Corp.*, 822 F.3d 1327, 1337 (Fed. Cir. 2016) (citing *Alice Corp. Pty. v. CLS Bank Int’l*, 573 U.S. 208, 217 (2014)). Petitioner’s characterization of the Challenged Claims impermissibly untethers the single element of a “memory space” from all the remaining claim language to assert that each and every one of the Challenged Claims

is directed exclusively to this single element. Petitioner also argues that each of the limitations of the Challenged Patent, other than the “memory space,” represent “well-understood, routine, and/or conventional” computer elements, without providing any analysis of what these other limitations require or how they are allegedly well-understood, routine, and/or conventional. Petition, 30. Petitioner’s conclusory arguments fail to show any likelihood of the Challenged Claims being found to be directed to ineligible subject matter.

1. Petitioner is Wrong About *Alice* Step One

The Challenged Claims are not directed to the abstract idea of a “memory space” as Petitioner contends. The Challenged Claims are instead directed to a “system for storing data” which includes device elements that are both physical and highly unconventional. *See* Ex. 2001, ¶¶46-58. These additional limitations further make it clear that the claims cannot be directed to a transitory signal, as no transitory signal could read on, among other limitations, “at least one controller to operate memory elements.”

The claimed subject matter of the Challenged Patent is very similar to an example in the USPTO Subject Matter Eligibility Guidelines of claims not directed to an abstract idea. *See* Ex. 2008 (USPTO § 101 Guidelines), 21 (example 27 reciting a method for storing BIOS in a system with volatile and non-volatile memory). This example recites a particular method for transferring and storing

BIOS in memory upon the local computer powering up. Similarly, here, the Challenged Claims recite a particular system that transfers retained data to a different physical address based on a data integrity test where there is “no apparent exception [*i.e.* abstract idea] recited in the claims,” thereby ensuring they are patent eligible. Ex. 2008, 22. Moreover, courts regularly find that claims relating to improvements in computer memory are directed to patent eligible subject matter. *See, e.g., Enfish*, 822 F.3d at 1346; *Visual Memory LLC v. NVIDIA Corp.*, 867 F.3d 1253 (Fed. Cir. 2017); *Ancora Techs., Inc. v. HTC Am., Inc.*, 908 F.3d 1343 (Fed. Cir. 2018), as amended (Nov. 20, 2018). Notably, in *Visual Memory*,⁵ the Federal Circuit overturned the district court’s finding of patent ineligibility, because the claimed

⁵ Claim 1 of the patent at issue in *Visual Memory*, which was found to be patent eligible by the Federal Circuit, recited in its entirety:

1. A computer memory system connectable to a processor and having one or more programmable operational characteristics, said characteristics being defined through configuration by said computer based on the type of said processor, wherein said system is connectable to said processor by a bus, said system comprising:

a main memory connected to said bus; and

a cache connected to said bus;

wherein a programmable operational characteristic of said system determines a type of data stored by said cache.

“computer memory system” was not directed to an abstract idea, and accordingly encompassed patent eligible subject matter, despite the claims at issue in that case containing significantly less detail defining the claimed memory system than those of the Challenged Patent. *Visual Memory*, 867 F.3d at 1262.

Similar to the system in *Visual Memory*, the system of the Challenged Claims improves computer functionality by allowing for selective mapping between a higher capacity, but lower endurance MLC module, and a higher endurance, but lower capacity SLC module, based in part on a “data integrity test” on data in an MLC module. Ex. 1001 at 5:2-10; Ex. 2001, ¶¶52-58. This selective mapping between different memory modules helps to optimize memory storage to improve system capacity, endurance, and access speed. Ex. 1001 at 4:20-31; Ex. 2001, ¶¶54-58. Moreover, the Challenged Claims recite significantly greater detail than the claims in *Visual Memory*, further confirming that the Challenged Patent does not tie up all ways of implementing any allegedly abstract idea.

2. Petitioner is Wrong About *Alice* Step Two

Second, even if the Challenged Claims were directed to an abstract idea, which PO does not concede, these claims would still be patent eligible under step 2B of the *Alice* framework, as they include inventive limitations that amount to “significantly more” than an abstract memory space *per se*. Ex. 2001, ¶¶48-49, 52-58. The Challenged Claims address a meaningful technical problem arising from

the need to balance the various parameters of capacity, endurance, and accessibility in memory systems. Ex. 2001, ¶¶51-58. As Dr. Khatri explains, the Challenged Claims embody a meaningful technical solution to this problem by, among other things, remapping logical memory to different physical addresses if data stored in an MLC nonvolatile memory element fails a data integrity test, which improves the performance of the memory system by, for example, ensuring that data is reliably stored in locations of memory where integrity is not in doubt. Petitioner also claims that every limitation of the Challenged Claims, other than the “memory space,” recites well-understood, routine, and/or conventional elements in a conventional arrangement, but fails to provide any analysis or evidence to support this unfounded argument. Petition, 30. To the contrary, the claims embody inventive techniques for improving memory operations as discussed above. Ex. 2001, ¶¶48-49, 52-58.

VII. GROUND 2: 35 U.S.C. § 112(a)

Petitioner asserts that five terms lack written description support and/or enablement. Petition, 30-37. These challenges fail.

A. The Petition Does Not Establish That Any Term Is Unpatentable Under 35 U.S.C. § 112(a)

A term has sufficient written description support if “the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). “To meet the

enablement requirement, the specification of a patent must teach those skilled in the art how to make and use the full scope of the claimed invention without undue experimentation.” *Martek Biosciences Corp. v. Nutrinova, Inc.*, 579 F.3d 1363, 1378 (Fed. Cir. 2009) (internal quotations and citation omitted). The Petition’s § 112(a) arguments fail.

1. 2.A: “Memory Space”

“Memory space” is clearly disclosed in the specification and is fully enabled. *See* Ex. 2001, ¶¶63-64. Before reaching the merits, however, this ground should be rejected outright as the Petition does not clearly identify or explain the basis for its challenge. Petitioner’s argument spans only four sentences, beginning as an apparent written description challenge but later ambiguously referencing enablement. *See* Petition, 30 (heading “VIII” labeled as “Written Description” challenges), 31 (initially asserting that the claims “lack a written description,” but later suggesting that the specification “fails to enable”). Written description and enablement are not the same thing, and neither PO nor the Board should be forced to guess what Petitioner is arguing. Petitioner’s unsubstantiated challenges must be rejected. *See Microbiotica, Limited v. Board of Regents, The University of Texas System*, PGR2023-00026, Paper 12 at 24, 27 (P.T.A.B. Nov. 21, 2023) (denying institution of written description and enablement grounds when petitioner “d[id] not provide sufficient analysis of the full disclosure of the [challenged] patent” and

included “enablement challenges repeat[ing] the written description arguments in one sentence, and provide[d] no more analysis, much less under the *Wands* factors”).

The Petition appears to argue that because the specification uses the term “memory space” to refer to a memory capacity, it is not proper for the claims to refer to “memory space” in any other sense. But in fact, the specification’s use of the term “memory space” is entirely consistent with how the term is used in the claims to describe the space where data is stored. For example, at column 5, line 12, the specification explains that the “total non-volatile *memory* storage *space*=MLC+SLC.” Ex. 1001, 5:12. This indicates that there are two spaces—MLC and SLC—where data is stored, and the total space is the combination of the two. Ex. 2001, ¶64. Figures 1, 2A-2B, and 4 of the Challenged Patent show examples of MLC and SLC memory space. For example, Figure 4 is shown below:

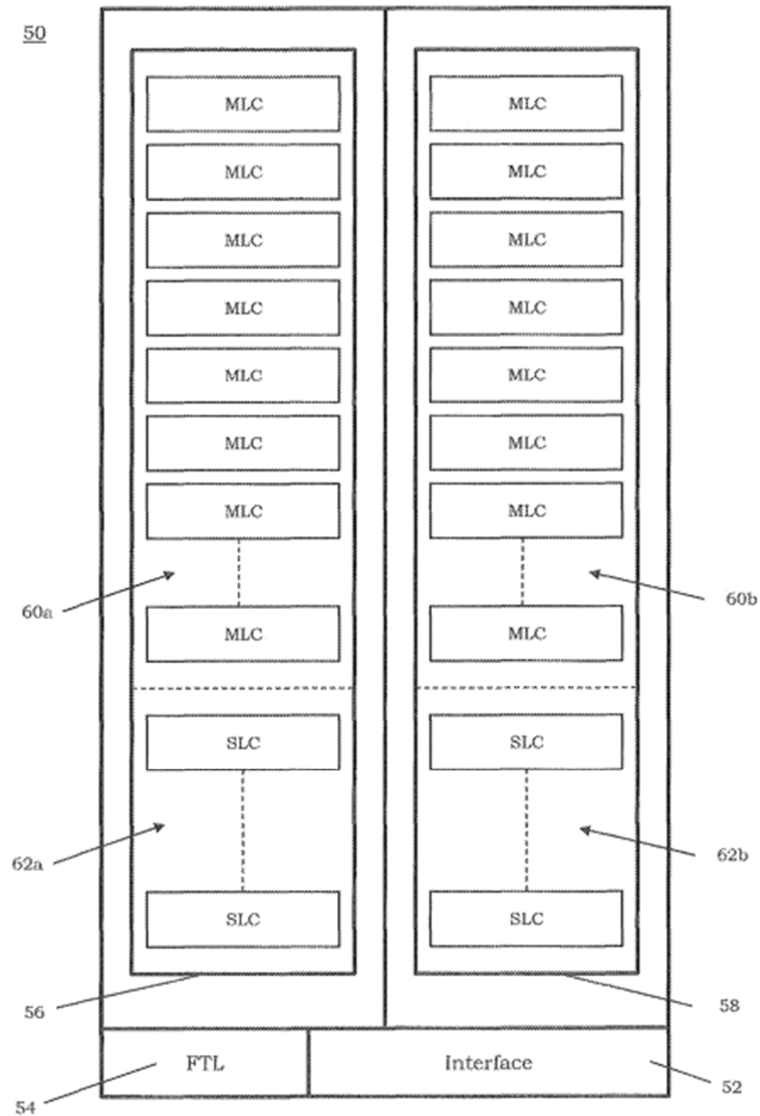


FIG. 4

Ex. 1001, Fig. 4.

2. 2.B: “Memory Element”

“Memory elements” are clearly disclosed in the specification, including in a patent (Ex. 2012) which the Challenged Patent incorporates by reference. Ex. 2001, ¶65. In another threadbare argument, Petitioner suggests that “memory element” is not “mentioned in the specification.” Petition, 32-33, 32. But that is not the test for

written description. The Federal Circuit has held that the specification does not need to use the exact language of the claims, noting that it is unnecessary to “recite the claimed invention *in haec verba*.” *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1352 (Fed. Cir. 2010) (en banc).

Applying the correct test, a POSA would have understood that the Challenged Patent demonstrates possession of the claimed “memory elements.” *See* Ex. 2001, ¶65. The specification states that cells of SLC or MLC flash memory may store a single bit or multiple bits per cell, respectively. Ex. 1001, 2:5-11. The specification shows in great detail, albeit with different words, how MLC and SLC memory elements are used to store data. *See, e.g.*, Ex. 1001, Figs. 1, 4, 5:33-6:67. “Memory element” was a readily understood term in the art, and simply refers to an element of memory. *See* Ex. 2001, ¶65.

3. 2.C: “Mapping...As Necessitated By The System To Maximize Lifetime”

A section 112 challenge to this term was already rejected in district court, and there is no merit to Phison’s challenge here. *See* Ex. 2006, 7. The specification clearly conveys possession of this term, and it was fully enabled. Ex. 2001, ¶66. Petitioner’s ground is again disjointed, beginning as a written description challenge but including references to enablement, and fails to articulate a clear argument. Petition, 33-35. Even so, the Challenged Patent explains—as is claimed—that mapping is performed to increase the “reliability and lifetime” of the memory. Ex.

1001, 1:35-42. Particularly, Figs. 2A-2B and 3A-3B show how data is remapped to boost or prolong the lifetime of the system. If, for example, there is failure of a data integrity test, the data is transferred to a block with higher endurance. *Id.*, 5:54-57. Similarly, if a block is heavily used, the data is mapped to a block that is less-used, or a higher-performance block. *Id.*, 3:19-26 (“selects an available target block with the lowest overall erase count”), 6:50-56 (“on a periodic basis, such as, for example, every 100 writes, or every 10,000 writes, transfer the contents of those blocks into the SLC NAND flash...”). In each case, the lifetime of the memory is maximized. *Id.*

4. 2.D: “Transfer Of Data...From Those Physical Addresses Determined To Have Failed The Data Integrity Test”

The specification clearly discloses and fully enables this term. Ex. 2001, ¶¶67-68. For example, Figures 2A-2B describe remapping a “physical address range” after a “failed data integrity test,” and Figures 3A-3B and the related disclosure describe transferring data to the remapped address. Ex. 1001, 6:5-43 (describing “repeat[ing]” the write process to the “next available” address after a failed data integrity test).

In another cursory challenge spanning only three sentences, Petitioner fails to demonstrate otherwise. Petition, 35. Petitioner does not rely on their expert for this ground. Petitioner incorrectly asserts that the claimed “transfer of data” would not

be “useful” because it “propagat[es] failed data[.]” *Id.*, 35. This is plainly incorrect—the claimed “transfer” does not propagate “failed data.” As a POSA would understand, it is often possible to read degraded data correctly from flash memory after a failure, for example through the use of error correcting codes which are commonplace in the industry. *See* Ex. 2001, ¶¶67-68. As another example, the Challenged Patent’s specification explains that, when data is remapped after a failed data integrity test, “the write is repeated” from “memory within the device controller.” Ex. 1001, 6:5-43, 6:42-43 (returning to write “step 110” upon failure of a data integrity test); Ex. 2001, ¶68. The memory within the device controller would not contain the failed data written to the non-volatile memory. *Id.* Petitioner’s unsubstantiated challenges must be rejected. *See Microbiotica*, PGR2023-00026, Paper 12 at 24, 27.

5. 2.E: “At Least One Memory Element”

A POSA would have found that the Challenged Patent’s specification clearly conveys possession of “at least one...memory element” and enables its full scope. Ex. 2001, ¶¶69-70. To start, it is again unclear whether this ground is a written description or enablement challenge. Petition, 30 (heading VIII presenting “written description” challenges), 36 (referencing whether terms are “enabled”). In any event, the specification provides a clear, enabling description of the “*at least one MLC nonvolatile* memory element” ([1c1]) and “*at least one SLC nonvolatile*

memory element” ([1c2]). For example, Figures 2A-2B (referencing MLC and SLC blocks) and Figure 4 (referencing MLC and SLC “flash memory modules”) disclose MLC and SLC memory elements. Considering this disclosure, a POSA would have understood how to make and use the full scope of the claimed invention without undue experimentation. Ex. 2001, ¶69.

As a practical matter, a POSA would understand that flash memory systems are large, typically containing megabytes, gigabytes, or even terabytes of storage, and comprising thousands of blocks. Ex. 2001, ¶70. But the Petition attempts to argue that a contrived, “single-blocks” system would not be useful yet technically meet the claim language. Petition, 37. That is not sufficient to prove unpatentability of a claim for lack of enablement. Rather, Petitioner must show that the ““number of inoperative embodiments [is] *significant*”” and that a POSA would have needed to ““experiment unduly in order to practice the claimed invention.”” *See Allergan et al. v. BTL Healthcare*, PGR2021-00020, Paper 16 at 22-23 (P.T.A.B. Jun. 16, 2021) (quoting *Atlas Powder Co. v. E.I. du Pont de Nemours & Co.*, 750 F.2d 1569, 1576 (Fed. Cir. 1984)). There is nothing “significant” about a single-block embodiment that would never be found in the real world.

In addition, Petitioner’s argument is facially false. Petitioner suggests that the claims of the Challenged Patent can be “met with *just one* SLC memory element and *one* MLC memory element...” Petition, 36. That is not what claim 1 requires.

Instead, [1c] requires at least *two* MLC nonvolatile memory elements ([1c1], requiring “a plurality”) and at least one SLC nonvolatile memory element ([1c2]).

VIII. GROUND 3: 35 U.S.C. § 112(b)

Petitioner asserts that six claims are indefinite. Petition, 37-45. These challenges fail. The district court has already touched on some of these issues in a prior claim construction order rejecting similar indefiniteness challenges to a parent patent. *See* Ex. 2006. And the district court will already have ruled by January 2025 on additional indefiniteness challenges, leaving no reason for the Board to consider the same arguments yet again. *See* Ex. 2004, 2-4.

A. The Petition Does Not Establish That Any Term Is Unpatentable Under 35 U.S.C. § 112(b)

1. 3.A: “Memory Space”

Petitioner argues in a cursory manner that “memory space” is indefinite because it is not described in the claim language to be “logical” or “physical.” Petition, 38. But “breadth is not indefiniteness.” *Niazi Licensing Corp. v. St. Jude Med. S.C., Inc.*, 30 F.4th 1339, 1347 (Fed. Cir. 2022) (citation omitted). A POSA would not find any ambiguity about what this term refers to. Ex. 2001, ¶¶71-75. To the contrary, claim 1 of the Challenged Patent requires that memory space be “associated” with physical memory elements and that non-volatile memory space “includes both multi-level cell (MLC) space and single level cell (SLC) space.” Ex.

1001, 7:29-32. Particularly in light of this context, a POSA would find no ambiguity regarding what “memory space” refers to. Ex. 2001, ¶¶73-74.

“Memory space” simply refers to where data is stored. Ex. 2001, ¶72. This is a simple term that is readily understood by POSAs and lay persons alike.

A POSA reading the claim language, in light of the specification and prosecution history, would have understand what is meant by this claim term. Claim 1 specifies:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space...

Ex. 1001, 7:29-32. It is abundantly clear from the face of the claim that the “memory space” is simply where data is stored. Ex. 2001, ¶73. Some of the data is stored in volatile memory space; some is stored in non-volatile memory space. *Id.* The data that is stored in non-volatile memory space may be stored in MLC or SLC memory space. *Id.* To the extent there is any doubt, the surrounding claim language specifies that data may be stored in memory elements, and these memory elements may be mapped into the memory space. Ex. 1001, 7:33-36. Furthermore, the specification makes it clear that the “total non-volatile memory storage space=MLC+SLC.” Ex. 1001, 5:12. In other words, the “memory space” refers to where data is stored, and “memory storage space” refers to the sum of the memories that make up a given memory. Ex. 2001, ¶74.

Petitioner cannot demonstrate that this term is indefinite, when “memory space” is commonly used to refer to “where data are...stored.” Ex. 2003 (Micheloni textbook), 485; *see also id.*, 493. Even Petitioner’s own patents use “memory space” to refer to the “addressable locations” where data is stored. Ex. 2007 (U.S. Patent App. 2007/0271609), ¶0007. When a previous petitioner, Micron, filed an IPR against U.S. Patent No. 10,950,300 (“300 Patent”) (Ex. 1011), of which the Challenged Patent is a continuation, Micron’s expert opined that “memory space” means “a set of addresses” where data is stored. Ex. 2011, ¶63 (“Taken together, a set of addresses is known as an ‘address space’ or ‘memory space.’”). That confirms that a POSA would have fully understood what is meant by “memory space.” Ex. 2001, ¶75.

2. 3.B: “Memory Element”

There is nothing confusing or indefinite about “memory element.” A POSA would have readily understood that a “memory element” is simply an element of memory. Ex. 2001, ¶¶76-81. “Memory element” is a well understood term in the art. For example, U.S. Patent 8,194,452, which the Challenged Patent incorporates by reference (*see* Ex. 1001, 1:24-31 (incorporating “U.S. patent application Ser. No. 12/915,177”)), refers to elements of memory. Ex. 2012, 2:52-54 (referring to “an exemplary NAND memory integrated circuit as one element of the...nonvolatile memory system”). Additionally, when a previous petitioner, Micron, filed an IPR

against the 300 Patent, Micron’s expert explained that “flash memory elements” were “well known to any POSA” by 2010. Ex. 2011, ¶59. There is nothing ambiguous about this term, and it should be given the full scope of its plain meaning.

There are even dictionary definitions for this term. Ex. 2013 (Oxford Dictionary of Computing), 312 (defining “memory element” as a “device that stores one item of information”). And one of Petitioner’s customers, Kingston, has patents that similarly uses “memory element” to broadly refer to an element where data is stored. Ex. 2014 (U.S. Patent App. 2010/0186084), ¶¶[0009], [0017]-[0020]. “These definitions [and references] confirm [this term] would have had [a] broad but understood meaning[] to a skilled artisan.” *Niazi*, 30 F.4th at 1350.

Petitioner argues that “memory element” is indefinite because it could refer to “blocks, pages, or bytes of data” or to “a cell.” Petition, 48. Here again, Petitioner confuses breadth with indefiniteness. *See Niazi*, 30 F.4th at 1347. A “memory element” is simply an element of memory, and the fact that it may be a broad term does not make it indefinite.

Petitioner also suggests that claim 1 allegedly includes “inoperative” embodiments. Petition, 39. But the Federal Circuit has held that the question of inoperative embodiments is irrelevant to indefiniteness, the basis of Petitioner’s ground. *See Exxon Rsch. & Eng’g Co. v. United States*, 265 F.3d 1371, 1382 (Fed. Cir. 2001), *abrogated on other grounds by Nautilus, Inc. v. Biosig Instruments, Inc.*,

572 U.S. 898, 134 S. Ct. 2120, 189 L. Ed. 2d 37 (2014) (“there is nothing indefinite about the claim language at issue in this case simply because it covers some embodiments that may be inoperable”).

3. 3.C: “Mapping...As Necessitated By The System To Maximize Lifetime”

The Western District of Texas already determined that this term is not indefinite, and that it should be given its plain meaning. *See* Ex. 2006, 7. There is no reason for the Board to change that construction here. Further, Phison has raised the same challenge in district court, and Phison’s challenge will have been adjudicated there by the January 9, 2025 *Markman* hearing. *See* Ex. 2004, 4. There is no need to relitigate the issue in a post-grant review.

A POSA would readily understand what it means to perform “mapping...as necessitated by the system to maximize lifetime.” Ex. 2001, ¶¶82-87. The point of the Challenged Patent is to increase the “reliability and lifetime” of the memory, and the specification is replete with examples of how to do this. Ex. 1001, 1:35-42. A POSA reading the specification would understand that this term refers to transferring data from MLC to SLC, or from heavily used MLC to less used MLC, in order to prolong or otherwise boost the lifetime of the memory. Ex. 2001, ¶84. Specifically, Figs. 2A-2B and 3A-3B of the Challenged Patent show how the data is remapped to boost or prolong the lifetime of the system. If, for example, there is failure of a data integrity test, the data is transferred to a block with higher endurance. Ex. 1001,

5:54-57. Similarly, if a block is heavily used, the data is transferred to a block that is less used, or a higher-performance block. *Id.*, 3:19-26 (“selects an available target block with the lowest overall erase count”), 6:50-56 (“on a periodic basis, such as, for example, every 100 writes, or every 10,000 writes, transfer the contents of those blocks into the SLC NAND flash...”). In each case, the lifetime of the memory is maximized. *Id.*

Further, previous petitioner Micron’s IPR against the 300 Patent (of which the Challenged Patent is a continuation) further confirms this term is not indefinite. When Micron’s expert was faced with this claim term (which also appears in claim 1 of the 300 Patent), he had no problem determining its claim scope and opined that it relates to rewriting data to more robust SLC cells to boost lifetime. *See* Ex. 2011, ¶85 (alleging in the “Technological Background” that “[i]n order to maximize the lifetime of devices, it was known to write frequently updated blocks...to SLC due to its higher erase cycle capacity and faster speed”), ¶¶183-186, 184 (citing the 300 Patent at 5:14-20 and 1:45-52, explaining that lifetime is increased by using MLC and SLC). Additionally, in its prior petition, Micron confirmed that this term does “not require further construction and can be afforded [its] plain and ordinary meaning.” Ex. 2016, 28.

Here, Petitioner Phison instead contends that this term is indefinite because claim 1 does not specify “what mapping is implicated” to maximize lifetime.

Petition, 40. Petitioner’s argument, in effect, is that the claim is too broad unless a specific “strategy/configuration” of mapping is claimed. *Id.* Again, Petitioner mistakes breadth for indefiniteness. *See Niazi*, 30 F.4th at 1347. The claim does not need to be limited to a specific type of mapping to be patentable.

4. 3.D: “Controller” Limited By Claimed Functions

Petitioner goes for the “Hail Mary” argument that this term is not only governed by § 112, ¶6, but it is also indefinite for lack of disclosed structure. But claim 1 never use the word “means,” and Petitioner cannot possibly overcome the presumption that § 112, ¶6 does not apply.⁶ Ex. 2001, ¶¶88-98.

In another jumbled argument, Petitioner contends that the “‘Controller’ is...a nonce word” and, thus, § 112, ¶6 applies. Petition, 41. This argument has no merit. The Federal Circuit and numerous other courts have consistently held that “controller” is not a nonce term, and it has a sufficiently definite structure. *See, e.g., Telcordia Techs., Inc. v. Cisco Sys., Inc.*, 612 F.3d 1365, 1377 (Fed. Cir. 2010) (“The record shows that an ordinary artisan would have recognized the controller as an

⁶ Petitioner references 35 U.S.C. § 112(f) but this is not the applicable statute. *See* Petition, 41. The Challenged Patent is a continuation of an application filed before September 16, 2012, and, therefore, contrary to Petitioner’s argument, the applicable statute is pre-AIA 35 U.S.C. § 112, ¶6.

electronic device with a known structure.”); *Via Vadis, LLC v. Buffalo Americas, Inc.*, 2016 WL 5239626, at *12 (W.D. Tex. Sept. 20, 2016), *rev’d in part on other grounds* *Vadis, LLC v. Blizzard Ent., Inc.*, 815 F. App’x 539 (Fed. Cir. 2020) (“Defendants are unable to overcome the presumption, arguing only that the word ‘controller’ is a nonce word, and that one of ordinary skill in the art would not have understood the term to imply or require any structure. The court disagrees.”); *Sysmex Corp. v. Beckman Coulter, Inc.*, 2021 WL 1259710, at *4 (D. Del. Apr. 6, 2021) (collecting four additional cases where courts found § 112, ¶ 6 does not apply to “controller”); *Capella Photonics, Inc. v. Fujitsu Network Commc’ns, Inc.*, 2021 WL 465430, at *23 (E.D. Tex. Feb. 9, 2021) (“[T]he Court understands that ‘control unit’ refers to a well-known class of structures also known as controllers.”).

The Challenged Patent’s specification confirms that the claimed “controller” is an electronic device with a known structure. The “Background” portion of the specification repeatedly refers to controllers as known devices that face specific challenges or perform specific tasks. Ex. 1001, 2:36-39 (“Sometimes, a plurality of files has to be combined and/or modified, which poses an enormous challenge for the memory *controller* device of a non-volatile memory system.”); 2:40-43 (“the vast majority of NAND flash in enterprise servers utilizes a SLC architecture, which further comprises a NAND flash *controller* and a flash translation layer (FTL)”); 3:4-7 (“wear leveling algorithms are used with the flash devices (as firmware

commonly known as FTL or managed by a *controller*”); 3:11-14 (“the *controller* maintains a lookup table”); 3:14-26 (“the *controller’s* wear-leveling algorithm determines which physical block to use each time data is programmed,... Depending on the wear-leveling method used, the *controller* typically either writes to....”).

A POSA would have understood the “controller” to be a component that uses firmware to “control” or “manage” the data flow to and from the memory. Ex. 2001, ¶93; Ex. 2003, 39 (Fig. 2.33, including a functional representation of a “Memory Controller”), 40-43. For example, a POSA would have known that firmware implemented by the controller may manage tasks such as wear leveling, garbage collection, and bad block management. Ex. 2003, 40; *see also* Ex. 1001, 3:6-7 (also referring to wear leveling performed by “firmware commonly known as FTL or managed by a controller”).

An overwhelming wealth of technical dictionaries and well-known textbooks confirms that a “controller” had a known structure. Ex. 2015 (Microsoft Computer Dictionary), 128 (defining “controller” as “a device that other devices rely on for access to a computer subsystem”); Ex. 2003, 39-40; *Va. Innovation Scis., Inc. v. Amazon.com, Inc.*, 2019 WL 4259020, at *13-15 (E.D. Tex. Sept. 9, 2019) (collecting “technical dictionary definitions...reinforcing that the term ‘controller’ refers to a known class of structures”); *Barkan Wireless IP Holdings, L.P. v.*

Samsung Elecs. Co., Ltd., 2019 WL 497902, at *21-23 (E.D. Tex. Feb. 7, 2019) (same); *see also Via Vadis*, 2016 WL 5239626, at *12 (“[D]ictionary definitions of ‘controller’ proffered by Plaintiffs show that one of ordinary skill in the art would understand this term to have an ordinary meaning.”).

In contrast, Petitioner provides no support for its argument that “controller” is a nonce term. Petition, 41. Petitioner cites the *Rain Computing* case, but this case involves an unrelated term and fails to counter the clear precedent establishing “controller” is not a nonce term. *See* 989 F.3d 1002, 1006 (Fed. Cir. 2021) (considering the term “user identification module,” where “module”—unlike “controller”—was a “well-known nonce word”).

Thus, § 112, ¶6 does not apply, and it is unnecessary to consider whether the specification provides sufficient structure. *See Virginia Innovation Scis., Inc. v. Amazon.com, Inc.*, 2019 WL 4259020, at *8 (E.D. Tex. Sept. 9, 2019) (explaining that “whether the patents disclose sufficient corresponding structure...is a distinct inquiry that arises *only if* 35 U.S.C. § 112, ¶ 6 is found to apply”).

Still, even if § 112, ¶6 applies, it is clear from the Challenged Patent’s specification that the “controller” provides a clear structure for performing the claimed functions. “[T]he specification need only disclose enough to permit one of ordinary skill in the art to perceive the bounds of the invention.” *Intelligent Automation Design, LLC v. Zimmer Biomet CMF & Thoracic, LLC*, 799 F. App’x

847, 852 (Fed. Cir. 2020) (cleaned up). As Dr. Khatri explains, the “specification teaches a series of instructions for the computer to follow...that reasonably bounds how the claimed invention might [perform the functionality].” *Id.*; *see also* Ex. 2001, ¶¶97-98. A POSA would have understood that the specification discloses algorithms for the claimed functionality. Ex. 2001, ¶¶97-98; *see also Typhoon Touch Techs., Inc. v. Dell, Inc.*, 659 F.3d 1376, 1385 (Fed. Cir. 2011) (“[T]he patent need only disclose sufficient structure for a [POSA] to provide an operative software program for the specified function.”). For example, Figures 2A-2B describe the data integrity test, including mapping and remapping addresses, and Figures 3A-3B provide a “flow chart illustrating” the invention. Ex. 1001, Figs. 2A-2B, 3A-3B, 4:52-57; *see* Ex. 2001, ¶97; *see also StrikeForce Techs. Inc. v. PhoneFactor Inc.*, 2015 WL 5708577, at *1 (D. Del. Sept. 29, 2015) (“I agree...that the flow charts and/or specification prose disclose algorithms for the various means-plus-function terms.”).

5. 3.E: Claims Reciting Method Steps In The Context Of A System

The Challenged Claims do not improperly mix apparatus elements and method steps, contrary to Petitioner’s contention (Petition, 43-44). Rather, they explain how the controller is configured to operate in the claimed system. Ex. 2001, ¶¶99-101. This is exactly what the case law allows and is entirely consistent with

IPXL. Here, the functional language in the claims describes how the controller is *configured* to operate. For example, claim 1 reads in part:

1. A system for storing data comprising:...

at least **one controller to operate** memory elements...

wherein the at least **one controller**, or the FTL, or a combination of both **maintain** an address table...

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein...

the controller...operable to store the received data in the given one of the MLC nonvolatile memory element as stored data and retain such received data in the random access volatile memory...

the controller performing a data integrity test...after the at least a Write access operation...

Ex. 1001, claim 1 (excerpts).

This claim simply describes the controller and how it is configured to operate within the system. In *IPXL*, the invalid claim recited a “*system of claim 2...wherein...the user uses the input means*” to change information. *IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005) (emphasis in original). ***Here, in contrast, there is nothing in any of the controller claims reciting***

a user action. A POSA would have understood that each verb simply describes how the *controller* is configured to operate, rather than referring to any user action. Ex. 2001, ¶100. Unlike *IPXL*, the Challenged Claims never refer to “the user.” “Though [the claim] includes active verbs—presents, receives, and generates—these verbs represent permissible functional language used to describe capabilities of the [claim elements].” *Mastermine Software v. Microsoft Corp.*, 874 F.3d 1307, 1315-16 (Fed. Cir. 2017) (collecting cases).

Petitioner argues that the claimed “controller performing a data integrity test” is indefinite because it may require “user choice” in determining when the test is performed. Petition, 43-44. This is wrong. Claim 1 merely states that the controller is configured to respond to a Write access operation by performing a data integrity test. This does not claim a user action. Rather, the claim states that the controller is “capable” of responding to a Write access operation. *See Mastermine Software, Inc. v. Microsoft Corp.*, 874 F.3d 1307, 1316 (Fed. Cir. 2017) (explaining that it is permissible to “claim the system’s capability to receive and respond to user selection”).

6. 3.F: Whether And When The Claimed Comparison Is Required

There is nothing ambiguous about term 3.F (“performing a data integrity test...after the at least a Write access operation”), and a POSA would have readily understood its scope. Ex. 2001, ¶102. Claim 1 makes clear that the “data integrity

test” is performed “after...a Write access operation.” And the specification provides further insight “whether and when” a “data integrity test” may be performed. Petition, 44-45. For example, the data integrity test may be performed “after every write.” Ex. 1001, 5:4-5 (“The controller conducts a data integrity test after every write.”); *see also id.*, 4:20-22. Alternately, the data integrity test may be performed only when “time permits.” *Id.*, 5:51-54 (“After each write to an address within a particular address range, the device controller 14 will—as time permits—perform a read on the address range to ensure the integrity of the written data.”). Thus, a POSA would have readily understood that data integrity tests performed after every Write access operation, or only after some Write access operations, to be within the scope of claim 1. Ex. 2001, ¶102. But all claim 1 requires is that the controller perform a data integrity test after “a Write access operation.”

Petitioner suggests that claim 1 does not provide sufficient guidance regarding “whether and when” the data integrity test must be performed and, accordingly, is somehow indefinite. Petition, 44-45. Petitioner suggests that the claim must explicitly state whether the data integrity test is performed after “*every* ‘Write Access.’” *Id.*, 45 (emphasis in original). But Petitioner cites no cases to support this contrived theory. Instead, again, Petitioner confuses breadth with indefiniteness. *See Niazi*, 30 F.4th at 1347. The claims need only inform the scope of the invention

with “reasonable certainty,” which claim 1 does here. *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014).

IX. GROUND 4: 35 U.S.C. § 103

The Petition’s obviousness arguments fail. First, Gavens itself does not disclose the use of random access volatile memory, and the Petition provides no basis to combine the embodiments of Gavens with any other disclosure of random access volatile memory. Second, the Petition fails to clearly show what in Gavens it contends is a “controller memory” and “random access volatile memory.” Finally, the Petition fails to show that a comparison between stored data and retained data is performed by the controller as part of a data integrity test.

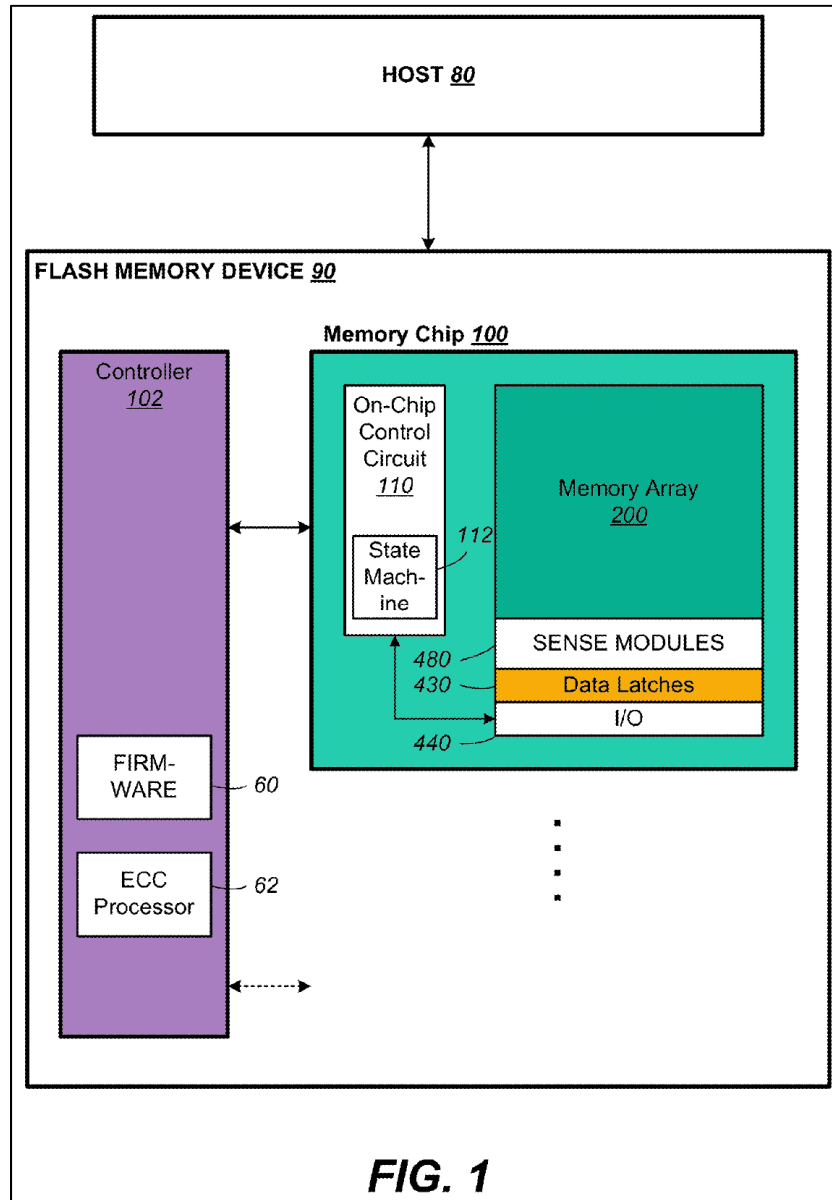
A. Overview Of The Cited Prior Art

Petitioner asserts that the claims are obvious over Gavens (U.S. Patent No. 8,634,240) (Ex. 1045) in view of the knowledge of a POSA. Petition, 45-75. In its single-reference § 103 ground, Petitioner also cites references that Gavens allegedly incorporates by reference, including: U.S. Patent Appl. Pub. No. 2011/0153912 (“Gorobets”) (Ex. 1049); U.S. Patent No. 6,456,528 (“Chen”) (Ex. 1040); U.S. Patent No. 5,930,167 (“Lee”) (Ex. 1050); and U.S. Patent Appl. Pub. No. 2010/0172180 (“Paley”) (Ex. 1051).

1. Gavens

Gavens discusses a problem that occurs with flash memory (a type of non-volatile memory)—as it ages, its error rate increases. Ex. 1045, 3:56-4:5; Ex. 2001, ¶¶105-124. To ensure data integrity in such situations, the memory uses a resource-intensive error correction code (ECC) to correct errors. Ex. 1045, 3:56-4:5. Gavens explains that this poses a problem because, “for most of the life time of the device [(before the device ages and the error rate increases)], the ECC is only marginally utilized, resulting in its large over-heads being wasted[.]” *Id.*, 3:67-4:2.

To perform ECC, Gavens describes a flash memory device including **controller 102** (highlighted purple) and **memory chip 100** (highlighted teal).



Ex. 1045, Fig. 1 (annotated), 8:13-39; Ex. 2001, ¶106. The memory chip includes an *on-chip* control circuit 110 with state machine 112. The memory chip also includes input/output (I/O) circuits, **data latches 430**, sense modules, and a non-volatile flash **memory array 200**. *Id.*, 4:13-16, 8:13-39. In contrast to the Challenged Patent, there is no mention of RAM in the memory chip 100, controller chip 102, or anywhere else in the flash memory device 90. In fact, the only time that

Gavens mentions RAM is in the “Background of the Invention,” when Gavens is *distinguishing* its purported invention from RAM. *Id.*, 1:26-29 (“Unlike RAM...that is also solid-state memory, flash memory is non-volatile”).

Before writing a page of data to the memory array, “ECC is computed for the data page” by the ECC Processor 62. *Id.*, 12:51-63. The page of write-data then consists of two portions: the “user data” and the computed ECC. *Id.*

When a page is read from the memory array, it is “shifted out” (or “toggled”) to **controller 102**. There, first an error detection code (EDC) “indicates the existence of any errors in the read data page[,]” and if there are errors, “the data page’s existing ECC is compared to a second version of the ECC computed on the read data [(the “user data”)].” *Id.*, 12:64-13:8.⁷

Gavens teaches that using ECC in this way—where the ECC must be programmed to correct the “worst-case” number of bits—is burdensome in terms of processing time as well as chip area on the controller:

Using ECC to correct a worst-case number of error bits will consume a great amount of processing time. The more bits it has to correct, the

⁷ This EDC/ECC relies entirely on data that is read from the non-volatile memory array. Thus, unlike the claimed invention of the Challenged Patent, this EDC/ECC does not involve a comparison of data read from the non-volatile memory with data *retained* in volatile memory (such as RAM). Ex. 2001, ¶108 n.1.

more computational time is required. The memory performance will be degraded. Additional dedicated hardware may be implemented to perform the ECC in a reasonable amount of time. *Such dedicated hardware can take up a considerable amount of space on the controller ASIC chip.* Moreover, for most of the life time of the device, *the ECC is only marginally utilized*, resulting in its large over-heads being wasted and realizing no real benefits.

Ex. 1045, 3:48-4:2; *see also id.*, 5:15-30, 13:9-16.

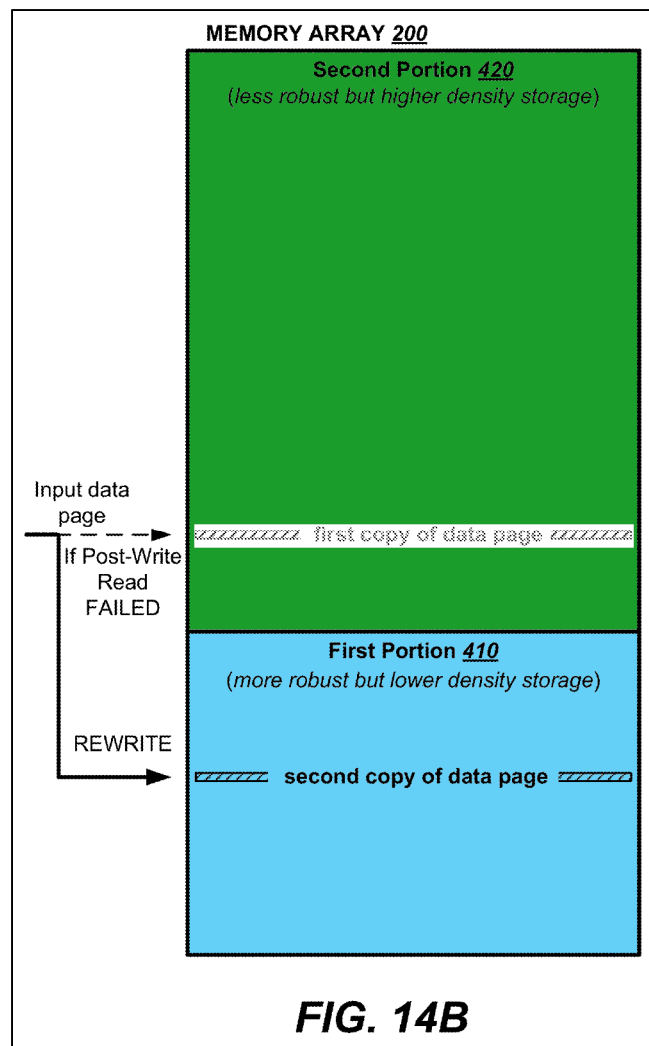
To address this problem, Gavens discloses the embodiments of Figures 14A-14B, 16A-16C, and 20A-20C, which describe the **memory array 200** of Figure 1 in greater detail. *See id.*, 8:13-15 (“Fig. 1 illustrates...a memory device in which the features of the present invention are embodied.”).

These embodiments rely on a memory with a first SLC portion (which is less error prone) and a second MLC portion (which is more error prone). Gavens explains that optimizing where data is stored (in the SLC or MLC portion) based on the expected number of error bits “allows a smaller and more efficient...ECC...to be designed for correcting a smaller number of error bits, thereby improving the performance and reducing the cost of the memory.” *Id.*, 4:28-31.

a. First Embodiment (Figs. 14A-14B)

Gavens describes a first embodiment with respect to Figures 14A-14B. *See* 1045, 17:24-26 (referring to “the embodiment described in Fig. 14A and Fig. 14B”). For this embodiment, as shown in Figure 14B below, Gavens describes a memory

array that relies on a “**lower density**” first portion 410 (*i.e.*, SLC) and a “**higher density**” second portion 420 (*i.e.*, MLC). *Id.*, 4:13-19, 16:14-28; Ex. 2001, ¶¶112-114. The MLC portion is more error prone than the SLC portion but can be used “for efficient storage.” Ex. 1045, 4:16-19, 16:41-45. Gavens explains that data can first be written to the MLC portion, then “read back in a post-write read operation to check for excessive error bits.” *Id.*, 4:19-21; *see also id.*, Fig. 14A, 16:41-56.



Id., Fig. 14B (annotated); Ex. 2001, ¶113.

Gavens explains that the post-write error detection process can check for errors in one of two ways: “either by comparison with the original copy which may be cached or by checking the EDC portion of the ECC.” Ex. 1045, 16:46-49. While Gavens at 16:46-49 does not specify how the “original copy” is cached, Gavens later explains that “[i]n the preferred embodiment” (where the antecedent basis of “the” refers to the immediately preceding “preferred embodiment” of Figures 14A-14B) the “data is cached in [a] first section of the first portion” of non-volatile memory (*i.e.*, a section of the non-volatile SLC memory). *Id.*, 18:1-8; *see also id.*, 16:14-16. Gavens does not describe caching the “original copy” in volatile memory.

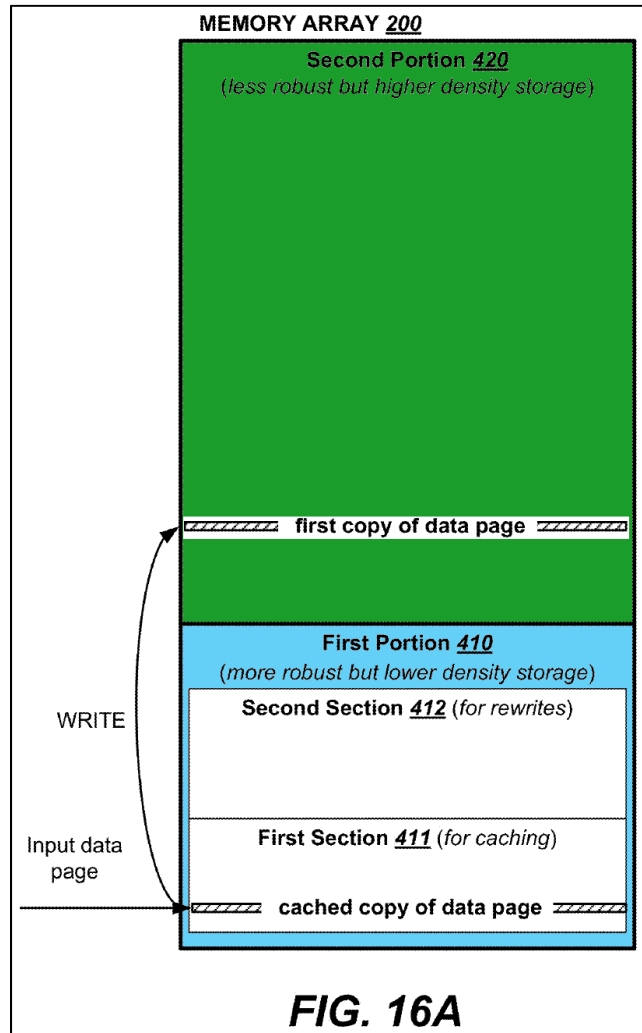
Once the error rate is checked, the device determines whether to keep the data in MLC or instead move it to SLC. If the stored data has an acceptable number of error bits, then the stored copy remains in the MLC and becomes the “valid” copy. *Id.*, 16:41-56. “If the error bits exceeded a predetermined amount, the data is” instead stored in “the less error-prone” SLC portion. *Id.*, 4:21-22; *see also id.*, Fig., 14B, 17:7-20, 18:1-8. To rewrite the data, Gavens teaches that the memory may rely on the “cached” copy of the original data or “correcting the errors bits [from the copy stored in the MLC] with the ECC.” *Id.*, 17:12-14; *see also id.*, 18:1-8.

b. Second Embodiment (Figs. 16A-16C)

Figures 16A-16C depict a second embodiment of Gavens. *See* Ex. 1045, 7:26-28 (referring to “the embodiment described in Fig. 16A to Fig. 16C”); Ex. 2001,

¶¶115-120. For this embodiment, Gavens teaches splitting the first portion (*i.e.*, the SLC portion) into a first section “for caching” and a second section “for rewrit[ing]” data. *Id.*, Fig. 16A, 18:9-23. Gavens emphasizes that this approach limits reliance on the controller 102. *See* Ex. 1045, Fig. 1, 3:60-4:2, 18:36-39.

As shown in Figure 16A below, Gavens explains that the lower density First Portion (*i.e.*, SLC) includes two sections—a “first section” 411 for caching write data, and a “second section” 412 for rewriting data from the higher density Second Portion (*i.e.*, MLC). *Id.*, 18:9-23.



Id., Fig. 16A (annotated); Ex. 2001, ¶116.

Incoming data is written both to the MLC and as a “cached copy” to the first section of the SLC. Ex. 1045, 18:21-29. Detecting the number of error bits is then “accomplished by comparison [of the data written to MLC] with the cached copy.” *Id.*, 18:40-44.

Gavens specifies that this comparison may be performed at the **data latches 430** (highlighted orange in Figure 1 above) on the **flash memory chip 100**. *Id.*,

16:46-49, 18:30-39. Gavens strongly recommends using **data latches 430** because it eliminates the need to “toggle” the data out to the **controller chip 102**, as would be required if using ECC Processor 62 for EDC-based error detection. *Id.*, 18:36-39; *see also id.*, 3:60-4:2. Gavens explains that “much time can be saved” by eliminating the need to toggle data to the controller chip, thus increasing the performance of the device. *Id.*

If there is an acceptable number of error bits, the MLC portion becomes the “valid” copy. *Id.*, 18:45-52, Fig. 16B. If there is an unacceptable number of error bits, the “cached copy” in the “first section” of the SLC is rewritten to the “second section” of the SLC. *Id.*, 18:53-67, Fig. 16C.

By caching the data in the non-volatile memory array and using the latches to compare the data, Gavens lowers overhead and reduces reliance on the controller chip. *Id.*, 18:40-67.

c. Third Embodiment (Figs. 20A-20C)

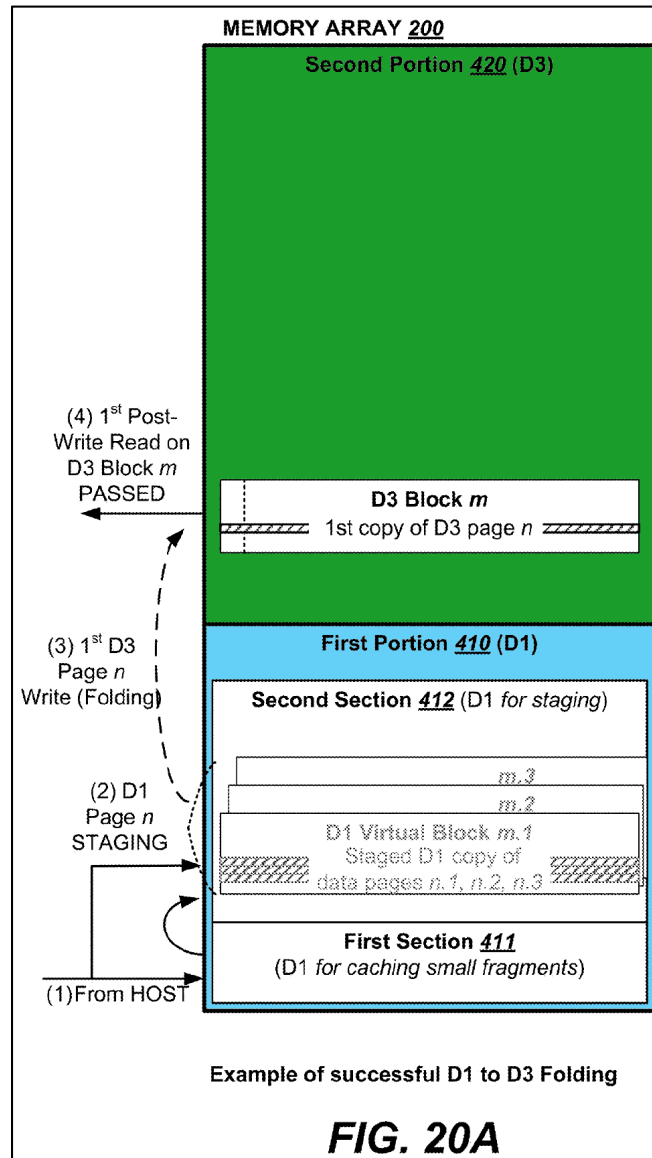
Gavens presents a third embodiment with Figures 20A-C. *See* 1045, 7:33-39, 20:30-58 (“In a preferred embodiment of yet another aspect of the invention, the high density portion of the memory (D3) has each memory storing 3 bits of data. The less error-prone, low density storage portion of the memory (D1) has each memory storing 1 bit of data. ... Figs. 20A-20C illustrate various examples of

implementing the post-write-read error management in a memory configured with D1 and D3 portions.”); Ex. 2001, ¶¶121-124.

In this embodiment, EDC/ECC is used to determine whether the MLC is too old for further programming. Like the first two embodiments described above, this embodiment also advocates caching data in the non-volatile memory array. As shown in Figure 20A below, during a write operation, input data from the host is first cached in a block of **D1 memory** (SLC) and subsequently written (“folded”) into a block of **D3 memory** (MLC). Ex. 1045, 20:30-40. During a “post-write-read” error management process, data written to the D3 block is compared to the cached version of that data in the D1 block to determine whether the error rate exceeds a threshold. *Id.*, 5:49-6:3, 20:30-59. If the D3 block does not have excessive errors, then the D3 block is determined to have good data and the original data in the D1 block is made obsolete. *Id.*

If the error rate in the D3 block is excessive, the D3 block is rejected and a retry takes place in which the D1 block is written/folded to a new D3 block. The new D3 block is then checked for errors. *Id.* If the new D3 block also has excessive errors, this process of rewriting data to new D3 blocks is repeated for a predetermined number of times before the D1 to D3 folding operation is abandoned. *Id.* Gavens explains that “[a]t this point the memory device is deemed too old for

further programming operations and is made read-only to preserve the integrity of the existing data stored in the memory device.” *Id.*, 20:47-50.



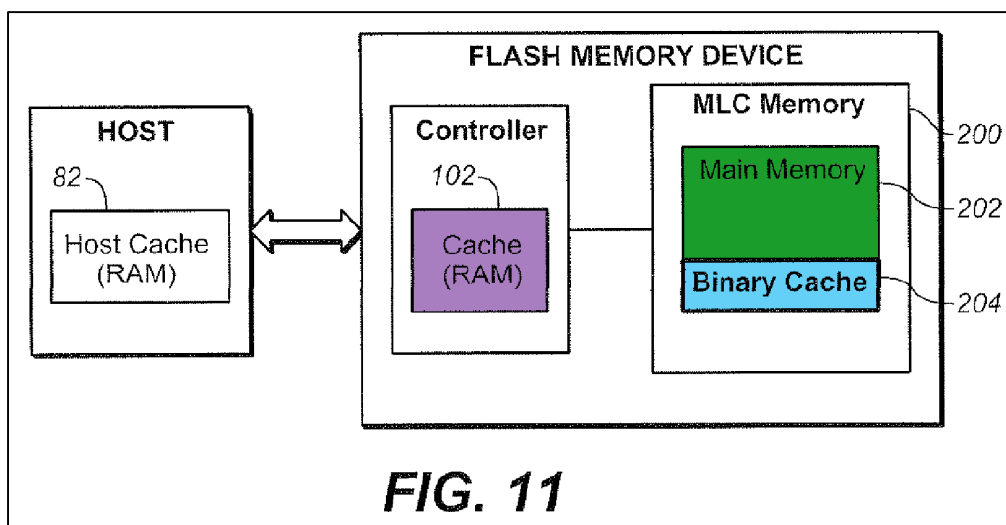
Id., Fig. 20A (annotated); Ex. 2001, ¶123.

Accordingly, unlike PO’s claimed invention, Gavens does not disclose caching or retaining data outside of the non-volatile memory array, or using data retained outside of the non-volatile memory array for detecting errors.

2. Gorobets

Like Gavens, Gorobets includes a non-volatile memory with SLC and MLC portions. Gorobets describes using the non-volatile SLC as a cache to aggregate data before it is written to MLC. *See* Ex. 2001, ¶¶125-127.

As shown in Figure 11 below, Gorobets describes a flash memory device with an **SLC portion** and an **MLC portion**. Ex. 1049, ¶¶104, 109. The **SLC portion** acts as “a cache for data to be written to the **[MLC] memory**.” *Id.*; *see also id.*, ¶108 (explaining the utility of the non-volatile SLC cache).



Ex. 1049, Fig. 11 (annotated); Ex. 2001, ¶126.

The flash memory device also relies on a controller, including a generic volatile **RAM-based cache**. Gorobets explains that this **cache** is “high-speed storage for *temporarily* storing data being passed between a high-speed and slower-

speed component of the system.” Ex. 1049, ¶109 (emphasis added); *see also id.*, ¶130.

Gorobets does not describe a volatile cache that stores data after it is written to the non-volatile memory—in contrast to the Challenged Patent, data is not *retained* in volatile memory. *See id.*, ¶¶24, 109, 130, 144.

3. Chen

Chen describes a non-volatile flash memory in which memory cells that usually store more than two bits of data (MLC) can instead be used to store fewer bits of data (*i.e.*, SLC) “when it is necessary or desirable to improve programming performance, or to extend the life of...the memory in terms of the number of erase and programming cycles that can be endured[.]” Ex. 1040, 2:59-3:15; Ex. 2001, ¶¶128-129. Chen explains that the flash memory uses a controller containing a generic “buffer memory for the user data being written to or read from the memory array.” Ex. 1040, 4:39-41. This “buffer memory” would not retain data after it is written to flash. Ex. 2001, ¶¶128-129.

4. Lee

Like Chen, Lee also describes a non-volatile flash memory with MLC and SLC portions. Ex. 1050, Abstract, Fig. 7. Lee explains that the non-volatile SLC portion can be used as a write cache. *Id.*; Ex. 2001, ¶130.

5. Paley

Like Gavens, Gorobets, and Lee, Paley describes a non-volatile memory in which a portion of the non-volatile memory is used as a cache. Ex. 1051, Abstract. Paley also describes a memory controller including a generic RAM-based cache for “maintain[ing] system control data and directory data[.]” *Id.*, ¶155; Ex. 2001, ¶¶131-132.

Gavens, Gorobets, Chen, Lee, and Paley—unlike the Challenged Patent and Dr. Rao’s claimed invention—do not disclose a volatile memory used to *retain* data for checking data integrity. Ex. 2001, ¶133.

B. The Board Should Exercise Its Discretion And Deny Institution Under 35 U.S.C. § 325(d)

The Board has discretion to deny institution when “the same or substantially the same prior art or arguments previously were presented to the Office.” 35 U.S.C. § 325(d). To determine whether a petition should be denied under 35 U.S.C. § 325(d), the Board applies the following two-part framework:

- (1) whether the same or substantially same art previously was presented to the Office or whether the same or substantially the same arguments were presented to the Office; and
- (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of the challenged claims.

Advanced Bionics, LLC v. Med-El Electromedizinische Geräte GmbH, No. IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020) (precedential). The *Advanced Bionics* framework considers the non-exclusive factors set forth in *Becton, Dickinson*. *Id.* at 7 (citing *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017)).

Here, both parts of the *Advanced Bionics* framework are met. Gavens—Petitioner’s primary reference in its single-reference § 103 ground—is not new to the Patent Office. And Petitioner does not even attempt to show that the Office “erred in a manner material to...patentability.” *Id.* Petitioner never mentions § 325(d). Thus, this ground should be denied under 35 U.S.C. § 325(d).

1. *Advanced Bionics* Part I – The Examiner Considered The Same Prior Art And the Substantially The Same Arguments During Prosecution

During prosecution of the Challenged Patent, the Applicant submitted U.S. Patent App. Pub. No. 2011/0096601 (the publication leading to Petitioner’s Gavens patent) (Ex. 2025) to the Examiner, who certified its review. *See* Ex. 1001, Cover at 2 (listing U.S. Patent App. Pub. No. 2011/0096601). Therefore, Part I of the *Advanced Bionics* framework is met. *See, e.g., Advance Medical Designs, Inc. v. Corbin Clinical Resources, LLC*, PGR2023-00041, Paper 12 at 24-25 (P.T.A.B. Jan. 23, 2024) (finding Part I met when a prior art reference was “submitted in an IDS”).

But this is not a situation where Gavens was cited only in an IDS. The Examiner considered another reference during the Challenged Patent's prosecution, U.S. Patent App. Pub. No. 2011/0099460 (Ex. 2009, Dusija), of which Gavens is a continuation-in-part. Gavens and Dusija are not only substantially the same—they are practically identical. *See* Ex. 2010 (annotated copy of Gavens including highlights to indicate material also present in Dusija). Figures 1 through 22C of Gavens and Dusija are identical. *See id.* And, other than non-substantive updates, Gavens's Detailed Description up to 24:33 is also identical. *See id.*

The Examiner thoroughly considered arguments based on Dusija during the Challenged Patent's prosecution. The Examiner relied on Dusija in multiple rejections, and discussions about Dusija span multiple pages of the prosecution history. *See* Ex. 2024 (546 Patent prosecution history), 50-61 (Applicant including a comprehensive discussion of Dusija and explaining how it is different from the pending claims), 80-84 (Examiner relying on Dusija in an obviousness rejection of the claims), 115-117 (Applicant again explaining why Dusija does not teach the pending claims), 131-135 (Examiner relying on Dusija in another rejection), 162 (prior to allowance, Applicant again explaining why Dusija is deficient). Notably, the Applicant explained in detail how Dusija does not teach using data retained in volatile memory for a data integrity test in the manner required by claim 1 of the Challenged Patent. *See* Ex. 2024, 50-61.

Finally, Dusija was central to numerous IPRs previously filed against family members of the Challenged Patent. Particularly, Micron previously filed IPR2021-01547, IPR2021-01548, IPR 2021-01549, and IPR2021-01550 against four patents of which the Challenged Patent is a continuation. Each of these IPRs rely on Dusija in its grounds. The Applicant submitted materials from these IPRs to the Examiner, and the Examiner certified that they reviewed them. *See* Ex. 1001, Cover (including in the “References Cited” over sixty submissions from these IPRs). Having extensively considered Dusija, the Examiner allowed the Challenged Patent.

Thus, the Petition relies on the same prior art (Gavens, cited in an IDS) and substantially the same arguments (based on Dusija, which was referenced extensively during prosecution) that were presented to the Office, and *Advanced Bionics* Part I is met.

2. *Advanced Bionics* Part II – The Examiner Made No Material Error

Petitioner ignores its clear issues under § 325(d), likely because it cannot rebut them. *See Nexus Pharmaceuticals, LLC v. Exela Pharma Sciences, LLC*, PGR2024-00016, Paper 9 at 27 (P.T.A.B. Aug. 8, 2024) (finding petitioner did “not sufficiently establish error, let alone material error by the Office” when “neither the [p]etition nor the [r]epley addresse[d]” the issue). Still, the Examiner made no material error during prosecution of the Challenged Patent.

To start, the Petition fails to rely on any teachings in Gavens that are unique to that reference and not already disclosed in Dusija. *See Advance Medical*, PGR2023-00041, Paper 12 at 21 (explaining that “the extent to which additional evidence and facts presented in the petition warrant reconsideration of the prior art or arguments” is considered as part of Part II of the *Advanced Bionics* framework). Specifically, for any citations from Gavens that do not appear in Dusija (*i.e.*, citations to the non-highlighted portions of Ex. 2010), Petitioner merely string-cites these alongside citations that do appear in Dusija. *See* Petition, 48 (citing Gavens at 6:18-21 alongside citations that appear in Dusija), 51 (same), 61 (citing 6:22-23), 62 (citing 6:4-6, 24:45-50, and 29:57-5), 68 (citing 6:23-25). Accordingly, the Petition does not rely on any portion of Gavens that is even arguably “new.” Thus, Petitioner relies on a continuation-in-part of a reference that the Examiner already thoroughly considered, cites overlapping disclosure, and fails to address this issue in its Petition.

Finally, Petitioner cannot show material error on part of the Patent Office because neither Gavens nor Dusija renders the claims of the Challenged Patent obvious. *See infra* Section IX.C (demonstrating numerous errors in the Petition’s single-reference obviousness ground). As explained below, the Petition contains multiple clear errors, and Gavens is completely different from the Challenged Patent’s claims.

Therefore, both parts of the *Advanced Bionics* framework are met, and the Board should deny institution of this ground under 35 U.S.C. § 325(d).

C. The Petition Does Not Establish That Independent Claim 1 Would Have Been Obvious Over Gavens

As discussed below, the Petition’s analysis is fatally flawed regarding four elements of claim 1 of the Challenged Patent.

1. [1a1]: “memory space containing *volatile memory space*”

For limitation [1a1]⁸, Petitioner fails to identify anything from Gavens corresponding to a “volatile memory space.” Ex. 2001, ¶¶135-141. The Petition conclusorily states that “Gavens discloses memory containing volatile RAM,” then string cites two lines and one figure of Gavens. Petition, 47. None of those portions of Gavens disclose or suggest a volatile memory space.

First, Petitioner cites Gavens 1:26 as teaching “RAM,” but that portion of Gavens teaches the opposite. Petition, 47. There, Gavens is merely describing the background of the invention. Gavens carefully distinguishes “nonvolatile storage” and how it is “*unlike* RAM.” Ex. 1045, 1:26-29 (“Unlike RAM (random access memory) that is also solid-state memory, flash memory is non-volatile, and retaining its stored data even after power is turned off.”). Non-volatile storage, as described

⁸ Petition, 47.

by Gavens at the foregoing disclosure, is not a “volatile memory space.” Ex. 2001, ¶136.

Second, Petitioner cites Gavens 1:18 as teaching “[n]on-volatile memory.” Petition, 47; *see* Ex. 1045, 1:17-20 (“This application relates to the operation of re-programmable non-volatile memory systems such as semiconductor flash memory, and, more specifically, to handling and efficient managing of errors in memory operation.”). A **non**-volatile memory system is clearly not a “**volatile** memory space.” Ex. 2001, ¶137.

Third, Petitioner cites “Memory array 200” of Figure 1. Petition, 47. As explained above (*see supra* Section IX.A.1) and as shown below, Figure 1 depicts a “**Flash** Memory Device” including a “Memory Array 200.” Memory array 200 is “flash memory.” Ex. 1045, 4:13-16 (“According to a general aspect of the invention,...a flash memory having an array of memory cells is configured with a first portion and a second portion.”). Flash memory is non-volatile memory. *See, e.g., id.*, 1:26-29 (“flash memory is non-volatile”); *see also id.*, 17:23-42, 17:41-42 (describing storing data in the first portion and second portion “in the nonvolatile memory”); Ex. 2001, ¶138. Thus, memory array 200 is a non-volatile flash memory array, not a “volatile memory space.”

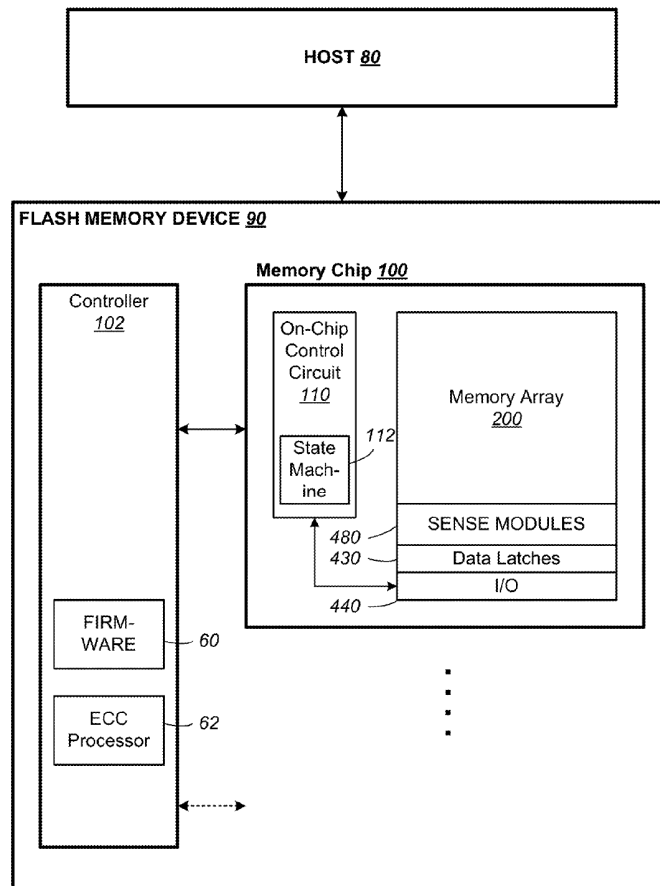


FIG. 1

Ex. 1045, Fig. 1.

Accordingly, Petitioner fails to show that Gavens teaches a “volatile memory space.” Notwithstanding, it is not PO’s duty—or the Board’s—to parse through Petitioner’s incomprehensible list of citations to guess what Petitioner is mapping to [1a1]; Petitioner has the duty to set forth its mapping to prior art clearly and with particularity, and has failed to do so. 35 U.S.C. § 322(a)(3).

Further, for the **separate limitation [1a2]** (which includes limitations specific to the non-volatile memory and is unrelated to the volatile memory space of [1a1]),

Petitioner includes “[f]or further reference” citations to Gorobets. Petition, 48. Petitioner string-cites portions of Gorobets as teaching a “Cache RAM...in the controller.” *Id.* But Petitioner does not explain how this is at all relevant to Petitioner’s mapping. It is not relevant. All that the Petition says is that these teachings somehow apply as “[f]urther reference” for [1a2]. Ex. 2001, ¶140.

Thus, Petitioner has not demonstrated with particularity how limitation [1a1] maps to a volatile memory space disclosed in the prior art, as required by 35 U.S.C. § 322(a)(3). The Petition lacks an “explanation of the significance of the evidence.” 37 C.F.R. § 42.22(a)(2). Therefore, ground 4 fails due to limitation [1a1] alone.

2. [1d]: “at least one *random access volatile memory* element”

The Petition’s deficiency regarding limitation [1a1], alone fatal, permeates into limitation [1d]. For [1d], Petitioner fails to identify with particularity how Gavens discloses a “random access volatile memory element.” Petition, 53-54; Ex. 2001, ¶¶142-153.

Again, Petitioner conclusorily states that “Gavens discloses volatile RAM,” then provides a string cite to Gavens and Gorobets. Petition, 53. Petitioner does not explain how [1d] is being mapped. Notwithstanding, even when Petitioner’s citations are considered individually, Petitioner cannot show that Gavens discloses or suggests the features of [1d]. Ex. 2001, ¶¶142-153.

First, Petitioner cites Gavens 1:26 as disclosing “RAM” (Petition, 53) but, as explained above in Section IX.C.1 for limitation [1a1], this is not true. Ex. 2001, ¶144.

Second, Petitioner cites the “[f]irst section 411” of Figure 16A of Gavens. Petition, 53. However, Gavens explains that first section 411 is part of a non-volatile memory. See Ex. 1045, 4:13-16, 19:1-24 (referring to storing data in “a first section of the first portion” and “a second section of the first portion” “in the nonvolatile memory”). Thus, “first section 411” is not a “random access *volatile* memory element.” Ex. 2001, ¶¶145-147.

Additionally, Petitioner’s reliance on Gavens’s first section 411 exemplifies Petitioner’s indiscriminate citation across Gavens’s embodiments throughout the Petition. Petitioner cites between embodiments without offering a proper analysis. Here, Petitioner cites the first section 411 of Figure 16A, which is part of Gavens’s **second** embodiment. Petition, 53. But Petitioner previously relied on the **first** embodiment of Gavens as teaching [1c]. See Petition, 50 (citing Figure 14A as teaching [1c]); see also Ex. 1045, 16:14-15 (referring to “Fig. 14A” as part of “a preferred embodiment”), 18:9-12 (referring to “Fig. 16A” as part of another “preferred embodiment”); see also *supra* Sections IX.A.1.a-IX.A.1.c (describing three embodiments of Gavens). Further, Petitioner relied on the **third** embodiment of Gavens for [1a2]. See Petition, 47 (citing 20:31-34, which describes the “D1” and

“D3” memory of Gavens’s third embodiment); *see also* Ex. 1045, 20:30-31 (referring to the “D1” and “D3” memory as part of a third “preferred embodiment of yet another aspect of the invention”).

Petitioner cannot mix and match Gavens’s embodiments without explaining how those embodiments would have been combined. *See In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) (“Whether a rejection is based on combining disclosures from multiple references, combining multiple embodiments from a single reference, or selecting from large lists of elements in a single reference, there must be a motivation to make the combination and a reasonable expectation that such a combination would be successful, otherwise a skilled artisan would not arrive at the claimed combination.”).

Third, Petitioner cites Gavens 4:35-37 as disclosing a “first portion [that] serves as a cache....” Petition, 53. But that portion of Gavens does not disclose or suggest that the “first portion” is a “random access volatile memory element.” Ex. 2001, ¶148. Instead, Gavens explains that the “first portion [that] serves as a cache” is in *non*-volatile memory. Ex. 1045, 4:14-15 (referring to a non-volatile “*flash*” memory having an array of memory cells...configured with a first portion and second portion”), 4:35-37 (explaining that the “first portion” in the non-volatile flash can be used as a “cache”).

Finally, Petitioner string-cites Gorobets as disclosing a “Cache RAM...in the controller.” Petition, 53-54. But the Petition says nothing about how the cited disclosure of Gorobets—directed to a volatile RAM-based cache for temporarily storing data in the controller—applies to or can be combined with the cited disclosure of Gavens—directed to a non-volatile cache for retaining data outside of the controller. The Petition’s analysis that Gavens discloses a “random access volatile memory element” is wrong. Petition, 54 (“Gavens and incorporated references *disclose*...”); Ex. 2001, ¶¶149-150.

To begin, Petitioner cites caches from Gavens and Gorobets that are entirely unrelated. Gavens’s second embodiment (that of first section 411 and Figure 16A) describes caching data in *non-volatile* memory where it is *retained* for use in error detection. *See* Ex. 1045, 18:21-44; *supra* Section IX.A.1; *see also* Petition, 53 (citing “First section 411” for [1d]). In contrast, Gorobets’s disclosure of RAM, as cited by Petitioner for [1d], is limited to a *volatile* RAM-based cache for *temporarily* storing data before it is passed to non-volatile memory. *See* Ex. 1049, ¶109 (explaining that the RAM-based cache “temporarily stor[es] data being passed” to non-volatile memory), ¶144 (explaining that the RAM-based cache is of “relatively limited capacity,” so as soon as data is “transferred out of [the] RAM” to the non-volatile memory, the RAM immediately “open[s] up” the space); *see also supra* Section IX.A.2 (providing an overview of Gorobets).

Further, Petitioner concedes that its citations to Gorobets are directed to “RAM...*in the controller*.” Petition, 54 (citing Ex. 1049 (Gorobets), ¶¶18, 56, 109, and 130). But Gavens teaches *against* using the controller for its error detection process. As described in Section IX.A.1 above, Gavens explains that data used for error detection should be cached in the non-volatile memory (*i.e.*, the “First section 411,” as cited by Petitioner) to avoid having to toggle data to the controller. Ex. 1045, 18:36-39. Gavens states that caching data in the non-volatile memory increases performance by reducing reliance on the controller chip. *See id.*, 18:36-67. Relying on a cache in the controller (as Petitioner cites from Gorobets) rather than a cache outside of the controller (as Petitioner cites from Gavens) would contradict the purpose of Gavens’s invention. Ex. 2001, ¶151.

Thus, to the extent Petitioner is alleging that Gavens through its incorporation of Gorobets itself discloses the claimed “random access volatile memory element,” that is incorrect. Petitioner’s cited teachings from Gavens and Gorobets are not only unlike—they are explicitly contradictory. *Id.*, ¶152. These distinct disclosures cannot be indiscriminately strung together through a series of unexplained citations. *See Captioncall, LLC v. Ultratec, Inc.*, No. IPR2020-01215, 2021 WL 278381, at *7 (P.T.A.B. Jan. 27, 2021). Petitioner cannot pick and choose between distinct elements from different disclosures. *See id.* (denying institution when petitioner relied on “distinct” embodiments from a reference and another reference that was

incorporated by reference, explaining that “[a]nticipation requires all elements arranged as in the claim without the need to pick and choose elements from different disclosures”).

Finally, the Petition has not included an obviousness analysis for [1d]. *See* Petition, 53-54. Still, to the extent Petitioner is attempting to rely on obviousness analysis for [1d], that also fails. Petitioner makes no mention of obviousness or any basis or rationale for modifying Gavens’s system to arrive at [1d].

Accordingly, Petitioner fails to show that Gavens discloses or suggests [1d]. Petitioner string cites numerous teachings but fails to provide any explanation or clear mapping. That aside, even “search[ing] through the cited portions,” Gavens cannot be found to disclose or suggest [1d]. *GN Resound A/S v. Oticon A/S*, IPR2015-00103, Paper 13, 6 (P.T.A.B. Jun. 18, 2015).

3. [1f]: “controller memory” and “random access volatile memory”

The ambiguity and error in Petitioner’s mapping of limitations [1a1] and [1d] compound further into the Petition’s treatment of limitation [1f]. Here, Petitioner fails to identify with particularity how Gavens discloses or suggests the “controller memory” ([1f1]) and the “random access volatile memory” ([1f2] and [1f4], and previously referenced in [1d]). *See supra* Section I.D.; Ex. 2001, ¶¶154-161. The Petition again provides a barrage of prior art citations but fails to explain how they map to the claims.

First, Petitioner declares that “Gavens discloses that the controller has buffer memory or cache memory for storing data received from a host...and the RAM for storing the data....” Petition, 58. But the Petition provides no explanation to support this statement. Instead, the Petition lists eleven citations from Gavens. *Id.*, 58-59. These citations do not make clear how Petitioner is mapping Gavens to the “controller memory” and “random access volatile memory.” Nor can they. Gavens does not rely on random access volatile memory. *See supra* Sections IX.A.1 (Gavens background), IX.C.1([1a1]), IX.C.2 ([1d]). And Petitioner does not identify any of Gavens’s disclosure as requiring a “controller memory.” *See, e.g.*, Petition, 58 (referring to a “controller 102” but never identifying a controller memory).

Further, Petitioner’s eleven citations improperly span multiple embodiments. Petitioner cites indiscriminately across these embodiments without conducting a proper obviousness analysis. *See* Petition, 58 (citing Gavens’s **first** embodiment of Figure 14A), 58-59 (citing Gavens’s **second** embodiment of Figure 16A), 59 (citing 5:53-54, corresponding to the **third** embodiment of Gavens); *see also supra* Sections IX.A.1.a-IX.A.1.c (describing these three embodiments of Gavens). “Petitioner’s challenge [incorrectly] treats the various features of [Gavens’s] different embodiments as if they are interchangeable with one another.” *Abiomed, Inc. v. Maquet Cardiovascular, LLC*, No. IPR2017-01204, 2017 WL 4804523, at *4 (P.T.A.B. Oct. 23, 2017) (denying institution).

Second, Petitioner also cites teachings from multiple references that Gavens incorporates by reference, including Gorobets, Chen, and Lee. But the Petition does not explain how the disparate teachings of these references, including generic RAMs and write caches, combine with the cited teachings of Gavens. *See supra* Sections IX.A.2-IX.A.4 (describing Gorobets, Chen, and Lee).

Petitioner again cites to the RAM of Gorobets. Petition, 59-60. While unclear, Petitioner appears to now rely on Gorobets’s RAM for the “controller memory” ([1f1]). *See* Petition, 60 (citing Gorobets ¶109 as rendering “obvious” “[u]se of RAM as a controller cache for the memory controller”). But for [1d], Petitioner already cited Gorobets’s RAM as disclosing the “random access volatile memory element.” *See* Petition, 54 (citing Gorobets ¶109 for [1d]); *supra* Section IX.C.2. Thus, to the extent Petitioner is mapping **both** the claimed “controller memory” and the “random access volatile memory element” onto the same thing in the prior art reference, this is improper. *See Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1254-55 (Fed. Cir. 2010).

Notwithstanding, to the extent the Petition is attempting to present an obviousness analysis regarding Gavens in view of Gorobets, a POSA would not have modified the non-volatile cache of Gavens to rely on the volatile cache of Gorobets. As explained above in Section IX.A.1 and for [1d], Gavens retains data in a non-volatile cache because this **reduces reliance on the controller**. *See* Ex. 1045, 18:36-

67. To instead rely on a volatile RAM-based cache located *in the controller*, as taught by Gorobets, would defeat the purpose of Gavens’s invention. *See id.*; Ex. 2001, ¶159. Petitioner provides no rationale to overcome this clear teaching away.

Additionally, Petitioner points *in a “see also” citation* to teachings from Chen and Lee of a generic “buffer memory” and a non-volatile (“flash”) “write cache,” respectively. Petition, 59-60. Petitioner provides no explanation how these teachings combine with Gavens or map to the claims. Nor can it. As explained above in Section IX.A.3, Chen teaches only a generic buffer and not the claimed “controller memory” and “random access volatile memory” of claim 1. *See* Ex. 1040 (Chen), 4:39-41. Likewise, by Petitioner’s own admission, Lee is unavailing, as it teaches only a *non*-volatile “flash...cache”—just like Gavens. Petition, 60; Ex. 2001, ¶160.

In addition, [1f] also requires that the “controller memory” and “random access volatile memory” have specific functionalities. For example, claim 1 requires a “controller memory *for storing received data*” ([1f1]) and, separately, “random access volatile memory” to “*retain such received data*” once it is written to MLC ([1f4]). Even if the Petition specifically identifies a “controller memory” and “random access volatile memory”—which it does not—the Petition also fails to show that Gavens discloses or suggests a “controller memory” and “random access volatile memory” with these required functionalities.

4. [1g]: “the *controller* performing a data integrity test”

The Petition is also incorrect regarding a *controller* *that performs* the “data integrity test” as required by limitation [1g]. Ex. 2001, ¶¶162-172. As claimed, the controller must perform the “data integrity test” by comparing data read *from MLC* with data *retained in random access volatile memory*. Petitioner does not show how these claim requirements are disclosed or suggested by the prior art.

First, Petitioner declares that “Gavens renders obvious” [1g]. Petition, 61-62. However, in a subsequent string cite spanning more than a page of text, Petitioner summarizes disclosure from Gavens unrelated to a *controller 102* (which Petitioner mapped to the claimed “controller” of [1b]; *see* Petition, 49) performing the “data integrity test.” *Id.*, 61-62.

To start, the Petition’s string cite improperly spans multiple embodiments without explanation. *See, e.g., id.*, 62 (citing Figure 15, corresponding to the first embodiment), 62 (citing 18:30-44, corresponding to the second embodiment). This issue is pervasive throughout the Petition, rendering proper analysis impossible.

Notwithstanding, in its string cite, Petitioner references the “data latches” of Gavens as comparing data in the MLC with data in the SLC cache. Petition, 62 (citing Ex. 1045, 18:30-44); *see also* Petition, 61 (referring to the “data laches [sic]” comparing data), 62 (referring to a “comparison with the original copy which may be cached”). But this cannot correspond to the claimed “data integrity test.” While

the claimed “data integrity test” must be performed *by the controller*, Gavens uses latches to compare data *on the memory chip*. See Ex. 1045, Figure 1A (showing the “Data Latches” 430 as part of the “Memory Chip 100”), 18:21-35; *see also supra* Section IX.A.1. The entire purpose of using the latches is to *avoid* using the controller. See Ex. 1045, 18:30-38. *The Petition even admits that “[t]he comparison is not made at the controller.”* Petition, 62. Thus, Gavens cannot and does not disclose or suggest a “*controller* performing” the data integrity test. Ex. 2001, ¶¶162-165.

Additionally, the claimed “data integrity test” requires comparing data read from MLC with data retained in *random access volatile memory*. In contrast, Gavens’s latches compare data read from MLC with data retained in *SLC non-volatile memory*. See Ex. 1045, 18:1-8 (stating that “the incoming data is cached in” the non-volatile flash memory), 18:30-35; *see also supra* Section IX.A.1. Gavens and the patented invention are distinct, and Gavens does not disclose or suggest [1g].

Finally, digging even further, Petitioner also references Gavens’s use of “the EDC portion of the ECC” to perform an “error check.” Petition, 62. But this EDC (error detection code) does not rely on data retained in RAM, as required by the claimed “data integrity test.” Instead, Gavens’s EDC relies entirely on data read from the MLC. See Ex. 1045, 12:49-13:16, 13:3-4 (“the data page’s existing ECC

is compared to a second version of the ECC *computed on the read data*”). Petitioner even admits this. Petition, 62 (“The controller 102 compares the ECC in the read data to a second version of ECC *computed from the read data*.”). Thus, Gavens’s EDC does not disclose or suggest [1g]. Ex. 2001, ¶¶166-167.

Second, Petitioner also cites disclosures from Gorobets and Paley, which Gavens allegedly incorporates by reference. Petition, 63. But the Petition does not coherently explain how this disclosure is relevant to or combined with Gavens. Gorobets and Paley would not have been understood by a POSA to be describing Gavens’s system. Ex. 2001, ¶¶168-171. These references cannot remedy the deficiency of Gavens regarding [1g].

At the top of page 63, Petitioner superficially proposes an obviousness basis for unpatentability.⁹ This basis lacks explanation and does not make sense. Petitioner does not explain what aspect of the claim limitation is missing in Gavens and, correspondingly, does not explain what from Gavens must be modified to arrive at the claim language. Petitioner also does not explain what teachings from Gorobets and/or Paley are being used to modify Gavens’s system, and why a POSA would

⁹ It is unclear whether Petitioner is invoking obviousness for [1g], or instead is relying on disclosures of Gavens itself. *See* Petition, 61-63. This lack of clarity is itself a basis for siding with PO on this ground.

have made any modification. Instead, Petitioner claims that it would have been obvious to compare data read from MLC with data retained in random access volatile memory, then provides a disjointed list of citations from Gorobets and Paley. *See* Petition, 63. Accordingly, Petitioner fails to perform a proper obviousness analysis, which requires, *inter alia*, ascertaining the “differences between the prior art and the claims at issue.” *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966). The Petition’s obviousness analysis is insufficient and must be rejected. “[O]bviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006).

Still, even when parsed individually, Petitioner’s citations fail to show that Gavens in view of Gorobets and/or Paley discloses or suggests the features of [1g]. Petitioner references citations from Gorobets relating to a RAM buffer. *See* Petition, 63 (citing Ex. 1049, ¶¶24, 109). But in that buffer, data is stored only “temporarily” before being written to non-volatile memory. Ex. 1049, ¶109. Gorobets says nothing about retaining data in its RAM for later use in a data integrity test performed by the controller. Petitioner’s remaining cites to Gorobets are also unavailing. *See* Petition, 63 (citing Ex. 1049, ¶104 (describing a “second portion” of the ***non-volatile*** flash memory being used as a cache), ¶130 (same), ¶144 (explaining that the RAM

is “opened up” immediately after data is written to the non-volatile memory)); Ex. 2001, ¶169.

Additionally, even if Petitioner presented a cognizable obviousness combination related to Gavens and Gorobets—which it does not—a POSA would not have combined these references to reach [1g]. Ex. 2001, ¶170. As explained above for [1d] and [1f], Gavens teaches away from using the controller for a data integrity test and instead espouses the benefits of limiting reliance on the controller when testing the integrity of data written to MLC. *See supra* Sections IX.C.2-IX.C.3. Gavens explains that “Data Latches” 430 that are part of the non-volatile “Memory Chip 100”—and completely separate from the “Controller 102”—should be used for error checking to avoid using the controller or any memory external to the non-volatile memory array. *See* Ex. 1045, 18:36-39; *see also supra* Section IX.A.1. Gorobets’s teaching of a generic RAM-based cache would not have led a POSA to concoct a modification to Gavens that reaches [1g]. Ex. 2001, ¶170.

Finally, *in a “see also” cite*, Petitioner references Paley’s disclosure of a “memory manager” that stores “control data and directory data....” Petition, 63. It is unclear how this could be relevant to a “data integrity test” or any other limitation of [1g]—and it is not relevant. Paley’s memory manager bears no relation to [1g]. Ex. 2001, ¶171.

Thus, Petitioner fails to show that Gavens discloses or suggests the features of [1g].

In conclusion, the Petition fails to coherently map Gavens to numerous limitations of claim 1. *See* 35 U.S.C. § 322(a)(3) (requiring mapping with “particularity”); 37 C.F.R. § 42.22(a)(2) (the “petition...must include...[a] full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence”). As explained above, Petitioner’s numerous string cites often encompass multiple embodiments, and it is unclear what Petitioner is mapping each claim element to. *See, e.g., DeSilva v. DiLeonardi*, 181 F.3d 865, 866-67 (Fed. Cir. 1999) (“A brief must make all arguments accessible to the judges, rather than ask them to play archeologist with the record.”); *A.C. Dispensing Equip. Inc. v. Prince Castle LLC*, IPR2014-00511, Paper 16 at 5-6 (P.T.A.B. Sept. 10, 2014) (“Petitioner should not expect the Board to search the record and piece together the evidence necessary to support Petitioner’s arguments.”); *GN Resound A/S v. Oticon A/S*, IPR2015-00103, Paper 13, 6 (denying institution on certain grounds, explaining that “[e]ssentially, Petitioner requires the Board to search through the cited portions of [the prior art] to map prior art disclosure with claim elements. It is a requirement of a Petition to align the evidence and arguments with the various limitations of the challenge claims.”).

**D. The Petition Does Not Establish That Dependent Claims 2-7
Would Have Been Obvious Over Gavens**

Petitioner's challenges to dependent claims 2-7 in ground 4 also lack merit, at least because these claims depend on claim 1, for which Petitioner's ground is deficient for the reasons stated above.

X. CONCLUSION

For the foregoing reasons, there is no reasonable likelihood of Petitioner prevailing with respect to even one of the Challenged Claims. Accordingly, the Petition should be denied.

Date: December 23, 2024

Respectfully submitted,

/Alan Whitehurst/

Alan Whitehurst

Reg. No. 43,263

awhitehurst@mckoolsmith.com

Nicholas T. Matich

Reg. No. L1,373

nmatich@mckoolsmith.com

Arvind Jairam

Reg. No. 62,759

ajairam@mckoolsmith.com

Christopher McNett

Reg. No. 64,489

cmcnett@mckoolsmith.com

Christian Dorman

Reg. No. 79,118

cdorman@mckoolsmith.com

McKool Smith, P.C.

1717 K St. NW, Suite 1000

Washington, DC 20006

Telephone: (202) 370-8300

Facsimile: (202) 370-8344

Counsel for Patent Owner

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner hereby certifies that the word count for the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** is 17,419 words, which is within the limit set in 37 C.F.R. §42.24(b)(1). This word count does not include the table of contents, table of authorities, exhibit list, certificate of word count, and certificate of service. This word count was prepared using Microsoft Word.

Date: December 23, 2024

By: /Alan Whitehurst/
Alan Whitehurst, Reg. No. 43,263

CERTIFICATE OF SERVICE

I hereby certify, in accordance with 37 C.F.R. § 42.205, that the foregoing
PATENT OWNER'S PRELIMINARY RESPONSE was served via electronic
mail on December 23, 2024 on the following counsel of record for Petitioner:

Hsuanyeh Chang, PhD
hsuanyeh@hsuanyeh.com
Stephen Y. Chow
Stephen.Y.Chow@hsuanyeh.com
Douglas E. Chin
Doug.Chin@hsuanyeh.com
Peter Yi
Peter.Yi@hsuanyeh.com
HSUANYEH LAW GROUP PC
11 Beacon Street, Suite 900
Boston MA 02108

Dated: December 23, 2024

By: /Alan Whitehurst/
Alan Whitehurst, Reg. No. 43,263