UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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**PHISON ELECTRONICS CORPORATION,**

Petitioner

v.

**VERVAIN, LLC,**

Patent Owner

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Post-Grant Review Case No. PGR2024-00048

Patent 11, 854,612

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# PETITION FOR POST-GRANT REVIEW OF U.S. PATENT NO. 11,854,612

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**STATUTES**

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## LIST OF EXHIBITS

| Exhibit | Description |
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| 1001 | U.S. Patent No. 11, 854,612, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao |
| 1002 | Declaration of Carl Sechen, Ph.D. |
| 1003 | U.S. Provisional Application No. 61/509,257, titled "IMPROVED LIFETIME MIXED LEVEL NAND FLASH SYSTEM" by Rao |
| 1004 | U.S. Patent No. 8,194,452, titled "NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES," to Rao |
| 1005 | U.S. Patent No. 8,891,298, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao |
| 1006 | *Intentionally omitted* |
| 1007 | U.S. Patent No. 9,196,385, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao |
| 1008 | *Intentionally omitted* |
| 1009 | U.S. Patent No. 9,997,240, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao |
| 1010 | *Intentionally omitted* |
| 1011 | U.S. Patent No. 10,950,300, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao |
| 1012 | Excerpts from prosecution history of '300 patent |
| 1013 | U.S. Patent No. 11,830,546, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao |

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| 1014 | Excerpts from prosecution history of '546 patent |
| 1015 | *Intentionally omitted* |
| 1016 | Excerpts from prosecution history of '612 patent |
| 1017-24 | *Intentionally omitted* |
| 1025 | Excerpts from Rino Micheloni, et al., INSIDE NAND FLASH MEMORIES (Springer 2010) |
| 1026 | Excerpts from NONVOLATILE MEMORY TECHNOLOGIES WITH EMPHASIS ON FLASH: A COMPREHENSIVE GUIDE TO UNDERSTANDING AND USING NVM DEVICES (Joe E. Brewer & Manzur Gill eds. Wiley-IEEE Press 2008) |
| 1027 | Excerpts from MICROSOFT COMPUTER DICTIONARY (5th ed. 2002) |
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| 1030 | Yu Cai et al., *Program Interference in MLC NAND Flash Memory: Characterization, Modeling and Mitigation* (IEEE 2013) |
| 1031 | Kang-Deog Suh et al., *A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme*, 30 IEEE J. Solid State Circuits 1149 (Nov. 1995) |
| 1032 | Eitan Yaakobi et al., *Error Characterization and Coding Schemes for Flash Memories* (2010 IEEE Globecom Workshops, Miami, FL at 1856-60) |
| 1033 | Evans, Chris, "Enterprise MLC: How flash vendors are boosting MLC write endurance" (June 3, 2011) |
| 1034 | Nelson Duann, SLC & MLC Hybrid (Silicon Motion Flash Memory Summit, Santa Clara, CA, Aug. 12, 2008) |
| 1035 | Ashish Jagmohan et. al., *Adaptive Endurance Coding for NAND Flash* (2010 IEEE Globecom Workshops, Miami, FL at 1841-45) |

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| 1036 | Sungjin Lee et al., *FlexFS: A Flexible Flash File System for MLC NAND Flash Memory* (2009 USENIX Annual Technical Conference, San Diego, CA, June 14-19, 2009) |
| 1037 | Minyoung Sung & Kanghee Kim, *Asymmetric Flash Volume Management*, 58 *IEEE Transactions on Consumer Electronics* 455 (May 2012) |
| 1038 | Greg Atwood et al., *Intel StrataFlash*™ Memory Technology Overview at 4, Intel Technology J. (Q4 1997) |
| 1039 | Taehee Cho et al., "A 3.3 V 1 Gb multi-level NAND flash memory with non-uniform threshold voltage distribution," *2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers,* ISSCC (Cat. No. 01CH37177) (2001) |
| 1040 | U.S. Patent No. 6,456,528, titled for "SELECTIVE OPERATION OF A MULTI-STATE NON-VOLATILE MEMORY SYSTEM IN A BINARY MODE" to Chen |
| 1041 | U.S. Patent No. 8,078,794, titled "HYBRID SSD USING A COMBINATION OF SLC AND MLC FLASH MEMORY ARRAYS," to Lee et al. |
| 1042 | U.S. Patent Appl. Pub. No. 2008/0140918, titled "HYBRID NON-VOLATILE SOLD STATE MEMORY SYSTEM" by Sutardja |
| 1043 | U.S. Patent Appl. Pub. No. 2009/0327591, titled "SLC-MLC COMINATION FLASH STORAGE," by Moshayedi |
| 1044 | U.S. Patent Appl. Pub. No. 2010/0172179, titled "SPARE BLOCK MANAGEMENT OF NON-VOLATILE MEMORIES," by Gorobets et al. |
| 1045 | U.S. Patent No. 8,634,240, titled "NON-VOLATILE MEMORY AND METHOD WITH ACCELERATED POST-WRITE READ TO MANAGE ERRORS," to Gavens et al. |

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| 1046 | U.S. Patent No. 8,806,301, titled "DATA WRITING METHOD FOR A FLASH MEMORY, AND CONTROLLER AND STORAGE SYSTEM USING THE SAME," to Yu et al. |
| 1047 | U.S. Patent Appl. Pub. No. 2010/0115192, titled "WEAR LEVELING METHOD FOR NON-VOLATILE MEMORY DEVICE HAVNG SINGLE AND MULTI LEVEL MEMORY CELL BLOCKS," by Lee |
| 1048 | U.S. Patent Appl. Pub. No. 2011/0271043, titled "SYSTEM AND METHOD FOR ALLOCATING AND USING SPARE BLOCKS IN A FLASH MEMORY," to Segal et al. |
| 1049 | U.S. Patent Appl. Pub. No. 2011/0153912, titled "MAINTAINING UPDATES OF MULTI-LEVEL NON-VOLATILE MEMORY IN BINARY NON-VOLATILE MEMORY," by Gorobets et al. |
| 1050 | U.S. Patent No. 5,930,167, titled "MULTI-STATE NON-VOLATILE FLASH MEMORY CAPABLE OF BEING ITS OWN TWO STATE WRITE CACHE," to Lee et al. |
| 1051 | U.S. Patent Appl. Pub. No. 2010/0172180, titled "NON-VOLATILE MEMORY AND METHOD WITH WRITE CACHE PARTITIONING," by Paley et al. |
| 1052 | U.S. Patent No. 8,225,035, titled "SYSTEMS AND METHODS FOR OPERATING A DISK DRIVE," to Colligan |
| 1053-59 | *Intentionally omitted* |
| 1060 | Docket list for *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex., filed March 8, 2024) |
| 1061 | Docket list for *Vervain, LLC v. Kingston Technology Company, Inc*., No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024) |
| 1062 | First Amended Complaint, Doc. No. 9 in *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex.) |

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|---|---|
| 1063 | Signed Agreed Scheduling Order, Doc. No. 16 in *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex.) |

## I. INTRODUCTION:

Phison Electronics Corporation ("Phison" or "Petitioner") requests post-grant review ("PGR") of all claims 1-7 (the "Challenged Claims") of U.S. Patent No. 11,854,612, entitled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao (the "'612 patent") (Ex. 1001), which is assigned to Vervain, LLC ("Vervain" or "Patent Owner"). The '612 patent was issued on issued on Dec. 26, 2023, on the fifth continuation application[1] of a chain of continuations from U.S. Pat. Appl. No. 13/455,267, filed on April 25, 2012,[2] which claimed priority of U.S. Provisional App. No. 61/509,257, filed on July 19, 2011 ("Provisional," Ex. 1003)

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[1] U.S. Appl. No. 18/373,071 filed Sept. 26, 2023.

[2] This application issued as U.S. Patent No. 8,891,298 (the "'298 patent," Ex. 1005). It was followed by division U.S. Appl. No. 14/525,411, filed Oct. 28, 2014, and issued as U.S. Patent No. 9,196,385 (the "'385 patent," Ex. 1007), by continuation U.S. Appl. No. 14/950,553, filed Nov. 24, 2015, and issued as U.S. Patent No. 9,997,240 (the "'240 patent," Ex. 1009), by continuation U.S. Appl. No. 16/006,299, filed June 12, 2018, and issued as U.S. Patent No. 10,950,300 (the "'300 patent," Ex. 1011), and by continuation U.S. Appl. No. 17/203,385 filed March 16, 2021, and issued as U.S. Patent No. 11,830,546 (the "'546 patent," Ex. 1013). Petitioner petitioned Aug. 27, 2024, for review of the '546 patent in PGR2024-00047.

and incorporated by reference the common disclosure of U.S. Patent No. 7,855,916 and U.S. Pat. Appl. No. 12/915,177, for "NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES," the latter published March 10, 2011, and issued as U.S. Patent No. 8,194,452 ("Rao '452," Ex. 1004).[3]

Two later continuation applications issued as U.S. Patent Nos. 11,967,369 and 11,967,370. All eight of these "Lifetime Patents," based on the same April 25, 2012, specification and claiming July 19, 2011, priority, are currently asserted (First Amended Complaint, Ex. 1062) by Vervain against Phison in *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex. filed March 8, 2024).[4]

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[3] The second of these "Embedded RAM Patents" is provided for its slightly more readable exhibits.

[4] All are asserted against a customer of Phison in *Vervain, LLC v. Kingston Technology Company, Inc*., *Kingston Digital, Inc., and Kingston Technology Corp*., No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024). The first four patents were asserted previously in *Vervain, LLC v. Micron Technology, Inc.; Micron Semiconductor Products, Inc.; and Micron Technology Texas, LLC,* No. 6:21-cv-00487 (W.D. Tex. filed May 10, 2021, settled April 21, 2023) and *Vervain, LLC v. Western Digital Corp.; Western Digital Technologies, Inc.; and HGST, Inc.,* No.

This Petition demonstrates by a preponderance of the evidence that the Challenged Claims are unpatentable as one of eight Lifetime Patents groups of claims that, in many verbal variations, purport to extend to fundamentally different technology only the basis for and a couple of well-known features of operation of POSITA-understood hybrid memory system of distinct Single-Level Cell ("SLC") and Multi-Level Cell ("MLC") NAND flash memory modules. Those features were presented in the specification common to all eight Lifetime Patents as preferential direction of data to an SLC module to improve "lifetime (endurance)" under two circumstances: (1) failure of a "data integrity" check of data written to a NAND flash location ('612 6:4-57); and (2) exceeding of a threshold count of "writes" to a NAND flash "block" (6:58-7:3, called "wear leveling" in the BACKGROUND 3:11-33). However, since the 2018 application which resulted in the fourth, '300 patent, the claims have recited abstract "memory spaces" and "memory elements" not described

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6:21-cv-00488 (W.D. Tex. filed May 10, 2021, settled Aug. 8, 2023). Micron petitioned this Board for *inter partes* review in Micron Technology, Inc. v. Vervain, LLC, IPR2021-001547 ('298 patent), IPR2021-001548 ('385 patent), IPR2021-001549 ('240 patent), and IPR2021-001550 ('300 patent), which were instituted on April 8 and 11, 2022, and terminated on April 4, 2023, on settlement after hearing but prior to final written decision.

in the specification and have not recited the second, wear-leveling feature, reciting instead a vague and unsupported "mapping . . . necessitated by the system to maximize lifetime" (7:50-52). Also, since the 2018 application, failure of the "data integrity" check results not in preferential direction to the SLC module, but "remapping . . . to a different physical range of addresses" (8:29-32).

Patent Owner Vervain should not be allowed to maintain its eight attempts to claim well-known NAND flash technology for technologies that it touts in the BACKGROUND (2:7-27) as operating on essentially different principles from erase-before-write NAND flash. Vervain should not be allowed to substitute abstract "memory space" (mentioned in the specification [5:25] only as a quantity of storage space) and vague "memory elements" (not mentioned at all) for the POSITA-understood, hard-wired NAND "pages" for parallel writing and NAND "blocks" for flash erasing. And the '612 method patent should not be allowed to avoid the requirement of claiming adequately disclosed structure by reciting verbose but indefinite, unsupported and pointless (inoperative) steps that incorrectly reflect known NAND flash operation. The Post-Grant Review is eminently appropriate for stopping the proliferation of bad patents such as the '612 patent.

## II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1):

### A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1):

Petitioner Phison Electronics Corporation is the real party-in-interest.

### B. Related Matters Under 37 C.F.R. § 42.8 (b)(2):

As set forth further at note 4 supra, the '612 patent (along with seven other patents based on the same specification) is currently asserted by Vervain against Phison and its customer (separately) in the Western District of Texas. In the Phison case a claim construction hearing is tentatively scheduled for December 5, 2024, and jury selection is tentatively scheduled for December 15, 2025 (*Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259, Doc. No. 16 (W.D. Tex. July 15, 2024) (Ex. 1063). Resolution of this Petition may simplify that litigation and promote settlement.

### C. Lead and Back Up Counsel Under 37 C.F.R. § 42.8(b)(3):

Pursuant to 37 C.F.R. § 42.8(b)(3), lead counsel for this Petition is Hsuanyeh Chang, PhD (Reg. No. 73,431) and back-up counsel are Stephen Y. Chow (Reg. No. 31,338), Douglas E. Chin (Reg. No. 66,713), and Peter Yi (Reg. No. 61,790). Pursuant to 37 C.F.R. § 42.10(b), Petitioner has filed a power of attorney designating the above-identified counsel.

### D. Service Information Under 37 C.F.R. § 42.8(b)(4):

Pursuant to 37 C.F.R. § 42.8(b)(4) service information for the Petition is as follows:

| Lead Counsel | Back-Up Counsel |
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Petitioner consents to electronic service at the above-identified email addresses.

## III. ADDITIONAL REQUIREMENTS:

### A. Payment of Fees Under 37 C.F.R. § 42.15:

The required fees are submitted herewith from Deposit Account No. 50-6685 (Order No. 1280-0009). If any additional fees are due at any time during this proceeding, the Office is authorized to charge such fees to Deposit Account No. 50-6685 (Order No. 1280-0009).

### B. Timing Under 37 C.F.R. § 42.202:

The present petition for post-grant review is filed within nine months after the grant of the '612 patent.

### C. Grounds for Standing Under 37 C.F.R. § 42.204(a):

Petitioner certifies that: (1) the '612 patent is eligible for post-grant review; and (2) Petitioner is not barred or estopped from requesting post-grant review of any claims of the '612 patent on the grounds identified herein.

## IV. NAND FLASH TECHNOLOGY BACKGROUND

Petitioner's expert, Dr. Carl Sechen, has provided in his declaration ("Sechen," Ex. 1002) a deep analysis of the state of NAND flash technology relied on by the Lifetime Patents (Sechen Section V), the embodiments advanced in the common specification (Sechen Section VII), the evolution of the Lifetime Patent claims from NAND flash technology to abstractions for alternative technologies (Sechen Section VIII), specific defects in the '612 claims (Sechen Section IX), and invalidity of those claims over the prior art in view of the POSITA's knowledge of the art (Sechen Section X). Following is a summary of the NAND flash memory technology underlying the '612 patent claim to a "method for storing data."

### A. Characteristic Nature of NAND Flash Memory

A **NAND flash cell** is type of transistor with an analog floating gate that can retain (store) a range of electrical charges associated with "threshold voltages" that,

applied to a control gate, allows conduction of electrical current from drain to source. (Sechen ¶¶ 26 [Fig. 2.1(a)], 30 [Figures 6 and 7 from Atwood {Ex. 1038}] and 31.)

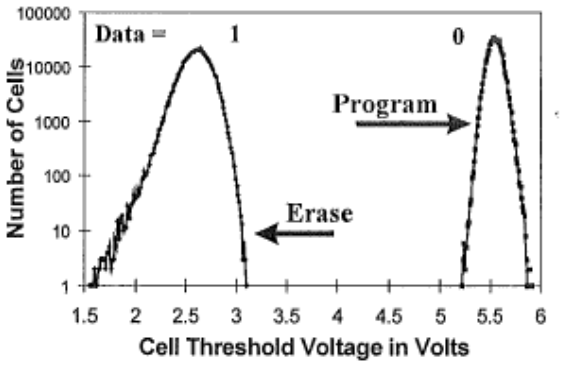



**Figure 6: Single bit/cell array threshold voltage histogram**

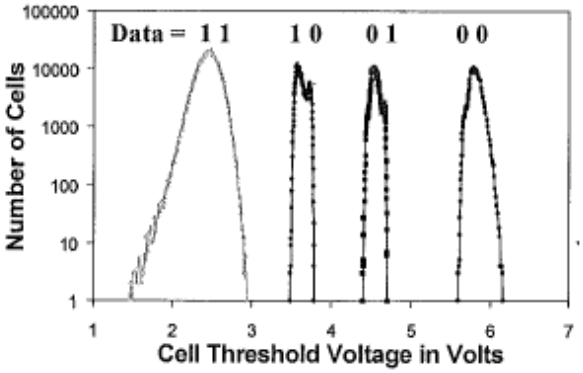



**Figure 7: Two bit/cell array threshold voltage histogram**

These threshold voltages/charges may be chosen to represent information to be stored, in earlier NAND memory operation, using two threshold voltage levels (Figure 6), the lower level to represent ("store") a logical "1" and the higher level to store a logical "0" of one bit of (binary) digital computer data. (*Id.*) The same NAND storage cell can use four threshold voltage levels (Figure 7) to represent four values corresponding to two bits of binary computer data (which in NAND memory operation is sourced from two distinct groups, "pages," of logical data). (*Id.*) An *n* power of two ($2^n$: eight, sixteen, . . .) threshold levels may be used in NAND flash operation to represent corresponding bits of *n* NAND flash pages. The analog floating gate threshold voltage levels are not limited to binary data representation. Thus, in an example from a prior art patent, seven threshold voltage levels were

shown, with the detection shown for four alternative charges in the storage cell by intersection with a reference current:

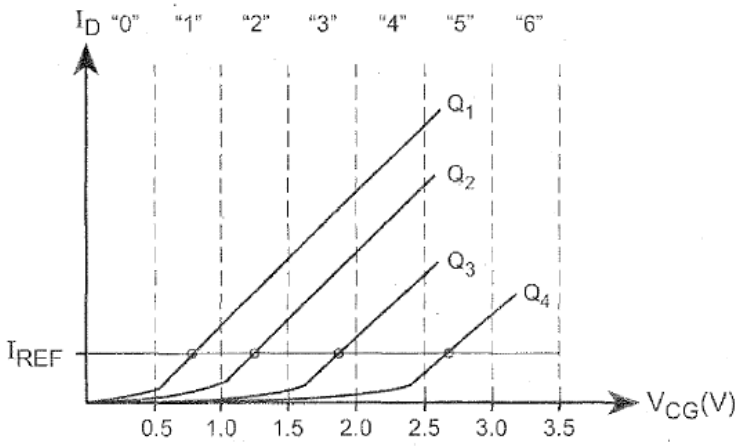



*FIG. 3*

(Sechen ¶ 31 [Fig. 3 from Gorobets '179 {Ex. 1044}]) This diagram also shows that just a storage cell does not make a memory. Even if a particular charge were permanent (read-only memory), there needs to be a way of retrieving the information to make it a memory (Sechen ¶ 31), not a useless "write-only memory." Circuity is required to select the storage cell, to provide a voltage to the control gate and to provide current to be detected, the latter two combined to provide the selection (Sechen ¶¶ 27 [Fig. 15.1 "word lines" and "bit lines" to select a storage cell] and 35 [Fig. 1(a)]). Also, for programmable use of the NAND floating gate (electrically erasable programmable read-only memory, "EEPROM", Sechen ¶ 25) technology, charging ("programming") to a threshold voltage level is "ratchet up," by incremental pulsing (to avoid overshooting) (*id.* ¶¶ 38-40) from an erased state.

To form NAND flash memory, NAND storage cells are hard wired in strings (*id.* ¶¶ 27, 35) (bit-line "columns") and word-line "rows" forming NAND "**pages**" each typically 2K storage cells programmed page by page. (Sechen ¶ 26.) A defining characteristic of NAND flash is that it is hard wired such that "**blocks**" **of** 64 **pages** are **erased in unison** in required preparation for writing to pages in that block that are not empty or previously erased (*id.* ¶¶ 26-27). Thus, unlike magnetic hard disk drives (and the Lifetime Patents' proposed alternative technologies) which allow "write in place" of data assigned to a particular physical location, updates to data (considered "logical") in NAND flash must be written to a new physical location that is empty or must be erased in preparation ("erase before write"). (*Id.*) To maintain logical visibility to the user (host computer) of a NAND flash memory device such as a Solid State Drive ("SSD") (shown at Sechen ¶ 27), there are maintained and updated tables in or available to a **NAND flash device controller**, shown as a hardware module or chip on an SSD circuit board (*id.*) to "map" logical locations visible to the user to physical locations in the NAND flash memory array ("L2P mapping"), which update for each data write (*id.*). The physical instances of NAND flash pages and blocks determine the Physical Block Addresses ("PBA") mapped from the construct of Logical Block Addresses ("LBA"). (*Id.*) This mapping and remapping is typically done with the software construct of a **Flash Translation Layer** ("**FTL**"). (*Id.*) The physical reading, writing and erasing of NAND flash

cells, characteristically organized in pages and blocks, is performed by circuity in a NAND flash memory module shown in multiples in Sechen paragraph 27 as "flash" or "flash memory" on a board, along with a block diagram showing the internal reading, writing and erasing functions. A POSITA would understand this to be a **NAND flash memory or module**. (*Id*.)

### B. Characteristic NAND Flash Memory Management

As reviewed at Sechen paragraphs 27-29, there are well-known processes of to manage the peculiarities of NAND flash memory. These include bad block management and garbage collection. Typically, "hot" data, *i.e.*, frequently updated (such as system) data, and "cold" (not-"hot") data are clustered in respective physical NAND flash blocks in order to facilitate efficient (fewer erase-and-re-writes) collecting of "valid" (un-updated) stored data and freeing up the blocks they otherwise occupy. In addition to avoiding unnecessary burdening of the NAND system operation with long "erases," this and other "wear leveling" processes are calculated to even out write and erase stresses on NAND memory blocks which have limited expected "endurance" ("lifetime") to prevent premature failure or retirement of enough blocks to compromise particular system use. (Sechen note 14 on lifetime.)

### C. Introduction of MLC and SLC Flash

**Multi-level cell (MLC) NAND flash**, developed in 1992-97, as described in Atwood (Ex. 1038), was the use of the NAND storage cell with four threshold

voltage levels to represent two bits of information. The first use known to Petitioner of the term "SLC" appeared in the 2001 Cho article that compares **"single-level program cell NAND flash (SLC)"** with the programming complexity and inefficiencies of MLC. (Ex. 1039, discussed at Sechen ¶¶ 32-33.) Although the terms have been shortened over the years to their acronyms, a POSITA would understand that "MLC" refers to the use of NAND storage cells, each storing one of four system-implemented threshold voltage levels written (pulse-incremented) in two passes – the first writing a "lower" (as least significant bit, "LSB") logical page and then a distinct "upper" (as most significant bit, "MSB") logical page by incrementing the floating gate charge to the desired voltage threshold level that represents those two bits (11, 10, 00, 01). (Sechen ¶¶ 35-39.) As reviewed at Sechen paragraphs 31-41, the charging for MLC memory is more complex and stressful than for SLC because of the narrower window for distinct threshold charges, multiple passes of writing, and incremental pulsing in each pass to avoid uncorrectable overshoot. Thus, a POSITA would understand that different circuitry is required for **MLC NAND flash memory** than for **SLC NAND flash memory**.

### D. Known Coordinated Use of SLC and MLC NAND Flash Modules:

At least because of the compression and multiple pulsing and passes of writing, it was well known that MLC NAND flash, while having more capacity (and thus lower cost of information per NAND cell) would wear more quickly (have less

"endurance") than SLC NAND flash. (Sechen ¶¶ 40-42.) Thus, it was proposed as early as 2008 to use hybrid systems of **SLC modules** and **MLC modules** in which more **frequently written**/updated (to logical locations) **data**, such as system data, user directories, and other user files accessed more frequently) would be written **preferentially to** a more robust **SLC module** while less frequently updated data such as user data would be written to the MLC module. (Sechen ¶ 43; Nelson Duann, SLC & MLC Hybrid (Silicon Motion Flash Memory Summit, Santa Clara, CA, Aug. 12, 2008) ["Duann," Ex. 1034]; U.S. Patent No. 8,078,794 to Lee et al., published Sept. 4, 2008 ["Lee '794," Ex. 1041].)

The **SLC module** preference was applied in 2008-09 to a variety of **wear leveling** techniques in 2008-09. (Sechen ¶¶ 44-45; Sutardja, U.S. Patent Appl. Pub. No. 2008/0140918 "Hybrid Non-Volatile Sold State Memory System" ["Sutardja," Ex. 1042]; Moshayedi U.S. Patent Appl. No. 2009/00327591 ["Moshayedi," Ex. 1043].)

**Two-state operation of MLC** (later called **pseudo-SLC)** was disclosed as early as 2002. (Sechen ¶ 46; U.S. Patent No. 6,456,528 to Chen for "Selective Operation of a Multi-State Non-Volatile Memory System in a Binary Mode" ["Chen '528," Ex. 1040]). Such use of MLC, because it uses the MLC memory circuitry and pulsed/phased writing, has inferior performance and endurance compared to "real" SLC. A SanDisk suite of patents (incorporating by reference among others,

Chen '528) disclosed the use of pSLC or lower-density mode use of MLC modules through partitioning and configuration for multiple uses, including responses to data integrity "fails" – to avoid unnecessary processing/latency, preferably later in the lifetime of the system when reliability statistically becomes an issue, and then using appropriate (to desired performance) error correction code ("ECC") schemes that allow the use of data with errors corrected upon reading, saving wear and latency. (Sechen ¶¶ 49-52, particularly note 12; U.S. Patent No. 8,634,240 to Gavens et al., published April 28, 2011 ["Gavens," Ex. 1045]; *also* U.S. Patent No. 8,806,301 to Yu, published April 14, 2011 [Ex. 1046].) Nothing disclosed in the '612 patent specification was new relative to the 2011 state of the art of NAND flash technology; to the contrary, the disclosed embodiments would not be enabled without the understood (by a POSITA) physical operation of the referenced SLC and MLC modules as SLC NAND flash modules and MLC NAND flash modules with supporting circuitry at least for their distinct organizations, reading, writing and erasing.

## V. THE '612 PATENT:

### A. The Specification:

The core system of MLC NAND flash and SLC NAND flash modules are described multiple times in the specification:

> two separate banks of NAND flash are maintained by a controller. One bank contains economical MLC NAND flash, while a

> second bank contains high endurance SLC NAND flash. The controller conducts a data integrity test after every write. If a particular address range fails a data integrity test, the address range is remapped from MLC NAND flash to SLC NAND flash.

(5:14-17 [emphasis added].) It is repeated in Fig. 4, described as

> two NAND flash memory banks **56** and **58**, whereby memory bank **56** comprises a plurality of MLC NAND flash memory modules **60***a* and a plurality of SLC NAND flash memory modules **62***a*. Memory bank **58** comprises a plurality of MLC NAND flash memory modules **60***b* and a plurality of SIX [sic] NAND flash memory modules **62***b*.

(7:8-14 [emphasis added].) Fig. 4 shows a physical memory device module including two banks each including 8+ **MLC flash memory modules** and 2+ **SLC NAND flash memory modules**).

Dr. Sechen critiques at paragraph 67 the DETAILED DESCRIPTION descriptions of the NAND flash method steps of Fig. 3A and 3B. The text of the latter is presented here with highlighting of points for consideration on this petition:

> FIGS. **3**A and **3**B are a flow chart illustrating a method for utilizing a NAND flash memory system incorporating one embodiment of the present disclosure. The method begins in a step **100**, when a command to write a quantum of data stored in DRAM to a particular location in NAND flash memory is received. In step **102**, the quantum of data is read from **[A1]** DRAM into memory within the device controller (which acts as the memory controller). **[B1]** In step **104**, both

the logical address range and the NAND flash physical address range to which the quantum of data is to be written, is read into memory of the device controller. **[B2]** In step **106**, the quantum of data to be written is combined with the contents of the NAND flash memory. **[B3]** In step **108**, the NAND flash physical address range to be written is erased. In step **110**, the combined data is written to the appropriate NAND flash physical address range. **[A3]**, **[B4]** In step **112** the NAND flash physical address range that was written in step **110** is read into device controller memory.

The flowchart continues in FIG. **3**B. **[A4]** In step **114** the NAND flash physical address range that was read into device controller memory is compared with the retained data representing the combination of the previous contents of the physical address range and the quantum of data to be written. In step **116**, if the retained data matches the newly stored data in the NAND flash memory, the write was a success, and the method exits in step **118**. However, if the retained data does not match the newly stored data in the NAND flash memory, the method executes step **120**, which identifies the next quantum of available SLC NAND flash memory addresses. In step **122**, a check is made to determine if additional SLC NAND flash memory is available, and, if not, the NAND flash memory system is marked as failed, prompting a system alert step **124**. However, if additional SLC NAND flash memory is available, the failed NAND flash physical address range is **[C]** remapped to the next available quantum of SLC NAND flash memory in step **126**. Execution then returns to step **110**, where the write is repeated.

(6:19-57 [emphasis added]). [A1]-[A4] highlights as issues (1) an ambiguity in claim 1 whether "retained data" resides in "controller memory," as well as (2) the inconsistent use of "physical address range" that was read into "device controller memory. [B1]-[B3] appears to be an incorrect reading of Fig. 3A as to the NAND flash operation of combining valid data with new data to be written to a new physical address. [C] is the manifestation of preferential writing into the SLC NAND flash memory that is dropped from express recitation in claims 1-7.

A two-sentence "application of one embodiment" (6:58-7:3) describes what appears to be "wear leveling" by "allocat[ing] 'hot' blocks i.e., those blocks that receive frequent writes, into the **SLC NAND flash memory module 28**, while allocating 'cold blocks; i.e., those blocks that only receive infrequent writes, into the **MLC NAND flash memory module 26**." Although this feature was not claimed in the '612 patent, it is a good example of how the '612 specification relies on known NAND flash memory operation specifically distinguishing an "SLC NAND flash memory module" from an "MLC NAND flash memory module."

**B. Abstraction of the Claims Since 2018:**

Section VIII of Dr. Sechen's declaration analyzes the unsupported abstraction of physical SLC and MLC memory modules of the system disclosed and claimed in the '298, '385 and '240 patents (respectively Ex. 1005 7:6-8:9, Ex. 1007 7:11-8:4, and Ex. 1009 7:30-8:7 and 8:20-59) to unsupported "memory space" and "memory

elements," introduced in the application for the '300 patent (June 12, 2018, Application at 14 [Ex. 1012 at 19]), nearly seven years after the priority date. (Sechen ¶ 74.) Also introduced was the abstraction away from the disclosed and '298, '385 and '240 patents' claimed preferential (NAND) remapping of some (logical) data to the SLC module a vague "mapping . . . necessitated by the system to maximize lifetime." (*Id.* ¶ 75.) The unsupported "memory space" and "memory element" abstractions permeate the '612 patent claims, which also fail to recite preferential mapping to an SLC memory module to enhance "lifetime."

### C. The Challenged Claims of the '612 Patent:

1. [1Pre] A method for storing data comprising:

[1a] maintaining an address table for a memory space containing volatile memory and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space and the volatile memory includes a random access volatile memory element;

[1b] [1b1] mapping logical and physical addresses adaptable to the system by the address table, wherein the [1b2] mapping is performed as necessitated by the system to maximize lifetime, and [1b3] wherein the mapping maps data in at least one of volatile or nonvolatile memories;

[1c] controlling during Write access operations and Read access operations a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element and [sic] at least one SLC memory module including at least one SLC nonvolatile

memory element and [sic] associated memory space using at least one controller;

[1d] storing received data within a controller memory associated with the at least one controller;

[1e] controlling access of [sic] the MLC and SLC nonvolatile memory elements and the random access volatile memory element for storage of the received data;

[1f] transferring [1f1] the stored received data from the controller memory [1f2] to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one given one of the MLC nonvolatile memory element as stored data;

[1g] retaining the received data in the random access volatile memory as retained data associated with the stored data;

[1h] performing a data integrity test on the stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules [1h1] after at least a Write access operation performed thereon, the performing of the data integrity test further comprising:

[1h2] reading the stored data to the controller memory;

[1h3] comparing the stored data in [sic] the controller memory in [sic] the given one of the MLC nonvolatile memory elements to the retained data that was associated [sic] with the data in the random access volatile memory by the controller during the Write access operation;

> [1i] remapping, [1i1] responsive to a failure of the data integrity test performed on the stored data by the controller, [1i2] the address space [sic] to a different physical range of addresses; and
>
> [1j] transferring data corresponding to the retained data [sic] to those remapped physical address [sic] from those physical addresses determined to have failed the data integrity test.

(7:42-8:36 [emphases added].) Essentially, claim 1 is a method claim version of the system claim 1 of the '546 patent (which defines its "controller" by reciting functional steps). Claim 1 of the '612 patent retains in [1a], [1c], and [1e]-[1j] the '300 and '546 patents' unsupported abstractions of "memory space" and "memory element," but, as in the '546 patent, includes in [1c] the '298, '385 and '240 patents' reference to physical MLC and SLC "memory modules." (Sechen ¶¶ 74, 76 and 77.) Claim 1 also retains in [1b] the '300 and '546 patents' "mapping . . . to maximize lifetime," while not reciting any preferential mapping to the SLC module, but only in [1j] to "a different physical range of addresses."

Claim 2 limits the "controller" to a software "module" or firmware "module." (8:37-39.) The abstract "controller" was not given any structure in the specification or claims as a "module" as the SLC and MLC hardware modules.[5]

[5] The counterpart '546 patent claim 2 so limited FTL, recited in its claim 1. (Ex. 1013 8:35-36.)

Claim 3 requires that one of the random access volatile memory ("RAVM") or the MLC and SLC "nonvolatile memory elements" are embedded in the controller. (8:40-43.)

Claim 4 requires that "the MLC and SLC nonvolatile memory elements" comprise flash memory. (8:44-46.)

Claim 5 requires the RAVM to be dynamic random access memory ("DRAM"). (8:47-49.)

Claim 6 requires the RAVM to be static random access memory ("SRAM"). (8:50-52.)

Claim 7 requires that an "SLC nonvolatile memory element includes a hard disk drive (HDD).

In view of the literal claims and disclosure of the '612 patent, the accompanying prior art references and supporting declaration of Dr. Sachen (Ex. 1002), Petitioner respectfully requests cancellation of the Challenged Claims as summarized in the following table.

| **Grounds** | **Exhibits** |
|---|---|
| **Ground 1:** Claims 1-7 are invalid under 35 U.S.C. § 112(a) because the '612 patent specification fails to provide a written description | 1001, 1002, 1004 |

| | |
|---|---|
| enabling, much less demonstrate the possession of any invention claimed. | |
| **Ground 2:** Claims 1-7 are invalid under 35 U.S.C. § 112(b) for failing to particularly point out and distinctly claim the subject matter which the inventor regards as his or her invention. | 1001, 1002, 1034, 1041, 1042, 1043, 1045 |
| **Ground 3:** Claims 1-7 are unpatentable under U.S.C. § 103 as obvious over Gavens and incorporated disclosures in view of a POSITA's knowledge of NAND flash technology. | 1001, 1002, 1003, 1034, 1040, 1041, 1042, 1043, 1045, 1049, 1050, 1051, 1052 |

### D. Person of Ordinary Skill in the Art

A person of ordinary skill in the art at the time of the claimed inventions would have a bachelor's degree in computer engineering, electrical engineering, computer science, or a closely related field, along with at least two years of experience in the design, development, implementation, or management of memory devices and systems. A person with an advanced degree in a relevant field, such as computer or electrical engineering, would require less experience in the development and use of

memory devices and systems. As is common, one could obtain equivalent knowledge and perspective from other life experiences as well. (Sechen ¶¶ 60-61.)

## VI. 37 C.F.R. § 42.204(b)(3): CLAIM CONSTRUCTION

Under 37 C.F.R. § 42.200(b), claims in a post-grant review proceeding are construed using the same claim construction standard that is used to construe claims in a civil action. This includes "construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent," *id*. The standard for claim construction was articulated by the Supreme Court in *Phillips v. AWH Corp.,* 415 F.3d 1303 (Fed. Cir. 2005). Although claim construction may "rely on extrinsic evidence…including expert and inventor testimony, dictionaries, and learned treatises," such evidence must be considered "in the context of the intrinsic evidence." *Id.* at 1317, 1319.

Petitioner contends that the terms of the Challenged Claims' "MLC memory modules" and "SLC memory module" (7:55 and 8:1) have distinct, established, customary meanings for a POSITA in computer memory, reflecting the development of NAND flash reviewed in Section IV over the decade before the July 19, 2011, priority date where "memory" and "module" also have distinct meanings:

- "MLC memory modules" means "modules comprising MLC non-volatile memory" *where*

"MLC non-volatile memory" means "non-volatile memory cells arranged with circuitry capable of storing multiple logical pages in a single physical page of cells" and

- "SLC memory module" means "module comprising SLC non-volatile memory" *where*

  "SLC non-volatile memory" means "non-volatile memory cells arranged with circuitry incapable of storing multiple logical pages in a single physical page of cells"

A POSITA would only understand "SLC" and "MLC" to refer to distinct NAND flash memory circuity, where "level" refers to page level programming, not the threshold voltage levels for which the common floating-gate storage "cell" uses two in "single level" (one-bit) operation (Sechen ¶¶ 30-43). Also, as explained by Dr. Sechen (¶ 65, notes 15-18), "modules" in the hardware context would be understood by the POSITA to mean an interchangeable unit, such as a chip that provides "a complete function" such as the NAND flash chips that organize the NAND memory arrays operated in flash block erase and page writes. That is, SLC and MLC modules are respectively "self-contained, complete function, interchangeable" SLC and MLC memory circuitry (plus possible packaging). The memory circuitry might otherwise be embedded, for example, with other circuitry in a die, such that the SLC/MLC memory is not self-contained or interchangeable.

"[SLC/MLC] flash" and "[SLC/MLC] memory" are sometimes used interchangeably with "[SLC/MLC] module, as in the '612 specification descriptions of "embodiments" FIGS. 2A and 2B (6:4-18), FIGS. 3A and 3B (6:19-57), and "wear leveling" (6:58-7:3). Compare FIG. 4 (7:4-14 "NAND flash memory modules") to the textbook depictions at paragraph 27 of the Sechen declaration:

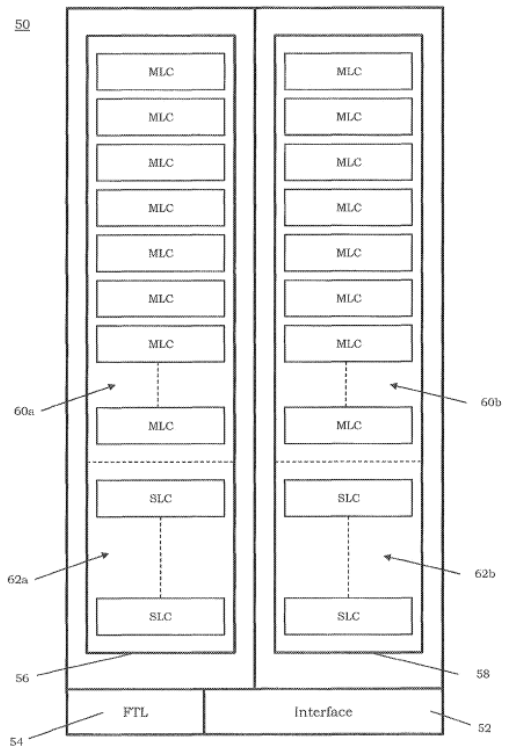
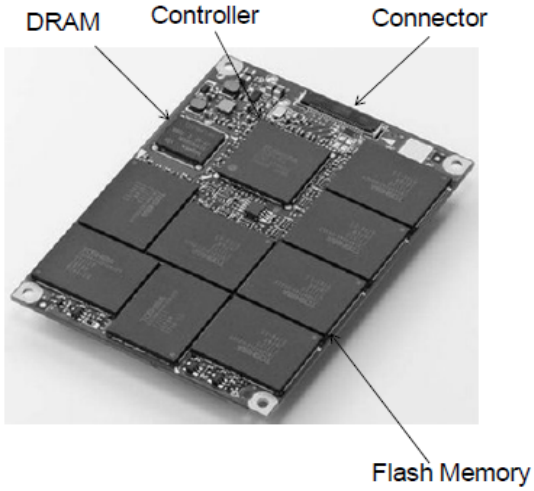



FIG. 4



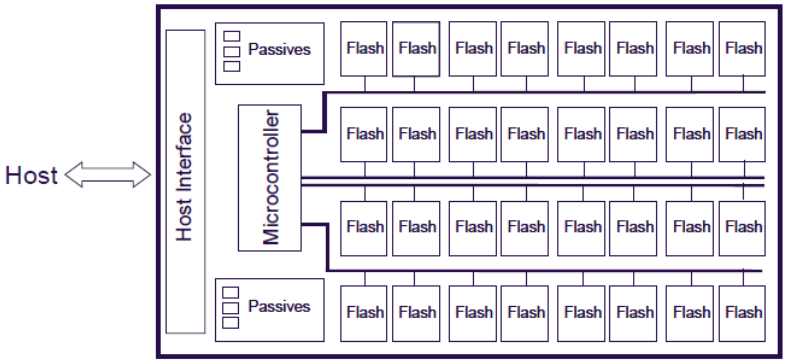




**Fig. 2.32.** Block diagram of a SSD

The distinction of "MLC" from "SLC" in the '612 specification and claims requires circuitry – not just a storage cell – different from "SLC" to program two logical pages into one physical page in "MLC" (Sechen ¶¶ 31-42). [6] Such circuity is shown in Fig. 6a of the incorporated Embedded RAM Patents disclosure (Ex. 1004) for a NAND flash module[7] (called "flash memory"):

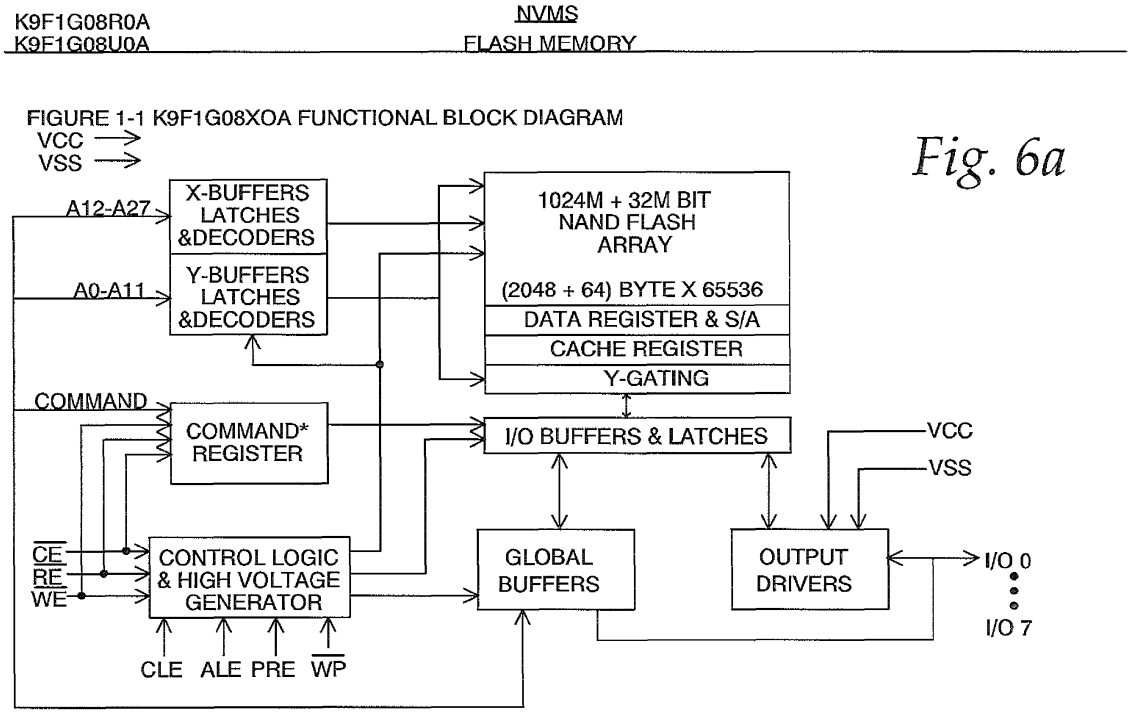



Fig. 6a

[6] "Pseudo-SLC" (two-state or one-bit) use of MLC is not "SLC" (Sechen ¶ 46); despite that use since at least 2001, there is no mention of it in the 2011 specification.

[7] Distinct SLC and MLC modules of this type used in the Moshayedi (Ex. 1043) hybrid system. (Sechen note 16.)

This is compared to the textbook depiction at paragraph 27 of the Sechen declaration:

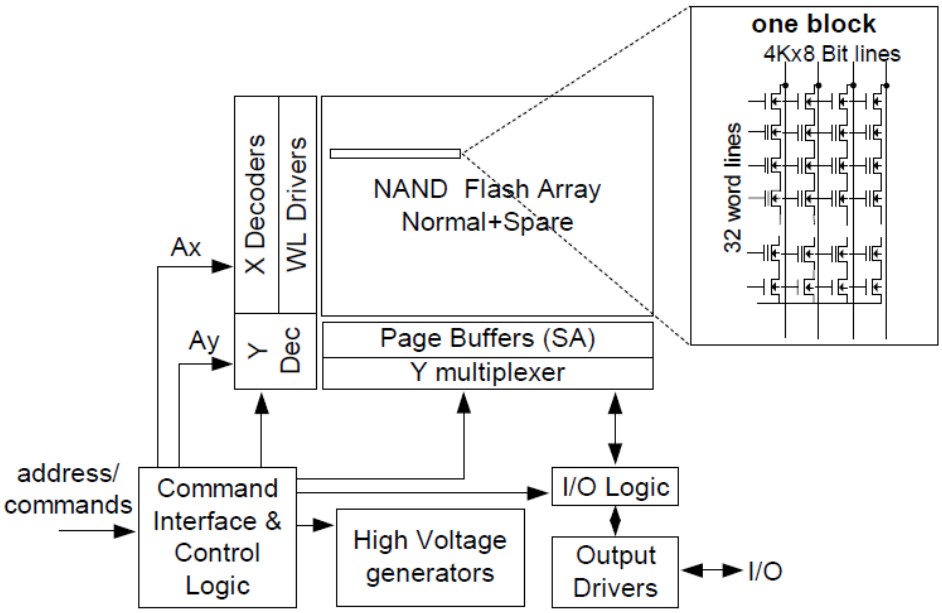



**Fig. 15.1.** NAND Flash memory block diagram

Thus, even if a POSITA needed to look to the specification to understand the references to SLC and MLC modules, the specification (including the incorporated disclosure) shows exactly the understood meaning. There is no disclosure in the specification of anything else. There is no reference to embedded memory and no reference to "SLC mode," although both were long known to the POSITA. Rather than the applicant acting as his own lexicographer to impermissibly change "SLC flash" from its ordinary and customary meaning to a POSITA, the specification prediction that CPM, RRAM or MAGRAM will replace "SLC flash" and "MLC flash" (2:10-12) confirms both the specification contemplation that the flash entities are distinct and that the alternative technologies are substitutable as *ejusdem generis*

(of the same kind) of memory function – even though they are distinguished as "write in place" instead of "erase-before-write" (2:22-25).

Specification Fig. 3A step 116 "match" (also 6:43 and 6:46) between data to be written ("retained data") and data as written supports the construction of "comparing" (8:24) as direct bit-by-bit match, unlike indirect methods such as ECC. This was corroborated in the '300 patent prosecution express surrender of coverage of ECC error detection (Oct. 8, 2020, Amendment at 8-9 [Ex. 1012 at 36-37]), which was repeated in a '546 prosecution argument (Sept. 22, 2023, Amendment at 13] [Ex. 1014 at 13] [requiring comparison in "two data stores"]).

Other important constructions are that the terms "memory space" and "memory element" are indefinite, as well as other terms that are indefinite in their usage in the claims, such as "mapping . . . as necessitated by the system to maximize lifetime." These are argued as indefinite in the § 112(b) Ground 2 below.

Petitioner reserves the right to argue more specific constructions in response to Patent Owner's responses.

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*Grounds for Review Under 37 C.F.R. § 42.204(b)(4)-(5)*:

## VII. GROUND 1: THE CHALLENGED CLAIMS LACK A WRITTEN DESCRIPTION DESCRIBING THE CLAIMED SUBJECT MATTER IN ACCORDANCE WITH 35 U.S.C. § 112(a).

As reviewed at paragraphs 72-76 of the Sechen declaration, (a) the abstraction in the '300 patent of "memory space" and "memory elements," departing from the disclosed and prior patents' hybrid memory system of SLC and MLC NAND flash modules with NAND flash-defined blocks and (2) the partial return in the '546 patent to modules and elements of suggested physicality. The Lifetime Patents seek exclusivity for operation of a genus of alternative technologies having greater endurance than MLC based on recitation of ordinary NAND flash operation and the SLC module species of NAND flash operation. However, even where substantial research was shown, as in *Amgen Inc. v. Sanofi*, 598 U.S. 594, 610 (2023), the specification must enable the full scope of the invention. Patent Owner should not be allowed to avoid showing possession of an innovative memory system by claiming NAND flash operation steps in abstract, unsupported terms of "memory space" and "memory element." As shown in Section IX, there is no invention here at all, but even before we get there, the '612 patent fails under the following 35 U.S.C. § 112(a) defects among the many that Dr. Sechen identifies at paragraphs 81-91 of his declaration:

**A. The Challenged Claims, Limited by "Memory Space," Particularly Step [1a] of "Maintaining an Address Table" for "Memory Space," Are Unsupported Under 35 U.S.C. § 112(a).**

The Challenged Claims lack a written description describing the claimed subject matter in accordance with 35 U.S.C. § 112(a) because the term "memory

space" (7:43-47, 8:3) is mentioned in the specification (other than in the summary of the '612 claims) only as a measure of memory capacity (5:23-25), and "space" otherwise referring to commercial market share (2:47). (*See* Sechen ¶ 74.) Unless that recited capacity is read to limit the "maintaining an address table" step, the recitation of "memory space" (as well as "(MLC) space" and "(SLC) space") in the claims is unsupported in the specification, which thus fails to enable a POSITA to practice the claimed invention at all, much less with substitution of alternative technologies that may have other limitations on an address table than "erase-before-write" NAND flash operation assumed. Certainly, the term is unsupported for other than NAND flash operation, for which there is no showing in the specification that such a claimed invention was possessed. The Challenged Claims thus fail as unsupported under 35 U.S.C. § 112(a).

### B. The Challenged Claims, Limited by Step [1b] of "Mapping . . . As Necessitated by the System To Maximize Lifetime," Are Unsupported Under 35 U.S.C. § 112(a).

The Challenged Claims lack a written description describing the claimed subject matter in accordance with 35 U.S.C. § 112(a) because the specification does not disclose "mapping . . . as necessitated by the system to maximize lifetime" (7:50-52). As reviewed in paragraphs 74 through 77 of the Sechen declaration (Ex. 1002), the '300 patent introduced (and the '546 and '612 patents retained) this limitation without any support in the common specification, with no mention of "maximiz[ing]

lifetime" of anything. The common specification makes no claim to maximize lifetime, but only "to boost the lifetime" or "provide long lifetime" for a NAND flash storage system. (Sechen note 14.) Dr. Sechen reviews the notions of extending or improving expected useful lifetime of a NAND flash memory system in the extensive background art, including through wear leveling, garbage collection and bad block management, with preference under some circumstances in operation of a hybrid SLC-MLC NAND flash system to map and write to SLC or pseudo-SLC (¶¶ 27-29 and 43-59, particularly notes 12 and 14). Some of these different (and not "necessary"[8]) approaches to enhancing useful lifetime of a NAND flash memory

[8] The only "mapping" that is "necessary" for the disclosed systems is the particular L2P mapping necessary for operation of NAND flash memory operation with its defining erase-a-block-before-writing requirement admittedly inapplicable to proposed alternative technologies. Moreover, that "mapping" in the context of a hybrid SLC and MLC NAND flash module, if it resulted as ordinarily in subsequent writing (preceded by erasure for data-occupied blocks), would *always* stress and thus incrementally decrease the useful lifetime of one block, leaving the other blocks, including any from which writing is remapped, at the same stage in life (subject to time effects) (Sechen ¶ 75). Thus, not every "mapping" would "maximize lifetime," while a certain mix of "mappings" might be calculated to avoid premature end to

system were acknowledged in the specification BACKGROUND (Sechen ¶ 62, note 14; 3:11-33: NAND flash wear leveling "prolonging the service life"). Dr. Sechen discusses the many ambiguities of the "maximize lifetime" clause at paragraphs 74, 75 and 82, including its abandonment of the Lifetime Patents theme of preferential mapping to an SLC NAND flash module and how, without that mechanism, there is no enablement of "maximizing lifetime." The bottom line is that the specification does not disclose any "mapping . . . necessitated by the system to maximize lifetime" of even the disclosed SLC-MLC NAND flash memory system, much less of memory systems of other than SLC-MLC NAND flash. The specification thus does not enable a POSITA to practice the claimed invention limited by the mapping step to "maximize lifetime" or show that the inventor actually "possessed" that claimed invention. Thus, the Challenged Claims fail under 35 U.S.C. § 112(a).

### C. The Challenged Claims Are Indefinite Under 35 U.S.C. § 112(a) Because Step [1c] of "Controlling" Is Unsupported.

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reliability of enough components to compromise the intended use of the system (*id.* note 14). One might "maximize lifetime" without consideration of cost by mapping only to physical memory that does not degrade by such mapping, but it such a system would not include SLC and MLC modules or steps [1f]-[1j] particular to hybrid SLC-MLC operation.

The controlling step [1c] is recited as performed "during Write access operations and Read access operations" on various "memory element[s]," "associated memory space" using "at least one controller." "Memory element[s]" and "memory space" are unsupported (Sechen ¶ 74 above). "Write access operations and Read access operations" are unsupported, as the terms do not appear in the specification, except by reference to a POSITA's understanding of NAND writing and reading. No details are provided as to what "controlling" means except by reference to that understanding, which includes erase-before-write, writing to pages and reading pages – it is not explained in the specification how it is applicable to the direct-write (and byte-level erase) alternative technologies. While the specification and claims gave physical structure to MLC and SLC memories and modules, no structure was given to the abstract "controller" (Sechen ¶ 66). Thus, the Challenged Claims fail under 35 U.S.C. § 112(a).

### D. The Challenged Claims, Limited by "Memory Element" in Steps [1c], [1e], [1f] and [1h], Are Unsupported Under 35 U.S.C. § 112(a).

The Challenged Claims lack a written description describing the claimed subject matter in accordance with 35 U.S.C. § 112(a) because the term "memory element" (8:1-2 {step [1c]}, 8:7-8 {step [1e]}, 8:11-13 {step [1f]}, and 8:19-26 {step [1h]}) is not even mentioned in the originally filed common specification – only in the summary added for the '612 claims (where it must be considered new matter).

As reviewed in paragraphs 74, 76 and 77 of the Sechen declaration, the '300 patent substituted (and the '546 and '612 patents retained) the terms "memory space" and "memory elements" for the NAND flash modules in place of the flash characteristic "plurality of individually erasable blocks" that were recited in the '298, '385 and '240 patent claims. However, the term "memory element" appears nowhere in the common specification, and "element" appears only as a boilerplate reference to claim elements (7:38-39).[9] To the extent that "memory elements" is considered a material limitation of the claimed system (as they must be), it is unsupported in the specification and the Challenged Claims fail as unsupported under 35 U.S.C. § 112(a).

### E. The Challenged Claims, Limited by Step [1i] of "Remapping . . . the Address Space to a Different Physical Range of Addresses," Are Unsupported Under 35 U.S.C. § 112(a) and Fail To Enable a Useful System for Storing Data.

The lack of support for and the indefiniteness of "space," including "address space" (Sechen ¶ 74) impart the same defects to this recitation, leaving at least the

[9] The word "element" is mentioned in the incorporated Embedded RAM Patents that described its Fig. 2 as an "exemplary NAND memory integrated circuit as one element of the NVMS" ('Rao '452 [Ex. 1004] 2:52-53), which corresponds to a NAND flash memory module.

question of how an "address space" is mapped to a "physical range," then remapped to a different one, which in any case is unsupported in those terms. Step [1i] is inoperative to extend lifetime of a memory system or component, since remapping and programming after a first programming incrementally decreases the lifetime of some target "physical range" without any benefit for the system as a whole (unlike the abandoned possible benefit of preferential remapping to SLC). Thus, the Challenged Claims fail under 35 U.S.C. § 112(a).

### F. Claim 3, Modifying Method Claim 1 to Operation of a System with an Embedded Memory in the "At Least One Controller," Is Unsupported and Inoperative Under 35 U.S.C. § 112(a).

Claim 3, "further comprising embedding at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements in the at least one controller" (8:40-43) is unsupported insofar as there is no mention of "elements" in the common specification (Sechen ¶ 74), much less "embedding" such "elements," or disclosure of any of these "elements in the device controller (or of any physical content of the controller). The incorporated Embedded RAM Patents, *e.g.*, Rao '452 (Ex. 1004) relate to use of volatile memory on the flash chip, although they show at Fig. 3 a controller with registers presumably using temporary memory. Dr. Sechen observes, at paragraph 90, that only an SRAM could possibly be embedded in the controller (typically a discrete chip as shown at Sechen ¶ 27), because the fabrication process for DRAM, such as suggested in Lifetime Patents

Fig. 1 (20) and Fig. 3A (102), is not compatible with the fabrication process for a CMOS controller chip. Obviously, MLC and SLC, in the quantity for which the '612 patent would be operative, could not be embedded in the controller. Claim 3 is independently unenabled under 35 U.S.C. § 112(a).

### G. Claim 3, Modifying Method Claim 1 to Operation of a System with an HDD Embedded Memory in the "At Least One SLC Nonvolatile Memory Element," Is Unsupported and Inoperative Under 35 U.S.C. § 112(a).

Claim 7, "wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD)" (8:53-55) is on its face contradictory if "element" is understood to be some physical component of an SLC memory module (as in claim 1, 8:2-3), which is clearly understood at least to involve NAND flash technology described in the specification. A POSITA would understand that it is physically impossible to install or somehow include a hard disk drive (HDD) on an SLC chip since the HDD is many orders of magnitude larger. (Sechen ¶ 91.) Claim 7 is independently unenabled under 35 U.S.C. § 112(a).

## VIII. GROUND 2: THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(b).

Claims 1-7 are invalid for indefiniteness under 35. U.S.C. 112(b) (formerly para. 2), because they recite limitations that, under *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898 (2014), considering the claims as a whole and as informed by the extrinsic record, fail to inform a POSITA with reasonable certainty

about the scope of the claimed invention. A patent must be "precise enough to afford clear notice of what is claimed, thereby 'appris[ing] the public of what is still open to them.'" *Id.* at 909. "Otherwise there would be a zone of uncertainty which enterprise and experimentation may enter only at the risk of infringement claims." *Id.* Among the multiple defects in the '612 patent claims that Dr. Sechen identifies at paragraphs 81-91, Petitioner raises here the following 35 U.S.C. § 112(b) defects:

### A. The Challenged Claims, Limited by "Memory Space," Particularly Step [1a] of "Maintaining an Address Table" for "Memory Space," Are Indefinite Under 35 U.S.C. § 112(b).

As reviewed at Section VII(A) (§ 112(a) lack of adequate written description), the meaning of the term "memory space" (7:43-47, 8:3) is only disclosed only as a measure of memory capacity, rendering the Challenged Claims that recite the term invalid under that statutory provision. If the term survives that challenge, it is nonetheless indefinite as to whether it refers to "logical" memory locations in a NAND flash L2P table or to something physical, such as the physical capacity available for NAND flash reading, writing and erasing for those logical memory locations. It is further indefinite by including a description of the object (address table) using mismatched concepts of MLC and SLC memory "spaces" and nonvolatile "memory" and "memory element." The term is even more indefinite in the context of other than NAND flash operation, which would not have the POSITA-

understood NAND flash L2P mapping and writing structure. The Challenged Claims thus fail as indefinite under 35 U.S.C. § 112(b).

### B. The Challenged Claims, Limited by Step [1b] of "Mapping . . . As Necessitated by the System To Maximize Lifetime," Are Indefinite Under 35 U.S.C. § 112(b).

As reviewed in paragraphs 74, 75 and 82 of the Sechen declaration, there are multiple axes of uncertainty in the claim 1 recitation of "mapping . . . as necessitated by the system to maximize lifetime" (7:51-52), carried over from the '300 patent extreme abstraction of previously claimed systems. Even if the limitation survives the §112(a) arguments in Section VII(B), there remain the questions, first, of at least what "mapping" is implicated. Every mapping (which is necessary for NAND flash memory operation, but perhaps not for alternative, "write in place" technologies) in the life of a NAND flash system, if followed ordinarily by writing, decreases expected useful lifetime. Claim 1 (and particularly the "maximize lifetime" clause) fails to specify any user-elected strategy/configuration of NAND flash mapping to distribute wear (stress), as reviewed extensively in the Sechen declaration (¶¶ 27-29, 43-45, and 48-59, particularly notes 12 and 14; Duann [Ex. 1034]; Lee '794 [Ex. 1041]; Surtardja [Ex. 1042]; Moyashedi [Ex. 1043]; and Gavens [1045]). The '612 patent omitted any claim to the DETAILED DESCRIPTION's two-sentence ("hot" block v. "cold" block) "wear leveling" (to the SLC or MLC modules) embodiment (6:58-7:3). It *might* refer to the step [1i] "remapping" (8:29) after failure of the step

[1h] "data integrity test" elements of claim 1 (8:18-28) which roughly follow the NAND flash method steps in Figs.3A and 3B, explained at 6:19-57. However, step [1h] is indefinite as to when the test and remapping are performed (*see* Section VIII(E)) and step [1i] is indefinite as to what is remapped to what (*see* Section VIII(G)) and step [1j] is indefinite as to what is transferred after remapping (*see* Section VIII(H)). On this uncertainty of what mapping is implicated, a POSITA and the public are not clearly apprised of what is claimed. Accordingly, the Challenged Claims fail as indefinite under 35 U.S.C. § 112(b).

### C. The Challenged Claims Are Indefinite Under 35 U.S.C. § 112(b) Because Step [1c] of "Controlling" Is Indefinite.

The lack of support identified at Section VII(C) for step [1c] "controlling" leave it without specific meaning, rendering the step indefinite. The recited step is in essence a step for a vague function of "controlling" undefined "Write access operations and Read access operations" among undefined "memory element[s]" and "associated memory space" using and undefined "at least one controller." Thirty-five U.S.C. § 112(f) has been applied through § 112(b) to find indefinite a functionally claimed limitation of a general term ("nonce" word) which is not supported in the specification by adequate disclosure of structure (physical or algorithmic). *E.g.*, *Rain Computing, Inc. v. Samsung Electronics America, Inc.*, 989 F.3d 1002 (Fed. Cir. 2021). The same considerations of providing the public notice

of what exclusivity is claimed applies here to render step [1c] and the Challenged Claims indefinite under 35 U.S.C. § 112(b).

### D. The Challenged Claims, Limited by "Memory Element," Particularly Steps [1e], [1f] and [1h] of "Maintaining an Address Table" for "Memory Elements," Are Indefinite Under 35 U.S.C. § 112(b).

A POSITA would not understand the scope of the term "memory element", even in the context of NAND flash – whether it refers to a cell, a block or something else less than a memory or memory module. (Sechen ¶ 84.) Thus, the Challenged Claims indefinite under 35 U.S.C. § 112(b).

### E. The Challenged Claims Are Indefinite Under 35 U.S.C. § 112(b) Because It Is Uncertain When the Recited "Data Integrity Test" Step [1h] Is Performed.

In the embodiment described in the specification with two separate banks of MLC and SLC, "the controller conducts a data integrity test after every write." (5:17-18 [emphasis added].) However, in the same column description of the (perhaps misnamed) "read-modify-write" scheme, the read-after-every-write execution is qualified by "if time permits." (5:64-66.) The claim itself is silent. Is a single read-after-write-and-compare initiated by a user an infringement charged to the manufacturer? A POSITA would not necessarily read claim 1 to require [1h] performing after every "at least a Write operation" (yet another term unsupported in the specification) for the entire lifetime of the memory system. It was observed (Sechen ¶ 53) that bit-by-bit comparison of "stored data" and "retained data" implied

in the specification Figs. 3A and 3B (which do not show, and the explanation does not mention ECC) for step [1h2] is very inefficient; reading the stored data into controller memory [1h1] to be compared to the retained data left there by [1f1] severely affects data throughput. This is in stark contrast to the prior art SanDisk systems that keep even incorrectly written data if they can be corrected by ECC upon reading and even defer deploying ECC until a statistically appropriate time. (*See* Sechen note 12.) It makes a substantial difference which reading is chosen, and the claim and specification do not provide adequate notice to the public. Because of this uncertainty, the Challenged Claims are invalid under 35 U.S.C. § 112(b) as indefinite.

### F. The Challenged Claims Limited by Step [1h2] of "Comparing the Stored Data in the Controller Memory in the Given One of the MLC Nonvolatile Memory Elements" Are Indefinite Under 35 U.S.C. § 112(b).

The grammatical ambiguity of the referent of the preposition "in" leaves ambiguous whether the stored data is in the controller memory or the MLC memory**.** (Sechen ¶ 86.) The indefiniteness of step [1h2] invalidates the Challenged Claims under 35 U.S.C. § 112(b) as indefinite.

### G. The Challenged Claims Limited by Step [1i] of "Remapping . . . the Address Space to a Different Physical Range of Addresses" Are Indefinite Under 35 U.S.C. § 112(b).

The lack of support for and the indefiniteness of "space," including "address space" (Sechen ¶ 74 above) impart the same defects to this recitation: how does an

"address space" get mapped to a "physical range," then remapped to a different one? (Sechen ¶ 87.) Again, there is lack of clarity whether "space" is a quantity of space, is "logical" space as a list of assigned logical "sectors" conforming to hard disk drive operation or the physical locations in flash memory (Sechen ¶ 27). The indefiniteness of step [1i] invalidates the Challenged Claims under 35 U.S.C. § 112(b) as indefinite.

## IX. GROUND 3: CLAIMS 1-7 OBVIOUS UNDER 35 U.S.C. § 103 OVER GAVENS IN VIEW OF POSITA KNOWLEDGE.

The '612 patent claims are obvious under *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007) because there is no gap between them and the prior art operation of hybrid SLC-MLC NAND flash systems: many prior art instances meet those claims, which have been abstracted to cover alternative technologies. Independent claim 1 of the '612 patent claims a method of operating a hybrid SLC-MLC memory system with known, necessary L2P mapping operations, a "data integrity check" feature, and an overall limitation of "mapping . . . to maximize lifetime." Such operation of hybrid SLC-MLC memory systems including actually useful "data integrity checks" and practical approaches to avoid premature unreliability of those systems has been detailed in multiple prior art textbooks, articles and patents reviewed in Sechen Declaration Section V(C). Gavens (Ex. 1045), among the SanDisk portfolio and

incorporating by reference others of that portfolio[10] currently appears to the Petitioner as the one reference in which the recited limitations of '612 claim 1 are most clearly disclosed in a range of compatible embodiments. Since the 2001 [Cho, Ex. 1039] emergence of the terms "multi-level program cell" (MLC) memory and (thereby distinguished) "single level program cell" (SLC) memory, there have been implementations of hybrid MLC memory modules and SLC memory modules availing of the endurance advantages of SLC. (*E.g.*, Lee '794 [Ex. 1041], Sutardja [Ex. 1042], and Moshayedi [Ex. 1043]. Many, including those disclosed in the

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[10] *See, e.g.*, U.S. Patent No. 6,456,528 to Chen ("Chen '528"), Ex. 1040, incorporated by reference at Gavens 16:29-40; U.S. Patent Appl. Pub. No. 2011/0153912 ("Gorobets '912"), Ex. 1044, incorporated by reference at Gavens 20:53-59; U.S. Patent No. 5,930,167 to Lee et al. ("Lee '167"), Ex. 1050, incorporated by reference at Gavens 17:57-67; U.S. Patent Appl. Pub. No. 2010/0172180, to Paley et al. ("Paley '180), Ex. 1051, incorporated by reference at Gavens 8:41-42. Hereinafter, it should be understood that reference to a specific portion of any of the above references is understood to be disclosed by Gavens due to incorporation by reference, as if the incorporated document was explicitly contained in Gavens.

SanDisk patent portfolio, involve the partitioning and configuration of some MLC blocks for one-level (two states) or pseudo-SLC (pSLC) operation. As reviewed at Sechen Declaration paragraph 46 and in Gavens itself (*e.g.*, 12:6-10) the pSLC mode of operations enjoys superior endurance compared to MLC in multi-level mode – though not as superior or as fast as "real" SLC which uses different circuitry – and it would be obvious to a POSITA to have one MLC module operating entirely in pSLC mode with an expectation of success for the relative superiority to MLC in multi-level mode[11] or use a "real" SLC module as understood by a POSITA from the embodiments actually disclosed in the specification. (Sechen ¶ 93.)

### A. Claim 1 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

If it is not invalidated for Grounds 1 and 2 (Sections VII and VIII above, addressed below are the limitations recited in claim 1 as set forth in the groupings as printed in the '612 patent, further labeled as in Section V(C) above:

[11] This would meet the Lifetime Patents specification suggestion that "SLC module" may be "any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash" and faster ('298 4:10-14).

**[1Pre] A method for storing data comprising:**

Petitioner contends the claimed method is only enabled for hybrid systems of SLC and MLC NAND memory modules storage but does not contend that the preamble of claim 1 is limiting.

(Sechen ¶ 96): To the extent the preamble is limiting, Gavens discloses "a system for storing data," namely, the "flash memory device 90" that includes memory array 200. ( Gavens, Fig. 1, ref. 90 and 16:41-17:20).

> **[1a] maintaining an address table for a memory space containing volatile memory and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space and the volatile memory includes a random access volatile memory element;**

(Sechen ¶ 97): **[1a1]** To the extent that this clause is not invalid as explained at least in paragraph 81 above, and "memory space" is understood to include all *physical* memory in the claimed system, Gavens discloses, or at least renders obvious, "memory space containing volatile memory space."

(Sechen ¶ 98): Gavens discloses memory containing volatile RAM and non-volatile memory array. (Gavens, 1:26: RAM; 1:18: Non-volatile memory; Fig. 1: Memory array 200 in memory chip 100.) Gavens states that his invention "relates to the operation of re-programmable non-volatile memory systems such as semiconductor flash memory, and, more specifically, to handling and efficient managing of errors in memory operation." (1:17-20.) Gavens, by its incorporation

of Gorobets '912, explicitly discloses volatile RAM (Gorobets '912, ¶ 130 and Fig. 20: "Data is transferred from a host 501 onto the memory 503, where it is initially stored on the *volatile buffer memory RAM 511*, which is typically part of the controller.) (emphasis added). The volatile RAM disclosed by Gorobets necessarily includes random access volatile memory elements.

(Sechen ¶ 99): **[1a2]** Gavens' non-volatile memory array includes a first portion of pseudo-SLC memory and a second portion of MLC memory. Specifically, Gavens states that the first portion has each memory cell storing one bit of data and the second portion has each memory cell storing more than one bit of data. (4:32-34; 17:21-23.) The high-density storage portion (D3) has each memory cell storing 3 bits of data. The low-density storage portion (D1) has each memory cell storing 1 bit of data. (5:15-17, 50-53, 16:22-24, 20:31-34.) As disclosed in Fig. 14A, col. 16:15-22, the array of memory cells 200 is partitioned into a first portion 410 of lower density and a second portion 420 of high density having each cell storing multiple bits. For further reference, see: Fig. 7, col. 11:55-56, 12:6-7: A binary memory or single-level cell (SLC) memory has a population of cells with each cell in one of two possible states; Fig. 8, col. 12:11-12, 31-33: A multi-state memory, for example, a triple-level cell or multi-level cell (TLC) or D3 memory has a population of cells with each cell in one of eight possible states, whereas a multi-level cell (MLC) or D2 memory has a population of cells with each cell in one of

four possible states; Abstract, col. 6:18-21, 15:62-66, 16:16-22: The memory has a first portion operating with lower density storage and a second portion operating with a higher density; Fig. 15 ref. 500, col. 17:27-29: Configuring memory into a first portion having memory cells operating with a margin of error larger than that of a second portion; in the incorporated Gorobets '912:

- Gorobets '912 fig. 1, ¶ 56: RAM 130 in the controller 100;
- Gorobets '912 fig. 11, ¶ 109: Cache RAM 102 in the controller;
- Gorobets '912 fig. 20, ¶ 130: Volatile RAM 511 in the controller and in the memory 503;
- Gorobets '912 ¶ 18: Controller RAM.

These configuration details are understood by a POSITA to be consistent with the system disclosed in Gavens, which would be understood, as incorporated disclosures below, to focus on different features of the more inclusive SanDisk NAND flash memory systems. Not only are the features disclosed, but in the analysis here, they are already combined with more than just a reasonable expectation of success. Thus, Gavens and its incorporated references disclose claim element **[1a]**.

**[1b] [1b1] mapping logical and physical addresses adaptable to the system by the address table, wherein the [1b2] mapping is performed as necessitated by the system to maximize lifetime, and [1b3] wherein the mapping maps data in at least one of volatile or nonvolatile memories;**

(Sechen ¶ 101): Gavens discloses the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories.

(Sechen ¶ 101): Relative to limitation **[1b1]**, Gavens discloses that the directory maps logical addresses and physical addresses adaptable to the NAND flash memory device. Relative to limitation **[1b2]**, to the extent it can be understood if it survives 35 U.S.C. § 112 scrutiny, it would met by the kind of NAND flash wear-management disclosed in Gavens and long known in the art (¶¶ 28, 29, 40-45, and 51-56 above) (or alternatively, the remapping of limitations **[1f]**, **[1g]** and **[1i]**): the mapping is performed as necessitated (implemented) by the flash memory device to maximize (increase) the (expected) lifetime of the flash memory device, and **[1b3]** the mapping maps a block of data in the non-volatile memory array. (8:36-39: A memory block management system implemented in the controller maps the logical sectors to the physical structure of the memory array; 15:2-6: An important consideration for flash memory is that it has an endurance problem as it ages with use. The error rate increases with the number of program-erase cycling; 16:34-37: It

is desirable to have longer operational life of memory cells (relates to maximizing lifetime); Fig. 15 ref. 550, col. 17:39-40: Identifying the last written copy as valid data for a subsequent read (relates to mapping); 11:19-22: The group of cells erasable together consists of one or more addressable erase units. The erase unit or a block stores one or more pages of data (relates to mapping blocks or pages). A page is a minimum unit of programming and reading; 21:21-23: Each block contains data from a well-defined group of logical addresses; 5:41-45: A hot count tracks the number of times each physical block has been cycled through erase and program operations.

(Sechen ¶ 102): Incorporated reference Paley '180 [Ex. 1051] Figs. 8-9, ¶¶ 155-159, 201-202 discloses: The memory-side memory manager 300 is implemented in the controller 100 to manage the storage and retrieval of the data of host logical sectors among metablocks of the flash memory. The memory manager 300 maintains system control data and directory data associated with its operations. The memory manager 300 comprises a back-end system 320, which includes a number of software modules including a media management layer 330 and a dataflow and sequencing layer 340. The media management layer 330 organizes logical data storage within a flash memory meta-block structure. The dataflow and sequencing layer 340 sequences and transfers sectors of data between a front-end system and a flash memory. The dataflow and sequencing layer 340 includes a flash

control layer 346. The memory manager 300 is preferably implemented in the controller 100 and translates logical addresses received from the host into physical addresses within the memory array.)

(Sechen ¶ 103): In addition, incorporated reference Gorobets '912 [Ex. 1049], Figs. 8-9, ¶¶ 95-99 discloses: The memory-side memory manager 300 is implemented in the controller 100 to manage the storage and retrieval of the data of host logical sectors among metablocks of the flash memory. The memory manager 300 maintains system control data and directory data associated with its operations. The memory manager 300 comprises a back-end system 320, which includes a number of software modules including a media management layer 330 and a dataflow and sequencing layer 340. The media management layer 330 organizes logical data storage within a flash memory meta-block structure. The dataflow and sequencing layer 340 sequences and transfers sectors of data between a front-end system and a flash memory. The dataflow and sequencing layer 340 includes a flash control layer 346. The memory manager 300 is preferably implemented in the controller 100 and translates logical addresses received from the host into physical addresses within the memory array.)

(Sechen ¶ 104): Incorporated reference Lee '167 [Ex. 1050] 2:54-3:7 discloses that it is advantageous to: evenly wear the memory (*i.e.*, maximize lifetime); avoid using one portion of memory much more than other portions; maintain separate

counts of the number of times that each sector has been erased and programmed to even the wear among the sectors. See also Chen '528 [Ex. 1040] 10:41-60: Storing the most frequently written data in SLC and less frequently written data in MLC avoids the need to replace blocks that reach their endurance limit-relates to maximizing lifetime).

(Sechen ¶ 105): Thus, element **[1b]** "maximizing" is met by the specific system life-extending approaches disclosed in Gavens, either background "wear leveling" reviewed above or remapping after integrity check which is disclosed in Gavens to meet elements **[1h]** and **[1i]**.

> **[1c] controlling during Write access operations and Read access operations [1c1] a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element and [sic] [1c2] at least one SLC memory module including at least one SLC nonvolatile memory element and [sic] associated memory space using at least one controller;**

(Sechen ¶ 106): Gavens discloses at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements. For example, Gavens discloses a controller that manages read operations and write operations on memory. (Fig. 1 ref. 102; 8:17-18, 32-35: A controller 102 manages one or more memory chips 100 in the memory device 90. The controller 102 controls and manages higher level memory operations (*e.g.*, write) on the memory

array 200; 2:56-58: A controller performs intelligent and higher level memory operations and interfacing.)

(Sechen ¶ 107): As explained at paragraph 93 above, Gavens differs from the claimed SLC and MLC NAND flash modules by having some portions of its aggregated MLC modules partitioned and configured to operate in pseudo-SLC (2-state or 1 bit) mode. (8:18-20 ["The memory chip 100 includes memory array 200 of memory cells with each cell capable of being configured as a multi-level cell ('MLC')]; 18:12-20 [explaining the array of memory cells 200 "partitioned" into portions with higher density (more bits per cell) and lesser density (fewer bits per cell) operation with associated margins of error; 17:59 ["A first portion is configured to store one bit per cell," citing Lee '167) Gavens clearly satisfies the **[1c1]** limitation of multiple MLC memory modules in the understood operation of a NAND flash system that employs Gavens's schemes of preferential writing to lower density memory. As to the **[1c2]** limitation of an SLC memory module, it would be obvious to a POSITA to have one MLC module operating entirely in pSLC mode with expectation of success for the relative superiority to MLC in multi-level mode or substitute a "real" SLC module understood by a POSITA to have even better endurance than pseudo-SLC (see ¶ 43 above), both with a clear expectation of success. Use of dedicated SLC and MLC modules for preferential writing was well-known prior to the priority date (¶¶ 40-42):

(Sechen ¶ 108): Lee '794 (Ex. 1041) discloses an allocation of logical blocks pre-determined to have most frequent writes (updates, such as system data and user directories) to a distinct SLC module and less frequent writes (user data) to a distinct MLC module. (Lee '794 [Ex. 1041] Fig. 2 refs. 226, 228, 5:10-13: The SLC flash memory array 226 portion of the module would include at least one flash memory "element." Likewise, the MLC flash memory array 228 portion of the module would include at least one MLC flash memory "element"; 6:53-7:39: allocation of logical blocks pre-determined to have most frequent writes (updates, such as system data and user directories) to a distinct SLC module and less frequent writes (user data) to a distinct MLC module.)

(Sechen ¶ 109): Sutardja (Ex. 1042) discloses a controller that is adapted to allocate those blocks (understood to be NAND flash) that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module (disclosed as higher-cost, faster memory distinct from another lower-cost, slower memory). (Sutardja [Ex. 1042] ¶ 141).

(Sechen ¶ 110): Moshayedi (Ex. 1043) discloses a controller that is adapted to allocate those blocks (again understood to be NAND flash) that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module (explicitly disclosed as distinct from an MLC non-volatile memory module). (Moshayedi, Ex. 1043 [Abstract] disclosing a system

that keeps frequently written data, which results in frequently erased blocks, in the SLC flash module, and relatively static data in MLC flash module.

(Sechen ¶ 111): Thus, Gavens discloses claim element **[1c]** with the POSITA's knowledge of obvious substitution of a "pure" SLC module for its partitioned and 2-state (pseudo-SLC) configured MLC module.

**[1d] storing received data within a controller memory associated with the at least one controller;**

(Sechen ¶ 112): Gavens discloses a first section 411 for caching in first portion 410. In Gavens, the first memory portion 401 corresponds to SLC, and is divided into a first section 411 and a second section. The first section 411 is used as a cache to temporarily store data that will be written permanently to the second portion (which corresponds to MLC). (Fig. 16A.) Gavens discloses that the first portion serves as a cache for incoming data, so a cache copy of the input data is programmed into the cache. (4:35-37.)

(Sechen ¶ 113): In addition, Gorobets '912 [Ex. 1049], incorporated by Gavens, discloses the step of storing received data within a controller memory (*e.g.*, RAM 511). (Gorobets: Fig. 20 and ¶ 130: "Data is transferred from a host 501 onto the memory 503, where it is initially stored on the volatile buffer memory RAM 511, which is typically part of the controller.") In a similar configuration, Gorobets also discloses RAM 130 which is part of controller 100. (Gorobets, Fig. 1 and ¶ 56.) *See*

*also* Fig. 11 and ¶ 109, referring to cache RAM 102 in the controller. Thus, Gavens discloses claim element **[1d]**.

**[1e] controlling access of [sic] the MLC and SLC nonvolatile memory elements and the random access volatile memory element for storage of the received data;**

(Sechen ¶ 114): Gavens discloses the step of controlling access to the MLC and SLC nonvolatile memory elements and the random access volatile memory element for storage of the received data. Gavens does so in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data.

(Sechen ¶ 115): For example, Gavens discloses that the controller has buffer memory or cache memory for storing data received from a host; the controller controls access of the first portion of SLC memory, the second portion of MLC memory, and the RAM for storing the data; and in a write operation, the controller transfers the data from the buffer memory or the cache memory to the second portion of MLC memory to store the data in the second portion of MLC memory. (Fig. 1 ref. 102, 8:17-18, 32-35: A controller 102 manages one or more memory chips 100 in the memory device 90. The controller 102 controls and manages higher level memory operations (e.g., write) on the memory array 200;12:64-67: As data is

received from a host, a page of data is staged in the controller 102. Further, as discussed above, Gavens discloses, through Gorobets, a volatile RAM in the controller. (Gorobets '912, [Ex. 1049], ¶ 130 and Fig. 20: "Data is transferred from a host 501 onto the memory 503, where it is initially stored on the volatile buffer memory *RAM 511*, which is typically part of the controller.) Due to overlap of claim elements, the discussion of the following (transferring the stored received data . . .) element also includes additional detail regarding this step, and that explanation is incorporated by reference here.

(Sechen ¶ 116): Thus, Gavens discloses claim element **[1e].**

> **[1f] transferring [1f1] the stored received data from the controller memory [1f2] to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one given one of the MLC nonvolatile memory element as stored data;**

(Sechen ¶ 117): Gavens discloses transferring the stored received data from the controller memory to a given on of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one given one of the MLC nonvolatile memory element as stored data.

(Sechen ¶ 118): Relative to limitation **[1f1]**, Gavens discloses the step of transferring stored received data from the controller memory. (12:64-67: As data is received from a host, a page of data is staged in the controller 102. Since Gavens discloses that the data is "staged" in the controller, Gavens must include some kind

of memory inside the controller. This memory would be the claimed "controller memory." Note that the claimed "controller memory" is not necessarily inside the controller but merely "associated" with the controller. That means the "controller memory" could be outside the controller but may be used or controlled by the controller. Further, as discussed above, Gavens discloses, through Gorobets, controller memory (specifically, volatile RAM in the controller) that initially stores received data for subsequent transfer to MLC and SLC elements. (Gorobets '912, [Ex. 1049], ¶ 130 and Fig. 20: "Data is transferred from a host 501 onto the memory 503, where it is initially stored on the volatile buffer memory *RAM 511*, which is typically part of the controller.)

(Sechen ¶ 119): The data page is then written to the memory array 200. (Gavens 16:41-49: The original copy of a page of incoming data is cached.) Gavens discloses that, in addition to staging the data from the host inside the controller, the data is also cached in the first section (using as a cache) of the first portion (i.e., SLC). A first copy of the page of incoming data is written to the second portion; Fig. 14A: Write input data page as first copy of data page in second portion 420 of higher density; Fig. 15 ref. 510, col. 17:30-31: Programming a first copy of a group of input data in the second portion. In Gavens, writing the data to the second portion 420 (MLC) is the claimed feature of storing the received data in the MLC as stored data; 4:18-19, 15:66-67: Data is written to the second portion; 18:1-4: The first portion is

divided into a first section and a second section, and the first section of the first portion serves as a cache.; 17:43-46: The first portion serves as a cache for incoming data, so a cache copy of the input data is programmed into the cache, then a first copy of the data is programmed into the second portion; Fig. 17 refs. 602, 610: Programming a cached copy of a group of input data in a first section of the first portion. Programming a first copy of the group of input data in the second portion.; Fig. 16A, 18:9-12: Cached copy of data page in first section 411 of first portion 410; 5:53-54: Input data is first staged in D1 (SLC) and subsequently folded into D3 (TLC).)

(Sechen ¶ 120): Gavens also discloses the claimed step by incorporation of Gorobets '912 [Ex. 1049]: The data is transferred from the host 501 onto the volatile buffer memory RAM 511 inside the controller, then transferred to the binary section D1 515 of the non-volatile memory 513, and then transferred to the MLC section D3 517 of the non-volatile memory 513. *Id.*, ¶¶ 130, 136, 143-44; abs., ¶ 95: The memory manager 300 is implemented in the controller 100, manages the storage and retrieval of data in the flash memory 200, and maintains system control data and directory data for the flash memory 200 and the controller RAM 130; Id., ¶ 104: Flash memory includes a first portion, which is the main memory, and a second portion, which is a cache of data to be written to the main memory; *Id.*, ¶¶ 24, 109: Use RAM as a controller cache of the memory controller.

(Sechen ¶ 121): Gavens also discloses the claimed step by incorporation of Chen '528 (Ex. 1040) 4:39-41: The controller 20 contains buffer memory for the user data being written to or read from the memory array.)

(Sechen ¶ 122): Gavens further discloses the claimed step by incorporation of Lee '167 [Ex. 1050] Abstract, Fig. 7, claims 1, 4: EEPROM flash memory includes an MLC portion and an SLC portion that is used as a write cache. Incoming data is first written to the SLC write cache, then later, the data is read from the SLC write cache and rewritten to MLC.

(Sechen ¶ 123): Thus, Gavens discloses claim element **[1f]**.

**[1g] retaining the received data in the random access volatile memory as retained data associated with the stored data;**

(Sechen ¶ 124): It would have been obvious to retain the data stored in the RAM so that the data stored in the RAM can serve as cache for faster access of the data in the future. In Gavens, the first portion 401 (which corresponds to SLC) is divided into a first section 411 and a second section. The first section 411 is used as a cache to temporarily store data that will be written permanently to the second portion (which corresponds to MLC). The first section 411 in Gavens is not RAM but is used the same way RAM is used in the industry, i.e., for temporary cache storage. (Fig. Fig. 16A: First section 411 for caching in first portion 410.) (Gorobets '912 [Ex. 1049] ¶¶ 24, 109: disclosing the use of volatile RAM as a controller cache

of the memory controller.) RAM is old and well-known for being used as a cache to temporarily hold data for any later use of the data, and as discussed above, Gorobets expressly discloses volatile RAM in the controller. *See* discussion of element [**1f1**], ¶ 118 above. Gavens and its incorporated references disclose RAM as well as using RAM as cache. Gavens and its incorporated references also disclose using a portion of SLC as a cache (like RAM) to temporarily hold a copy of the data until the writing of a copy of the data to MLC completes successfully. In case the write to MLC fails, the data is not lost but kept in the SLC cache. Gavens also discloses holding a copy of the data in the controller memory in order to perform the data integrity check comparison. It would have been obvious to use the RAM in Gavens (instead of the SLC cache and instead of the controller memory) to store a copy of the data received from the host for the same reasons/advantages, i.e., a copy of the data is available to perform the data integrity check comparison and the data isn't lost if the write to MLC fails. Thus, Gavens discloses claim element **[1g]**.

> **[1h] performing a data integrity test on the stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules [1h1] after at least a Write access operation performed thereon, the performing of the data integrity test further comprising:**
>
> **[1h2] reading the stored data to the controller memory;**
>
> **[1h3] comparing the stored data in [sic] the controller memory in [sic] the given one of the MLC nonvolatile memory elements to the retained data that was associated [sic] with the data in the random access volatile memory by the controller during the Write access operation;**

(Sechen ¶ 125): Gavens discloses the step of performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation.

(Sechen ¶ 126): More specifically, relating to steps **[1h]** and**[1h1]**, Gavens discloses performing a post-write read check on the data stored in the second portion of MLC memory after the write operation by reading the data from the second portion of MLC memory to data laches or the controller and comparing the read data

to a cached copy of the data. (Abstract; 6:22-23: After a copy of data is written to the second portion, the data is read from the second portion and checked for errors; 4:19-21, 15:67-16:1: After the data is written to the second portion, the data is read back to check for excessive error bits. Gavens discloses checking for errors after every write as well as waiting for the wear count to reach a certain threshold and then checking for errors after each write; 5:1-3: After writing to a high density storage portion, a post-write read checks if the error rate is within a prescribed limit (Gavens discloses ECC); 6:4-6, 24:45-50: Post-write reading every memory cell to check what has been written; Title: Post-write read to manage errors.) Although ECC is preferred for less processing, Gavens also discloses a check for errors "by comparison with the original copy which may be cached" (16:47-49).

(Sechen ¶ 127): Relating to step [**1h2**], Gavens also discloses reading the stored data to the controller memory. (Fig. 15 ref. 520, col. 17:32-33: Reading the first copy from the second portion; 4:55-60: The first copy in the second portion and the cached copy in the first portion are loaded into a set of data laches on an integrated circuit chip and compared to check for error bits.) Gavens further discloses the step [**1h3**] of comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated [sic] with the data in the random access volatile memory by the controller during the Write access operation. (16:46-49: The first copy of the data page is read

back in a post-write read to determine if there are any errors by comparing with the original copy which was cached (Gavens discloses bit-by-bit comparison); 18:30-44: The memory array includes data latches onto which the first copy in the second portion and the cached copy in the first portion can be loaded and compared. The comparison is not made at the controller. In Gavens, the sets of data being compared aren't both stored in the controller memory; 12:67-13:4, 29:57-59: Data is read from the second portion, latched in the data latches 430, and shifted out to the controller 102. Although the two sets of data being compared are loaded into data latches 430 inside the memory chip 100 for comparison, the data is shifted out to the controller in order to perform the comparison.)

(Sechen ¶ 128): Gavens' controller 102 compares the ECC in the read data to a second version of ECC computed from the read data. Gavens expressly discloses that this error check may be "either by comparison with the original copy which may be cached **or** by checking the EDC portion of the ECC" (16:47-49 [emphasis added]). Although Rao's direct comparison is wasteful, it was a known alternative. (*See* ¶¶ 50, 52 and 53 above.)

(Sechen ¶ 129): It would have been obvious to compare the data read from the second portion of MLC memory to a cached copy of the data retained in the RAM. RAM is old and well-known for being used as a cache to temporarily hold data for any later use of the data, and as discussed above, Gavens, through incorporation of

Gorobets '912, discloses volatile RAM in the controller. *See* discussion of element [**1f1**] above, incorporated here by reference. Further, Gavens may not have specifically mentioned the use of volatile RAM in his controller because RAM was already an old and well-known technology at the time of his invention. It also would have been obvious to a POSITA at the time of the invention to use Gorobets '912's volatile controller RAM to hold the "retained data" for performing the claimed comparison as part of the data integrity test, because any available memory (whether RAM or SLC cache) can be used to temporarily hold data for the purpose of a data integrity check comparison.

(Sechen ¶ 130): Paley '180 also discloses controller RAM 130 that would be obvious to use for the comparison. (Paley '180 [Ex. 1051], ¶ 155: The memory manager 300 in the controller 100 maintains system control data and directory data associated with its operations among the flash memory 200 and the controller RAM 130.)

(Sechen ¶ 131): Accordingly, Gavens discloses claim limitation **[1h].**

> **[1i] remapping, responsive to a failure of the data integrity test performed on the stored data by the controller, the address space [sic] to a different physical range of addresses; and**

(Sechen ¶ 132): Gavens discloses that a failure of the data integrity test performed on the stored data by the controller results in a remapping of address space to a different physical range of addresses and transfer of data corresponding to the

retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test.

(Sechen ¶ 133): For example, Gavens discloses that a failure of the post-write read check performed on the data stored in the second portion of MLC memory by the controller results in a remapping of the logical address of the data from the physical address in the second portion of MLC memory to a different physical address in the first portion of SLC memory and a rewriting of the cached data to the first portion of SLC memory. (Fig. 14B: If post-write read failed, then rewrite the input data page as a second copy of data page in first portion 410 of lower density; 5:3-7: If post-write read checks results in an error rate above the prescribed limit, then the data is rewritten to another, less error-prone portion that has each memory cell storing fewer data bits per cell; 17:9-12: After the post-write read detects that the number of error bits in the data page has exceeded the predetermined amount, a second copy of the data page is made from the original data which was cached, and the second copy is rewritten to the first portion; 17:50-56: "if the post-write read has detected an excessive amount of error in the first copy, the cached copy in the first portion will replace the first copy in the second portion as valid data. The first copy will become obsolete and *a directory in a block management system embodied in the firmware of the controller (see FIG. 1) will be update[d] to direct subsequent access to the cached copy.*" (emphasis added)).

(Sechen ¶ 134): See also Gavens Fig. 15, refs. 530, 540,17:34-38: Does the error exceed a predetermined number of error bits? If yes, then programming a second copy of the group of input data in the first portion; Abstract, 6:23-25: If the copy in the second portion has excessive error bits, then a copy is written to the first portion; 4:21-22, 16:1-3: If error bits exceed a predetermined amount, then the data is rewritten at the less error-prone first portion; 18:53-67: After a post-write read detects excessive number of error bits, a second copy of the data page is taken from the cached copy and rewritten to the second section of the first portion. The directory in the block management system embodied in the firmware of the controller is updated to direct subsequent access to the second copy.

(Sechen ¶ 135): Thus, Gavens discloses limitation **[1i]**

> **[1j] transferring data corresponding to the retained data [sic] to those remapped physical address [sic] from those physical addresses determined to have failed the data integrity test.**

(Sechen ¶ 136): At 18:53-67, Gavens discloses the step of transferring data corresponding to the retained data to remapped physical addresses from those physical addresses determined to have failed the data integrity test. Specifically, if the write to the second portion (MLC) failed, then a copy is made of the copy of the data that was cached in the first section (cache) of the first portion (SLC) and the newly created copy is stored in the second section of the first portion (SLC). Gavens discloses a cached copy of the data in the SLC cache (i.e., the first section of the first

portion). Even if the "retained data" in this element is interpreted as still being stored in the "random access volatile memory" (that restriction does not appear), then this step is still obvious because Gavens discloses that the copy of the data is stored in the SLC cache (the first section of the first portion), and, as discussed above, use of any available memory for a comparison is obvious, and both RAM and SLC cache were well-known at the time of invention.

(Sechen ¶ 137): Gavens discloses that a failure of the data integrity test performed on the stored data by the controller results in a remapping of address space to a different physical range of addresses (as discussed above) *and* a transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test.

(Sechen ¶ 138): For example, Gavens discloses transferring (rewriting) of the cached data to the first portion of SLC memory. (Fig. 14B: If post-write read failed, then rewrite input data page as a second copy of data page in first portion 410 of lower density; 5:3-7: Upon data integrity failure, the data is rewritten to another, less error-prone portion that has each memory cell storing fewer data bits per cell; 17:9-12: After errors are found, a second copy of the data page is made from the original data which was cached, and the second copy is rewritten to the first portion.)

(Sechen ¶ 139): See also Fig. 15, refs. 530, 540, col. 17:34-38: (also discussed above regarding element [**1i**] Upon error, programming a second copy of the group

of input data in the first portion; Abstract, 6:23-25: Upon data integrity failure, a copy is written to the first portion; 4:21-22, 16:1-3: If error bits exceeds a predetermined amount, then the data is rewritten at the less error-prone first portion; 18:53-67: After a post-write read detects an excessive number of error bits, a second copy of the data page is taken from the cached copy and rewritten to the second section of the first portion. The directory in the block management system embodied in the firmware of the controller is updated to direct subsequent access to the second copy.

(Sechen ¶ 140): See also 4:62-67: After the directory in a block management is updated to direct subsequent access to the cached copy in the first portion (as described in detail above regarding element [**1i**], the cached copy in the first portion replaces the first copy in the second portion as the valid data; 17:15-20: The second copy in the first portion replaces the first copy in the second portion as the valid data. Thus, Gavens discloses element **[1j]**.

* * * * * * * * * * *

(Sechen ¶ 141): In summary, Gavens, with its incorporated references, meets each limitation of '612 claim 1 with known operations of known hybrid SLC-MLC NAND flash memory module systems and mixed SLC-mode and MLC-mode operation of MLC memory, with the POSITA's understanding that Gavens's extensive technology-justified teachings are readily combined and extended (with a

clear expectation of success) to provide the claim's base MLC and SLC modules. The dependent claims do not vary any method steps but are merely limitations of the base hybrid SLC-MLC NAND flash memory system.

### B. Claim 2 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

**[2Pre] The system of claim 1,**

(Sechen ¶ 142): See Section IX(A) for claim 1.

**[2] wherein the FTL is a software module, or a firmware module containing software updates.**

(Sechen ¶ 143): Gavens discloses that the FTL is a software module, or a firmware module containing software updates. For example, Gavens discloses that the memory block management system implemented in the controller is software. (Fig. 1, ref. 102, col. 8:36-39: A memory block management system implemented in the controller 102 maps the logical sectors to the physical structure of the memory array; Fig. 1, ref. 60, 8:44-45: The firmware 60 provides code to implement the functions of the controller 102; 18:64-67: A directory in the block management system embodied in the firmware of the controller is updated to direct subsequent access to the second copy; 4:62-67: A directory in a block management system embodied in the firmware of the controller is updated to render the first copy in the second portion obsolete and to direct subsequent access to the cached copy in the

first portion. The cached copy in the first portion replaces the first copy in the second portion as the valid data.)

(Sechen ¶ 144): See also 17:15-20: A directory in a block management system embodied in the firmware of the controller is updated to render the first copy in the second portion obsolete and to direct subsequent access to the second copy in the first portion. The second copy in the first portion replaces the first copy in the second portion as the valid copy. Thus, Gavens, in view of the knowledge of a POSITA, discloses claim 2.

### C. Claim 3 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

#### 1. [3Pre] The system of claim 1,

(Sechen ¶ 145): See Section IX(A) for claim 1.

#### 2. [3] wherein at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller.

(Sechen ¶ 146): Gavens discloses at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller.

(Sechen ¶ 147): For example, Gavens, by incorporation of Gorobets '912, discloses that the RAM is embedded in the controller. (20:53-59: The entire disclosure of Gorobets '912 [Ex. 1049] is incorporated by reference:

- Gorobets '912 fig. 1, ¶ 56: RAM 130 in the controller 100;

- Gorobets '912 fig. 11, ¶ 109: Cache RAM 102 in the controller;
- Gorobets '912 fig. 20, ¶ 130: RAM 511 in the controller;
- Gorobets '912 ¶ 18: Controller RAM.)

(Sechen ¶ 148): See also Gavens (8:40-43: The entire disclosure of Paley '180 [Ex. 1050] is incorporated by reference:

- Paley '180 Fig. 1, ¶ 119: RAM 130 in the controller 100;
- Paley '180 Fig. 15, ¶ 197: Cache RAM 102 in the controller).

(Sechen ¶ 149): Thus, Gavens, in view of the knowledge of the POSITA, discloses claim 3.

### D. Claim 4 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

#### 1. [4Pre] The system of claim 1,

(Sechen ¶ 150): See Section IX(A) for claim 1.

#### 2. [4] wherein the MLC and SLC nonvolatile memory elements comprise flash memory.

(Sechen ¶ 151): Gavens, which would be understood by a POSITA to describe a NAND flash system with multiple MLC NAND flash modules, expressly describes its MLC non-volatile memory modules as including MLC NAND flash memory elements, which by definition are flash memory. (Fig. 4, 9:49-50: A page of memory cells in the memory array 200 is organized in the NAND configuration; 1:18-19, 4:14-18: Flash memory having a first portion and a second portion storing higher

density compared to the first portion; 2:65-66, 8:65-67: Flash memory devices with NAND string structures; Fig. 1 ref. 90: Flash memory device.)

(Sechen ¶ 152): As explained at paragraphs 93 and 107-110, a POSITA would readily and successfully substitute for Gavens' partitions of MLC memory elements configured for 2-state pseudo-SLC operation an SLC non-volatile memory module which is understood to include SLC NAND flash memory elements. As to Gavens's MLC NAND flash memory operated in pseudo-SLC mode, they are also described as flash memory. (Fig. 4, col. 9:49-50: A page of memory cells in the memory array 200 is organized in the NAND configuration; 1:18-19, 4:14-18: Flash memory having a first portion and a second portion storing higher density compared to the first portion; 2:65-66, 8:65-67: Flash memory devices with NAND string structures; Fig. 1: Flash memory device 90.)

(Sechen ¶ 153): Thus, Gavens, in view of the knowledge of the POSITA, discloses claim 4.

### E. Claim 5 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

#### 1. [5Pre] The system of claim 1,

(Sechen ¶ 154): See Section IX(A) for claim 1.

**2. [5] The system of claim 1, wherein the random access volatile memory element is dynamic random access memory.**

(Sechen ¶ 155): In view of a POSITA's understanding that dynamic random access memory (DRAM) is common type of random access memory (RAVM) that may be used for purposes of temporarily holding data to be compared as is the recited role of RAVM in claim 1, it would be an obvious choice for Gavens's alternative data comparison (16:47-49). The background art supports such use. For example, Moshayedi (Ex. 1043) discloses dynamic random access memory. (Moshayedi, Fig. 1, ref. 106, ¶¶ 3-4, 28, 53-55, 67: DRAM.)

(Sechen ¶ 156): Further, Duann (Ex. 1034) discloses dynamic random access memory. (Duann page 6: Utilize DRAM as cache.) Thus, Gavens, in view of the knowledge of the POSITA, discloses claim 5.

## F. Claim 6 Is Obvious Over Gavens, Including Incorporated references, in View of Knowledge of the POSITA.

**1. [6Pre] The system of claim 1,**

(Sechen ¶ 157): See Section IX(A) for claim 1.

**2. [6] wherein the random access volatile memory element is static random access memory.**

(Sechen ¶ 158): Similar to claim 5, in view of a POSITA's understanding that static random access memory (SRAM) is a common type of random access memory (RAVM) that may be used for purposes of temporarily holding data to be compared

as is the recited role of RAVM in claim 1, it would be an obvious choice for Gavens's alternative data comparison (16:47-49). Gavens itself discloses use of SRAM. (8:40-43: The entire disclosure of Paley '180 [Ex. 1051] is incorporated by reference. Paley '180 ¶¶ 423-425, 502-503, 506: SRAM.) Other uses with NAND flash systems were known, including Duann (Ex. 1034) for a hybrid SLC and MLC system. (Duann page 6: SRAM as cache.) The incorporated Embedded RAM Patents, published March 10, 2011, before the '612 priority date, specifically proposed using the "SRAM of the block" among 1,024 blocks of a commercial NAND flash module (Rao '452 [Ex. 1004] 2:19-39, Figs. 6a and 6b) to enhance speed of reading and writing. Thus, Gavens, in view of the knowledge of the POSITA, discloses claim 6.

### G. Claim 7 Is Obvious Over Gavens, Including Incorporated references, in View of Knowledge of the POSITA and/or Colligan.

#### 1. [7Pre] The system of claim 1,

(Sechen ¶ 159): See Section IX(A) for claim 1.

#### 2. [7] wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD).

(Sechen ¶ 160): A POSITA would understand that it is physically impossible for an SLC flash memory chip (much less an included "element") to include a hard disk drive, where the latter is orders of magnitude larger than a flash chip. If this and all the inconsistencies with claim 1 were ignored, including the antecedent of being a

part of an "SLC" module and changing the nature of an "SLC nonvolatile memory element," a POSITA would know that there are some useful combinations of flash and HDD such as disclosed in U.S. Patent No. 8,225,035 to Colligan (Ex. 1052) 2:33-36, 5:40-6:6, 7:67-8:2, and 8:23-25 (flash memory could supplement HDDs for more frequent writes) and the POSITA could **call** a combination of disk(s) 24 and SLC flash 28 of '612 Fig. 1 an "SLC nonvolatile memory element" to replace bad MLC blocks as physical address destinations. Thus, Gavens, in view of the knowledge of the POSITA, discloses claim 7 with its overstretched construction of "element."

## X. THE PENDING LITIGATIONS IN THE WESTERN DISTRICT OF TEXAS DO NOT WARRANT DENYING INSTITUTION.

With eight Lifetime Patents based on word variations of claims to expand to alternative technologies essentially two features of hybrid SLC-MLC NAND flash memory operation, "data integrity test" and "wear leveling" (the latter dropped in this case of the '612 patent), post grant review – designed to catch recently issued patents on clear defects – is the more appropriate place for review (for each patent in detail) compared to the District Court where those word variations can escape scrutiny. That is because of the limitation of District Court litigation to claims asserted against accused instrumentalities and because of the limited competence and resources of, and issues for, the District Court and the requested jury. The Board may take notice that even construction of the multiple terms of the eight Lifetime

Patents are restricted in number in District Court (per party, and even "sides" in related cases as present here), even counting contentions of indefiniteness. Yet, as demonstrated in the above-stated grounds (Sections VII, VIII, and IX), the case against the '612 patent – which does not even recite the preferential writing to an SLC NAND flash module as known but restated in the specification – is compelling. Balancing of the six factors set forth by the Board in *Apple Inc. v. Fintiv, Inc*., IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential) does not warrant denying institution here. Rather, institution would best serve the interest in "system efficiency, fairness, and patent quality" (*id.* at 5), allowing due resolution of the substantial patentability questions (*id.* at 15).

As to *Fintiv* Factor 5, the petitioner and defendant in the parallel proceeding are the same party. Phison has acted to file this petition expeditiously within the nine months allowed from issuance, where it received first notice of Vervain's assertion in the Complaint filed March 8, 2024, and the First Amended Complaint filed May 13, 2024 (Ex. 1062). The District Court has not issued any substantive opinions regarding the scope or validity of the Challenged Claims. The parallel proceeding is in an early stage: the Court has not yet decided Phison's motion to dismiss (*see* Docket List [Ex. 1060] entries 12 and 24), the Petitioners have not otherwise answered, fact discovery has not yet proceeded beyond automatic disclosure and Phison's invalidity and subject-matter eligibility contentions were

filed on August 16, 2024, and claim construction materials exchanged in accordance with the Scheduling Order (Ex. 1063). A *Markman* hearing is initially scheduled for December 5, 2024. (*Id.*) Thus, as to Factor 3, there has not been overriding investment in the parallel proceeding; to the contrary, the requirements of the parallel proceeding will limit Markman construction to twelve terms between the parties for eight patents of verbal variations of the same specification. Thus, as to Factor 4, there is overlap, in the greater inclusiveness of the requested review as the District Court will not consider all the issues properly raised in this Petition, the pending PGR2024-00047 of the '546 patent, and others for review of the six other variant patents that Petitioner may petition.

Factors 1 (stay) and 2 (proximity of trial dates) do not significantly weigh for or against instituting the requested PGR. Petitioner does not know if the District Court will stay the case if trial by this Board is instituted and the Court has *tentatively* set jury selection for December 15, 2025 (Scheduling Order [Ex. 1063] at 4).

Regarding the sixth factor (merits, other circumstances), the merits strongly weigh in favor of instituting trial as shown through the strength of the grounds in this Petition. "Other circumstances" favor institution. As described at note 4 *supra*, there are separate suits by Patent Owner Vervain (following the same template) against Phison and a customer (Kingston Docket List [Ex. 1061]). This presents the complexity of eight patents with method and apparatus claims that Vervain asserts

against multiple, sometimes competing products (that thus must be held confidential between the defendants) that implicate third-party actors who may be implicated in divided or indirect infringement as users who select the configuration or performance of the claimed system. Moreover, unlike Phison, its customer defendant in the other case has moved to dismiss for improper venue and to transfer (Kingston Docket List [Ex. 1061] entries 13 and 20) with attendant discovery and confidentiality proceedings (*id*. entries 15 and 16).

The interest of the public in cleaning away such verbal variants of questionable innovation in the Lifetime Patents are best served by the requested review. As with Factor 4, the Board may take notice that such litigation, if it reaches trial, will have been drastically reduced in claims and theories asserted – this begins with the limitation of terms for construction for eight patents. A PGR trial, in contrast, allows a focus on resolving all Challenged Claims in a single patent, and may substantially simplify district court trial without the extensive district court discovery for which the America Invents Act offered this alternative before the Board. And, of course, Petitioner has shown its case to be compelling.

## XI. CONCLUSION

Petitioner submits that for the reasons set forth above, supported by the declaration of Dr. Sechen and the Exhibits, it has been shown that more likely than

not, Challenged Claims 1-7 are invalid under all of 35 U.S.C. §§ 101, 112(a), 112(b), and 103 and should reviewed by the Board and canceled.

Date: September 25, 2024

Respectfully submitted,
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**CERTIFICATION OF SERVICE (37 C.F.R. § 42.6(e))**

The undersigned hereby certifies that the above-captioned Petition for Post Grant Review of U.S. Patent No. 11,854,612 (and accompanying exhibits), was served in its entirety on September 25, 2024, upon Patent Owner's correspondent of record via overnight courier:

*Patent owner's correspondent*
*address of record for U.S. Patent No. 11,854,612*

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## CERTIFICATION OF WORD COUNT (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the attached Petition, including footnotes, but not the cover page, exhibit list, table of contents, mandatory notices, and certifications, contains 18,008 words, as measured by the Word Count function of Microsoft Word. This is less than the limit of 18,700 words as specified by 37 C.F.R. § 42.24(a)(ii).

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