UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PHISON ELECTRONICS CORPORATION,

Petitioner

v.

VERVAIN, LLC,

Patent Owner

Post-Grant Review Case No. PGR2024-00047

Patent 11,830,546

PETITION FOR POST-GRANT REVIEW OF U.S. PATENT NO. 11,830,546

TABLE OF CONTENTS

I. INTRODUCTION: 1

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1): 4

A. REAL PARTY-IN-INTEREST UNDER 37 C.F.R. § 42.8(B)(1): 4

B. RELATED MATTERS UNDER 37 C.F.R. § 42.8(B)(2): 5

C. LEAD AND BACK UP COUNSEL UNDER 37 C.F.R. § 42.8(B)(3): 5

D. SERVICE INFORMATION UNDER 37 C.F.R. § 42.8(B)(4): 5

III. ADDITIONAL REQUIREMENTS: 6

A. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15: 6

B. TIMING UNDER 37 C.F.R. § 42.202: 7

C. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.204(A): 7

IV. NAND FLASH TECHNOLOGY BACKGROUND 7

A. CHARACTERISTIC NATURE OF NAND FLASH MEMORY 7

B. CHARACTERISTIC NAND FLASH MEMORY MANAGEMENT 9

C. INTRODUCTION OF MLC AND SLC FLASH 9

D. KNOWN COORDINATED USE OF SLC AND MLC NAND FLASH MODULES: 10

V. THE '546 PATENT: 12

A. THE SPECIFICATION: 12

B. ABSTRACTION OF THE CLAIMS SINCE 2018: 17

C. THE CHALLENGED CLAIMS OF THE '546 PATENT: 18

D. PERSON OF ORDINARY SKILL IN THE ART 22

VI. 37 C.F.R. § 42.204(B)(3): CLAIM CONSTRUCTION 23

VII. GROUND 1: THE CHALLENGED CLAIMS CLAIM PATENT-INELIGIBLE SUBJECT MATTER UNDER 35 U.S.C. § 101 AS DIRECTED TO AN ABSTRACT IDEA, NAMELY, "MEMORY SPACE," WITHOUT CLAIMING SUBSTANTIALLY MORE THAN ASPECTS OF THE OPERATION OF A GENERAL-PURPOSE COMPUTER. 28

VIII. GROUND 2: THE CHALLENGED CLAIMS LACK A WRITTEN DESCRIPTION DESCRIBING THE CLAIMED SUBJECT MATTER IN ACCORDANCE WITH 35 U.S.C. § 112(A). 30

A. THE CHALLENGED CLAIMS LIMITED BY "MEMORY SPACE" ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A). 31

B. THE CHALLENGED CLAIMS LIMITED BY "MEMORY ELEMENT" ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A). 32

C. THE CHALLENGED CLAIMS LIMITED BY "MAPPING . . . AS NECESSITATED BY THE SYSTEM TO MAXIMIZE LIFETIME" ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A). 33

D. THE CHALLENGED CLAIMS LIMITED BY "TRANSFER OF DATA . . . FROM THOSE PHYSICAL ADDRESSES DETERMINED TO HAVE FAILED THE DATA INTEGRITY TEST" ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A) AND FAIL TO RECITE A USEFUL SYSTEM FOR STORING DATA. 35

E. THE CHALLENGED CLAIMS LIMITED BY "AT LEAST ONE MEMORY ELEMENT" ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A) AND FAIL TO RECITE A USEFUL SYSTEM FOR STORING DATA. 35

IX. GROUND 3: THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(B). 37

A. THE CHALLENGED CLAIMS LIMITED BY "MEMORY SPACE" ARE INDEFINITE UNDER 35 U.S.C. § 112(B). 38

B. THE CHALLENGED CLAIMS LIMITED BY "MEMORY ELEMENT" ARE INDEFINITE UNDER 35 U.S.C. § 112(B). 38

C. THE CHALLENGED CLAIMS LIMITED BY "MAPPING . . . AS NECESSITATED BY THE SYSTEM TO MAXIMIZE LIFETIME" ARE INDEFINITE UNDER 35 U.S.C. § 112(B)…. 39

D. THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(B) FOR THEIR RECITATION OF AN ABSTRACT "CONTROLLER" LIMITED BY FUNCTIONS IN THE CLAIMS THAT ARE UNSUPPORTED BY STRUCTURE (PHYSICAL OR ALGORITHMIC) IN THE SPECIFICATION. 40

E. THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(B) BECAUSE THEY RECITE METHOD STEPS IN THE CONTEXT OF A CLAIM TO A SYSTEM. 43

F. THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(B) BECAUSE IT IS UNCERTAIN WHETHER AND WHEN THE RECITED COMPARISON TEST IS REQUIRED TO BE PERFORMED. 44

X. GROUND 4: CLAIMS 1-7 OBVIOUS UNDER 35 U.S.C. § 103 OVER GAVENS IN VIEW OF POSITA KNOWLEDGE. 45

A. CLAIM 1 IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA. 46

1. [1Pre] A system for storing data comprising: 46

2. [1a] [1a1] memory space containing volatile memory space and [1a2] nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space; 47

3. [1b] at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements; 49

4. [1c] a bank of nonvolatile memory, including: [1c1] a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and [1c2]at least one SLC memory module including at least one SLC nonvolatile memory element;..... 49

5. [1d] at least one random access volatile memory element; 53

6. [1e] a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements; 54

7. [1f] the controller [1f1] having associated controller memory for storing received data therein, the controller [1f2] controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the receved data therein as stored data, the controller, [1f3] in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, [1f4] operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data; 57

8. [1g] the controller [1g1] performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by [1g2] readig the stored data to the controller memory and [1g3] comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation; 61

9. [1h] wherein [1h1] the address table maps logical and physical addresses adaptable to the system, wherein [1h2] the mapping is performed as necessitated by the system to maximize lifetime, and wherein [1h3] the

mapping maps blocks, pages, or bytes of dat in either volatile or nonvolatile, or both, memories; and..... 64

10. [1i] wherein a failure of the data integrity test performed on the stored data by the controller results in [1i1] a remapping of address space to a different physical range of addresses and [1i2] transfer of data corresponding to the retained data to thoe remapped physical addresses from those physical addresses determined to have failed the data integrity test..... 67

B. CLAIM 2 IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA..... 70

1. [2Pre] The system of claim 1, ... 70

2. [2] wherein the FTL is a software module, or a firmware module containing software updates..... 70

C. CLAIM 3 IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA..... 71

1. [3Pre] The system of claim 1, ... 71

2. [3] wherein at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller... 71

D. CLAIM 4 IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA..... 72

1. [4Pre] The system of claim 1, ... 72

2. [4] wherein the MLC and SLC nonvolatile memory elements comprise flash memory… 72

E. CLAIM 5 IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA. 73

1. [5Pre] The system of claim 1, ... 73

2. [5] The system of claim 1, wherein the random access volatile memory element is dynamic random access memory. 73

F. CLAIM 6 IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA. 74

1. [6Pre] The system of claim 1, ... 74

2. [6] wherein the random access volatile memory element is static random access memory. 74

G. CLAIM 7 IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA AND/OR COLLIGAN…. 75

1. [7Pre] The system of claim 1, ... 75

2. [7] wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD). 75

XI. THE PENDING LITIGATIONS IN THE WESTERN DISTRICT OF TEXAS DO NOT WARRANT DENYING INSTITUTION. 76

XII. CONCLUSION 79

TABLE OF AUTHORITIES

CASES

Alice Corp. Pty. Ltd. v. CLS Bank International,

573 U.S. 208 (2014) ---------- 28, 29

Amgen Inc. v. Sanofi,

598 U.S. 594 (2023) ----------31

Apple Inc. v. Fintiv, Inc.,

IPR2020-00019 (P.T.A.B. Mar. 20, 2020) ----------77

Bilski v. Kappos,

561 U.S. 593 (2010) ----------28

In re Nuijten,

500 F.3d 1346 (Fed. Cir. 1319)) ----------30

IPXL Holdings, LLC v. Amazon.com, Inc.,

430 F.3d 1377 (Fed. Cir. 2005) ---------- 43, 44

KSR Int'l Co. v. Teleflex Inc.,

550 U.S. 398 (2007) ----------45

Mayo Collaborative Services v. Prometheus Laboratories, Inc.,

566 U.S. 66 (2012)----------29

Nautilus, Inc. v. Biosig Instruments,

572 U.S. 898 (2014) ----------37

Phillips v. AWH Corp.,

415 F.3d 1303 (Fed. Cir. 2005) ----------23

Rain Computing, Inc. v. Samsung Electronics America, Inc.,

989 F.3d 1002 (Fed. Cir. 2021) ----------41

Vervain, LLC v. Kingston Technology Company, Inc. et al.,

No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024)---------- 2, 78, 79

Vervain, LLC v. Micron Technology, Inc. et al.,

No. 6:21-cv-00487 (W.D. Tex. filed May 10, 2021)---------- 2

Vervain, LLC v. Phison Electronics Corp.,

No. 1:24-cv-00259 (W.D. Tex. filed March 8, 2024)---------- 2, 5, 77, 78

Vervain, LLC v. Western Digital Corp. et al.,

No. 6:21-cv-00488 (W.D. Tex. filed May 10, 2021)---------- 2

STATUTES

35 U.S.C. § 101 ---------- passim

35 U.S.C. § 103 ---------- 45, 80

35 U.S.C. § 112(a)---------- passim

35 U.S.C. § 112(b) ---------- passim

OTHER AUTHORITIES

37 C.F.R. § 42.6(e) ---------- 81, 82

37 C.F.R. § 42.8(a)(1)---------- 4

37 C.F.R. § 42.8(b)(1) ---------- 4

37 C.F.R. § 42.8 (b)(2)---------- 5

37 C.F.R. § 42.8(b)(3) ---------- 5

37 C.F.R. § 42.8(b)(4) ---------- 5

37 C.F.R. § 42.15 ---------- 6

37 C.F.R. § 42.200(b) ----------23

37 C.F.R. § 42.202 ---------- 7

37 C.F.R. § 42.204(a) ---------- 7

37 C.F.R. § 42.204(b)(3) ----------23

37 C.F.R. § 42.24(a)(ii) ----------82

Manual of Patent Examining Procedure ("MPEP") § 2173.05(p)(II) ---------- 43, 44

LIST OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,830,546, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao
1002	Declaration of Carl Sechen, Ph.D.
1003	U.S. Provisional Application No. 61/509,257, titled "IMPROVED LIFETIME MIXED LEVEL NAND FLASH SYSTEM" by Rao
1004	U.S. Patent No. 8,194,452, titled "NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES," to Rao
1005	U.S. Patent No. 8,891,298, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao
1006	*Intentionally omitted*
1007	U.S. Patent No. 9,196,385, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao
1008	*Intentionally omitted*
1009	U.S. Patent No. 9,997,240, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao
1010	*Intentionally omitted*
1011	U.S. Patent No. 10,950,300, titled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," to Rao
1012	Excerpts from prosecution history of '300 patent
1013	*Intentionally omitted*
1014	Excerpts from prosecution history of '546 patent

1015-24	*Intentionally omitted*
1025	Excerpts from Rino Micheloni, et al., INSIDE NAND FLASH MEMORIES (Springer 2010)
1026	Excerpts from NONVOLATILE MEMORY TECHNOLOGIES WITH EMPHASIS ON FLASH: A COMPREHENSIVE GUIDE TO UNDERSTANDING AND USING NVM DEVICES (Joe E. Brewer & Manzur Gill eds. Wiley-IEEE Press 2008)
1027	Excerpts from MICROSOFT COMPUTER DICTIONARY (5th ed. 2002)
1028-29	*Intentionally omitted*
1030	Yu Cai et al., *Program Interference in MLC NAND Flash Memory: Characterization, Modeling and Mitigation* (IEEE 2013)
1031	Kang-Deog Suh et al., *A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme*, 30 IEEE J. Solid State Circuits 1149 (Nov. 1995)
1032	Eitan Yaakobi et al., *Error Characterization and Coding Schemes for Flash Memories* (2010 IEEE Globecom Workshops, Miami, FL at 1856-60)
1033	Evans, Chris, "Enterprise MLC: How flash vendors are boosting MLC write endurance" (June 3, 2011)
1034	Nelson Duann, SLC & MLC Hybrid (Silicon Motion Flash Memory Summit, Santa Clara, CA, Aug. 12, 2008)
1035	Ashish Jagmohan et. al., *Adaptive Endurance Coding for NAND Flash* (2010 IEEE Globecom Workshops, Miami, FL at 1841-45)
1036	Sungjin Lee et al., *FlexFS: A Flexible Flash File System for MLC NAND Flash Memory* (2009 USENIX Annual Technical Conference, San Diego, CA, June 14-19, 2009)

1037	Minyoung Sung & Kanghee Kim, *Asymmetric Flash Volume Management*, 58 *IEEE Transactions on Consumer Electronics* 455 (May 2012)
1038-39	*Intentionally omitted*
1040	U.S. Patent No. 6,456,528, titled for "SELECTIVE OPERATION OF A MULTI-STATE NON-VOLATILE MEMORY SYSTEM IN A BINARY MODE" to Chen
1041	U.S. Patent No. 8,078,794, titled "HYBRID SSD USING A COMBINATION OF SLC AND MLC FLASH MEMORY ARRAYS," to Lee et al.
1042	U.S. Patent Appl. Pub. No. 2008/0140918, titled "HYBRID NON-VOLATILE SOLD STATE MEMORY SYSTEM" by Sutardja
1043	U.S. Patent Appl. Pub. No. 2009/0327591, titled "SLC-MLC COMINATION FLASH STORAGE," by Moshayedi
1044	U.S. Patent Appl. Pub. No. 2010/0172179, titled "SPARE BLOCK MANAGEMENT OF NON-VOLATILE MEMORIES," by Gorobets et al.
1045	U.S. Patent No. 8,634,240, titled "NON-VOLATILE MEMORY AND METHOD WITH ACCELERATED POST-WRITE READ TO MANAGE ERRORS," to Gavens et al.
1046	U.S. Patent No. 8,806,301, titled "DATA WRITING METHOD FOR A FLASH MEMORY, AND CONTROLLER AND STORAGE SYSTEM USING THE SAME," to Yu et al.
1047	U.S. Patent Appl. Pub. No. 2010/0115192, titled "WEAR LEVELING METHOD FOR NON-VOLATILE MEMORY DEVICE HAVNG SINGLE AND MULTI LEVEL MEMORY CELL BLOCKS," by Lee

1048	U.S. Patent Appl. Pub. No. 2011/0271043, titled "SYSTEM AND METHOD FOR ALLOCATING AND USING SPARE BLOCKS IN A FLASH MEMORY," to Segal et al.
1049	U.S. Patent Appl. Pub. No. 2011/0153912, titled "MAINTAINING UPDATES OF MULTI-LEVEL NON-VOLATILE MEMORY IN BINARY NON-VOLATILE MEMORY," by Gorobets et al.
1050	U.S. Patent No. 5,930,167, titled "MULTI-STATE NON-VOLATILE FLASH MEMORY CAPABLE OF BEING ITS OWN TWO STATE WRITE CACHE," to Lee et al.
1051	U.S. Patent Appl. Pub. No. 2010/0172180, titled "NON-VOLATILE MEMORY AND METHOD WITH WRITE CACHE PARTITIONING," by Paley et al.
1052	U.S. Patent No. 8,225,035, titled "SYSTEMS AND METHODS FOR OPERATING A DISK DRIVE," to Colligan
1053-59	*Intentionally omitted*
1060	Docket list for *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex., filed March 8, 2024)
1061	Docket list for *Vervain, LLC v. Kingston Technology Company, Inc.*, No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024)
1062	First Amended Complaint, Doc. No. 9 in *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex.)
1063	Signed Agreed Scheduling Order, Doc. No. 16 in *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex.)

I. INTRODUCTION:

Phison Electronics Corporation ("Phison" or "Petitioner") requests post-grant review ("PGR") of claims 1-7 (the "Challenged Claims") of U.S. Patent No. 11,830,546, entitled "LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM," issued Nov. 28, 2023 ("the '546 patent") (Ex. 1001), assigned to Vervain, LLC ("Vervain" or "Patent Owner"). The '546 patent was issued on the fourth continuation application[1] of a chain of continuations from U.S. Pat. Appl. No. 13/455,267, filed on April 25, 2012,[2] which claimed priority of U.S. Provisional App. No. 61/509,257, filed on July 19, 2011 ("Provisional," Ex. 1003) and incorporated by reference the common disclosure of U.S. Patent No. 7,855,916 and

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[1] U.S. Appl. No. 17/203,385, filed March 16, 2021.

[2] This application issued as U.S. Patent No. 8,891,298 (the "'298 patent," Ex. 1005). It was followed by continuation U.S. Appl. No. 14/525,411, filed Oct. 28, 2014, and issued as U.S. Patent No. 9,196,385 (the "'385 patent," Ex. 1007), by continuation U.S. Appl. No. 14/950,553, filed Nov. 24, 2015, and issued as U.S. Patent No. 9,997,240 (the "'240 patent," Ex. 1009), and by continuation U.S. Appl. No. 16/006,299, filed June 12, 2018, and issued as U.S. Patent No. 10,950,300 (the "'300 patent," Ex. 1011).

U.S. Pat. Appl. No. 12/915,177, for "NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES," the latter published March 10, 2011, and issued as U.S. Patent No. 8,194,452 ("Rao '452," Ex. 1004).[3]

Three later continuation applications issued as U.S. Patents Nos. 11,854,612, 11,967,369 and 11,967,370. All eight of these "Lifetime Patents," based on the same April 25, 2012, specification claiming July 19, 2011, priority, are currently asserted (First Amended Complaint, Ex. 1062) by Vervain against Phison in *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex. filed March 8, 2024).[4]

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[3] The second of these "Embedded RAM Patents" is provided for its slightly more readable exhibits.

[4] All are asserted against a customer of Phison in *Vervain, LLC v. Kingston Technology Company, Inc.*, *Kingston Digital, Inc., and Kingston Technology Corp.*, No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024). The first four patents were asserted previously in *Vervain, LLC v. Micron Technology, Inc.; Micron Semiconductor Products, Inc.; and Micron Technology Texas, LLC,* No. 6:21-cv-00487 (W.D. Tex. filed May 10, 2021, settled April 21, 2023) and *Vervain, LLC v. Western Digital Corp.; Western Digital Technologies, Inc.; and HGST, Inc.,* No. 6:21-cv-00488 (W.D. Tex. filed May 10, 2021, settled Aug. 8, 2023). Micron

This Petition demonstrates by a preponderance of the evidence that the Challenged Claims are unpatentable as one of eight patent groups that, in verbal variations, purport to extend to fundamentally different technology a couple of well-known operations of POSITA-understood Single-Level Cell ("SLC") and Multi-Level Cell ("MLC") NAND flash hardware modules. Those two operations apply preferential NAND-flash "mapping" to the SLC module under circumstances that might benefit from the SLC module's operation which is less taxing on its expected service life than the MLC module's multi-level (greater data density) operation is on its expected service life. The claimed "system[s] for storing data" comprise the two NAND flash modules and an abstract "controller" recited as performing functions or steps that variously paraphrase the same four paragraphs (or fewer as for the '546 patent) of the common DETAILED DESCRIPTION. Two paragraphs describe (incorrectly) the Fig. 3A and 3B "integrity test" method steps for NAND flash operation. One outlines the operation of the characteristic NAND flash "Flash

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petitioned this Board for *inter partes* review in Micron Technology, Inc. v. Vervain, LLC, IPR2021-001547 ('298 patent), IPR2021-001548 ('385 patent), IPR2021-001549 ('240 patent), and IPR2021-001550 ('300 patent), which were instituted on April 8 and 11, 2022, and terminated on April 4, 2023, on settlement after hearing but prior to final written decision.

Translation Layer" shown as a functional block in Fig. 4 in a memory device module with multiple SLC and MLC NAND flash modules. The fourth describes (incorrectly) NAND flash "wear leveling," which does not appear explicitly in the claims of the '546 patent.

Patent Owner Vervain should not be allowed to maintain its eight attempts to claim well-known NAND flash technology for technologies it touts in the BACKGROUND as operating on essentially different principles from NAND. Vervain should not be allowed to substitute abstract "memory space" (mentioned in the specification only as a quantity of storage space) and vague "memory elements" (not mentioned at all) for the POSITA-understood, hard-wired NAND "pages" for writing and "blocks" for flash erasing. The '546 patent claims do not even recite wear leveling or preferential redirection to SLC – only what one might imagine to "maximize lifetime." The Post-Grant Review is eminently appropriate for stopping proliferation of bad patents such as the '546 patent's unsupported abstraction of its own misstatement of well-known NAND flash technology.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1):

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1):

Petitioner Phison Electronics Corporation is the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8 (b)(2):

As set forth further at note 4 supra, the '546 patent (along with seven other patents based on the same specification) is currently asserted by Vervain against Phison and its customer (separately) in the Western District of Texas. In the Phison case a claim construction hearing is tentatively scheduled for December 5, 2024, and jury selection tentatively scheduled for December 15, 2025 (*Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259, Doc. No. 16 (W.D. Tex. July 15, 2024) (Ex. 1063). Resolution of this proceeding may simplify that litigation and promote settlement.

C. Lead and Back Up Counsel Under 37 C.F.R. § 42.8(b)(3):

Pursuant to 37 C.F.R. § 42.8(b)(3), lead counsel for this Petition is Hsuanyeh Chang, PhD (Reg. No. 73,431) and back-up counsel are Stephen Y. Chow (Reg. No. 31,338), Douglas E. Chin (Reg. No. 66,713), and Peter Yi (Reg. No. 61,790). Pursuant to 37 C.F.R. § 42.10(b), Petitioner has filed a power of attorney designating the above-identified counsel.

D. Service Information Under 37 C.F.R. § 42.8(b)(4):

Pursuant to 37 C.F.R. § 42.8(b)(4) service information for the Petition is as follows:

Lead Counsel	Back-Up Counsel
Hsuanyeh Chang, PhD Reg. No. 73,431	Stephen Y. Chow Reg. No. 31,338

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Petitioner consents to electronic service at the above-identified email addresses.

III. ADDITIONAL REQUIREMENTS:

A. Payment of Fees Under 37 C.F.R. § 42.15:

The required fees are submitted herewith from Deposit Account No. 50-6685 (Order No. 1280-0009). If any additional fees are due at any time during this proceeding, the Office is authorized to charge such fees to Deposit Account No. Deposit Account No. 50-6685 (Order No. 1280-0009).

B. Timing Under 37 C.F.R. § 42.202:

The present petition for post-grant review is filed within nine months after the grant of the '546 patent.

C. Grounds for Standing Under 37 C.F.R. § 42.204(a):

Petitioner certifies that: (1) the '546 patent is eligible for post-grant review; and (2) Petitioner is not barred or estopped from requesting post-grant review of any claims of the '546 patent on the grounds identified herein.

IV. NAND FLASH TECHNOLOGY BACKGROUND

Petitioner's expert, Dr. Carl Sechen, has provided in his declaration ("Sechen," Ex. 1002) a deep analysis of the state of NAND flash technology relied on by the Lifetime Patents (Sechen Section V), the embodiments advanced in the common specification (Sechen Section VII), the evolution of the Lifetime Patent claims from NAND flash technology to abstractions for alternative technologies (Sechen Section VIII), specific defects in the '546 claims (Sechen Section IX), and invalidity of those claims over the prior art in view of the POSITA's knowledge of the art. Summarized here are the salient points regarding the technology background applicable to the '546 patent version of the "system for storing data."

A. Characteristic Nature of NAND Flash Memory

A **NAND flash cell** is type of transistor with a floating gate that stores information by charges associated with "threshold voltages," with a charged state

corresponding to a higher threshold voltage typically associated with a logical "0," while minimal charge associated with a logical "1." (Sechen ¶ 26.) These cells are hard wired in NAND flash to write to a NAND "**page**" of typically 2K cells or bits of logical information. (*Id.*) A defining, characteristic of NAND flash is that it is hard wired such that "**blocks**" **of** 64 **pages** are **erased in unison** in required preparation for writing to pages in that block that are not empty or previously erased (*Id.* ¶¶ 26-27). Thus, unlike magnetic hard disk drives (and the Lifetime Patents' proposed alternative technologies) which allow "write in place" of data assigned to a particular physical location, updates to data (considered "logical") in NAND flash must be written to a new physical location that is empty or must be erased in preparation ("erase before write"). (*Id.*) Thus, to maintain logical visibility to the user (host computer) of a NAND flash memory device such as a Solid State Drive ("SSD") (shown at Sechen ¶ 27), there are maintained and updated tables in or available to a **NAND flash device controller**, shown as a hardware module or chip on an SSD circuit board (*id.*) to "map" logical locations visible to the user to physical locations in the NAND flash memory array ("L2P mapping"), which update for each data write (*id.*). The physical nature of NAND flash pages and blocks determine the Physical Block Addresses ("PBA") mapped from the construct of Logical Block Addresses ("LBA"). (*Id.*) This mapping and remapping is typically done with the software construct of a **Flash Translation Layer** ("**FTL**"). (*Id.*) The physical

reading, writing and erasing of NAND flash cells, characteristically organized in pages and blocks, is performed by circuity in a NAND flash memory module shown in multiples in Sechen paragraph 27 as "flash" or "flash memory" on a board, along with a block diagram showing the internal reading, writing and erasing functions. A POSITA would understand this to be a **NAND flash memory or module**. (*Id*.)

B. Characteristic NAND Flash Memory Management

As reviewed at Sechen paragraphs 27-29, there were known processes of "wear leveling" for NAND flash memory, including garbage collection and bad block management peculiar to NAND flash, where "hot" data, that is frequently updated (logical) data and "cold" (or not-"hot") data are clustered in physical NAND flash blocks to facilitate efficient (fewer re-writes) application of NAND-characteristic garbage collection, all of which is calculated to even stresses caused by write-erase cycles that challenge the rated, expected "endurance" of NAND flash blocks (subject to the most stressful erase), failure (and relegation to "bad blocks") enough of which may compromise the usefulness of the memory system. (*See* Sechen notes 8 and 9 on lifetime.)

C. Introduction of MLC and SLC Flash

Multi-level cell (MLC) NAND flash, developed in 1992-97, is distinguished from the pre-existing, re-designated **Single-level cell (SLC) NAND flash** that is two-state (each cell holding a binary bit of information). In contrast, MLC involves

the compression of multiples of two threshold voltages into the charge window available for a physical cell. Generally, MLC refers to two-levels or four threshold voltages (charges) written in two passes as "lower" (less significant bit, "LSB") and "upper" (most significant bit, "MSB") pages incrementing charge to the desired threshold value representing two bits (11, 10, 00, 01). (Sechen ¶¶ 30-32.) As reviewed at Sechen paragraphs 31-37, the charging for MLC is more complex than for SLC because of the narrower window for distinct threshold charges, multiple passes of writing, and incremental pulsing in each pass to avoid uncorrectable overshoot. Thus, a POSITA would understand that different circuitry is required for an **MLC NAND flash module** than for an **SLC NAND flash module**.

D. Known Coordinated Use of SLC and MLC NAND Flash Modules:

At least because of the compression and multiple pulsing and passes of writing, it was well known that MLC NAND flash, while having more capacity (and thus lower cost of information per NAND cell) would wear more quickly (have less "endurance") than SLC NAND flash. (Sechen ¶¶ 38-39.) Thus, it was proposed as early as 2008 to use hybrid systems of SLC modules and MLC modules in which more **frequently written**/updated (to logical locations) **data**, such as system data and user directories) would be written **preferentially to** a more robust **SLC module** while less frequently updated data such as user data would be written to the MLC module. (Sechen ¶ 40; Nelson Duann, SLC & MLC Hybrid (Silicon Motion Flash

Memory Summit, Santa Clara, CA, Aug. 12, 2008) ["Duann," Ex. 1034]; U.S. Patent No. 8,078,794 to Lee et al., published Sept. 4, 2008 ["Lee '794," Ex. 1041].)

The **SLC module** preference was applied in 2008-09 to **wear leveling** in 2008-09. (Sechen ¶ 41; Sutardja, U.S. Patent Appl. Pub. No. 2008/0140918 "Hybrid Non-Volatile Sold State Memory System" ["Sutardja," Ex. 1042]; Moshayedi U.S. Patent Appl. No. 2009/00327591 ["Moshayedi," Ex. 1043].)

Two-state operation of MLC (later called **pseudo-SLC)** was disclosed as early as 2002. (Sechen ¶ 43; U.S. Patent No. 6,456,528 to Chen for "Selective Operation of a Multi-State Non-Volatile Memory System in a Binary Mode" ["Chen '528," Ex. 1040]). Such use of MLC, because it uses the MLC module physical characteristic, circuitry and pulsed/phased writing, has inferior performance and endurance compared to "real" SLC. A SanDisk suite of patents (incorporating by reference among others, Chen '528) disclosed the use of pSLC or lower-density mode use of MLC modules through partitioning and configuration for multiple uses, including responses to data integrity "fails" – to avoid unnecessary processing/latency, preferably later in the lifetime of the system when reliability statistically becomes an issue, and then using appropriate (to desired performance) error correction code ("ECC") schemes that allow the use of data with errors corrected upon reading, saving wear and latency. (Sechen ¶¶ 48-50, particularly note 8; U.S. Patent No. 8,634,240 to Gavens et al., published April 28, 2011

["Gavens," Ex. 1045]; *also* U.S. Patent No. 8,806,301 to Yu, published April 14, 2011 [Ex. 1046].) Nothing disclosed in the '546 patent specification was new relative to the 2011 state of the art of NAND flash technology; to the contrary, the disclosed embodiments would not be enabled without the understood (by a POSITA) physical operation of the referenced SLC and MLC modules as SLC NAND flash modules and MLC NAND flash modules with supporting circuitry at least for their distinct organizations, reading, writing and erasing.

V. THE '546 PATENT:

A. The Specification:

The core system of MLC NAND flash and SLC NAND flash modules are repeated multiple times in the specification:

> two separate banks of NAND flash are maintained by a controller. One bank contains economical MLC NAND flash, while a second bank contains high endurance SLC NAND flash. The controller conducts a data integrity test after every write. If a particular address range fails a data integrity test, the address range is remapped from MLC NAND flash to SLC NAND flash.

(5:1-7 [emphasis added].) It is repeated in Fig. 4, described as

> two NAND flash memory banks **56** and **58**, whereby memory bank **56** comprises a plurality of MLC NAND flash memory modules **60***a* and a plurality of SLC NAND flash memory modules **62***a*. Memory bank **58** comprises a plurality of MLC NAND

> flash memory modules **60***b* and a plurality of SLC NAND flash memory modules **62***b*.

(6:61-67 [emphasis added].) Fig. 4 shows a physical memory device module including two banks each including 8+ **MLC flash memory modules** and 2+ **SLC NAND flash memory modules**). The SUMMARY states:

> there is provided a system for storing data which comprises at least one MLC nonvolatile memory module (hereinafter referred to as "MLC module") and at least one SLC non-volatile memory module (hereinafter referred to as "SLC module"), each module comprises a plurality of individually erasable blocks. The data storage system according to one embodiment of the present disclosure further comprises a controller for controlling both the at least one MLC module and the at least one SLC module. In particular, the controller maintains an address map comprising a list of individual logical address ranges each of which maps to a similar range of physical addresses within either the at least one MLC module or the at least one SLC module. After each write to (flash) memory, the controller conducts a data integrity check to ensure that the data was written correctly. When the data was not written correctly, the controller modifies the table so that the range of addresses on which the write failed is remapped to the next available range of physical addresses within the at least one SLC module.

(4:8-26 [emphasis added].) The "plurality of individually erasable blocks" is characteristic of NAND flash erase required for writing in NAND flash modules

typically with a thousand blocks, with supporting circuitry as shown in the Embedded RAM Patents incorporated into the specification (Rao '452 [Ex. 1004] Figs. 6a and 6b). The specification suggests PCM, RRAM and MAGRAM as technologies that could be substituted for the much-recited "SLC module" – but only explains their operation as "write in place" (2:1-8) in fundamental contrast to NAND flash. There is nothing to enable substitution for the NAND module recited through the specification and shown in the incorporated Embedded RAM Patents.

In contrast to the physical specification of the SLC and MLC modules, the other component of the core system, the "controller," is provided no structure, not even characterized as a hardware or software module (compared to the FTL "component" characterized in claim 2 as a software or firmware module). Instead, "controller" is only limited in the claims by its recited functions or actions, which in turn are explained only by (a) a two-paragraph explanation of the NAND flash memory method steps of Figs. 3A and 3B (6:5-34) and "additional" embodiments of (b) a paragraph restating NAND flash FTL shown in Fig. 4 separate from the controller (6:57-67) and (c) the fourth, two-sentence paragraph that confuses NAND flash "wear leveling" (6:44-56).

Dr. Sechen critiques in detail at paragraphs 60, 63 and 64 both the BACKGROUND and DETAILED DESCRIPTION descriptions of the NAND flash

method steps of Fig. 3A and 3B. The text of the latter is presented here with highlighting of points for consideration on this petition:

> FIGS. **3**A and **3**B are a flow chart illustrating a method for utilizing a NAND flash memory system incorporating one embodiment of the present disclosure. The method begins in a step **100**, when a command to write a quantum of data stored in DRAM to a particular location in NAND flash memory is received. In step **102**, the quantum of data is read from **[A1]** DRAM into memory within the device controller (which acts as the memory controller). **[B1]** In step **104**, both the logical address range and the NAND flash physical address range to which the quantum of data is to be written, is read into memory of the device controller. **[B2]** In step **106**, the quantum of data to be written is combined with the contents of the NAND flash memory. **[B3]** In step **108**, the NAND flash physical address range to be written is erased. In step **110**, the combined data is written to the appropriate NAND flash physical address range. **[A3]**, **[B4]** In step **112** the NAND flash physical address range that was written in step **110** is read into device controller memory.
>
> The flowchart continues in FIG. **3**B. **[A4]** In step **114** the NAND flash physical address range that was read into device controller memory is compared with the retained data representing the combination of the previous contents of the physical address range and the quantum of data to be written. In step **116**, if the retained data matches the newly stored data in the NAND flash memory, the write was a success, and the method exits in step **118**. However, if the retained data does not match the newly stored data in the NAND flash

> memory, the method executes step **120**, which identifies the next quantum of available SLC NAND flash memory addresses. In step **122**, a check is made to determine if additional SLC NAND flash memory is available, and, if not, the NAND flash memory system is marked as failed, prompting a system alert step **124**. However, if additional SLC NAND flash memory is available, the failed NAND flash physical address range is **[C]** <u>remapped to</u> the next available quantum of <u>SLC NAND flash memory</u> in step **126**. Execution then returns to step **110**, where the write is repeated.

(6:5-43 [emphasis added]). [A1]-[A4] highlights as issues (1) an ambiguity in claim 1 whether "retained data" resides in "controller memory," as well as (2) the inconsistent use of "physical address range" that was read into "device controller memory. [B1]-[B3] appears to be an incorrect reading of Fig. 3A as to the NAND flash operation of combining valid data with new data to be written to a new physical address. [C] is the manifestation of preferential writing into the SLC NAND flash memory that is dropped from express recitation in claims 1-7.

The two-sentence "wear leveling" embodiment discloses structure only by reference to known NAND flash technology: [5]

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[5] Even then, the two sentences confuse whether access to logical blocks or physical blocks are counted, particularly compared to the clustering of "hot" and "cold"

> Another application of one embodiment of the present disclosure, not depicted in any of the drawings, is to allocate "hot" blocks; i.e., those blocks that receive frequent writes, into the **SLC NAND flash memory module 28**, while allocating "cold" blocks; i.e., those blocks that only receive infrequent writes, into the **MLC NAND flash memory module 26**. This could be accomplished within the device controller **14** described above, which could simply maintain a count of those blocks that are accessed (written to) most frequently, and, on a periodic basis, such as, for example, every 1000 writes, or every 10,000 writes, transfer the contents of those blocks into the SLC NAND flash memory module **28**.

(6:44-56 [emphasis added].) None of this appears in the '546 claims.

B. Abstraction of the Claims Since 2018:

Section VIII of Dr. Sechen's declaration analyzes the unsupported abstraction of physical SLC and MLC modules of the system disclosed and claimed in the '298, '385 and '240 patents (respectively Ex. 1005 7:6-8:9, Ex. 1007 7:11-8:4, and Ex. 1009 7:30-8:7 and 8:20-59) to "memory space" and "memory elements," introduced in the application for the '300 patent (June 12, 2018, Application at 14 [Ex. 1012 at 19]), nearly seven years after the priority date. (Sechen ¶ 71.) Also introduced was

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logical data in ordinary NAND flash wear leveling and garbage collection. (Sechen ¶¶ 60 and 64.)

the abstraction away from the disclosed and '298, '385 and '240 patents-claimed preferential (NAND) remapping of some (logical) data to the SLC module to "mapping . . . necessitated by the system to maximize lifetime." (*Id.* ¶ 72.)

C. The Challenged Claims of the '546 Patent:

Challenged claim 1 of the '546 patent is its only independent claim:

1. A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements;

a bank of nonvolatile memory, including:

a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and

at least one SLC memory module including at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements;

the controller having associated controller memory for storing received data therein, the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data;

the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the <u>mapping</u> is performed as <u>necessitated by the system to maximize lifetime</u>, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

> wherein a failure of the data integrity test performed on the stored data by the controller results in a remapping of address space to a different physical range of addresses and transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test.

(7:28-8:34 [emphasis added].) The claim retains from the '300 patent the unsupported abstraction of "memory space" but reintroduces the '298, '385 and '240 patents physical MLC and SLC "memory modules" (Sechen ¶ 73). It also retained the '300 patent "mapping . . . to maximize lifetime," while not reciting any preferential mapping to the SLC module, but only to "a different physical range of addresses."

Claim 2 limits the "FTL" to a software "module" or firmware "module." Neither the abstract "controller" nor the FTL were given any structure as a "module" as the SLC and MLC hardware modules.

Claim 3 requires that one of the random access volatile memory ("RAVM") or the MLC and SLC "nonvolatile memory elements" are embedded in the controller.

Claim 4 requires that "the MLC and SLC nonvolatile memory elements" comprise flash memory.

Claim 5 requires the RAVM to be dynamic random access memory ("DRAM").

Claim 6 requires the RAVM to be static random access memory ("SRAM")

Claim 7 requires that an "SLC nonvolatile memory element includes a hard disk drive (HDD).

In view of the literal claims and disclosure of the '546 patent, the accompanying prior art references and supporting declaration of Dr. Sachen (Ex. 1002), Petitioner respectfully requests cancellation of the Challenged Claims as summarized in the following table.

Grounds	Exhibits
Ground 1: Claims 1-7 are unpatentable under 35 U.S.C. § 101 as directed at the abstract idea of a "memory space."	1001, 1002
Ground 2: Claims 1-7 are invalid under 35 U.S.C. § 112(a) because '546 patent specification fails to provide written description enabling, much less demonstrate the possession of any invention claimed.	1001, 1002, 1004

Ground 3: Claims 1-7 are invalid under 35 U.S.C. § 112(b) for failing to particularly point out and distinctly claim the subject matter which the inventor regards as his or her invention, among other things, claiming a combination of known SLC and MLC NAND flash modules with an abstract controller defined by functions ambiguously stated and not provided structure (physical or algorithmic) by the specification.	1001, 1002, 1034, 1041, 1042, 1043, 1045
Ground 4: Claims 1-7 are unpatentable under U.S.C. § 103 as obvious over Gavens and incorporated disclosures in view of a POSITA's knowledge of NAND flash technology.	1001, 1002, 1003, 1034, 1040, 1041, 1042, 1043, 1045, 1049, 1050, 1051, 1052

D. Person of Ordinary Skill in the Art

A person of ordinary skill in the art at the time of the claimed inventions would have a bachelor's degree in computer engineering, electrical engineering, computer science, or a closely related field, along with at least two years of experience in the design, development, implementation, or management of memory devices and

systems. A person with an advanced degree in a relevant field, such as computer or electrical engineering, would require less experience in the development and use of memory devices and systems. As is common, one could obtain equivalent knowledge and perspective from other life experiences as well. (Sechen ¶¶ 57 and 58).

VI. 37 C.F.R. § 42.204(b)(3): CLAIM CONSTRUCTION

Under 37 C.F.R. § 42.200(b), claims in a post-grant review proceeding are construed using the same claim construction standard that is used to construe claims in a civil action. This includes "construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent," *id*., and is standard articulated by the Supreme Court in *Phillips v. AWH Corp.,* 415 F.3d 1303 (Fed. Cir. 2005). Although claim construction may "rely on extrinsic evidence…including expert and inventor testimony, dictionaries, and learned treatises," such evidence must be considered "in the context of the intrinsic evidence." *Id.* at 1317, 1319.

Petitioner takes the initial position that the terms of the Challenged Claims "MLC memory modules" and "SLC memory module" (7:38 and 7:40) have established, customary meanings for a POSITA in computer memory, reflecting the development of NAND flash reviewed in Section IV over the decade before the July 19, 2011, priority date:

- "MLC memory modules" means "Physical modules each comprising an array of NAND cells as well as circuitry for writing two logical pages in two passes into a single row (physical page) of cells, for reading either page in that single row of cells, and for erasing a block of cells at one time."
- "SLC memory modules" means "Physical modules each comprising an array of NAND cells as well as circuitry for writing one logical page in one pass into a single row (physical page) of cells, for reading that page in that single row of cells, and for erasing a block of cells at one time."

A POSITA would only understand SLC and MLC to refer to NAND flash memory, at least because MLC multiple page level writing is distinguished from SLC single page level writing, and that distinction "SLC" is not applied to other non-volatile memory (Sechen ¶ 30). Also, as explained by Dr. Sechen (¶ 62, notes 10-13), "modules" in the hardware context would be understood by the POSITA to mean an interchangeable unit, such as a chip that provides "a complete function" such as the NAND flash chips that organize the NAND memory arrays operated in flash block erase and page writes. That is the foundational basis of the claimed system expressly disclosed as including two distinct, physical NAND flash modules, as reviewed at Section V(A) with the "NAND flash memory modules" description of (7:61-67) of the Fig. 4 embodiment. Fig. 4 is compared below to the textbook depictions at paragraph 27 of the Sechen declaration:

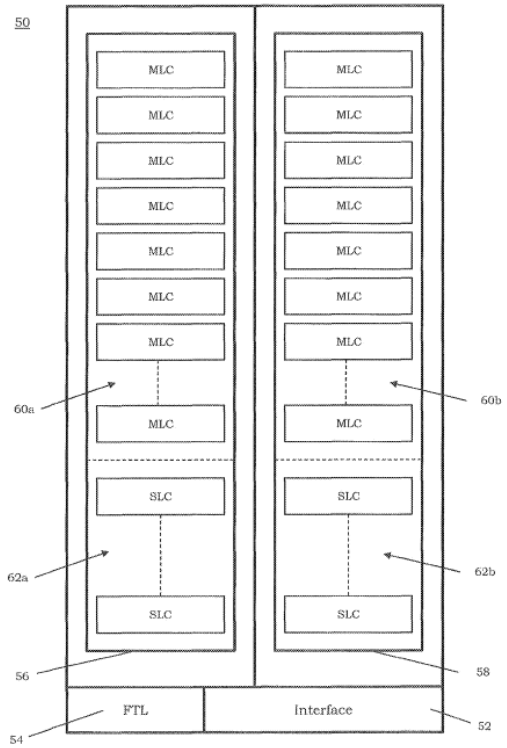
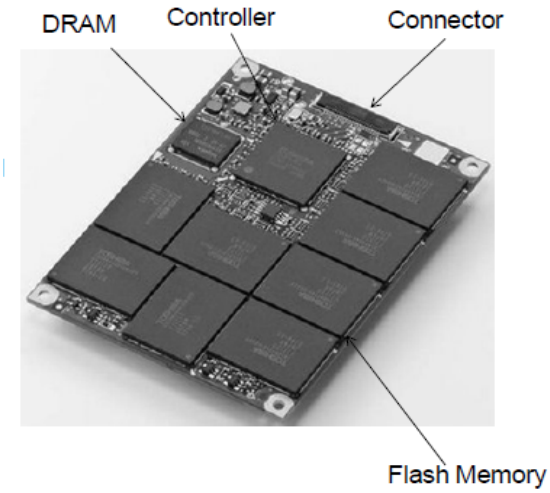


FIG. 4



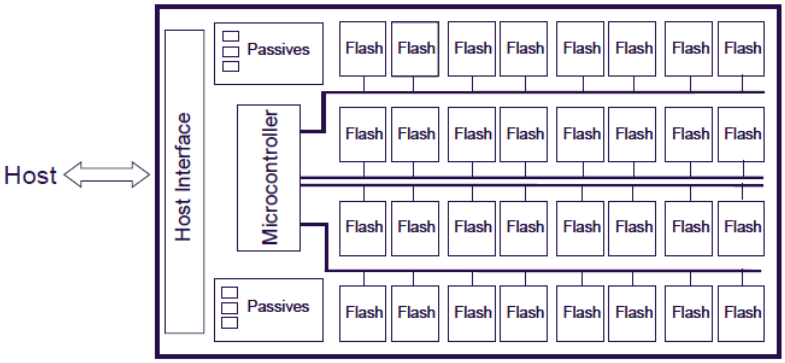


Fig. 2.32. Block diagram of a SSD

Further, the incorporated Embedded RAM Patents disclosure (Ex. 1004) intrinsically shows a NAND flash module with the required circuitry:

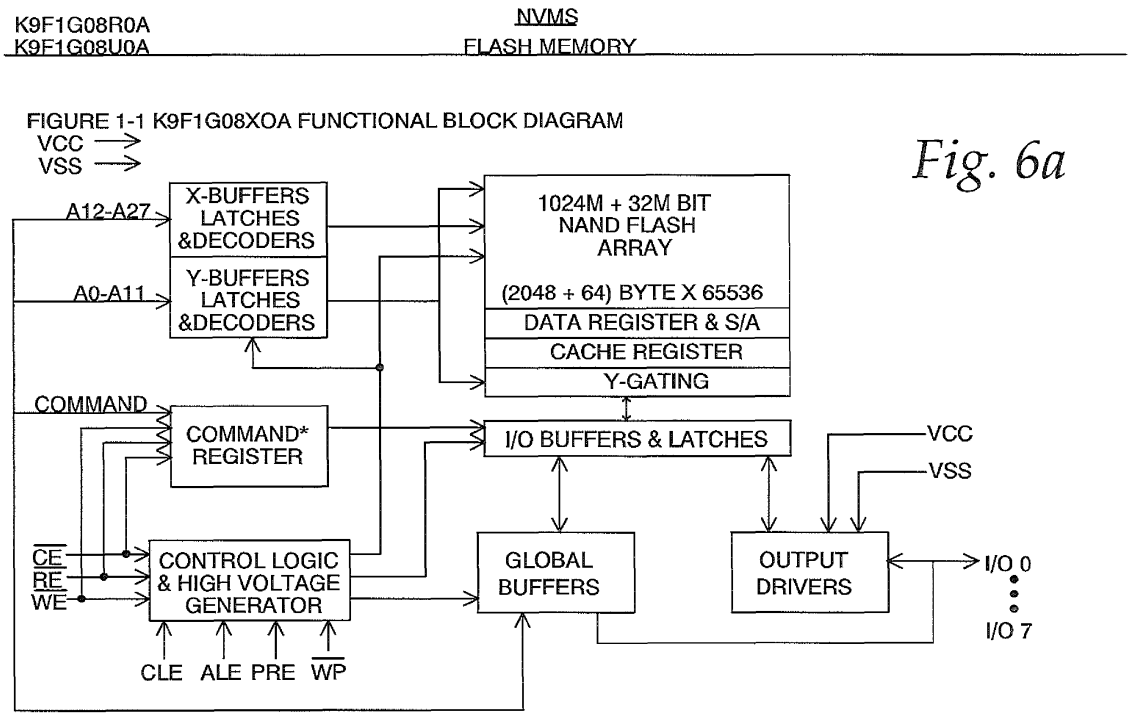


Fig. 6a

This is compared to textbook depiction at paragraph 27 of the Sechen declaration:

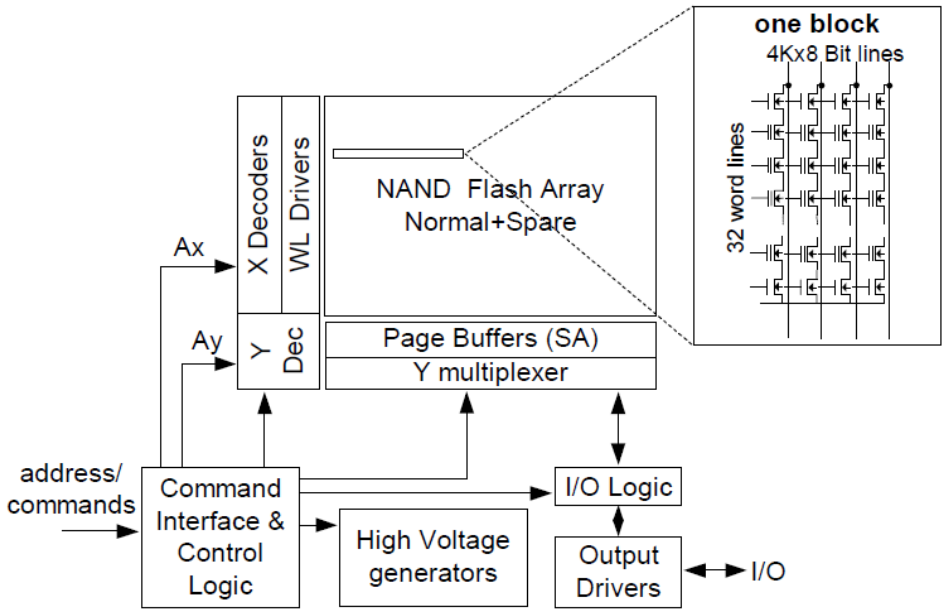


Fig. 15.1. NAND Flash memory block diagram

Thus, even if the POSITA needed to look to the specification to understand the references to SLC and MLC modules, required to operate the system claimed, the specification (including the incorporated disclosure) shows exactly the understood meaning. There is no disclosure in the specification of anything else. Although the specification suggests that CPM, RRAM or MAGRAM can be substituted for "SLC module," it is not a definition that "SLC module" means something other than its ordinary and customary meaning as a NAND flash module – which would be contradicted by the alternative technology's touted "write in place" that is fundamentally different from NAND flash.

Specification Fig. 3A step 116 "match" (also 6:29 and 6:32) between data to be written ("retained data") and data as written supports the construction of "comparing" (8:16) as direct bit-by-bit match, unlike indirect methods such as ECC. This was corroborated in the '300 patent prosecution express surrender of coverage of ECC error detection (Oct. 8, 2020, Amendment at 8-9 [Ex. 1012 at 36-37]), which was repeated in '546 prosecution argument (Sept. 22, 2023, Amendment at 13] [Ex. 1014 at 13] [requiring comparison in "two data stores"]).

Other important constructions are that the terms "memory space" and "memory element" are indefinite, as well as other terms that are indefinite in their

usage in the claims, such as "mapping . . . as necessitated by the system to maximize lifetime." These are argued as indefinite in the § 112(b) Ground 3 below.

Petitioner reserves the right to argue more specific constructions in response to Patent Owner's responses.

* * * * * * *

Grounds for Review Under 37 C.F.R. § 42.204(b)(4)-(5):

VII. GROUND 1: THE CHALLENGED CLAIMS CLAIM PATENT-INELIGIBLE SUBJECT MATTER UNDER 35 U.S.C. § 101 AS DIRECTED TO AN ABSTRACT IDEA, NAMELY, "MEMORY SPACE," WITHOUT CLAIMING SUBSTANTIALLY MORE THAN ASPECTS OF THE OPERATION OF A GENERAL-PURPOSE COMPUTER.

The Challenged Claims claim patent-ineligible subject matter under 35 U.S.C. § 101 as directed to an abstract idea without claiming substantially more than aspects of the operation of a general-purpose computer, such as limitations that improve the operation of such a computer. The Supreme Court has consistently expressed its concern with a patent claim preempting a field that would otherwise be open to inventive development, *Alice Corp. Pty. Ltd. v. CLS Bank International*, 573 U.S. 208, 216 (2014), *citing Bilski v. Kappos*, 561 U.S. 593, (2010) (finding a patent-ineligible abstract idea in a "long prevalent" practice). To prevent this preemption, the Court has held that patents directed to ineligible subject matter such as "abstract ideas" may not gain eligibility through recitation of elements or combination of elements, such as "computer functions [that] are 'well-understood, routine,

conventional activit[ies]' previously known to the industry." *Alice*, 573 U.S. at 225, *quoting Mayo Collaborative Services v. Prometheus Laboratories, Inc.*, 566 U.S. 66, 73 (2012). It is now familiar that the 35 U.S.C. § 101 subject matter eligibility analysis is divided into a step one of "determin[ing] whether the claims at issue are directed to a patent-ineligible concept,' such as an abstract idea" (*Alice*, 573 U.S. at 217) and, if so, a step two of "consider[ing] the elements of each claim both individually and 'as an ordered combination' to determine whether the elements 'transform the nature of the claim' into a patent-eligible application" (*id.*, *quoting Mayo*, 566 U.S. at 77-79).

As reviewed in paragraphs 71 and 73 of the Sechen declaration (Ex. 1002), the '300 patent substituted (and the '546 patent retained) the term "memory space" for the well-known SLC and MLC NAND flash modules. However, the word "space" appears in the specification only in the context of memory capability, for hard disk drives, "HDD space" (2:40) and total SLC and MLC memory in the recommended proportion in order to avail of the benefits of the disclosed hybrid SLC-MLC NAND flash system (5:10-12). A POSITA would therefore understand "memory space" in the context of the '546 patent to be a *storage capacity property* of a memory. The unqualified claiming of a property is an abstract idea or "disembodied concept" at the heart of what the Supreme Court's 35 U.S.C. § 101 jurisprudence regards as unpatentable subject matter. The claims fail to *integrate* the

claimed "memory space" into a practical application, and they do not provide an inventive concept to counterweigh (provide "significantly more than") the unqualified claiming of the property of "memory space." Particularly, the remaining limitations of these claims simply recite "well-understood, routine, and/or conventional" elements in a conventional arrangement and fail to recite an inventive concept. Thus, the claims fail the Alice/Mayo test and are ineligible subject matter under 35 U.S.C. § 101.

The same conclusion may be reached for the unqualified nature of the claiming of "memory space," which extends to subject matter well established to be outside of the scope of the patent statute. For example, the claim does not require that the "memory space" property be other than some transitory "signal" (information) (*compare In re Nuijten*, 500 F.3d 1346 (Fed. Cir. 1319)); it thus is ineligible as a "signal *per se.*"

The Challenged Claims are thus invalid as ineligible under 35 U.S.C. § 101.

VIII. <u>GROUND 2</u>: THE CHALLENGED CLAIMS LACK A WRITTEN DESCRIPTION DESCRIBING THE CLAIMED SUBJECT MATTER IN ACCORDANCE WITH 35 U.S.C. § 112(a).

As reviewed at paragraphs 71-73 of the Sechen declaration, (a) the abstraction in the '300 patent of "memory space" and "memory elements," departing from the disclosed and prior patents' hybrid memory system of SLC and MLC NAND flash modules with NAND flash-defined blocks and (2) the partial return in the '546 patent

to modules and elements of suggested physicality, introduce a host of issues with the later claims, which are attendant to the unsupported generalization of the claimed system and the abandonment of preferential writing to SLC NAND flash. The Lifetime Patents, particularly the '546 patent, purport to claim a species of NAND flash operation to a genus of "all nonvolatile memory having superior endurance to MLC NAND." However, even where substantial research was shown, as in *Amgen Inc. v. Sanofi*, 598 U.S. 594, 610 (2023), the specification must enable the full scope of the invention. As shown in Section X, there is no invention here at all, but even before we get there, the '546 patent fails under the following 35 U.S.C. § 112(a) defects among the many that Dr. Sechen identifies at paragraphs 76-91 of his declaration:

A. The Challenged Claims Limited by "Memory Space" Are Unsupported Under 35 U.S.C. § 112(a).

The challenged claims lack a written description describing the claimed subject matter in accordance with 35 U.S.C. § 112(a) because the term "memory space" (7:29-32) is mentioned in the specification only as a measure of memory capacity (2:40 and 5:10-12). Unless the recited capacity is read to limit the claimed system, the use of "memory space" in the claims is unsupported in the specification, which thus fails to enable a POSITA to practice the claimed invention. Certainly, the term is unsupported for other than NAND flash operation. (*See* Sechen ¶¶ 71,

73 and 80.) The Challenged Claims thus fail as unsupported under 35 U.S.C. § 112(a).

B. The Challenged Claims Limited by "Memory Element" Are Unsupported Under 35 U.S.C. § 112(a).

The Challenged Claims lack a written description describing the claimed subject matter in accordance with 35 U.S.C. § 112(a) because the term "memory element" (7:33-42, and *passim*) is not even mentioned in the specification. As reviewed in paragraphs 71 and 73 of the Sechen declaration (Ex. 1002), the '300 patent substituted (and the '546 patent retained) the terms "memory space" and "memory elements" for the NAND flash modules and their recited characteristic "plurality of individually erasable blocks." However, the term "memory element" appears nowhere in the specification, and "element" appears only as a boilerplate reference to claim elements (7:24-25).[6] To the extent that "memory elements" is considered a material limitation of the claimed system (as they must be), it is

[6] The word "element" is mentioned in the incorporated Embedded RAM Patents that described its Fig. 2 as an "exemplary NAND memory integrated circuit as one element of the NVMS" ('Rao '452 [Ex. 1004] 2:52-53), which corresponds to a NAND flash memory module.

unsupported in the specification and the claims fail as unsupported under 35 U.S.C. § 112(a).

C. The Challenged Claims Limited by "Mapping . . . As Necessitated by the System To Maximize Lifetime" Are Unsupported Under 35 U.S.C. § 112(a).

The Challenged Claims lack a written description describing the claimed subject matter in accordance with 35 U.S.C. § 112(a) because the specification does not disclose "mapping . . . as necessitated by the system to maximize lifetime" (8:24-25). As reviewed in paragraphs 72 and 73 of the Sechen declaration (Ex. 1002), the '300 patent introduced (and the '546 patent retained) this limitation without any support in the specification, including any mention of "maximiz[ing] lifetime" of anything. Dr. Sechen reviews the notions of extending or improving expected useful lifetime of a NAND flash memory system in the extensive background art, including through wear leveling, garbage collection and bad block management, with preference under some circumstances in operation of a hybrid SLC-MLC NAND flash system to map and write to SLC or pseudo-SLC (¶¶ 27-29, 38, and 40-56 particularly notes 8 and 9). Some of these different (and not "necessary"[7])

[7] The only "mapping" that is "necessary" for the disclosed systems is the particular L2P mapping necessary for operation of NAND flash memory operation with its defining erase-a-block-before-writing requirement admittedly inapplicable to

approaches to enhancing useful lifetime of a NAND flash memory system were acknowledged in the specification BACKGROUND (Sechen ¶ 60, note 9; 2:61-3:26: NAND flash wear leveling "prolonging the service life"). Dr. Sechen discusses the many ambiguities of the "maximize lifetime" clause at paragraphs 72, 73 and 77, including its abandonment of the Lifetime Patents theme of preferential mapping to an SLC NAND flash module. The bottom line is that it is unexplained in the specification any "mapping . . . necessitated by the system to maximize lifetime" of even the disclosed SLC-MLC NAND flash memory system, much less of memory systems of other than SLC-MLC NAND flash. The specification thus does not enable a POSITA to practice the claimed invention limited by the "maximize

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proposed alternative technologies. Moreover, that "mapping" in the context of a hybrid SLC and MLC NAND flash module, if it resulted as ordinarily in subsequent writing (preceded by erasure for data-occupied blocks), would *always* stress and thus incrementally decrease the useful lifetime of one block, leaving the other blocks, including any from which writing is remapped, at the same stage in life (subject to time effects) (Sechen ¶ 72). Thus, not every "mapping" would "maximize lifetime," while a certain mix of "mappings" might be calculated to avoid premature end to reliability of enough components to compromise the intended use of the system (*id.* note 9).

lifetime" clause or show that the inventor actually "possessed" that claimed invention. Thus, the claims fail under 35 U.S.C. § 112(a).

D. The Challenged Claims Limited by "Transfer of Data . . . From Those Physical Addresses Determined To Have Failed the Data Integrity Test" Are Unsupported Under 35 U.S.C. § 112(a) and Fail To Recite a Useful System for Storing Data.

The Challenged Claims lack a written description describing the claimed subject matter in accordance with 35 U.S.C. § 112(a) because the specification does not disclose "transfer of data . . . from a physical address determined to have failed the data integrity test" (8:31-34) and thus fails to enable a POSITA to practice the claimed invention. Further, the recited transfer would be pointless as propagating failed data, and its recital fails to recite a useful system for storing data. Thus, the claims as limited by this language fail under 35 U.S.C. § 112(a).

E. The Challenged Claims Limited by "At Least One Memory Element" Are Unsupported Under 35 U.S.C. § 112(a) and Fail To Recite a Useful System for Storing Data.

The Challenged Claims, limited by a minimal "at least one [MLC]/[SLC] nonvolatile memory element" in each [MLC]/[SLC] memory module (7:39-41), even if the term "memory element" were itself to pass the 35 U.S.C. §§ 112(a) and 112(b) challenge here, are unsupported under § 112(a) and fail to recite a useful system for storing data. Unlike some plausibility for the three pre-2018 Lifetime Patents' recitation of MLC and SLC modules with a "plurality of individually erasable blocks," the '546 patent's system with those modules having only "at least

one . . . memory element" (and without understood NAND flash circuitry for erasing/writing blocks) would not be understood by the POSITA as enabled by the specification (Sechen ¶ 82). The specification discloses two two-bank embodiments that purport to avail of the superior endurance of SLC. There is suggested a beneficial mix is "SLC NAND flash equal to 12.5% or 25% of MLC NAND flash" (5:10-12), which is consistent with Fig. 4 showing two banks each of 2+ SLC modules compared to 8+ MLC modules (which with MLCs storing twice SLCs, meeting the suggested 12.5% ratio). Figs. 6a and 6b of incorporated Rao '452 (Ex. 1004) show a Samsung NAND flash chip K9F108XOA with a "1024M + 32M BIT NAND FLASH ARRAY," clearly a "module" of 1-bit cells, *i.e.*, SLCs. The context thus is one SLC module of 1,024 blocks of 64 pages each. Contrasting with this context, each of the "system for storing data" recited in the claims of the '546 patent is met with just one SLC memory element and one MLC memory element each in a plurality of MLC modules). It is recited in claim 1 of the '546 patent that its system's mapping is of "blocks, pages, or bytes of data" (8:25-26). If a single block satisfies the requirements of the systems recited in the claims of the '546 patent, as literally it would (even allowing mapping of two MLC blocks in claim 1 of the '546 patent), that system would not be a useful one. It would be much less than the system disclosed by the specification as having multiple SLC and MLC modules each of a thousand blocks, useful for the disclosed and claimed preferential writing to an SLC

module. In a minimal, single-blocks system as claimed, there could be no multiple writes at all, given the NAND flash requirement of writing each update to another physical address, much less to enhance or maximize lifetime of the block or the system. And there is nothing in the specification describing the sufficient number of blocks or "memory elements" needed for the claimed inventions to enhance or maximize lifetime, or any way to determine a sufficient number. For at least these reasons, claim 1 of the '546 patent and all its dependent claims, are invalid under 35 U.S.C. § 112(a).

IX. GROUND 3: THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(b).

Claims 1-7 are invalid for indefiniteness under 35. U.S.C. 112(b) (formerly para. 2), because they recite limitations that, under *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898 (2014), considering the claims as a whole and as informed by the extrinsic record, fail to inform a POSITA with reasonable certainty about the scope of the claimed invention. A patent must be "precise enough to afford clear notice of what is claimed, thereby 'appris[ing] the public of what is still open to them.'" *Id.* at 909. "Otherwise there would be a zone of uncertainty which enterprise and experimentation may enter only at the risk of infringement claims." *Id.* Dr. Sechen identifies at paragraphs 76-91 multiple defects in the '546 patent claims, but Petitioner expressly raises here the following 35 U.S.C. § 112(b) defects:

A. The Challenged Claims Limited by "Memory Space" Are Indefinite Under 35 U.S.C. § 112(b).

As reviewed at Sections VII (§ 101 ineligibility) and VIII (A) (§ 112(a) lack of adequate written description), the meaning of the term "memory space" (7:29-32) is only disclosed only as a measure of memory capacity, rendering the Challenged Claims that recite the term invalid under those statutory provisions. If the term survives those challenges, it is nonetheless indefinite as to whether it refers to "logical" memory locations in a NAND flash L2P table or to something physical, such as the physical capacity available for NAND flash reading, writing and erasing for those logical memory locations. The term is even more indefinite in the context of other than NAND flash operation, which would not have the POSITA-understood NAND flash L2P mapping and writing structure. (*See* Sechen ¶¶ 71, 73 and 80.) The Challenged Claims thus fail as indefinite under 35 U.S.C. § 112(b).

B. The Challenged Claims Limited by "Memory Element" Are Indefinite Under 35 U.S.C. § 112(b).

The Challenged Claims, limited by the open-ended term "memory element" (7:39-41; *see* Sechen ¶ 71) are indefinite as that term. On its face, "memory element" is so open-ended that it could be any of claim 1's mapping is of "blocks, pages, or bytes of data" (8:25-26), or even a cell. As explained in Section VIII(B) (§ 112(a) inoperativeness), reading the term in context, "at least one [MLC]/[SLC] nonvolatile memory element" in each [MLC]/[SLC] memory module (7:39-41), even if the

POSITA chose "block," the system recited minimally would be inoperative. Moreover, the context raises the issue of whether the "memory element" is an SLC NAND module as shown in Fig. 2 of the incorporated Embedded RAM Patents (Rao 452 [Ex. 1004] 2:52-53; note 6 *supra*), and the recited "SLC memory module" (7:40) is something more inclusive, such as the "NAND flash memory module 50" of Fig. 4 (6:57-59). If the system is not limited to an SLC-MLC NAND flash system with POSITA-understood structure including NAND L2P mapping, block erase, multiple level page write-pulsing, the uncertainty is increased. The Challenged Claims thus fail as indefinite under 35 U.S.C. § 112(b).

C. The Challenged Claims Limited by "Mapping . . . As Necessitated by the System To Maximize Lifetime" Are Indefinite Under 35 U.S.C. § 112(b).

As reviewed in paragraphs 72, 73, 78 and 88 of the Sechen declaration, there are multiple axes of uncertainty in the claim 1 recitation of "mapping . . . as necessitated by the system to maximize lifetime" (8:24-25), carried over from the '300 patent extreme abstraction of previously claimed systems. Even if the limitation survives the §112(a) arguments in Section VIII(C), there remain the questions, first, of at least of what "mapping" is implicated. As explained in Section VIII(C) every mapping (which is necessary for NAND flash memory operation, but perhaps not for alternative, "write in place" technologies) in the life of a NAND flash system, if followed ordinarily by writing, decreases expected useful lifetime. Claim

1 (and particularly the "maximize lifetime" clause) fails to specify any user-elected strategy/configuration of NAND flash mapping to distribute wear (stress), as reviewed extensively in the Sechen declaration (¶¶ 27-29, 38, and 40-56, particularly notes 8 and 9; Duann [Ex. 1034]; Lee '794 [Ex. 1041]; Surtardja [Ex. 1042]; Moyashedi [Ex. 1043]; and Gavens [1045]). The '546 patent omitted any claim to the DETAILED DESCRIPTION's two-sentence ("hot" block v. "cold" block) "wear leveling" (to the SLC or MLC modules) embodiment (6:44-56) explained at note 5 *supra* (Sechen ¶¶ 60 and 64) to confuse logical and physical blocks. It *might* refer to the "remapping" (8:29) of the "data integrity test" elements of claim 1 (8:1-21 and 8:28-34) which roughly follow the NAND flash method steps in Figs.3A and 3B, explained at 6:5-44. However, the elements confuse what is transferred after remapping (see Section VIII(D)) and themselves are indefinite as when the test and remapping are performed (see Section IX(F). Just on the uncertainty of what mapping is implicated, a POSITA and the public are not clearly apprised of what is claimed. Accordingly, the Challenged Claims fail as indefinite under 35 U.S.C. § 112(b).

D. The Challenged Claims Are Indefinite Under 35 U.S.C. § 112(b) for Their Recitation of an Abstract "Controller" Limited by Functions in the Claims that Are Unsupported by Structure (Physical or Algorithmic) in the Specification.

Although two of the three main components of the disclosed and claimed in the '298, '385 and '240 patents are well-understood MLC and SLC NAND flash

modules with their supporting physical organization of and operations with NAND flash pages and blocks, the "controller" was left open-ended with no physical structure or even a tether to technology. The indefiniteness remains in the '546 patent even though there are recited additional components of a "random access volatile memory element" (7:42) and a (somewhat) distinct FTL (7:43-46). 35 U.S.C. § 112(f) has been applied through § 112(b) to find indefinite a functionally claimed limitation of a general term ("nonce" word) which is not supported in the specification by adequate disclosure of structure (physical or algorithmic). *E.g.*, *Rain Computing, Inc. v. Samsung Electronics America, Inc.*, 989 F.3d 1002 (Fed. Cir. 2021). "Controller" is such a nonce word, and the specification does not adequately disclose structure for its claimed functions.

Dr. Sechen reviews at paragraphs 64 and 65 of his declaration the basic functions attributed to the Lifetime Patent's "controller" – in the context of NAND flash operation. He specifically examined in paragraph 78 the functions attributed to the "controller" of '546 patent claim 1 (7:33) and found that none were provided structural (physical or algorithmic) detail in the specification. For example, the claim-recited functions of the "controller" are "to operate memory elements and

associated memory space" (7:33-34),[8] to "maintain an address table [that "maps logical and physical addresses adaptable to the system"] (7:44-46, 8:21-22], and "control[] access" of memory elements "for storage of the received data therein" (7:48-51). The claims also call for the controller to be "operable" to store data in the newly formulated MLC element and a newly recited random access volatile memory ("RAVM"). (8:5-8 [emphasis added]). None of these is disclosed in the specification, particularly relative to the new notions of MLC "element" and RAVM. The claims further call for the controller "performing a data integrity test . . . after at least a Write access operation . . . by comparing the stored data in the controller memory . . . to the retained data" (8:10-18 [emphasis added]) where failure "results in a remapping . . . and transfer" (8:28-31 [emphasis added]). There is no disclosure of how often and how long after a write operation (assumed for NAND flash operation) an integrity test is performed (see Section IX(F)). As detailed at paragraph 86 of Dr. Sechen's declaration, the identity and location of "the controller" memory are themselves indefinite. The "result"-based claiming is also problematic. Perhaps most importantly, the controller is responsible (with the FTL) for maintaining the address table that does the L2P mapping (7:45-46) and that

[8] The controller operates "Read access" (7:35-36) where there is no disclosure in the specification of "Read access" other than assumed for NAND flash.

mapping function "is performed as necessitated by the system to maximize lifetime" (8:22-25). As explained at Section IX(C), that "mapping . . . to maximize lifetime" function was not mentioned in the specification, much less with any structure, physical or algorithmic. And the function itself is indefinite as explained at Section IX(C).

Thus, the Challenge Claims fail to inform a POSITA with reasonable certainty and are thereby indefinite under 35 U.S.C. § 112(b).

E. The Challenged Claims Are Indefinite Under 35 U.S.C. § 112(b) Because They Recite Method Steps in the Context of a Claim to a System.

The '546 system claim 1 is based on known NAND flash memory systems with variations of functions following the method steps of Fig. 3A and 3B. In essence, its claims are to a method of operation of a system. However, stated as system clams but reciting the functional steps of the controller, the claims are invalid for impermissibly mixing product and process claims across different § 101 classifications, found to be indefinite under § 112(b). *IPXL Holdings, LLC v. Amazon.com, Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005); Manual of Patent Examining Procedure ("MPEP") § 2173.05(p)(II). A reason for this is to provide notice to a manufacturer of a product of how the product infringes rather than whether a user of the product takes steps that infringes the claimed steps. Here, as

alleged by Patent Owner in the pending suit, Phison is "a market leader in NAND Flash controllers" (Amended Complaint [Ex. 1062] ¶ 6).

In particular, claim 1 of the '546 patents is invalid under 35 U.S.C. § 112(b) for indefiniteness for the "controller *performing* a data integrity test." This is a method step within the system claim, which render the claims invalid under *IPXL* and MPEP § 2173.05(p)(II). As explained in Section IX(F), claim 1 doesn't specify when the recited comparison test is performed. Dr. Sechen explains at paragraphs 46 and 66 (and notes 8, 9 and 30 in particular), there are multiple options, exemplified under Gavens (Ex. 1045), to selectively configure a system to deploy data integrity tests (particularly indirect, ECC tests) and "adaptive rewrite" strategies at a statistically appropriate time late in the lifetime of a NAND flash memory system. Thus, it may be the user's choice if and when some of the recited controller functions are performed.

For these reasons, the Challenged Claims are invalid under 35 U.S.C. § 112(b) as indefinite.

F. The Challenged Claims Are Indefinite Under 35 U.S.C. § 112(b) Because It Is Uncertain Whether and When the Recited Comparison Test Is Required To Be Performed.

The Challenged Claims are indefinite under 35 U.S.C. § 112(b) because the limitation, "performing a data integrity test . . . after the at least a Write access operation" (8:10-13) does not specify when the test is performed other than after

some "Write access" – and not necessarily after *every* "Write access." In the embodiment described in the specification with two separate banks of MLC and SLC, "the controller conducts a data integrity test after every write." (5:1-7 [emphasis added].) However, in the same column description of the (perhaps misnamed) "read-modify-write" scheme, the read-after-every-write execution is qualified by "if time permits." (5:49-54.) The '546 patent claim 1 is silent on the issue. As explained in paragraph 79 of Dr. Sechen's declaration, a user might not wish to perform the resource-intensive bit-by-bit comparison test recited in claim 1 on any regular basis, when other well-known options in the prior NAND flash art (*e.g.*, Gavens [Ex. 1045]) keep incorrectly written data if they can be corrected by ECC upon reading and even defer deploying ECC until a statistically appropriate time. Because of this uncertainty, the Challenged Claims are invalid under 35 U.S.C. § 112(b) as indefinite.

X. GROUND 4: CLAIMS 1-7 OBVIOUS UNDER 35 U.S.C. § 103 OVER GAVENS IN VIEW OF POSITA KNOWLEDGE.

The '546 patent claims are obvious under *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007) because there is no gap between the prior art of multiple hybrid SLC-MLC NAND flash systems with post-write read bad-block management and wear leveling (Section IV) and the scope of the '546 claims, which are supported only by two hybrid SLC-MLC NAND flash embodiments fully quoted at Section V(A). A representative invalidating instance of the claims – that necessarily include,

if not limited only to NAND flash – is Gavens (Ex. 1045, incorporating by reference others of a large SanDisk portfolio), which discloses the '546 elements, where some MLC blocks are partitioned and configured for one-level (two states) or pseudo-SLC ("pSLC") operation. As reviewed by Dr. Sechen (¶ 43) and Gavens itself (*e.g.*, 12:6-10) the pSLC mode of operations enjoys superior endurance compared to MLC in multi-level mode, and it would be obvious to a POSITA to have one MLC module operating entirely in pSLC mode with expectation of success for the relative superiority to MLC in multi-level mode or use a "real" SLC module with assured success for the role (Sechen ¶ 93). The background art is exemplified by Duann (Ex. 1034), Lee '794 (Ex. 1041), Sutardja (Ex. 1042), and Moshayedi (Ex. 1043), which use SLC modules with MLC modules for similar functions and come to mind and would otherwise be obvious to combine with assured success. Claims 1-7 are obvious over Gavens in view of POSITA knowledge of computer memories.

A. Claim 1 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

1. [1Pre] A system for storing data comprising:

(Sechen ¶ 96): To the extent the preamble is limiting, Gavens discloses "a system for storing data," namely, the "flash memory device 90" that includes memory array 200. (Gavens, Fig. 1, ref. 90 and 16:41-17:20).

2. [1a] [1a1] memory space containing volatile memory space and [1a2] nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space;

(Sechen ¶ 97): **[1a1]** To the extent that this clause is not indefinite and "memory space" is understood to include all memory in the claimed system, Gavens discloses, or at least renders obvious, "memory space containing volatile memory space."

(Sechen ¶ 98): Gavens discloses memory containing volatile RAM and non-volatile memory array. (1:26: RAM; 1:18: Non-volatile memory; Fig. 1: Memory array 200 in memory chip 100.)

(Sechen ¶ 99): **[1a2]** Gavens' non-volatile memory array includes a first portion of pseudo-SLC memory and a second portion of MLC memory. Specifically, Gavens states that the first portion has each memory cell storing one bit of data and the second portion has each memory cell storing more than one bit of data. (4:32-34; 17:21-23.) The high-density storage portion (D3) has each memory cell storing 3 bits of data. The low-density storage portion (D1) has each memory cell storing 1 bit of data. (5:15-17, 50-53, 16:22-24, 20:31-34.) As disclosed in Fig. 14A, col. 16:15-22, the array of memory cells 200 is partitioned into a first portion 410 of lower density and a second portion 420 of high density having each cell storing multiple bits. For further reference, see: Fig. 7, col. 11:55-56, 12:6-7: A binary memory or single-level cell (SLC) memory has a population of cells with

each cell in one of two possible states; Fig. 8, col. 12:11-12, 31-33: A multi-state memory, for example, a triple-level cell or multi-level cell (TLC) or D3 memory has a population of cells with each cell in one of eight possible states, whereas a multi-level cell (MLC) or D2 memory has a population of cells with each cell in one of four possible states; Abstract, col. 6:18-21, 15:62-66, 16:16-22: The memory has a first portion operating with lower density storage and a second portion operating with a higher density; Fig. 15 ref. 500, col. 17:27-29: Configuring memory into a first portion having memory cells operating with a margin of error larger than that of a second portion; 20:53-59: The entire disclosure of Gorobets U.S. Appl. Ser. No. 12/642,584, published as U.S. Patent Appl. Pub. No. 2011/0153912 ("Gorobets '912," Ex. 1049) is incorporated into Gavens by reference:

- Gorobets '912 fig. 1, ¶ 56: RAM 130 in the controller 100;
- Gorobets '912 fig. 11, ¶ 109: Cache RAM 102 in the controller;
- Gorobets '912 fig. 20, ¶ 130: RAM 511 in the controller and in the memory 503;
- Gorobets '912 ¶ 18: Controller RAM.

These configuration details are understood by a POSITA to be consistent with the system disclosed in Gavens, which would be understood, as incorporated disclosures below, to focus on different features of the more inclusive SanDisk NAND flash memory systems. Not only are the features disclosed, but in my

analysis here, they are already combined with more than just a reasonable expectation of success. Thus, Gavens and incorporated references disclose claim element [1a].

3. [1b] at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements;

(Sechen ¶ 100): Gavens discloses at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements. For example, Gavens discloses a controller that manages read operations and write operations on memory. (Fig. 1 ref. 102; 8:17-18, 32-35: A controller 102 manages one or more memory chips 100 in the memory device 90. The controller 102 controls and manages higher level memory operations (*e.g.*, write) on the memory array 200; 2:56-58: A controller performs intelligent and higher level memory operations and interfacing.) Thus, Gavens discloses claim element [1b].

4. [1c] a bank of nonvolatile memory, including: [1c1] a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and [1c2]at least one SLC memory module including at least one SLC nonvolatile memory element;

(Sechen ¶ 101): **[1c]** Gavens discloses a bank of nonvolatile memory, including: a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and 2-state use of a partition of the MLC modules,

which obviously may be substituted with at least one SLC memory module including at least one SLC nonvolatile memory element. (*See* Sutardja [Ex. 1042], Moshayedi [Ex. 1043], and Lee '794 [Ex. 1041] as explained below.).

(Sechen ¶ 102): Gavens (Ex. 1045) discloses a bank of non-volatile memory chips including MLC (NAND flash) memory. (Fig. 1; 8:13-21: A memory device 90 includes one or more memory chips 100, which includes a memory array 200 of memory cells, which are capable of storing one or more bits of data; 1:18: Non-volatile memory; 9:49-54: A bank of NAND strings in the memory array comprises a series of memory transistors daisy-chained by their sources and drains; 10:31-34: A bank of p sense modules across an array of memory cells operates in parallel to read or program a group of p memory cells in parallel; Fig. 14A, col. 16:15-22: The array of memory cells 200 is partitioned into a first portion 410 configured for lower density (*e.g.*, pseudo-SLC) operation and a second portion 420 configured for high density (*e.g.*, native MLC, having each cell storing multiple bits) operation; 4:32-34, 17:21-23: The first portion has each memory cell storing one bit of data and the second portion has each memory cell storing more than one bit of data; 5:15-17, 50-53, 16:22-24, 20:31-34: The high-density storage portion (D3) has each memory cell storing 3 bits of data. The low-density storage portion (D1) has each memory cell storing 1 bit of data; 11:55-56, 12:6-7: A binary memory or single-level cell (SLC) memory has a population of cells with each cell in one of two possible states; Fig.

8; 12:11-12, 31-33: A multi-state memory or multi-level cell (MLC) memory has a population of cells with each cell in one of four possible states; Abstract; 6:18-21, 15:62-66, 16:16-22: The memory has a first portion operating with lower density storage and a second portion operating with a higher density; Fig. 15 ref. 500; 17:27-29: Configuring memory into a first portion having memory cells operating with a margin of error larger than that of a second portion; Fig. 6; 11:9-10: A memory array organized in erasable blocks; 11:4-8: The array of memory cells is divided into blocks of memory cells. Each block contains the minimum number of memory cells that are erased together as understood in NAND flash operation.)

(Sechen ¶ 103): Gavens differs from the claimed SLC and MLC NAND flash modules by having some portions of its aggregated MLC modules partitioned and configured to operate in pseudo-SLC (2-state or 1 bit) mode. (8:18-20 ["The memory chip 100 includes memory array 200 of memory cells with each cell capable of being configured as a multi-level cell ('MLC')]; 18:12-20 [explaining the array of memory cells 200 "partitioned" into portions with higher density (more bits per cell) and lesser density (fewer bits per cell) operation with associated margins of error; 17:59 ["A first portion is configured to store one bit per cell," citing U.S. Patent No. 5,930,167 to Lee et al. ["Lee '167," Ex. 1050], incorporated by reference.]) Gavens clearly satisfies the **[1c1]** limitation of multiple MLC memory modules in the understood operation of a NAND flash system that employs Gavens's schemes of

preferential writing to lower density memory. As to the **[1c2]** limitation of an SLC memory module, it would be obvious to a POSITA to have one MLC module operating entirely in pSLC mode with expectation of success for the relative superiority to MLC in multi-level mode or substitute a "real" SLC module understood by a POSITA to have even better endurance than pseudo-SLC (Sechen ¶ 43), both with a clear expectation of success. Use of dedicated SLC and MLC modules for preferential writing was well-known prior to the priority date (Sechen ¶¶ 40-42).

(Sechen ¶ 104): Lee '794 (Ex. 1041) discloses an allocation of logical blocks pre-determined to have most frequent writes (updates, such as system data and user directories) to a distinct SLC module and less frequent writes (user data) to a distinct MLC module. (Lee '794 [Ex. 1041] Fig. 2 refs. 226, 228, 5:10-13: The SLC flash memory array 226 portion of the module would include at least one flash memory "element." Likewise, the MLC flash memory array 228 portion of the module would include at least one MLC flash memory "element"; 6:53-7:39: allocation of logical blocks pre-determined to have most frequent writes (updates, such as system data and user directories) to a distinct SLC module and less frequent writes (user data) to a distinct MLC module.)

(Sechen ¶ 105): Sutardja (Ex. 1042) discloses a controller that is adapted to allocate those blocks (understood to be NAND flash) that receive the most frequent

writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module (disclosed as higher-cost, faster memory distinct from another lower-cost, slower memory). (Sutardja [Ex. 1042] ¶ 141).

(Sechen ¶ 106): Moshayedi (Ex. 1043) discloses a controller that is adapted to allocate those blocks (again understood to be NAND flash) that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module (explicitly disclosed as distinct from an MLC non-volatile memory module). (Moshayedi [Ex. 1043] Abstract, disclosing a system that keeps frequently written data, which results in frequently erased blocks, in the SLC flash module, and relatively static data in MLC flash module.

(Sechen ¶ 107): Thus, Gavens discloses claim element [1c] with the POSITA's knowledge of obvious substitution of a "pure" SLC module for its partitioned and 2-state (pseudo-SLC) configured MLC module.

5. [1d] at least one random access volatile memory element;

(Sechen ¶ 108): Gavens discloses at least one random access volatile memory element. For example, Gavens discloses volatile RAM. (1:26: RAM; Fig. 16A: First section 411 for caching in first portion 410; 4:35-37: The first portion serves as a cache for incoming data, so a cache copy of the input data is programmed into the cache; 20:53-59: The entire disclosure of Gorobets '912 [Ex. 1049], is incorporated by reference:

- Gorobets '912 fig. 1, ¶ 56: RAM 130 in the controller 100.
- Gorobets '912 fig. 11, ¶ 109: Cache RAM 102 in the controller.
- Gorobets '912 fig. 20, ¶ 130: RAM 511 in the controller and in the memory 503.
- Gorobets '912 ¶ 18: Controller RAM.)

Sechen declaration paragraph 99 applies, and thus Gavens and incorporated references disclose claim element [1d].

6. [1e] a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements;

(Sechen ¶ 109): The '546 patent uses "flash translation layer (FTL)" to refer to the well-known concept of translating logical host addresses to physical flash addresses, *i.e.*, the functionality that implements the logical-to-physical address map. (2:40-43.) That is, the FTL "make[s] linear flash memory [flash addresses] appear to the system like a disk drive [via logical host addresses]." (3:61-65.)

(Sechen ¶ 110): Gavens discloses a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements. For example, Gavens discloses that a controller implements a memory block management system that maintains a directory in memory. (Fig. 1 ref. 102; 8:17-18, 32-39: The controller 102 manages one or more memory chips 100 in the memory device 90. The controller 102

manages higher-level memory operations, for example, read and write. A memory block management system implemented in the controller 102 maps the logical sectors to the physical structure of the memory array; 2:56-58: A controller performs intelligent and higher level memory operations and interfacing; Fig. 15 ref. 550; 17:39-40: Identifying the last written copy as valid data for a subsequent read; 20:53-59.)

(Sechen ¶ 111): Gavens 20:53-59: The entire disclosure of Gorobets '912 (Ex. 1049), is incorporated by reference. (Gorobets '912 Figs. 8-9, ¶¶ 95-99: The memory-side memory manager 300 is implemented in the controller 100 to manage the storage and retrieval of the data of host logical sectors among metablocks of the flash memory. The memory manager 300 comprises a back-end system 320, which includes a number of software modules including a media management layer 330 and a dataflow and sequencing layer 340. The media management layer 330 organizes logical data storage within a flash memory meta-block structure. The dataflow and sequencing layer 340 sequences and transfers sectors of data between a front-end system and a flash memory. The dataflow and sequencing layer 340 includes a flash control layer 346. The memory manager 300 is preferably implemented in the controller 100 and translates logical addresses received from the host into physical addresses within the memory array.)

(Sechen ¶ 112): See also Gavens 8:40-43: The entire disclosure of U.S. Patent Appl. Pub. No. 2010/0172180 by Paley ("Paley '180," Ex. 1051) is incorporated by reference. (Paley '180 figs. 8-9, ¶¶ 155-159, 201-202: The memory-side memory manager 300 is implemented in the controller 100 to manage the storage and retrieval of the data of host logical sectors among metablocks of the flash memory. The memory manager 300 maintains system control data and directory data associated with its operations. The memory manager 300 comprises a back-end system 320, which includes a number of software modules including a media management layer 330 and a dataflow and sequencing layer 340. The media management layer 330 organizes logical data storage within a flash memory meta-block structure. The dataflow and sequencing layer 340 sequences and transfers sectors of data between a front-end system and a flash memory. The dataflow and sequencing layer 340 includes a flash control layer 346. The memory manager 300 is preferably implemented in the controller 100 and translates logical addresses received from the host into physical addresses within the memory array.)

(Sechen ¶ 113): See also U.S. Prov. Pat. Appl. No. 61/509,257 (Ex. 1003, admitted prior art as stated in the "Description of the Prior Art" section) ¶ 7, also in the BACKGROUND of '546, as reviewed at ¶ 60 above): The flash translation layer (FTL) performs the function of mapping logical pages to physical flash pages.

(Sechen ¶ 114): Accordingly, Gavens discloses, or at least renders obvious, that "wherein the at least one controller, or FTL, or a combination of both [Gavens' controller implementing the FTL layer] maintain an address table [Gavens' directory, *i.e.*, logical-to-physical map] in one or more of the memory elements [Gavens' non-volatile memory] and random access volatile memory [RAM in Gavens' controller]." Thus, Gavens discloses claim element [1e].

7. [1f] the controller [1f1] having associated controller memory for storing received data therein, the controller [1f2] controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored data, the controller, [1f3] in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, [1f4] operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data;

(Sechen ¶ 115): Gavens renders obvious the controller having associated controller memory for storing received data therein, the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the

given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data.

(Sechen ¶ 116): For example, Gavens discloses that the controller has buffer memory or cache memory for storing data received from a host; the controller controls access of the first portion of SLC memory, the second portion of MLC memory, and the RAM for storing the data; and in a write operation, the controller transfers the data from the buffer memory or the cache memory to the second portion of MLC memory to store the data in the second portion of MLC memory. (Fig. 1 ref. 102, 8:17-18, 32-35: A controller 102 manages one or more memory chips 100 in the memory device 90. The controller 102 controls and manages higher level memory operations (e.g., write) on the memory array 200; 12:64-67: As data is received from a host, a page of data is staged in the controller 102. The data page is then written to the memory array 200; 16:41-49: The original copy of a page of incoming data is cached. A first copy of the page of incoming data is written to the second portion; Fig. 14A: The write input data page is the first copy of the data page in the second portion 420 of higher density; Fig. 15 ref. 510, col. 17:30-31: Programming a first copy of a group of input data in the second portion; 4:18-19, 15:66-67: Data is written to the second portion; 18:1-4: The first portion is divided into a first section and a second section, and the first section of the first portion serves

as a cache; 17:43-46: The first portion serves as a cache for incoming data, so a cache copy of the input data is programmed into the cache, then a first copy of the data is programmed into the second portion; Fig. 17 refs. 602, 610: Programming a cached copy of a group of input data in a first section of the first portion. Programming a first copy of the group of input data in the second portion.; Fig. 16A, 18:9-12: A cached copy of data page in the first section 411 the of first portion 410; 5:53-54: Input data is first staged in D1 (SLC) and subsequently folded into D3 (TLC).)

(Sechen ¶ 117): See also Gavens 16:29-40: The entire disclosure of Chen '528 is incorporated by reference. (Chen '528 [Ex. 1040] 4:39-41: The controller 20 contains buffer memory for the user data being written to or read from the memory array.)

(Sechen ¶ 118): Further, Gavens 20:53-59: The entire disclosure of Gorobets '912 (Ex. 1049), is incorporated by reference:

- Gorobets '912 ¶¶ 130, 136, 143-44: The data is transferred from the host 501 onto the volatile buffer memory RAM 511 inside the controller, then transferred to the binary section D1 515 of the non-volatile memory 513, and then transferred to the MLC section D3 517 of the non-volatile memory 513.
- Gorobets '912 abs., ¶ 95: The memory manager 300 is implemented in the controller 100, manages the storage and retrieval of data in the flash memory 200, and maintains system control data and directory data for the flash memory 200 and the controller RAM 130.

- Gorobets '912 ¶ 104: Flash memory includes a first portion, which is the main memory, and a second portion, which is a cache of data to be written to the main memory.

(Sechen ¶ 119): See also 17:57-67: The entire disclosure of Lee '167 is incorporated by reference. (Lee '167 [Ex. 1050] Abstract, Fig. 7, claims 1, 4: EEPROM flash memory includes an MLC portion and an SLC portion that is used as a write cache. Incoming data is first written to the SLC write cache, then later, the data is read from the SLC write cache and rewritten to MLC.)

(Sechen ¶ 120): It would have been obvious to retain the data stored in the RAM so that the data stored in the RAM can serve as cache for faster access of the data in the future. (Gavens 20:53-59: The entire disclosure of Gorobets '912 [Ex. 1049] is incorporated by reference. Gorobets '912 ¶¶ 24, 109: Use of RAM as a controller cache of the memory controller.)

(Sechen ¶ 121): Despite the ambiguity in claim elements [1f] and [1g] as to "controller memory" and RAVM, explained at Sechen declaration paragraphs 85 and 86 above, if the claim survives 35 U.S.C. § 112 challenge, Gavens, as reviewed above, discloses [1f1] "associated controller memory" and [1f4] RAVM in its cache and by incorporated disclosures that are consistent with Gavens operations for holding incoming data written to the MLC module. Gavens thus discloses this limitation [1f].

8. [1g] the controller [1g1] performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by [1g2] reading the stored data to the controller memory and [1g3] comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

(Sechen ¶ 122): Gavens renders obvious the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation.

(Sechen ¶ 123): For example, Gavens discloses that the controller performs a post-write read check on the data stored in the second portion of MLC memory after the write operation by reading the data from the second portion of MLC memory to data laches or the controller and comparing the read data to a cached copy of the data. (Abstract; 6:22-23: After a copy of data is written to the second portion, the data is read from the second portion and checked for errors; 4:19-21, 15:67-16:1:

After the data is written to the second portion, the data is read back to check for excessive error bits; 5:1-3: After writing to a high density storage portion, a post-write read checks if the error rate is within a prescribed limit; 6:4-6, 24:45-50: Post-write reading every memory cell to check what has been written; Title: Post-write read to manage errors.)

(Sechen ¶ 124): See also Fig. 15 ref. 520, 17:32-33: Reading the first copy from the second portion; 4:55-60: The first copy in the second portion and the cached copy in the first portion are loaded into a set of data laches on an integrated circuit chip and compared to check for error bits; 16:46-49: The first copy of the data page is read back in a post-write read to determine if there are any errors by comparing with the original copy which was cached; 18:30-44: The memory array includes data latches onto which the first copy in the second portion and the cached copy in the first portion can be loaded and compared. The comparison is not made at the controller; 12:67-13:4, 29:57-59: Data is read from the second portion, latched in the data latches 430, and shifted out to the controller 102. The controller 102 compares the ECC in the read data to a second version of ECC computed from the read data. Gavens expressly discloses that this error check may be "either by <u>comparison with the original copy which may be cached</u> **or** by checking the EDC portion of the ECC" (16:47-49 [emphasis added]). Although Rao's direct comparison is wasteful, it was a known alternative. (*See* Sechen ¶¶ 47, 49 and 50).

(Sechen ¶ 125): It would have been obvious to compare the data read from the second portion of MLC memory to a cached copy of the data retained in the RAM. (20:53-59): The entire disclosure of Gorobets '912, is incorporated by reference:

- Gorobets '912 ¶¶ 24, 109: Use RAM as a controller cache of the memory controller.
- Gorobets '912 ¶ 104: Flash memory includes a first portion, which is the main memory, and a second portion, which is a cache of data to be written to the main memory.
- Gorobets '912 ¶¶ 130, 136, 143-44: The data is transferred from the host 501 onto the volatile buffer memory RAM 511 inside the controller, then transferred to the binary section D1 515 of the non-volatile memory 513, and then transferred to the MLC section D3 517 of the non-volatile memory 513.

(Sechen ¶ 126): See also Gavens 8:40-43: The entire disclosure of Paley '180 (Ex. 1049) is incorporated by reference. (Paley '180 ¶ 155: The memory manager 300 in the controller 100 maintains system control data and directory data associated with its operations among the flash memory 200 and the controller RAM 130.

(Sechen ¶ 127): Accordingly, Gavens discloses this limitation [1g].

9. [1h] wherein [1h1] the address table maps logical and physical addresses adaptable to the system, wherein [1h2] the mapping is performed as necessitated by the system to maximize lifetime, and wherein [1h3] the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

(Sechen ¶ 128): Gavens discloses the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories.

(Sechen ¶ 129): Relative to limitation **[1h1]**, Gavens discloses that the directory maps logical addresses and physical addresses adaptable to the NAND flash memory device. Relative to limitation **[1h2]**, to the extent it can be understood if it survives 35 U.S.C. § 112 scrutiny, it would met by the kind of NAND flash wear-management disclosed in Gavens and long known in the art (Sechen ¶¶ 28, 29, 40-45, and 51-56) (or alternatively, the remapping of limitations [1f], [1g] an [1i]): the mapping is performed as necessitated (implemented) by the flash memory device to maximize (increase) the (expected) lifetime of the flash memory device, and **[1h3]** the mapping maps a block of data in the non-volatile memory array. (8:36-39: A memory block management system implemented in the controller maps the logical sectors to the physical structure of the memory array; 15:2-6: An important consideration for flash memory is that it has an endurance problem as it ages with use. The error rate increases with the number of program-erase cycling; 16:34-37: It

is desirable to have longer operational life of memory cells; Fig. 15 ref. 550, col. 17:39-40: Identifying the last written copy as valid data for a subsequent read; 11:19-22: The group of cells erasable together consists of one or more addressable erase units. The erase unit or a block stores one or more pages of data. A page is a minimum unit of programming and reading; 21:21-23: Each block contains data from a well-defined group of logical addresses; 5:41-45: A hot count tracks the number of times each physical block has been cycled through erase and program operations.

(Sechen ¶ 130): See also Gavens 8:40-43: The entire disclosure of Paley '180 is incorporated by reference. (Paley '180 [Ex. 1051] Figs. 8-9, ¶¶ 155-159, 201-202: The memory-side memory manager 300 is implemented in the controller 100 to manage the storage and retrieval of the data of host logical sectors among metablocks of the flash memory. The memory manager 300 maintains system control data and directory data associated with its operations. The memory manager 300 comprises a back-end system 320, which includes a number of software modules including a media management layer 330 and a dataflow and sequencing layer 340. The media management layer 330 organizes logical data storage within a flash memory meta-block structure. The dataflow and sequencing layer 340 sequences and transfers sectors of data between a front-end system and a flash memory. The dataflow and sequencing layer 340 includes a flash control layer 346. The memory manager 300

is preferably implemented in the controller 100 and translates logical addresses received from the host into physical addresses within the memory array.)

(Sechen ¶ 131): See further Gavens 20:53-59: The entire disclosure of Gorobets '912 is incorporated by reference. (Gorobets '912 [Ex. 1049] Figs. 8-9, ¶¶ 95-99: The memory-side memory manager 300 is implemented in the controller 100 to manage the storage and retrieval of the data of host logical sectors among metablocks of the flash memory. The memory manager 300 maintains system control data and directory data associated with its operations. The memory manager 300 comprises a back-end system 320, which includes a number of software modules including a media management layer 330 and a dataflow and sequencing layer 340. The media management layer 330 organizes logical data storage within a flash memory meta-block structure. The dataflow and sequencing layer 340 sequences and transfers sectors of data between a front-end system and a flash memory. The dataflow and sequencing layer 340 includes a flash control layer 346. The memory manager 300 is preferably implemented in the controller 100 and translates logical addresses received from the host into physical addresses within the memory array.)

(Sechen ¶ 132): See also Gavens 17:57-67: The entire disclosure of Lee '167 is incorporated by reference (Lee '167 [Ex. 1050] 2:54-3:7: The usual desire to evenly wear the memory. Avoid using one portion of memory much more than other portions. Maintain separate counts of the number of times that each sector has been

erased and programmed to even the wear among the sectors); Gavens 16:29-40: The entire disclosure of Chen '528 (Ex. 1040) is incorporated by reference (Chen '528 10:41-60: Storing the most frequently written data in SLC and less frequently written data in MLC avoids the need to replace blocks that reach their endurance limit).

(Sechen ¶ 133): Thus, element [1h] is met by the more specific system life-extending approaches disclosed in Gavens, either background "wear leveling" reviewed above or remapping which is disclosed in Gavens to meet elements [1f], [1g] and 1[i].

10. [1i] wherein a failure of the data integrity test performed on the stored data by the controller results in [1i1] a remapping of address space to a different physical range of addresses and [1i2] transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test.

(Sechen ¶ 134): Gavens discloses a failure of the data integrity test performed on the stored data by the controller results in a remapping of address space to a different physical range of addresses and transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test.

(Sechen ¶ 135): For example, Gavens discloses that a failure of the post-write read check performed on the data stored in the second portion of MLC memory by the controller results in a remapping of the logical address of the data from the

physical address in the second portion of MLC memory to a different physical address in the first portion of SLC memory and a rewriting of the cached data to the first portion of SLC memory. (Fig. 14B: If post-write read failed, then rewrite the input data page as a second copy of data page in first portion 410 of lower density; 5:3-7: If post-write read checks results in an error rate above the prescribed limit, then the data is rewritten to another, less error-prone portion that has each memory cell storing fewer data bits per cell; 17:9-12: After the post-write read detects that the number of error bits in the data page has exceeded the predetermined amount, a second copy of the data page is made from the original data which was cached, and the second copy is rewritten to the first portion). Again, Gavens expressly discloses that this error check may be "either by comparison with the original copy which may be cached **or** by checking the EDC portion of the ECC" (16:47-49 [emphasis added]).

(Sechen ¶ 136): See also Gavens Fig. 15, refs. 530, 540,17:34-38: Does the error exceed a predetermined number of error bits? If yes, then programming a second copy of the group of input data in the first portion; Abstract, 6:23-25: If the copy in the second portion has excessive error bits, then a copy is written to the first portion; 4:21-22, 16:1-3: If error bits exceeds a predetermined amount, then the data is rewritten at the less error-prone first portion; 18:53-67: After a post-write read detects excessive number of error bits, a second copy of the data page is taken from

the cached copy and rewritten to the second section of the first portion. The directory in the block management system embodied in the firmware of the controller is updated to direct subsequent access to the second copy. Thus, Gavens discloses limitation **[1i1]**.

(Sechen ¶ 137): See also 4:62-67: A directory in a block management system embodied in the firmware of the controller is updated to render the first copy in the second portion obsolete and to direct subsequent access to the cached copy in the first portion. The cached copy in the first portion replaces the first copy in the second portion as the valid data; 17:15-20: A directory in a block management system embodied in the firmware of the controller is updated to render the first copy in the second portion obsolete and to direct subsequent access to the second copy in the first portion. The second copy in the first portion replaces the first copy in the second portion as the valid data. Thus, Gavens discloses limitation **[1i2]** and element **[1i]**.

(Sechen ¶ 138): In the rewriting reviewed in the immediately preceding paragraph showing disclosure of limitation [1i1], the rewriting is clearly a transfer of "data corresponding to retained data," such as in "the original data which was cached" to "those remapped physical addresses from those physical addresses determined to have failed the data integrity test," that is, the "bad" MLC blocks. Thus, Gavens discloses limitation [1i2].

* * * * * * * * * * *

(Sechen ¶ 139): In summary, Gavens, with its incorporated references, discloses each limitation of '546 claim 1 as understandable, with the POSITA's understanding that Gavens's extensive technology-justified teachings are readily combined and extended (with clear expectation of success) to meet the claim's base MLC and SLC modules and unsupported abstractions.

B. Claim 2 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

1. [2Pre] The system of claim 1,

See Section X(A) for claim 1.

2. [2] wherein the FTL is a software module, or a firmware module containing software updates.

(Sechen ¶ 141): Gavens discloses the FTL is a software module, or a firmware module containing software updates. For example, Gavens discloses that the memory block management system implemented in the controller is software. (Fig. 1, ref. 102, col. 8:36-39: A memory block management system implemented in the controller 102 maps the logical sectors to the physical structure of the memory array; Fig. 1, ref. 60, 8:44-45: The firmware 60 provides code to implement the functions of the controller 102; 18:64-67: A directory in the block management system embodied in the firmware of the controller is updated to direct subsequent access to the second copy; 4:62-67: A directory in a block management system embodied in the firmware of the controller is updated to render the first copy in the second portion

obsolete and to direct subsequent access to the cached copy in the first portion. The cached copy in the first portion replaces the first copy in the second portion as the valid data.)

(Sechen ¶ 142): See also 17:15-20: A directory in a block management system embodied in the firmware of the controller is updated to render the first copy in the second portion obsolete and to direct subsequent access to the second copy in the first portion. The second copy in the first portion replaces the first copy in the second portion as the valid copy. Thus, Gavens, in view of the knowledge of a POSITA, discloses claim 2.

C. Claim 3 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

1. [3Pre] The system of claim 1,

See Section X(A) for claim 1.

2. [3] wherein at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller.

(Sechen ¶ 144): Gavens discloses at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller.

(Sechen ¶ 145): For example, Gavens discloses that the RAM is embedded in the controller. (20:53-59: The entire disclosure of Gorobets '912 [Ex. 1049] is incorporated by reference:

- Gorobets '912 fig. 1, ¶ 56: RAM 130 in the controller 100;
- Gorobets '912 fig. 11, ¶ 109: Cache RAM 102 in the controller;
- Gorobets '912 fig. 20, ¶ 130: RAM 511 in the controller;
- Gorobets '912 ¶ 18: Controller RAM.)

(Sechen ¶ 146): See also Gavens (8:40-43: The entire disclosure of Paley '180 [Ex. 1050] is incorporated by reference:

- Paley '180 Fig. 1, ¶ 119: RAM 130 in the controller 100;
- Paley '180 Fig. 15, ¶ 197: Cache RAM 102 in the controller).

(Sechen ¶ 147): Thus, Gavens, in view of the knowledge of the POSITA, discloses claim 3.

D. Claim 4 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

1. [4Pre] The system of claim 1,

See Section X(A) for claim 1.

2. [4] wherein the MLC and SLC nonvolatile memory elements comprise flash memory.

(Sechen ¶ 149): Gavens, which would be understood by a POSITA to describe a NAND flash system with multiple MLC NAND flash modules, expressly describes its MLC non-volatile memory modules as including MLC NAND flash memory elements, which by definition are flash memory. (Fig. 4, 9:49-50: A page of memory cells in the memory array 200 is organized in the NAND configuration; 1:18-19,

4:14-18: Flash memory having a first portion and a second portion storing higher density compared to the first portion; 2:65-66, 8:65-67: Flash memory devices with NAND string structures; Fig. 1 ref. 90: Flash memory device.)

(Sechen ¶ 150): As explained at Sechen declaration paragraphs 93 and 101-107, a POSITA would readily and successfully substitute for Gavens' partitions of MLC memory elements configured for 2-state pseudo-SLC operation an SLC non-volatile memory module which is understood to include SLC NAND flash memory elements. As to Gavens's MLC NAND flash memory operated in pseudo-SLC mode, they are also described as flash memory. (Fig. 4, col. 9:49-50: A page of memory cells in the memory array 200 is organized in the NAND configuration; 1:18-19, 4:14-18: Flash memory having a first portion and a second portion storing higher density compared to the first portion; 2:65-66, 8:65-67: Flash memory devices with NAND string structures; Fig. 1: Flash memory device 90.)

(Sechen ¶ 151): Thus, Gavens, in view of the knowledge of the POSITA, discloses claim 4.

E. Claim 5 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

1. [5Pre] The system of claim 1,

See Section X(A) for claim 1.

2. [5] The system of claim 1, wherein the random access volatile memory element is dynamic random access memory.

(Sechen ¶ 153): In view of a POSITA's understanding that dynamic random access memory (DRAM) is common type of random access memory (RAVM) that may be used for purposes of temporarily holding data to be compared as is the recited role of RAVM in claim 1, it would be an obvious choice for Gavens's alternative data comparison (16:47-49). The background art supports such use. For example, Moshayedi (Ex. 1043) discloses dynamic random access memory. (Moshayedi, Fig. 1, ref. 106, ¶¶ 3-4, 28, 53-55, 67: DRAM.)

(Sechen ¶ 154): Further, Duann (Ex. 1034) discloses dynamic random access memory. (Duann page 6: Utilize DRAM as cache.) Thus, Gavens, in view of the knowledge of the POSITA, discloses claim 5.

F. Claim 6 Is Obvious Over Gavens, Including Incorporated references, in View of Knowledge of the POSITA.

1. [6Pre] The system of claim 1,

See Section X(A) for claim 1.

2. [6] wherein the random access volatile memory element is static random access memory.

(Sechen ¶ 156): Similar to claim 5, in view of a POSITA's understanding that static random access memory (SRAM) is common type of random access memory (RAVM) that may be used for purposes of temporarily holding data to be compared

as is the recited role of RAVM in claim 1, it would be an obvious choice for Gavens's alternative data comparison (16:47-49). Gavens itself discloses use of SRAM. (8:40-43: The entire disclosure of Paley '180 [Ex. 1051] is incorporated by reference. Paley '180 ¶¶ 423-425, 502-503, 506: SRAM.) Other uses with NAND flash systems were known, including Duann (Ex. 1034) for a hybrid SLC and MLC system. (Duann page 6: SRAM as cache.) The incorporated Embedded RAM Patents, published March 10, 2011, before the '546 priority date, specifically proposed using the "SRAM of the block" among 1,024 blocks of a commercial NAND flash module (Rao '452 [Ex. 1004] 2:19-39, Figs. 6a and 6b) to enhance speed of reading and writing. Thus, Gavens, in view of the knowledge of the POSITA, discloses claim 6.

G. Claim 7 Is Obvious Over Gavens, Including Incorporated references, in View of Knowledge of the POSITA and/or Colligan.

1. [7Pre] The system of claim 1,

See Section X(A) for claim 1.

2. [7] wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD).

(Sechen ¶ 158): A POSITA would understand that it is physically impossible for an SLC flash memory chip (much less an included "element") to include a hard disk drive, where the latter is orders of magnitude larger than a flash chip. If this and all the inconsistencies with claim 1 were ignored, including the antecedent of

being a part of an "SLC" module and changing the nature of an "SLC nonvolatile memory element," a POSITA would know that there are some useful combinations of flash and HDD such as disclosed in U.S. Patent No. 8,225,035 to Colligan (Ex. 1052) 2:33-36, 5:40-6:6, 7:67-8:2, and 8:23-25 (flash memory could supplement HDDs for more frequent writes) and the POSITA could **call** a combination of disk(s) 24 and SLC flash 28 of '546 Fig. 1 an "SLC nonvolatile memory element" to replace bad MLC blocks as physical address destinations. Thus, Gavens, in view of the knowledge of the POSITA, discloses claim 7 with an overstretched construction of "element."

(Sechen ¶ 159): For the reasons given above, claims 1-7 of the '546 patent are invalid [as obvious over Gavens in view of POSITA knowledge].

XI. THE PENDING LITIGATIONS IN THE WESTERN DISTRICT OF TEXAS DO NOT WARRANT DENYING INSTITUTION.

With eight Lifetime Patents based on verbal variations of claims to essentially the same two embodiments (in this case of the '546 patent, one embodiment) of a common specification restating known NAND flash operations and reserving application to admittedly fundamentally different technologies, post grant review – designed to catch recently issued patents on clear defects, not limited to the written art basis for later *inter partes* review – is the more appropriate place for review (for each patent in detail) compared to the District Court where those verbal variations can escape scrutiny because of the limitations of the District Court and the requested

jury. As demonstrated in the above-stated grounds (Sections VII, VIII, IX and X), the case against the '546 patent – which does not even recite the preferential writing to an SLC NAND flash module as known but restated in the specification – is compelling. Balancing of the six factors set forth by the Board in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential) does not warrant denying institution here. Rather, institution would best serve the interest in "system efficiency, fairness, and patent quality" (*id.* at 5), allowing due resolution of the substantial patentability questions (*id.* at 15).

As to *Fintiv* Factor 5, the petitioner and defendant in the parallel proceeding. Phison has acted to file this petition expeditiously within the nine months allowed from issuance, where it received first notice of Vervain's assertion in the Complaint filed March 8, 2024, and the First Amended Complaint filed May 13, 2024 (Ex. 1062). The District Court has not issued any substantive opinions regarding the scope or validity of the challenged claim. The parallel proceeding is in an early stage: the Court has not yet decided Phison's motion to dismiss (*see* Docket List [Ex. 1060] entries 12 and 24), the Petitioners have not otherwise answered, fact discovery has not yet proceeded beyond automatic disclosure and Phison's invalidity and subject-matter eligibility contentions were just filed on August 16, 2024, in accordance with the Scheduling Order (Ex. 1063). A *Markman* hearing is initially scheduled for December 5, 2024. (*Id.*) Thus, as to Factor 3, there has not been

overriding investment in the parallel proceeding; to the contrary, the requirements of the parallel proceeding will limit Markman construction to twelve terms between the parties for eight patents of verbal variations of the same specification. Thus, as to Factor 4, there is overlap, in the greater inclusiveness of the requested review as the District Court will not consider all the issues properly raised in this petition and others for review of the seven other variant patents that Petitioner may petition.

Factors 1 (stay) and 2 (proximity of trial dates) do not significantly weigh for or against instituting the requested PGR. Petitioner does not know if the District Court will stay the case if trial by this Board is instituted and the Court has *tentatively* set jury selection for December 15, 2025 (Scheduling Order [Ex. 1063] at 4).

Regarding the sixth factor (merits, other circumstances), the merits strongly weigh in favor of instituting trial as shown through the strength of the grounds in this petition. "Other circumstances" favor institution. As described at note 4 *supra*, there are separate suits by Patent Owner (following the same template) against Phison and a customer (Kingston Docket List [Ex. 1061]). This presents the complexity of eight patents with method and apparatus claims that Vervain asserts against multiple, sometimes competing products (that thus must be held confidential between the defendants) that implicate third-party actors who may be implicated in divided or indirect infringement as users who select the configuration or performance of the claimed system (see Section IX(E) on mixed product/process

claiming). Moreover, unlike Phison, its customer defendant in the other case has moved to dismiss for improper venue and to transfer (Kingston Docket List [Ex. 1061] entries 13 and 20) with attendant discovery and confidentiality proceedings (*id*. entries 15 and 16).

The interest of the public in cleaning away such verbal variants of questionable innovation in the Lifetime Patents are best served by the requested review. As with Factor 4, the Board may take notice that such litigation, if it and by the time it reaches trial, will have been drastically reduced in claims and theories asserted – this begins with the limitation of terms for construction for eight patents. A PGR trial, in contrast, allows a focus on resolving all challenged claims in a single patent, and may substantially simplify district court trial without the extensive district court discovery for which the America Invents Act offered this alternative before the Board. And, of course, Petitioner has shown its case to be compelling.

XII. CONCLUSION

Petitioner submits that for the reasons set forth above, supported by the declaration of Dr. Sechen and the Exhibits, it has been shown that more likely than

not, Challenged Claims 1-7 are invalid under all of 35 U.S.C. §§ 101, 112(a), 112(b), and 103 and should reviewed by the Board and canceled.

Date: August 27, 2024

Respectfully submitted,
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CERTIFICATION OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above-captioned Petition for Post Grant Review of U.S. Patent No. 11,573,546 (and accompanying exhibits), was served in its entirety on August 27, 2024, upon Patent Owner's correspondent of record via Priority Mail Express®:

Patent owner's correspondent
address of record for U.S. Patent No. 11,830,546

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CERTIFICATION OF WORD COUNT (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the attached Petition, including footnotes, but not the cover page, exhibit list, table of contents, mandatory notices, and certifications, contains 17,781 words, as measured by the Word Count function of Microsoft Word. This is less than the limit of 18,700 words as specified by 37 C.F.R. § 42.24(a)(ii).

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