

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PHISON ELECTRONICS CORPORATION,

Petitioner

v.

VERVAIN, LLC,

Patent Owner

Post-Grant Review Case No. PGR2025-00010

Patent 11,967,369

PETITION FOR POST-GRANT REVIEW OF

U.S. PATENT NO. 11,967,369

TABLE OF CONTENTS

I.	INTRODUCTION:	1
II.	MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1):	6
	A. REAL PARTY-IN-INTEREST UNDER 37 C.F.R. § 42.8(B)(1):	6
	B. RELATED MATTERS UNDER 37 C.F.R. § 42.8 (B)(2):	6
	C. LEAD AND BACK UP COUNSEL UNDER 37 C.F.R. § 42.8(B)(3):	6
	D. SERVICE INFORMATION UNDER 37 C.F.R. § 42.8(B)(4):	7
III.	ADDITIONAL REQUIREMENTS:	8
	A. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15:	8
	B. TIMING UNDER 37 C.F.R. § 42.202:	8
	C. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.204(A):	8
IV.	NAND FLASH TECHNOLOGY BACKGROUND	8
	A. CHARACTERISTIC NATURE OF NAND FLASH MEMORY	9
	B. CHARACTERISTIC NAND FLASH MEMORY MANAGEMENT	11
	C. INTRODUCTION OF MLC AND SLC FLASH	12
	D. KNOWN HYBRID USE OF SLC AND MLC NAND FLASH MODULES WITH STRATEGIES OF PREFERENTIAL MAPPING, WEAR LEVELING AND ERROR MANAGEMENT	14
V.	THE ‘369 PATENT: THE 2012 COMMON SPECIFICATION AND DIVERGENCE OF THE ‘300 CLAIMS	15
	A. THE COMMON SPECIFICATION RECITED AND RELIED ON A KNOWN HYBRID SYSTEM OF MLC AND SLC MODULES AND ITS OPERATION.	16
	B. THE FIRST THREE LIFETIME PATENTS ON OPERATION OF A KNOWN HYBRID MLC-SLC NAND FLASH MEMORY SYSTEM.	18

C.	2018 ‘300 PATENT ABSTRACTION OF THE DISCLOSED HYBRID MLC-SLC FLASH SYSTEM; ‘546 PARTIAL RESTORATION BUT FURTHER DEPARTURE ..	18
D.	INCONSISTENT RESTORATION IN ‘369 OF “MEMORY MODULE” AND RAVM AS A “MEMORY ELEMENT”	20
E.	THE CHALLENGED CLAIMS OF THE ‘369 PATENT:	21
F.	PERSON OF ORDINARY SKILL IN THE ART	27
VI.	37 C.F.R. § 42.204(B)(3): CLAIM CONSTRUCTION	27
VII.	GROUND 1: THE CHALLENGED CLAIMS CLAIM PATENT-INELIGIBLE SUBJECT MATTER UNDER 35 U.S.C. § 101 AS DIRECTED TO AN ABSTRACT IDEA, NAMELY, “MEMORY SPACE,” WITHOUT CLAIMING SUBSTANTIALLY MORE THAN ASPECTS OF THE OPERATION OF A GENERAL-PURPOSE COMPUTER.....	29
VIII.	GROUND 2: THE CHALLENGED CLAIMS LACK A WRITTEN DESCRIPTION DESCRIBING THE CLAIMED SUBJECT MATTER IN ACCORDANCE WITH 35 U.S.C. § 112(A).....	32
A.	THE CHALLENGED CLAIMS LIMITED BY “MEMORY SPACE” ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A).	33
B.	THE CHALLENGED CLAIMS LIMITED BY “MEMORY ELEMENT” ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A).	33
C.	THE CHALLENGED CLAIMS LIMITED BY “MAPPING . . . AS NECESSITATED BY THE SYSTEM TO MAXIMIZE LIFETIME” ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A).	34
D.	THE CHALLENGED CLAIMS RECITING RAVM, CONTROLLER MEMORY AND THEIR RESPECTIVE RELATIONSHIPS TO STORED AND RETAINED DATA ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A).	36
E.	THE CHALLENGED CLAIMS LIMITED BY “AT LEAST ONE MEMORY ELEMENT” ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A) AND FAIL TO RECITE A USEFUL SYSTEM FOR STORING DATA.	37
IX.	GROUND 3: THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(B).	39

A. THE CHALLENGED CLAIMS LIMITED BY “MEMORY SPACE” ARE INDEFINITE UNDER 35 U.S.C. § 112(B).	39
B. THE CHALLENGED CLAIMS LIMITED BY “MEMORY ELEMENT” ARE INDEFINITE UNDER 35 U.S.C. § 112(B).	40
C. THE CHALLENGED CLAIMS LIMITED BY “MAPPING . . . AS NECESSITATED BY THE SYSTEM TO MAXIMIZE LIFETIME” ARE INDEFINITE UNDER 35 U.S.C. § 112(B).	40
D. THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(B) FOR THEIR RECITATION OF A “CONTROLLER” LIMITED BY FUNCTIONS IN THE CLAIMS THAT ARE UNSUPPORTED BY STRUCTURE (PHYSICAL OR ALGORITHMIC) IN THE SPECIFICATION.	42
E. THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(B) BECAUSE THEY RECITE METHOD STEPS IN THE CONTEXT OF A CLAIM TO A SYSTEM.	44
F. THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(B) BECAUSE IT IS UNCERTAIN WHETHER AND WHEN THE RECITED COMPARISON TEST IS REQUIRED TO BE PERFORMED.	46
X. GROUND 4: CLAIMS 1-10 ARE OBVIOUS UNDER 35 U.S.C. § 103 OVER GAVENS IN VIEW OF POSITA KNOWLEDGE.	46
A. CLAIM 1 IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA.	47
1. [1a] [1a1] memory space containing logical and physical volatile memory space and nonvolatile memory space, [1a2] wherein the logical and physical nonvolatile memory space includes both multi-level cell (MLC) logical and physical memory space and single level cell (SLC) logical and physical memory space;	50
2. [1b] a bank of physical nonvolatile memory, including:	51
[1b1] a plurality of physical MLC memory modules, each including at least one physical MLC nonvolatile memory element having a physical address within the physical MLC nonvolatile memory space that can be mapped to a logical address in the MLC logical nonvolatile memory space, and	51

- [1b2] at least one SLC memory module including at least one physical SLC nonvolatile memory element having a physical address within the physical SLC nonvolatile memory space that can be mapped into the SLC logical nonvolatile memory space; 51
3. [1c] at least one random access volatile physical memory element that exists in the logical volatile memory space; 52
4. [1d] at least one controller [1d1] to operate physical memory elements and associated memory space for associated Write access operations to the physical memory elements and Read access operations from the physical memory elements, [1d2] the controller having a controller memory associated therewith for storing received data therein; 54
5. [1e] a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements; 55
6. [1f] [1f1] the controller controlling access of the physical MLC and SLC nonvolatile memory elements and the random access volatile physical memory elements for storage of the received data therein as stored data, [1f2] the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the physical MLC nonvolatile memory elements in an associated physical MLC memory module, [1f3] operable to store the received data in the given one of the physical MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile physical memory element as retained data associated with stored data; 59
7. [1g] the controller [1g1] performing a data integrity test on stored data in the given one of the physical MLC nonvolatile memory elements in the associated one of the physical MLC memory modules after the at least a Write access operation performed thereon by [1g2] reading the stored data to the controller memory and [1g3] comparing the stored data in the controller memory in the given one of the physical MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile physical memory element by the controller during the Write access operation; 61

8. [1h] wherein the address table maps logical addresses to physical addresses of the memory system, wherein the mapping is performed as necessitated by the memory system to maximize lifetime; and 62
9. [1i] wherein a failure of the data integrity test performed on the stored data by the controller results in [1i1] a remapping of logical address space to a different physical range of addresses in the physical address space and [1i2] transfer of data corresponding to the retained data to those remapped physical addresses in the physical address space from those physical addresses in the physical address space determined to have failed the data integrity test. 63
- B. CLAIM 2 TO A SOFTWARE FTL IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA.. 63**
- C. CLAIM 3, LIMITED TO RAVM, MLC OR SLC IN THE CONTROLLER, IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA..... 64**
- D. CLAIMS 4 AND 9, LIMITED TO THE NATURE OF MLC AND SLC MEMORY AS FLASH AND REMAPPING TO THE LATTER, ARE OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA. 65**
- E. CLAIMS 5 AND 6, LIMITED TO THE TYPE OF THE RAVM, ARE OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA. 67**
- F. CLAIM 7, LIMITED TO AN SLC ELEMENT INCLUDING AN HDD, IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA AND/OR COLLIGAN..... 69**
- G. CLAIM 8, LIMITED TO A CONTROLLER ASSOCIATED WITH AN EXTERNAL PROCESSOR, IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA AND/OR COLLIGAN.... 70**
- H. CLAIM 10, LIMITED TO AN FTL ASSOCIATED WITH THE MLC AND SLC MODULES, IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA AND/OR COLLIGAN.... 70**

XI. THE PENDING LITIGATIONS IN THE WESTERN DISTRICT OF TEXAS DO NOT WARRANT DENYING INSTITUTION.....	71
XII. CONCLUSION	75

TABLE OF AUTHORITIES

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Alice Corp. Pty. Ltd. v. CLS Bank International,

573 U.S. 208 (2014)-----30

Amgen Inc. v. Sanofi,

598 U.S. 594 (2023)-----32

Apple Inc. v. Fintiv, Inc.,

IPR2020-00019 (P.T.A.B. Mar. 20, 2020)----- 71, 72

Aristocrat Techs. Austl. Pty Ltd. v. Int’l Game Tech.,

521 F.3d 1328 (Fed. Cir. 2008)-----43

Bilski v. Kappos,

561 U.S. 593 (2010)-----30

Egenera, Inc. v. Cisco Sys.,

972 F.3d 1367 (Fed. Cir. 2020)-----42

Ergo Licensing, LLC v. CareFusion 303, Inc.,

673 F.3d 1361 (Fed. Cir. 2012) -----43

In re Nuijten,

500 F.3d 1346 (Fed. Cir. 1319))-----32

IPXL Holdings, LLC v. Amazon.com, Inc.,

430 F.3d 1377 (Fed. Cir. 2005)-----45

KSR Int’l Co. v. Teleflex Inc.,

550 U.S. 398 (2007)-----46

Mayo Collaborative Services v. Prometheus Laboratories, Inc.,

566 U.S. 66 (2012) -----30

Media Rights Techs., Inc. v. Capital One Fin. Corp.,

800 F.3d 1366 (Fed. Cir. 2015)-----43

Nautilus, Inc. v. Biosig Instruments,

572 U.S. 898 (2014)-----39

Rain Computing, Inc. v. Samsung Electronics America, Inc.,

989 F.3d 1002 (Fed. Cir. 2021)-----42

Rembrandt Data Technologies, LP v. AOL, LLC,

641 F.3d 1331 (Fed. Cir. 2011)-----46

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No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024)-----3, 73

Vervain, LLC v. Micron Technology, Inc., et al,

No. 6:21-cv-00487 (W.D. Tex. filed May 10, 2021) ----- 3

Vervain, LLC v. Phison Electronics Corp.,

No. 1:24-cv-00259 (W.D. Tex. filed March 8, 2024)----- 3, 6, 72, 73

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No. 6:21-cv-00488 (W.D. Tex. filed May 10, 2021) ----- 3

STATUTES

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35 U.S.C. § 112(a)----- passim

35 U.S.C. § 112(b) ----- passim

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37 C.F.R. § 42.8(a)(1)----- 6

37 C.F.R. § 42.8(b)(1) ----- 6

37 C.F.R. § 42.8(b)(2) ----- 6

37 C.F.R. § 42.8(b)(3) ----- 6

37 C.F.R. § 42.8(b)(4) ----- 7

37 C.F.R. § 42.10(b) ----- 7

37 C.F.R. § 42.15 ----- 8

37 C.F.R. § 42.24(a)(ii)-----77

37 C.F.R. § 42.100(b)-----27

37 C.F.R. § 42.202 ----- 8

Petition for Post-Grant Review of U.S. Patent No. 11,967,369

37 C.F.R. § 42.204(a) -----	8
37 C.F.R. § 42.204(b)(3) -----	27
37 C.F.R. § 42.204(b)(4) -----	29
37 C.F.R. § 42.204(b)(5) -----	29
Manual of Patent Examining Procedure (“MPEP”) § 2173.05(p)(II) -----	45

LIST OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,967,369, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1002	Declaration of Carl Sechen, Ph.D.
1003	U.S. Provisional Application No. 61/509,257, titled “IMPROVED LIFETIME MIXED LEVEL NAND FLASH SYSTEM” by Rao
1004	U.S. Patent No. 7,855,916, titled “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES,” to Rao
1005	U.S. Patent No. 8,891,298, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1006	Excerpts from prosecution history of ’298 patent
1007	U.S. Patent No. 9,196,385, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1008	<i>Intentionally omitted</i>
1009	U.S. Patent No. 9,997,240, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1010	<i>Intentionally omitted</i>
1011	U.S. Patent No. 10,950,300, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1012	Excerpts from prosecution history of ’300 patent
1013	U.S. Patent No. 11,830,546, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao

1014-1024	<i>Intentionally omitted</i>
1025	Excerpts from Rino Micheloni, et al., <i>INSIDE NAND FLASH MEMORIES</i> (Springer 2010)
1026	Excerpts from <i>NONVOLATILE MEMORY TECHNOLOGIES WITH EMPHASIS ON FLASH: A COMPREHENSIVE GUIDE TO UNDERSTANDING AND USING NVM DEVICES</i> (Joe E. Brewer & Manzur Gill eds. Wiley-IEEE Press 2008)
1027	Excerpts from <i>MICROSOFT COMPUTER DICTIONARY</i> (5 th ed. 2002)
1028-1029	<i>Intentionally omitted</i>
1030	Yu Cai et al., <i>Program Interference in MLC NAND Flash Memory: Characterization, Modeling and Mitigation</i> (IEEE 2013)
1031	Kang-Deog Suh et al., <i>A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme</i> , 30 IEEE J. Solid State Circuits 1149 (Nov. 1995)
1032	Eitan Yaakobi et al., <i>Error Characterization and Coding Schemes for Flash Memories</i> (2010 IEEE Globecom Workshops, Miami, FL at 1856-60)
1033	Evans, Chris, “Enterprise MLC: How flash vendors are boosting MLC write endurance” (June 3, 2011)
1034	Nelson Duann, <i>SLC & MLC Hybrid</i> (Silicon Motion Flash Memory Summit, Santa Clara, CA, Aug. 12, 2008)
1035	Ashish Jagmohan et. al., <i>Adaptive Endurance Coding for NAND Flash</i> (2010 IEEE Globecom Workshops, Miami, FL at 1841-45)
1036	Sungjin Lee et al., <i>FlexFS: A Flexible Flash File System for MLC NAND Flash Memory</i> (2009 USENIX Annual Technical Conference, San Diego, CA, June 14-19, 2009)

1037	Minyoung Sung & Kanghee Kim, <i>Asymmetric Flash Volume Management</i> , 58 <i>IEEE Transactions on Consumer Electronics</i> 455 (May 2012)
1038	Greg Atwood et al., Intel StrataFlash™ <i>Memory Technology Overview</i> , Intel Technology J. (Q4 1997)
1039	Taehee Cho et al., “A 3.3 V 1 Gb multi-level NAND flash memory with non-uniform threshold voltage distribution,” 2001 <i>IEEE International Solid-State Circuits Conference. Digest of Technical Papers</i> , ISSCC (Cat. No.01CH37177) (2001)
1040	U.S. Patent No. 6,456,528, titled for “SELECTIVE OPERATION OF A MULTI-STATE NON-VOLATILE MEMORY SYSTEM IN A BINARY MODE” to Chen
1041	U.S. Patent No. 8,078,794, titled “HYBRID SSD USING A COMBINATION OF SLC AND MLC FLASH MEMORY ARRAYS,” to Lee et al.
1042	U.S. Patent Appl. Pub. No. 2008/0140918, titled “HYBRID NON-VOLATILE SOLD STATE MEMORY SYSTEM” by Sutardja
1043	U.S. Patent Appl. Pub. No. 2009/0327591, titled “SLC-MLC COMINATION FLASH STORAGE,” by Moshayedi
1044	U.S. Patent Appl. Pub. No. 2010/0172179, titled “SPARE BLOCK MANAGEMENT OF NON-VOLATILE MEMORIES,” by Gorobets et al.
1045	U.S. Patent No. 8,634,240, titled “NON-VOLATILE MEMORY AND METHOD WITH ACCELERATED POST-WRITE READ TO MANAGE ERRORS,” to Gavens et al.
1046	U.S. Patent No. 8,806,301, titled “DATA WRITING METHOD FOR A FLASH MEMORY, AND CONTROLLER AND STORAGE SYSTEM USING THE SAME,” to Yu et al.

1047	U.S. Patent Appl. Pub. No. 2010/0115192, titled “WEAR LEVELING METHOD FOR NON-VOLATILE MEMORY DEVICE HAVNG SINGLE AND MULTI LEVEL MEMORY CELL BLOCKS,” by Lee
1048	U.S. Patent Appl. Pub. No. 2011/0271043, titled “SYSTEM AND METHOD FOR ALLOCATING AND USING SPARE BLOCKS IN A FLASH MEMORY,” to Segal et al.
1049	U.S. Patent Appl. Pub. No. 2011/0153912, titled “MAINTAINING UPDATES OF MULTI-LEVEL NON-VOLATILE MEMORY IN BINARY NON-VOLATILE MEMORY,” by Gorobets et al.
1050	U.S. Patent No. 5,930,167, titled “MULTI-STATE NON-VOLATILE FLASH MEMORY CAPABLE OF BEING ITS OWN TWO STATE WRITE CACHE,” to Lee et al.
1051	U.S. Patent Appl. Pub. No. 2010/0172180, titled “NON-VOLATILE MEMORY AND METHOD WITH WRITE CACHE PARTITIONING,” by Paley et al.
1052	U.S. Patent No. 8,225,035, titled “SYSTEMS AND METHODS FOR OPERATING A DISK DRIVE,” to Colligan
1053-1055	<i>Intentionally omitted</i>
1056	U.S. Patent App. Pub. No. 2009/0172267, “REFRESH METHOD OF A FLASH MEMORY,” by Oribe et al.
1057	U.S. Patent No. 5,936,971, titled “MULTI-STATE FLASH EEPROM SYSTEM WITH CACHE MEMORY, to Harari et al.
1058	PCT Pub. No. WO 03/027828, “METHOD OF WRITING DATA TO NON-VOLATILE MEMORY,” by Gorobets et al.
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1062	Gheorghe Samachisa et al., <i>A 128K Flash EEPROM Using Double-Polysilicon Technology</i> , SC-22 IEEE J. Solid State Circuits 676 (Oct. 1987)
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1068	Taehee Cho et al., <i>A Dual-Mode NAND Flash Memory: 1-Gb Multilevel and High-Performance 512-Mb Single Level Modes</i> , 36 IEEE J. Solid State Circuits 1700 (Nov. 2001)
1069	Ken Takeuchi, <i>A Multipage Cell Architecture for High-Speed Programming Multilevel NAND Flash Memories</i> , 33 IEEE J. Solid-State Circuits 1228 (Aug. 1998)
1070	Garth Goodson & Rahul Iyer, <i>Design Tradeoffs in a Flash Translation Layer</i> , HPCA [High Performance Computer Architecture] WEST 2010 Conference, Bangalore, India
1071-1079	<i>Intentionally omitted</i>

Petition for Post-Grant Review of U.S. Patent No. 11,967,369

1080	Docket list for <i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-00259 (W.D. Tex., filed March 8, 2024)
1081	Docket list for <i>Vervain, LLC v. Kingston Technology Company, Inc.</i> , No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024)
1082	First Amended Complaint, Doc. No. 9 in <i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-00259 (W.D. Tex.)
1083	Signed Agreed Scheduling Order, Doc. No. 16 in <i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-00259 (W.D. Tex.)

I. INTRODUCTION:

Phison Electronics Corporation (“Phison” or “Petitioner”) requests post-grant review (“PGR”) of claims 1-10 (the “Challenged Claims”) of U.S. Patent No. 11,967,369, entitled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” issued Apr. 23, 2024 (“the ‘369 patent”) (Ex. 1001), assigned to Vervain, LLC (“Vervain” or “Patent Owner”). The ‘369 patent was issued on the fifth continuation application¹ of a chain of continuations from U.S. Pat. Appl. No. 13/455,267, filed on April 25, 2012,² which claimed priority of U.S. Provisional App. No. 61/509,257, entitled “IMPROVED LIFETIME MIXED LEVEL NON-

¹ U.S. Appl. No. 18/387,546, which was filed Nov. 7, 2023.

² This application issued as U.S. Patent No. 8,891,298 (“the “298 patent,” Ex. 1005). It was followed by continuation U.S. Appl. No. 14/525,411, filed Oct. 28, 2014, issued as U.S. Patent No. 9,196,385 (the “385 patent,” Ex. 1007), by continuation U.S. Appl. No. 14/950,553, filed Nov. 24, 2015, issued as U.S. Patent No. 9,997,240 (the “240 patent,” Ex. 1009), by continuation U.S. Appl. No. 16/006,299, filed Jun. 12, 2018, issued as U.S. Patent No. 10,950,300 (the “300 patent,” Ex. 1011), and by U.S. Appl. No. 17/203,385, filed Mar. 16, 2021, issued as U.S. Patent No. 11,830,546 (the “546 patent,” Ex. 1013), leading to the ‘369 patent.

VOLATILE MEMORY SYSTEM,” filed on July 19, 2011 (“Provisional,” Ex. 1003) and incorporated by reference U.S. Patent No. 7,855,916 (“Rao ‘916,” Ex. 1004).^{3, 4}

A branch continuation application issued as U.S. Patent Nos. 11,854,612 (“the ‘612 patent”), and three later continuation applications so far issued as U.S. Patents Nos. 11,967,370, 12,119,054, and 12,136,455. The first eight of these ten “Lifetime Patents,” based on the same April 25, 2012, specification claiming July 19, 2011, priority, are currently asserted (First Amended Complaint, Ex. 1082, leave to amend granted, Ex. 1080 [Dec. 18, 2024, entry]) by Vervain against Phison in *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex. originally filed March

³ (U.S. Pat. Appl. No. 12/256,362 incorporated in the ‘369 patent [1:29-37], along with U.S. Pat. Appl. No. 12/915,177, both entitled, “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES,” the latter issued as U.S. Patent No. 8,194,452.)

⁴ Forty information disclosure statement (“IDS”) documents were filed with the April 25, 2012, ‘298 application (cited here by “IDS#_” in reference to their listing on the three IDSs filed that day [Ex. 1006 at 26-36]).

8, 2024).⁵ Petitioner has petitioned for reviews by this Board in six pending proceedings.⁶

⁵ All are asserted against a customer of Phison in *Vervain, LLC v. Kingston Technology Company, Inc., Kingston Digital, Inc., and Kingston Technology Corp.*, No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024). The first four patents were asserted previously in *Vervain, LLC v. Micron Technology, Inc.; Micron Semiconductor Products, Inc.; and Micron Technology Texas, LLC*, No. 6:21-cv-00487 (W.D. Tex. filed May 10, 2021, settled April 21, 2023) and *Vervain, LLC v. Western Digital Corp., et al*, No. 6:21-cv-00488 (W.D. Tex. filed May 10, 2021, settled Aug. 8, 2023). Micron petitioned this Board for *inter partes* review in *Micron Technology, Inc. v. Vervain, LLC*, IPR2021-001547 (‘298 patent), IPR2021-001548 (‘385 patent), IPR2021-001549 (‘240 patent), and IPR2021-001550 (‘300 patent), which were instituted on April 8 and 11, 2022, and terminated on April 4, 2023, on settlement after hearing but prior to final written decision.

⁶ *Phison Electronics Corp. v. Vervain, LLC*, PGR2024-00047 (‘546 patent, accorded filing date Aug. 27, 2024 [Paper No. 5]), PGR2024-00048 (‘612 patent accorded filing date Sept. 25, 2024 [Paper No. 5]), IPR2025-00212 (‘298 patent, accorded filing date Nov. 25, 2024 [Paper No. 5]), IPR2025-00213 (‘385 patent, filed Dec. 4,

This Petition demonstrates by a preponderance of the evidence that the Challenged Claims are unpatentable as one of ten patent groups that, by variations of words ambiguously or never used in the common specification, lay claim to a functionally described, known by 2011 “data integrity test” operation for hybrid “MLC” and “SLC” NAND flash memory systems established a decade earlier. Although the first three Lifetime Patents claimed this operation and a variation of known wear leveling as an adaptation of a “controller” for a system of known, distinct MLC and SLC “modules,” beginning in 2018, the remaining Lifetime Patents, on the same 2012 functional description, claimed abstract “memory spaces” with “MLC” and “SLC” “memory elements” operated with the “data integrity test.” In the ‘300 prosecution, a previously undistinguished, but NAND-flash common “random access volatile memory” (“RAVM”) was elevated then demoted from an “element” in the “memory space” (which has no practical function). The ‘546 patent re-elevated the RAVM and added the also previously undistinguished, but NAND-flash common “controller memory” – but not to the “memory space.” The subject ‘369 patent added to the verbal thicket by reciting new subdivisions of “logical and physical” “memory spaces.” None of these variations have any technological import

2024), IPR2025-00214 (‘240 patent, filed Dec. 6, 2024), and IPR2025-00215 (‘300 patent, filed Dec. 17, 2024).

– as they may not, in view of the 2012 common “support” of a two-paragraph functional (and ambiguous) description of “a method for utilizing a NAND flash memory system.” They only serve to provide a veil for the verbal legerdemain for procurement and assertion of now ten Lifetime Patents on the same inadequate, functional description of a then known NAND flash error management operation.

The only independent claim 1 recites the abstract “memory space” that provides no technical benefit. It claims the NAND-flash “mapping” operation of that space with “MLC,” “SLC” and RAVM “elements” by which, in words with ambiguous reference, the “controller” (with NAND-common Flash Translation Layer [“FTL”] software) writes data to MLC as “stored data” and “reads” the “stored data” to the “controller memory” and compares it to the original, “retained data” (in RAVM) in a “data integrity test,” which if failed, results in “remapping” and “transferring” the retained data to “a different physical range of addresses in the physical address space.” All the while or at some unspecified time, “the mapping is performed as necessitated by the system to maximize lifetime.” In addition to the impermissible patenting of the abstract idea of “memory space” (Ground 1), these terms (and others in the dependent claims) themselves and in recited combination invalidate the Challenged Claims for lack of support and/or operability (Ground 2) and for indefiniteness (Ground 3). Were the Challenged Claims to survive these challenges, to the extent understood by a POSITA, they are known prior art,

exemplified by U.S. Patent No. 8,634,240 to Gavens et al. (“Gavens,” Ex. 1045) and its incorporated references, or obvious in view of the knowledge of the POSITA (Ground 4). Post-Grant Review of the Challenged Claims is eminently appropriate for stopping proliferation of bad patents such as the ‘369 patent’s unsupported abstraction of its own misstatement of well-known NAND flash technology.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1):

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1):

Petitioner Phison Electronics Corporation is the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8 (b)(2):

As set forth further at note 5 *supra*, the ‘369 patent (along with seven other patents based on the same specification) is currently asserted by Vervain against Phison and its customer (separately) in the Western District of Texas. In the Phison case a claim construction hearing (on twelve terms proposed by Phison and its customer) is tentatively scheduled for January 9, 2025, and jury selection tentatively scheduled for December 15, 2025 (*Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259, Doc. No. 16 (W.D. Tex. July 15, 2024) (Ex. 1063). Resolution of this proceeding may simplify that litigation and promote settlement.

C. Lead and Back Up Counsel Under 37 C.F.R. § 42.8(b)(3):

Pursuant to 37 C.F.R. § 42.8(b)(3), lead counsel for this Petition is Hsuanyeh Chang, PhD (Reg. No. 73,431) and back-up counsel are Stephen Y. Chow (Reg. No.

31,338), Douglas E. Chin (Reg. No. 66,713), and Peter Yi (Reg. No. 61,790).

Pursuant to 37 C.F.R. § 42.10(b), Petitioner has filed a power of attorney designating the above-identified counsel.

D. Service Information Under 37 C.F.R. § 42.8(b)(4):

Pursuant to 37 C.F.R. § 42.8(b)(4) service information for the Petition is as follows:

Lead Counsel	Back-Up Counsel
Hsuanyeh Chang, PhD Reg. No. 73,431 HSUANYEH LAW GROUP PC 11 Beacon Street, Suite 900 Boston MA 02108 (617) 886-9088 (Phone) hsuanyeh@hsuanyeh.com	Stephen Y. Chow Reg. No. 31,338 HSUANYEH LAW GROUP PC 11 Beacon Street, Suite 900 Boston MA 02108 (617) 886-9288 (Phone) Stephen.Y.Chow@hsuanyeh.com
	Douglas E. Chin Reg. No. 66,713 HSUANYEH LAW GROUP PC 11 Beacon Street, Suite 900 Boston MA 02108 (617) 886-9488 (Phone) Doug.Chin@hsuanyeh.com
	Peter Yi Reg. No. 61,790 HSUANYEH LAW GROUP PC 11 Beacon Street, Suite 900 Boston MA 02108 (617) 886-9188 (Phone) Peter.Yi@hsuanyeh.com

Petitioner consents to electronic service at the above-identified email addresses.

III. ADDITIONAL REQUIREMENTS:

A. Payment of Fees Under 37 C.F.R. § 42.15:

The required fees are submitted herewith from Deposit Account No. 50-6685 (Order No. 1280-0015). If any additional fees are due at any time during this proceeding, the Office is authorized to charge such fees to Deposit Account No. Deposit Account No. 50-6685 (Order No. 1280-0015).

B. Timing Under 37 C.F.R. § 42.202:

The present petition for post-grant review is filed within nine months after the grant of the ‘369 patent.

C. Grounds for Standing Under 37 C.F.R. § 42.204(a):

Petitioner certifies that: (1) the ‘369 patent is eligible for post-grant review; and (2) Petitioner is not barred or estopped from requesting post-grant review of any claims of the ‘369 patent on the grounds identified herein.

IV. NAND FLASH TECHNOLOGY BACKGROUND

Petitioner’s expert, Dr. Carl Sechen, has provided in his declaration (“Sechen,” Ex. 1002) a deep analysis of the state of NAND flash technology relied on by the Lifetime Patents (Sechen Section V), the embodiments admitted or advanced in the common specification (Sechen Section VII), the evolution of the

Lifetime Patent claims from NAND flash technology to abstractions (Sechen Section VIII), specific defects in the ‘369 claims (Sechen Section IX), and the obviousness of those claims over the Gavens (Ex. 1045) in view of the POSITA’s knowledge of the art (Sechen Section X). Following is a summary of the NAND flash memory technology underlying the Challenged Claims to a “system for storing data,” based on an abstracted, but known MLC and SLC NAND flash modules and a “controller” coupled to them and maintaining known NAND flash address mapping and “adapted” to perform optional, also known, error management and wear leveling.

A. Characteristic Nature of NAND Flash Memory

A **NAND flash cell** is type of transistor with a floating gate that can retain electrical charges associated with “threshold voltages” that, applied to a control gate, allows conduction of electrical current from drain to source. (Sechen ¶¶ 26 [Fig. 2.1(a)], 40 [Figures 6 and 7 from Atwood {Ex. 1038}] and 41.)

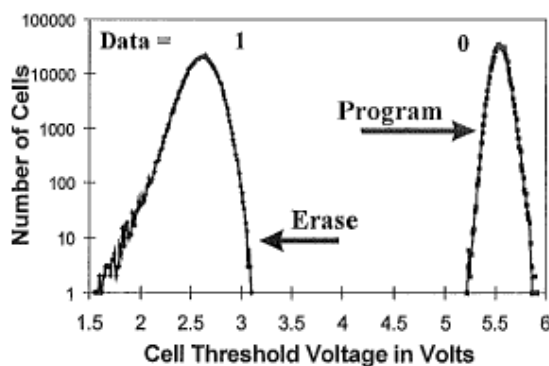


Figure 6: Single bit/cell array threshold voltage histogram

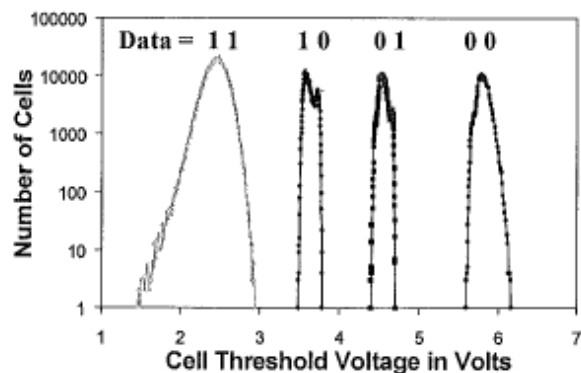


Figure 7: Two bit/cell array threshold voltage histogram

These threshold voltages may be chosen to represent information to be stored, in “classic” NAND memory operation, using two threshold voltage levels (Figure 6), the lower level to represent (“store”) a logical “1” and the higher level to store a “0” of one bit of digital computer data. (*Id.*) The same storage cell can use four threshold voltage levels (Figure 7) to represent four values corresponding to two bits of binary computer data (which in NAND memory operation is sourced from two distinct groups, “pages,” of logical data). (*Id.*) An n power of two (2^n : eight, sixteen, . . .) threshold levels may be used in NAND flash operation to represent corresponding bits of n pages (*id.* ¶¶ 40 and 42-43). But a cell or group of cells do not constitute “memory,” which requires circuitry for selecting, programming (writing) and reading the cell or group of cells (*id.* ¶¶ 26 and 29)

To form **NAND flash memory**, storage cells are hard wired in strings (bit-line “columns”) and word-line “rows” forming “**pages**” each typically 2K storage cells **programmed** (written) **page by page**. (*Id.* ¶ 26.) NAND flash is so characterized by wiring of its storage cells in typically 64-page “**blocks**,” individually **erased in unison** to prepare for writing of new pages (*id.* ¶¶ 28-30). Unlike magnetic hard disk drives and other technologies that allow “write in place” of data at a physical location assigned to prior versions, in NAND flash programming, an update to stored data must be written to a physical location that is erased in preparation (“erase before write”); erasure, a much longer process than

writing, is done in the background, when there are no user-requested read or write operations. (*Id.*) To maintain logical visibility to the user of a NAND flash memory device such as a Solid State Drive (“SSD”) (shown at Sechen ¶ 30), there are maintained and updated tables in or available to a **NAND flash device controller**, shown as a hardware module or chip on an SSD circuit board (*id.*) to “map” logical locations to physical locations in the NAND flash memory array (“**L2P mapping**”), which update for each data write (*id.* ¶¶ 30 and 31). The physical instances of NAND flash pages and blocks determine the **Physical Block** Addresses (“PBA”) mapped from the construct of **Logical Block** Addresses (“LBA”). (*Id.* ¶¶ 32-34.) This mapping and remapping is performed with the software **Flash Translation Layer** (“FTL”) of the controller with **address tables** in **controller RAM** and **backup** in the flash memory. (*Id.* ¶¶ 31-38.) The physical reading, writing and erasing of NAND flash cells is performed by circuitry in a NAND flash memory module, shown in multiples in Sechen paragraphs 29 and 30 (“flash,” “flash memory” or just “NAND”) on a board, along with a block diagram identifying reading, writing and erasing functions (*id.* ¶ 29). A POSITA would understand this to be a **NAND flash memory or module**. (*Id.* ¶ 30.)

B. Characteristic NAND Flash Memory Management

Sechen paragraphs 34-38 outline common processes in the use of NAND flash memory. These include **bad block management** and **garbage collection** to make

available adequate numbers of blocks for new writes without unnecessary, time-consuming erasures. Typically, “hot” data, *i.e.*, frequently updated (such as system data, and “cold” (not-“hot”) data are clustered in respective physical blocks in order to facilitate efficient (fewer erase-and-re-writes) collecting of “valid” (un-updated) stored data and freeing up the blocks they otherwise occupy. Related “**wear leveling**” processes (“dynamic” at the time of writing and “static” in the background) even out write and erase stresses on NAND memory blocks – which have limited expected “endurance” (“lifetime”) – aiming to avoid premature failure or retirement of enough blocks that would compromise system use. (Sechen ¶ 39 [**system lifetime**].)

C. Introduction of MLC and SLC Flash

Multi-level cell (MLC) NAND flash, developed in 1992-97, as described in Atwood (Ex. 1038), was the use of the NAND storage cell with four threshold voltage levels to represent two bits of information. (Sechen ¶¶ 40-41.) The first known use of the term “SLC” was in a 2001 article that called the established technology “**single-level program cell NAND flash (SLC)**” and compared it with then new MLC. (Ex. 1039, Sechen ¶ 42.) Although the terms have been shortened over the years, a POSITA would understand that “MLC” refers to the use of NAND storage cells, each storing two bits written in two passes – a “lower” (least significant bit, “LSB”) logical page and then a distinct “upper” (most significant bit, “MSB”)

logical page. (*Id.* ¶ 43.) That is, MLC flash memory allows writing **two logical data pages into one physical page of memory**. As reviewed at Sechen paragraph 43 (particularly Sechen note 17), the programming of MLC memory is more complex and stressful than SLC because of MLC's narrower window for distinct threshold charges and its multiple passes of writing; also, a page-wide set of latches (**page buffer**) is required for reading *each* level of logical page programming. Thus, a POSITA would understand that different circuitry is required for **MLC NAND flash memory** than for **SLC NAND flash memory**, and that **SLC NAND flash memory is incapable of storing more than one logical data page in one physical page of memory**.

Two-state operation of MLC (later called **pseudo-SLC**) was disclosed by 2002. (Sechen ¶ 49; U.S. Patent No. 6,456,528 to Chen for "Selective Operation of a Multi-State Non-Volatile Memory System in a Binary Mode" ["Chen '528," Ex. 1040] [one-bit *mode* of writing only one logical data page into one MLC physical page of memory]). This mode of MLC use, applying the MLC memory circuitry and pulsed/phased writing, has inferior performance and endurance relative to "real" SLC. A SanDisk suite of patents (incorporating by reference among others, Chen '528) disclosed lower-density (pSLC) *mode* use of MLC modules through partitioning and configuration for multiple reasons, including faster processing for caching writes and error management (*e.g.*, Gavens [Ex. 1045]; U.S. Patent No.

8,806,301 to Yu et al., published Apr. 14, 2011 [Ex. 1046], explained at Sechen ¶¶ 53-56).

D. Known Hybrid Use of SLC and MLC NAND Flash Modules with Strategies of Preferential Mapping, Wear Leveling and Error Management

Because of the compression of its threshold levels and its multiple passes of writing, MLC NAND flash was well-known to wear more quickly (have less “endurance”) and perform more slowly than SLC NAND flash. (Sechen ¶¶ 40-42.) Thus, it was proposed as early as 2008 to use hybrid systems of **SLC modules** and **MLC modules** in which more **frequently written/updated data**, such as system data, user directories, and certain user files, would be written **preferentially to** a more robust **SLC module** while less frequently updated data would be written to the MLC module. (Sechen ¶ 46; Nelson Duann, SLC & MLC Hybrid (Silicon Motion Flash Memory Summit, Santa Clara, CA, Aug. 12, 2008) [“Duann,” Ex. 1034]; U.S. Patent No. 8,078,794 to Lee et al., published Sept. 4, 2008 [“Lee ‘794,” Ex. 1041].)

This **SLC module preference** was applied in 2008-09 to a variety of **wear leveling** techniques to avoid premature failure of a system by some components reaching their endurance limits before others. (Sechen ¶¶ 47-48 and 58-60; *e.g.*, Sutardja [Ex. 1042]; Moshayedi [Ex. 1043].)

Additional tools or techniques were known in the art before the priority date to avoid premature failure by applying **error management near the end of life of**

the system, with **preferential writing to SLC** upon failure of some “data integrity test” of an MLC location. (Sechen ¶¶ 53-56 and 58-61, *e.g.*, Gavens [Ex. 1045].)

The availability to the POSITA of these **preferential writing to SLC** techniques to avoid premature failure makes obvious the base claim 1 of the ‘369 patent. Nothing disclosed in the ‘369 patent specification was new relative to the 2011 state of the art of NAND flash technology; to the contrary, the disclosed embodiments would not be enabled without the understood (by a POSITA) physical operation of the distinctly referenced SLC and MLC modules as SLC NAND flash modules and MLC NAND flash modules with supporting circuitry at least for their distinct organizations, reading, writing and erasing.

V. THE ‘369 PATENT: The 2012 Common Specification and Divergence of the ‘300 Claims

The 2012 common specification of the Lifetime Patents discloses no more technology than known, hybrid MLC and SLC NAND flash memory module systems with two proposed features of operation, variants of common flash wear leveling and error management. The first three patents claimed that known system with those operational features and were issued based on the perceived novelty of their recited “transfer” of data to the SLC module following “failure” of their recited “data integrity test.” In the 2018 application resulting in the ‘300 patent, the same 2012 system was rewritten for a “memory space” abstraction mentioned in the

specification only as quantity of storage, while elevating to a claim element an RAVM used in various flash memory roles and not clearly identified in the common specification, much less as an advance in the art. In the next, '546 patent, common “controller memory,” ambiguously referenced in the common specification, was introduced to the claim language. The next, subject '369 patent divided “memory space” into “logical and physical” memory space, not adding but detracting from clarity of physical operation, with its only import as a verbal smokescreen for claims to the known data integrity test.

A. The Common Specification Recited and Relied on a Known Hybrid System of MLC and SLC Modules and Its Operation.

The core disclosed system of known MLC NAND flash and SLC NAND flash modules is described multiple times in the specification. (*E.g.*, 4:15-20, 5:6-10, 6:66-7:5; Sechen ¶ 69.) Fig. 4 shows a physical memory device module including two banks each including 8+ **MLC flash memory modules** and 2+ **SLC NAND flash memory modules**). A controller “coupled” to the MLC and SLC modules performs L2P/FTL functions essential for NAND flash operation and also performs common wear leveling. (3:1-33 [BACKGROUND FTL/wear leveling]; *compare* Sechen ¶¶ 34-36.) Only two features are proposed in the DETAILED DESCRIPTION, for “increasing the reliability and lifetime of a NAND flash storage system” (5:1-7:31).

The first, “data integrity test” feature is shown as the NAND flash method steps of Figs. 3A and 3B, explained in the text (6:11-48). Dr. Sechen identifies (§ 71) substantial ambiguities and inconsistencies even as to the disclosed comparison of “**stored data**” and “**retained data.**” The specification text is unclear as to whether addresses are compared or data written to those addresses (Sechen note 39) and what “**device controller memory**” is referenced at different steps (Sechen note 38). The only RAM mentioned is “**DRAM**” where data to be written to flash is held (6:14-16); “DRAM 20” of generic Fig. 1 is explained as “controlled” by the controller 14 among other possible memories such as rotating disk or the distinct MLC and SLC **modules** (5:30-48). But “**volatile memory**” is admitted in the ‘369 BACKGROUND for “**buffering, caching**” (3:61-62).

The second feature is functionally stated in two sentences, the first describing what wear leveling by “**allocat[ing]** ‘hot’ blocks i.e., those **blocks** that receive frequent writes, into the **SLC NAND flash memory module 28**, while allocating ‘cold’ blocks; i.e., those blocks that only receive infrequent writes, into the MLC NAND flash memory module 26.” (6:49-61 [emphasis added].) A second sentence suggests implementation by “**maintain[ing]** a count of those blocks that are accessed (written to) most frequently” and “**transfer[ring]** the contents of those blocks into the SLC NAND flash memory module 28” – “on a periodic basis” such as “every 10,000 writes.” (6:55-61 [emphasis added].) Multiple ambiguities (Sechen § 73),

most importantly whether the referenced blocks are the **physical blocks** individually erased in flash memory **or logical blocks** mapped to them in flash operation.

B. The First Three Lifetime Patents on Operation of a Known Hybrid MLC-SLC NAND Flash Memory System

The first three Lifetime Patents claimed the known, physical hybrid flash system of (1) an **MLC memory module** ('298 [Ex. 1005] 7:31-32, '385 [Ex. 1007] 7:14-15, '240 [Ex. 1009] 7:31-32), (2) a distinct **SLC memory module** ('298 7:33-34, '385 7:16-17, '240 7:33-34) and (3) a **controller/FTL** "coupled" to the **modules** performing *ordinary L2P address mapping* ('298 7:13-25, '385 7:19-28, '240 7:35-46), **adding operational features** of a **data integrity test** ('298 7:26-32, '385 7:29-36, '240 7:47-54) and **wear leveling** ('298 8:1-9, '385 7:41-8:4, '240 7:55-87). The only limitation not found in the prior art multi-modal NAND flash system of U.S. Patent Appl. Pub. No. 2010/0172179 ("Gorobets '179," Ex. 1044) was the recited wear-leveling "**transfer**" of the contents of "blocks" not clearly logical or physical (Sechen ¶¶ 75-78).

C. 2018 '300 Patent Abstraction of the Disclosed Hybrid MLC-SLC Flash System; '546 Partial Restoration but Further Departure

On June 12, 2018 – six years after the April 25, 2012, filing of the specification common to all the Lifetime Patents – the application resulting in the '300 patent was filed with its original independent claim rewriting the base hybrid

MLC-SLC NAND flash memory system into an unsupported and vague mix of “memory spaces” and “memory elements,” including “at least one random access volatile memory element” (June 12, 2018, [‘300] Application at 14 [Ex. 1012 at 14]), although the only RAVM mentioned in the common specification relating to any suggested invention was the “DRAM” where host data is received for the disclosed data integrity test (6:14-16) and “volatile memory” in the BACKGROUND art for “caching, buffering” (3:61-62). As explained at paragraphs 80 and 81 of the Sechen declaration, the new terms and recitations had no basis in the specification and made no contribution to structural clarity (notice), but to the contrary, appeared intentionally vague to cover technology other than the known and relied-upon (for operational structure) system of MLC and SLC NAND flash modules; moreover there was no claim to the wear leveling and “transfer” that distinguished Gorobets ‘179 (Sechen ¶ 81). Confronted therefore with continuing rejection over the Gorobets ‘179 multi-modal NAND flash system, amendments were made that altered connections between the claim elements. (Sechen ¶¶ 82, 83.) In partial resolution of the vagueness of “memory space,” the claims were amended so that the MLC and SLC “memory elements” were “mapped” to their respective “memory spaces,” that, with the recited controller mapping, made clear that those “memory spaces” were logical addresses or “logical address space,” although the RAVM became no longer an “element” mapped to its “volatile memory space” (Sechen note

49, discussing Oct. 8, 2020, [‘300] Amendment at 2-5 [Ex. 1012 at 71-74). Ultimately, the ‘300 claims were allowed after an argument that the asserted art did not disclose enough “conventional cache” to perform the comparison of the recited data integrity test. (Sechen ¶ 83, quoting the argument at Oct. 8, 2020, [‘300] Amendment at 9 [Ex. 1012 at 78] and reciting the Examiner’s reliance at Jan. 27, 2021, [‘300] Notice of Allowability at 2 [Ex. 1012 at 86].) But no such departure from the conventional NAND flash was suggested, much less disclosed in the specification or limited in the claims.

D. Inconsistent Restoration in ‘369 of “Memory Module” and RAVM as a “Memory Element”

In the ‘546 patent, followed by the ‘369 patent, the terms “MLC memory module” and “SLC memory module” returned as part of a “bank of nonvolatile memory” (‘546 7:37-41, ‘369 7:41-52), but with each module only requiring one undefined “element” – in contrast to the pre-2018 patents requiring at least a flash “individually erasable block” (Sechen ¶ 84). The ‘546 patent also introduced, and the ‘369 patent retained, recitation of a “controller memory” in various roles, including, after receiving and “transferring” data to MLC, “reading the stored data [in MLC] to the controller memory and comparing the stored data in the controller memory in the [MLC] to the retained data that was associated with the stored data in the [RAVM] by the controller” (‘546 8:15-21 [emphasis added], ‘369 8:19-24)).

Although the controller was recited as “operable” to “retain such received data” in RAVM (*e.g.*, ‘369 8:9-13), no such operation, which would involve multiple steps, was disclosed – compared to the DETAILED DESCRIPTION appearance that such retained data was left in the controller memory after incoming data was combined with valid existing data and written to MLC. (Sechen ¶ 84). The ’369 memory space is further divided into “logical and physical volatile memory space” (7:34-35), which pointlessly and confusingly conflicts with a reasonable construction in the ‘300 patent that the MLC and SLC nonvolatile elements mapped to the logical address space of the “memory space” (Sechen note 49). And the RAVM is restored to a “physical element” which paradoxically “exists in the logical volatile memory space” (7:53-55) in contrast to “controller memory” not a part of “memory space” at all. (Sechen ¶ 84.)

E. The Challenged Claims of the ‘369 Patent:

Challenged claim 1 of the ‘546 patent is its only independent claim:

1. A system for storing data comprising:

[1a] [1a1] memory space containing logical and physical volatile memory space and nonvolatile memory space, [1a2] wherein the logical and physical nonvolatile memory space includes both multi-level cell (MLC) logical and physical memory space and single level cell (SLC) logical and physical memory space;

[1b] a bank of nonvolatile memory, including:

- [1b1] a plurality of physical MLC memory modules, each including at least one physical MLC nonvolatile memory element having a physical address within the physical MLC nonvolatile memory space that can be mapped to a logical address in the MLC logical nonvolatile memory space, and
- [1b2] at least one SLC memory module including at least one physical SLC nonvolatile memory element having a physical address within the physical SLC nonvolatile memory space that can be mapped into the SLC logical nonvolatile memory space;
- [1c] at least one random access volatile physical memory element that exists in the logical volatile memory space;
- [1d] at least one controller [1d1] to operate physical memory elements and associated memory space for associated Write access operations to the physical memory elements and Read access operations from the physical memory elements, [1d2] the controller having a controller memory associated therewith for storing received data therein;
- [1e] a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the physical memory elements;
- [1f] [1f1] the controller controlling access of the physical MLC and SLC nonvolatile memory elements and the random access volatile physical memory elements for storage of the received

data therein as stored data, [1f2] the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the physical MLC nonvolatile memory elements in an associated physical MLC memory module, [1f3] operable to store the received data in the given one of the physical MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile physical memory element as retained data associated with stored data;

[1g] the controller [1g1] performing a data integrity test on stored data in the given one of the physical MLC nonvolatile memory elements in the associated one of the physical MLC memory modules after the at least a Write access operation performed thereon by [1g2] reading the stored data to the controller memory and [1g3] comparing the stored data in the controller memory in the given one of the physical MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile physical memory element by the controller during the Write access operation;

[1h] wherein the address table maps logical addresses to physical addresses of the memory system, wherein the mapping is performed as necessitated by the memory system to maximize lifetime; and

[1i] wherein a failure of the data integrity test performed on the stored data by the controller results [1i1] in a remapping of logical address space to a different physical range of addresses in the

physical address space and [1i2] transfer of data corresponding to the retained data to those remapped physical addresses in the physical address space from those physical addresses in the physical address space determined to have failed the data integrity test.

(7:34-8:36 [emphasis and labels added].) The claim retains from the ‘300 patent the unsupported abstraction of “memory space” and though reciting physical MLC and SLC modules, recited new and inconsistent components of and relations within the technologically inconsequential “memory space” (Sechen ¶ 84). Claim 1 also retained the ‘300 patent indefinite “mapping . . . to maximize lifetime,” while not reciting any preferential mapping to the SLC module, but only to “a different physical range of addresses.” (Sechen ¶ 81.) The other claims depend from claim 1:

Claim 2 limits the “FTL” to a software “module” or firmware “module.” Neither the abstract “controller” nor the FTL were given any structure as a “module” in the ‘369 specification as were the SLC and MLC hardware modules.

Claim 3 requires that one of the RAVM or the MLC and SLC “memory elements” is embedded in the controller. No memory other than “controller memory” is disclosed in the ‘369 specification as so embedded, so it could be one of “at least one RAVM.”

Claim 4 requires that “the physical MLC and SLC nonvolatile memory elements” to comprise flash memory, which those terms imply in any case.

Claims 5 and 6 require respectively the RAVM to be dynamic random access memory (“DRAM”) and static random access memory (“SRAM”), both obvious choices for the caching function assigned to RAVM.

Claim 7 requires that an “SLC nonvolatile memory element includes a hard disk drive (HDD), which is nonsensical.

Claim 8 requires at least one controller to be “associated” with a processor external to the memory system, which is generally how a memory system is used..

Claim 9 requires that “remapped” [after failure of the data integrity test] physical addresses are to the SLC module.

Claim 10 requires that the FTL is “associated” with the MLC and SLC modules.

In view of the literal claims and disclosure of the ‘369 patent, the accompanying prior art references and supporting declaration of Dr. Sachin (Ex. 1002), Petitioner respectfully requests cancellation of the Challenged Claims as summarized in the following table.

Grounds	Exhibits
Ground 1: Claims 1-10 are unpatentable under 35 U.S.C. § 101 as directed at the abstract idea of a “memory space.”	1001, 1002

Ground 2: Claims 1-10 are invalid under 35 U.S.C. § 112(a) because ‘369 patent specification fails to provide enabling written description, much less demonstrate the possession of any invention claimed.	1001, 1002, 1004
Ground 3: Claims 1-10 are invalid under 35 U.S.C. § 112(b) for failing to particularly point out and distinctly claim the subject matter which the inventor regards as his or her invention, including because of failure to disclose structure for controller and FTL functions, recitation of method steps in the system claims, and undefined terms and inconsistent recitation.	1001, 1002, 1034, 1041, 1042, 1043, 1045
Ground 4: Claims 1-7 are unpatentable under U.S.C. § 103 as obvious over Gavens and incorporated disclosures in view of a POSITA’s knowledge of NAND flash technology.	1001, 1002, 1003, 1034, 1040, 1041, 1042, 1043, 1045, 1049, 1050, 1051, 1052, 1056, 1057, 1058

F. Person of Ordinary Skill in the Art

A person of ordinary skill in the art at the time of the claimed inventions would have a bachelor's degree in computer engineering, electrical engineering, computer science, or a closely related field, along with at least two years of experience in the design, development, implementation, or management of memory devices and systems. A person with an advanced degree in a relevant field, such as computer or electrical engineering, would require less experience in the development and use of memory devices and systems. As is common, one could obtain equivalent knowledge and perspective from other life experiences as well. (Sechen ¶¶ 63 and 64).

VI. 37 C.F.R. § 42.204(b)(3): CLAIM CONSTRUCTION

Under 37 C.F.R. § 42.200(b), claims in a post-grant review proceeding are construed using the same standard as that in a civil action. This includes “construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent,” *id.* The standard for claim construction is set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

MLC and SLC memory/module/element have the following meanings based on POSITA understanding (Sections IV(C)-(D) and V(A)-(B) *supra*: Sechen ¶¶ 42-50, 66-69, 75-78, 80, 84 and 87), especially because of Dr. Rao's specific

choice of using the term “SLC module” and not “SLC mode” in the DETAILED DESCRIPTION, given his disclosure of a SLC chip in the incorporated Rao ‘916 (Ex. 1004, Figs. 6 and 7) and the distinct reference to “SLC” mode in the documents submitted with the 2012 specification:⁷

- **“MLC memory modules”** means “modules comprising MLC non-volatile memory” *where*

“MLC non-volatile memory” means “**non-volatile memory cells arranged with circuitry *capable* of storing multiple logical pages in a single physical page of cells**” and

- **“SLC memory module”** means “module comprising SLC non-volatile memory” *where*

“SLC non-volatile memory” means “**non-volatile memory cells arranged with circuitry *incapable* of storing multiple logical pages in a single physical page of cells**”

When MLC first appeared, distinguishing the established two-threshold-voltage level memory as “SLC,” “level” referred to its single “level” of memory programming (Sechen ¶¶ 40-43): a cell cannot be a “memory” without the means for writing and retrieving, namely the circuitry (Sechen ¶ 26, note 6), where **SLC memory** does not have the circuitry to store two pages in one page of cells (‘369

⁷ (E.g., Sechen notes 14, 15 & 19, Ex. 1068 (IDS#11), Ex. 1069 (IDS#8)).

2:59-64 [SLC can only be written once], Sechen ¶¶ 43, 49, 87 and notes 17 & 51). “Module” is a complete hardware component, interchangeable with a chip (Sechen ¶ 30, note 8). In the ‘369 claims, the terms “MLC” and “SLC” also modify “elements.” Because of the known and disclosed “page architecture” of NAND flash (Rao ‘916 1:39-58, Fig. 9; Sechen note 34, ¶ 87), to the extent that those terms are not found indefinite or inoperative, “MLC memory element” and “SLC memory element” should be construed as NAND-mappable/addressable physical pages that are those distinct memory types (*MLC pages that can be mapped to multiple logical pages simultaneously* and *SLC pages that can only be mapped to one logical page*).

* * * * *

Grounds for Review Under 37 C.F.R. § 42.204(b)(4)-(5):

VII. GROUND 1: THE CHALLENGED CLAIMS CLAIM PATENT-INELIGIBLE SUBJECT MATTER UNDER 35 U.S.C. § 101 AS DIRECTED TO AN ABSTRACT IDEA, NAMELY, “MEMORY SPACE,” WITHOUT CLAIMING SUBSTANTIALLY MORE THAN ASPECTS OF THE OPERATION OF A GENERAL-PURPOSE COMPUTER.

The Challenged Claims claim patent-ineligible subject matter under 35 U.S.C. § 101 as directed to an abstract idea without claiming substantially more than aspects of the operation of a general-purpose computer, such as limitations that improve the operation of such a computer. The Supreme Court has consistently expressed its concern with a patent claim preempting a field that would otherwise be open to inventive development, *Alice Corp. Pty. Ltd. v. CLS Bank International*, 573 U.S.

208, 216 (2014), *citing Bilski v. Kappos*, 561 U.S. 593, (2010) (finding a patent-ineligible abstract idea in a “long prevalent” practice). To prevent this preemption, the Court has held that patents directed to ineligible subject matter such as “abstract ideas” may not gain eligibility through recitation of elements or combination of elements, such as “computer functions [that] are ‘well-understood, routine, conventional activit[ies]’ previously known to the industry.” *Alice*, 573 U.S. at 225, *quoting Mayo Collaborative Services v. Prometheus Laboratories, Inc.*, 566 U.S. 66, 73 (2012). It is now familiar that the 35 U.S.C. § 101 subject matter eligibility analysis is divided into a step one of “determin[ing] whether the claims at issue are directed to a patent-ineligible concept,’ such as an abstract idea” (*Alice*, 573 U.S. at 217) and, if so, a step two of “consider[ing] the elements of each claim both individually and ‘as an ordered combination’ to determine whether the elements ‘transform the nature of the claim’ into a patent-eligible application” (*id.*, *quoting Mayo*, 566 U.S. at 77-79).

As reviewed at paragraph 80 of the Sechen declaration (Ex. 1002), in 2018, the ‘300 patent claims dropped mention of the known, physical MLC and SLC NAND flash “modules” that were the foundation of the 2012 common specification and first three Lifetime Patents and introduced its claimed memory system instead as a “memory space” with MLC and SLC “memory spaces” (‘300 7:38-42), a construct retained in the ‘369 patent (7:35-40) with further subdivisions. The word

“space” appears in the specification only to describe *market share*, “HDD space” (‘369 2:46), and relative *storage capacity* for the base hybrid SLC and MLC to avail of the use of SLC to boost lifetime (5:13-18). A POSITA would understand “memory space” in this context to be a *storage capacity property* of a memory. The unqualified claiming of a property is an abstract idea or “disembodied concept” at the heart of what the Supreme Court’s 35 U.S.C. § 101 jurisprudence regards as unpatentable subject matter. The claims fail to *integrate* the claimed “memory space” into a practical application, and they do not provide an inventive concept to counterweigh (provide “significantly more than”) the unqualified claiming of the property of “memory space.” Particularly, the remaining limitations of these claims simply recite “well-understood, routine, and/or conventional” elements in a conventional arrangement and fail to recite an inventive concept. Thus, the claims fail the Alice/Mayo test and are ineligible subject matter under 35 U.S.C. § 101.

The further subdivision in the ‘369 patent claims of “memory space” into “logical and physical” memory spaces (7:35-40; Sechen ¶ 84) did not provide the construct with any practical application: it simply states the *existence* of logical and physical addresses for “memory elements,” which do not include the “controller memory.” It does not even state the function of the FTL address table (7:50-53, 7:64-65), “well-understood, routine and conventional,” which itself is a transitory “signal” (information) ineligible as a “signal *per se*.” (*see In re Nuijten*, 500 F.3d

1346 (Fed. Cir. 1319)). (Also Sechen ¶¶ 95 and 102.) The “memory space” construct serves no technological purpose (Sechen ¶ 91) – only verbal camouflage for post-2018 claims to the same 2012 data integrity test in a known hybrid MLC-SLC NAND flash memory system.

The Challenged Claims are thus invalid as ineligible under 35 U.S.C. § 101.

VIII. GROUND 2: THE CHALLENGED CLAIMS LACK A WRITTEN DESCRIPTION DESCRIBING THE CLAIMED SUBJECT MATTER IN ACCORDANCE WITH 35 U.S.C. § 112(a).

As reviewed at paragraphs 79-84 of the Sechen declaration, (a) the abstraction in the ‘300 patent of “memory space” and “memory elements,” departing from the known hybrid memory system of SLC and MLC NAND flash modules with NAND flash-defined blocks, introducing “RAVM,” (2) the partial return in the ‘546 patent to “modules,” introducing “controller memory,” and (3) the further, paradoxical division of “memory space” into “logical and physical” memory space in the ‘369 elements of suggested physicality, do not identify any advance in the art overlooked in the pre-2018 patents but merely provide a verbal thicket to support the proliferation of Lifetime Patents. If there were some such advance in the newly recited “memory spaces,” RAVM and controller memory, it needed to be identified and enabled. If the “memory space” construct is to cover a genus of “all nonvolatile memory having superior endurance to MLC NAND,” the specification must enable the full scope of the invention. *Amgen Inc. v. Sanofi*, 598 U.S. 594, 610 (2023)

(substantial research results not adequate). As shown in Section X, there is no invention here at all, but even before one gets there, the ‘369 patent verbal thicket is exposed for unsupported and inoperable relationships between new terms, including those identified at paragraph 91-102 of Dr. Sechen’s declaration, which invalidate the Challenged Claims under 35 U.S.C. § 112(a):

A. The Challenged Claims Limited by “Memory Space” Are Unsupported Under 35 U.S.C. § 112(a).

The Challenged Claims are unsupported by any written description of the term “memory space” (7:35-40), where the term was used only to describe *market share* (2:46), and relative *storage capacity* (5:13-18). Unless read onto the recited memory spaces to limit relative “logical and physical” MLC and SLC memory spaces, these recitations provide no support to the claim recitations. And even if the capacity limitation were so read, there is nothing to support RAVM being part of the “memory space” (no mention of logical or physical address for RAVM) and “controller memory” not being part of it. (Sechen ¶¶ 84 and 91.) The Challenged Claims thus fail as unsupported under 35 U.S.C. § 112(a).

B. The Challenged Claims Limited by “Memory Element” Are Unsupported Under 35 U.S.C. § 112(a).

The Challenged Claims are unsupported by any written description of the term “memory element” (7:42-52, and *passim*), which is not even mentioned in the specification and for which “element” appears only as a boilerplate reference to

claim elements (7:27-31).⁸ (*Also* Sechen ¶¶ 80, 84 and 92.) To the extent that “memory elements” is considered a material limitation of the claimed system (as they must be), it is unsupported in the specification, and the Challenged Claims fail as unsupported under 35 U.S.C. § 112(a).

C. The Challenged Claims Limited by “Mapping . . . As Necessitated by the System To Maximize Lifetime” Are Unsupported Under 35 U.S.C. § 112(a).

The Challenged Claims lack any written description of “mapping . . . as necessitated by the system to maximize lifetime” (8:26-27). As reviewed in paragraph 81 of the Sechen declaration (Ex. 1002), the ‘300 patent introduced (and the ‘369 patent retained) this limitation without any support in the specification, including any mention of “maximiz[ing] lifetime” of anything. Dr. Sechen reviews the notions of extending or improving expected useful lifetime of a NAND flash memory system in the extensive background art, including through wear leveling, garbage collection and bad block management, with preference under some

⁸ The word “element” is mentioned in the incorporated Rao ‘916 description of its Fig. 2 as an “exemplary NAND memory integrated circuit as one element of the NVMS” (2:43-45). It would be absurd to consider this the “memory element” of ‘369 claim 1 “that can be mapped to a logical address” (7:44-45, 7:51-52).

circumstances in operation of a hybrid SLC-MLC NAND flash system to map and write to SLC or pseudo-SLC (¶¶ 39, 46-48, and 58-62 particularly notes 20 & 26). Some of these different (and not “necessary”⁹) approaches to enhancing useful lifetime of a NAND flash memory system were acknowledged in the specification BACKGROUND (Sechen ¶ 67, note 26; 3:21-26: NAND flash wear leveling “prolonging the service life”). Dr. Sechen discusses some of the ambiguities of the “maximize lifetime” clause at paragraph 81, including its abandonment of the

⁹ The only “mapping” that is “necessary” for the disclosed systems is the particular L2P mapping necessary for operation of NAND flash memory operation with its defining erase-a-block-before-writing requirement admittedly inapplicable to proposed alternative technologies. Moreover, that “mapping” in the context of a hybrid SLC and MLC NAND flash module, if it resulted as ordinarily in subsequent writing (preceded by erasure for data-occupied blocks), would *always* stress and thus incrementally decrease the useful lifetime of one block, leaving the other blocks, including any from which writing is remapped, at the same stage in life (subject to time effects) (Sechen ¶ 72). Thus, not every “mapping” would “maximize lifetime,” while a certain mix of “mappings” might be calculated to avoid premature end to reliability of enough components to compromise the intended use of the system (*id.* note 9).

Lifetime Patents theme of preferential mapping to an SLC NAND flash module. The bottom line is that it is unexplained in the specification any “mapping . . . necessitated by the system to maximize lifetime” of even the disclosed SLC-MLC NAND flash memory system, much less of memory systems of other than SLC-MLC NAND flash. The specification thus does not enable a POSITA to practice the claimed invention limited by the “maximize lifetime” clause or show that the inventor actually “possessed” that claimed invention. Thus, the claims fail under 35 U.S.C. § 112(a).

D. The Challenged Claims Reciting RAVM, Controller Memory and Their Respective Relationships to Stored and Retained Data Are Unsupported Under 35 U.S.C. § 112(a).

The Challenged Claims are unsupported by any written description of the post-2018 recited RAVM and controller memory and their relationship to “stored data” and “retained” data. As detailed in paragraph 71 of the Sechen declaration, the specification description of the data integrity test feature of the Lifetime Patents memory systems left much unexplained, particularly the nature and role of the “controller memory” and how it appeared that “retained data” was the data left in the controller memory after combination of valid data from flash after new data was “read from DRAM” (Sechen notes 38 & 39). As explained at paragraphs 83 and 84 of the Sechen declaration, the ‘300 claims left open the possibility that RAVM could be controller memory where retained data was left, until and even after the ‘546

patent recited a distinct controller memory with a different express role. Both ‘300 claim 1 (7:59-60) and ‘369 claim 1 (8:9-13) provide that the controller is “operable” to “retain such received data” in RAVM, but there is no explanation either in the specification how that is done – whether the “stored received data” recited as transferred “from” the controller memory to flash (8:5-9) is also transferred from the controller memory to the RAVM to be held as “retained data” and then, in “reading the stored data to the controller memory” (8:17-18) “and comparing the stored data in the controller memory in the given one of the physical MLC nonvolatile memory to the retained data” (8:18-21). Putting aside the apparently misplaced modifier, there is no disclosure in the claim or specification where or how the “stored data” in controller memory is compared to the “retained data.” If these were advances in the art, they are not enabled. Thus, the claims as limited by this language fail under 35 U.S.C. § 112(a).

E. The Challenged Claims Limited by “At Least One Memory Element” Are Unsupported Under 35 U.S.C. § 112(a) and Fail To Recite a Useful System for Storing Data.

The Challenged Claims, to a system merely having “at least one physical [MLC]/[SLC] nonvolatile memory element” in each “physical [MLC]/[SLC] memory module” (7:42-52), even if the term “memory element” were itself to pass the 35 U.S.C. §§ 112(a) and 112(b) challenges here, are unsupported under § 112(a) and fail to recite a useful system for storing data. The specification discloses two

two-bank embodiments that purport to avail of the superior endurance of SLC. There is suggested a beneficial mix in “SLC NAND flash equal to 12.5% or 25% of MLC NAND flash” (5:16-18), which is consistent with Fig. 4 showing two banks each of 2+ SLC modules compared to 8+ MLC modules (which with MLCs storing twice SLCs, meeting the suggested 12.5% ratio). Figs. 6a and 6b of incorporated Rao ‘916 (Ex. 1004) show a Samsung NAND flash chip K9F108XOA with a “1024M + 32M BIT NAND FLASH ARRAY,” clearly an SLC “module” (Fig. 8 [100K p/e cycle]). The context thus is one SLC module of 1,024 blocks of 64 pages each. Contrasting with this disclosure (and thus unsupported by it), each of the “system[s] for storing data” recited in the claims of the ‘369 patent is met with just one SLC memory element and one MLC memory element each in a plurality of MLC modules – and a POSITA would understand, in the “page architecture” of NAND flash (*e.g.*, Rao ‘916 1:39-58) in which the write operations are of a page, that an “MLC” and an “SLC” “memory element” should be construed respectively as one MLC physical page (row of cells) and one SLC physical page (Sechen ¶ 87). If “modules” of one page of physical memory satisfied the literal requirements of the systems recited in the Challenged Claims, as literally it would, that system would not be a useful one. There could be no multiple writes, given the NAND flash requirement of writing each update to another physical address, much less mapping maximize lifetime of the system. And there is nothing in the specification describing

the sufficient number of blocks or “memory elements” needed for the claimed inventions to enhance or maximize lifetime, or any way to determine a sufficient number. For at least these reasons, claim 1 of the ‘546 patent and all its dependent claims, are invalid under 35 U.S.C. § 112(a).

IX. GROUND 3: THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(b).

Claims 1-7 are invalid for indefiniteness under 35. U.S.C. 112(b) (formerly para. 2), because they recite limitations that, under *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898 (2014), considering the claims as a whole and as informed by the extrinsic record, fail to inform a POSITA with reasonable certainty about the scope of the claimed invention. A patent must be “precise enough to afford clear notice of what is claimed, thereby ‘appris[ing] the public of what is still open to them.’” *Id.* at 909. “Otherwise there would be a zone of uncertainty which enterprise and experimentation may enter only at the risk of infringement claims.” *Id.* Dr. Sechen identifies at paragraphs 76-91 multiple defects in the ‘369 patent claims, but Petitioner expressly raises here the following 35 U.S.C. § 112(b) defects:

A. The Challenged Claims Limited by “Memory Space” Are Indefinite Under 35 U.S.C. § 112(b).

As reviewed at Sections VII (§ 101 ineligibility) and VIII (A) (§ 112(a) lack of adequate written description), the meaning of the term “memory space” (7:34-40) was disclosed only as a measure of memory capacity, rendering the Challenged

Claims that recite the term invalid under those statutory provisions. If the term survives those challenges, under its further subdivision into “logical and physical” nonvolatile memory space that are mapped to each other and the physical nonvolatile element, it remains indefinite in view of the recitation that RAVM “physical memory element” “exists in the logical volatile memory space,” and the controller memory is no part of the space at all. The Challenged Claims thus fail as indefinite under 35 U.S.C. § 112(b).

B. The Challenged Claims Limited by “Memory Element” Are Indefinite Under 35 U.S.C. § 112(b).

The Challenged Claims, limited by the open-ended term “memory element” (7:42-52 and passim 7:56-:20; *see* Sechen ¶ 80) are indefinite as that term. On its face, “memory element” is so open-ended that it could be any of ‘300 claim 1’s mapping of “blocks, pages, or bytes of data” (‘300 8:25-26), or even a cell. Even though the term is modified by “physical” and “having a physical address” mappable to the respective logical space, it remains unclear what mappable subdivision of what NAND flash module is claimed. The Challenged Claims thus fail as indefinite under 35 U.S.C. § 112(b).

C. The Challenged Claims Limited by “Mapping . . . As Necessitated by the System To Maximize Lifetime” Are Indefinite Under 35 U.S.C. § 112(b).

As reviewed in paragraph 81 of the Sechen declaration, there are multiple axes of uncertainty in the claim 1 recitation of “mapping . . . as necessitated by the system

to maximize lifetime” (8:26-28), carried over from the ‘300 patent extreme abstraction of previously claimed systems. Even if the limitation survives the §112(a) arguments in Section VIII(C), there remain the questions, first, of at least of what “mapping” is implicated. As explained in Section VIII(C) every mapping (which is necessary for NAND flash memory operation, but perhaps not for alternative, “write in place” technologies) in the life of a NAND flash system, if followed ordinarily by writing, decreases expected useful lifetime. Claim 1 (and particularly the “maximize lifetime” clause) fails to specify any user-elected strategy/configuration of NAND flash mapping to distribute wear (stress), as reviewed extensively in the Sechen declaration (¶¶ 27-29, 38, and 40-56, particularly notes 20 & 26; Duann [Ex. 1034]; Lee ‘794 [Ex. 1041]; Surtardja [Ex. 1042]; Moyashedi [Ex. 1043]; and Gavens [1045]). The ‘369 patent omitted any claim to the DETAILED DESCRIPTION’s two-sentence (“hot” block v. “cold” block) “wear leveling” (to the SLC or MLC modules) embodiment (6:69-61). It *might* refer to the “remapping” (8:29) of a failed “data integrity test” of claim 1 (8:29-36) which roughly follow the NAND flash method steps in Figs. 3A and 3B, explained at 6:11-48. However, elements themselves are indefinite as when the test and remapping are performed (see Section IX(F). Just on the uncertainty of what mapping is implicated, a POSITA and the public and the public are not clearly apprised of what

is claimed. Accordingly, the Challenged Claims fail as indefinite under 35 U.S.C. § 112(b).

D. The Challenged Claims Are Indefinite Under 35 U.S.C. § 112(b) for Their Recitation of a “Controller” Limited by Functions in the Claims that Are Unsupported by Structure (Physical or Algorithmic) in the Specification.

Although two of the three main components of the disclosed and claimed in the ‘298, ‘385 and ‘240 patents are well-understood MLC and SLC NAND flash modules with their supporting physical organization of and operations with NAND flash pages and blocks, the “controller” was left open-ended with no physical structure or even a tether to technology. The indefiniteness remains in the ‘369 patent even though there are recited additional components of the RAVM (7:53-55), controller memory (7:60-62) and a (somewhat) distinct FTL (7:63-67). Thirty-five U.S.C. § 112(f) has been applied through § 112(b) to find indefinite a functionally claimed limitation of a general term (“nonce” word) which is not supported in the specification by adequate disclosure of structure (physical or algorithmic). *E.g.*, *Rain Computing, Inc. v. Samsung Electronics America, Inc.*, 989 F.3d 1002 (Fed. Cir. 2021). “Controller” is such a nonce word, and the specification does not adequately disclose structure for its claimed functions. Even if not recited in connection with a nonce word, the term fails under § 112(f) if it recites “a function but not sufficient structure for performing the function.” *Egenera, Inc. v. Cisco Sys.*, 972 F.3d 1367, 1373 (Fed. Cir. 2020). Where there are multiple claimed functions,

as in ‘369 claim 1, there must be disclosed “adequate corresponding structure to perform all of the claimed functions.” *Media Rights Techs., Inc. v. Capital One Fin. Corp.*, 800 F.3d 1366, 1374 (Fed. Cir. 2015). Where, as here, a general purpose computer or processor is claimed, special programming (an algorithm) is required to be disclosed. *Ergo Licensing, LLC v. CareFusion 303, Inc.*, 673 F.3d 1361, 1364–65 (Fed. Cir. 2012); *Aristocrat Techs. Austl. Pty Ltd. v. Int’l Game Tech.*, 521 F.3d 1328, 1333 (Fed. Cir. 2008).

The DETAILED DESCRIPTION recited no physical structure and no special programming for the “controller,” only general functions of NAND flash operation and the data integrity test (Sechen ¶¶ 70-73.) The functions recited in claim 1 for the controller include operating memory elements and associated memory space [1d1] (7:56-60), controlling access of a physical memory element for storage [1f1] (8:1-4), transferring stored received data [1f2] (8:4-8), operable to store and retain data [1f3] (8:9-13), performing a data integrity test [1g1] (8:14-17), reading the stored data to controller memory [1g2] (8:17-18), comparing the stored data [1g3] (8:18-23); whereupon failure of the data integrity test, a result, presumably attributable to the controller, are the functions of remapping [1i2] (8:30-32) and transferring [1i3] (8:32-36) retained data to a different physical address. The controller, in conjunction with FTL also maintains an address table [1e] (7:63-66) and performs mapping [1h] (8:24-27). These functions are presented in the

specification with no more detail than in the claims. (Sechen ¶ 94.) The Challenged Claims fail to inform a POSITA with reasonable certainty and are therefore indefinite under 35 U.S.C. § 112(b).

E. The Challenged Claims Are Indefinite Under 35 U.S.C. § 112(b) Because They Recite Method Steps in the Context of a Claim to a System.

Section V *supra* (Sechen Section VIII) showed that ‘369 claim 1 is merely a verbally camouflaged recitation of a hybrid MLC-NAND flash system known in 2011 and described and relied upon in the DETAILED DESCRIPTION with a data integrity test feature.¹⁰ Notwithstanding and corroborated by the post-2018 recitation of known RAVM and controller memory, there was no new apparatus or *capability* disclosed or claimed. The only thing putatively new was the “method for utilizing a NAND flash memory system” (6:11-12) of Figs. 3A and 3B described in functional steps (6:11-48) and claimed in ‘369 as functions of the controller (Section IX(D)): “the [at least one] controller, or the FTL, or a combination of both *maintain* an address table . . .” (7:63-66 [1e]), “the controller *controlling* access . . .” (8:1-4 [1f1]), “the controller, in at least a Write access operation *transferring* the stored received

¹⁰ The other feature in the DETAILED DESCRIPTION, wear leveling with a “transfer” that distinguished it from Gorobets ‘179, an example of multi-mode NAND flash memory, is not claimed in the ‘369 patent.

data . . .” (8:4-8 [1f2]), “the controller *performing* a data integrity test . . .by *reading* . . . and *comparing* the stored data . . .” (8:17-23 [1g2], [1g3]). Such claiming of a physical system (known or otherwise) reciting method steps is invalid for impermissibly mixing product and process limitations across different § 101 classifications, found to be indefinite under § 112(b). *IPXL Holdings, LLC v. Amazon.com, Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005); Manual of Patent Examining Procedure (“MPEP”) § 2173.05(p)(II).¹¹ The rule is particularly applicable here where the controller is the conventional NAND flash apparatus for performing the functional steps recited (maintaining an address table, controlling access, transferring, reading, and comparing data) and no new *capability* was disclosed or claimed (or implied) – only the *option* of performing the data integrity test at an unspecified time (*see* Section IX(F) *infra*). *See Rembrandt Data*

¹¹ The rule provides notice to a manufacturer of a product of whether its physical product infringes without knowledge whether a user of the product performs steps that infringe. Here, as alleged by Patent Owner in the pending suit, Phison is “a market leader in [manufacturing] NAND Flash controllers” (Amended Complaint [Ex. 1062] ¶ 6), while a user may elect to use error management features only late in the life of a NAND flash system, if at all. (*E.g.*, Sechen note 20.)

Technologies, LP v. AOL, LLC, 641 F.3d 1331, 1339 (Fed. Cir. 2011). Thus, the Challenged Claims are invalid under 35 U.S.C. § 112(b) as indefinite.

F. The Challenged Claims Are Indefinite Under 35 U.S.C. § 112(b) Because It Is Uncertain Whether and When the Recited Comparison Test Is Required To Be Performed.

The limitation, “performing a data integrity test . . . after the at least a Write access operation” (8:14-18) does not specify when the test is performed other than after some “Write access” – and not necessarily after *every* “Write access.” The DETAILED DESCRIPTION introduces in one place that “the controller conducts a data integrity test after every write.” (5:10-11 [emphasis added].) However, in a more detailed explanation, the execution of the test is qualified by “if time permits.” (5:57-60.) ‘369 patent claim 1 doesn’t even require performance of the test after *every* write, only after *a* write. Also, known error management techniques (Gavens [Ex. 1045] shown in Section X *infra* to disclose the recited data integrity test) delayed to near the end of life of the system (*e.g.*, Sechen note 20), applied only to a sampling of writes (Gavens 6:3-16), or not at all. The Challenged Claims are invalid under 35 U.S.C. § 112(b) as indefinite.

X. GROUND 4: CLAIMS 1-10 ARE OBVIOUS UNDER 35 U.S.C. § 103 OVER GAVENS IN VIEW OF POSITA KNOWLEDGE.

The ‘369 patent claims are obvious under *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007) because there is no gap between the prior art of multiple hybrid SLC-MLC NAND flash systems with post-write read error management (Section IV

supra) and the scope of the ‘369 claims. (Sechen ¶ 103): To the extent understandable, independent claim 1 of the ‘369 patent claims a memory system that would describe known hybrid MLC-SLC flash memory systems as described in the DETAILED DESCRIPTION [Sechen Section VII(B)] with known, necessary L2P mapping operations and at some time performs a “data integrity test” by comparing data written to flash with the data to be written to flash, with a general operation to avoid premature failure. Multiple alternative “data integrity checks” and approaches to avoid premature unreliability of NAND flash systems, including SLC-MLC hybrids, have been detailed in multiple prior art textbooks, articles and patents, as reviewed in [Sechen Section V(C)]. Gavens and its incorporated references disclose or render obvious the Challenged Claims in view of the knowledge of the POSITA.

A. Claim 1 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶ 104): Gavens (Ex. 1045), among the SanDisk portfolio and incorporating by reference others of that portfolio,¹² is a published reference that

¹² See, e.g., U.S. Patent No. 6,456,528 to Chen (“Chen ‘528”), Ex. 1040, incorporated by reference at Gavens 16:29-40 (binary mode operation); U.S. Patent Appl. Pub. No. 2011/0153912 by Gorobets et al. (“Gorobets ‘912”), Ex. 1049, incorporated by reference at Gavens 20:53-59 (post-write-read error management

discloses a complete multi-modal NAND flash system with the ordinary L2P/FTL function of its controller, a variety of post-write read error detection and management schemes, and the capability of and compatibility for employing other known tools (disclosed in incorporated documents and exemplified in paragraphs 58-61 above) used to avoid premature NAND system failure.

Although the Gavens system is not a “pure” SLC-MLC hybrid system, since the 2001 (*e.g.*, Cho, Ex. 1039) emergence of the terms “multi-level program cell”

with binary mode portion); U.S. Patent No. 5,930,167 to Lee et al. (“Lee ‘167”), Ex. 1050, incorporated by reference at Gavens 17:57-67 (MLC with binary mode cache); U.S. Patent Appl. Pub. No. 2010/0172180 by Paley et al. (“Paley ‘180”), Ex. 1051, incorporated by reference at Gavens 8:41-42 (block management system). In turn, both Gorobets ‘912 (¶¶ [0020], [0024]) and Paley ‘180 (¶¶ [0023], [0027]) incorporate by reference U.S. Patent No. 5,936,971 to Harari et al. (“Harari”), Ex. 1057, for using RAM in write cache for flash, and PCT Pub. No. WO 03/027828 by Gorobets et al. (“Gorobets PCT”), Ex. 1058, for buffering mapping information. Hereinafter, it should be understood that reference to a specific portion of any of the above references is understood to be disclosed by Gavens due to incorporation by reference, as if the incorporated document was explicitly contained in Gavens.

(MLC) memory and (thereby distinguished) “single level program cell” (SLC) memory, there have been implementations of hybrid MLC memory modules and SLC memory modules availing of the endurance advantages of SLC. (Sechen ¶ 105, *e.g.*, Lee ’794 [Ex. 1041], Sutardja [Ex. 1042], and Moshayedi [Ex. 1043].) Many NVM implementations disclosed in the SanDisk patent portfolio, such as Gavens, involve the partitioning and configuration of some MLC (or TLC) blocks for one-level (two states) or pseudo-SLC (pSLC) operation. (Sechen ¶ 92.) The pSLC mode of operation enjoys superior endurance compared to MLC in multi-level mode – though not as superior or as fast as “real” (native”) SLC memory which uses different circuitry. (Sechen ¶¶ 49, 105; *also* Gavens 12:6-10.) It would be obvious to a POSITA to use an MLC module operating entirely in pSLC mode (and thus be considered a pSLC memory module, which, as mentioned in [Sechen ¶ 49], are marketed as such), still with endurance superior to MLC in multi-level mode, or use a “real” or “native” SLC module, both with assured success. (Sechen ¶ 105.) Gavens clearly is a system for storing data as recited in the claim 1 preamble. (Sechen ¶ 108, Gavens Fig. 1 (90), 8:13-17.) It discloses or makes obvious, with its incorporated references, each of the limitations of the following elements of claim 1 in view of the knowledge of the POSITA:

1. **[1a] [1a1] memory space containing logical and physical volatile memory space and nonvolatile memory space, [1a2] wherein the logical and physical nonvolatile memory space includes both multi-level cell (MLC) logical and physical memory space and single level cell (SLC) logical and physical memory space;**

The **[1a]** memory space construct is abstract, unnecessary, unsupported and indefinite. (Sections VII, VIII(A) and IX(A) *supra*; Sechen ¶¶ 80, 91 and 101.) To the extent understood as including the aggregate of physical and logical addresses of MLC, SLC, and RAVM (even such addresses are not disclosed for it), Gavens satisfies the element by disclosing these components (Sechen ¶ 109): **[1a1]** “memory space” is disclosed as explained in Sections X(A)(2)-(3) *infra*, “logical and volatile,” “volatile memory space” in Section X(A)(3) [RAVM] and “nonvolatile memory space in Section X(A)(2) [MLC and SLC], the latter which also discloses **[1a2]** requiring MLC and SLC nonvolatile memories. Gavens and incorporated references, in view of POSITA knowledge, makes obvious claim element **[1a]**.

2. [1b] a bank of physical nonvolatile memory, including:

[1b1] a plurality of physical MLC memory modules, each including at least one physical MLC nonvolatile memory element having a physical address within the physical MLC nonvolatile memory space that can be mapped to a logical address in the MLC logical nonvolatile memory space, and

[1b2] at least one SLC memory module including at least one physical SLC nonvolatile memory element having a physical address within the physical SLC nonvolatile memory space that can be mapped into the SLC logical nonvolatile memory space;

[1b] Gavens discloses a bank of physical nonvolatile memory. (Fig. 1; 8:13-21; Sechen ¶ 113.) **[1b1]** (Sechen ¶ 113): The array of memory cells 200 is partitioned into a first portion 410 configured for lower density (*e.g.*, pseudo-SLC) operation and a second portion 420 configured for high density (*e.g.*, native MLC, having each cell storing multiple bits) operation. (Fig. 14A, 16:15-22.) The Gavens controller maps logical “memory spaces” (addresses) to the physical memory (addresses) (8:36-39). **[1b2]** (Sechen ¶ 114): Gavens discloses the above partition (also mappable) where the “first portion has each memory cell storing one bit of data and [a] second portion has each memory cell storing more than one bit of data” (4:32-34, 12:6-8 [calling memory operating in 1-bit mode “binary” or “SLC” memory]). These would render it obvious to a POSITA to substitute a “native” SLC flash memory module for the Gavens first portion element with assured success. (*Also*

Sechen ¶ 105.) Gavens, in view of POSITA knowledge, makes obvious claim element [1b].

3. [1c] at least one random access volatile physical memory element that exists in the logical volatile memory space;

(Sechen ¶ 116): It is well-known to use RAVM (also known as “RAM”) in a NAND flash controller as a staging or cache location for data to be written to the flash memory. (*E.g.*, Rao ‘916 [Ex. 1004] Fig. 3 [“Data Reg.”].) Gavens incorporated by reference Gorobets ‘912 (Ex. 1049) and Paley ‘180 (Ex. 1051), the latter expressly for block management (note 53 above). Both share Fig. 1 showing a controller 100 with RAM 130, shown in Gorobets ‘912 Fig. 11 and Paley ‘180 Fig. 15 as “Cache (RAM) 102” within the controller. Gorobets ‘912 explains the controller cache 102 as one of a series of “high speed storage for temporarily storing data being passed between a higher speed component of the system” (¶ [0109]) and as a “volatile buffer memory . . . which is typically part of the controller” for host-originated “logically consecutive data” before staging in the binary portion of MLC that it shares with the Gavens embodiment. Paley ‘180 similarly explains that “[t]ypically high-speed volatile RAM are employed . . . in a controller cache 102 of the memory controller.” (¶ [0197].) Both Gorobets ‘912 and Paley ‘180 incorporated by reference (note 53 above) (1) Harari (Ex. 1057), which shows as part of its Fig. 8

“cache buffer 705” as part of a cache system 701 “as part of the controller,” explained at 12:20-35, 13:24-42 and 12:58-14:11, and (2) Gorobets PCT (Ex. 1058) 11:10-12:3 [controller SRAM buffers logical sector data, quoted at Sechen ¶ 116].) A POSITA would further understand that there would be random access volatile memory for controller functions in the controller, including mapping (*e.g.*, Rao ‘916 [Ex. 1004] Fig. 3 [“InstReg.” and “Add- Map”]; Moshayedi [Ex. 1043] Fig. 2 [RAM 214]) as disclosed in Gavens, at least in incorporated references Gorobets PCT 11:12-13, Gorobets ‘912 ¶ [0018] and Harari Fig. 8 (memory 709).

(Sechen ¶ 116): It is also well-known to use DRAM (external to a controller chip) in a memory system such as shown on an SSD in Micheloni Fig.1.16 (Ex. 1025 at 14, reproduced at ¶ 30 above) in the same detail as DRAM 20 in ‘369 Fig. 1. As an example, Fig. 1 of Moshayedi (Ex. 1043) shows DRAM 106 external to controller 102 and controlling banks of SLC modules (112) and MLC modules (114), much as ‘369 Fig. 1. Moshayedi explains that “DRAM 106 may be used to buffer data to be written into the flash array 108 . . . which may be incoming data from a host system/and or data being rewritten from one portion of the flash array 108 to another portion of the flash array 108.” ([¶ [0028]].) The DRAM can also be used for tables and linked lists which may be stored to SLC on power-down. (*Id.* ¶ [0053].) Either qualify as “at least one” RAVM. Because only a certain number of parallel bits may

be received from the host or sent to a memory array, there may be multiple caches (including the flash memory chip page buffer).

Gavens and incorporated references disclose or, in view of the POSITA's knowledge of NAND flash, claim element **[1c]**.

4. **[1d] at least one controller [1d1] to operate physical memory elements and associated memory space for associated Write access operations to the physical memory elements and Read access operations from the physical memory elements, [1d2] the controller having a controller memory associated therewith for storing received data therein;**

(Sechen ¶ 118): **[1d1]** Gavens Fig. 1 shows controller 102. The controller 102 manages one or more memory chips 100 in the memory device 90. (8:17-18, 32-35.) Taking the “memory space” as logical addresses, in Gavens, “[a] memory block management system implemented in the controller stages the [logical] sectors and maps and stores them to the physical structure of the memory array” (8:36-39).

(Sechen ¶ 119): **[1d2]** As explained at [Section X(A)(3) *supra*], Gavens and its incorporated reference, Gorobets PCT (Ex. 1058) discloses in-controller RAVM for storing (caching) received data. It is also common to use off-controller DRAM for data caching (*e.g.*, ¶ 31 above, Moshayedi Fig. 1(106), ¶ [0028]).

Gavens and incorporated references disclose or, in view of the POSITA's knowledge of NAND flash, claim element **[1d]**.

5. **[1e] a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements;**

(Sechen ¶ 121): An FTL would be understood by the POSITA as the software layer supporting the L2P functions of a NAND controller ([Sechen ¶¶ 31-38], Micheloni [Ex. 1025] at 40, 492-98, and 516-17 [Fig. 18.3]), and thus is included within a NAND controller performing such functions as disclosed in Gavens. Gavens discloses the ordinary NAND controller function: “A memory block management system implemented in the controller stages the sectors and maps and stores them to the physical structure of the memory array” (8:36-39.) Gavens discloses updating of “a directory in a block management system embedded in the firmware of the controller (see Fig. 1)” to direct accesses to one or the other portions of the memory (17:17-19, 18:47-49, 18:64-66). Gavens, for further explanation of block management, incorporated by reference Paley ‘180 ([Sechen note 52]).

(Sechen ¶ 122): Incorporated reference Paley ‘180 (Ex. 1051) provides further detail:

A memory-side memory manager 300 is implemented in the controller 100 of the memory system 90 to manage the storage and retrieval of the data of host logical sectors among metablocks of the flash memory 200. The memory manager comprises a front-end system 310 and a back-end system 320. The front-end system 310 includes a host interface 312. The back-end system 320 includes a number of

software modules for managing erase, read and write operations of the metablocks. The memory manager also maintains system control data and directory data associated with its operations among the flash memory 200 and the controller RAM 130.

(¶ [0155] [emphasis added]; *also* Gorobets ‘912 ¶ [0095].) Paley explains the use of “the currently prevalent LBA interface” (¶ [0020]). “The memory manager 300 is preferably implemented in the controller 100. It translates logical addresses received from the host into physical addresses within the memory array, where the data are actually stored, and then keeps track of these address translations.” (¶ [0150].) Referring to Fig. 9, “the media management layer 330” (¶ [0157]) and “dataflow and sequencing layer 340” (¶ [0158]) combine to perform the role of FTL. Specifically, the media management layer handles “updates, tables and lists used for logical-to-physical address translation and free block management, and wear leveling based on hot counts” (¶ [0201] [emphasis added]). As further explained in the incorporated Gorobets PCT (Ex. 1058), the media management layer is implemented in firmware “control[ing] the transfer of data sectors between the logical interface 14 to host 12 and the physical interface 18 to Flash memory 20” (Gorobets PCT 13:5-8 [emphasis added]) with the following algorithms:

The data structures required to support the Cyclic Storage [7:20-24: “method of ensuring uniformity of distribution of use”¹³] media management algorithms [18:1-10: (1) Data Write location to write host data, (2) Block Erase controlling erasure of obsolete data, (3) Block Sequencing of flash blocks used for storing data, and (4) Address Translation controlling “mapping of host logical addresses to physical memory addresses”] are stored principally in flash memory 10 together with the host data sectors, with only a very limited amount of control data being held temporarily in the control processor’s volatile RAM 30. Information held in the volatile memory 30 is non-critical, and can be reconstructed from flash memory if the power supply is interrupted.

(27:22-28:5 [emphasis added].) As explained at [Sechen ¶ 34], it was well-known, as corroborated by Goodson (submitted with the 2012 ‘298 application), that the address tables were loaded in controller RAVM and backed up in the flash memory. The NAND flash memory system disclosed in Gavens as further detailed in its incorporated references [note 12 *supra*] explained:

¹³ An objective is “to obtain even use of blocks in the non-volatile memory for storage of data over a long period of operation, and to avoid ‘hot-spots’ in non-volatile memory usage, thereby increasing the reliability of the memory system.” (Gorobets PCT 2:4-8 [emphasis added].)

The top level of hierarchy of the mapping structure [Fig. 5 schematic of the “address translation process”] is the sector address table 52, which is a master table containing a physical address for every logical sector stored in the system 10 and which is stored in Flash memory 20. . . .

The sector address record 56 is a list stored in the controller’s memory volatile memory SRAM 30 It may also be reconstructed during device initiation from the sequence of recently written sectors which may be traced in the Flash memory 20. The intermediate temporary sector address table 54 is contained in flash memory 20 and is updated with the contents of the sector address record 56

This hierarchy of mapping structures . . . efficiently supports logical to physical address translation . . . even if electrical power is unpredictably removed from the system 10.

(Gorobets PCT [Ex. 1058] 26:11-27:21 [emphasis added].) Gavens thus discloses an FTL that maintains address tables in both the RAVM and the flash memory. Gavens and its incorporated references disclose element **[1e]**.

6. **[1f] [1f1] the controller controlling access of the physical MLC and SLC nonvolatile memory elements and the random access volatile physical memory elements for storage of the received data therein as stored data, [1f2] the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the physical MLC nonvolatile memory elements in an associated physical MLC memory module, [1f3] operable to store the received data in the given one of the physical MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile physical memory element as retained data associated with stored data;**

(Sechen ¶ 124): See [Sections X(A)(2)-(5) *supra*] regarding common controller operations of the Gavens controller. [Also 369 2:28-3:10 [writing host data to NAND flash nonvolatile memory]; Sechen ¶¶ 30-38).

(Sechen ¶ 125): **[1f1]** It was shown in [Sections X(A)(2)-(5)] that Gavens discloses a controller which “cooperates with the [NAND flash] memory chip [MLC partially operable in 2-state, pSLC mode, obviously substitutable with ‘real’ SLC] and controls and manages high level operations,” for example, a host write translated in logical sectors to the memory array (8:32-36) [thus storage of data received from the host 80 in Fig. 1]; the operation obviously involves control of the RAM data cache or buffer disclosed by Gavens ([Section X(A)(3)], *e.g.*, incorporated Paley ‘180 ¶ [0197]) where the received data may be received as recited in claim element [1d] and temporarily stored (or retained).

(Sechen ¶ 126): [1f2] In one variant of the Gavens post-write-read error management embodiment of Figs. 14 and 15 (explaining text at 16:13-17:42), user data is written to the higher density (*e.g.*, MLC) portion as a “first copy.” (Gavens 16:41-45.) It is obvious that the controller controls this operation, transferring data “from” a memory or cache associated with it ([Sechen ¶ 119 [1d2]]). With the POSITA understanding that the transferred “stored received data” is the data written to (and “to be stored” in) MLC, the recited “Write access” operation is satisfied by the Gavens error management embodiment by “storing” data in the MLC [1f3] while operating the system to maintain the “original copy which may be cached” (16:46-49 [emphasis added]) as the “retained data” in the assumed, common on-controller or associated external RAVM (or both) ([Section X(A)(3) *supra.*) As explained at [Sechen ¶¶ 71 and 93], no more (but less) detail is provided in the ‘369 DETAILED DESCRIPTION. Gavens thus discloses, in view of POSITA knowledge, claim element [1f].

7. **[1g] the controller [1g1] performing a data integrity test on stored data in the given one of the physical MLC nonvolatile memory elements in the associated one of the physical MLC memory modules after the at least a Write access operation performed thereon by [1g2] reading the stored data to the controller memory and [1g3] comparing the stored data in the controller memory in the given one of the physical MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile physical memory element by the controller during the Write access operation;**

Gavens discloses multiple techniques for error management. (Sechen ¶¶ 53-55, 128.) (Sechen ¶ 129): One, referenced in Section X(A)(6) *supra*, in a “post write read,” provides a check for errors [1g1], [1g3] “by comparison with the original copy which may be cached” (16:46-49 [emphasis added]) – which may be in the RAVM of the controller memory or associated DRAM ([Sechen ¶¶ 116 and 122]). If the number of error bits is less than a predetermined amount, the first copy is deemed valid and subsequent reads of the data page will be from that copy with any errors corrected by ECC. (16:50-56.) If the number is greater, then a copy is written to the lower density, lower error rate (more robust, *e.g.*, pSLC) portion; this is performed in one embodiment by copying from a cached copy “of the original data.” (17:9-11.) In the Gavens NAND flash technology corpus, “[u]sing RAM in a write cache operating with flash memory has been disclosed” (*e.g.*, Gorobets ‘912 [Ex. 1049] ¶ [0024], Paley ‘180 [Ex. 1051] ¶ [0027]). The “original data” temporarily stored (“cached” in RAM, understood to be RAVM) is compared to the stored (in

flash) data, and if the stored data fails to match, the “original data” (temporarily stored or “retained”) is sent to the more robust pSLC. Thus, this error management variant discloses a data integrity test on written (stored) data that compares it against retained (cached) “original data” in RAM cache. It would be obvious that the “stored data” to be compared would be **[1g2]** written to the controller memory (where the Gavens/Gorobets cache has space for at least two write units, nominally, pages) for comparison using logic on the controller chip (*e.g.*, incorporated Rao ‘916 [Ex. 1004] Fig. 1 [“ALU”]). (Sechen ¶ 130): It would be obvious to substitute a “real” SLC memory for the 2-state partition of Gavens. Gavens and incorporated references, in view of POSITA knowledge, makes obvious claim element **[1g]**.

8. [1h] wherein the address table maps logical addresses to physical addresses of the memory system, wherein the mapping is performed as necessitated by the memory system to maximize lifetime; and

(Sechen ¶ 132): Incorporate explanation in [Section X(A)(5) *supra*] regarding Gavens’s use of address tables to map logical and physical addresses that may be blocks or pages in ordinary NAND flash operation. To the extent that the “maximize lifetime” limitation can be understood (*see* [Sechen ¶ 81]), Gavens’s (1) flash system media management wear leveling ([Sechen ¶ 122 and note 13 *supra*]) and (2) error management disclosing ([Section X(A)(6) *supra*]) claim elements **[1g]** and **[1i]** remapping and transfer for data integrity failure each satisfy this limitation by enhancing lifetime.

9. [1i] wherein a failure of the data integrity test performed on the stored data by the controller results in [1i1] a remapping of logical address space to a different physical range of addresses in the physical address space and [1i2] transfer of data corresponding to the retained data to those remapped physical addresses in the physical address space from those physical addresses in the physical address space determined to have failed the data integrity test.

(Sechen ¶¶ 134-135): To the extent understood, as explained in [Section X(A)(6) *supra*], in the Gavens embodiment, after the data stored in the less robust (MLC) portion fails a data integrity test by exceeding a predetermined number of bit errors, the “original data” is rewritten to the more robust (pSLC) portion (Gavens 17:9-12). For that to occur, the original data must be remapped [1i1], and any “transfer” [1i2] in this context is the writing of that original data to the remapped – different – location (physical address), thereby satisfying the remapping and transfer limitations. Gavens discloses claim element [1i].

* * * * *

(Sechen ¶ 137): Gavens and its incorporated references make obvious, in view of knowledge of the POSITA, each limitation of ‘369 claim 1.

B. Claim 2 to a Software FTL Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 139 and 140): Claim 2, the system of claim 1 “*wherein the FTL flash translation layer is a software module, or a firmware module containing*

software updates,” is obvious at least because, in addition to the obviousness of the base claim (Section [X(A) *supra*]): As explained in Section [X(A)(6) *supra*], Gavens disclosed though its reference for block management (8:40-43), namely, Paley ‘180 (Ex. 1051) (¶¶ [0155]-[0159], [0201]), which further incorporated Gorobets PCT (Ex. 1058) [note 14 *supra*], disclosed the use of a media management layer and a dataflow and sequencing layer that perform: a) the L2P mapping/translation, and b) the wear leveling and block management functions of known FTL (*compare* ‘300 3:3-35, [Sechen ¶¶ 34-38]). The next sentence in Gavens (8:44-45) refers to firmware 60 to implement the functions of the controller, and Gorobets PCT disclosed its sector sequencer, media management layer and flash controller layer, “control[ling] the transfer of data sectors between the logical interface 14 to host 12 and the physical interface 10 to Flash memory 20,” specifically as firmware (12:22-13:8), clearly updatable as located in SRAM (11:10-13).

Gavens and its incorporated references disclose **claim 2**.

C. Claim 3, Limited to RAVM, MLC or SLC in the Controller, Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 142 and 142): Claim 3, the system of claim 1 “*wherein at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller,*” is obvious at least because, in addition to the obviousness of the base claim (Section [X(A) *supra*]): As explained

in Section [X(A)(3) *supra*], Gavens discloses, through incorporated references, the embedding of RAVM in the controller both as a data cache and as a temporary location for data for other controller functions (*e.g.*, respectively, Gorobets ‘912 [Ex. 1049] ¶ [0197], [0018] ; *also*, Gorobets PCT [Ex. 1058] 11:10-13 [both]). Although there was an argument made during prosecution of the ‘300 patent application that two “blocks” of “nonvolatile [sic, probably ‘volatile’] memory” were required for the data integrity test and that a “conventional cache” was not that large (¶ 83 above), there is no support in the specification for any hardware departure from the known hybrid MLC-SLC memory system and no claim is made to such a new hardware combination. Indeed, incorporated Gorobets PCT (Ex. 1058) explained that “[s]ufficient capacity in the SRAM 30 is allocated for buffering of two sectors” (11:24-12:2) (Sechen ¶ 147): Thus, Gavens, in view of the knowledge of the POSITA, discloses **claim 3**.

D. Claims 4 and 9, Limited to the Nature of MLC and SLC Memory as Flash and Remapping to the Latter, Are Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 144-147 and 160-162): Claims 4 and 9, the system of claim 1 wherein [4] “*the physical MLC and SLC nonvolatile memory elements comprise flash memory*” and [9] “*the remapped physical addresses in the physical address space are located in the SLC memory*” are obvious at least because, in addition to the obviousness of the base claim (Section [X(A) *supra*]): These limitations are

inherent in the understood meanings of “MLC” and “SLC” and the superior endurance of SLC over MLC.

(Sechen ¶¶ 145 and 146 [**claim 4** “flash”]): Gavens, which would be understood by a POSITA to describe a NAND flash system with multiple MLC NAND flash modules, expressly describes its MLC non-volatile memory modules as including MLC NAND flash memory elements, which by definition are flash memory. (Fig. 4, 9:49-50 [page of memory cells in the memory array 200 is organized in the NAND configuration], 1:18-19, 4:14-18 [flash memory having a first portion and a second portion storing higher density compared to the first portion], 2:65-66, 8:65-67 [flash memory devices with NAND string structures; Fig. 1 (90) [flash memory device].) As explained at [Sechen ¶¶ 105 and 114], a POSITA would readily and successfully substitute for Gavens’s partitions of MLC memory elements configured for 2-state pseudo-SLC operation an SLC non-volatile memory module which is understood to include SLC NAND flash memory elements. As to Gavens’s MLC NAND flash memory operated in pseudo-SLC mode, they are also described as flash memory. (Fig. 4, 9:49-50 [a page of memory cells in the memory array 200 is organized in the NAND configuration], 1:18-19, 4:14-18 [flash memory having a first portion and a second portion storing higher density compared to the first portion], 2:65-66, 8:65-67 [flash memory devices with NAND string structures], Fig. 1 [flash memory device 90].)

(Sechen ¶¶ 161-162 [**claim 9** remap to SLC]): As explained in Section [X(A)(9) *supra*], in that Gavens error management embodiment, after the data stored in the less robust (MLC) portion fails a data integrity test by exceeding a predetermined number of bit errors, the “original data” is rewritten to the more robust (pSLC) portion (Gavens 17:9-12). (Sechen ¶ xx]): It is admitted art that SLC memory has higher endurance than MLC memory (‘300 3:44-50 [50-100K writes v. 3-10K writes]). The Gavens embodiment making obvious the system of claim 1 (Section X(A)) includes a portion of the memory having cells “configured as lower density storage . . . operating in two states [pSLC mode for] faster programming and a longer operational life” (Gavens 16:19-35). (Sechen ¶¶ 141 and 145 [both claims]): As explained in [Sechen ¶¶ 105 and 114], it would be obvious to substitute “real” SLC memory for the pSLC portion in Gavens; it would be a faster process ([Sechen ¶ 117])

Thus, Gavens and incorporated references, in view of the knowledge of the POSITA, disclose or render obvious **claims 4 and 9**.

E. Claims 5 and 6, Limited to the Type of the RAVM, Are Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 148-149 and 138-139): Claims 5 and 6, the system of claim 1 “*wherein the random access volatile memory is*” [5] “*dynamic random access memory*” and [6] “*static random access memory,*” are obvious at least because, in

addition to the obviousness of the base claim (Section [IX(A) *supra*]), in view of a POSITA's understanding that dynamic random access memory (DRAM) and static random access memory (SRAM) are common types of random access volatile memory (RAVM) that may be used for purposes of temporarily holding data to be compared as is the recited role of RAVM in claim 1, either would be an obvious choice for Gavens's cache of "original data" for comparison (16:47-49).

(Sechen ¶ 136 [**claim 5** DRAM]): The background art supports such use of DRAM for cache and other NAND flash functions. (*E.g.*, Moshayedi [Ex. 1043] Fig. 1 (106), ¶ [0028] [Dynamic Random Access Memory 106 shown external to but "can be present in controller 102" and "may be used to buffer data to be written into the flash array 108"], *also* ¶ [0004] [DRAM used in management of read and write operations of flash, contain addressing table correlating logical and physical addresses], ¶ [0053] [DRAM for linked lists, saved on SLC], ¶ [0054] [DRAM for tables and 4K logical blocks of data cache], ¶ [0067][suitable amounts of DRAM for different SLC-MLC combinations]; Duann (Ex. 1034), p. 6 [utilize DRAM as cache].)

(Sechen ¶ 139 [claim 6 SRAM]): Gavens discloses the use of SRAM through incorporation of Gorobets PCT (Ex. 1058) (11:10-12:3 [buffering of logical data and storage of control data and tables], *quoted* at ¶ 109 above; *also* Paley '180 Fig. 17, ¶¶ [0423]-[0425], [0502], [0503], [0506] [SRAM for storing "group address

tables”]). Duann (Ex. 1034), p. 6, suggested “[b]igger internal SRAM as cache” for a hybrid SLC and MLC system.

Thus, Gavens, in view of the knowledge of the POSITA, makes obvious **claims 5 and 6.**

F. Claim 7, Limited to an SLC Element Including an HDD, Is Obvious Over Gavens, Including Incorporated references, in View of Knowledge of the POSITA and/or Colligan.

(Sechen ¶¶ 154-155): Claim 7, the system of claim 1 “*wherein the at least one physical SLC nonvolatile memory element includes a hard disk drive (HDD),*” is obvious at least because, in addition to the obviousness of the base claim (Section [X(A) *supra*]): A POSITA would understand that it is physically impossible for an SLC flash memory chip (much less an included “element”) to include a hard disk drive, where the latter is orders of magnitude larger than a flash chip. If this and all the inconsistencies with claim 1 were ignored, including the antecedent of being a part of an “SLC” module and changing the nature of an “SLC nonvolatile memory element,” a POSITA would know that there are some useful combinations of flash and HDD such as disclosed in U.S. Patent No. 8,225,035 to Colligan (Ex. 1052) 2:33-36, 5:40-6:6, 7:67-8:2, and 8:23-25 (flash memory could supplement HDDs for more frequent writes) and the POSITA could **call** a combination of disk(s) 24 and SLC flash 28 of ‘546 Fig. 1 an “SLC nonvolatile memory element” to replace bad MLC blocks as physical address destinations. Thus, Gavens, in view of the

knowledge of the POSITA, discloses **claim 7** with an overstretched construction of “element.”

G. Claim 8, Limited to a Controller Associated with an External Processor, Is Obvious Over Gavens, Including Incorporated references, in View of Knowledge of the POSITA and/or Colligan.

(Sechen ¶¶ 157-158): Claim 8, the system of claim 1 “*wherein the at least one controller is associated with a processor external to the memory system,*” is obvious at least because, in addition to the obviousness of the base claim (Section [X(A) *supra*]): Gavens Fig. 1 shows communication of the controller 101 with a host (computer/processor) 80 external to the memory system 90. Thus, Gavens and its incorporated references, in view of the knowledge of the POSITA, make obvious **claim 8**.

H. Claim 10, Limited to an FTL Associated with the MLC and SLC Modules, Is Obvious Over Gavens, Including Incorporated references, in View of Knowledge of the POSITA and/or Colligan.

(Sechen ¶¶ 154-155): Claim 10, the system of claim 1 “*wherein the FTL is associated with the MLC memory modules and the SLC memory modules in the bank of physical nonvolatile memory,*” is obvious at least because, in addition to the obviousness of the base claim (Section [X(A) *supra*]): As shown in [Section X(A)(5) *supra*], Gavens’s FTL, maintaining the address maps for the MLC and SLC modules, clearly is associated with the MLC and SLC modules. Moreover, the

address maps are also backed up in flash. Thus, Gavens and its incorporated references, in view of the knowledge of the POSITA, make obvious **claim 9**.

* * * * *

In sum, Gavens (Ex. 1045) and its incorporated references, in view of the knowledge of the POSITA, make obvious each of the Challenged Claims 1-10 of the ‘369 patent. (Sections X(A)-(H) *supra*; Sechen ¶¶ 103-166.)

XI. THE PENDING LITIGATIONS IN THE WESTERN DISTRICT OF TEXAS DO NOT WARRANT DENYING INSTITUTION.

With eight current patents asserted by Vervain against Phison based on varying word claims to the same two “data integrity test” and “wear leveling” functions described in the same specification for a known hybrid SLC-MLC NAND flash memory, review by this Board is more appropriate than by the District Court where those word variations can escape scrutiny. Construction of the multiple terms of the eight patents are restricted in number (12) in the District Court (per “side” in related cases as present here), even counting contentions of indefiniteness. As demonstrated in the above-stated grounds (Sections VII-X *supra*), the case against this patent is compelling. Balancing of the six factors set forth by the Board in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential) does not warrant denying institution here. Rather, institution would best serve the interest in “system efficiency, fairness, and patent quality” (*id.* at 5), allowing due

resolution of the substantial patentability questions (*id.* at 15).

As to *Fintiv* Factor 5, the petitioner and defendant in the parallel proceeding are the same party. Phison filed this petition expeditiously, where it received first notice of Vervain's assertion in the Complaint filed March 8, 2024, and the First Amended Complaint filed May 13, 2024 (Ex. 1082), leave to amend granted Dec. 18, 2024 (Ex. 1080). No substantive opinions have issued regarding the scope or validity of the Challenged Claims. The parallel proceeding is still in an early stage: the Court recently granted-in-part Phison's motion to dismiss (*see* Docket List [Ex. 1080] entries 12, 24, 26 and 38), Phison has not otherwise answered, fact discovery just commenced and claim construction materials exchanged in accordance with the Scheduling Order (Ex. 1083). A *Markman* hearing, initially scheduled for December 5, 2024, is postponed until January 9, 2025. ([Ex. 1080] entry 39) Thus, as to Factor 3, there has not been overriding investment in the parallel proceeding; to the contrary, the requirements of the parallel proceeding limited Markman construction to twelve terms between the parties for eight patents of verbal variations of the same specification. Thus, as to Factor 4, there is overlap, in the greater inclusiveness of the requested review as the District Court will not consider all the issues properly raised in this Petition, pending PGR2024-00047, PGR2024-00048, IPR2025-00212, IPR2025-00213, IPR2025-00214 and IPR2025-00215, and others that Petitioner may petition.

Factors 1 and 2 do not significantly weigh for or against instituting the requested IGR. Petitioner does not know if the District Court will stay the case if trial by this Board is instituted and the Court has *tentatively* set jury selection for December 15, 2025 (Scheduling Order [Ex. 1083] at 4).

Regarding the sixth factor, the merits strongly weigh in favor of instituting trial as shown through the strength of the grounds in this Petition. “Other circumstances” favor institution. As described at note 5 *supra*, there are separate suits by Patent Owner Vervain (following the same template) against Phison and a customer (Kingston Docket List [Ex. 1081]). This presents the complexity of eight patents with method and apparatus claims that Vervain asserts against multiple, sometimes competing products (that thus must be held confidential between the defendants) that implicate third-party actors who may be implicated in divided or indirect infringement as users who select the configuration or performance of the claimed system. Moreover, unlike Phison, its customer defendant in the other case moved to dismiss for improper venue and to transfer (Kingston Docket List [Ex. 1081] entries 13 and 20) with attendant discovery and confidentiality proceedings (*id.* entries 15 and 16).

The interest of the public in cleaning away such verbal variants of questionable innovation in the eight Vervain patents are best served by the requested review. The Board may take notice that such litigation, if it reaches trial, will have

been drastically reduced in claims and theories asserted – beginning with the limitation of terms for construction for eight patents. A trial before the Board, in contrast, may resolve all Challenged Claims reviewed, substantially simplifying district court trial without the extensive district court discovery for which the America Invents Act offered this alternative before the Board – especially appropriate for the recent Lifetime Patents issued on verbal variations. And, of course, Petitioner has shown its case to be compelling.

XII. CONCLUSION

Petitioner submits that for the reasons set forth above, it has been shown that more likely than not, the Challenged Claims are invalid under all of 35 U.S.C. §§ 101, 112(a), 112(b), and 103 and should reviewed by the Board and canceled.

Date: December 26, 2024

Respectfully submitted,
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CERTIFICATION OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above-captioned Petition for Inter Partes Review of U.S. Patent No. 11,967,369 (and accompanying exhibits), was served in its entirety on December 26, 2024, upon Patent Owner's correspondent of record via USPS Express Priority Mail:

*Patent owner's correspondent
address of record for U.S. Patent No. 11,967,369*

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CERTIFICATION OF WORD COUNT (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the attached Petition, including footnotes, but not the cover page, exhibit list, table of contents, mandatory notices, and certifications, contains 16,556 words, as measured by the Word Count function of Microsoft Word. This is less than the limit of 18,700 words as specified by 37 C.F.R. § 42.24(a)(ii).

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