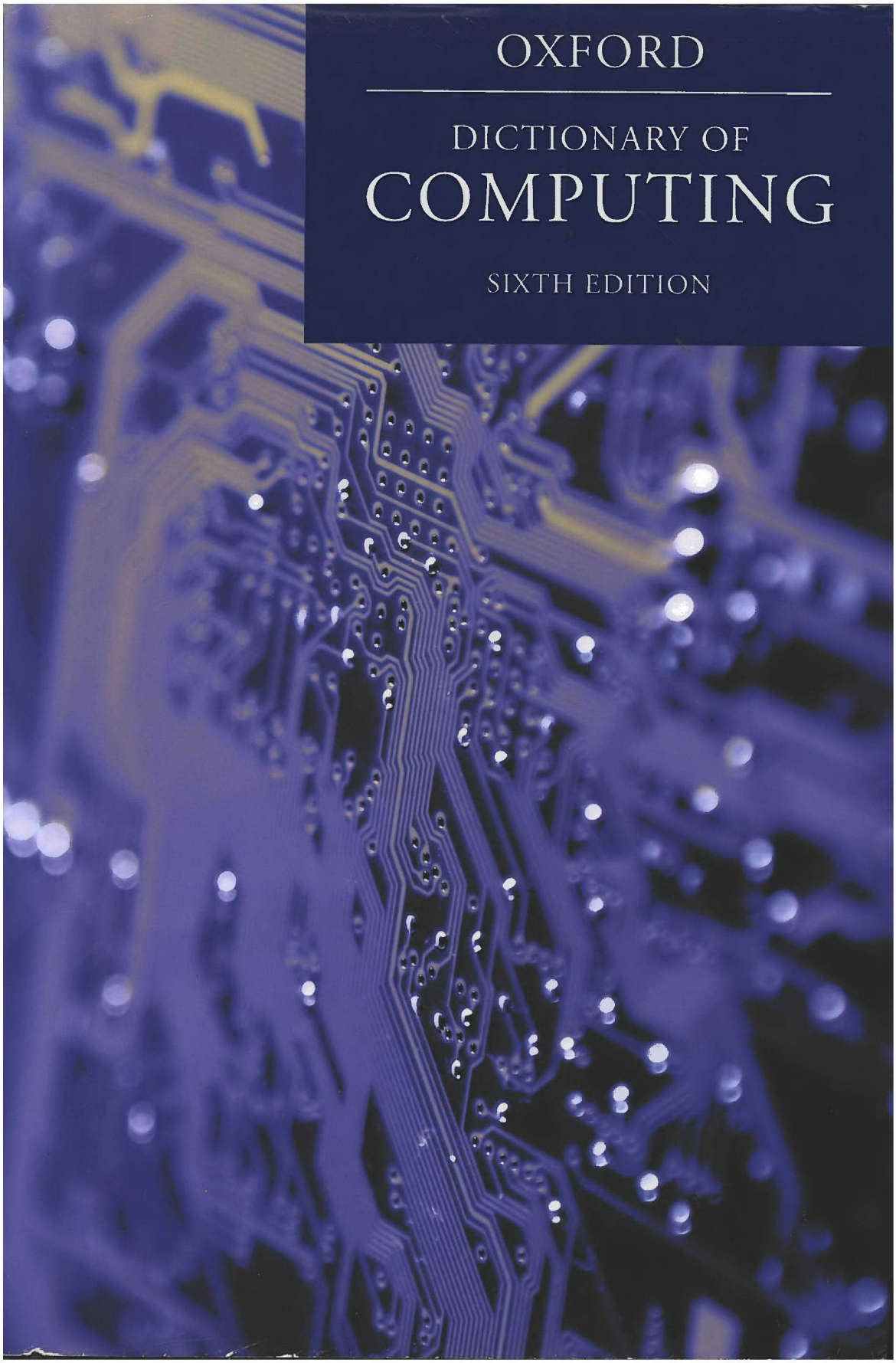
OXFORD
DICTIONARY OF
COMPUTING
SIXTH EDITION

A Dictionary of

Computing

SIXTH EDITION

OXFORD
UNIVERSITY PRESS

OXFORD
UNIVERSITY PRESS
Great Clarendon Street, Oxford OX2 6DP
Oxford University Press is a department of the University of Oxford.
It furthers the University's objective of excellence in research, scholarship,
and education by publishing worldwide in
Oxford New York
Auckland Cape Town Dar es Salaam Hong Kong Karachi
Kuala Lumpur Madrid Melbourne Mexico City Nairobi
New Delhi Shanghai Taipei Toronto
With offices in
Argentina Austria Brazil Chile Czech Republic France Greece
Guatemala Hungary Italy Japan Poland Portugal Singapore
South Korea Switzerland Thailand Turkey Ukraine Vietnam
Oxford is a registered trade mark of Oxford University Press
in the UK and in certain other countries
Published in the United States
by Oxford University Press Inc., New York

© Market House Books Ltd, 1983, 1986, 1990, 2004, 2008

The moral rights of the author have been asserted
Database right Oxford University Press (maker)

First edition 1983
Second edition 1986
Third edition 1990
Fourth edition 1996
Fifth edition 2004
Sixth edition 2008

All rights reserved. No part of this publication may be reproduced,
stored in a retrieval system, or transmitted in any form or by any means,
without the prior permission in writing of Oxford University Press,
or as expressly permitted by law, or under terms agreed with the appropriate
reprographics rights organization. Enquiries concerning reproduction
outside the scope of the above should be sent to the Rights Department,
Oxford University Press, at the address above

You must not circulate this book in any other binding or cover
and you must impose this same condition on any acquirer

British Library Cataloguing in Publication Data
Data available

Library of Congress Cataloging in Publication Data
Data available

Typeset by Market House Books Ltd.
Printed in Great Britain
on acid-free paper by
Clays Ltd, St Ives plc

ISBN 978–0–19–923401–1

10 9 8 7 6 5 4 3 2 1

referring to the internal storage of a computer that can be directly addressed by operating instructions. *See* MAIN MEMORY, CACHE, SEMICONDUCTOR MEMORY, MEMORY HIERARCHY, MEMORY MANAGEMENT.

memory card An *add-in card containing memory chips either directly mounted on the card or arranged in *SIMMS that plug into sockets on the card.

memory compaction (block compaction) Any of several methods used to relocate information blocks in main memory in order to maximize the available free space in the memory. *See also* STORAGE ALLOCATION.

memory cycle **1.** The complete sequence of events for a unit of memory to go from a quiescent state through a read and/or write phase and back to a quiescent state. **2.** The minimum length of time that is required between successive accesses (read or write) to a memory. *See also* CYCLE.

memory data register (MDR) A *register used for holding information (either program words or data words) that is in the process of being transferred from the memory to the central processor, or vice versa.

memory dump A representation, which can be read by a person, of the contents at some time of some part of the main memory of a computer system. A variety of representation formats might be employed, but typically these would all be relatively low-level – e.g. purely numeric or assembler-code format. A memory dump is normally taken for *postmortem purposes.

memory element A device that stores one item of information: if it has q stable states it is said to be *q-ary, and if $q = 2$ it is said to be binary. It is usually implemented electronically, sometimes with the assistance of the magnetic, optical, or acoustic properties of a storage medium. In practice, most memory elements are binary. In fast computer circuitry, the *flip-flop is the most common type of memory element.

Memory elements are employed specifically in computer memories and generally in *sequential circuits. A memory element is any smallest part of such a system that possesses more than one stable state. For example, a binary *shift register contains four flip-flops and has 16 states, but each of its four memory elements has only two states; a similar ternary shift register would have 81 states, but would still consist of four memory elements, each having three states.

memory fill An aid to program debugging in which every location in the memory is filled with a predetermined character before being overwritten by the incoming program.

memory guard A form of hardware *interlock used in some systems to control access to memory that is currently involved in a peripheral transfer. At the time of initiating the transfer the channel sets an indication that the buffer area is associated with the transfer; this indication is cleared by the channel on completion of the transfer. Any attempt to access the buffer area (other than by the channel) will suspend the process attempting to access the buffer until the transfer has been completed.

memory hierarchy For physically different kinds of *memory there are significant differences in the time to read or write the contents of a particular *location in memory, the amount of information that is read or written on a given occasion, the total volume of information that can be stored, and the unit costs of storing a given amount of information. To optimize its use and to achieve greater efficiency and economy, memory is organized in a hierarchy with the highest performance and in general the most expensive devices at the top, and with progressively lower performance and less costly devices in succeeding layers. The contents of a typical memory hierarchy, and the way in which data moves between adjacent layers, might be organized as follows.

1. **Register** – A single word held in each *register of the *processor; typically a word contains 4 bytes. This is sometimes not thought of as part of the hierarchy.
2. **Cache** – Groups of words within the *cache; typically a single group in the cache will hold 64 words (say 256 bytes), and there will be, say, 1024 such groups, giving a total cache of 256 Kbytes. Single words pass between the cache and registers within the processor. All transfers into and out of the cache are controlled entirely by hardware.
3. **Main memory** – Words within the main (*random-access) memory. On a very high performance system, groups of words corresponding to a group within the cache are transferred between the cache and the main memory in a single cycle of main memory.