UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PHISON ELECTRONICS CORPORATION,
Petitioner,

v.

VERVAIN, LLC,
Patent Owner.

PGR2025-00010
U.S. Patent No. 11,967,369

PATENT OWNER'S REQUEST FOR DISCRETIONARY DENIAL OF INSTITUTION

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EXHIBIT LIST

Exhibit No.	Description
2001	Declaration of Dr. Sunil Khatri
2002	[RESERVED]
2003	[RESERVED]
2004	[RESERVED]
2005	[RESERVED]
2006	*Vervain v. Western Digital Corp. et al.*, No. 6:21-cv-488-ADA, Dkt. 41 (W.D. Tex. Jan. 24, 2022) (Claim Construction Order)
2007	[RESERVED]
2008	[RESERVED]
2009	U.S. Patent Application Pub. No. 2011/0099460 ("Dusija")
2010	Highlighted Version of U.S. Patent No. 8,634,240 ("Gavens"), indicating which material from Gavens is also present in U.S. Patent Application Pub. No. 2011/0099460 ("Dusija")
2011	[RESERVED]
2012	[RESERVED]
2013	[RESERVED]
2014	[RESERVED]
2015	[RESERVED]
2016	[RESERVED]
2017	[RESERVED]
2018	*Vervain, LLC v. Phison Electronics Corporation*, No. 1:24-cv-259-ADA, Dkt. 16 (W.D. Tex. Jul. 15, 2024) (agreed scheduling order)

Exhibit No.	Description
2019	[RESERVED]
2020	[RESERVED]
2021	"Judge Albright Patent FAQ," https://www.txwd.uscourts.gov/for-attorneys/judge-albright-courtroom-faq/. Accessed December 18, 2024)
2022	[RESERVED]
2023	Judge Albright's Standing Order Governing Proceedings (OGP) 4.4—Patent Cases, Filed January 23, 2024.
2024	Excerpts from the Prosecution History of U.S. Patent No. 11,830,546
2025	U.S. Patent App. Pub. No. 2011/0096601 to Gavens et al. ("Gavens-601")
2026	[RESERVED]
2027	[RESERVED]
2028	[RESERVED]
2029	[RESERVED]
2030	[RESERVED]
2031	Preliminary Claim Constructions for *Vervain, LLC v. Phison Electronics Corporation*, No.1:24-cv-259-ADA and *Vervain, LLC v. Kingston Technology Company., et al*., No. 1:24-cv-254-ADA – email from Mr. Brown received on February 5, 2025.
2032	Markman Hearing Transcript dated February 6, 2025, for *Vervain, LLC v. Phison Electronics Corporation,* No. 1:24-cv-259-ADA and *Vervain, LLC v. Kingston Technology Company., et al.* No. 1:24-cv-254-ADA.

Exhibit No.	Description
2033	*Vervain v. Western Digital Corp. et al.*, No. 6:21-cv-00488-ADA, Dkt. 180 (W.D. Tex. Jul. 26, 2023) (Redacted Copy of Order on the Pending Motions and Motions *In Limine*).
2034	[RESERVED]
2035	[RESERVED]
2036	[RESERVED]
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2038	[RESERVED]
2039	*Phison Electronics Corp. v. Vervain, LLC*, PGR2024-00047, Paper 9 (P.T.A.B. Mar. 17, 2024) (Decision Denying Institution of Post-Grant Review of U.S. Patent No. 11,830,546)
2040	[RESERVED]
2041	*Phison Electronics Corp. v. Vervain, LLC*, PGR2024-00048, Paper 9 (P.T.A.B. April 28, 2025) (Decision Denying Institution of Post-Grant Review of U.S. Patent No. 11,854,612)
2042	Docket Sheet for *Vervain, LLC v. Phison Electronics Corporation*, No. 1:24-cv-259-ADA (W.D. Tex.) (accessed May 12, 2025)
2043	Phison's Final Invalidity Contentions served on February 28, 2025 in *Vervain, LLC v. Phison Electronics Corporation*, No. 1:24-cv-259-ADA (W.D. Tex.)
2044	"Interim Processes for PTAB Workload Management Memorandum," issued March 26, 2025, https://www.uspto.gov/sites/default/files/documents/InterimProcesses-PTABWorkloadMgmt-20250326.pdf. Accessed May 13, 2025.

I. INTRODUCTION

Pursuant to the "Interim Processes for PTAB Workload Management Memorandum" issued March 26, 2025 ("the *PTAB Memorandum*") and the Board's Notice Extending the Deadline for Discretionary Briefing dated April 14, 2025 (Paper 7), Patent Owner Vervain, LLC ("PO" or "Vervain") respectfully submits this brief requesting that the Director exercise her discretion to deny institution of the Petition for Post Grant Review (PGR) (Paper 2) of U.S. Patent No. 11,967,369 ("369 Patent" or "the Challenged Patent") filed by Phison Electronics Corporation ("Phison" or "Petitioner").

The Director should exercise her discretion and deny institution under 35 U.S.C. § 324(a)—instituting this Petition would require a considerable and inefficient use of the Board's resources. The parties are already litigating a parallel case in district court, which involves the Challenged Patent and seven others. The parallel case is well past its infancy. Before the institution decision is due in this PGR proceeding, the district court will have already held the *Markman* hearing, and the parties will have completed fact discovery and submitted expert reports. And trial in the district court case is scheduled for ***eight months before*** the final written decision deadline here. Furthermore, Petitioner advances overlapping invalidity grounds in district court but ***has not stipulated to any estoppel*** in the event this

Petition is instituted. The advanced parallel proceeding should proceed, and this Petition should be denied.

Further, the Petition is weak on the merits. The Petition includes four grounds of unpatentability challenging claims 1-10 ("Challenged Claims"), most of which have already been rejected by the district court or the Board. Revisiting those arguments now would unnecessarily burden the Board's resources. The first ground is a meritless challenge under 35 U.S.C. §§ 112(a), which was already been rejected by the Board in a decisions denying institution of a related PGR. *See* Ex. 2039 (denying institution of PGR2024-00047). The next two grounds include eleven cursory challenges under 35 U.S.C. §§ 112(a), and 112(b)—ten of these challenges have already been rejected by the Board in its decisions denying institution of related PGRs or by the district court in claim construction rulings. *See* Exs. 2031, 2032 (*Markman* hearing transcript), 2039, 2041 (denying institution of PGR2024-00048).

The third ground relies on a single-reference obviousness theory based on U.S. Patent No. 8,634,240 ("Gavens") (Ex. 1045)—a reference already considered by the USPTO, thus implicating 35 U.S.C. § 325(d). Moreover, the argument underlying Petitioner's Gavens ground was already rejected by the Board in its decisions denying institution of the related PGRs. *See* Exs. 2039, 2041. Specifically, the obviousness ground fails to reconcile key differences between the Challenged Claims and Gavens. The Challenged Claims require a data integrity test

performed by a controller based on data retained in random access volatile memory (RAM)—a feature that Gavens neither discloses nor suggests.

Accordingly, PO respectfully requests that the Director exercise her discretion to deny institution of the Petition.

II. BACKGROUND

A. The 369 Patent And The Vervain Patent Family

U.S. Patent No. 11,967,369 (the "Challenged Patent") belongs to a family of patents including U.S. Patent Nos. 8,891,298; 9,196,385; 9,997,240; 10,950,300; 11,830,546; 11,854,612; 11,967,369; and 11,967,370 (the "Vervain Patents"). These patents share the same specification and are continuations stemming from U.S. Patent No. 8,891,298.

The Vervain Patents, each entitled "Lifetime Mixed Level Non-Volatile Memory System," have effective filing dates of July 19, 2011. Ex. 1001, Cover. Dr. G. R. Mohan Rao is the sole named inventor of the Vervain Patents.

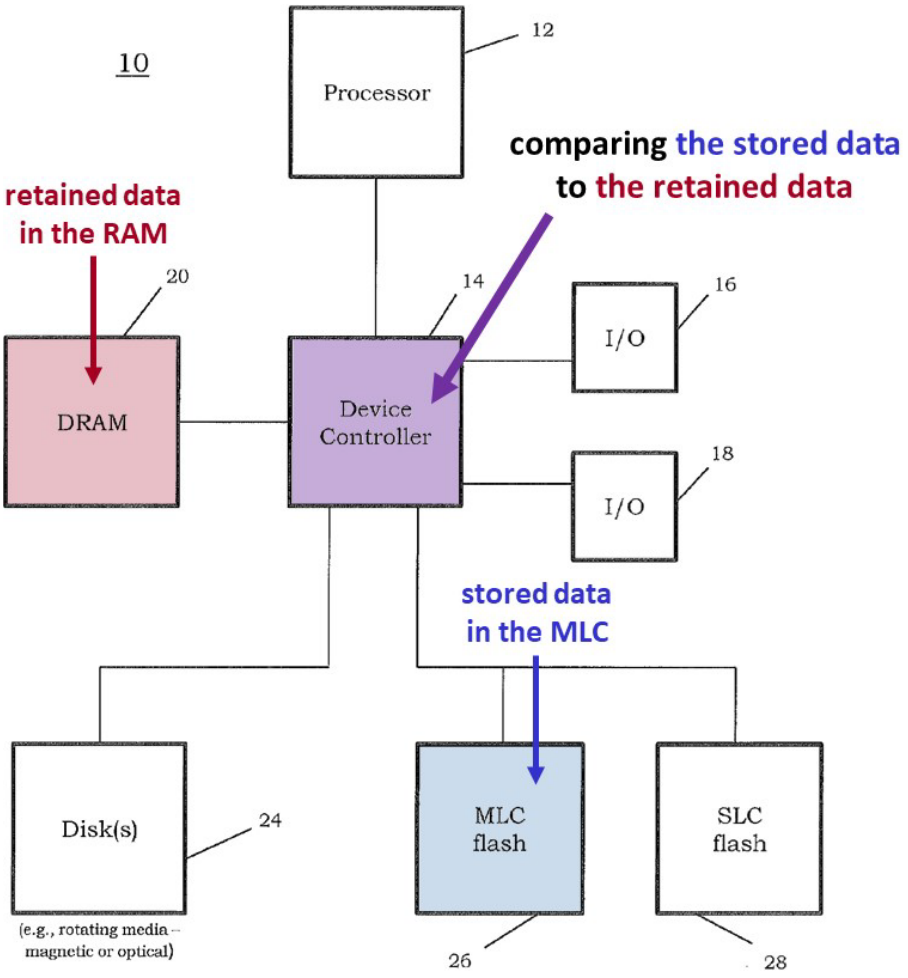
At a high level, the Vervain Patents describe a reliable flash memory storage system combining both single-level cell (SLC) and multi-level cell (MLC) non-

volatile memories.[1] Ex. 1001, Abstract; Ex. 2001, ¶37. SLC memory stores 1 bit per cell, and MLC memory stores more than 1 bit per cell. Ex. 1001, 2:11-17; Ex. 2001, ¶¶32-34. In general, SLC is faster and less prone to errors, but requires more space and power to store a given amount of data. Ex. 1001, 1:54-59.

The Vervain Patents describe a particular way of writing data to MLC and performing a data integrity test. The data integrity test checks the integrity of the data (*i.e.*, whether errors have occurred). The Vervain Patents explain that, if the data integrity test reveals a problem such as corrupt data, the data can be remapped to SLC (which is less error-prone) or other MLC blocks. Ex. 1001, 3:11-33, 5:57-6:61.

As seen in Figure 1 below, the Vervain Patents describe a controller (purple) that controls a dynamic random access memory (DRAM) (red).

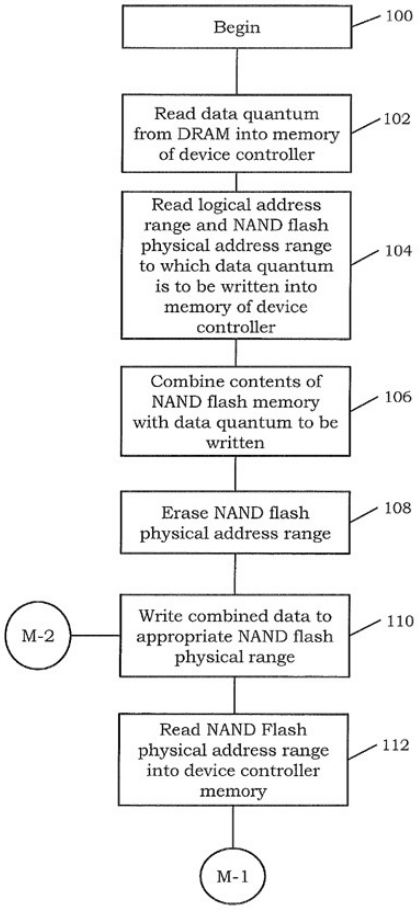
[1] Non-volatile memories can store information even after the system is powered off. Flash memory is a specific type of non-volatile memory, where data is stored in "blocks" of "pages." Ex. 1001, 2:50-57; Ex. 2001, ¶27.



Ex. 1001, Fig. 1 (annotations added), 5:30-31.

The DRAM is used during a write access operation to the MLC flash (highlighted blue). The data to be written to the MLC flash is maintained (or retained) in the DRAM. Ex. 1001, 5:55-57. If time permits, the controller performs a data integrity test on the data that was stored in the MLC. *Id.*, 5:57-60. If the stored data fails the data integrity test, the address range for the stored data is remapped to a new location (*e.g.*, the SLC flash). *Id.*, 5:60-5:63.

Figures 3A and 3B show in more detail how the DRAM and controller are used during the write access operation and data integrity test.



Id., Fig. 3A.

The write access operation begins at step 100. *Id*., 6:13-16. In step 102, the data to be written to the MLC is read from the DRAM into a controller memory. *Id*., 6:16-18. In step 104, the controller obtains the logical and physical address ranges for the data to be written to the MLC. *Id*., 6:18-21. In step 106, the controller combines the data from the DRAM with data from the MLC. *Id*., 6:21-23. In step 108, the controller erases the physical address range where the data is being written.

Id., 6:23-24. Finally, in step 110, the combined data is written to the MLC flash. *Id*., Fig. 3A (step 110), 6:24-26.

The data integrity test begins at the bottom of Figure 3A and continues to Figure 3B (below). In step 112, the data that was stored in the MLC ("the stored data") is read into the controller memory. *Id*., 6:26-28. In step 114, the stored data is compared to the data that was retained in the DRAM. *Id*., 6:29-34.

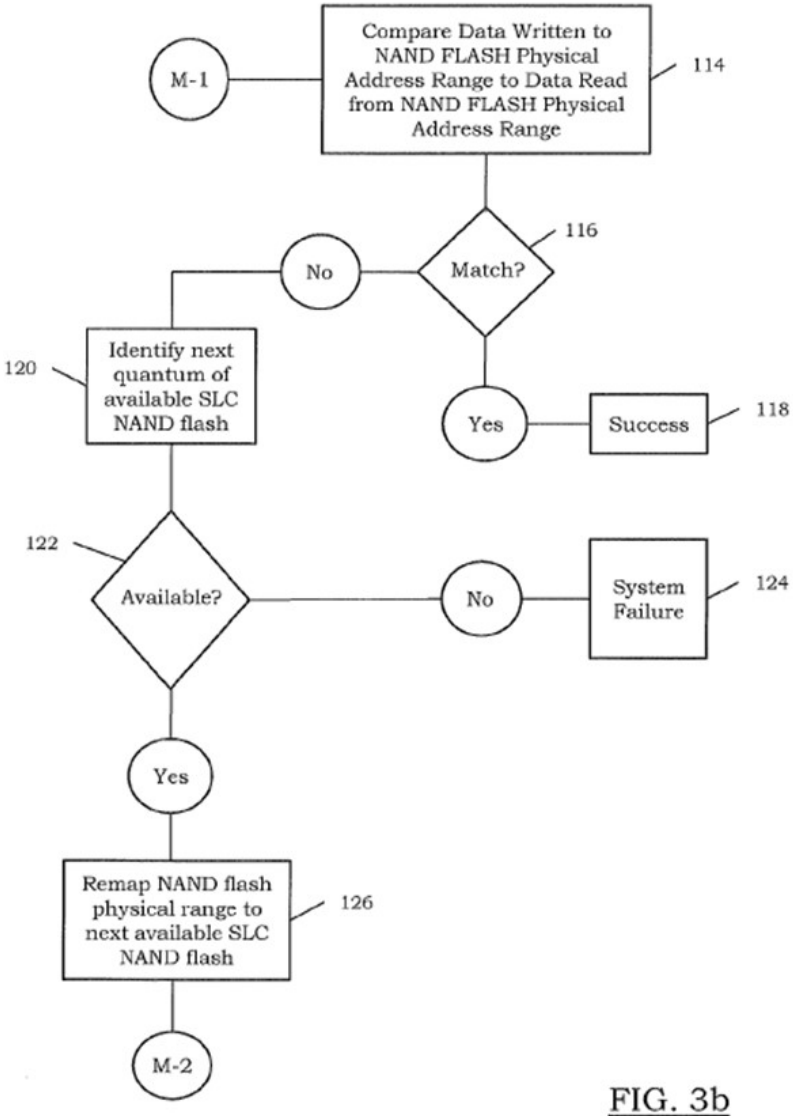


FIG. 3b

Id., Fig. 3B.

If there is a match, the data was successfully stored in the MLC. *Id*., 6:34-36. If not, the retained data is written to another location (*e.g*., SLC). *Id*., 6:36-40.

1. The Challenged Claims

Dr. Rao recognized that there were advantages in retaining data at the random access volatile memory (RAM) to assist with the data integrity test. Accordingly, data retained in RAM is a key feature of the invention claimed in the Challenged Patent.

The Challenged Patent includes one independent claim, Claim 1. Claim 1 is representative for purposes of this brief and requires a system for storing data comprising: (1) MLC non-volatile memory; (2) SLC non-volatile memory; and (3) a data integrity test performed at the controller based upon data retained in random access volatile memory (shown in red font below). The data retained at the RAM is particularly important to limitation [1f], and the "data integrity test" in [1g].

Claim 1	
[1Pre]	A memory system for storing data comprising:
[1a]	memory space containing logical and physical volatile memory space and nonvolatile memory space, wherein the logical and physical nonvolatile memory space includes both multi-level cell (MLC) logical and physical memory space and single level cell (SLC) logical and physical memory space;

[1b]	a bank of physical nonvolatile memory, including: [1b1] a plurality of physical MLC memory modules, each including at least one physical MLC nonvolatile memory element having a physical address within the physical MLC nonvolatile memory space that can be mapped to a logical address in the MLC logical nonvolatile memory space, and [1b2] at least one SLC memory module including at least one physical SLC nonvolatile memory element having a physical address within the physical SLC nonvolatile memory space that can be mapped into the SLC logical nonvolatile memory space;
[1c]	at least one random access volatile physical memory element that exists in the logical volatile memory space;
[1d]	at least one controller to operate physical memory elements and associated memory space for associated Write access operations to the physical memory elements and Read access operations from the physical memory elements, the controller having a controller memory associated therewith for storing received data therein;
[1e]	a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the physical memory elements;
[1f]	[1f1] the controller controlling access of the physical MLC and SLC nonvolatile memory elements and the random access volatile physical memory elements for storage of the received data therein as stored data, [1f2] the controller, in at least a Write access operation transferring the

	stored received data from the controller memory to a given one of the physical MLC nonvolatile memory elements in an associated physical MLC memory module, [1f3] operable to store the received data in the given one of the physical MLC nonvolatile memory elements as stored data and **retain such received data in the random access volatile physical memory element as retained data** associated with stored data;
[1g]	the controller [1g1] **performing a data integrity test** on stored data in the given one of the physical MLC nonvolatile memory elements in the associated one of the physical MLC memory modules after the at least a Write access operation performed thereon by [1g2] reading the stored data to the controller memory and [1g3] **comparing the stored data in the controller memory in the given one of the physical MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile physical memory element** by the controller during the Write access operation;
[1h]	wherein the address table maps logical addresses to physical addresses of the memory system, wherein the mapping is performed as necessitated by the memory system to maximize lifetime; and
[1i]	wherein a failure of the data integrity test performed on the stored data by the controller results in a remapping of logical address space to a different physical range of addresses in the physical address space and transfer of data corresponding to the retained data to those remapped physical addresses in the physical address space from those physical

	addresses in the physical address space determined to have failed the data integrity test.

B. Petitioner's IPR And PGR Filings

Petitioner filed requests for *inter partes* review and post grant review challenging each of the Vervain Patents—U.S. Patent Nos. 8,891,298 (IPR2025-00212); 9,196,385 (IPR2025-00213); 9,997,240 (IPR2025-00214); 10,950,300 (IPR2025-00215); 11,830,546 (PGR2024-00047); 11,854,612 (PGR2024-00048); 11,967,369 (PGR2025-00010); and 11,967,370 (PGR2025-00011).

The Board has already denied institution of two petitions on the merits—PGR2024-00047 and PGR2024-00048 ("the Denied PGRs"). *See* Exs. 2039, 2041. The Board issued detailed decisions denying institution, substantively rejecting each of Petitioner's grounds. *See generally id.*

The Board is expected to issue a decision on whether to institute IPR2025-00212 by June 26, 2025.

The Director is expected to decide by July 14, 2025, whether to exercise her discretion to deny institution of the five remaining petitions, including the present Petition. If the Director does not exercise her discretion, the Board is expected to decide whether to deny institution on the merits by August 14, 2025.

C. The Parallel District Court Litigation

On May 13, 2024, Patent Owner ("PO") filed an amended complaint against Phison asserting infringement of the Vervain Patents in *Vervain, LLC v. Phison Electronics Corporations*, No. 1:24-cv-259-ADA (W.D. Tex.) ("the Parallel Litigation"). *See* Ex. 1082 (First Amended Complaint, filed May 13, 2024); *see also* Ex. 2042 (docket sheet showing the original Complaint, filed March 8, 2024, which asserted infringement of the first six Vervain Patents).

The Parallel Litigation is well underway. The parties completed claim construction briefing, and the Court (with Judge Albright presiding) provided constructions for the disputed terms—all in PO's favor—at a *Markman* hearing on February 6, 2025. *See* Exs. 2031-2032. Fact discovery opened on December 9, 2024, and the parties exchanged final invalidity and infringement contentions on February 28, 2025. *See* Exs. 2018, 2037. The Petitioner then moved for leave to file amended final invalidity contentions on March 27, 2025, and PO moved for leave to file amended final infringement contentions on May 2, 2025. *See* Ex. 2042.

Further, the Parallel Litigation is rapidly approaching trial. Fact discovery closes on July 7, 2025, necessitating that the parties begin depositions in June. *See* Ex. 2018. Opening expert reports are due July 11, 2025, followed by summary judgment and *Daubert* motions on September 12. *See* Ex. 2018. ***Trial is scheduled to begin on December 15, 2025***. *See id.*

D. Prior Litigation Involving The Vervain Patents

Vervain previously asserted four of the Vervain Patents—U.S. Patent Nos. 8,891,298; 9,196,385; 9,997,240; and 10,950,300—against Western Digital and Micron in *Vervain, LLC v. Micron Technology, Inc. et al.*, No. 6:21-cv-487-ADA (W.D. Tex) and *Vervain, LLC v. Western Digital Corp et al.*, No. 6:21-cv-488-ADA (W.D. Tex.) ("the Prior Litigation"). In these cases, the Court held a *Markman* hearing and ruled on summary judgment motions, maintaining the validity of the Vervain Patents. *See, e.g.*, Exs. 2006 (Caim Construction Order, issued January 24, 2022), 2033 (Summary Judgment Order).

Further, in these cases, Micron filed IPRs against U.S. Patent Nos. 8,891,298; 9,196,385; 9,997,240; and 10,950,300 (*see* IPR2021-01547, -01548, -01549, and -01550). These IPRs were terminated prior to Final Written Decisions, following the parties' joint motions to terminate after reaching a settlement.

III. THE DIRECTOR SHOULD EXERCISE HER DISCRETION AND DENY INSTITUTION UNDER 35 U.S.C. § 324(a)

The Director should exercise her discretion and deny institution on all grounds because of the significant overlap with the Parallel Litigation, which is scheduled for trial well before a Final Written Decision would be expected here.

As shown below, the *Fintiv* factors all weigh in favor of denying institution under 35 U.S.C. § 324(a). *See NXP USA, Inc. v. Impinj, Inc.*, PGR2022-00005, Paper 18 at 7 (P.T.A.B. May 2, 2022) (weighing *Fintiv* factors and denying

institution under 35 U.S.C. § 324(a)); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) ("*Fintiv*").

A. Factor 1: The Parallel Litigation Has Not Been Stayed And Is Unlikely To Be Stayed Even If This Petition Is Instituted

This factor weighs against institution because a stay of the Parallel Litigation is highly unlikely. Petitioner has not sought a stay, and the Board's institution decision is expected by August 14, 2025. Given the timing and complexity of the Parallel Litigation, it is improbable that Judge Albright would grant a stay even if the Petition is instituted.

Particularly, August 14, 2025, is after the ***close*** of fact discovery (July 7, 2025), and after the parties serve opening (July 11, 2025) and rebuttal (August 8, 2025) expert reports. *See* Ex. 2018. Accordingly, the Court will have "expended significant resources," and would be unlikely to grant a stay. *See, e.g.*, *Sonrai Memory Ltd. v. LG Elecs. Inc.*, No. 6:21-cv-00168-ADA, 2022 WL 2307475, at *3 (W.D. Tex. June 27, 2022) (denying stay when fact discovery opened two weeks before the institution decision).

Further, in the Parallel Litigation, PO asserted ***eight patents*** against Petitioner Phison. *See* Ex. 1082, ¶2. Phison filed IPR or PGR petitions against each of these patents. But the Board has already denied institution on two of those petitions—PGR2024-00047 and PGR2024-00048. *See* Exs. 2039, 2041. In circumstances such as these, it is even more unlikely that the Court would grant a stay. *See Smart Mobile*

Techs. LLC v. Apple Inc., No. 6:21-cv-00603-ADA, 2023 WL 5051374, at *6 (W.D. Tex. Aug. 8, 2023) (denying stay based on instituted IPRs when institution was not granted on all asserted patents).

Thus, Factor 1 weighs against institution.

B. Factor 2: The Board Would Likely Issue A Final Written Decision Eight Months After Trial

This factor weighs against institution because trial is scheduled to begin eight months before the projected final written decision. Should the Director not exercise her discretion to deny institution, the Board is expected to decide whether to institute by August 14, 2025. Accordingly, the projected statutory deadline for a final written decision would be August 14, 2026—***eight months after the December 15, 2025, trial date***. *See* Ex. 2018. Judge Albright is highly unlikely to move this trial date, as he has a practice of "not mov[ing] the trial date except in extreme situations." Ex. 2021; *see also NXP USA*, PGR2022-00005, Paper 18 at 9 (weighing factor 2 in favor of discretionary denial when "the currently scheduled trial in the parallel proceeding is scheduled to begin over two months before our deadline to reach a final decision"); *Google LLC v. Cerence Operating Co.*, IPR2024-01465, 2025 WL 1182608, at *4 (P.T.A.B. Apr. 23, 2025) (weighing factor 2 in favor of discretionary denial when "the district court has set a trial date of October 6, 2025, which is almost seven months before the final written decision in this proceeding would be due in late April

2026" and "nothing in the…record indicates a trial in the District Court Litigation would not take place months before our deadline to reach a final decision").

C. Factor 3: The Court And Parties Have Invested Heavily In The Parallel Litigation

This factor weighs against institution because the parties and the Court have invested and will continue to invest significant resources in the Parallel Litigation. The Board weighs "the amount and type of work already completed in the parallel litigation by the court and the parties at the time of the institution decision." *Fintiv*, IPR2020-00019, Paper 11 at 9.

By the time the Board decides whether to institute this PGR in August 2025, the parties will have completed *Markman* briefing (Nov. 22, 2024); briefed a motion to dismiss (which the Court resolved on Dec. 2, 2024); exchanged final infringement and invalidity contentions (Feb. 28, 2025); moved to amend those contentions (Mar. 27, 2025 and May 2, 2025); completed fact discovery (closes July 7, 2025); exchanged opening expert reports (July 11, 2025); and exchanged rebuttal expert reports (Aug. 8, 2025). *See* Exs. 2018, 2037, 2042. In addition, the parties will have completed extensive document production and numerous fact and expert witness depositions.

Furthermore, the Court will have held the *Markman* hearing and issued its constructions (Feb. 6, 2025) and ruled on numerous discovery disputes. *See* Exs. 2031 (Court's preliminary claim constructions), 2032 (transcript for the February 6

Markman hearing, during which the Court adopted its preliminary constructions). At the *Markman* hearing, the Court already rejected most of the indefiniteness grounds raised in this Petition. *See* Ex. 2031; *infra* Section III.D (explaining the overlap between the indefiniteness arguments in the Parallel Litigation and this proceeding); *see also Fintiv*, Paper 11 at 10 ("[D]istrict court claim construction orders may indicate that the court and parties have invested sufficient time in the parallel proceeding to favor denial.")

Thus, the Court and the parties have invested and will continue to invest significant resources in the Parallel Litigation and, accordingly, this factor weighs against institution. *See NXP USA*, PGR2022-00005, Paper 18 at 9-10 (weighing factor 3 in favor of discretionary denial where the *Markman* hearing and the service of final infringement and invalidity contentions occurred before the Board's institution decision deadline); *Motorola Sols., Inc. v. Stellar, LLC*, IPR2024-01205, 2025 WL 947070, at *1 (P.T.A.B. Mar. 28, 2025) (Order Granting Director Review, Vacating the Decision Granting Institution, and Denying Institution of *Inter Partes* Review) (finding "factor 3 strongly favors discretionary denial" when "the parties had served extensive infringement and invalidity contentions, served opening and rebuttal expert reports, filed claim construction briefs, and conducted several depositions" and "[t]he court also had held a claim construction hearing and construed the disputed claim terms").

D. Factor 4: There Is Significant Overlap Between Issues Raised In This Petition And In The Parallel Litigation

This factor weighs against institution given the significant overlap between the Petition and the Parallel Litigation. The Parallel Litigation involves the same 369 Patent as this proceeding, along with seven additional patents. *See* Ex. 1082. Further, the Parallel Litigation already involves most of the grounds raised in the Petition. For example, the indefiniteness grounds raised in grounds 2.A through 2.E were already rejected by the Court during the *Markman* hearing. *See* Exs. 2031, 2032. The other grounds—including those related to patent eligibility, written description, and obviousness—have similarly been raised in Petitioner Phison's invalidity contentions in the Parallel Litigation.

Ground 1 § 101: Phison's invalidity contentions identify the same patent eligibility argument included in this Petition. *Compare* Petition, 29-32, 29 (arguing that the claimed "memory space" is "directed to an abstract idea") *with* Ex. 2043 (Petitioner Phison's invalidity contentions), 40-41 ("claims 1-18 of the '370 patent are invalid under 35 U.S.C. § 101 because they are directed to or recite the abstract idea of 'memory space(s).'").

Ground 2 § 112(a): Phison's invalidity contentions identify ***all five*** §112(a) challenges identified in the Petition—2.A through 2.E. Petition, 32-39 (including grounds 2.A through 2.E); *see* Ex. 2043 (Petitioner Phison's invalidity contentions), 20-21 ("memory space," ground 2.A), 19-20 ("memory element," ground 2.B), 24-

26 ("mapping…as necessitated by the system to maximize lifetime," ground 2.C), 26-27 (the "RAVM" and "controller memory" and their "respective relationships to stored and retained data," ground 2.D), and 36-38 ("at least one memory element" does not provide a "useful" system, ground 2.E).

Ground 3 § 112(b): Indefiniteness is an issue of claim construction. The parties already completed *Markman* briefing, and the Court construed the claims during a *Markman* hearing on February 6, 2025. *See* Exs. 2031, 2032. During the *Markman* hearing, the Court ***already rejected five of the six indefiniteness grounds included in the Petition***. *See* Ex. 2032 (*Markman* hearing transcript), 31:14-36:25 (ground 3.A, "memory space"), 41:25-43:7 (ground 3.B, "memory element"), 50:9-54:1 (ground 3.C, "mapping…as necessitated by the system to maximize lifetime"), 22:14-30:5 (ground 3.D, "controller" limited by functions), 37:1-42:1 (ground 3.E, "method steps in the context of a claim to a system").

Additionally, while the Court did not decide Petitioner's challenge alleging that it is "uncertain whether and when the recited comparison test [the "data integrity test"] is required to be performed" (ground 3.F), this is because, at the *Markman* hearing, Petitioner was instead arguing that "data integrity test" was ***not indefinite*** and should be narrowly construed. *See* Ex. 2031, 5 (including Petitioner's proposed construction for "data integrity test" in the Parallel Litigation).

Furthermore, while Petitioner's ground 3.F was not addressed at the *Markman* hearing, this was Petitioner's choice. Phison could have requested that the Court also consider whether this term was indefinite but chose not to do so. *See* Ex. 2023, 7 (permitting parties to seek "leave of Court" to request construction of additional terms). Even so, Phison ***identified ground 3.F in its invalidity contentions and could attempt to later raise it with the Court***. *See* Ex. 2043, 29-30 (ground 3.F).

Ground 4 § 103: The Parallel Litigation involves the same Gavens reference (U.S. Patent No. 8,634,240, Ex. 1045) that Petitioner relies on in ground 4. Gavens is the ***only primary reference*** identified for the 369 Patent in Phison's Invalidity Contentions. *See* Ex. 2043, 7. And Phison charted Gavens to the claims. *See id.* (referencing charts included in "Exhibit G").

Despite this significant overlap, ***Petitioner has not filed a Sotera stipulation or any other stipulation*** to mitigate concerns of duplicative efforts between the District Court and the Board, as well as any concerns regarding potentially conflicting decisions. *See Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 19 (P.T.A.B. Dec. 1, 2020). If this Petition is instituted, Petitioner would necessarily rely on its Gavens ground both before the Board and in the Parallel Litigation, including in its expert report and at trial. Further, during the *Markman* hearing, the District Court already decided most of the indefiniteness grounds

presented in the Petition—Petitioner now requests that the Board conflict with the Court's decisions with this PGR.

Thus, this factor weighs heavily against institution. *See NXP USA*, PGR2022-00005, Paper 18 at 11-12 (weighing factor 4 in favor of discretionary denial when the petitioner "d[id] not offer a stipulation" and "assert[ed] the same prior art in both proceedings").

E. Factor 5: The Parties Are The Same In Both Proceedings

The Petitioner and the defendant in the Parallel Litigation "are the same party," so "this factor weighs in favor of discretionary denial." *NXP USA*, PGR2022-00005, Paper 18 at 12.

F. Factor 6: Other Circumstances Weigh Against Institution

1. The Merits Of The Petition Are Weak[2]

The Petition includes ***thirteen*** cursory grounds that are difficult to decipher and weak on the merits. *See* Petition, Table of Contents (including one ground under 35 U.S.C §101, five grounds under 35 U.S.C. §112(a); six grounds under 35 U.S.C.

[2] Patent Owner also filed a "Preliminary Response On The Merits And Other Non-Discretionary Considerations" on May 14, 2025, which provides a more detailed explanation of the Petition's numerous substantive weaknesses.

§112(b); and one ground under 35 U.S.C. §103). Almost all the grounds have already been considered—and rejected—by the Board or the Western District.

Ground 1 § 101: The Board already rejected Petitioner's argument under §101—arguing that the claimed "memory space" is "directed to an abstract idea" (Petition, 29-32, 29)—in its decision denying institution of U.S. Patent No. 11,830,546. *See* Ex. 2039 (Board's decision denying institution of PGR2024-00047), 22-25, 23 ("[W]e understand 'memory space' as referencing physical memory rather than an abstract property."). Thus, this ground is weak on the merits.

Ground 2 § 112(a): The arguments underlying ***four out of five*** of Petitioner's §112(a) grounds have already been rejected by the Board in its decision denying institution of U.S. Patent No. 11,830,546. *See* Ex. 2039 (Board's decision denying institution of PGR2024-00047), 30-31 (rejecting the "memory space" written description argument, corresponding to Petitioner's ground 2.A), 31-32 (rejecting the "memory element" written description argument, corresponding to Petitioner's ground 2.B), 32-33 (rejecting the "mapping…as necessitated by the system to maximize lifetime," written description argument, corresponding to Petitioner's ground 2.C), 31-32 and 41-42 (rejecting the written description and enablement arguments for "at least one…memory element space," corresponding to Petitioner's ground 2.E). Petitioner copied the substance of its arguments for grounds 2.A through 2.C and 2.E from PGR2024-00047. *Compare* Petition, 32-39 *with*

PGR2024-00047, Paper 2 (petition), 31-37 (P.T.A.B. Aug. 27, 2024) (including substantively the same arguments as Petitioner's grounds 2.A through 2.C and 2.E).

The single remaining §112(a) ground (2.D, "RAVM, Controller Memory And Their Respective Relationships To Stored And Retained Data") is a conclusory challenge which is readily rebutted by the detailed description of the Vervain Patent's specification. *See* Ex. 2001 (expert declaration of Dr. Sunil Khatri, which is further referenced in PO's "Preliminary Response On The Merits And Other Non-Discretionary Considerations"), ¶¶67-70; *see also Deeper, UAB v. Vexilar, Inc.*, IPR2018-01310, Paper 7 at 41–43 (P.T.A.B. Jan. 24, 2019) (informative) (denying institution where the petitioner showed a reasonable likelihood of success on just 2 of 23 challenged claims). Indeed, Petitioner's disjointed argument for ground 2.D begins as an apparent "written description" challenge but ends with an unclear assertion that the claims "are not enabled." Petition, 36-37. And Petitioner's challenge ***includes no analysis of the Challenged Patent's specification itself***, instead citing only the claim language, and includes no analysis "under the *Wands* factors." *See Microbiotica, Limited v. Board of Regents, The University of Texas System*, PGR2023-00026, Paper 12 at 24, 27 (P.T.A.B. Nov. 21, 2023) (denying institution of written description grounds when petitioner "d[id] not provide sufficient analysis of the full disclosure of the [challenged] patent").

Finally, none of Petitioner's §112(a) arguments warrant consideration because Petitioner failed to present its grounds with adequate explanation and clarity. Ground 2.A spans only four sentences, and ground 2.B spans only two sentences. Petition, 31-32, 35; *see also see Microbiotica*, PGR2023-00026, Paper 12 at 24, 27. Further, as explained above, for ground 2.D, Petitioner does not even make clear whether it is challenging written description, enablement, or both. *See* Petition, 36-37. Petitioner's grounds have not been presented with the requisite particularity and fail to provide an explanation of the significance of the evidence; accordingly, these grounds are without merit and do not warrant further review by the Board. *See* 37 C.F.R. § 42.22(a)(2); 35 U.S.C. § 312(a)(3).

Ground 3 § 112(b): In the Parallel Litigation, as explained above in Section III.D, the Court ***already rejected five of six*** indefiniteness grounds repeated in this Petition, instead construing the challenged claim terms to have their plain and ordinary meanings. *See* Exs. 2031, 2032.

Furthermore, the Board rejected ***all six*** of Petitioner's §112(b) arguments in its decision denying institution of PGR2024-00047. *See* Ex. 2039, 56-57 (rejecting Petitioner's argument for ground 3.A: "we agree with Patent Owner that an ordinarily skilled artisan would understand 'memory space' as describing where data is stored"); 57-58 (rejecting Petitioner's argument for ground 3.B: "we agree with Patent Owner that the term 'memory element' has a 'broad but understood' meaning

to an ordinarily skilled artisan"); 58-59 (rejecting Petitioner's argument for ground 3.C, where Petitioner argued that "mapping…as necessitated by the system to maximize lifetime" is indefinite); 59-61, 59 (rejecting Petitioner's argument for ground 3.D: "we agree with Patent Owner that the term 'controller'…refers to a known class of structures"); 61-62 (rejecting Petitioner's argument for ground 3.E); 62 (rejecting Petitioner's argument for ground 3.F); *see also* Ex. 2006, 7 (earlier litigation, not involving the Challenged Patent but involving its parent patents, in which the court also determined that that term identified in ground 3.C is not indefinite).

Thus, all of Petitioner's §112(b) arguments ***have already been rejected on the merits*** by the District Court or the Board. There is no reason for the Board to revisit these arguments again here.

Finally—like the §112(a) challenges—many of Petitioner's §112(b) challenges are similarly cursory, lacking the required particularity and failing to provide adequate explanation or evidentiary support to warrant the Board's review. For example, grounds 3.A and 3.B each consist of only three sentences. Petition, 39-40.

Ground 3 § 103: Petitioner presents a single-reference obviousness ground based on Gavens, U.S. Patent No. 8,634,240 (Ex. 1045). As preliminary matter, this ground is weak on the merits because it fails to provide a clear mapping to the prior

art and omits even a basic obviousness analysis to support its conclusory assertions about what a person of ordinary skill ("POSA") would have "understood." Notwithstanding, Petitioner's ground—to the extent it can be understood—relies on modifications to Gavens that a POSA would have never made and that cannot be supported. Indeed, the Board already considered a similar argument, which it rejected in denying institution of PGR2024-00047 and PGR2024-00048. *See* Exs. 2039, 2041.

The merits of Petitioner's Gavens ground are facially weak. Strikingly, in its argument for limitation [1c], Petitioner ambiguously cites distinct disclosure from ***six different references***: Gavens itself, along with tertiary references Gorobets 912 (Ex. 1049), Paley 180 (Ex. 1051), Harari (Ex. 1057), and Gorobets PCT (Ex. 1058)—which Gavens allegedly incorporates by reference—and Moshayedi (Ex. 1043), which is unrelated to Gavens. *See* Petition, 52-54. Petitioner, however, fails to clearly map the distinct teachings of these references to what is claimed, for example to identify what it contends maps to the "random access volatile physical memory element" (RAM) of limitation [1c]. *See id.* In effect, Petitioner's ground asks the Board to pick and choose between distinct elements from different disclosures; thus, Petitioner has not demonstrated with particularity how limitation [1c] maps to the prior art, as required by 35 U.S.C. § 312(a)(3). *See also Captioncall, LLC v. Ultratec, Inc.*, IPR2020-01215, 2021 WL 278381, at *7 (P.T.A.B. Jan. 27,

2021) (denying institution when petitioner relied on "distinct" embodiments from a reference and another reference that was incorporated by reference, explaining that "[a]nticipation requires all elements arranged as in the claim without the need to pick and choose elements from different disclosures"); *Masimo Corp. v. Apple Inc.*, IPR2023-00745, Paper 44 (final written decision), 36 (P.T.A.B. Oct. 15, 2024) (determining that the challenged claim is not unpatentable, explaining: "In essence, Petitioner invites the Board to piece together a single theory that meets all claim elements from these disparate theories that each require distinct structures….") (citing *Amazon.com, Inc., et al. v. Avago Technologies General IP (Singapore) PTE. LTD.*, IPR2017-01112, Paper 11, at 13 (P.T.A.B. Aug. 23, 2017) ("Petitioner is inviting us to assume the role of archeologist of the record, which invitation we decline.")); *Nearmap US, Inc. v. Eagle View Technologies, Inc.*, IPR2024-00716, Paper 9, 18 (P.T.A.B. Oct. 9, 2024) (denying institution of *inter partes* review, explaining that "[t]he question before us is not whether we could come up with a way to understand how the asserted prior art could render the challenge claims unpatentable, but rather did Petitioner provide the arguments and evidence to show that the challenged claims are unpatentable."); *Netflix, Inc. v. DivX, LLC*, 84 F.4th 1371, 1379 (Fed. Cir. 2023) ("While the Board should review a petition holistically, it is not obligated to cobble together assertions from different sections of a petition

or citations of various exhibits in order to infer every possible permutation of a petitioner's argument." (cleaned up)).

Furthermore, Petitioner repeatedly relies on what it contends a "POSITA would…understand" and what would have been "the POSITA understanding" but fails to provide the requisite obviousness analysis. *See, e.g.*, Petition, 53 (limitation [1c]), 60 (limitation [1f]). For example, for limitation [1f], Petitioner appears to rely on a "cache" taught by Gavens and conclusory asserts that this "cache" would be "***assumed***" to be implemented in RAM. Petition, 60 (citing Ex. 1045 (Gavens), 16:46-49). Petitioner then appears to further assume that this "cache" retains data in RAM (Petitioner ambiguously refers to a "common on-controller or associated external RAVM [(RAM)] (or both)") for use in the data integrity test, as required by limitation [1f]. Petition, 60. Petitioner, however, fails to provide the requisite obviousness analysis to support its misinterpretation of Gavens. *See* Ex. 2001, ¶¶133-165 (providing, along with PO's Preliminary Response On The Merits filed concurrently with this brief, a detailed description of the technical weaknesses in Petitioner's argument, including how Gavens *teaches away* from a RAM-based cache located in the controller).

For example, Petitioner does not explain what aspect of the claim limitation is missing in Gavens and, correspondingly, does not explain what from Gavens must be modified to arrive at the claim language. And Petitioner also does not explain

whether any of the allegedly incorporated references' RAM mentioned elsewhere in the Petition[3] is being used to modify Gavens's system, and why or how a POSA would have been motivated to make any modification. Petitioner fails to perform a proper obviousness analysis, which requires, among other things, ascertaining the "differences between the prior art and the claims at issue." *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966); *see also In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) ("Whether a rejection is based on combining disclosures from multiple references, combining multiple embodiments from a single reference, or selecting from large lists of elements in a single reference, there must be a motivation to make the combination and a reasonable expectation that such a combination would be successful, otherwise a skilled artisan would not arrive at the claimed combination."). The Petition's obviousness analysis is insufficient and must be rejected.

Petitioner made the same error in its reliance on Gavens in PGR2024-00047 and PGR2024-00048, which the Board noted in denying institution of those petitions on the merits. The Board agreed with PO's arguments and determined that Gavens

[3] For example, in its ground for limitation [1f], Petitioner also mentions Paley 180 (Petition, 59) and, as discussed above, Petitioner provides a scattershot citation to numerous tertiary references related to RAM with its arguments for limitation [1c].

does not teach a system that relies on *any* RAM, let alone a RAM-based cache that retains data for use in a data integrity test, as Petitioner appears to contend here. *See* Ex. 2041, 42 (decision denying institution of PGR2024-00048, finding: "Gavens's invention is directed specifically to non-volatile memory" and "a [POSA] would [not] have found Gavens to teach or suggest [a memory system] that includes RAM."); Ex. 2039, 76 (decision denying institution of PGR2024-00047, where the Board determined that "Gavens does not disclose 'random access volatile memory' according to claim 1, e.g. in a 'system' with, among other things, a 'controller' and a 'bank of nonvolatile memory'").

Furthermore, the Board also already determined that Petitioner's failure to provide the requisite obviousness analysis—for example, to explain how and why a POSA would have misinterpreted Gavens—is fatal to its ground. *See, e.g.*, Ex. 2041, 43 ("As Patent owner correctly notes, 'Petitioner…does not state whether Gorobets's 'RAM' is being used to modify Gavens's system, and why a POSA would have made any modification.'"); Ex. 2039, 71, 76 ("Petitioner does not explain how the teachings of Gorobets [912] and Paley 'combine with the cited teachings of Gavens' to yield" a claim limitation requiring "comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the ***retained data that was associated with the stored data in the random access volatile memory***" (emphasis added)).

Accordingly, the Petition's weak merits—which have already been rejected by the Board and Western District—weigh heavily against institution. *See also* Ex. 2044, 2 (stating that "The strength of the unpatentability challenge" should be considered in determining whether to discretionarily deny a petition). Most of Petitioner's challenges "ha[ve] already been adjudicated" and the Board should not expend its resources to revisit these arguments here. Ex. 2044, 2 (noting that, in evaluating whether to exercise discretion to deny institution, the Director should consider "[w]hether the PTAB or another forum has already adjudicated the validity or patentability of the challenged patent claims").

2. The Petition Relies Heavily On Expert Testimony

"The extent of the petition's reliance on expert testimony" should also be considered in assessing whether to exercise discretion to deny institution. Ex. 2044, 2. This Petition is heavily reliant on expert testimony. Petitioner's 35 U.S.C. §§101, 112(a), and 112(b) grounds (twelve of the thirteen grounds in the Petition) rely primarily on the opinions of their expert—Dr. Sechen. *See generally* Petition, 29-46.

And Petitioner's 35 U.S.C. §103 ground—based solely on "Gavens ***in view of POSITA Knowledge***"—likewise relies heavily on expert testimony to establish what constitutes the relevant knowledge of a POSITA and how a POSITA would have

artificially reconstructed Gavens to fit the language of the Challenged Claims. *See generally* Petition, 46-71.

Therefore, Petitioner's heavy reliance on expert testimony underscores that these arguments are more appropriately resolved in the Parallel Litigation—further supporting discretionary denial.

3. The Challenged Patent Belongs To A Family Of Patents With Settled Expectations

The "[s]ettled expectations of the parties, such as the length of time the claims have been in force" should also be considered in assessing whether to exercise discretion to deny institution. Ex. 2044, 2. Here, the first four Vervain Patents—parent to the 369 Patent—were successfully litigated in the Prior Litigation. *See supra* Sections II.A and II.D. This family of patents, which claims priority to ***2011***, embodies the inventions of a single inventor, Dr. G. R. Mohan Rao. The longstanding nature of these patents and the settled expectations surrounding Dr. Rao's inventions further support discretionary denial.

4. Instituting This Petition Would Be An Inefficient Use Of The Board's Resources

The Petition asserts thirteen cursory grounds of questionable merit, including one under 35 U.S.C. §101, five under 35 U.S.C. §112(a) and six under 35 U.S.C. §112(b). For example, grounds III.A ("memory space") and III.B ("memory element") are addressed in just ***three*** sentences. *See* Petition, 39-40. If instituted,

the Board would be obligated to evaluate and issue a final written decision on ***all*** these deficient grounds, requiring unnecessary expenditure of resources. The Petition's scattershot presentation of weak challenges thus further supports discretionary denial under 35 U.S.C. §324(a). *See Chevron Oronite Co. v. Infineum USA L.P.*, IPR2018-00923, Paper 9 at 10–11 (P.T.A.B. Nov. 7, 2018) (informative); *Deeper, UAB v. Vexilar, Inc.*, IPR2018-01310, Paper 7 at 41–43 (P.T.A.B. Jan. 24, 2019) (informative) (denying institution where the petitioner showed a reasonable likelihood of success on just 2 of 23 challenged claims); *Samsung Electronics America, Inc. et al. v. Collision Communications, Inc.*, IPR2024-01247, Paper 14, 21-22 (P.T.A.B. Feb. 7, 2025) (denying institution where the petitioner failed to show a reasonable likelihood of success for 16 of 18 challenged claims).

5. Instituting This Petition Would Unnecessarily Burden The Board's Resources

Finally, Petitioner filed eight separate petitions challenging the eight patents asserted in the Parallel Litigation. The Board has already denied institution of two of those petitions. *See* Exs. 2039, 2041. As a result, only six petitions remain pending. The purpose of discretionary denial is to "allay[] concerns about inefficiency and duplication of efforts." *Fintiv*, Paper 11 at 6. Instituting six separate PGRs/IPRs to address only some of the issues currently being addressed in the single, mature district court case would be inefficient and an unnecessary expenditure of the Board's resources.

This inefficiency is further illustrated by the mismatch in scope: while Petitioner challenged 10 claims in this Petition, PO is currently asserting only 8 claims from the Challenged Patent in the Parallel Litigation. And the number of asserted claims may decrease when the parties "meet and confer…to discuss significantly narrowing the number of claims asserted" by June 6, 2025. Ex. 2018. Requiring the Board to adjudicate at least two additional claims not asserted in the Parallel Litigation would impose an unnecessary burden—especially given that the validity of the asserted claims will already be resolved at trial, as explained above.

Thus, all *Fintiv* factors—including multiple additional circumstances—weigh against institution, and the Director should exercise her discretion to deny institution under 35 U.S.C. § 324(a).

IV. THE DIRECTOR SHOULD EXERCISE HER DISCRETION AND DENY INSTUTION UNDER 35 U.S.C. § 325(d)

The Board has discretion to deny institution when "the same or substantially the same prior art or arguments previously were presented to the Office." 35 U.S.C. § 325(d). To determine whether a petition should be denied under 35 U.S.C. § 325(d), the Board applies the following two-part framework:

> (1) whether the same or substantially same art previously was presented to the Office or whether the same or substantially the same arguments were presented to the Office; and

(2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of the challenged claims.

Advanced Bionics, LLC v. Med-El Electromedizinishe Geräte GmbH, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020) (precedential). The *Advanced Bionics* framework considers the non-exclusive factors set forth in *Becton, Dickinson*. *Id.* at 7 (citing *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017)).

Here, both parts of the *Advanced Bionics* framework are met for Petitioner's obviousness ground. Gavens—Petitioner's primary reference in its single-reference §103 ground—is not new to the Patent Office. And Petitioner does not even attempt to show that the Office "erred in a manner material to…patentability." *Id.* Petitioner never mentions §325(d). Thus, this ground should be discretionarily denied institution under 35 U.S.C. §325(d).

A. *Advanced Bionics* Part I – The Examiner Considered The Same Prior Art And Substantially The Same Arguments During Prosecution

During prosecution of the Challenged Patent, the Applicant submitted U.S. Patent App. Pub. No. 2011/0096601 (the publication leading to Petitioner's Gavens patent) (Ex. 2025) to the Examiner, who certified its review. *See* Ex. 1001, Cover at 2 (listing U.S. Patent App. Pub. No. 2011/0096601). Therefore, Part I of the *Advanced Bionics* framework is met. *See, e.g.*, *Advance Medical Designs, Inc. v.*

Corbin Clinical Resources, LLC, PGR2023-00041, Paper 12 at 24-25 (P.T.A.B. Jan. 23, 2024) (finding Part I met when a prior art reference was "submitted in an IDS").

But this is not a situation where Gavens was cited only in an IDS. During prosecution of U.S. Patent No. 11,830,546 ("546 Patent")—of which the Challenged Patent is a continuation[4]—the Examiner considered another reference, U.S. Patent App. Pub. No. 2011/0099460 ("Dusija"), of which Gavens is a continuation-in-part. *See* Ex. 2009. Gavens and Dusija are not only substantially the same—they are practically identical. *See* Ex. 2010 (annotated copy of Gavens including highlights to indicate material also present in Dusija). Figures 1 through 22C of Gavens and Dusija are identical. *See id.* And, other than non-substantive updates, Gavens's Detailed Description up to 24:33 is also identical. *See id.*

The Examiner thoroughly considered arguments based on Dusija during the 546 Patent's prosecution. The Examiner relied on Dusija in multiple rejections, and discussions about Dusija span multiple pages of the prosecution history. *See* Ex. 2024 (546 Patent prosecution history), 50-61 (Applicant including a comprehensive discussion of Dusija and explaining how it is different from the pending claims), 80-84 (Examiner relying on Dusija in an obviousness rejection of the claims), 115-117

[4] The Challenged Patent is a continuation of the 546 Patent; accordingly, these patents share the same specification. *See also supra* Section II.A.

(Applicant again explaining why Dusija does not teach the pending claims), 131-135 (Examiner relying on Dusija in another rejection), 162 (prior to allowance, Applicant again explaining why Dusija is deficient). Notably, the Applicant explained in detail how Dusija does not teach using data retained in volatile memory for a data integrity test in the manner required by claim 1 of the Challenged Patent. *See* Ex. 2024, 50-61.

Furthermore, Dusija was central to numerous IPRs previously filed against family members of the Challenged Patent. Particularly, Micron previously filed IPR2021-01547, IPR2021-01548, IPR 2021-01549, and IPR2021-01550 against four patents of which the Challenged Patent is a continuation. Each of these IPRs rely on Dusija in its grounds. The Applicant submitted materials from these IPRs to the Examiner, and the Examiner certified that they reviewed them. *See* Ex. 1001, Cover at 4-5 (including in the "References Cited" over sixty submissions from these IPRs). Having extensively considered Dusija, the Examiner allowed the Challenged Patent.

Thus, the Petition relies on the same prior art (Gavens, cited in an IDS) and substantially the same arguments (based on Dusija, which was referenced extensively during prosecution of the 546 Patent) that were presented to the Office, and *Advanced Bionics* Part I is met.

B. *Advanced Bionics* Part II – The Examiner Made No Material Error

Petitioner fails to address the clear issues under § 325(d), likely because it cannot rebut them. *See Nexus Pharmaceuticals, LLC v. Exela Pharma Sciences, LLC*, PGR2024-00016, Paper 9 at 27 (P.T.A.B. Aug. 8, 2024) (finding petitioner did "not sufficiently establish error, let alone material error by the Office" when "neither the [p]etition nor the [r]eply addresse[d]" the issue). Still, the Examiner made no material error during prosecution of the Challenged Patent.

Petitioner's single-reference obviousness ground does not rely on any teachings in Gavens that are unique to that reference and not also disclosed in Dusija. *See Advance Medical*, PGR2023-00041, Paper 12 at 21 (explaining that "the extent to which additional evidence and facts presented in the petition warrant reconsideration of the prior art or arguments" is considered as part of Part II of the *Advanced Bionics* framework). Accordingly, the Petition does not rely on any portion of Gavens that is even arguably "new." Thus, Petitioner relies on a continuation-in-part of a reference that the Examiner already thoroughly considered, cites overlapping disclosure, and fails to address this issue in its Petition.

Therefore, Petitioner cannot show material error on part of the Patent Office because neither Gavens nor Dusija, nor any other tertiary reference Petitioner cites, renders the claims of the Challenged Patent obvious. As explained above and in Patent Owner's Preliminary Response on the Merits filed in parallel with this brief,

the Petition contains multiple clear errors, and Gavens is completely different from the Challenged Patent's claims. *See also* Ex. 2001, ¶¶89-141 (providing a detailed description of the deficiencies in Petitioner's obviousness ground).

Therefore, both parts of the *Advanced Bionics* framework are met, and the Director should exercise her discretion to deny institution of Petitioner's obviousness ground under 35 U.S.C. § 325(d).

V. CONCLUSION

For the foregoing reasons, the Director should exercise her discretion to deny institution.

Date: May 14, 2025

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner hereby certifies that the word count for the foregoing **PATENT OWNER'S REQUEST FOR DISCRETIONARY DENIAL OF INSTITUTION** is 8,065 words, which is within the limit set in 37 C.F.R. §42.24(b)(1). This word count does not include the table of contents, table of authorities, exhibit list, certificate of word count, and certificate of service. This word count was prepared using Microsoft Word.

Date: May 14, 2025

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CERTIFICATE OF SERVICE

I hereby certify, in accordance with 37 C.F.R. § 42.205, that the foregoing **PATENT OWNER'S REQUEST FOR DISCRETIONARY DENIAL OF INSTITUTION** was served via electronic mail on May 14, 2025 on the following counsel of record for Petitioner:

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