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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	VRVN.01.01.US5
	Application Number	
Title of Invention	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	G.R. Mohan		Rao	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Allen	TX	US

Mailing Address of Inventor:

Address 1	1611 Willingham Drive
Address 2	

City	State/Province	Postal Code	Country
Allen	TX	75013	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. — Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	40672		
Email Address	patents@naifeh.com	Add Email	Remove Email

Application Information:

Title of the Invention	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM		
Attorney Docket Number	VRVN.01.01.US5	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	5	**Suggested Figure for Publication (if any)**	

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Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	40672		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	16006299	2018-06-12

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	VRVN.01.01.US5
	Application Number	
Title of Invention	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16006299	Continuation of	14950553	2015-11-24	9997240	2018-06-12
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14950553	Continuation of	14525411	2014-10-28	9196385	2015-11-24
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14525411	Division of	13455267	2012-04-25	8891298	2014-11-18
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
13455267	Claims benefit of provisional	61509257	2011-07-19		

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

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☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	VRVN.01.01.US5
	Application Number	
Title of Invention	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	VRVN.01.01.US5
	Application Number	
Title of Invention	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	VERVAIN, LLC

Mailing Address Information For Applicant:

Address 1	7424 Mason Dells Drive		
Address 2			
City	Dallas	**State/Province**	TX
Country	US	Postal Code	75230
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	VRVN.01.01.US5
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Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

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Signature:

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NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Timothy Bliss, Reg No. 50925/			Date (YYYY-MM-DD)	2021-03-16
First Name	Timothy	Last Name	Bliss	Registration Number	50925

Additional Signature may be generated within this form by selecting the Add button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	VRVN.01.01.US5
	Application Number	
Title of Invention	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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PGR2025-00010

LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application No. 16/006,299, filed June 11, 2018, entitled LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM, which is a continuation of U.S. Patent Application No. 14/950,553, filed November 24, 2015, entitled LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM, which a continuation of U.S. Patent Application No. 14/525,411, filed October 28, 2014, entitled LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM, which is a divisional of U.S. Patent Application No. 13/455,267, filed April 25, 2012, LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM, which claims the benefit of U.S. Provisional Application No. 61/509,257, filed July 19, 2011, entitled LIFETIME MIXED LEVEL NAND FLASH SYSTEM, the disclosures of which are hereby incorporated by reference in their entirety.

[0002] This application is also related to U.S. Patent Application No. 12/256,362, filed October 22, 2008, entitled NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES, and U.S. Patent Application No. 12/915,177, filed October 29, 2010, entitled NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES, the disclosures of which are hereby incorporated by reference in their entirety.

TECHNICAL FIELD

[0003] This application relates to a system and method for providing reliable storage through the use of non-volatile memories and, more particularly, to a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use of a combination of single-level cell (SLC) and multi-level cell (MLC) NAND flash storage without substantially raising the cost of the NAND

flash storage system. The memory in a total non-volatile memory system may contain some SRAM (static random-access memory), DRAM (dynamic RAM), RRAM (resistive RAM), PCM (phase change memory), MAGRAM (magnetic random-access memory), NAND flash, and one or more HDDs (hard disk drives) when storage of the order of several terabytes is required. The SLC non-volatile memory can be flash, PCM, RRAM, MAGRAM or any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash, and it provides for data access speeds that are faster than that of MLC flash or rotating storage media (e.g., HDDs).

BACKGROUND

[0004] Non-volatile memories provide long-term storage of data. More particularly, non-volatile memories can retain the stored data even when not powered. Magnetic (rotating) hard disk drives (HDD) dominate this storage medium due to lower cost compared to solid state disks (SSD). Optical (rotating) disks, tape drives and others have a smaller role in long-term storage systems. SSDs are preferred for their superior performance (fast access time), mechanical reliability and ruggedness, and portability. Flash memory, more specifically NAND flash, is the dominant SSD medium today.

[0005] RRAM, PCM, MAGRAM and others, wi11likely play a larger role in the future, each of them having their own advantages and disadvantages. They may ultimately replace flash memories, initially for use as a "write buffer" and later to replace "SLC flash" and "MLC flash." MLC NAND flash is a flash memory technology using multiple levels per cell to allow more bits to be stored using the same number of transistors. In SLC NAND flash technology, each cell can exist in one of two states, storing one bit of information per cell. Most MLC NAND flash memory has four possible states per cell, so it can store two bits of information per cell.

[0006] These semiconductor technology driven "flash alternatives," i.e., RRAM, PCM, MAGRAM and others, have several advantages over any (SLC or MLC) flash because they: 1) allow data to be written over existing data (without prior erase of existing data), 2) allow for an erase of individual bytes or pages (instead of having to

erase an entire block), and 3) possess superior endurance (1,000,000 write-erase cycles compared to typical 100,000 cycles for SLC flash and less than 10,000 cycles for MLC flash).

[0007] HDDs have several platters. Each platter contains 250-5,000 tracks (concentric circles). Each track contains 64 to 256 sectors. Each sector contains 512 bytes of data and has a unique "physical (memory) address." A plurality of sectors is typically combined to form a "logical block" having a unique "logical address." This logical address is the address at which the logical block of physical sectors appears to reside from the perspective of an executing application program. The size of each logical block and its logical address (and/or address ranges/boundaries) is optimized for the particular operating system (OS) and software applications executed by the host processor. A computer OS organizes data as "files." Each file may be located (stored) in either a single logical block or a plurality of logical blocks, and therefore, the location of files typically traverses the boundaries of individual (physical) sectors. Sometimes, a plurality of files has to be combined and/ or modified, which poses an enormous challenge for the memory controller device of a non-volatile memory system.

[0008] SSDs are slowly encroaching on the HDD space and the vast majority of NAND flash in enterprise servers utilizes a SLC architecture, which further comprises a NAND flash controller and a flash translation layer (FTL). NAND flash devices are generally fragmented into a number of identically sized blocks, each of which is further segmented into some number of pages. It should be noted that asymmetrical block sizes, as well as page sizes, are also acceptable within a device or a module containing devices. For example, a block may comprise 32 to 64 pages, each of which incorporates 2 - 4 Kbit of memory. In addition, the process of writing data to a NAND flash memory device is complicated by the fact that, during normal operation of, for example, single-level storage (SLC) , erased bits (usually all bits in a block with the value of ‘1’) can only be changed to the opposite state (usually ‘0’) once before the entire block must be erased. Blocks can only be erased in their entirety, and, when erased, are usually written to ‘1’ bits. However, if an erased block is already there, and if

the addresses (block, page, etc.) are allowed, data can be written immediately; if not, a block has to be erased before it can be written to.

[0009] FTL is the driver that works in conjunction with an existing operating system (or, in some embedded applications, as the operating system) to make linear flash memory appear to the system like a disk drive, i.e., it emulates a HDD. This is achieved by creating "virtual" small blocks of data, or sectors, out of flash's large erase blocks and managing data on the flash so that it appears to be "write in place" when in fact it is being stored in different locations in the flash. FTL further manages the flash so that there are clean/ erased places to store data.

[0010] Given the limited number of writes that individual blocks within flash devices can tolerate, wear leveling algorithms are used within the flash devices (as firmware commonly known as FTL or managed by a controller) to attempt to ensure that "hot" blocks, i.e., blocks that are frequently written, are not rendered unusable much faster than other blocks. This task is usually performed within a flash translation layer. In most cases, the controller maintains a lookup table to translate the memory array physical block address (PBA) to the logical block address (LBA) used by the host system. The controller's wear-leveling algorithm determines which physical block to use each time data is programmed, eliminating the relevance of the physical location of data and enabling data to be stored anywhere within the memory array and thus prolonging the service life of the flash memory. Depending on the wear-leveling method used, the controller typically either writes to the available erased block with the lowest erase count (dynamic wear leveling); or it selects an available target block with the lowest overall erase count, erases the block if necessary, writes new data to the block, and ensures that blocks of static data are moved when their block erase count is below a certain threshold (static wear leveling).

[0011] MLC NAND flash SSDs are slowly replacing and/ or coexisting with SLC NAND flash in newer SSD systems. MLC allows a single cell to store multiple bits, and accordingly, to assume more than two values; i.e., ‘0’ or ‘1’. Most MLC NAND flash architectures allow up to four (4) values per cell; i.e., ‘00’, ‘01’, ‘10’, or ‘11’. Generally,

MLC NAND flash enjoys greater density than SLC NAND flash, at the cost of a decrease in access speed and lifetime (endurance). It should be noted, however, that even SLC NAND flash has a considerably lower lifetime (endurance) than rotating magnetic media (e.g., HDDs), being able to withstand only between 50,000 and 100,000 writes, and MLC NAND flash has a much lower lifetime (endurance) than SLC NAND flash, being able to withstand only between 3,000 and 10,000 writes. As is well known in the art, any "write" or "program" to a block in NAND flash (floating gate) requires an "erase" (of a block) before "write."

[0012] Despite its limitations, there are a number of applications that lend themselves to the use of MLC flash. Generally, MLC flash is used in applications where data is read many times (but written few times) and physical size is an issue. For example, flash memory cards for use in digital cameras would be a good application of MLC flash, as MLC can provide higher density memory at lower cost than SLC memory.

[0013] When a non-volatile storage system combines HDD, SLC and MLC (setting aside volatile memory for buffering, caching etc) in a single (hybrid) system, new improvements and solutions are required to manage the methods of writing data optimally for improved life time (endurance) of flash memory. Accordingly, various embodiments of a NAND flash storage system that provides long lifetime (endurance) storage at low cost are described herein.

[0014] The following description is presented to enable one of ordinary skill in the art to make and use the disclosure and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present disclosure is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

SUMMARY

[0015] According to one embodiment of the present disclosure, there is provided a system for storing data which comprises at least one MLC nonvolatile memory module (hereinafter referred to as "MLC module") and at least one SLC non-volatile memory module (hereinafter referred to as "SLC module"), each module comprises a plurality of individually erasable blocks. The data storage system according to one embodiment of the present disclosure further comprises a controller for controlling both the at least one MLC module and the at least one SLC module. In particular, the controller maintains an address map comprising a list of individual logical address ranges each of which maps to a similar range of physical addresses within either the at least one MLC module or the at least one SLC module. After each write to (flash) memory, the controller conducts a data integrity check to ensure that the data was written correctly. When the data was not written correctly, the controller modifies the table so that the range of addresses on which the write failed is remapped to the next available range of physical addresses within the at least one SLC module. The SLC module can be (NAND) flash, PCM, RRAM, MAGRAM or any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash, and it provides for data access speeds that are faster than that of MLC flash or rotating storage media (e.g., HDDs).

[0016] According to another embodiment of the present disclosure, there is provided a system for storing data which comprises a controller that is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The present disclosure will be more fully understood by reference to the following detailed description of one or more preferred embodiments when read in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout the views and in which:

[0018] FIG. 1 is a block diagram of a computer system incorporating one embodiment of the present disclosure;

[0019] FIGS. 2A and 2B are drawings depicting a translation table/address map in accordance with one embodiment of the present disclosure;

[0020] FIGS. 3A and 3B are a flow chart illustrating an exemplary method for use in implementing one embodiment of the present disclosure; and

[0021] FIG. 4 is a block diagram depicting one embodiment of the present disclosure for implementation within a NAND flash module.

DETAILED DESCRIPTION

[0022] The present disclosure is directed to the reliable storage of data in read and write memory, and, in particular, to the reliable storage of data in non-volatile memory, such as, for example, NAND flash. Generally, and in particular regard to NAND flash memory, two separate banks of NAND flash are maintained by a controller. One bank contains economical MLC NAND flash, while a second bank contains high endurance SLC NAND flash. The controller conducts a data integrity test after every write. If a particular address range fails a data integrity test, the address range is remapped from MLC NAND flash to SLC NAND flash. As the SLC NAND flash is used to boost the lifetime (endurance) of the storage system, it can be considerably lesser in amount than the MLC NAND flash. For example, a system may set SLC NAND flash equal to 12.5% or 25% of MLC NAND flash (total non-volatile memory storage space=MLC+SLC).

[0023] Turning to the Figures and to FIG. 1 in particular, a computer system 10 depicting one embodiment of the present disclosure is shown. A processor 12 is coupled to a device controller 14, such as a chipset, using a data link well known in the art, such as a parallel bus or packet-based link. The device controller 14 provides interface functions to the processor 12. In some computer systems, the device controller 14 may be an integral part of the (host) processor 12. The device controller 14 provides a number of input/output ports 16 and 18, such as, for example, serial ports (e.g., USB ports and Firewire ports) and network ports (e.g., Ethernet ports and 802.11 "Wi-Fi" ports). The device controller 14 may also control a bank of, for example, DRAM 20. In addition, the device controller 14 controls access to one or more disks 24, such as, for example, a rotating magnetic disk, or an optical disk, as well as two or more types of NAND flash memory. One type of NAND flash memory is a MLC NAND flash memory module 26. Another type of NAND flash memory is a SLC NAND flash memory module 28.

[0024] The device controller 14 maintains a translation table/address map which may include address translations for all devices in the computer system. Nonetheless, the discussion in the present disclosure will be limited only to NAND flash memory modules. In particular, the device controller 14 maintains a translation table that maps logical computer system addresses to physical addresses in each one of the MLC- and SLC-NAND flash memory modules 26 and 28, respectively. As MLC flash memory is less expensive than SLC flash memory, on a cost per bit basis, the translation table will initially map all logical NAND flash addresses to the MLC NAND flash memory module 26. The address ranges within the translation table will assume some minimum quantum, such as, for example, one block, although a smaller size, such as one page could be used, if the NAND flash has the capability of erasing the smaller size quantum.

[0025] A "read-modify-write" scheme is used to write data to the NAND flash. Data to be written to NAND flash is maintained in DRAM 20. After each write to an address within a particular address range, the device controller 14 will—as time permits—perform a read on the address range to ensure the integrity of the written data. If a data

integrity test fails, the address range is remapped from the MLC NAND flash memory module 26 to the next available address range in the SLC NAND flash memory module 28.

[0026] FIGS. 2A and 2B illustrate one embodiment of a translation table/address map of the present disclosure. In Figure. 2A, a list of logical address ranges (R0-RN) is translated to physical address ranges. As illustrated, all of the logical address ranges are translated to blocks on the MLC NAND flash memory module 26. However, through the application of a data integrity verification check (explained in more detail below) it is determined that, for example, address range R2 corresponds to failed quanta of data stored in block 2 of the MLC NAND flash memory module 26. FIG. 2B shows the quanta of data which failed the data integrity verification check (see FIG. 2A) remapped to the next available range of physical addresses within the SLC NAND flash memory module 28, in this example, SLC/block 0.

[0027] FIGS. 3A and 3B are a flow chart illustrating a method for utilizing a NAND flash memory system incorporating one embodiment of the present disclosure. The method begins in a step 100, when a command to write a quantum of data stored in DRAM to a particular location in NAND flash memory is received. In step 102, the quantum of data is read from DRAM into memory within the device controller (which acts as the memory controller). In step 104, both the logical address range and the NAND flash physical address range to which the quantum of data is to be written, is read into memory of the device controller. In step 106, the quantum of data to be written is combined with the contents of the NAND flash memory. In step 108, the NAND flash physical address range to be written is erased. In step 110, the combined data is written to the appropriate NAND flash physical address range. In step 112 the NAND flash physical address range that was written in step 110 is read into device controller memory.

[0028] The flowchart continues in FIG. 3B. In step 114 the NAND flash physical address range that was read into device controller memory is compared with the retained data representing the combination of the previous contents of the physical

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address range and the quantum of data to be written. In step 116, if the retained data matches the newly stored data in the NAND flash memory, the write was a success, and the method exits in step 118. However, if the retained data does not match the newly stored data in the NAND flash memory, the method executes step 120, which identifies the next quantum of available SLC NAND flash memory addresses. In step 122, a check is made to determine if additional SLC NAND flash memory is available, and, if not, the NAND flash memory system is marked as failed, prompting a system alert step 124. However, if additional SLC NAND flash memory is available, the failed NAND flash physical address range is remapped to the next available quantum of SLC NAND flash memory in step 126. Execution then returns to step 110, where the write is repeated.

[0029] Another application of one embodiment of the present disclosure, not depicted in any of the drawings, is to allocate "hot" blocks; i.e., those blocks that receive frequent writes, into the SLC NAND flash memory module 28, while allocating "cold" blocks; i.e., those blocks that only receive infrequent writes, into the MLC NAND flash memory module 26. This could be accomplished within the device controller 14 described above, which could simply maintain a count of those blocks that are accessed (written to) most frequently, and, on a periodic basis, such as, for example, every 1000 writes, or every 10,000 writes, transfer the contents of those blocks into the SLC NAND flash memory module 28.

[0030] FIG. 4 depicts another embodiment of the present disclosure. The embodiment is entirely resident within a NAND flash module 50. In particular, a standard NAND flash interface 52 is managed by flash translation layer (FTL) logic 54. The flash translation layer (FTL) 54 manages two NAND flash memory banks 56 and 58, whereby memory bank 56 comprises a plurality of MLC NAND flash memory modules 60a and a plurality of SLC NAND flash memory modules 62a. Memory bank 58 comprises a plurality of MLC NAND flash memory modules 60b and a plurality of SLC NAND flash memory modules 62b.

[0031] This embodiment of the present disclosure could function similarly to the system level embodiment discussed earlier with reference to FIGS 1-3B, but the control functions, such as maintenance of the translation table/address map (FIGS. 2A and 2B), could be conducted within the flash translation layer (FTL) 54 instead of in a device controller 14.

[0032] Embodiments of the present disclosure relate to a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use of a combination of multi-level cell (MLC) and single-level cell (SLC) NAND flash storage. The above description is presented to enable one of ordinary skill in the art to make and use the disclosure and is provided in the context of a patent application and its requirements. While this disclosure contains descriptions with reference to certain illustrative aspects, it will be understood that these descriptions shall not be construed in a limiting sense. Rather, various changes and modifications can be made to the illustrative embodiments without departing from the true spirit, central characteristics and scope of the disclosure, including those combinations of features that are individually disclosed or claimed herein. Furthermore, it will be appreciated that any such changes and modifications will be recognized by those skilled in the art as an equivalent to one or more elements of the following claims, and shall be covered by such claims to the fullest extent permitted by law.

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WHAT IS CLAIMED IS:

1. A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element;

at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements; and

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories.

2. The system of Claim 1, wherein the memory elements are a module, standalone device, or multi-chip package.

3. The system of Claim 1, wherein at least one of the volatile or nonvolatile memories are embedded in the at least one controller.

4. The system of Claim 1, wherein the nonvolatile memory is flash memory.

5. The system of Claim 1, wherein the nonvolatile memory is phase-change memory.

6. The system of Claim 1, wherein the nonvolatile memory is magnetic random access memory.

7. The system of Claim 1, wherein the volatile memory is dynamic random access memory.

8. The system of Claim 1, wherein the volatile memory is static random access memory.

9. The system of Claim 1, wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD).

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ABSTRACT

A flash controller for managing at least one MLC non-volatile memory module and at least one SLC non-volatile memory module. The flash controller is adapted to determine if a range of addresses listed by an entry and mapped to said at least one MLC non-volatile memory module fails a data integrity test. In the event of such a failure, the controller remaps said entry to an equivalent range of addresses of said at least one SLC non-volatile memory module. The flash controller is further adapted to determine which of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and allocating those blocks that receive frequent writes to the SLC non-volatile memory module and those blocks that receive infrequent writes to the MLC non-volatile memory module.

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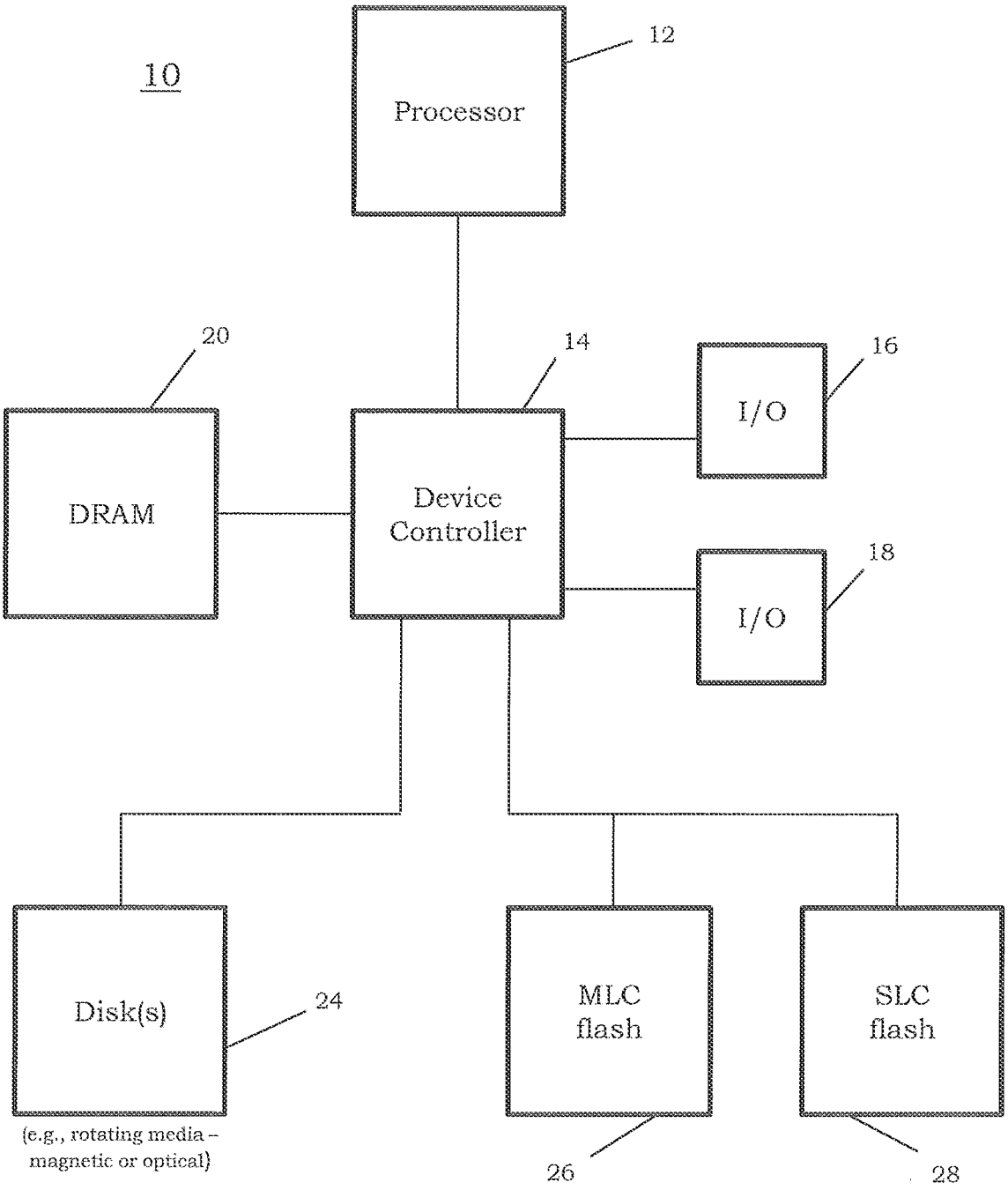

10
Processor
12
20
14
16
DRAM
Device Controller
I/O
18
I/O
Disk(s)
24
(e.g., rotating media – magnetic or optical)
MLC flash
SLC flash
26
28

FIG. 1

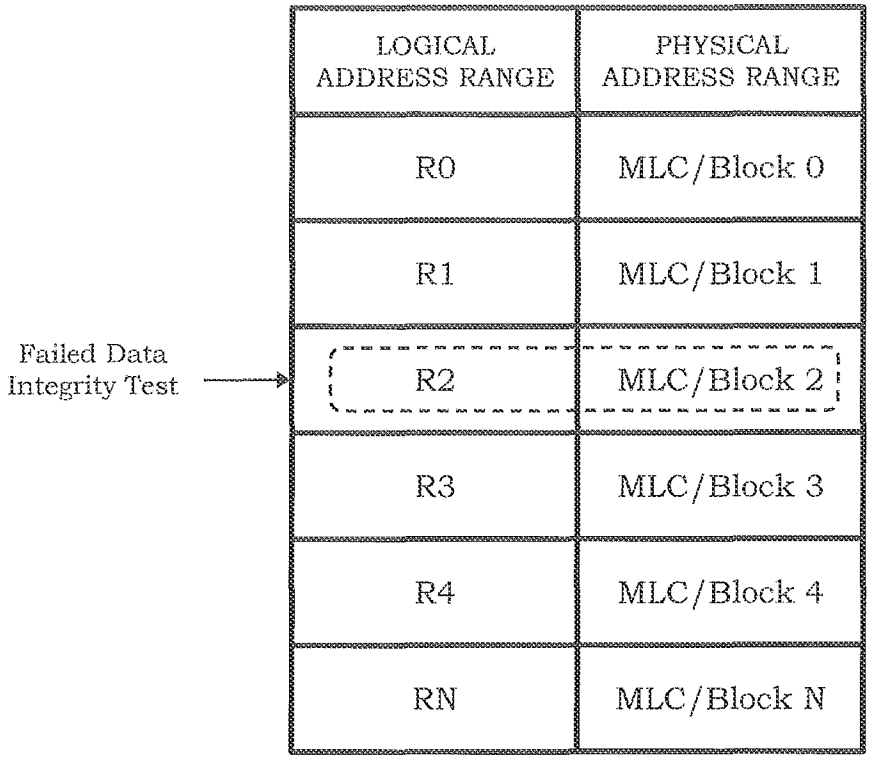

LOGICAL ADDRESS RANGE
PHYSICAL ADDRESS RANGE
R0
MLC/Block 0
R1
MLC/Block 1
Failed Data Integrity Test
R2
MLC/Block 2
R3
MLC/Block 3
R4
MLC/Block 4
RN
MLC/Block N

FIG. 2A

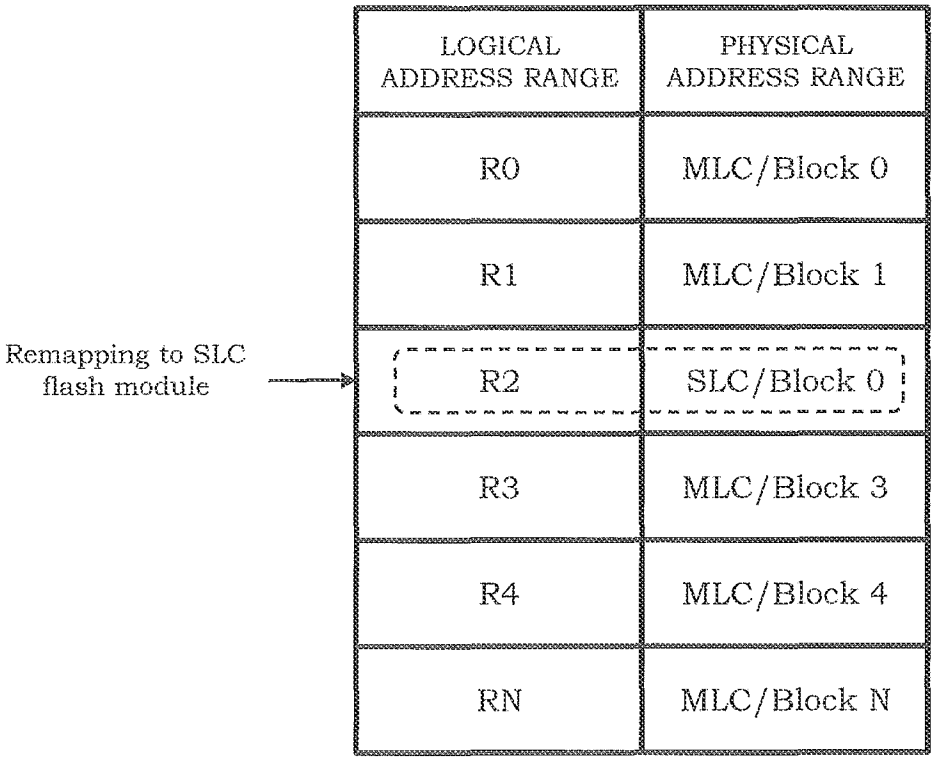

LOGICAL ADDRESS RANGE
PHYSICAL ADDRESS RANGE
R0
MLC/Block 0
R1
MLC/Block 1
Remapping to SLC flash module
R2
SLC/Block 0
R3
MLC/Block 3
R4
MLC/Block 4
RN
MLC/Block N

FIG. 2B

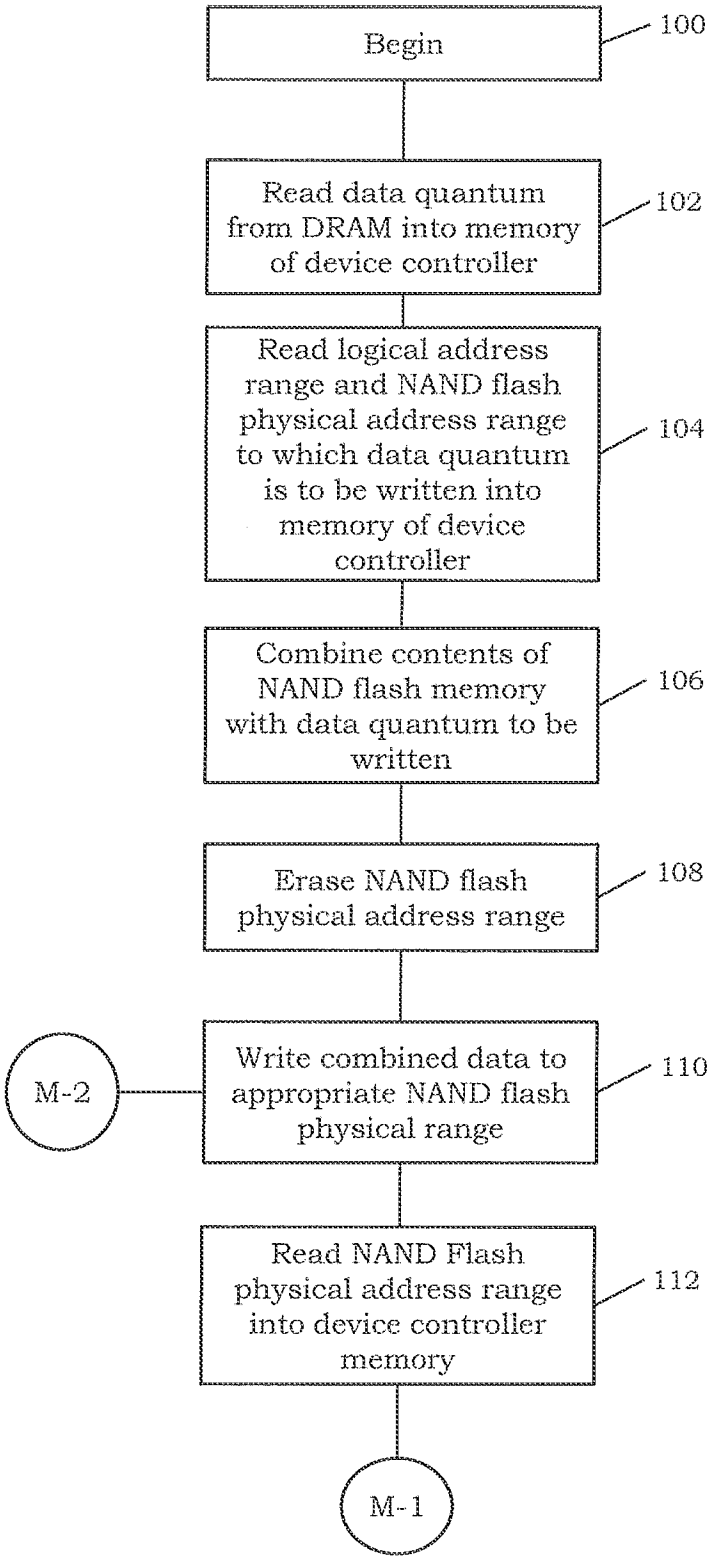

Begin
100
Read data quantum from DRAM into memory of device controller
102
Read logical address range and NAND flash physical address range to which data quantum is to be written into memory of device controller
104
Combine contents of NAND flash memory with data quantum to be written
106
Erase NAND flash physical address range
108
M-2
Write combined data to appropriate NAND flash physical range
110
Read NAND Flash physical address range into device controller memory
112
M-1

FIG. 3A

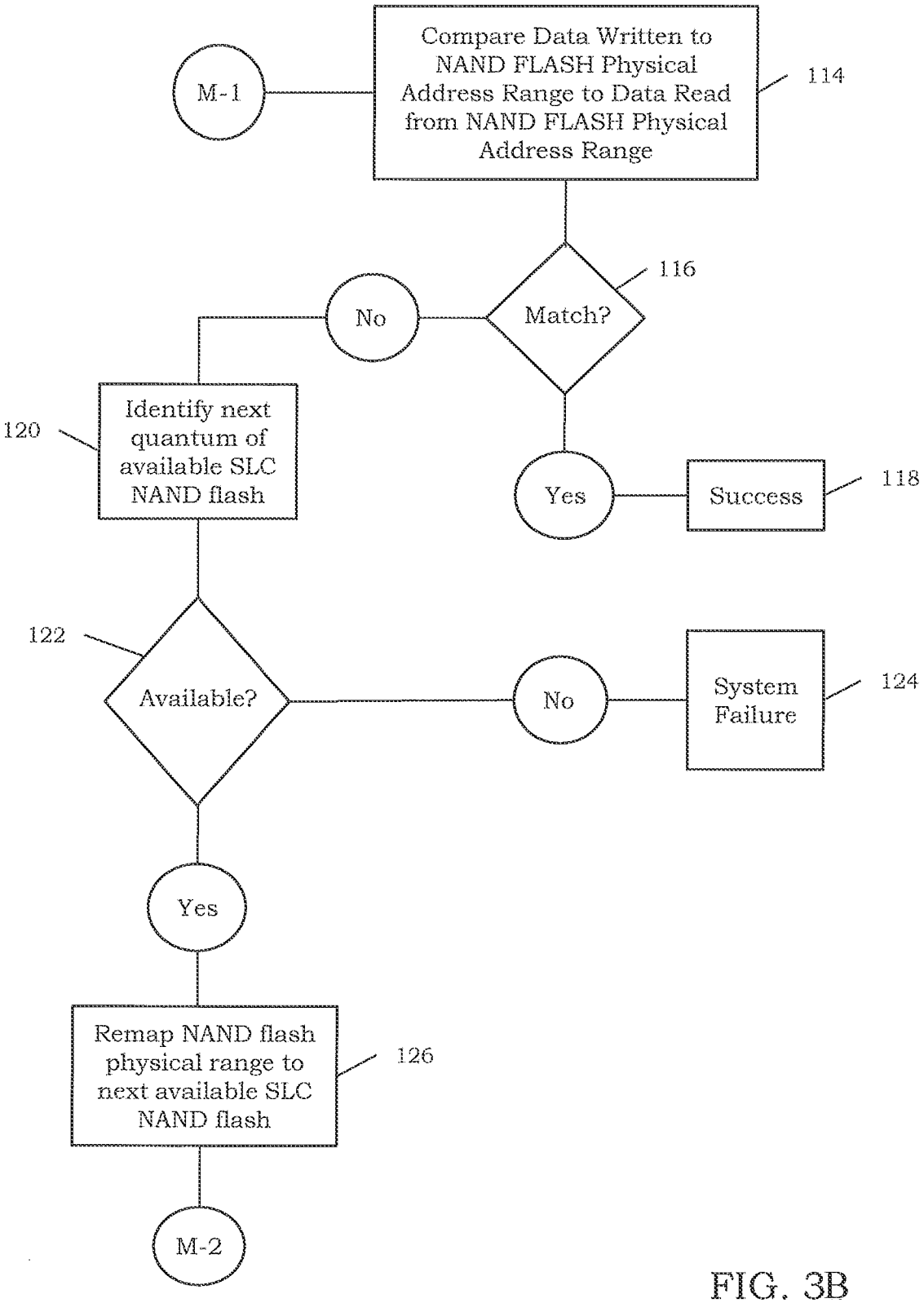

M-1
Compare Data Written to NAND FLASH Physical Address Range to Data Read from NAND FLASH Physical Address Range
114
Match?
116
No
Yes
Success
118
Identify next quantum of available SLC NAND flash
120
Available?
122
No
System Failure
124
Yes
Remap NAND flash physical range to next available SLC NAND flash
126
M-2

FIG. 3B

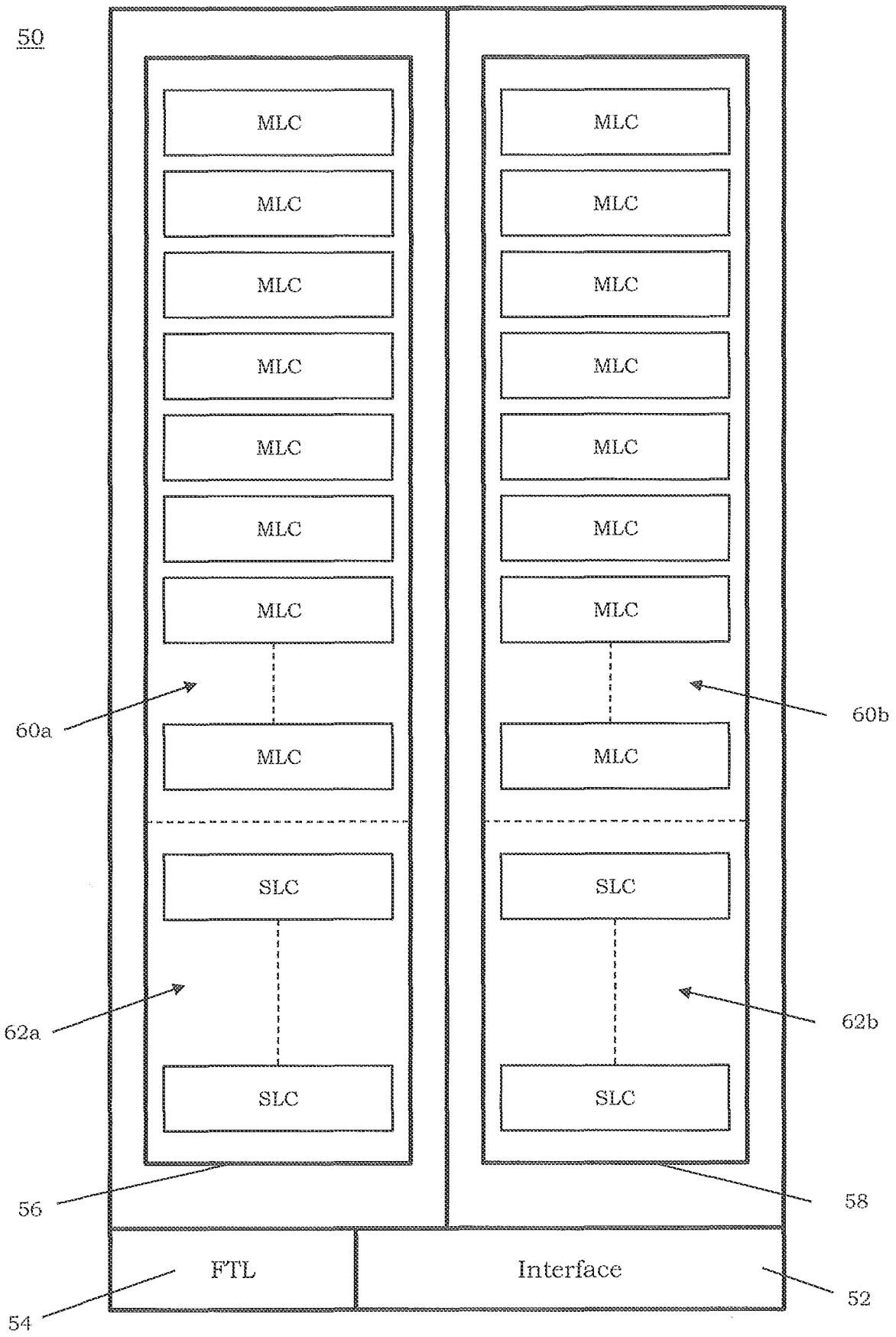

50
MLC
MLC
MLC
MLC
MLC
MLC
MLC
MLC
MLC
MLC
MLC
MLC
MLC
MLC
MLC
MLC
60a
60b
SLC
SLC
SLC
SLC
62a
62b
56
58
FTL
Interface
54
52

FIG. 4

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/203,385	03/16/2021	G.R. Mohan Rao	VRVN60-35360	6508

25883 7590 02/08/2022

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DALLAS, TX 75380

EXAMINER	
HIDALGO, FERNANDO N	

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
02/08/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPdocketing@munckwilson.com
admin@dalpat.com
eofficeaction@appcoll.com

Office Action Summary	Application No. 17/203,385	Applicant(s) Rao, G.R. Mohan	
	Examiner FERNANDO N HIDALGO	Art Unit 2827	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 3/16/2021.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-9 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-9 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 3/16/2021 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Examiner's Note

The examiner has cited particular passages including column and line numbers, paragraphs as designated numerically and/or figures as designated numerically in the references as applied to the claims below for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claims, other passages, paragraphs and figures of any and all cited prior art references may apply as well. It is respectfully requested from the applicant, in preparing an eventual response, to fully consider the context of the passages, paragraphs and figures as taught by the prior art and/or cited by the examiner while including in such consideration the cited prior art references in their entirety as potentially teaching all or part of the claimed invention. MPEP 2141.02 VI: "**PRIOR ART MUST BE CONSIDERED IN ITS ENTIRETY, INCLUDING DISCLOSURES THAT TEACH AWAY FROM THE CLAIMS**." MPEP 2123 (I): "**PATENTS ARE RELEVANT AS PRIOR ART FOR ALL THEY CONTAIN**."

Additionally, in an effort to provide a timely Office response to amendments the Applicant may file in response to this Office Action, it is respectfully requested that every effort be made to provide **specific** (page No., paragraph No., FIG. No., etc.) Specification/Drawings support in the instant Application for such amendments on accompanying remarks/arguments filings.

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Claim Objections

2. **Claim(s) 1** is objected to because of the following informalities: at line three (3) it is claimed "multilevel" cell; it appears this may be an unintentional typographical error; the specification does not include this terminology while including "multi-level." Additionally, the claim expressly requires "wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space." And later includes: "at least one MLC nonvolatile memory element; at least one SLC nonvolatile memory element." Given that the claim first requires "wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space," it is of logical consequence, implicit and self-evident that such MLC and SLC spaces include at least one MLC memory element and at least one SLC memory element. Thus the latter claim limitation does not further limit the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

4. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claim(s) 1-4 and 7-9** is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over US Publication No. 20100172179 to Gorobets et al. ("Gorobets") in view of Publication: "Design Tradeoffs in a Flash Translation Layer" to Goodson et al. ("Goodson").

As to **claim 1**, Gorobets teaches substantially the claimed invention, including: A system for storing data (As found in at least FIGS. 1, 8, 12, 15, 20) comprising: memory space containing volatile memory space and nonvolatile memory space (As found in at least FIG. 15: volatile Cache RAM 102, and nonvolatile memory 200), wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space (As found in at least FIG. 15, MLC 202 and SLC binary cache 204; further, as found in at least [0129]: binary cache configured as one bit of data in each cell); at least one controller to operate memory elements and associated memory space (As found in at least FIGS. 8 and 15, controller 300 or unnumbered "Controller" in FIG. 15 to operate memory 200); at least one MLC nonvolatile memory element; at least one SLC nonvolatile memory element (As found in at least FIGS. 15, 20 and [0129]: 202 and or 2003 including at least one MLC, while 204 and or 2001 including at least one SLC); at least one random access volatile memory element (As found in at least FIG. 15: 102); wherein the at least one controller maintain an address table in one or more of the memory elements (As found in at least FIGS. 8 and 15, and as found in at least [0096]); and wherein the address table maps logical and physical addresses adaptable to the system (As found in at least [0096]), wherein the mapping is performed as necessitated by the system to maximize lifetime,

and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories (As found in at least [0152-0154]: mapping defective elements at the cell, sectors, block, or other structural level; lifetime increase by means of spare block management usage).

While Gorobets may not expressly teach an FTL flash translation layer, Goodson, relevantly and complementarily, teaches and documents the purpose and motivation for using FTL for flash memory devices (As set, for example, on the title itself: Design tradeoffs in a flash translation layer, and as found in §§ 1-2: providing purpose of flash translation layer).

Gorobets and Goodson are analogous art because they are from the same filed of endeavor regarding memory devices that may include nonvolatile flash memory.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to complement the teachings of Gorobets as set forth in this Office action and as found in the reference with the relevant and complementary teachings of Goodson also as set forth in this Office action and as found in the reference. It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Goodson to the teachings of Gorobets such that an FTL (as explained by Goodson) is used with the flash device taught by Gorobets for the purpose of allowing the files system of the flash memory device to maintain the block interface of the disk without sacrificing the tighter integration and control over how the flash is managed and

because it hides the complexity of the flash by providing a logical block interface for the flash device.

Therefore, it would have been obvious to combine Gorobets with Goodson to make the above modification.

As **claim(s) 2 and 9**, Gorobets et al. explain that flash memory is most commonly provided in the form of a memory card (i.e., module or standalone unit as claimed) or a flash drive (i.e., module or standalone unit or hard drive, as claimed) (see background 4] [0015]). Because Gorobets et al. embodiments involve flash memory, the provisions of being a module, standalone device or hard drive, as Claimed, are met.

As to **claim 3**, Gorobets et al. teach at least one of the volatile or nonvolatile memories are embedded in the at least one controller (see Fig. 15 volatile Cache (RAM) 102 is embedded within Controller).

As to **claim 4**, Gorobets et al. teachs the nonvolatile memory (Figs. 15 MLC Memory) is flash memory because the device is a flash memory device (see 4] [0135]; see also, Fig. 15, which labels the memory device as a "Flash Memory Device").

As **claim(s) 7 and 8**, although Gorobets et al. teach the volatile memory (Fig. 15 Cache (RAM) 102), they are silent with respect to the specific type of volatile memory—- whether DRAM or SRAM as claimed. Gorobets et al. does not mention or show any aspects of the type of volatile memory employed

OFFICIAL NOTICE is taken that DRAM and SRAM are volatile memory types that have been frequently used as volatile memory in computer systems, and these two types of volatile memory are obvious variants and their tradeoffs are well-documented in the prior art. For example, although SRAM is faster than DRAM, SRAM requires more components per cell because typical prior art CMOS SRAM cell involve six transistors (6T-SRAM), whereas the counterpart typical DRAM cell requires one transistor and one capacitor (1T1C). DRAM, however, has been well-established in the industry as a main memory for computing systems. The real estate required per cell is smaller than that for SRAM, meaning more storage capacity at cheaper cost. The tradeoff is that DRAM must include refresh circuitry to account for decay rate of the capacitors. Although SRAM is typically used for cache memory, DRAM is often employed as well.

It would have obvious to one of ordinary skill in the art before the invention use DRAM or SRAM for the volatile memory as claimed because of the reasons discussed above.

6. **Claim 5** is rejected under pre-AIA35 U.S.C. 103(a) as being unpatentable over Gorobets et al. in view of Goodson et al., as applied to claim 1, further in view U.S. Publication No. 20090268513 to De Ambroggiet et al. ("De Ambroggiet"), further in view of US Publication No. 20100058018 to Kund et al. ("Kund").

As to **claim 5**, Gorobets et al. fail to teach that the memory could be anything other than flash EEPROM or other types of charge trapping memory see e.g. 4] [0010] describing the various types of memory.

De Ambroggiet al. teaches that one type of resistive memory (RRAM), Phase Change (PCRAM or PCM) can be configured to be partially SLC and partially MLC.

Kund et al. teach generally that "Emerging memory technologies such as resistive memory (e.g., resistive random access memories such as phase change random access memory (PCRAM), conductive bridge random access memory (CBRAM), and magnetic random access memory (MRAM) offer certain advantages over DRAM, Flash and other conventional types of memory devices in terms of switching speeds, size, power consumption, and non-volatility." 4] [0016].

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the flash EEPROM taught by Gorobets et al. with the PCM taught by De Ambroggiet al. in view of the PCM advantages over flash EEPROM taught by Kund et al. because the emerging memories (such as PCRAM) offer switching speed, size, power-consumption, and non-volatility advantages over flash memory.

7. **Claim 6** is rejected under pre-AIA35 U.S.C. 103(a) as being unpatentable over Gorobets et al. in view of Goodsonetal., as applied to claim 1, further in view of US

Publication No. 20090307418 to Chen et al. ("Chen"), and further in view of Kundet al. ("Kund").

As to **claim 6**, Gorobets et al. fail to teach that the memory could be anything other than flash EEPROM or other types of charge trapping memory see e.g. 4 [0010] describing the various types of memory.

Chen et al. teach that MRAM could be used as SLCin conjunction with some other memory type being used as MLC to create a hybrid density memory. See e.g. [0031].

Kund et al. teach generally that "Emerging memory technologies such as resistive memory (e.g., resistive random access memories such as phase change random access memory (PCRAM), conductive bridge random access memory (CBRAM), and magnetic random access memory (MRAM)) offer certain advantages over DRAM, Flash and other conventional types of memory devices in terms of switching speeds, size, power consumption, and non-volatility." 4] [0016].

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the SLC flash EEPROM taught by Gorobets et al. with the SLC MRAM in view of the MRAM advantages over flash EEPROM taught by Kund et al. because the emerging memories (such as MRAM) offer switching speed, size, power-consumption, and non-volatility advantages over flash memory.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claim(s) 1-9 rejected on the ground of nonstatutory double patenting as being unpatentable over claim(s) 1-12 of U.S. Patent No. **10950300**. Although the claims at issue are not identical, they are not patentably distinct from each other because the instant claims are obviated by the patented claims. A later patent claim is not patentably distinct from an earlier patent claim if the later claim is **obvious** over (in a non-statutory double patent rejection) the earlier claim. In re Lonqi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were **obvious** over claims in four prior art patents); In re Bercl, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). Ely Lilly and Co. v Bar Laboratories, Inc., United States Court of Appeals for the Federal Circuit, on petition for rehearing en banc (decided: May 30, 2001). Furthermore, the subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application claim obvious common subject matter, wherein the claims of the instant Application and

broader renderings of the Patent claims, in brief and saliently: a system for storing data comprising: memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space; at least one controller to operate memory elements and associated memory space; at least one MLC nonvolatile memory element; at least one SLC nonvolatile memory element; at least one random access volatile memory element; an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements; and wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories. Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to FERNANDO N HIDALGO whose telephone number is (571)270-3306. The examiner can normally be reached M-F 9:00-7:30 ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 5712721852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FERNANDO N. HIDALGO
Primary Examiner
Art Unit 2827

/Fernando Hidalgo/
Primary Examiner, Art Unit 2827

Notice of References Cited	Application/Control No. 17/203,385	Applicant(s)/Patent Under Reexamination Rao, G.R. Mohan	
	Examiner FERNANDO N HIDALGO	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20100172179-A1	07-2010	Gorobets; Sergey Anatolievich	G06F12/0246	365/185.11
*	B	US-20090268513-A1	10-2009	De Ambroggi; Luca	G11C13/0004	438/102
*	C	US-20100058018-A1	03-2010	Kund; Michael	G11C13/0033	711/E12.001
*	D	US-20090307418-A1	12-2009	Chen; Ming-Dar	G06F12/0246	711/E12.083
	E					
	F					
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	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/203,385	Rao, G.R. Mohan
	Examiner	Art Unit
	FERNANDO N HIDALGO	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/03/2022								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/203,385	Filing Date 03/16/2021	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	08/08/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 7	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/DORIAN EVANS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	G. R. Mohan RAO
Serial No.:	17/203,385
Confirmation No.:	6508
Filed:	March 16, 2021
Group:	2827
Examiner:	Fernando N. HIDALGO
For:	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

AMENDMENT AND RESPONSE TO OFFICE ACTION

This communication is responsive to the Examiner's Office Action dated February 8, 2022. Reconsideration is respectfully requested.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks/Arguments begin on page 4 of this paper.

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level ~~multilevel~~ cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space;

a bank of nonvolitile memory, including:

a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element[[;]], and

at least one SLC memory module including at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements; ~~and~~

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein, the controller, in at least a Write access operation to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store data in the given one of the MLC nonvolatile memory elements and retain such stored data in the random access volatile memory;

the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

2. (Currently Amended) The system of Claim 1, wherein the ~~memory elements are a module, standalone device, or multi-chip package~~ FTL, flash translation layer, is a software module, or a firmware module containing software updates.

3. (Currently Amended) The system of Claim 1, wherein at least one of the random access volatile memory or the MLC and SLC nonvolatile ~~memories~~ memory elements are embedded in the at least one controller.

4. (Currently Amended) The system of Claim 1, wherein the MLC and SLC nonvolatile memory [[is]] elements comprise flash memory.

5. (Cancelled)

6. (Cancelled)

7. (Currently Amended) The system of Claim 1, wherein the random access volatile memory element is dynamic random access memory.

8. (Currently Amended) The system of Claim 1, wherein the random access volatile memory element is static random access memory.

9. (Original) The system of Claim 1, wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD).

REMARKS

Applicant has carefully reviewed the Office Action dated February 8, 2022. Applicant has amended Claims 1-4, 7 and 8, and cancelled Claims 5 and 6 to more clearly point out the present inventive concept. Reconsideration and favorable action is respectfully requested.

Claim 1 has been objected to because of the use of the term "multilevel" which was set forth in the specification as "multi-level." This has been changed in the claim. Further, the Examiner objected to the fact that the claim defines an MLC and an SLC memory space and then defines MLC and SLC memory elements. The Examiner's argument seems to be that a memory space must include a memory element. However, a memory element is a physical device that needs to be mapped into the space, either physical or logical, to exist within that space. Therefore, Applicant believes that the way the term is utilized in the claim is actually limiting.

Claims 1 – 4, 7 and 8 have been amended to incorporate the limitations that were added to the parent application, US Patent Application Serial Number 16/006,299 (the '299 Application). Since the objections were similar, the following discussion is basically a replication of the arguments set forth in the parent application. Additionally, the claims have been amended to define the memory modules as being formed in a bank of memory modules. Each of the memory modules can include the memory elements.

USC §103(a) Rejection

Claims 1 – 4 and 7 – 9 stand rejected under 35 USC §103(a) as being unpatentable over the combination of *Gorobets* in view of *Goodson*. This rejection is respectfully traversed with respect to the claims as currently presented.

The *Gorobets* reference does not disclose or suggest a remapping operation wherein the remapping operation is for the purpose of improving the endurance. Rather, all that the *Gorobets* reference does is remap for wearability in accordance with a wearability algorithm. There is no integrity check that is performed for this operation. Further, there is no indication that the remapping of the physical address space will be from a memory element having a relatively lower

endurance in another memory element to that another memory element. The *Goodson* reference does not cure this deficiency. Therefore, Applicant respectfully requests withdrawal the 35 USC §103 rejection with respect to Claims 1 – 4 and 7 – 9.

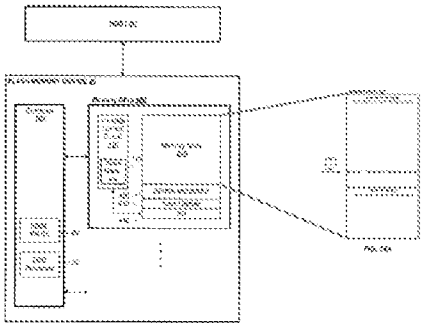
In the '299 application, the Examiner had also combined with respect to a later amended claim, *Goodson* and *Oribe* with *Gorobets*. Since the current claim reflects amendments that were overcome in the '299 Application, they will not be repeated here.

The '299 Application matured into Issued Patent No. 10,950,300, which was the subject of an IPR, IPR2021-01550. In this IPR, the primary reference was US Patent Publication 2011-0099460 to *Dusiji* (the "*Dusija*" Application). Applicant believes a discussion of this reference is warranted relating to the current amended claim.

***Dusiji* Discussion**

The *Dusija* reference is a system that runs a data integrity check on a multi-chip Flash memory that incorporates two different levels of memory, an MLC Flash memory and an SLC Flash memory. In the data integrity operation, data is first written to specific storage location in a section 420 (MLC), which is a less robust but higher density storage area (Figure 14A) than the SLC section 410, and then an error determination operation performed after the Write operation to determine if the stored data has incurred any errors due to the specific storage location having excessive "wear." This determination of errors can be achieved either by 1) an ECC check of a retrieved copy of the stored data or 2) by comparison with a cached copy of the stored data.

First, though, a description of the data flow for receiving a page of data and writing it to the Flash in *Dusiji* would be helpful. Figure 1of *Dusiji* illustrates the high-level architecture of the memory with the associated memory layout of the memory array 200 as depicted in Figure 14A:



There are, first, a plurality of memory chips 100 that each have an associated memory array 200. Each chip 100 has an on-chip controller 110. Second, there is a main controller 102 that controls all of the chips 100. The main controller 102 receives data to be written to one of the chips 100 and transfers the data to that chip's controller 110, and that chip 100 and its controller 110 then interfaces with the associated memory array 200 to perform memory operations thereon in conjunction with a state machine 112 for chip level memory operations. The memory array 200 (Figure 14A) is comprised of a first portion 410 (SLC) and a second portion 420 (MLC). In the data storage area, data is at a minimum first stored in the array as a first copy and, if using the cached operation, a cached copy is also stored, such that two copies of the data can be stored therein. A determination is then made as to existing bit errors in the stored data exceeding a predetermined threshold.

This determination operation involves either 1) a first determination operation of examining an ECC portion of the first copy and processing it through an error correcting algorithm or 2) a second determination operation of comparing the first copy to the cached second copy. If the bit errors are less than the threshold, then the first copy is used in both of the first and second determination operations. If the bit errors are determined to exceed the threshold, the first copy is discarded and the directory pointed to a new updated copy stored in the more robust portion (SLC) of the memory.

The above operation of discarding the first copy and updating the directory utilizing a new updated copy as the accessible copy is facilitated by a number of methods:

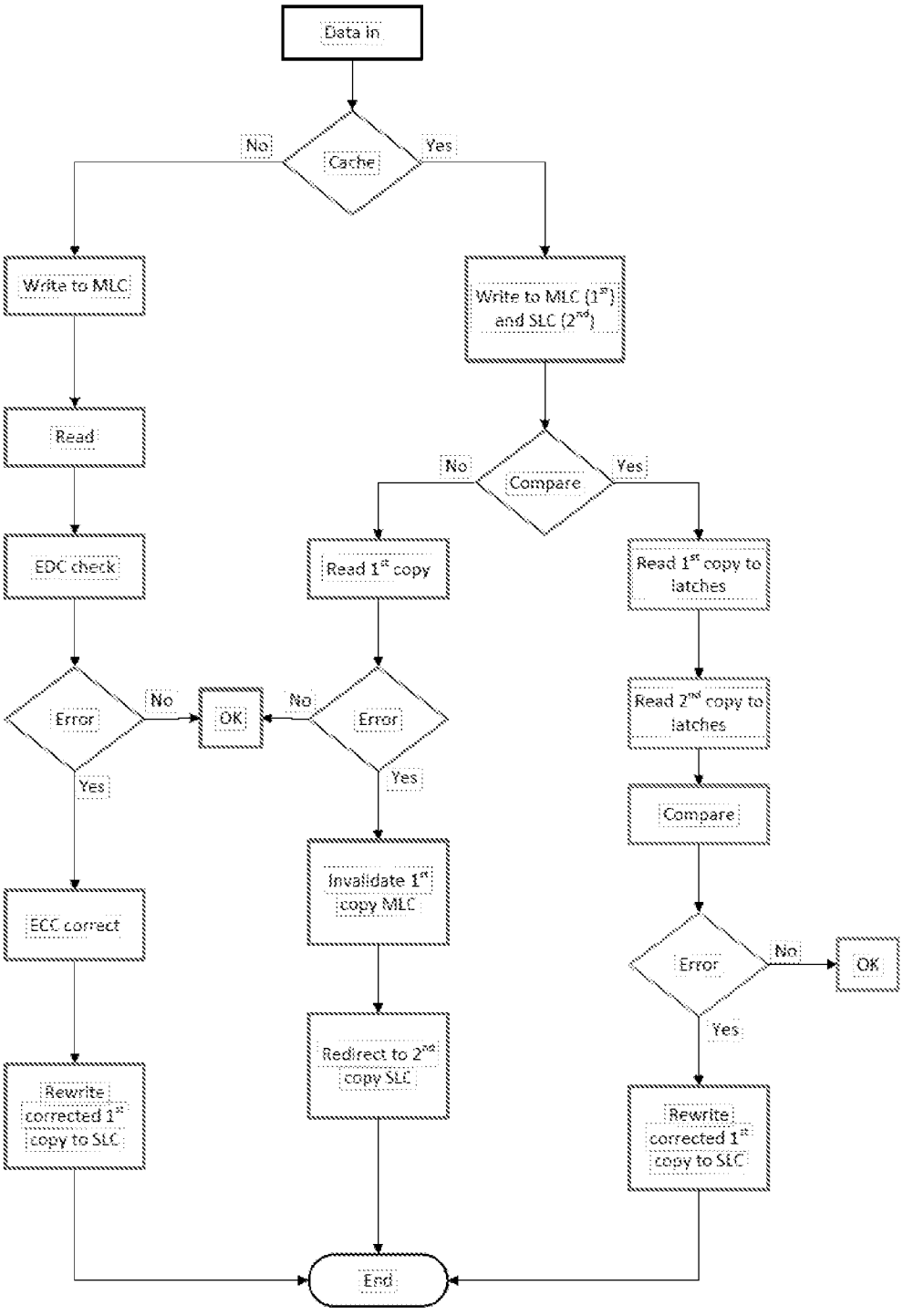
1) Method 1 – No Cache Required - Read the first copy and use ECC to determine if bit errors are high and then use ECC to correct the bit errors in the first copy and rewrite a corrected first copy to another location and mark original first copy as invalid and update directory to point to the corrected first copy i.e., the new updated copy, in a rewrite operation;
2) Method 2 - Cache Copy Required - Read the first copy and use ECC to determine if bit errors are high and then mark the first copy as invalid and then update the directory to indicate that the cached second copy stored in the first portion is now the valid copy, i.e., the new updated copy – no rewrite required; and
3) Method 3 - Access both the first copy and the cached second copy and feed to hardware comparator for bit error determination followed by a Read of the cached second copy and rewrite of the accessed cached second copy to the more robust section of the array (SLC) as the new updated copy in a rewrite operation.

This overall data verification process is described as follows in *Dusija*:

> *[0111] When a page of incoming data is to be written to the memory array 200, it is preferably stored in the high density second portion for the sake of efficiency and high capacity. Thus a first copy of the data page is written to the second portion.*
>
> *[0112] Later, the first copy of the data page is read back in a "post write read" to determine if there are any errors. This is accomplished either by comparison with the original copy which may be cached or by checking the EDC portion of the ECC.*

Here, *Dusija* provides for two methods of determining if an error exists, the first being by comparison with the "original copy" and the second by checking the EDC portion of the ECC. These will be described in more detail hereinbelow.

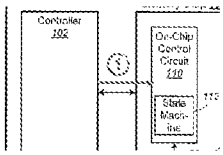
The flow of data and the various operations performed by different portions of the system will be described as follows, with reference to the relevant portions of the Specification of *Dusiji*. The following flow diagram depicts the different pats:



Step 1 - Data is transferred from the controller 102 at the system level to the control circuitry 110 on the chip 100. This is described in ¶[0060]:

[0060] The controller 102 co-operates with the memory chip and controls and manages higher level memory operations. For example, in a host write, the host 10 sends data to be written to the memory array 100 in logical sectors allocated from a file system of the host's operating system.

This is depicted as follows:



Step 2 – The controller then writes or "programs" the data to the memory array 200 (¶[0111]). In this operation, there are two Write operations that are performed when a cached copy is required. This is described in ¶¶ [0021] and [0127] as follows:

[0021] In the preferred embodiment, the first portion is further provided with a first section and a second section. The incoming data is cached in the first section of the first portion and a first copy of the data is written to the second portion.

[0127] In an alternative embodiment, the first portion serves as a cache for incoming data, so a cache copy of the input data is programmed into the cache. Then a first copy of data is programmed into the second portion.

However, the embodiment of Figures14A-B indicates that the error detection can be by ECC or comparison with a cached copy. (¶ [0112]).

[0112] Later, the first copy of the data page is read back in a "post write read" to determine if there are any errors. This is accomplished either by comparison with the original copy which may be cached or by checking the EDC portion of the ECC.

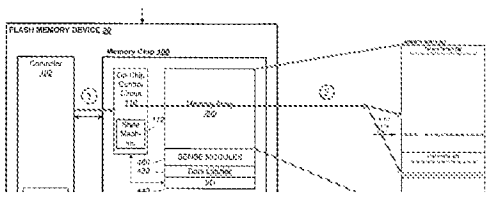
There is no specific description as to where this cached copy is obtained from in ¶ [0112]. As will be described hereinbelow, the only discussion of a cache location is a description of the first portion (SLC) being used as a cache. But *Dusiji* does refer to incorporated by reference patents, USP 6,456,528 and USP 5,930,167. The '528 patent referenced relative to the two different MLC and SLC portions and the '167 patent refers to using the non-volatile memory as a write cache, stating at Col 2, ll. 43-49:

This technique has the advantage of initially writing data with the higher speed of low data density storage while enjoying the benefits of high density long term

storage of the data. Data are initially stored with a low density for only a short time in any unused part of the flash EEPROM memory. No separate write cache memory, such as those implemented with a volatile memory, need be employed.

Applicant believes it is reasonable that any cached copy is cached in the first portion (SLC). As such, this is an operation that requires two (2) programming operations, or Writes, in order to place a cached copy of the data in the first portion (SLC) of the memory array and a "first copy" in the second portion (MLC) of the memory array 200. Figure 14B addresses a rewrite operation as either from a corrected copy of the first page or from a cached copy. (¶[0116])

The operation of Figures 14A-B will first be described. This is depicted as follows with the cached copy (not required for ECC method of correction) depicted in the following annotated diagram in green and the first copy depicted in yellow:



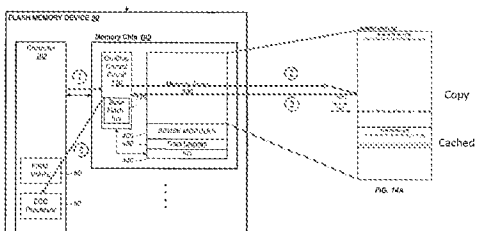
Once the data is stored in the first (SLC) portion and the second (MLC) portion, the next process is to determine if errors exist. This process is set out in ¶[0112] as follows:

[0112] Later, the first copy of the data page is read back in a "post write read" to determine if there are any errors. This is accomplished either by comparison with the original copy which may be cached or by checking the EDC portion of the ECC.

Thus, there are two processes for determining the existence of an error. The first process is by checking the EDC portion of the ECC (no cached cpy required) and the second is by comparing the first copy with the cached copy (cached copy required). Figure 15 sets forth a flow chart for the first process.

ECC - first process

Step 3 – Read back the first copy to determine if there are errors, depicted as follows:



In this operation, the first copy is pulled back up to the controller 102 and the associated ECC Processor 62 to make the determination as to if the number of error bits exceeds a predetermined number (¶[0113])[1]. As noted in the Background of the Invention section, ¶ ¶[0014]-[0016], the disadvantage of utilizing very powerful ECC to correct large errors is described. Detection of the errors requires a certain amount of processing time at the controller 102 but correction thereof can be processing intensive. Thus, the ECC circuitry can determine a threshold of error bits that exceeds a "predetermined amount" (¶[0113]) as being the point at which the determination has been made to invalidate the first copy and store either 1) the Error Corrected copy (Method 1 above) or 2) the cached copy (Method 2 above). Note that Method 1 does not need any cached copy to be stored.

Step 4 – A rewrite operation is performed if the number of error bits has exceeded the predetermined number. ¶ [0116] sets forth:

> *After the post-write read detects the number of error bits in the data page has exceeded the predetermined amount, a second copy of the data page is rewritten to the first portion. The second copy is of the original data which may be cached or in another embodiment, by retrieving the first copy and correcting the error bits with the ECC.*

This rewrite is also described in step 540 of Figure 15. Thus, the operation can proceed in two ways (Methods 1 or 2 above).

The first (Method 1 above) is to read the first copy from the second portion 420 (MLC) of the memory array 200 to the control circuitry 110, examine the EDC portion to determine if the error bits exceed the predetermined amount, and, if so, read the first copy and correct the errors therein with ECC at the controller 102. This corrected copy is then written to the first portion 410 (SLC) as a second copy and the first copy invalidated (Method 1 above) – no cache

[1] ¶ ¶[0113] and [[0088] indicated that the ECC processor 66 and the controller 102 are responsible for all of the detection and correction.

copy required but a rewrite operation required. This is basically the flow discussed in Figure 15, as step 540 just describes rewriting a second copy to the first portion (SLC).

Further, after the discussion of Figure 15, an "alternate embodiment" is disclosed as follows:

> *[0127] In an alternative embodiment, the first portion serves as a cache for incoming data, so a cache copy of the input data is programmed into the cache. Then a first copy of data is programmed into the second portion.*
>
> *[0128] If the post-write read has not detected an excessive amount of error in the first copy, the first copy will be deemed valid and subsequent read will be directed to access the first copy.*
>
> *[0129] On the other hand, if the post-write read has detected an excessive amount of error in the first copy, the cached copy in the first portion will replace the first copy in the second portion as valid data. The first copy will become obsolete and a directory in a block management system embodied in the firmware of the controller (see FIG. 1) will be update to direct subsequent access to the cached copy.*

This embodiment relates to the operation of Figures 14A-B. ¶[0129] states "*the cached copy in the first portion will* ***replace*** *the first copy in the second portion as valid data. The first copy will become obsolete and a directory in a block management system embodied in the firmware of the controller (see FIG. 1) will be update to direct subsequent access to the cached copy.*" This operation does not require the cached copy to be read and rewritten to the first portion as a separate second copy from the original cached copy discussed hereinbelow with respect to Figures 16A-C. All that is required is to mark the first copy in the second portion (MLC) as invalid and then update the directory to point to the cached copy in the first portion. This embodiment relates to the second method (Method 2 above) wherein the first copy is read from the second portion 420 (MLC) of the memory array 200 to the controller, a quick error detection performed using the EDC portion of the ECC to determine if the error bits exceed the predetermined amount, and, if so, the first copy is invalidated and the directory updated to point to the cached copy as the second and valid copy.

Compare – Second Process

In the process where a compare operation is utilized to determine if errors exist, the only disclosure in *Dusiji* regarding this compare operation employs a compare operation *at the chip level* below the controller. However, *Dusiji* does say that the comparison is made with the original copy which may be "cached." If an error is determined to exist, then the cached copy in the first portion (SLC) is read and then rewritten to a rewrite section in the SLC first portion 410 (Figures 16A-C).

The disclosure in *Dsuiji* as to the compare operation relates to the use of the data latches, as set forth in the following language from ¶ ¶[0135] – [0136]:

> *[0135] According to another preferred embodiment, the memory array is provided with a set of data latches on an integrated circuit chip, the checking of the error bits in the first copy is accomplished by loading the first copy and the cached copy into the set of data latches and making a comparison at the set of data latches.*
>
> *[0136] By not making the comparison at the controller, the data does not have to be toggled out to the controller, much time can be saved. FIG. 1 shows the data latches 430, which is on-chip, for the data comparison to take place.*

This sets forth that checking of error bits in the embodiment of Figures 14A-B is accomplished by loading the first copy of the cached data into the data latches and then perform a comparison. It is noted that ¶[0135] indicates this is in accordance with "another preferred embodiment." But, in this embodiment, it is stated in ¶[0136] that it is *undesirable* to utilize the controller for the compare operation.

Distinctions over the Teachings of *Dsuiji*

Claim 1, as amended, includes the language:

> *the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein, the controller, in at least a Write access operation to a given one of the MLC nonvolatile memory element in an associated MLC memory module, operable to store data in the given one of the MLC*

nonvolatile memory elements and retain such stored data in the random access volatile memory;

the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory;

This claim language requires both a random access memory element for storage of retained data and that the data integrity check be performed *at the controller level* with a compare operation of retained data and stored data.

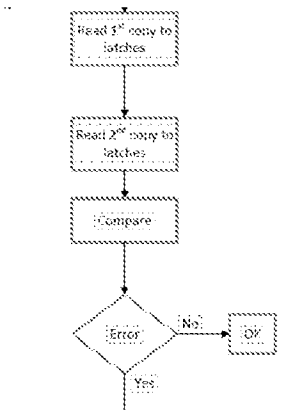
The first embodiment of relevance is that of Figures 14A-B. This is an operation that utilizes either an ECC check or a comparison with a cached (retained) copy to determine wear. In the embodiment wherein a compare operation is disclosed, ¶ [0112] states *"[l]ater, the first copy of the data page is read back in a "post write read" to determine if there are any errors. This is accomplished either by comparison with the original copy which may be cached or by checking the EDC portion of the ECC."* There is no specific description in this ¶ [0112] as to where the cache exists. There is also no description of how this comparison operation is facilitated in this ¶ [0112]. In ¶ [0116], it is stated that, in the event of an error, the original data can be retrieved from a second copy of the original data "*which may be cached or in another embodiment, by retrieving the first copy and correcting the error bits with the ECC.*" In ¶ [0112], *Dusiji* does not state where this cached data is stored. However, based on the statement in ¶ ¶ [0020]-[0021] the preferred embodiment for the cache location is SLC memory:

[0020] In an alternative embodiment, the first portion serves as a cache for incoming data, so a cache copy of the input data is programmed into the cache. Then a first copy of data is programmed into the second portion. If the post-write read has not detected an excessive amount of error in the first copy, the first copy will be deemed valid and subsequent access will be directed to access the first copy. On the other hand, if the post-write read has detected an excessive amount of error in the first copy, the cached copy in the first portion will replace the first copy in the second portion as valid data. The first copy will become obsolete and subsequent access will be directed to the cached copy.

[0021] In the preferred embodiment, the first portion is further provided with a

first section and a second section. The incoming data is cached in the first section of the first portion and a first copy of the data is written to the second portion. Afterwards, the first copy in the second portion is read back to check for excessive error bits. If the error bits exceeded a predetermined amount, a second copy of the in coming data is written to the second section of the first portion.

Thus, *Dusiji* discloses only caching a copy in the SLC non-volatile memory and carrying out the comparison below the controller level. There is no suggestion that the data can be retained (cached) in other than the non-volatile memory and, further, it is stated that the compare operation "not" be carried out at the controller level (¶ [0136]), as *the data does not have to be toggled out to the controller, much time can be saved.* This compare operation is different than the ECC operation requiring the first copy to be retrieved, as illustrated by the red portion of the above included flow diagram:



Even though this compare operation requires an additional Write operation to store the cached copy in a rewrite, *Dusiji* recognizes this and provides a solution by enabling the post-read-write operation only at the end of life for the memory:

[0152] In another aspect of the invention, an enhanced post-write read error management is implemented. The post-write read is not enabled at the beginning of life of a memory device. The error rate of the memory device at the beginning of life is very low and there is no need to operate the post-write read. This avoids wasting time to do post-write read. As the memory device ages through use, the enhanced post-write read and error management of the invention is enabled at a predetermined age of the device.

[0153] In a preferred embodiment, the age of the memory device is determined by a hot count maintained with each erase block of memory cells. The

hot count tracks the endurance or the number of times the erase block has been cycled through erase and program operations. Whenever a hot count of an erase block passes a predetermined hot count threshold, the enhanced post-write-read error management will commence and operate until the end of life of the memory device.

Since *Dusiji* recognizes the issue with the multiple Writes required by the post-read-write operation and provides a solution therefore, there is no need to find another solution.

Thus, Applicant believes that *Dusiji*, taken alone or in combination with any cited reference, does not anticipate or render obvious any of the currently amended claims.

Applicant has now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicant respectfully requests full allowance of the claims as amended.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ghowison@munckwilson.com.

Recognizing that Internet communications are not secure, Applicant hereby authorizes the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application by video conferencing, instant messaging, or electronic mail. Applicant understands that a copy of these communications will be made of record in the application file.

Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 50-0208/VRVN60-35360.

Respectfully submitted,
MUNCK WILSON MANDALA, LLP
Attorneys for Applicant

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August 8, 2022

PTO/SB/22 (10-20)
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PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number (Optional): VRVN60-35360

Application Number: 17/203,385

Filed: March 16, 3021

For: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Art Unit: 2827

Examiner: Fernando N. HIDALGO

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
☐ One month (37 CFR 1.17(a)(1))	$220	$110	$55	$
☐ Two months (37 CFR 1.17(a)(2))	$640	$320	$160	$
☑ Three months (37 CFR 1.17(a)(3))	$1,480	$740	$370	$ 1480
☐ Four months (37 CFR 1.17(a)(4))	$2,320	$1,160	$580	$
☐ Five months (37 CFR 1.17(a)(5))	$3,160	$1,580	$790	$

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-0208.

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WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. 37 CFR 3.73(b) statement is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration number 30,646.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Gregory M. Howison, Reg. #30646/ — Signature

August 8, 2022 — Date

Gregory M. Howison — Typed or printed name

972-628-3600 — Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of ONE forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/08a (01-22)
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(Not for submission under 37 CFR 1.99)

Application Number	17203385
Filing Date	2021-03-16
First Named Inventor	G.R. Mohan Rao
Art Unit	2827
Examiner Name	Fernando N. HIDALGO
Attorney Docket Number	VRVN60-35360

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	Application Number	17203385
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	First Named Inventor	G.R. Mohan Rao
	Art Unit	2827
	Examiner Name	Fernando N. HIDALGO
	Attorney Docket Number	VRVN60-35360

	1	IPR2021-01547 Decision Granting Institution of Inter Partes Review	
	2	IPR2021-01547 Patent Owner's Corrected Preliminary Response	
	3	IPR2021-01547 Patent Owner's Response	
	4	IPR2021-01547 Exhibit 2001: Declaration of Sunil P. Khatri	
	5	IPR2021-01547 Exhibit 2009: Invalidity Claim Chart for the '298 Patent (Dusija)	
	6	IPR2021-01547 Exhibit 2010: Invalidity Claim Chart for the '298 Patent (Saturdja)	
	7	IPR2021-01547 Exhibit 2011: Invalidity Claim Chart for the '298 Patent (Moshayedi)	
	8	IPR2021-01547 Exhibit 2012 Claim Construction Order	
	9	IPR2021-01547 Exhibit 2014 Declaration of Sunil P. Khatri	
	10	IPR2021-01547 Exhibit 2015 Remote Deposition of Dr. David Liu	
	11	IPR2021-01547 Exhibit 2016 US Pat. 8,285,940 Reid	

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	Filing Date	2021-03-16
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2827
	Examiner Name	Fernando N. HIDALGO
	Attorney Docket Number	VRVN60-35360

	12	IPR2021-01548 Decision Granting Institution of Inter Partes Review	
	13	IPR2021-01548 Patent Owner's Preliminary Response	
	14	IPR2021-01548 Patent Owner's Response	
	15	IPR2021-01548 Exhibit 2004: US Pat. 10,950,3000 Rao	
	16	IPR2021-01548 Exhibit 2009: Invalidity Claim Chart for the '385 Patent (Dusija)	
	17	IPR2021-01548 Exhibit 2010: Invalidity Claim Chart for the '385 Patent (Saturdja)	
	18	IPR2021-01548 Exhibit 2011: Invalidity Claim Chart for the '385 Patent (Moshayedi)	
	19	IPR2021-01548 - Exhibit 2012 Claim Construction Order	
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	Examiner Name	Fernando N. HIDALGO
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	23	IPR2021-01549 Decision Granting Institution of Inter Partes Review	
	24	IPR2021-01549 Patent Owner's Preliminary Response	
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	26	IPR2021-01549 Exhibit 2009: Invalidity Claim Chart for the '240 Patent (Dusija)	
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	30	IPR2021-01549 Exhibit 2016 US Pat. 8,285,940 Reid	
	31	IPR2021-01549 - Exhibit 2012 Claim Construction Order	
	32	IPR2021-01550 Decision Granting Institution of Inter Partes Review	
	33	IPR2021-01550 Patent Owner's Corrected Preliminary Response	

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	34	IPR2021-01550 Patent Owner's Response	
	35	IPR2021-01550 Exhibit 2009: Invalidity Claim Chart for the '300 Patent (Dusija)	
	36	IPR2021-01550 Exhibit 2010: Invalidity Claim Chart for the '300 Patent (Saturdja)	
	37	IPR2021-01550 Exhibit 2012 Claim Construction Order	
	38	IPR2021-01550 Exhibit 2014 Declaration of Sunil P. Khatri	
	39	IPR2021-01550 Exhibit 2015 Remote Deposition of Dr. David Liu	
	40	IPR2021-01550 Exhibit 2017 US Pat. 5,721,862 Sartore et al.	
	41	IPR2021-01550 Exhibit 2019 US Pat. 5,535,399 Blitz et al.	
	42	Ethan Chen; Tones Yen; Advantech: Ultra MLC Technology Introduction; October 5, 2012, 10 pages	
	43	Rino Micheloni, Luna Crippa, Alessia Marelli; Springer: Inside NAND Flash Memories; 2010; ISBN 978-90-481-9430-8; 12 pages	
	44	Microsoft Computer Dictionary Fifth Edition; Definition for Data Integrity; 2002, ISBN 0-7356-1495-4	

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	Examiner Name	Fernando N. HIDALGO
	Attorney Docket Number	VRVN60-35360

	45	Frank Hargrave; Hargrave's Communications Dictionary excerpt; IEEE Press Marketing; 2001; ISBN 0-7803-6020-6; 9 pages
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	47	Micron's Preliminary Invalidity Contentions

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17203385
	Filing Date	2021-03-16
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2827
	Examiner Name	Fernando N. HIDALGO
	Attorney Docket Number	VRVN60-35360

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Gregory M. Howison, Reg. #30646/	Date (YYYY-MM-DD)	2022-08-08
Name/Print	Gregory M. Howison	Registration Number	30646

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/203,385	03/16/2021	G.R. Mohan Rao	VRVN60-35360	6508

25883 7590 09/09/2022

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EXAMINER
HIDALGO, FERNANDO N

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
09/09/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Vervain Ex. 2024 p. 73 of 193
Vervain v. Phison
PGR2025-00010

Office Action Summary	Application No. 17/203,385	Applicant(s) Rao, G.R. Mohan	
	Examiner FERNANDO N HIDALGO	Art Unit 2827	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 8/8/22.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-4 and 7-9 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-4 and 7-9 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Examiner's Note

The examiner has cited particular passages including column and line numbers, paragraphs as designated numerically and/or figures as designated numerically in the references as applied to the claims below for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claims, other passages, paragraphs and figures of any and all cited prior art references may apply as well. It is respectfully requested from the applicant, in preparing an eventual response, to fully consider the context of the passages, paragraphs and figures as taught by the prior art and/or cited by the examiner while including in such consideration the cited prior art references in their entirety as potentially teaching all or part of the claimed invention. MPEP 2141.02 VI: "**PRIOR ART MUST BE CONSIDERED IN ITS ENTIRETY, INCLUDING DISCLOSURES THAT TEACH AWAY FROM THE CLAIMS**." MPEP 2123 (I): "**PATENTS ARE RELEVANT AS PRIOR ART FOR ALL THEY CONTAIN**."

Additionally, in an effort to provide a timely Office response to amendments the Applicant may file in response to this Office Action, it is respectfully requested that every effort be made to provide **specific** (page No., paragraph No., FIG. No., etc.) Specification/Drawings support in the instant Application for such amendments on accompanying remarks/arguments filings.

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

2. **Claim(s) 5-6** have been cancelled.

Response to Arguments

3. Applicant's arguments(hereinafter "arguments") filed 8/8/2022 have been fully considered but they are not persuasive. Additionally, applicant's arguments with respect to claim(s) 1-4 and 7-9 have been considered but are moot because the new ground of rejection does not rely on any reference applied in the prior rejection of record for any teaching or matter specifically challenged in the argument. At the outset, it is noted that the arguments include analysis/discussion on the "Dusija" reference. The Office action dated 2/8/2022, which presumably the arguments are a response to, does not include any reference at all about the Dusija reference; no claim rejection or objection, or anything at all of any kind is based on any teachings the Dusija reference may include. It would seem the inclusion in the arguments of analysis/discussion of the Dusija reference is an attempt to preemptively disqualify such reference from being considered in any claim rejection/objection as teachings any obviating or anticipating subject mater that may potentially be claimed, be claimed in the future. The arguments on page 16 expressly submit: "Applicant believes that Dusiji, taken alone or in combination with **any cited reference**, does not anticipate or render obvious any of the currently amended claims." (emphasis added) Thus, it would seem the arguments have already unilaterally and preemptively decided that the Dusija reference, a reference not cited at all in any prior Office action, is henceforth disqualified even in combination with **any cited reference**, presumably even reference that may cited down the road along prosecution of the instant Application. This cannot be.

Moreover, in traversing the rejection to claim 1, at least based on the actual references cited in the prior Office action, the arguments on page 4 submit: "Further, there is no indication that the remapping of the physical address space will be from a memory element having a relatively lower endurance in another memory element to that another memory element." Firstly, "remapping of the physical address space will be from a memory element having a relatively lower endurance in another memory element to that another memory element," makes absolutely no sense whatever. An attempt to summarize this sentence between quotation marks is as follows: remapping … from a memory element … in another memory element to that another memory element. If this makes sense, an invitation is made herein for a response explaining its meaning. Secondly, even if the sentence above between quotation marks makes sense, and this is not conceded at all, Whether the alleged "remapping" -the claim includes mapping- is from memory having a relatively lower endurance, the claim as amended dated 8/8/2022 does not make such requirement. There is no clam at all of remapping from memory having lower endurance. It would seem the arguments would like the impermissible importation of subject matter from the specification into the claim. (2111 MPEP) If this subject matter is important to the invention, and provided it does find support in the specification, such subject matter is invited to be made part of the claims.

Furthermore, the arguments on page 4 also submit: "The Gorobets reference does not disclose or suggest a remapping operation wherein the remapping operation is for the purpose of improving the endurance. Rather, all that the Gorobets reference does is remap for wearability in accordance with a wearability algorithm." Whether the Gorobets reference **all it does** is remapping wearability according to a wearability

algorithm, is merely an allegation, one without weight since the invention as claimed does not concern such allegation. However, on whether the Gorobets reference teaches remapping for the purpose of improving endurance, this has already been addressed in the prior Office action, and as found in at least paragraphs [0152-0154]: "The result is a **limited effective lifetime of the memory cells**; that is, memory cell eventual fail to operate properly, usually failing to program or erase properly... To account for this, memory devices frequently employ defect management procedure and **remap defective elements** at the cell, sectors, block, or other structural level." (emphasis added)

The prior Office action dated 2/8/2022 includes nonstatutory double patenting claim rejections. The arguments provide, it would seem, no response of any kind to these claim rejections. Absence of any relevant response in the arguments does not make such double patenting claim rejections conveniently go away. The double patenting claim rejection is thus maintained and set forth below in this Office action.

In regard to newly introduced claim limitations dated 8/8/2022:

a bank of nonvolitile memory, including: a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element[[;]], and at least one SLC memory module including at least one SLC nonvolatile memory element (As found in at least FIG. 15, at least paragraphs [0090], [0135] in the teachings of Gorobets: the memory 200 is organized into blocks; and that 200 is partitioned into MLC modules an LSC memory modules (SLC is described as binary mode cells; also refer to [0108]).

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein,

the controller, in at least a Write access operation to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store data in the given one of the MLC nonvolatile memory elements and retain such stored data in the random access volatile memory (While the teachings of Gorobets as modified may not expressly teach the claimed limitation above, US Patent No. 8516172 to Karamcheti et al. ("Karamcheti") and/or US Publication No. 20100318879 to Yu ("Yu"), in relevant and complementary manner at the very least obviate such claim limitation; Karamcheti in at least FIG. 7 and at least Column 3, lines 28-41; and Yu in at least paragraph [0057] and at least FIGS. 2, 4-6).

the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory (While the teachings of Gorobets as modified may not expressly teach the claimed limitation above, obviating such claim limitation, CN 101739312 A to Kawaguchi ("Kawaguchi") provides in at least claims 1 and 5: backup data temporarily stored in the volatile memory, keeps the erased area as the backup data in the flash memory, the erased area has no data, and the backup data is written in the erased area ... backing up the backup data newly stored in the said non-volatile memory with recently written in the destination address data comparing the newly storing backup data than the most recently written backup data updating, if the backup data of the most recently written and the newly storing backup data is inconsistent, then the newly storing

backup data from the erased area start address is written in the erased area; and the updating destination address and the start address of the erased area).

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance (While the teachings of Gorobets as modified may not expressly teach the claimed limitation above, obviating such claim limitation, US Publication No. 20110099460 to Dusija et al. ("Dusija") provides in at least paragraphs [0109], [0111-0112], [0116-0117], [0119-0124]).

Claim Objections

4. Claim(s) 1 is objected to because of the following: it is claimed, in part: "the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein, the controller, in at least a Write access operation to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store data in the given one of the MLC nonvolatile memory elements and **retain such stored data in the random access volatile memory**." (emphasis added) However, there is no apparatus, step, function or method that previously or afterwards provides that data is previously stored, written or programmed in the random access volatile memory for such non-existing data to be somehow retained in such volatile memory. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

6. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claim(s) 1-4 and 7-9** is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over US Publication No. 20100172179 to Gorobets et al. ("Gorobets") in view of Publication: "Design Tradeoffs in a Flash Translation Layer" to Goodson et al. ("Goodson"), further in view of US Patent No. 8516172 to Karamcheti et al. ("Karamcheti") and/or US Publication No. 20100318879 to Yu ("Yu"), and further in view of CN 101739312 A to Kawaguchi ("Kawaguchi"), and further in view of US Publication No. 20110099460 to Dusija et al. ("Dusija")

As to **claim 1**, Gorobets teaches substantially the claimed invention, including: A system for storing data (As found in at least FIGS. 1, 8, 12, 15, 20) comprising: memory space containing volatile memory space and nonvolatile memory space (As found in at least FIG. 15: volatile Cache RAM 102, and nonvolatile memory 200), wherein the nonvolatile memory space includes both

multilevel cell (MLC) space and single level cell (SLC) space (As found in at least FIG. 15, MLC 202 and SLC binary cache 204; further, as found in at least [0129]: binary cache configured as one bit of data in each cell); at least one controller to operate memory elements and associated memory space (As found in at least FIGS. 8 and 15, controller 300 or unnumbered "Controller" in FIG. 15 to operate memory 200); at least one MLC nonvolatile memory element; at least one SLC nonvolatile memory element (As found in at least FIGS. 15, 20 and [0129]: 202 and or 2003 including at least one MLC, while 204 and or 2001 including at least one SLC); at least one random access volatile memory element (As found in at least FIG. 15: 102); wherein the at least one controller maintain an address table in one or more of the memory elements (As found in at least FIGS. 8 and 15, and as found in at least [0096]); and wherein the address table maps logical and physical addresses adaptable to the system (As found in at least [0096]), wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories (As found in at least [0152-0154]: mapping defective elements at the cell, sectors, block, or other structural level; lifetime increase by means of spare block management usage).

While Gorobets may not expressly teach an FTL flash translation layer, Goodson, relevantly and complementarily, teaches and documents the purpose and motivation for using FTL for flash memory devices (As set, for example, on the title itself: Design tradeoffs in a flash translation layer, and as found in §§ 1-2: providing purpose of flash translation layer).

Section (3) above in this Office action is incorporated herein fully and completely, and made part of the claim rejection.

Gorobets and Goodso and Karamcheti and Yu and Kawaguchi and Dusija are analogous art because they are from the same filed of endeavor regarding memory devices that may include nonvolatile memory.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to complement the teachings of Gorobets as set forth in this Office action and as found in the reference with the relevant and complementary teachings of Goodson and Karamcheti and Yu and Kawaguchi and Dusija also as set forth in this Office action and as found in the reference. It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Goodson to the teachings of Gorobets such that an FTL (as explained by Goodson) is used with the flash device taught by Gorobets for the purpose of allowing the files system of the flash memory device to maintain the block interface of the disk without sacrificing the tighter integration and control over how the flash is managed and because it hides the complexity of the flash by providing a logical block interface for the flash device. Moreover, volatile memory, including cache memory, typically has a fast operation and is used to collect data fast, data that may in turn be stored in non-volatile memory for further processing; it is an obvious advantage that data written in volatile memory and its copy written in non-volatile memory be one and the same; circuits and methods to compare the two are well-known, well-understood in the art.

Therefore, it would have been obvious to combine Gorobets with Goodson and Karamcheti and Yu and Kawaguchi and Dusija to make the above modification.

As **claim(s) 2 and 9**, Gorobets et al. explain that flash memory is most commonly provided in the form of a memory card (i.e., module or standalone unit as claimed) or a flash drive (i.e., module or standalone unit or hard drive, as claimed) (see background 4] [0015]). Because Gorobets et al. embodiments involve flash memory, the provisions of being a module, standalone device or hard drive, as Claimed, are met.

As to **claim 3**, Gorobets et al. teach at least one of the volatile or nonvolatile memories are embedded in the at least one controller (see Fig. 15 volatile Cache (RAM) 102 is embedded within Controller).

As to **claim 4**, Gorobets et al. teaches the nonvolatile memory (Figs. 15 MLC Memory) is flash memory because the device is a flash memory device (see 4] [0135]; see also, Fig. 15, which labels the memory device as a "Flash Memory Device").

As **claim(s) 7 and 8**, although Gorobets et al. teach the volatile memory (Fig. 15 Cache (RAM) 102), they are silent with respect to the specific type of volatile memory— whether DRAM or SRAM as claimed. Gorobets et al. does not mention or show any aspects of the type of volatile memory employed

OFFICIAL NOTICE is taken that DRAM and SRAM are volatile memory types that have been frequently used as volatile memory in computer systems, and these two types of volatile memory are obvious variants and their tradeoffs are well-documented in the prior art. For example, although SRAM is faster than DRAM, SRAM requires more components per cell because typical prior art CMOS SRAM cell involve six transistors (6T-SRAM), whereas the counterpart typical DRAM cell requires one transistor and one capacitor (1T1C). DRAM, however, has been well-established in the industry as a main memory for computing systems. The real estate required per cell is smaller than that for SRAM, meaning more storage capacity at cheaper cost. The tradeoff is that DRAM must include refresh circuitry to account for decay rate of the capacitors. Although SRAM is typically used for cache memory, DRAM is often employed as well.

It would have obvious to one of ordinary skill in the art before the invention use DRAM or SRAM for the volatile memory as claimed because of the reasons discussed above.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at

least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For

more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claim(s) 1-4 and 7-9 rejected on the ground of nonstatutory double patenting as being unpatentable over claim(s) 1-12 of U.S. Patent No. **10950300**. Although the claims at issue are not identical, they are not patentably distinct from each other because the instant claims are obviated by the patented claims. A later patent claim is not patentably distinct from an earlier patent claim if the later claim is **obvious** over (in a non-statutory double patent rejection) the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were **obvious** over claims in four prior art patents); In re Bercl, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). Ely Lilly and Co. v Bar Laboratories, Inc., United States Court of Appeals for the Federal Circuit, on petition for rehearing en banc (decided: May 30, 2001). Furthermore, the subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application claim obvious common subject matter, wherein the claims of the instant Application and broader renderings of the Patent claims, in brief and saliently: a system for storing data comprising: memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space; at least one controller to operate memory elements and associated memory space; at least one MLC nonvolatile memory element; at least one SLC nonvolatile memory element; at least one random

access volatile memory element; an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements; and wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories. Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to FERNANDO N HIDALGO whose telephone number is (571)270-3306. The examiner can normally be reached M-F 9:00-7:30 ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 5712721852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FERNANDO N. HIDALGO
Primary Examiner
Art Unit 2827

/Fernando Hidalgo/
Primary Examiner, Art Unit 2827

Notice of References Cited	Application/Control No. 17/203,385	Applicant(s)/Patent Under Reexamination Rao, G.R. Mohan	
	Examiner FERNANDO N HIDALGO	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20100172179-A1	07-2010	Gorobets; Sergey Anatolievich	G06F12/0246	365/185.11
*	B	US-8516172-B1	08-2013	Karamcheti; Vijay	G06F11/3058	710/62
*	C	US-20100318879-A1	12-2010	YU; Bum-seok	G06F11/1004	711/105
*	D	US-20110099460-A1	04-2011	Dusija; Gautam Ashok	G11C16/3495	711/E12.001
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N	CN-101739312-A	06-2010	CN	KAWAGUCHI T	G06F12/0246
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/203,385	Rao, G.R. Mohan
	Examiner	**Art Unit**
	FERNANDO N HIDALGO	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/03/2022	09/02/2022							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	-							
	6	✓	-							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/203,385	Filing Date 03/16/2021	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	03/09/2023	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 7	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/JERMAINE D MINOR/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	17203385
Filing Date	16-Mar-2021
First Named Inventor	G.R. Mohan Rao
Attorney Docket Number	VRVN60-35360
Title of Invention	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
VERVAIN, LLC	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

10950300

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.	
Applicant claims the following fee status: ○ Small Entity ○ Micro Entity ◉ Regular Undiscounted I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.	
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application Registration Number 66850 ○ A sole inventor ○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ○ A joint inventor; all of whom are signing this request	
Signature	/William G. Howison, Reg. #66850/
Name	William G. Howison

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	17203385
Filing Date:	16-Mar-2021
Title of Invention:	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Filer:	William G. Howison/Anna Nguyen
Attorney Docket Number:	VRVN60-35360

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	170	170
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**170**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 17203385

Filing Date: 16-Mar-2021

Applicant/Patent under Reexamination: Rao

Electronic Terminal Disclaimer filed on March 9, 2023

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	47656182
Application Number:	17203385
International Application Number:	
Confirmation Number:	6508
Title of Invention:	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	25883
Filer:	William G. Howison/Anna Nguyen
Filer Authorized By:	William G. Howison
Attorney Docket Number:	VRVN60-35360
Receipt Date:	09-MAR-2023
Filing Date:	16-MAR-2021
Time Stamp:	12:12:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$170
RAM confirmation Number	E202339C12205405
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	41475 405440e85fb539c98273b36fce25104764e23d99	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37939 7a360691712f768aaea22102a1d77171e929e38c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	79414		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/30EFS (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	17/203,385	Filing Date	2021-03-16	Docket Number (if applicable)	VRVN60-35360	Art Unit	2827
First Named Inventor	G.R. Mohan Rao			Examiner Name	Fernando N. HIDALGO		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 500208

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

PTO/SB/30EFS (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/William G. Howison, Reg. #66850/	Date (YYYY-MM-DD)	2023-03-09
Name	William G. Howison	Registration Number	66850

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	G. R. Mohan RAO
Serial No.:	17/203,385
Confirmation No.:	6508
Filed:	March 16, 2021
Group:	2827
Examiner:	Fernando N. HIDALGO
For:	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

AMENDMENT AFTER FINAL

This communication is responsive to the Examiner's Office Action dated September 9, 2022. Applicant is submitting herewith a Request for Continued Examination. Applicant requests that any previously non-entered Amendments not be entered.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.
Remarks/Arguments begin on page 5 of this paper.

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space;

a bank of ~~nonvolitile~~ nonvolatile memory, including:

a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and

at least one SLC memory module including at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements;

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of received data therein as stored data, the controller, in at least a Write access operation to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements and retain such received ~~stored~~ data in the random access volatile memory as retained data associated with stored data;

the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at least a Write access operation performed thereon by comparing the stored data in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed on the stored data by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test to achieve enhanced endurance.

2. (Previously Presented) The system of Claim 1, wherein the FTL, flash translation layer, is a software module, or a firmware module containing software updates.

3. (Previously Presented) The system of Claim 1, wherein at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller.

4. (Previously Presented) The system of Claim 1, wherein the MLC and SLC nonvolatile memory elements comprise flash memory.

5. (Cancelled)

6. (Cancelled)

7. (Previously Presented) The system of Claim 1, wherein the random access volatile memory element is dynamic random access memory.

8. (Previously Presented) The system of Claim 1, wherein the random access volatile memory element is static random access memory.

9. (Original) The system of Claim 1, wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD).

REMARKS

Applicant has carefully reviewed the Office Action dated September 9, 2022. Applicant has amended Claim 1 to more clearly point out the present inventive concept. Reconsideration and favorable action is respectfully requested.

Applicant's response to "Response to Arguments"

In the section "Response to Arguments," the Examiner made comments regarding Applicant's inclusion of an argument relating to the *Dusija* reference in the 8/8/22 Response. Even though this was not included in the 2/8/22 Office Action rejection, Applicant felt that a description of this reference would be important to the Examiner and important to the record to ensure that any and all relevant information was considered by the Examiner. Thus, a detailed description of this reference was provided and it was noted that Applicant did not believe that this reference obviated or anticipated the claims. This was a primary purpose for inclusion of this argument. With respect to this Response, Applicant hereby incorporates herein all the arguments with respect to *Dusija* that were provided in the 8/2/2022 Response.

The Examiner commented on the language that was provided in the arguments on page 4 - "Further there is no indication that the remapping of the physical address space will be from a memory element having a relatively lower endurance and another memory element to that another memory element." This particular language should have read as follows: "Further there is no indication that the remapping of the physical address space will be from a memory element having a relatively lower endurance *than* another memory element to that another memory element." This language merely highlights the fact that the remapping operation is from a memory element having determined via an integrity check that the memory element is at the end of life and to then remap the physical address associated with this memory element to a different memory element that is not at the end of life, i.e., the memory has not been written to or read from a sufficient amount of times to wear out that memory element. This is then followed by moving of data from one memory element to the remapped memory element. The improvement of endurance is effected by this remapping operation in that the new memory element is one that has not arguably been used and, as such, it has a longer life.

Claim Objections

The Examiner on Page 7 of the Office Action has objected to the language "retain such stored data in the random access volatile memory." Applicant believes that the Examiner's issue with this language is that there is no support for retaining "stored data." The language of the claim has been changed to the following:

> *the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of received data therein as stored data, the controller, in at least a Write access operation to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements and retain such received ~~stored~~ data in the random access volatile memory as retained data associated with stored data;*

This amended language clearly refers to the fact that what is retained is a copy of the received data wherein, during a Write access operation, the received data is stored in the non-volatile memory as "stored data" and the received data is retained in volatile memory as "retained data."

35 USC §103 Rejection

Claims 1 – 4 and 7 – 9 stand rejected under 35 USC §103(a) as being unpatentable over *Gorobets* in view of the publication *Goodson* and further in view of *Karamcheti, Yu, Kawaguchi* and *Dusija*. This rejection is respectfully traversed with respect to the claims is currently amended.

Gorobets, the primary reference, describes a system for reassigning spare blocks between two different memories. This is best depicted in Figure 20 as follows:

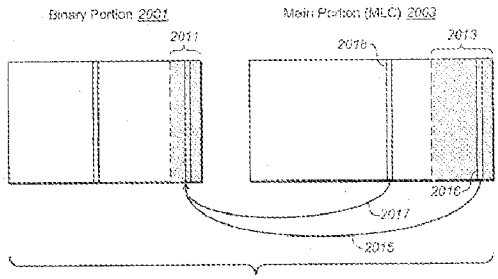


FIG. 20

There is defined a set of spare blocks in a pool of spare blocks (¶[0152]) that can be reassigned. This is best defined in the exemplary embodiment of *Gorobets* as follows:

> [0154] In the exemplary embodiment, a spare block is a free block above the minimum required for system functionality in its normal fashion, where at least one free block is used to perform consolidations and compactions. Additionally, the minimum may include a certain number of blocks which can be used as binary cache block and update blocks, to guarantee certain level of performance. There may be some blocks allocated to be temporary closed update blocks, so that the system does not need to update free block list (FBL) and group access table (GAT) every time a new block is fully written. When the number of free blocks reaches the minimum, the system can then either go to Read-Only mode immediately, or it is possible to use less blocks as update blocks and so on, but this will gradually affect performance. The spare blocks are extra blocks above the predefined minimum and can be described as blocks that can be used to compensate for block failures before the system becomes reduced from its fully functional and, for example, goes into an "end of life" type scenario, such as a Read-Only mode or other measured described in U.S. patent publication number US-2007-0266200-A1.

The primary aspect with respect to how these are transferred is stated that "*the two partitions have separate spare block pools, but spare blocks can be transferred from the pool for the lower endurance MLC partition to the pool for the higher endurance binary partition. This allows for a relatively small pool to be kept for the binary partition, but should the need arise, for blocks to be transferred over form the MLC block pool.*" The embodiment as set forth in Figure 20 is described as follows at ¶[0159]:

> [0159] The concept can be illustrated schematically using FIG. 20. (It will be understood that the arrangement shown is just conceptual and the physical layout on a device need not group all the spare blocks together, etc.) The memory is partitioned into two sections, the binary section 2001 and MLC section 2003. The partition may be a fixed, hard partition or a dynamic or other soft partition. Each partition has spare block pool, shown as 2011 and 2013. The binary spare block pool 2011 is initially assigned few spare blocks, from none to a few, with one or two taken as the exemplary embodiment. The MLC spare block pool

> 2013 initially assigned a larger number of blocks. Some of these initially allotted spare may be lost at testing, being reassigned to cover for bad blocks from the production process. In any case, when the binary section 2001 needs a spare block due to, say, a programming failure, it will first check its own spare block pool 2011 and appropriate the needed block if one is available; if not, it will then request one to be reassigned as shown at 2015 from the MLC spare block pool 2013, which is then treated as the needed binary spare block. If there are no available spares in 2013 to be reassigned, the device goes into end of life mode.

Thus, *Gorobets* is directed to reassigning spare blocks in one section of the memory to spare blocks in another section of the memory. The spare blocks exist primarily to allow for defective memory blocks. (¶[0156]). When a block is found to be defective in one section of the memory, it can be reassigned to the spare block pool of the other section. (¶[0165]). In ¶[0025], *Gorobets* makes the statement that "*in response to determining that a block from the second partition is defective when operating in the second mode, the controller can reassigned to determine block to the first partition to be a spare block usable to replace a defective block in the first section and operated according to the first mode.*" Thus, *Gorobets* does nothing more than reassign blocks once a block is determined to be defective. The Specification of *Gorobets* only refers to the fact that some memory devices "frequently employed defect management procedure and remapped effective elements at the cell, sectors, block, or other structural level." (¶[0152]). There is no description as to how a defect is determined, nor is there any description as to transferring of data from a determined defective block to a spare block. All that is described is the reassignment of spare blocks from one memory to the other to be utilized to solve the problem as stated in ¶[0156] "*however, this would result in the device reaching its end of life scenario when either of the pools is fully used, regardless of the state of the other pool*."

The Examiner has addressed these shortcomings in *Gorobets* in Section (3) of the Office Action.

The Examiner has stated with respect to the Write access operation as follows:

> the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein, the controller, in at least a Write access operation to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store data in the given one of the MLC nonvolatile memory elements and retain such stored data in the random access volatile memory (While the teachings of Gorobets as modified may not expressly teach the claimed limitation above, US Patent No. 8516172 to Karamcheti et al.

("Karamcheti") and/or US Publication No. 20100318879 to Yu ("Yu"), in relevant and complementary manner at the very least obviate such claim limitation; Karamcheti in at least FIG. 7 and at least Column 3, lines 28-41 ; and Yu in at least paragraph [0057] and at least FIGS. 2, 4-6).

Gorobets does not teach any retention of the received data (in the amended claim) in the volatile memory. The Examiner is relying upon the disclosure of *Karamcheti* and *Yu* for the support of this feature.

Karamcheti and *Yu* References

Karamcheti discloses the operation of, during a Write operation, storing the Write data in a backup register (516) for the purpose of a rewrite operation. *Karamcheti* states as follows:

> Computer memory can be error prone. NVRAM may have an error for example when one or two bits in a block are not written properly. This may be due to a worn bit location or from a weak programming voltage during a program cycle. After writing a block, the NVRAM verifies that the block was written properly. If the block was unable to be written without error, a backup write (rewrite) process is provided to get the delayed write data stored to a different block in the same or possibly different NVRAM device. (Col. 18, ll. 1-9)

The determination of whether a Write operation has been successful is first determined and then, if failed, a rewrite is performed from the backup register (516). The information in the backup register or buffer is only used for the rewrite operation and is not used for any type of compare operation. There is no suggestion or disclosure in *Karamcheti* that any data in the NVMD is pulled back up into the controller and utilized for a data integrity check. Rather, the determination of a failure is made at the NVMD. Thus, all that *Karamcheti* discloses is buffering data in a RAM for the purpose of writing to a Flash. This data is not retained in the RAM after writing to the Flash but, rather, it is only buffered or retained in the RAM for the purpose of rewriting when it is determined that data cannot be written to the Flash at that particular sector. Thus, there is no "retained data" that is associated with stored data because, once data is reliably stored, there is no use for the data anymore.

The *Yu* reference discloses the operation of receiving Write data from a host and then determining if this data exists in DRAM. If it does, then the CRC of the received Write data and

the CRC of the data stored in the DRAM are compared. If they are the same, then the corresponding data in the DRAM is compared to the received Write data. However, the actual Write operation to the FLASH is set forth in the description of Figure 2 at ¶ [0035] as follows:

> If the LBA included in the write command SCMD does not exist in the DRAM **180**, the flash memory controller **144** may read the data that is stored in the flash memory **160** at the location indicated by the LBA (**S230**). The data read from the flash memory **160** may then be written to the DRAM **180** (**S240**).

Thus, *Yu* does not "retain" the written data from the host in the DRAM but, rather, first stores it in the FLASH memory, then reads it from the FLASH memory, and then stores it in the DRAM. There is no compare operation of data from the FLASH operation with memory from the DRAM but, rather, only a comparison of data from the DRAM with data received from the host.

Kawaguchi Reference

The Examiner is utilizing the *Kawaguchi* reference in regards to the following statement and the integrity check limitation:

> the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory (While the teachings of Gorobets as modified may not expressly teach the claimed limitation above, obviating such claim limitation, CN 101739312 A to Kawaguchi ("Kawaguchi") provides in at least claims 1 and 5: backup data temporarily stored in the volatile memory, keeps the erased area as the backup data in the flash memory, the erased area has no data, and the backup data is written in the erased area ... backing up the backup data newly stored in the said non-volatile memory with recently written in the destination address data comparing the newly storing backup data than the most recently written backup data updating, if the backup data of the most recently written and the newly storing backup data is inconsistent, then the newly storing backup data from the erased area start address is written in the erased area; and the updating destination address and the start address of the erased area).

The *Kawaguchi* reference is a Chinese reference and is directed to temporarily storing backup data in a volatile memory. An erased area is saved (or reserved) in the flash memory for the backup data. Claim 5 refers to the operation wherein information in the volatile memory that is to be written to the backup area of the flash memory is first compared with information in the flash memory to determine if it is the same. If not, then the data is written to a new area in the

erased area. Claim 5 (which has been obtained from a machine translation from ESpace) is as follows:

> The backup method according to claim 4, further comprising:
>
> comparing backup data newly stored in the volatile memory with backup data most recently written to the destination address, the newly stored backup data being newer than the most recently written backup data;
>
> if the most recently written backup data is inconsistent with the newly stored backup data, writing the newly stored backup data into the erased area from a starting address of the erased area; and
>
> updating the destination address and start address of the erased area.

The overall operation of the backup process is described in the translation of *Kawaguchi* beginning at ¶[0062] as follows:

> In the following, the backup process in normal operation performed by the CPU 1d is explained with reference to the flowchart in FIG. 7.
>
> [0062]
>
> The backup process is repeatedly performed at predetermined intervals.
>
> Like the backup process, the CPU 1d performs updating of the backup data stored in the common storage area of the RAM 1gto the latest obtained backup data at predetermined intervals during the initialization process in normal operation.
>
> In other words, in normal operation, the backup data stored in the common storage area of the RAM 1g is sequentially updated with new backup data.
>
> Hereinafter, the backup process will be described assuming the above-mentioned situation.
>
> [0063]
>
> As shown in Figure 7, during the backup process, the CPU 1d executes a data writing process (step S10) to the flash memory1h.
>
> During the data writing process, the backup data stored in the public storage area of the RAM 1g and the backup data stored in the latest data destination address of the flash memory 1h are compared.
>
> If two kinds of backup data are not consistent (that is, meet predetermined condition), then read the backup data from the public storage area of RAM 1g, and write this backup data sequentially from the starting address of the erased area of flash memory1h Flash 1h.

The actual operation of comparing and rewriting of data to the flash is described beginning at ¶[0064] as follows:

> [0064]

> Specifically, it is assumed that the latest data destination address of the speed data among the backup data stored in the common storage area of the RAM 1g as shown in FIG. 8 is the address of the sector "1002".
>
> In this case, the CPU 1d compares the speed data stored in the common storage area of the RAM 1g with the speed data stored in the sector "1002" of the flash memory 1h.
>
> [0065]
>
> If the two kinds of data are inconsistent, then CPU 1d reads the speed data from the public storage area of RAM 1g, and writes the read speed data into the starting address of the erased area (the address of sector "2002"), As shown in Figure 9.
>
> Simultaneously, the CPU 1d updates the last data destination address of the speed data stored in the RAM 1g to the address of the sector "2002", and also updates the start address of the erased area to the address of the sector "2003".

Kawaguchi discloses an operation wherein incoming data that is defined as backup data is first compared to previously written backup data in a particular written section of the flash. Since flash has to be erased in a particular sector before more information can be written to that location, i.e., overwriting the data, new data has to be written to another sector, but there is no suggestion or disclosure that there is any problem with the integrity of that data in that particular sector; rather, all that is disclosed is that data exists there. Thus, a comparison is made of the data in the RAM with the data in a particular sector, sector "1002" in this example. If the data in this sector does not compare with the data in the RAM, the data in the RAM is then written to a new sector, sector "2002." There is no data integrity check performed to determine if the data in that sector that did not compare true with the data in the RAM. If the result is a bad comparison, all that means is that the data remains in that sector, and therefore the buffered data in the RAM is written to another sector. All that *Kawaguchi* discloses is a check on whether the data to be written already exists within a particular sector and, if not, it is written into another sector.

In the presently claimed embodiment, the data read from the non-volatile memory is compared with data in the volatile memory that is already known to be the same as that in the non-volatile memory. If there is an error between the data read from the non-volatile memory with the data stored in the volatile memory in the currently claimed embodiment, this indicates some issue with the non-volatile memory and, therefore, a remapping operation will have to be performed and the data then transferred from the volatile memory to the non-volatile memory in a different sector.

Dusija Reference

The Examiner is utilizing the *Dusija* reference with reference to the following statement:

> wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance (While the teachings of Gorobets as modified may not expressly teach the claimed limitation above, obviating such claim limitation, US Publication No. 20110099460 to Dusija et al. ("Dusija") provides in at least paragraphs [0109], [0111-0112], [0116-0117], [0119-0124]).

The Examiner has not described how the *Dusija* reference is being applied. However, as noted hereinabove, Applicant has provided a detailed analysis of the *Dusija* reference relative to the claims as previously presented and the limitations thereof, but those arguments are equally applicable to the currently amended claims. However, the Examiner has only utilized this reference with respect to remapping of the data in the FLASH.

It is noted that ¶ ¶ [0119-0124] relate to the description of the operation in Figure 15. This was discussed in detail in the 8/8/2022 Response beginning at Page 10 to the top of Page 12. This particular operation only involves an integrity check which checks the ECC bits with no comparison of any data. There is no need for any comparison operation.

It is also noted that, beginning at the top of Page 12, an alternate embodiment was described wherein a cached copy will replace the first copy in the second portion as valid data. However, this portion of the current rejection only deals with the mapping operation. But there is no suggestion, as set forth in the 8/8/2022 Response, that this mapping is in response to "a failure of the data integrity test performed by *the controller*." *Dusija* does not perform the integrity check at the controller; rather, the integrity check is performed in logic circuitry associated with the Flash, which is architecturally below the operation of the controller.

Examiner's basis for Motivation to Combine

On Page 10 of the 9/9/2022 Office Action, the Examiner has stated that "*Gorobets and Goodso[sic] and Karamcheti and Yu and Kawaguchi and Dusija are analogous art because they*

are from the same filed of endeavor regarding memory devices that may include nonvolatile memory." The only support for this statement is with respect to applying the teachings of Goodson to Gorobets "*for the purpose of allowing the files system of a flash memory device to maintain the block interface of the desk without sacrificing the tighter integration and control over how the flash is managed and because it hides the complexity of the flash by providing a logical block interface for the flash device."* (Page 10 of OA).

With respect to the combination of the references cited by the Examiner:

> the *Gorobets* reference is a reference that is concerned only with reassigning spare blocks. This is done for wearability concerns, but there is no description as to how to detect errors or what to do after an error is detected.
>
> The Examiner is utilizing the *Karamcheti* reference for the writing of data to the memory and retaining of data in the volatile RAM. However, as explained above, *Karamcheti* receives data and buffers it into RAM. It then attempts to write this data to the Flash. If the Write operation fails, then the buffered data in the RAM is written to another location. There is no "retained data" that is associated with any stored data that is maintained in the RAM. There is no need to retain the data once there is a valid Write operation.
>
> The Examiner is also utilizing the *Yu* reference for the writing of data to the memory and retaining of data in the volatile RAM. *Yu* does not "retain" the written data from the host in the DRAM but, rather, first stores it in the FLASH memory and then reads it from the FLASH memory and then stores it in the DRAM. There is no compare operation of data from the FLASH operation with memory from the DRAM but, rather, only a comparison of data from the DRAM with data received from the host.
>
> The Examiner is utilizing the *Kawaguchi* reference for the integrity check wherein a comparison is made at the controller between the retained data and a retrieved copy of the stored data. In *Kawaguchi*, a comparison is made of the data in the RAM with the data in a particular sector. If the data in this sector does not compare with the data in the RAM, the data in the RAM is then written to a new sector. There is no data integrity check performed. All that *Kawaguchi* discloses is a check on whether the data to be written already exists within a particular sector and, if not, write it into another sector.

> The Examiner is utilizing the *Dusija* reference for the purpose of the remapping operation. However, this remapping operation is performed in response to the controller performing the integrity check. There is no such operation by the controller disclosed in *Dusija*.

None of the references cited by the Examiner disclose storing data in the non-volatile memory and retaining a copy of that data as retained data in non-volatile memory and then utilizing the controller to perform a data integrity check by a comparison operation, wherein the comparison operation compares retrieve data from the non-volatile memory with the retained data in the volatile memory. This operation is done at the controller level.

Applicant has now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicant respectfully requests full allowance of the claims as amended.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at whowison@munckwilson.com.

Recognizing that Internet communications are not secure, Applicant hereby authorizes the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application by video conferencing, instant messaging, or electronic mail. Applicant understands that a copy of these communications will be made of record in the application file.

Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 50-0208/VRVN60-35360.

Respectfully submitted,
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Electronic Patent Application Fee Transmittal

Application Number:	17203385
Filing Date:	16-Mar-2021
Title of Invention:	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Filer:	William G. Howison/Anna Nguyen
Attorney Docket Number:	VRVN60-35360

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	1253	1	1480	1480
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1360	1360
		Total in USD ($)		**2840**

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EXAMINER	
HIDALGO, FERNANDO N	

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
03/22/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPdocketing@munckwilson.com
admin@dalpat.com
eofficeaction@appcoll.com

Office Action Summary	Application No. 17/203,385	Applicant(s) Rao, G.R. Mohan	
	Examiner FERNANDO N HIDALGO	Art Unit 2827	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 3/9/23.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-4 and 7-9 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-4 and 7-9 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Examiner's Note

The examiner has cited particular passages including column and line numbers, paragraphs as designated numerically and/or figures as designated numerically in the references as applied to the claims below for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claims, other passages, paragraphs and figures of any and all cited prior art references may apply as well. It is respectfully requested from the applicant, in preparing an eventual response, to fully consider the context of the passages, paragraphs and figures as taught by the prior art and/or cited by the examiner while including in such consideration the cited prior art references in their entirety as potentially teaching all or part of the claimed invention. MPEP 2141.02 VI: "**PRIOR ART MUST BE CONSIDERED IN ITS ENTIRETY, INCLUDING DISCLOSURES THAT TEACH AWAY FROM THE CLAIMS**." MPEP 2123 (I): "**PATENTS ARE RELEVANT AS PRIOR ART FOR ALL THEY CONTAIN**."

Additionally, in an effort to provide a timely Office response to amendments the Applicant may file in response to this Office Action, it is respectfully requested that every effort be made to provide **specific** (page No., paragraph No., FIG. No., etc.) Specification/Drawings support in the instant Application for such amendments on accompanying remarks/arguments filings.

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

2. **Claim(s) 5-6** have been cancelled.

Terminal Disclaimer

3. The terminal disclaimer filed on 3/9/2023 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of **US Patent No. 10950300** has been reviewed and is accepted. The terminal disclaimer has been recorded.

Response to Arguments

4. Applicant's arguments (hereinafter "arguments") filed 3/9/2023 have been fully considered but they are not persuasive, except in partially overcoming previous objections to claim 1; thus, parts of such objections are now withdrawn. Moreover, while the arguments seemingly make no mention of a filing of Terminal Disclaimers (TD) to overcome Double Patenting (DP) claim rejections, such TD has been made of record dated 3/9/2032 and as such previous claim rejections under nonstatutory DP have been overcome, and said DP claim rejection is withdrawn.

The arguments on at least pages 9-10 seem to make an attempt to dispute "Gorobets and Goodso and Karamcheti and Yu and Kawaguchi and Dusija are analogous art because they are from the same filed of endeavor regarding memory devices that may include nonvolatile memory," asserted in Office action dated 9/9/2022. It is not clear whether the arguments dispute that any of the references cited in such Office action teach, among other things, memory devices that may include nonvolatile memory. However, even a cursory study of the cited references uncovers teachings that involve memory that includes nonvolatile memory, and/or flash memory; it is noted here, and only offered for the sake of completeness in view of ample teachings in the record,

that flash memory is nonvolatile memory. That flash memory is nonvolatile memory is not novel, it is not new, the record attests to that.

Lastly, claim amendments dated 3/9/2023 involve only claim 1. Claim 1, as amended, includes, in part: "the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of received data therein as stored data, the controller, in at least a Write access operation to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements and retain such received ~~stored~~ data in the random access volatile memory as retained data associated with stored data;"

It seems the amendments introduced make an attempt to overcome previous claim objection. However, while the claim limitation begins with "the controller," it calls upon "the controller" in the middle of the claim limitation seemingly giving it no purpose, other than to make the claim at the very least objectionable or even rejectable under indefiniteness. Moreover, setting aside the issue of "the controller" in the middle of the claim limitation, the claim limitation, in brief, seems to claim that the controller controls access of nonvolatile and volatile memory elements for storage of received data therein as stored data (note: only data that has been received by memory generally can be stored; if data that **has not** been received by memory generally were possible to be stored in such memory, the state of the art would be quite different, indeed; and it is argued that such scheme is not one the present Application includes). That is, both nonvolatile and volatile memory elements store received data therein as stored data. And that in a write access operation (note: storing data in memory generally is

effectuated in write operations; for example, a read access operation does not effectuate the storing of data in memory), nonvolatile memory elements store the received data and that the received data is retained in the volatile memory elements. That is, both the volatile and nonvolatile memory elements store received data. In sum, while the claim limitation amendments attempt to clarify such claim limitation as previously introduced, and in response to a previous claim objection, the inventive concept behind the claim limitation has not changed, and therefore at the very least **previous claim rejections are still valid and maintained**, as previously presented and made by obviating teachings found in at least: US Patent No. 8516172 to Karamcheti et al. ("Karamcheti") and/or US Publication No. 20100318879 to Yu ("Yu"), in relevant and complementary manner at the very least obviate such claim limitation; Karamcheti in at least FIG. 7 and at least Column 3, lines 28-41; and Yu in at least paragraph [0057] and at least FIGS. 2, 4-6).

Claim 1, as amended, includes, in part: "the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at least a Write access operation performed thereon by comparing the stored data in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;"

For similar reasons set forth above, while the claim limitation amendments attempt to clarify such claim limitation as previously introduced, and in response to a previous claim objection, the inventive concept behind the claim limitation has not

changed, and therefore at the very least **previous claim rejections are still valid and maintained**, as previously presented and made by obviating teachings found in at least: CN 101739312 A to Kawaguchi ("Kawaguchi") as found in at least claims 1 and 5.

Response to Arguments dated 8/8/2022

(maintained herein to make the record whole)

5. Applicant's arguments(hereinafter "arguments") filed 8/8/2022 have been fully considered but they are not persuasive. Additionally, applicant's arguments with respect to claim(s) 1-4 and 7-9 have been considered but are moot because the new ground of rejection does not rely on any reference applied in the prior rejection of record for any teaching or matter specifically challenged in the argument. At the outset, it is noted that the arguments include analysis/discussion on the "Dusija" reference. The Office action dated 2/8/2022, which presumably the arguments are a response to, does not include any reference at all about the Dusija reference; no claim rejection or objection, or anything at all of any kind is based on any teachings the Dusija reference may include. It would seem the inclusion in the arguments of analysis/discussion of the Dusija reference is an attempt to preemptively disqualify such reference from being considered in any claim rejection/objection as teachings any obviating or anticipating subject matter that may potentially be claimed, be claimed in the future. The arguments on page 16 expressly submit: "Applicant believes that Dusiji, taken alone or in combination with **any cited reference**, does not anticipate or render obvious any of the currently amended claims." (emphasis added) Thus, it would seem the arguments have already unilaterally and preemptively decided that the Dusija reference, a reference not cited at all in any prior Office action, is henceforth disqualified even in combination with **any cited**

reference, presumably even reference that may cited down the road along prosecution of the instant Application. This cannot be.

Moreover, in traversing the rejection to claim 1, at least based on the actual references cited in the prior Office action, the arguments on page 4 submit: "Further, there is no indication that the remapping of the physical address space will be from a memory element having a relatively lower endurance in another memory element to that another memory element." Firstly, "remapping of the physical address space will be from a memory element having a relatively lower endurance in another memory element to that another memory element," makes absolutely no sense whatever. An attempt to summarize this sentence between quotation marks is as follows: remapping … from a memory element … in another memory element to that another memory element. If this makes sense, an invitation is made herein for a response explaining its meaning. Secondly, even if the sentence above between quotation marks makes sense, and this is not conceded at all, Whether the alleged "remapping" -the claim includes mapping- is from memory having a relatively lower endurance, the claim as amended dated 8/8/2022 does not make such requirement. There is no clam at all of remapping from memory having lower endurance. It would seem the arguments would like the impermissible importation of subject matter from the specification into the claim. (2111 MPEP) If this subject matter is important to the invention, and provided it does find support in the specification, such subject matter is invited to be made part of the claims.

Furthermore, the arguments on page 4 also submit: "The Gorobets reference does not disclose or suggest a remapping operation wherein the remapping operation is for the purpose of improving the endurance. Rather, all that the Gorobets reference

does is remap for wearability in accordance with a wearability algorithm." Whether the Gorobets reference **all it does** is remapping wearability according to a wearability algorithm, is merely an allegation, one without weight since the invention as claimed does not concern such allegation. However, on whether the Gorobets reference teaches remapping for the purpose of improving endurance, this has already been addressed in the prior Office action, and as found in at least paragraphs [0152-0154]: "The result is a **limited effective lifetime of the memory cells**; that is, memory cell eventual fail to operate properly, usually failing to program or erase properly... To account for this, memory devices frequently employ defect management procedure and **remap defective elements** at the cell, sectors, block, or other structural level." (emphasis added)

The prior Office action dated 2/8/2022 includes nonstatutory double patenting claim rejections. The arguments provide, it would seem, no response of any kind to these claim rejections. Absence of any relevant response in the arguments does not make such double patenting claim rejections conveniently go away. The double patenting claim rejection is thus maintained and set forth below in this Office action.

In regard to newly introduced claim limitations dated 8/8/2022:

a bank of nonvolitile memory, including: a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element[[;]], and at least one SLC memory module including at least one SLC nonvolatile memory element (As found in at least FIG. 15, at least paragraphs [0090], [0135] in the teachings of Gorobets: the memory 200 is organized into blocks; and that 200 is partitioned into MLC modules an LSC memory modules (SLC is described as binary mode cells; also refer to [0108]).

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein, the controller, in at least a Write access operation to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store data in the given one of the MLC nonvolatile memory elements and retain such stored data in the random access volatile memory (While the teachings of Gorobets as modified may not expressly teach the claimed limitation above, US Patent No. 8516172 to Karamcheti et al. ("Karamcheti") and/or US Publication No. 20100318879 to Yu ("Yu"), in relevant and complementary manner at the very least obviate such claim limitation; Karamcheti in at least FIG. 7 and at least Column 3, lines 28-41; and Yu in at least paragraph [0057] and at least FIGS. 2, 4-6).

the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory (While the teachings of Gorobets as modified may not expressly teach the claimed limitation above, obviating such claim limitation, CN 101739312 A to Kawaguchi ("Kawaguchi") provides in at least claims 1 and 5: backup data temporarily stored in the volatile memory, keeps the erased area as the backup data in the flash memory, the erased area has no data, and the backup data is written in the erased area ... backing up the backup data newly stored in the said non-volatile memory with recently written in the destination address data comparing the newly storing backup data than the most recently written backup data updating, if the backup data of the most recently written

and the newly storing backup data is inconsistent, then the newly storing backup data from the erased area start address is written in the erased area; and the updating destination address and the start address of the erased area).

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance (While the teachings of Gorobets as modified may not expressly teach the claimed limitation above, obviating such claim limitation, US Publication No. 20110099460 to Dusija et al. ("Dusija") provides in at least paragraphs [0109], [0111-0112], [0116-0117], [0119-0124]).

Claim Objections

6. Claim(s) 1 is objected to because of the following: it is claimed, in part: "the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of received data therein as stored data, the controller, in at least a Write access operation to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements and retain such received ~~stored~~ data in the random access volatile memory as retained data associated with stored data;" **For analysis and reasons for this claim objection, section three (3) above is referenced herein fully and completely and made integral part of this claim objection.**

Claim Rejections - 35 USC § 112

7. The following is a quotation of 35 U.S.C. 112(b):

> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

> The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claim(s) 1** is rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention. **For analysis and reasons for this claim objection, section three (3) above is referenced herein fully and completely and made integral part of this claim rejection.**

9. **Claim(s) 2-4 and 7-9** depend from claim 1 and as such are also rejected for the same reasons.

Claim Rejections - 35 USC § 103

10. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

11. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the

time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. **Claim(s) 1-4 and 7-9** is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over US Publication No. 20100172179 to Gorobets et al. ("Gorobets") in view of Publication: "Design Tradeoffs in a Flash Translation Layer" to Goodson et al. ("Goodson"), further in view of US Patent No. 8516172 to Karamcheti et al. ("Karamcheti") and/or US Publication No. 20100318879 to Yu ("Yu"), and further in view of CN 101739312 A to Kawaguchi ("Kawaguchi"), and further in view of US Publication No. 20110099460 to Dusija et al. ("Dusija")

As to **claim 1**, Gorobets teaches substantially the claimed invention, including: A system for storing data (As found in at least FIGS. 1, 8, 12, 15, 20) comprising: memory space containing volatile memory space and nonvolatile memory space (As found in at least FIG. 15: volatile Cache RAM 102, and nonvolatile memory 200), wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space (As found in at least FIG. 15, MLC 202 and SLC binary cache 204; further, as found in at least [0129]: binary cache configured as one bit of data in each cell); at least one controller to operate memory elements and associated memory space (As found in at least FIGS. 8 and 15, controller 300 or unnumbered "Controller" in FIG. 15 to operate memory 200); at least one MLC nonvolatile memory element; at least one SLC nonvolatile memory element (As found in at least FIGS. 15, 20 and [0129]: 202 and or 2003 including at least one MLC, while 204 and or 2001 including at least one SLC); at least one random access volatile memory element (As found in at least FIG. 15: 102); wherein the at least one controller maintain an address table

in one or more of the memory elements (As found in at least FIGS. 8 and 15, and as found in at least [0096]); and wherein the address table maps logical and physical addresses adaptable to the system (As found in at least [0096]), wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories (As found in at least [0152-0154]:

mapping defective elements at the cell, sectors, block, or other structural level; lifetime increase by means of spare block management usage).

While Gorobets may not expressly teach an FTL flash translation layer, Goodson, relevantly and complementarily, teaches and documents the purpose and motivation for using FTL for flash memory devices (As set, for example, on the title itself: Design tradeoffs in a flash translation layer, and as found in §§ 1-2: providing purpose of flash translation layer).

Section (4) and (5) above in this Office action is incorporated herein fully and completely, and made part of the claim rejection.

Gorobets and Goodso and Karamcheti and Yu and Kawaguchi and Dusija are analogous art because they are from the same filed of endeavor regarding memory devices that may include nonvolatile memory.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to complement the teachings of Gorobets as set forth in this Office action and as found in the reference with the relevant and complementary teachings of Goodson and Karamcheti and Yu and Kawaguchi and Dusija also as set forth in this Office action and as found in the reference. It

would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Goodson to the teachings of Gorobets such that an FTL (as explained by Goodson) is used with the flash device taught by Gorobets for the purpose of allowing the files system of the flash memory device to maintain the block interface of the disk without sacrificing the tighter integration and control over how the flash is managed and because it hides the complexity of the flash by providing a logical block interface for the flash device. Moreover, volatile memory, including cache memory, typically has a fast operation and is used to collect data fast, data that may in turn be stored in non-volatile memory for further processing; it is an obvious advantage that data written in volatile memory and its copy written in non-volatile memory be one and the same; circuits and methods to compare the two are well-known, well-understood in the art.

Therefore, it would have been obvious to combine Gorobets with Goodson and Karamcheti and Yu and Kawaguchi and Dusija to make the above modification.

As **claim(s) 2 and 9**, Gorobets et al. explain that flash memory is most commonly provided in the form of a memory card (i.e., module or standalone unit as claimed) or a flash drive (i.e., module or standalone unit or hard drive, as claimed) (see background 4] [0015]). Because Gorobets et al. embodiments involve flash memory, the provisions of being a module, standalone device or hard drive, as Claimed, are met.

As to **claim 3**, Gorobets et al. teach at least one of the volatile or nonvolatile memories are embedded in the at least one controller (see Fig. 15 volatile Cache (RAM) 102 is embedded within Controller).

As to **claim 4**, Gorobets et al. teaches the nonvolatile memory (Figs. 15 MLC Memory) is flash memory because the device is a flash memory device (see 4] [0135]; see also, Fig. 15, which labels the memory device as a "Flash Memory Device").

As **claim(s) 7 and 8**, although Gorobets et al. teach the volatile memory (Fig. 15 Cache (RAM) 102), they are silent with respect to the specific type of volatile memory— whether DRAM or SRAM as claimed. Gorobets et al. does not mention or show any aspects of the type of volatile memory employed

OFFICIAL NOTICE is taken that DRAM and SRAM are volatile memory types that have been frequently used as volatile memory in computer systems, and these two types of volatile memory are obvious variants and their tradeoffs are well-documented in the prior art. For example, although SRAM is faster than DRAM, SRAM requires more components per cell because typical prior art CMOS SRAM cell involve six transistors (6T-SRAM), whereas the counterpart typical DRAM cell requires one transistor and one capacitor (1T1C). DRAM, however, has been well-established in the industry as a main memory for computing systems. The real estate required per cell is smaller than that for SRAM, meaning more storage capacity at cheaper cost. The tradeoff is that DRAM must include refresh circuitry to account for decay rate of the capacitors.

Although SRAM is typically used for cache memory, DRAM is often employed as well.

It would have obvious to one of ordinary skill in the art before the invention use DRAM or SRAM for the volatile memory as claimed because of the reasons discussed above.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to FERNANDO N HIDALGO whose telephone number is (571)270-3306. The examiner can normally be reached M-F 9:00-7:30 ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 5712721852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For

additional questions, contact the Electronic Business Center (EBC) at 866-217-9197

(toll-free). If you would like assistance from a USPTO Customer Service

Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FERNANDO N. HIDALGO
Primary Examiner
Art Unit 2827

/Fernando Hidalgo/
Primary Examiner, Art Unit 2827

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/203,385	Rao, G.R. Mohan
	Examiner	Art Unit
	FERNANDO N HIDALGO	2827

CPC - Searched*		
Symbol	Date	Examiner
G11C11/5635 OR G06F11/1068 OR G06F11/1072 OR G06F12/0246 OR G11C11/5621 OR G11C11/5678 OR G11C16/16 OR G11C16/3495 OR G11C29/52 OR G11C29/76 OR G06F2212/7202 OR G11C2211/5641	02/03/2022	fh
(G11C11/5635 OR G06F11/1068 OR G06F11/1072 OR G06F12/0246 OR G11C11/5621 OR G11C11/5678 OR G11C16/16 OR G11C16/3495 OR G11C29/52 OR G11C29/76 OR G06F2212/7202 OR G11C2211/5641)	09/02/2022	fh
(G11C11/5635 or G06F11/1068 or G06F11/1072 or G06F12/0246 or G11C11/5621 or G11C11/5678 or G11C16/16 or G11C16/3495 or G11C29/52 or G11C29/76 or G06F2212/7202 or G11C2211/5641)	03/17/2023	fh

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
365	185.03	02/03/2022	fh

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/Fernando Hidalgo/ Primary Examiner, Art Unit 2827	

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PGR2025-00010

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/203,385	Rao, G.R. Mohan
	Examiner	Art Unit
	FERNANDO N HIDALGO	2827

Search Notes		
Search Notes	**Date**	**Examiner**
searched PE2E	02/03/2022	fh
searched: inventor, assignee, inventive concept, cpc, ccls	02/03/2022	fh
searched: inventor, assignee, inventive concept, cpc, ccls	09/02/2022	fh
IPR2021-01550 Reviewed Inter Partes Review of US Patent No. 10950300	09/02/2022	fh
IPR2021-01550 Reviewed Inter Partes Review of US Patent No. 10950300	03/17/2023	fh
consulted with David J. Makiya and Amir Zarabian on IPR	03/17/2023	fh

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**

/Fernando Hidalgo/ Primary Examiner, Art Unit 2827	

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PGR2025-00010

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/203,385	Rao, G.R. Mohan
	Examiner	**Art Unit**
	FERNANDO N HIDALGO	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/03/2022	09/02/2022	03/17/2023						
	1	✓	✓	✓						
	2	✓	✓	✓						
	3	✓	✓	✓						
	4	✓	✓	✓						
	5	✓	-	-						
	6	✓	-	-						
	7	✓	✓	✓						
	8	✓	✓	✓						
	9	✓	✓	✓						

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-22)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17203385
Filing Date	2021-03-16
First Named Inventor	G.R. Mohan Rao
Art Unit	2827
Examiner Name	Fernando N. HIDALGO
Attorney Docket Number	VRVN60-35360

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	101739312	CN	A	2010-06-16	Kawaguchi		X

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /FH/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17203385
Filing Date	2021-03-16
First Named Inventor	G.R. Mohan Rao
Art Unit	2827
Examiner Name	Fernando N. HIDALGO
Attorney Docket Number	VRVN60-35360

	1	IPR2021-01550 Exhibit 1071 Micron's Hearing Demonstratives	
	2	IPR2021-01550 Exhibit 2020 Remote Deposition of Dr. David Liu	
	3	IPR2021-01550 Patent Owner's Notice of Deposition of Dr. David Liu	
	4	IPR2021-01550 Patent Owner's Request for Oral Argument	
	5	IPR2021-01550 Patent Owner's Sur-Reply	
	6	IPR2021-01550 Petitioner's Notice of Deposition of Dr. Sunil P. Khatri	

If you wish to add additional non-patent literature document citation information please click the Add button [Add]

EXAMINER SIGNATURE

Examiner Signature	/Fernando Hidalgo/ (03/17/2023)	Date Considered	03/17/2023

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17203385
Filing Date	2021-03-16
First Named Inventor	G.R. Mohan Rao
Art Unit	2827
Examiner Name	Fernando N. HIDALGO
Attorney Docket Number	VRVN60-35360

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/William G. Howiosn, Reg. #66850/	Date (YYYY-MM-DD)	2023-03-09
Name/Print	William G. Howison	Registration Number	66850

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	G. R. Mohan Rao
Serial No.:	17/203,385
Confirmation No.:	6508
Filed:	March 16, 2021
Group:	2827
Examiner:	Fernando N. HIDALGO
For:	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

AMENDMENT AND RESPONSE TO OFFICE ACTION

This communication is responsive to the Examiner's Office Action dated March 22, 2023. Applicant requests that any previously non-entered Amendments not be entered. Reconsideration is respectfully requested.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements;

a bank of nonvolatile memory, including:

a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and

at least one SLC memory module including at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements;

the controller having associated controller memory for storing received data therein, the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data;

the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of

the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed on the stored data by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the retained ~~stored~~ data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test ~~to achieve enhanced endurance~~.

2. (Previously Presented) The system of Claim 1, wherein the FTL, flash translation layer, is a software module, or a firmware module containing software updates.

3. (Previously Presented) The system of Claim 1, wherein at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller.

4. (Previously Presented) The system of Claim 1, wherein the MLC and SLC nonvolatile memory elements comprise flash memory.

5. (Cancelled)

6. (Cancelled)

7. (Previously Presented) The system of Claim 1, wherein the random access volatile memory element is dynamic random access memory.

8. (Previously Presented) The system of Claim 1, wherein the random access volatile memory element is static random access memory.

9. (Original) The system of Claim 1, wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD).

REMARKS

Applicant has carefully reviewed the Office Action dated March 22, 2023. Applicant has amended Claim 1 to more clearly point out the present inventive concept. Reconsideration and favorable action is respectfully requested.

35 USC §112 Rejection

The Examiner has rejected Claim(s) 1 135 USC §112(b) as being indefinite for failing to particularly point out and distantly claim the subject matter which the inventor regards as the invention. The Examiner has specifically referred to section three (3) in the current Office Action. However, applicant believes that the Examiner was referring to section four (4), as section three (3) refers to the acceptance of the Terminal Disclaimer. This rejection is respectfully traversed with respect to the claims as currently amended, the withdrawal of which is respectfully requested.

In the Examiner's Response in section 4, the Examiner commented on the fact that the "controller" as set forth in the claim had no purpose in the original claim and the purpose was arguably defined in the middle section of the claim. However, the original claim language for introducing the term "controller" is as follows:

at least one controller to operate memory elements and associated memory space

the operation of the "controller" in the middle of the claim previously presented was set forth as follows:

> *the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of received data therein as stored data, the controller, in at least a Write access operation to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements and retain such*

received data in the random access volatile memory as retained data associated with stored data;

the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at least a Write access operation performed thereon by comparing the stored data in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

Thus, the "controller" is first defined as "to operate memory elements and associated memory space" and then further functioning for "controlling access of the nonvolatile memory elements and the random access volatile memory elements for storage of received data therein." For clarity, Claim 1 has been amended as follows:

at least one controller to operate memory elements and associated memory space <u>for associated Write access operations to the memory elements and Read access operations from the memory elements</u>;

This clarification is believed to overcome the Examiner's objection to the structure of the claim.

The Examiner had set forth in section eight (8) the following with respect to the 35 USC §112 rejection:

> 8. Claim(s) 1 is rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention. **For analysis and reasons for this claim objection, section three (3) above is referenced herein fully and completely and made integral part of this claim rejection.**

The Examiner has further made the comment in section four (4):

> Moreover, setting aside the issue of "the controller" in the middle of the claim limitation, the claim limitation, in brief, seems to claim that the controller controls access of nonvolatile and volatile memory elements for storage of received data therein as stored data (note: only data that has been received by memory generally can be stored; if data that has not been received by memory generally were possible to be stored in such memory, the state of the art would be quite different, indeed; and it is argued that such scheme is not one the present Application includes). That is, both nonvolatile and volatile memory elements store received data therein as stored data. And that in a write access operation (note: storing data in memory generally is effectuated in write operations; for example, a read access operation does not effectuate the storing of data in memory), nonvolatile memory elements store the received data and that the received data is retained in the volatile memory elements. That is, both the volatile and nonvolatile memory elements store received data.

In general, Applicant believes the Examiner is considering that the language of storing "received data" as "stored data" makes the claim indefinite. However, Applicant argues that, when data is received by a memory, what is actually stored in a particular memory element may not be the actual received data. In some memories, such as volatile memories, i.e., the DRAMs, error correction bits can be added before storeage of any data bit therein, such that any errors or faults in the memory elements, i.e., a bad memory element resulting in an incorrectly stored bit, can be tolerated. Subsequent reading out of this stored data results in corrected data that accurately matches the received data, the point being that the stored data may not actually completely match the data received by the memory. In a similar manner, it is recognized that FLASH nonvolatile memory has an issue as to wearability, wherein certain portions of the memory will wear out as a result of multiple Writes, resulting in bad memory elements. Thus, error correction bits can be added to account for faulty memory elements to tolerate a certain number of bad memory elements or, as is the purpose for the present invention set forth in the current application, data can just be written to another area of the memory and that faulty portion of the memory marked as a bad section of the physical memory. In any event, it should be recognized that the "stored data" may not actually be the exact "received data" due to possible faulty memory elements. For example, received data with a value of "10001010" could be first written to the memory and then read out as a value of "100X1010" with the fifth bit being in error due to a faulty memory element at that location. Thus, what is stored is not actually the received data. The language of the claim prior to the current amendments:

the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at

least a Write access operation performed thereon by comparing the stored data in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

sets forth that the controller compares the "stored data" with the "retained data" during a Write access operation. If the integrity check fails, then a remapping operation ensues. If the "stored data" was in fact the "retained data," which "retained data" is the "received data," the integrity check would never fail. Thus, Applicant believes that there is no indefiniteness with respect to defining "stored data" as being different from "received data." Applicant respectfully requests withdrawal of the 35 USC §112 rejection respect to Claim 1 on this basis.

35 USC §103 Rejection

Claims 1 – 4 and 7 – 9 stand rejected under 35 USC §103(a) over *Gorobets* in view of *Goodson* and further in view of *Karamcheti* and/or *Yu* and further in view of *Kawaguchi* and further in view of *Dusija*. This rejection is respectfully traversed in view of the claims as currently amended.

The Examiner has noted the following with respect to the arguments in section four (4) as follows:

> a bank of nonvolitile memory, including: a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element[[;]], and at least one SLC memory module including at least one SLC nonvolatile memory element (As found in at least FIG. 15, at least paragraphs [0090], [0135] in the teachings of Gorobets: the memory 200 is organized into blocks; and that 200 is partitioned into MLC modules an LSC memory modules (SLC is described as binary mode cells; also refer to [0108]).

Applicant believes that this may be an incorrect interpretation of the claim. The claim requires that there be a plurality of separate MLC memory modules and at least one SLC memory module in the bank of nonvolatile memory. This relates to Figure 4 of current application:

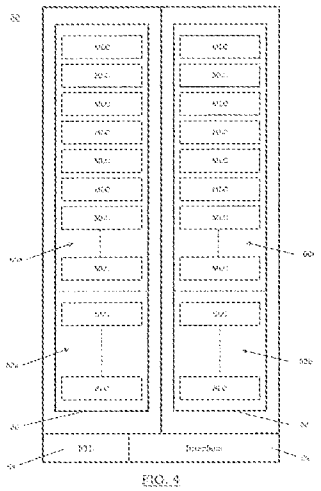


FIG. 4

Gorobets at ¶[0090} states that "[t]he memory 200 is organized into blocks, each block of cells being a minimum unit of erase." Thus, a block can only be either an MLC memory block or SLC memory block. Since this is a minimum unit of erase, a block can only exist in one of the memories and calm not include both SLC and MLC memory elements. Applicant believes that *Dusija* is a better reference for this aspect in Figure 1 as follows:

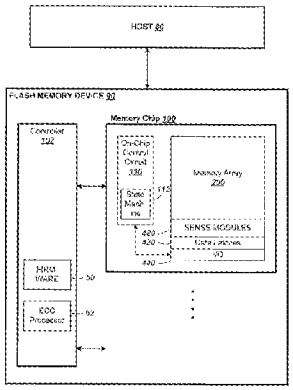


FIG. 1

Karamcheti and *Yu* References

The Examiner's next argument relates to the retained data aspect of the claim in volatile memory. The Examiner stated as follows in section four (4) as follows:

> the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein, the controller, in at least a Write access operation to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store data in the given one of the MLC nonvolatile memory elements and retain such stored data in the random access volatile memory (While the teachings of Gorobets as modified may not expressly teach the claimed limitation above, US Patent No. 8516172 to Karamcheti et al. ("Karamcheti") and/or US Publication No. 20100318879 to Yu ("Yu"), in relevant and complementary manner at the very least obviate such claim limitation; Karamcheti in at least FIG. 7 and at least Column 3, lines 28-41 ; and Yu in at least paragraph [0057] and at least FIGS. 2, 4-6).

The Examiner is noted that *Gorobets* does not expressly teach this limitation. This rejection was specifically responded to and the Response filed 3/9/23. The following was set forth by Applicant in that Response with respect to *Karamcheti* and *Yu* on pages 9 and 10:

> The determination of whether a Write operation has been successful is first determined and then, if failed, a rewrite is performed from the backup register (516). The information in the backup register or buffer is only used for the rewrite operation and is not used for any type of compare operation. There is no suggestion or disclosure in *Karamcheti* that any data in the NVMD is pulled back up into the controller and utilized for a data integrity check. Rather, the determination of a failure is made at the NVMD. Thus, all that *Karamcheti* discloses is buffering data in a RAM for the purpose of writing to a Flash. This data is not retained in the RAM after writing to the Flash but, rather, it is only buffered or retained in the RAM for the purpose of rewriting when it is determined that data cannot be written to the Flash at that particular sector. Thus, there is no "retained data" that is associated with stored data because, once data is reliably stored, there is no use for the data anymore.
>
> ...
>
> Thus, *Yu* does not "retain" the written data from the host in the DRAM but, rather, first stores it in the FLASH memory, then reads it from the FLASH memory, and then stores it in the DRAM. There is no compare operation of data from the FLASH operation with memory from the DRAM but, rather, only a comparison of data from the DRAM with data received from the host.

Applicant had made the argument that the combination of these two references *Karamcheti* and *Yu* does not disclose the limitation of the "retained data" in the volatile memory as a part of the Write access operation. Claim 1 had been amended as follows with respect to the "retained data":

> *the controller having associated controller memory for storing received data therein, the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored*

data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data;

These amendments are supported by the following language in the Specification as filed:

> FIGS. 3A and 3B are a flow chart illustrating a method for utilizing a NAND flash memory system incorporating one embodiment of the present disclosure. The method begins in a step 100, when a command to write a quantum of data stored in DRAM to a particular location in NAND flash memory is received, in step 102, the quantum of data is read from DRAM into memory within the device controller (which acts as the memory controller). In step 104, both the logical address range and the NAND flash physical address range to which the quantum of data is to be written, is read into memory of the device controller. In step 106, the quantum of data to be written is combined with the contents of the NAND flash memory. In step 108, the NAND flash physical address range to be written is erased. In step 110, the combined data is written to the appropriate NAND flash physical address range. In step 112 the NAND flash physical address range that was written in step 110 is read into device controller memory.

In accordance with the Specification, there is provided a DRAM for storage of received data therein, but a Write access operation also loads the received data to be stored "into memory of the device controller." The contents of the controller memory are then written to the FLASH. This is then followed by a step wherein the stored data is read back into the controller memory. The Specification then sets forth the following:

> The flowchart continues in FIG. 3B. In step **114** the NAND flash physical address range that was read into device controller memory is compared with the retained data representing the combination of the previous contents of the physical address range and the quantum of data to be written. …

Thus, there is required at least a controller memory that is used in the Write access operation and a copy of the data from the DRAM, i.e., two data stores.

Karamcheti is a reference that operates during a Write Access to Receive Data - Buffer in RAM - Write to FLASH – Verify - Rewrite on Verify. The Verify operation does not involve any compare operation and, if fact, there is no compare operation. The data is maintained in the buffer,

but only for the purpose of a Write operation to the FLASH. Even though it may be held there for multiple Writes, the data is only designated for a single Write. There is no suggestion this buffer could be used for a data store in a compare operation as the data is *discarded* after a Write is complete.

Yu is an operation that has the primary purpose of reducing the number of data programming operations required for multiple Writes (¶[0053]):

> [0053] As described above with reference to the storage device 100 and the data storing method 200 according certain embodiments of the inventive concept, the write data received from the host is filtered in order to avoid performing a programming operation for the write data when it is already similarly stored in the flash memory 160. Using this write data filtering approach, the number of data programming operations directed to the flash memory 160 may be reduced, and the write endurance of the flash memory 160 may be extended. As described above, if the write endurance of the flash memory 160 is improved, the reliability of the storage device 100 including the flash memory 160 and the lifespan of the storage device 100 may be increased.

During a Write access operation, volatile memory such as RAM is utilized to determine whether data already exists in Flash. This is thus an operation of Receive Data – Verify Data not already stored in FLASH – Write to FLASH if not already stored. There is no operation to determine if data written to FLASH memory is corrupt by comparing to retained data and then rewriting the data from the retained data to a different location in FLASH. The purpose of *Yu* is completely different than the purpose set forth in the current application which is related to first writing data to a FLASH location than, if failed, rewriting that data from a retained data location in volatile memory to another location in FLASH. It is clear that *Yu* does not disclose or suggest a Receive – Retain (in volatile memory) – Write (from controller memory) – Read (to controller memory) – Compare (data in controller memory to retained data in volatile memory) – Rewrite operation. Rather, *Yu* actually teaches against performing a Write operation before any comparison operation. The specific reasoning in *Yu* is to actually reduce the number of data programming operations.

Kawaguchi Reference

The Examiner with respect to the next element of the Claim 1 presented the following argument on Pages 9 - 10 of the current Office Action:

> the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory (While the teachings of Gorobets as modified may not expressly teach the claimed limitation above, obviating such claim limitation, CN 101739312 A to Kawaguchi ("Kawaguchi") provides in at least claims 1 and 5: backup data temporarily stored in the volatile memory, keeps the erased area as the backup data in the flash memory, the erased area has no data, and the backup data is written in the erased area ... backing up the backup data newly stored in the said non-volatile memory with recently written in the destination address data comparing the newly storing backup data than the most recently written backup data updating, if the backup data of the most recently written and the newly storing backup data is inconsistent, then the newly storing backup data from the erased area start address is written in the erased area; and the updating destination address and the start address of the erased area).

Claim 1 has been amended with respect to this limitation as follows:

> *the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;*

In this Amendment, the data is first read to the "controller memory" and then this read data stored in the controller memory is compared to the retained data. This thus requires two data stores. This Amendment is supported by the following portion of the Specification:

> The flowchart continues in FIG. 3B. In step **114** the NAND flash physical address range that was read into device controller memory is compared with the retained data representing the combination of the previous contents of the physical address range and the quantum of data to be written. In step **116** if the retained data matches the newly stored data in the NAND flash memory, the write was a success, and the method exits in step **118**. However, if the retained data does not match the newly stored data in the NAND flash memory, the method executes step **120**, which identifies the next quantum of available SLC NAND flash memory addresses.

Kawaguchi is a new reference and the Examiner has only provided the translation of the claims in support of the rejection with respect to such language. Applicant has had the full Patent translated and provided such as part of the record.

The problem that *Kawaguchi* is faced with is dealing with increased amounts of backup data when monitoring a system such as an automobile, wherein a solution to this increased amount of backup data is to utilize a Flash memory, which would be more desirable than what was used before, EEPROM memory. ¶[0008]. Flash memory is desirable from the standpoint that it is faster to write to as compared to EEPROM. The problem though, is that the number of times it can be written to is less than EEPROM. ¶[0009]. One issue with Flash memory that is noted is that the erasing and writing of data to a particular location can take a long time. The solution is to temporarily store the data in the volatile memory, i.e., RAM, reserve erased areas in the Flash memory for backup data and then write the backup data into a different erased area for each backup operation. ¶[0011].

The overall backup operation includes a comparison step, which is what the Examiner has referred to with respect to the current Rejection. Current Claim 1 requires that *after a Write access operation of the received data,* and as part of a data integrity check, a Read operation is performed on that written and stored data followed by a compare operation with the retained data stored in volatile memory. If the compare operation is True, then the data integrity check has passed. If False, then the retained data in a volatile memory is then rewritten to another physical location after remapping, it being noted that the same logical address applies to the Write access operation after remapping. Thus, the operation is to – 1) Receive data, 2) Write the received data into volatile memory as retained data and into the Flash as stored data, 3) Read the stored data from Flash and transfer to the controller for comparison with the stored retained data in the volatile memory, 4) If True, do nothing and, if False, remap the logical address to a different physical address, and 5) rewrite the retained data from the volatile memory through the controller to the new physical address, but at the same logical address.

In *Kawaguchi*, the primary purpose of the overall system is to store backup data in nonvolatile memory. Backup data is continually collected and temporarily stored in RAM - volatile memory. This is a periodic operation. This all occurs based upon some type of predetermined

condition as a trigger. ¶[0046]. The backup operation is described with respect to Figure 7 and ¶[0062]. From the Specification, the operation is to backup the collected data in the RAM to the Flash in an area that has been erased, i.e., a free (erased) area. In this manner, it is faster to just Write to a free area rather than perform an erase followed by a Write operation. This just requires a large number of erased sectors which can be sequentially written-two on subsequent Writes. Of course, once the Flash has filled up, is a necessary to erase the contents. It is noted that only one sector will actually have any viable data that is useful, as all of the old sectors that are not erased or free have old backup data stored therein. It is more efficient to just do a bulk erase at some periodic interval for a portion of the Flash when the Flash is determined to be reaching its limit.

A destination address of a designated sector in the Flash is maintained such that, when it is determined that data is to be transferred from the volatile memory to the Flash, i.e., a trigger, that destination address is initially utilized to access the Flash for a Read operation of the previously stored backup information. This particular destination address is the last address to which data was written to the Flash. The reason for this is that it is desirable to determine if the last Write of information resulted in information stored therein that has not changed in the RAM or volatile memory at the current time, i.e., no additional backup information has been collected. Thus, during a backup operation, the first thing to do is check the Flash at the last written-to location by reading the data therefrom and comparing it to the current data in the volatile memory. If the data has changed, then the destination address is changed with a different logical address associated with the different sector and then a Write operation performed to transfer the data from the volatile memory to Flash at that new logical address. Thus, the overall operation is to – 1) Receive data, 2) Store the received data in volatile memory, 3) Read stored data from the Flash at a first destination address which was the last address associated with a Write operation to the Flash, 4) Compare that read data with the data stored in the volatile memory, 5) If False, change the destination address and Write the data from the volatile memory to the Flash at this new destination address. Thus, the operation is a Receive – Store in RAM – Read FLASH – Compare – Write to FLASH.

The primary purpose of *Kawaguchi* is to improve the backup operation in a system for collecting sensor data in a system, such as an automobile. The existing operation involved backing

of the data in non-volatile memory such as a EEPROM. All this required prior to using Flash was buffering information and then just performing a Write operation to the EEPROM. This only required transferring of data to a logical address within the memory space of the system, wherein new data would write over old data, noting that it was not necessary to change the logical address. *Kawaguchi* sought to improve the operation of the prior system by incorporating Flash as the non-volatile memory. This provided some advantages, as noted above, in that it could arguably have faster Writes, be less expensive, etc. The main problem with Flash is that one cannot Write the same logical address every time because that would require writing over previous data. As the previous data is no longer viable, there is no reason to retain such data and writing over of such data would be a normal thing when storing data in the form of backup data, allowing one to keep the same logical address. As noted, a Write access operation with respect to an EEPROM only needs a Write command to a particular logical address in order to write over old and no longer useful backup data with the new backup data. A Flash, on the other hand, if only a single logical address were utilized, would require an erase of the data followed by a Write to the erased location. This was noted as a problem, which made it less desirable than an EEPROM. The solution in *Kawaguchi* was to just provide a large number of writeable (erased) sectors in the Flash and control a changeable destination address to store data in only different erased sectors for each Write operation. Of course, periodically, the Flash memory would have to be erased to create more free and erased sectors. However, there was one more improvement that *Kawaguchi* provided for and that was for first examining the previously written data before transfer of any data and comparing it to the current data in the volatile memory to determine if a Write to the Flash was necessary. This is best stated in ¶[0072] as follows:

> In other words, in this embodiment, the flash memory 1h is not rewritten by a simple rewriting process including data erasing and data writing.
>
> In contrast, an erasing process requiring a long processing time is performed only when the backup data is not updated(rewritten), so that an erased area of a predetermined size is always left.
>
> Therefore, only a non-time-consuming writing process is performed when the backup data is actually updated.
>
> **Therefore, the time required to rewrite the backup data stored in the flash memory 1h can be reduced.** (Emphasis Added)

This process utilizing the comparator in the backup process does not relate to any Write access operation; rather, all it does is determine whether to initiate a Write access operation. The above-noted claim limitation specifically requires the compare operation to occur after a Write access operation. *Kawaguchi* utilizes this compare operation to determine whether to transfer or Write data to Flash. It is not part of the Write operation of the device with the Flash. Further, the comparison of the previously captured backup data is made with different data than what was stored in the previous Write operation to the Flash. By definition, if the comparison results in a false comparison, that means the data in the volatile memory is different than the data which was previously stored in the volatile memory and which was transferred to the Flash in the previous Write operation. As such, Applicant believes that *Kawaguchi* does not disclose or suggest any type of compare operation of "retained data" after a Write access operation. *Kawaguchi* does nothing more than disclose the operation of comparing data in one memory before writing to a second memory to reduce the number of data transfer operations if the first memory has not had the contents thereof changed between the two sequential Write operations.

Applicant believes that none of the references to *Gorobets, Goodson, Karamcheti* and/or *Yu, Kawaguchi* or *Dusija*, taken singly or in combination, obviate or anticipate the invention as defined by the amended claims. No combination of these claims describes or suggests the operation of performing a Write operation of non-volatile memory by utilizing a volatile memory for storage of received data as retained data, storing received data in nonvolatile memory at a first location in accordance with a first logical address and then reading this stored information back to the controller in the controller memory and comparing it with the retained data in the volatile memory at the controller level. If false, the physical address is remapped to the same logical address and a rewrite performed. None of the references discloses or suggests the use of the two memories at the controller level for the overall operation and doing a comparison at the controller level with the data stored in these two memories. Applicant therefore respect request withdrawal of the 35 USC §103 rejections with respect to Claims 1 – 4 and 7 – 9.

Applicant has now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicant respectfully requests full allowance of the claims as amended.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ghowison@munckwilson.com.

Recognizing that Internet communications are not secure, Applicant hereby authorizes the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application by video conferencing, instant messaging, or electronic mail. Applicant understands that a copy of these communications will be made of record in the application file.

Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 50-0208/VRVN60-35360.

Respectfully submitted,
MUNCK WILSON MANDALA, LLP
Attorneys for Applicant

/Gregory M. Howison, Reg. #30646/

Gregory M. Howison
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GMH/jsr
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Dallas, Texas 75380
Tel: 972-628-3600
Fax: 972-628-3616
September 22, 2023

Electronic Patent Application Fee Transmittal

Application Number:	17203385
Filing Date:	16-Mar-2021
Title of Invention:	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Filer:	Gregory Michael Howison/Joselyn Rodriguez
Attorney Docket Number:	VRVN60-35360

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	1253	1	1480	1480
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**1740**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

25883 7590 10/11/2023

MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

EXAMINER
HIDALGO, FERNANDO N

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/11/2023

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/203,385	03/16/2021	G.R. Mohan Rao	VRVN60-35360	6508

TITLE OF INVENTION: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	01/11/2024

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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PGR2025-00010

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25883 7590 10/11/2023
MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/203,385	03/16/2021	G.R. Mohan Rao	VRVN60-35360	6508

TITLE OF INVENTION: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	01/11/2024

EXAMINER	ART UNIT	CLASS-SUBCLASS
HIDALGO, FERNANDO N	2827	365-185030

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via Patent Center or EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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Vervain v. Phison
PGR2025-00010

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/203,385	03/16/2021	G.R. Mohan Rao	VRVN60-35360	6508

25883 7590 10/11/2023

MUNCK WILSON MANDALA L.L.P
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DALLAS, TX 75380

EXAMINER	
HIDALGO, FERNANDO N	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 10/11/2023

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/203,385	Applicant(s) Rao, G.R. Mohan	
	Examiner FERNANDO N HIDALGO	Art Unit 2827	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 9/22/23.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-4 and 7-9 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☑ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/Fernando Hidalgo/
Primary Examiner, Art Unit 2827

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

2. **Claim(s) 5-6** have been cancelled.

Terminal Disclaimer

3. The terminal disclaimer filed on 3/9/2023 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of **US Patent No. 10950300** has been reviewed and is accepted. The terminal disclaimer has been recorded.

Allowable Subject Matter

4. **Claim(s) 1-4 and 7-9** are allowed.

5. The following is an examiner's statement of reasons for allowance: the pertinent prior art of record, and in light of such record as a whole under **MPEP 1302.14** guidance, and further guidance under **MPEP 2103: "the claim as a whole must be considered,"** does not teach or suggest the combination of claim limitations making the whole of the claims of the claimed invention, particularly as set forth in representative claim(s) 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to FERNANDO N HIDALGO whose telephone number is (571)270-3306. The examiner can normally be reached M-F 9:00-7:30 ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 5712721852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FERNANDO N. HIDALGO
Primary Examiner
Art Unit 2827

/Fernando Hidalgo/
Primary Examiner, Art Unit 2827

Notice of References Cited	Application/Control No. 17/203,385	Applicant(s)/Patent Under Reexamination Rao, G.R. Mohan	
	Examiner FERNANDO N HIDALGO	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-10950300-B2	03-2021	Rao; G. R. Mohan	G11C29/52	1/1
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/203,385	Rao, G.R. Mohan
	Examiner	**Art Unit**
	FERNANDO N HIDALGO	2827

CPC						
Symbol					**Type**	**Version**
G11C	/	11	/	5635	F	2013-01-01
G06F	/	12	/	0246	I	2013-01-01
G11C	/	16	/	3495	I	2013-01-01
G06F	/	11	/	1068	I	2013-01-01
G06F	/	11	/	1072	I	2013-01-01
G11C	/	11	/	5621	I	2013-01-01
G11C	/	11	/	5678	I	2013-01-01
G11C	/	29	/	52	I	2013-01-01
G11C	/	29	/	76	I	2013-01-01
G11C	/	16	/	16	I	2013-01-01
G06F	/	2212	/	7202	A	2013-01-01
G11C	/	2211	/	5641	A	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	7	
/Fernando Hidalgo/ Primary Examiner, Art Unit 2827	26 September 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3A and 3B

U.S. Patent and Trademark Office — Part of Paper No.: 20230926

Vervain Ex. 2024 p. 176 of 193
Vervain v. Phison
PGR2025-00010

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/203,385	Rao, G.R. Mohan
	Examiner	**Art Unit**
	FERNANDO N HIDALGO	2827

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G11C	/	11	/	56

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
365	185.03

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 7	
/Fernando Hidalgo/ Primary Examiner, Art Unit 2827 (Primary Examiner) 26 September 2023 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3A and 3B

U.S. Patent and Trademark Office Part of Paper No.: 20230926

Vervain Ex. 2024 p. 177 of 193
Vervain v. Phison
PGR2025-00010

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/203,385	Rao, G.R. Mohan
	Examiner	**Art Unit**
	FERNANDO N HIDALGO	2827

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
2	2														
3	3														
4	4														
	5														
	6														
5	7														
6	8														
7	9														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	7	
/Fernando Hidalgo/ Primary Examiner, Art Unit 2827	26 September 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3A and 3B

U.S. Patent and Trademark Office Part of Paper No.: 20230926

Vervain Ex. 2024 p. 178 of 193
Vervain v. Phison
PGR2025-00010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	G. R. Mohan RAO
Serial No.:	17/203,385
Confirmation No.	6508
Filed:	March 16, 2021
Notice of Allowance Mailed:	October 11, 2023
Group:	2827
Examiner:	Fernando N. HIDALGO
For:	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

AMENDMENT UNDER RULE 312

The above-identified application has been carefully reviewed prior to the payment of the Issue Fee. It is requested that the following amendments be entered under the provisions of Rule 312.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks begin on page 5 of this paper.

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements;

a bank of nonvolatile memory, including:

a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and

at least one SLC memory module including at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

a[[n]] [[FTL]] flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements;

the controller having associated controller memory for storing received data therein, the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data;

the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed on the stored data by the controller results in a remapping of [[the]] address space to a different physical range of addresses and transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test.

2. (Currently Amended) The system of Claim 1, wherein the FTL~~, flash translation layer,~~ is a software module, or a firmware module containing software updates.

3. (Previously Presented) The system of Claim 1, wherein at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller.

4. (Previously Presented) The system of Claim 1, wherein the MLC and SLC nonvolatile memory elements comprise flash memory.

5. (Cancelled)

6. (Cancelled)

7. (Previously Presented) The system of Claim 1, wherein the random access volatile memory element is dynamic random access memory.

8. (Previously Presented) The system of Claim 1, wherein the random access volatile memory element is static random access memory.

9. (Original) The system of Claim 1, wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD).

REMARKS

Subsequent to the receipt of a Notice of Allowance, this application was carefully reviewed prior to payment of the Issue Fee. The errors noted during this review have been corrected by this Amendment Under Rule 312. It is respectfully submitted that the foregoing amendments do not affect the merits of the application and are proper subject matter for an Amendment Under Rule 312.

Entry of this Amendment is respectfully requested.

Respectfully submitted,
MUNCK WILSON MANDALA, LLP
Attorneys for Applicant(s)

/William G. Howison, Reg. #66850/

William G. Howison
Registration No. 66850

WGH/klh
P.O. Drawer 800889
Dallas, Texas 75380
Tel: 972-628-3600
Fax: 972-628-3616
October 13, 2023

Electronic Patent Application Fee Transmittal

Application Number:	17203385
Filing Date:	16-Mar-2021
Title of Invention:	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Filer:	William G. Howison/Joselyn Rodriguez
Attorney Docket Number:	VRVN60-35360

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1200**

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25883 7590 10/11/2023
MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/203,385	03/16/2021	G.R. Mohan Rao	VRVN60-35360	6508

TITLE OF INVENTION: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	01/11/2024

EXAMINER	ART UNIT	CLASS-SUBCLASS
HIDALGO, FERNANDO N	2827	365-185030

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: VERVAIN, LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Dallas, Texas

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via Patent Center or EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 50-0208

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /William G. Howison, Reg. #66850/ Date October 13, 2023

Typed or printed name William G. Howison Registration No. 66,850

Vervain Ex. 2024 p. 186 of 193
Vervain v. Phison
PGR2025-00010

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/203,385	03/16/2021	G.R. Mohan Rao	VRVN60-35360	6508

25883 7590 10/30/2023
MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

EXAMINER	
HIDALGO, FERNANDO N	

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
10/30/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPdocketing@munckwilson.com
admin@dalpat.com
eofficeaction@appcoll.com

Vervain Ex. 2024 p. 187 of 193
Vervain v. Phison
PGR2025-00010

Response to Rule 312 Communication	Application No.	Applicant(s)	
	17/203,385	Rao, G.R. Mohan	
	Examiner	Art Unit	AIA (FITF) Status
	FERNANDO N HIDALGO	2827	No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 13 October 2023 under 37 CFR 1.312 has been considered, and has been:

a) ☑ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.

Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

f) ☐ not entered because the supplemental or corrected Application Data sheet (ADS)

☐ was not accompanied by a petition to accept an unintentionally delayed claim under 37 CFR 1.55 or 27 CFR 1.78;

☐ did not identify the information being changed in accordance with 37 CFR 1.76(c)(2);

☐ was not properly signed in accordance with 37 CFR 1.76(e) (or 37 CFR 1.33(b) for applications filed prior to September 16, 2012).

/Fernando Hidalgo/
Primary Examiner, Art Unit 2827

Do Enter, /fh/, 10/24/23

VRVN60-35360 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	G. R. Mohan RAO
Serial No.:	17/203,385
Confirmation No.	6508
Filed:	March 16, 2021
Notice of Allowance Mailed:	October 11, 2023
Group:	2827
Examiner:	Fernando N. HIDALGO
For:	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

AMENDMENT UNDER RULE 312

The above-identified application has been carefully reviewed prior to the payment of the Issue Fee. It is requested that the following amendments be entered under the provisions of Rule 312.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks begin on page 5 of this paper.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/203,385	11/28/2023	11830546	VRVN60-35360	6508

25883 7590 11/08/2023

MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at https://patentcenter.uspto.gov/. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

The USPTO is implementing electronic patent issuance with a transition period, during which period the USPTO will mail a ceremonial paper copy of the electronic patent grant to the correspondence address of record. Additional copies of the patent (i.e., certified and presentation copies) may be ordered for a fee from the USPTO's Certified Copy Center at https://certifiedcopycenter.uspto.gov/index.html. The Certified Copy Center may be reached at (800)972-6382.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Center (https://patentcenter.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PATENT CENTER site https://patentcenter.uspto.gov for additional inventors):

G.R. Mohan Rao, Allen, TX;

APPLICANT(s) (Please see PATENT CENTER site https://patentcenter.uspto.gov for additional applicants):

VERVAIN, LLC, Dallas, TX;

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/203,385	03/16/2021	G.R. Mohan Rao	VRVN60-35360	6508

25883 7590 11/28/2023
MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

EXAMINER	
HIDALGO, FERNANDO N	

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
11/28/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPdocketing@munckwilson.com
admin@dalpat.com
eofficeaction@appcoll.com

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.
17/203,385	28-Nov-2023	11830546

MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

EGRANT NOTIFICATION

Your electronic patent grant (eGrant) is now available, which can be accessed via Patent Center at https://patentcenter.uspto.gov

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