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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR UNITED STATES PATENT**

LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM****CROSS-REFERENCE TO RELATED APPLICATIONS**

[0001] This application is a Continuation of U.S. Patent Application No. 14/525,411, filed October 28, 2014, published on October 1, 2015, as U.S. Publication No. 2015-0278013, now U.S. Patent No. 9,196,385, issued on November 24, 2015, entitled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM” (Atty. Dkt. No. GR TD-32620). Application No. 14/525,411 is a Division of U.S. Patent Application No. 13/455,267, filed April 25, 2012, published on January 24, 2013, as U.S. Publication No. 2013-0021846, now U.S. Patent No. 8,891,298, issued on November 18, 2014, entitled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM” (Atty. Dkt. No. GR TD-32619). Application No. 13/455,267 claims benefit of U.S. Provisional Application No. 61/509,257, filed July 19, 2011, entitled “LIFETIME MIXED LEVEL NAND FLASH SYSTEM” (Atty. Dkt. No. GR TD-32624). Patent Nos. 9,196,385 and 8,891,298 and Patent Application Publication Nos. 2015-0278013 and 2013-0021846 are hereby incorporated by reference in their entirety. This application also incorporates by reference the complete disclosure of U.S. Patent Application No. 12/256,362, filed October 22, 2008, published on April 30, 2009, as U.S. Publication No. 2009-0109787, now U.S. Patent No. 7,855,916, issued on December 21, 2010, entitled “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES” (Atty. Dkt. No. GR TD-32614). This application also incorporates by reference the complete disclosure of U.S. Patent Application No. 12/915,177, filed October 29, 2010, published on March 10, 2011, as U.S. Publication No. 2011-0060870, now U.S. Patent No. 8,194,452, issued on June 5, 2012, entitled “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES” (Atty. Dkt. No. 32615).

TECHNICAL FIELD

[0002] This application relates to a system and method for providing reliable storage through the use of non-volatile memories and, more particularly, to a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use of a combination of single-level cell (SLC) and multi-level cell (MLC) NAND flash storage without substantially raising the cost of the NAND flash storage system. The memory in a total non-volatile memory system may contain some SRAM (static random-access memory), DRAM (dynamic RAM), RRAM (resistive RAM), PCM (phase change memory), MAGRAM (magnetic random-access memory), NAND flash, and one or more HDDs (hard disk drives) when storage of the order of several terabytes is required. The SLC non-volatile memory can be flash, PCM, RRAM, MAGRAM or any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash, and it provides for data access speeds that are faster than that of MLC flash or rotating storage media (e.g., HDDs).

BACKGROUND

[0003] Non-volatile memories provide long-term storage of data. More particularly, non-volatile memories can retain the stored data even when not powered. Magnetic (rotating) hard disk drives (HDD) dominate this storage medium due to lower cost compared to solid state disks (SSD). Optical (rotating) disks, tape drives and others have a smaller role in long-term storage systems. SSDs are preferred for their superior performance (fast access time), mechanical reliability and ruggedness, and portability. Flash memory, more specifically NAND flash, is the dominant SSD medium today.

[0004] RRAM, PCM, MAGRAM and others, will likely play a larger role in the future, each of them having their own advantages and disadvantages. They may ultimately replace flash memories, initially for use as a "write buffer" and later to replace "SLC flash" and "MLC flash." MLC NAND flash is a flash memory technology using multiple levels per cell to allow more bits to be stored using the same number of transistors. In SLC NAND flash technology, each cell can exist in one of two states, storing one bit of information per cell. Most MLC NAND flash memory has four possible states per cell, so it can store two bits of information per cell.

[0005] These semiconductor technology driven "flash alternatives," i.e., RRAM, PCM, MAGRAM and others, have several advantages over any (SLC or MLC) flash because they: 1) allow data to be written over existing data (without prior erase of existing data), 2) allow for an erase of individual bytes or pages (instead of having to erase an entire block), and 3) possess superior endurance (1,000,000 write-erase cycles compared to typical 100,000 cycles for SLC flash and less than 10,000 cycles for MLC flash).

[0006] HDDs have several platters. Each platter contains 250-5,000 tracks (concentric circles). Each track contains 64 to 256 sectors. Each sector contains 512 bytes of data and has a unique "physical (memory) address." A plurality of sectors is typically combined to form a "logical block" having a unique "logical address." This logical address is the address at which the logical block of physical sectors appears to reside from the perspective of an executing application program. The size of each logical block and its logical address (and/or address ranges/boundaries) is optimized for the particular operating system (OS) and software

applications executed by the host processor. A computer OS organizes data as "files." Each file may be located (stored) in either a single logical block or a plurality of logical blocks, and therefore, the location of files typically traverses the boundaries of individual (physical) sectors. Sometimes, a plurality of files has to be combined and/ or modified, which poses an enormous challenge for the memory controller device of a non-volatile memory system.

[0007] SSDs are slowly encroaching on the HDD space and the vast majority of NAND flash in enterprise servers utilizes a SLC architecture, which further comprises a NAND flash controller and a flash translation layer (FTL). NAND flash devices are generally fragmented into a number of identically sized blocks, each of which is further segmented into some number of pages. It should be noted that asymmetrical block sizes, as well as page sizes, are also acceptable within a device or a module containing devices. For example, a block may comprise 32 to 64 pages, each of which incorporates 2 - 4 Kbit of memory. In addition, the process of writing data to a NAND flash memory device is complicated by the fact that, during normal operation of, for example, single-level storage (SLC) , erased bits (usually all bits in a block with the value of '1') can only be changed to the opposite state (usually '0') once before the entire block must be erased. Blocks can only be erased in their entirety, and, when erased, are usually written to '1' bits. However, if an erased block is already there, and if the addresses (block, page, etc.) are allowed, data can be written immediately; if not, a block has to be erased before it can be written to.

[0008] FTL is the driver that works in conjunction with an existing operating system (or, in some embedded applications, as the operating system) to make linear flash memory appear to the system like a disk drive, i.e., it emulates a HDD. This is achieved by creating "virtual" small blocks of data, or sectors, out of flash's large erase blocks and managing data on the flash so that it appears to be "write in place" when in fact it is being stored in different locations in the flash. FTL further manages the flash so that there are clean/ erased places to store data.

[0009] Given the limited number of writes that individual blocks within flash devices can tolerate, wear leveling algorithms are used within the flash devices (as firmware commonly known as FTL or managed by a controller) to attempt to ensure that "hot" blocks, i.e., blocks that are frequently written, are not rendered unusable much faster than other blocks. This task is

usually performed within a flash translation layer. In most cases, the controller maintains a lookup table to translate the memory array physical block address (PBA) to the logical block address (LBA) used by the host system. The controller's wear-leveling algorithm determines which physical block to use each time data is programmed, eliminating the relevance of the physical location of data and enabling data to be stored anywhere within the memory array and thus prolonging the service life of the flash memory. Depending on the wear-leveling method used, the controller typically either writes to the available erased block with the lowest erase count (dynamic wear leveling); or it selects an available target block with the lowest overall erase count, erases the block if necessary, writes new data to the block, and ensures that blocks of static data are moved when their block erase count is below a certain threshold (static wear leveling).

[0010] MLC NAND flash SSDs are slowly replacing and/ or coexisting with SLC NAND flash in newer SSD systems. MLC allows a single cell to store multiple bits, and accordingly, to assume more than two values; i.e., '0' or '1'. Most MLC NAND flash architectures allow up to four (4) values per cell; i.e., '00', '01', '10', or '11'. Generally, MLC NAND flash enjoys greater density than SLC NAND flash, at the cost of a decrease in access speed and lifetime (endurance). It should be noted, however, that even SLC NAND flash has a considerably lower lifetime (endurance) than rotating magnetic media (e.g., HDDs), being able to withstand only between 50,000 and 100,000 writes, and MLC NAND flash has a much lower lifetime (endurance) than SLC NAND flash, being able to withstand only between 3,000 and 10,000 writes. As is well known in the art, any "write" or "program" to a block in NAND flash (floating gate) requires an "erase" (of a block) before "write."

[0011] Despite its limitations, there are a number of applications that lend themselves to the use of MLC flash. Generally, MLC flash is used in applications where data is read many times (but written few times) and physical size is an issue. For example, flash memory cards for use in digital cameras would be a good application of MLC flash, as MLC can provide higher density memory at lower cost than SLC memory.

[0012] When a non-volatile storage system combines HDD, SLC and MLC (setting aside volatile memory for buffering, caching etc) in a single (hybrid) system, new improvements and

solutions are required to manage the methods of writing data optimally for improved life time (endurance) of flash memory. Accordingly, various embodiments of a NAND flash storage system that provides long lifetime (endurance) storage at low cost are described herein.

[0013] The following description is presented to enable one of ordinary skill in the art to make and use the disclosure and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present disclosure is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

SUMMARY

[0014] According to one embodiment of the present disclosure, there is provided a system for storing data which comprises at least one MLC nonvolatile memory module (hereinafter referred to as "MLC module") and at least one SLC non-volatile memory module (hereinafter referred to as "SLC module"), each module comprises a plurality of individually erasable blocks. The data storage system according to one embodiment of the present disclosure further comprises a controller for controlling both the at least one MLC module and the at least one SLC module. In particular, the controller maintains an address map comprising a list of individual logical address ranges each of which maps to a similar range of physical addresses within either the at least one MLC module or the at least one SLC module. After each write to (flash) memory, the controller conducts a data integrity check to ensure that the data was written correctly. When the data was not written correctly, the controller modifies the table so that the range of addresses on which the write failed is remapped to the next available range of physical addresses within the at least one SLC module. The SLC module can be (NAND) flash, PCM, RRAM, MAGRAM or any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash, and it provides for data access speeds that are faster than that of MLC flash or rotating storage media (e.g., HDDs).

[0015] According to another embodiment of the present disclosure, there is provided a system for storing data which comprises a controller that is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The present disclosure will be more fully understood by reference to the following detailed description of one or more preferred embodiments when read in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout the views and in which:

[0017] FIG. 1 is a block diagram of a computer system incorporating one embodiment of the present disclosure;

[0018] FIG. 2 is a drawing depicting a translation table/address map in accordance with one embodiment of the present disclosure;

[0019] FIGS. 3a and 3b are a flow chart illustrating an exemplary method for use in implementing one embodiment of the present disclosure; and

[0020] FIG. 4 is a block diagram depicting one embodiment of the present disclosure for implementation within a NAND flash module.

DETAILED DESCRIPTION

[0021] The present disclosure is directed to the reliable storage of data in read and write memory, and, in particular, to the reliable storage of data in non-volatile memory, such as, for example, NAND flash. Generally, and in particular regard to NAND flash memory, two separate banks of NAND flash are maintained by a controller. One bank contains economical MLC NAND flash, while a second bank contains high endurance SLC NAND flash. The controller conducts a data integrity test after every write. If a particular address range fails a data integrity test, the address range is remapped from MLC NAND flash to SLC NAND flash. As the SLC NAND flash is used to boost the lifetime (endurance) of the storage system, it can be considerably lesser in amount than the MLC NAND flash. For example, a system may set SLC NAND flash equal to 12.5% or 25% of MLC NAND flash (total non-volatile memory storage space=MLC+SLC).

[0022] Turning to the Figures and to Figure 1 in particular, a computer system 10 depicting one embodiment of the present disclosure is shown. A processor 12 is coupled to a device controller 14, such as a chipset, using a data link well known in the art, such as a parallel bus or packet-based link. The device controller 14 provides interface functions to the processor 12. In some computer systems, the device controller 14 may be an integral part of the (host) processor 12. The device controller 14 provides a number of input/output ports 16 and 18, such as, for example, serial ports (e.g., USB ports and Firewire ports) and network ports (e.g., Ethernet ports and 802.11 “Wi-Fi” ports). The device controller 14 may also control a bank of, for example, DRAM 20. In addition, the device controller 14 controls access to one or more disks 24, such as, for example, a rotating magnetic disk, or an optical disk, as well as two or more types of NAND flash memory. One type of NAND flash memory is a MLC NAND flash memory module 26. Another type of NAND flash memory is a SLC NAND flash memory module 28.

[0023] The device controller 14 maintains a translation table/address map which may include address translations for all devices in the computer system. Nonetheless, the discussion in the present disclosure will be limited only to NAND flash memory modules. In particular, the device controller 14 maintains a translation table that maps logical computer system addresses to physical addresses in each one of the MLC- and SLC-NAND flash memory modules 26 and 28,

respectively. As MLC flash memory is less expensive than SLC flash memory, on a cost per bit basis, the translation table will initially map all logical NAND flash addresses to the MLC NAND flash memory module 26. The address ranges within the translation table will assume some minimum quantum, such as, for example, one block, although a smaller size, such as one page could be used, if the NAND flash has the capability of erasing the smaller size quantum.

[0024] A “read-modify-write” scheme is used to write data to the NAND flash. Data to be written to NAND flash is maintained in DRAM 20. After each write to an address within a particular address range, the device controller 14 will—as time permits—perform a read on the address range to ensure the integrity of the written data. If a data integrity test fails, the address range is remapped from the MLC NAND flash memory module 26 to the next available address range in the SLC NAND flash memory module 28.

[0025] Figure illustrates one embodiment of a translation table/address map of the present disclosure. In Figure. 2a, a list of logical address ranges (R0-RN) is translated to physical address ranges. As illustrated, all of the logical address ranges are translated to blocks on the MLC NAND flash memory module 26. However, through the application of a data integrity verification check (explained in more detail below) it is determined that, for example, address range R2 corresponds to failed quanta of data stored in block 2 of the MLC NAND flash memory module 26. Figure 2b shows the quanta of data which failed the data integrity verification check (see Figure 2a) remapped to the next available range of physical addresses within the SLC NAND flash memory module 28, in this example, SLC/block 0.

[0026] Figures. 3a and 3b are a flow chart illustrating a method for utilizing a NAND flash memory system incorporating one embodiment of the present disclosure. The method begins in a step 100, when a command to write a quantum of data stored in DRAM to a particular location in NAND flash memory is received. In step 102, the quantum of data is read from DRAM into memory within the device controller (which acts as the memory controller). In step 104, both the logical address range and the NAND flash physical address range to which the quantum of data is to be written, is read into memory of the device controller. In step 106, the quantum of data to be written is combined with the contents of the NAND flash memory. In step 108, the NAND flash physical address range to be written is erased. In step 110, the combined data is written to

the appropriate NAND flash physical address range. In step 112 the NAND flash physical address range that was written in step 110 is read into device controller memory.

[0027] The flowchart continues in Figure 3b. In step 114 the NAND flash physical address range that was read into device controller memory is compared with the retained data representing the combination of the previous contents of the physical address range and the quantum of data to be written. In step 116, if the retained data matches the newly stored data in the NAND flash memory, the write was a success, and the method exits in step 118. However, if the retained data does not match the newly stored data in the NAND flash memory, the method executes step 120, which identifies the next quantum of available SLC NAND flash memory addresses. In step 122, a check is made to determine if additional SLC NAND flash memory is available, and, if not, the NAND flash memory system is marked as failed, prompting a system alert step 124. However, if additional SLC NAND flash memory is available, the failed NAND flash physical address range is remapped to the next available quantum of SLC NAND flash memory in step 126. Execution then returns to step 110, where the write is repeated.

[0028] Another application of one embodiment of the present disclosure, not depicted in any of the drawings, is to allocate “hot” blocks; i.e., those blocks that receive frequent writes, into the SLC NAND flash memory module 28, while allocating “cold” blocks; i.e., those blocks that only receive infrequent writes, into the MLC NAND flash memory module 26. This could be accomplished within the device controller 14 described above, which could simply maintain a count of those blocks that are accessed (written to) most frequently, and, on a periodic basis, such as, for example, every 1000 writes, or every 10,000 writes, transfer the contents of those blocks into the SLC NAND flash memory module 28.

[0029] FIG. 4 depicts another embodiment of the present disclosure. The embodiment is entirely resident within a NAND flash module 50. In particular, a standard NAND flash interface 52 is managed by flash translation layer (FTL) logic 54. The flash translation layer (FTL) 54 manages two NAND flash memory banks 56 and 58, whereby memory bank 56 comprises a plurality of MLC NAND flash memory modules 60a and a plurality of SLC NAND flash memory modules 62a. Memory bank 58 comprises a plurality of MLC NAND flash memory modules 60b and a plurality of SLC NAND flash memory modules 62b.

[0030] This embodiment of the present disclosure could function similarly to the system level embodiment discussed earlier with reference to Figures 1-3b, but the control functions, such as maintenance of the translation table/address map (Figure 2), could be conducted within the flash translation layer (FTL) 54 instead of in a device controller 14.

[0031] Embodiments of the present disclosure relate to a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use of a combination of multi-level cell (MLC) and single-level cell (SLC) NAND flash storage. The above description is presented to enable one of ordinary skill in the art to make and use the disclosure and is provided in the context of a patent application and its requirements. While this disclosure contains descriptions with reference to certain illustrative aspects, it will be understood that these descriptions shall not be construed in a limiting sense. Rather, various changes and modifications can be made to the illustrative embodiments without departing from the true spirit, central characteristics and scope of the disclosure, including those combinations of features that are individually disclosed or claimed herein. Furthermore, it will be appreciated that any such changes and modifications will be recognized by those skilled in the art as an equivalent to one or more elements of the following claims, and shall be covered by such claims to the fullest extent permitted by law.

WHAT IS CLAIMED IS:

1. A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

5 at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module; and

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wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module.

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ABSTRACT

A flash controller for managing at least one MLC non-volatile memory module and at least one SLC non-volatile memory module. The flash controller is adapted to determine if a range of addresses listed by an entry and mapped to said at least one MLC non-volatile memory module fails a data integrity test. In the event of such a failure, the controller remaps said entry to an equivalent range of addresses of said at least one SLC non-volatile memory module. The flash controller is further adapted to determine which of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and allocating those blocks that receive frequent writes to the SLC non-volatile memory module and those blocks that receive infrequent writes to the MLC non-volatile memory module.

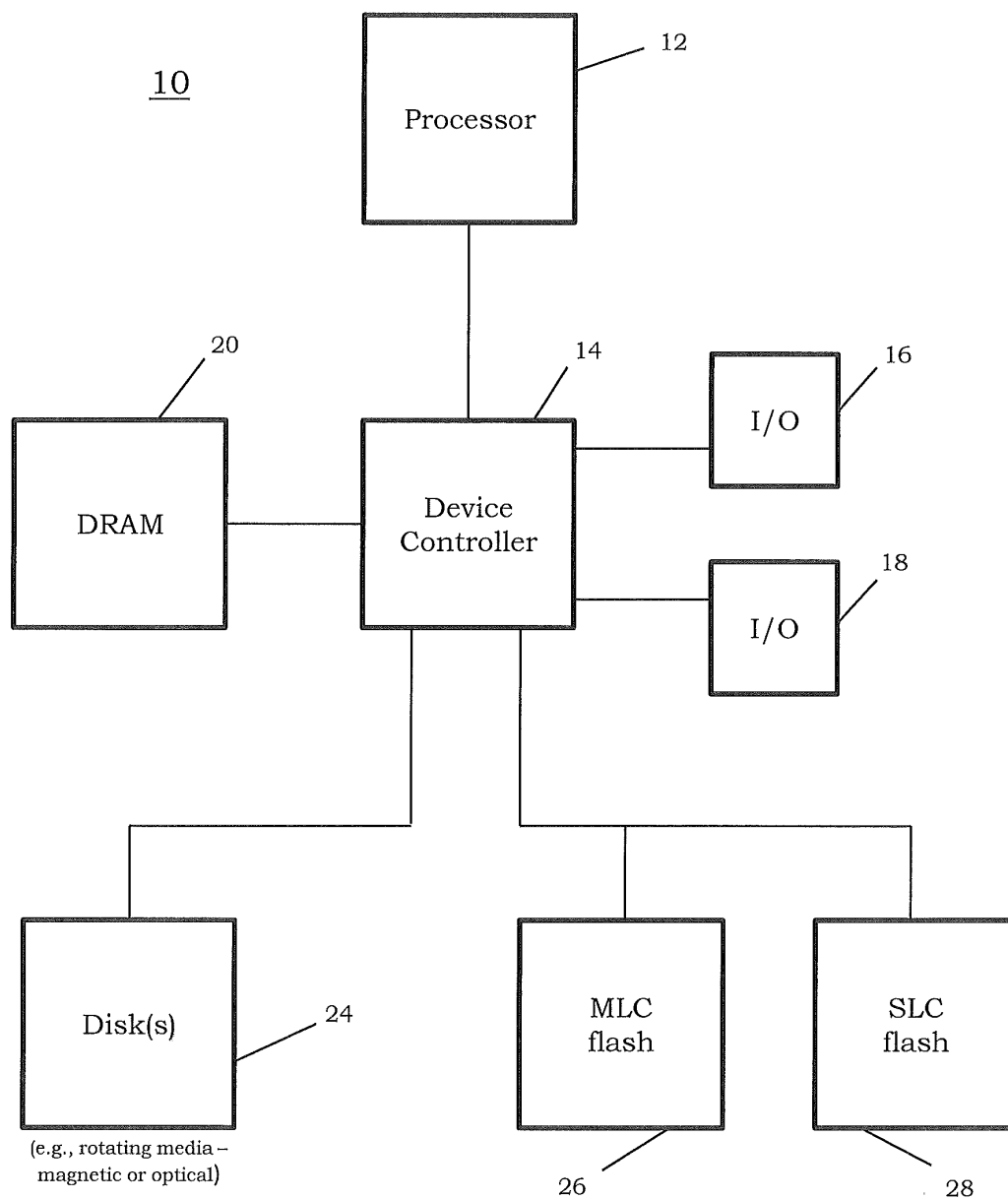


FIG. 1

LOGICAL ADDRESS RANGE	PHYSICAL ADDRESS RANGE
R0	MLC/Block 0
R1	MLC/Block 1
R2	MLC/Block 2
R3	MLC/Block 3
R4	MLC/Block 4
RN	MLC/Block N

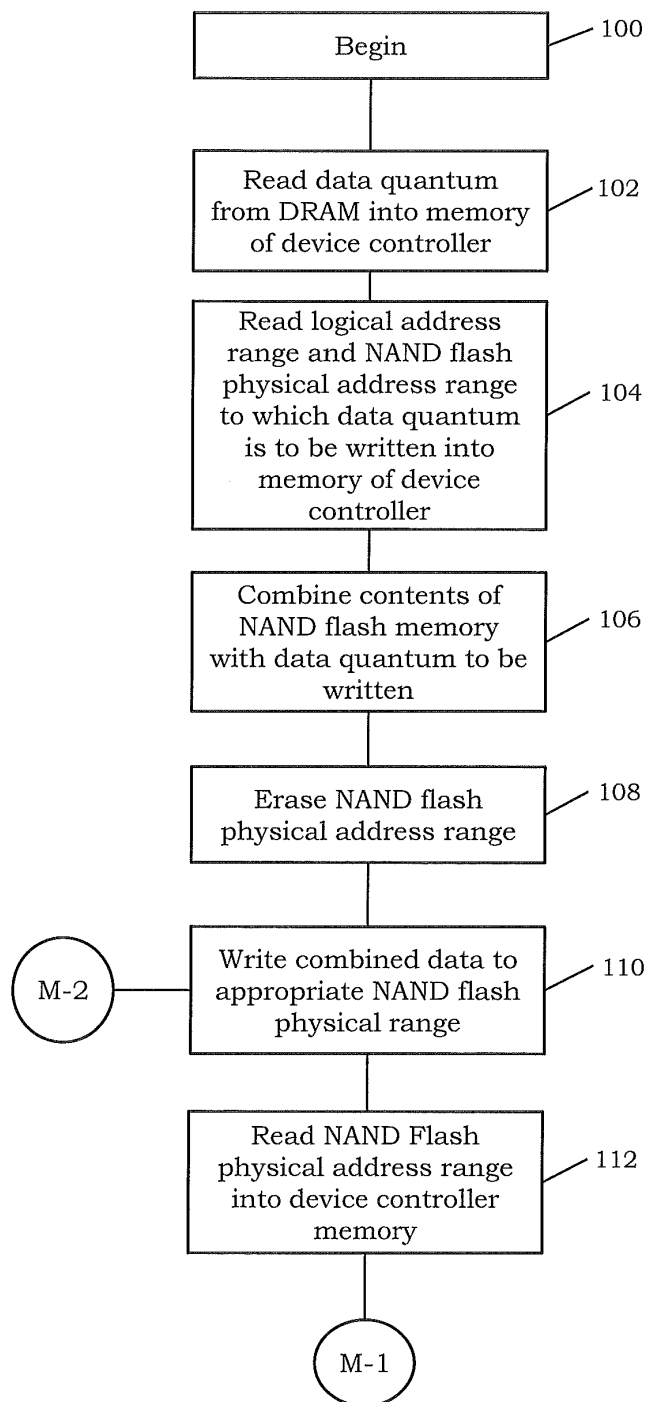
Failed Data Integrity Test →

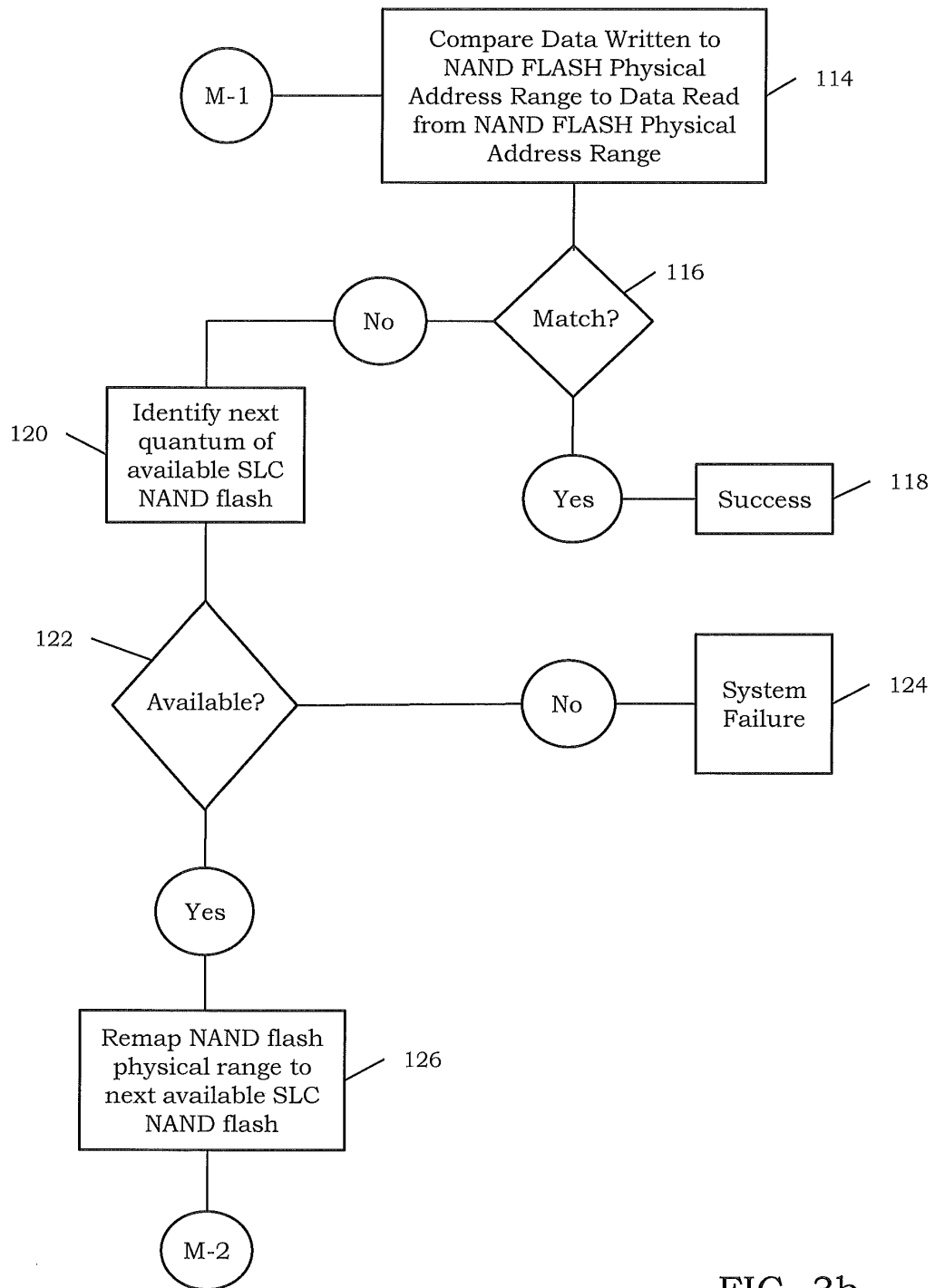
FIG. 2a

LOGICAL ADDRESS RANGE	PHYSICAL ADDRESS RANGE
R0	MLC/Block 0
R1	MLC/Block 1
R2	SLC/Block 0
R3	MLC/Block 3
R4	MLC/Block 4
RN	MLC/Block N

Remapping to SLC flash module →

FIG. 2b

FIG. 3a

FIG. 3b

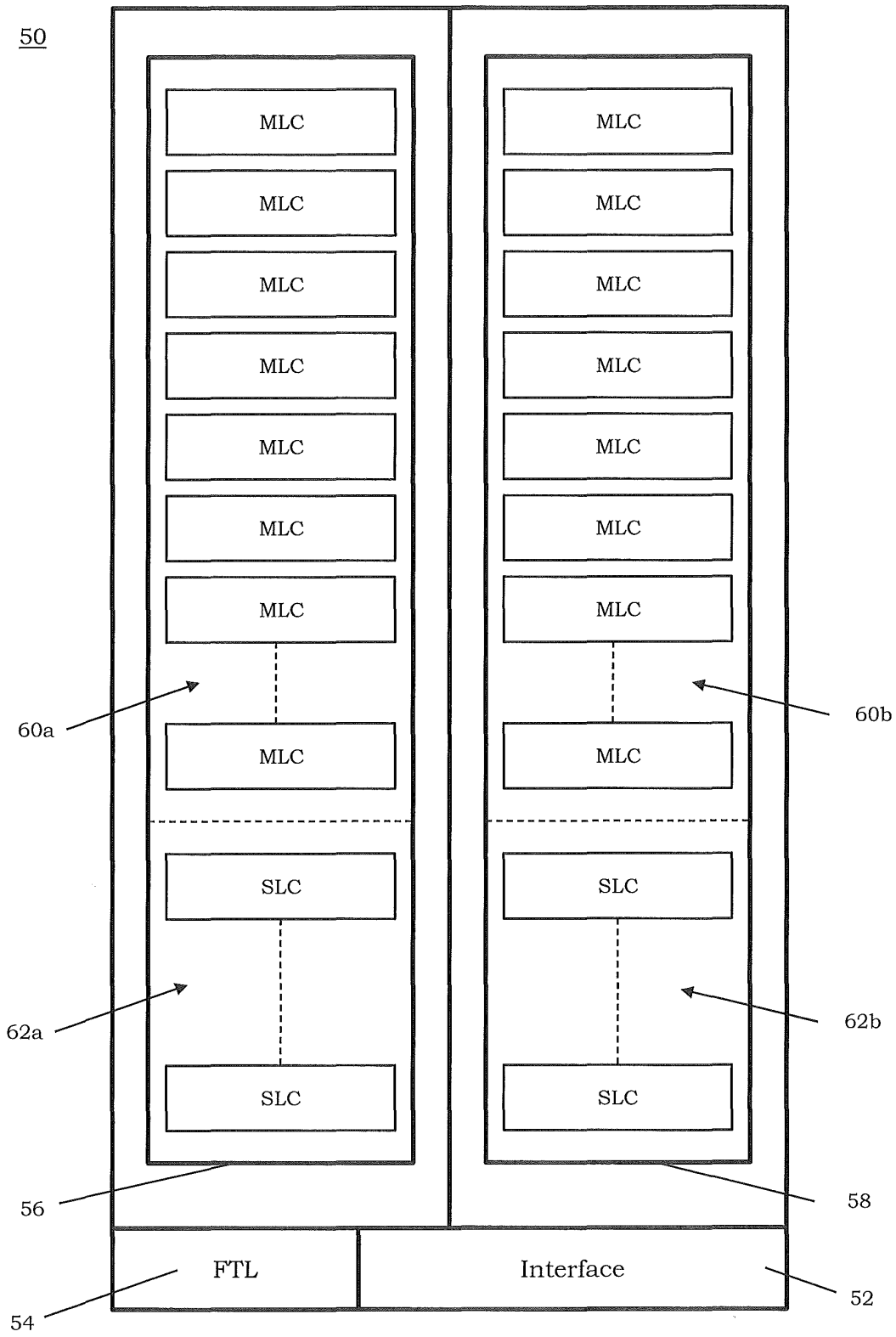


FIG. 4



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14/950,553	11/24/2015	G.R. Mohan Rao	GRTD-32800	1038
25883 7590 03/16/2016 HOWISON & ARNOTT, L.L.P. P.O. BOX 741715 DALLAS, TX 75374-1715			EXAMINER REIDLINGER, RONALD LANCE	
			ART UNIT 2824	PAPER NUMBER
			NOTIFICATION DATE 03/16/2016	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 14/950,553	Applicant(s) RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 February 2016.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 2/15/2016 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.
2. Claim 1 is pending.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).
4. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP §

717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(I)(1) - 706.02(I)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

5. The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/forms/. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. **An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission.** For more information about eTerminal Disclaimers, refer to:

<http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp>.

6. **Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1 of U.S. Patent No. 8,891,298.** Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 of the '298 patent completely anticipates all the limitations of claim 1 of the current application.

7. **Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1 of U.S. Patent No. 9,196,385.** Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 of the '385 patent completely anticipates all the limitations of claim 1 of the current application.

Claim Rejections - 35 USC § 102

8. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

9. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. **Claim 1 is rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Gorobets et al. (US 2010/0172179 A1).**

Regarding claim 1, Gorobets et al. teach,

A system for storing data (e.g. Fig. 20) comprising:

at least one MLC non-volatile memory module (Fig. 20 Main Portion MLC No. 2003) comprising a plurality of individually erasable blocks (this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one SLC non-volatile memory module (Fig. 20 Binary Portion No. 2001) comprising a plurality of individually erasable blocks (again, this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]); and

a controller (Fig. 8 Memory Manager No. 300) coupled to the (Flash Memory No. 200) at least one MLC non-volatile memory module and the at least one SLC non-

volatile memory module (See Fig. 20), the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules (maps logical addresses to physical addresses, see ¶ [0096]), the address map comprising a list of logical address ranges (e.g. a block) accessible by a computer system (logical addresses), the list of logical address ranges having a minimum quanta of addresses (the minimum quantity of addresses is different depending on the operation, for an erase, a block is the minimum erase unit and a page is the minimum programming unit, see ¶ [0017]), wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module (maps logical addresses to physical addresses, see ¶ [0096]); and

wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses (Fig. 20 block 2018) within the at least one MLC non-volatile memory module (Main Portion (MLC) No. 2003), fails a data integrity test (e.g. failure programming only the upper page, but still usable as binary, see ¶ [0165]), and, in the event of such a failure, the controller remaps (No. 2017) the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module (remapped to the spare binary block, see ¶ [0165]).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R LANCE REIDLINGER whose telephone number is

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(571)270-7353. The examiner can normally be reached on 11:30am - 9:00pm Mon-Thur and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571)272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R LANCE REIDLINGER/
Examiner, Art Unit 2824

Notice of References Cited	Application/Control No. 14/950,553		Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER		Art Unit 2824	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2010/0172179 A1	07-2010	Gorobets; Sergey Anatolievich	G06F12/0246	365/185.09
*	B	US-8,891,298 B2	11-2014	Rao; G. R. Mohan	G11C16/3495	365/148
*	C	US-9,196,385 B2	11-2015	Rao; G. R. Mohan	G11C16/3495	1/1
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 14950553	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner LANCE REIDLINGER	Art Unit 2824

CPC- SEARCHED		
Symbol	Date	Examiner
G11C 11/5621, 2211/5641, 2029/1806, 29/50004, 29/76, 29/765	3/7/2016	RLR
G06F 11/1068, 11/1072	3/7/2016	RLR

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Reviewed Parent Applications' Search/Prosecution History	3/7/2016	RLR
Inventor Search Conducted in EASt	3/7/2016	RLR
See Attached EAST Search History	3/7/2016	RLR

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/LANCE REIDLINGER/ Examiner.Art Unit 2824	
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	(14/950553 14/525411 13/455267).app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/07 12:24
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L4	2568	g11c29/76.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/07 12:55
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L7	6295	g06f11/1068,1072.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/07 12:55
L8	4705	g11c11/5621.cpc.	US-PGPUB;	OR	ON	2016/03/07

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S2	2	12/567771.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:07
S3	5314	SLC! and MLC!	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:09
S4	3345	S3 and address and page	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:10
S5	904	S4 and test\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:10
S6	662	S5 and (map mapped mapping re\$1map\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:11
S7	177	S4 and test\$3 with fail\$3	US-PGPUB; USPAT; USOCR;	OR	ON	2014/06/13 13:11

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S10	1160	MLC! same test\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:14
S11	46	S9 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:14
S12	1	13/096736.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:42
S13	2	"20100172179".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:43
S15	2	12/348825.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 14:14
S16	6	((("5671128") or ("6948026") or ("20030110343") or ("20030123301") or ("20050144516") or ("20090187798"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/06/13 14:17
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S19	5	"2011060870".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 14:25
S20	3	"20110060870".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 14:25
S21	7	(US-20090268513-\$ or US-20090327590-\$ or US-20110271043-\$ or US-20100172179-\$).did. or (US-8379460-\$ or US-8417988-\$ or US-8422303-\$).did.	US-PGPUB; USPAT	OR	ON	2014/06/13 14:34
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S25	1	S21 and MRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 15:29
S26	61	MRAM with MLC	US-PGPUB; USPAT;	OR	ON	2014/06/13 15:30

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S27	7	advantages with MRAM with PCRAM with (flash eeprom)	US-PGPUB; USPAT	OR	ON	2014/06/13 16:16
S28	118	((("G R Mohan") near2 (Rao)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/06/13 16:48
S29	5196	SLC and MLC	US-PGPUB; USPAT	OR	ON	2014/06/13 16:49
S30	8	S3 and S28	US-PGPUB; USPAT	OR	ON	2014/06/13 16:49
S31	205	gorobets near2 sergey.in.	US-PGPUB; USPAT	OR	ON	2014/06/13 16:59
S32	245	wear adj leveling.ti.	US-PGPUB; USPAT	OR	ON	2014/06/13 16:59
S33	4	S31 and S32	US-PGPUB; USPAT	OR	ON	2014/06/13 17:00
S34	84	flag same slc same MLC	US-PGPUB; USPAT	OR	ON	2014/06/13 19:54
S35	1	"20060171210".pn.	US-PGPUB; USPAT	OR	ON	2014/06/13 19:56
S36	2	flag same Tlc same MLC	US-PGPUB; USPAT	OR	ON	2014/06/13 19:59
S37	411	flag same ((three triple tri!) adj (level state bit) TLC) same (MLC DLC BLC (double two bi) adj (level state bit))	US-PGPUB; USPAT	OR	ON	2014/06/13 20:03
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S40	90	S37 and S39	US-PGPUB; USPAT	OR	ON	2014/06/13 20:04
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S45	629	flag and S44	US-PGPUB; USPAT	OR	ON	2014/06/14 18:01
S46	27101	read\$3 adj voltage	US-PGPUB; USPAT	OR	ON	2014/06/14 18:02
S47	332	S45 and S46	US-PGPUB; USPAT	OR	ON	2014/06/14 18:02

S48	178033	first near2 read\$3	US-PGPUB; USPAT	OR	ON	2014/06/14 18:02
S49	124427	second near2 read\$3	US-PGPUB; USPAT	OR	ON	2014/06/14 18:02
S50	179	S48 and S49 and S46 and S45	US-PGPUB; USPAT	OR	ON	2014/06/14 18:03
S51	1	masaki near2 fujio.in.	US-PGPUB; USPAT	OR	ON	2014/06/14 18:08
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S53	725	flag same S48 same S49	US-PGPUB; USPAT	OR	ON	2014/06/14 18:22
S54	69	S44 and S53	US-PGPUB; USPAT	OR	ON	2014/06/14 18:22
S55	92	S53 same (word adj line wordline)	US-PGPUB; USPAT	OR	ON	2014/06/14 18:24
S56	39	S44 and S55	US-PGPUB; USPAT	OR	ON	2014/06/14 18:24
S57	5	flag and S52	US-PGPUB; USPAT	OR	ON	2014/06/14 18:30
S84	763	Rao near2 Mohan.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:29
S85	0	Rao near2 "G.R. Mohan".in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:32
S86	0	"G.R. Mohan".in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:32
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S89	65851	rao.in.	US-PGPUB; USPAT; USOCR;	OR	ON	2015/09/08 04:32

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S90	17889	mohan.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:33
S91	295	S87 and S88 and S89 and S90	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:33
S92	2054	SLC! same test\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:35
S93	1297	MLC! same test\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:35
S94	68	S92 and S93	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:35
S95	7281	SLC! and MLC!	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:35
S96	4720	S95 and address and page	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:35
S97	273	S96 and test\$3 with fail\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:35
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		re\$1map\$4)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			04:35
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S102	764	g11c29/765.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:48
S103	1234	g11c29/50004.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:49
S104	5523	g06f11/1068,1072.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:50
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S120	2	("9196385" "8891298").pn.	USPAT	OR	ON	2016/03/07 02:41

EAST Search History (Interference)

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S58	919	single adj (level bit data) adj (cell memory element).clm.	US-PGPUB; USPAT	OR	ON	2014/08/25 07:04
S59	2720	(plural multiple multi) adj (level bit data) adj (cell memory element).clm.	US-PGPUB; USPAT	OR	ON	2014/08/25 07:05
S60	1138	MLC!.clm.	US-PGPUB; USPAT	OR	ON	2014/08/25 07:05
S61	651	SLC!.clm.	US-PGPUB; USPAT	OR	ON	2014/08/25 07:05
S62	3190	S59 S60	US-PGPUB; USPAT	OR	ON	2014/08/25 07:05
S63	3063	S58 S59	US-PGPUB; USPAT	OR	ON	2014/08/25 07:05
S64	2725	S62 and S63	US-PGPUB; USPAT	OR	ON	2014/08/25 07:05
S65	101412	"365".clas.	US-PGPUB; USPAT	OR	ON	2014/08/25 07:06
S66	1486	S64 and S65	US-PGPUB; USPAT	OR	ON	2014/08/25 07:06
S67	3807	365/185.03.ccls.	US-PGPUB; USPAT	OR	ON	2014/08/25 07:06
S68	1818	365/185.09.ccls.	US-PGPUB; USPAT	OR	ON	2014/08/25 07:06
S69	5784	365/201.ccls.	US-PGPUB; USPAT	OR	ON	2014/08/25 07:06

S70	10934	S67 S68 S69	US-PGPUB; USPAT	OR	ON	2014/08/25 07:06
S71	885	S70 and S64	US-PGPUB; USPAT	OR	ON	2014/08/25 07:07
S72	282940	address.clm.	US-PGPUB; USPAT	OR	ON	2014/08/25 07:07
S73	389370	(table map).clm.	US-PGPUB; USPAT	OR	ON	2014/08/25 07:08
S74	17911	S72 near3 S73	US-PGPUB; USPAT	OR	ON	2014/08/25 07:08
S75	284287	test\$3.clm.	US-PGPUB; USPAT	OR	ON	2014/08/25 07:08
S76	4	S64 and S74 and S75	US-PGPUB; USPAT	OR	ON	2014/08/25 07:08
S77	1	13/"Term Removed"	US-PGPUB; USPAT	OR	ON	2014/08/25 07:10
S78	1266	S58 S61	US-PGPUB; USPAT	OR	ON	2014/08/25 07:15
S79	652	S78 and S62	US-PGPUB; USPAT	OR	ON	2014/08/25 07:15
S80	134	S70 and S79	US-PGPUB; USPAT	OR	ON	2014/08/25 07:16
S81	5	S75 and S80	US-PGPUB; USPAT	OR	ON	2014/08/25 07:16
S82	11706	365/148,158,163,171,173.ccls.	US-PGPUB; USPAT	OR	ON	2014/08/25 07:17
S83	17	S79 and S82	US-PGPUB; USPAT	OR	ON	2014/08/25 07:17
S109	101	g11c2029/1806.cpc.	US-PGPUB; USPAT	OR	ON	2015/09/08 04:53
S110	1205	g11c2211/5641.cpc.	US-PGPUB; USPAT	OR	ON	2015/09/08 04:53
S111	1056	g11c29/76.cpc.	US-PGPUB; USPAT	OR	ON	2015/09/08 04:53
S112	377	g11c29/765.cpc.	US-PGPUB; USPAT	OR	ON	2015/09/08 04:54
S113	574	g11c29/50004.cpc.	US-PGPUB; USPAT	OR	ON	2015/09/08 04:54

EAST Search History

S114	2553	g06f11/1068,1072.cpc.	US-PGPUB; USPAT	OR	ON	2015/09/08 04:54
S115	2088	g11c11/5621.cpc.	US-PGPUB; USPAT	OR	ON	2015/09/08 04:54
S116	6751	S109 S110 S111 S112 S113 S114 S115	US-PGPUB; USPAT	OR	ON	2015/09/08 04:54
S117	247	flash adj translation adj layer.clm.	US-PGPUB; USPAT	OR	ON	2015/09/08 04:55
S118	337	(flash adj translation adj layer FTL!).clm.	US-PGPUB; USPAT	OR	ON	2015/09/08 04:55
S119	21	S116 and S118	US-PGPUB; USPAT	OR	ON	2015/09/08 04:55

3/7/2016 12:57:40 PM

C:\Users\rreidlinger\Documents\EAST\Workspaces\13455267.wsp



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BIB DATA SHEET

CONFIRMATION NO. 1038

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
14/950,553	11/24/2015	365	2824	GRTD-32800		
RULE						
APPLICANTS Greenthread, LLC, Dallas, TX; INVENTORS G.R. Mohan Rao, Allen, TX; ** CONTINUING DATA ***** This application is a CON of 14/525,411 10/28/2014 PAT 9196385 which is a DIV of 13/455,267 04/25/2012 PAT 8891298 which claims benefit of 61/509,257 07/19/2011 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** ** SMALL ENTITY ** 12/11/2015						
Foreign Priority claimed	☐ Yes ☒ No	☐ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	☐ Yes ☒ No		TX	5	1	1
Verified and	/R LANCE REIDLINGER/	Initials				
Acknowledged	Examiner's Signature					
ADDRESS						
HOWISON & ARNOTT, L.L.P. P.O. BOX 741715 DALLAS, TX 75374-1715 UNITED STATES						
TITLE						
LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM						
FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		
800						

To: patents@dalpat.com,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 25883

Mar 16, 2016 05:42:52 AM

Dear PAIR Customer:

HOWISON & ARNOTT, L.L.P
P.O. BOX 741715
DALLAS, TX 75374-1715
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 25883 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

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Application	Document	Mailroom Date	Attorney Docket No.
14950553	CTNF	03/16/2016	GRTD-32800
	892	03/16/2016	GRTD-32800

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PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: RAO, G.R. Mohan
Serial No.: 14/950,553
Confirmation No.: 1038
Filed: November 24, 2015
Group: 2824
Examiner: REIDLINGER, Ronald Lance
For: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

AMENDMENT AND RESPONSE TO OFFICE ACTION

This communication is responsive to the Examiner's Office Action dated March 16, 2016. Reconsideration is respectfully requested.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

5 at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module; ~~and~~

10

wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module; and

15

wherein the controller is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module.

20

2. (New) The system of Claim 1, wherein the MLC and SLC each comprise flash memories.

3. (New) The system of Claim 1 wherein the MLC comprises a flash memory and the SLC comprises a resistive RAM (RRAM).

4. (New) The system of Claim 1, wherein the MLC comprises a flash memory and SLC comprises a dynamic random access memory (DRAM).

5. (New) The system of Claim 1, wherein the MLC comprises a flash memory and the SLC comprises an SRAM.

6. (New) A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

5 at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;

15 wherein the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and

20 wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

wherein the controller is further adapted to maintain a count of those blocks that are accessed most frequently and, on a periodic basis, transfer the contents of those blocks into the SLC non-volatile memory module.

7. (New) The system of Claim 6, wherein the MLC and SLC each comprise flash memories.
8. (New) The system of Claim 6 wherein the MLC comprises a flash memory and the SLC comprises a resistive RAM (RRAM).
9. (New) The system of Claim 6, wherein the MLC comprises a flash memory and SLC comprises a dynamic random access memory (DRAM).
10. (New) The system of Claim 6, wherein the MLC comprises a flash memory and the SLC comprises an SRAM.

REMARKS

Applicant has carefully reviewed the Office Action dated March 16, 2016. Applicant has amended Claim 1 to more clearly point out the present inventive concept. Reconsideration and favorable action is respectfully requested.

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1 of both U.S. Patent Numbers 8,891,298 and 9,196,385. Applicant believes the amended claims overcome this rejection and, therefore, withdrawal of this rejection is respectfully requested.

Claim 1 stands rejected under 35 USC 102 (b) as being anticipated by *Gorobets et al.* This rejection is respectfully traversed with respect to the amended Claim 1 and the newly added claims.

Claim 1 has been amended to include the following language:

wherein the controller is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module

New independent Claim 6 is similar to the original Claim 1 with the additional language:

where in the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and

.....

wherein the controller is further adapted to maintain a count of those blocks that are accessed most frequently and, on a periodic basis, transfer the contents of those blocks into the SLC non-volatile memory module.

Gorobets does not disclose these features and, therefore, the amended Claim 1 and the newly added Claims 2 – 10 are believed to overcome this reference and, therefore, Applicant respect the request withdrawal the 35 USC section 102 (b) rejection with respect to Claim 1.

Applicant has now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicant respectfully requests full allowance of the claims as amended. Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 20-0780/GRTD-32800 of HOWISON & ARNOTT, L.L.P.

Respectfully submitted,
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September 16, 2016



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/950,553	11/24/2015	G.R. Mohan Rao	GRTD-32800	1038
25883 7590 12/29/2016 HOWISON & ARNOTT, L.L.P. P.O. BOX 741715 DALLAS, TX 75374-1715			EXAMINER REIDLINGER, RONALD LANCE	
			ART UNIT 2824	PAPER NUMBER
			NOTIFICATION DATE 12/29/2016	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@dalpat.com

Office Action Summary	Application No. 14/950,553	Applicant(s) RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 September 2016.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-10 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-10 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 2/15/2016 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 8/11/2016.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.
2. Claims 1-10 are pending.
3. Claims 1 and 6 are independent.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).
5. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a

result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

6. The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. ***An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission.*** For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-l.jsp.

7. **Claims 1-3 and 6-8 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 4-7 and 11 of U.S. Patent No. 9,196,385.** Although the claims at issue are not identical, they are not patentably distinct from each other because the differences would have been obvious to one of ordinary skill in the art at the time of the invention.

Regarding claim 1, claim 1 of the '385 patent anticipates the vast majority of the claim but uses a FTL instead of a controller and doesn't claim that the blocks that receive infrequent writes be segregated into the MLC nonvolatile memory module.

However the FTL is a type of controller and since the high write areas are being transferred to SLC, by process of elimination, the lower write areas are inherently going to be MLC.

Regarding claim 6, claims 1 and 11 of the '385 patent anticipate the vast majority of the claim but uses a FTL instead of a controller and doesn't claim the hot and cold designation and that the blocks that receive infrequent writes be allocated into the MLC nonvolatile memory module. However the FTL is a type of controller. Further, the claims require figuring out the most frequent write blocks, this is essentially designating those blocks as hot blocks and since the high write areas are being transferred to SLC, by process of elimination, the lower write areas are inherently going to be cold blocks and MLC.

8. **Claims 1-3 and 6-8 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1 and 4-6 and 11 of U.S. Patent No. 8,891,298.** Although the claims at issue are not identical, they are not patentably distinct from each other because the differences would have been obvious to one of ordinary skill in the art at the time of the invention.

The reasons presented for the double patenting rejection in view of the '298 are substantially similar to those presented for the rejection in view '385 patent.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. **Claims 4, 5, 9 and 10 rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description**

requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention.

Independent claims 1 and 6 both require “a SLC **non-volatile** memory module.” Claims 4 and 9 require that the SLC comprises a DRAM. Claims 5 and 10 require that the SLC comprises an SRAM. It is of note that DRAM and SRAM are almost universally volatile memories. Further, while there is support for having SRAM and DRAM as part of the overall system (see Spec. ¶ [0002]) there is no discussion of the SRAM or DRAM being part of the SLC non-volatile memory module or the SLC. The SLC is expressly limited to “flash, PCM, RRAM, MAGRAM or any other solid-state **non-volatile** memory...” (See *id.*, emphasis added.) SRAM is not mentioned elsewhere in the specification and DRAM is only mentioned in ¶¶ [0002, 0022, 0024 and 0026]. In ¶¶ [0022, 0024 and 0026], DRAM is presented as part of the controller and separate from the memory modules.

Claim Rejections - 35 USC § 103

11. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

12. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. **Claims 1, 2, 6 and 7 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. (US 2010/0172179 A1) in view of Duann (Silicon**

Motion Inc., Flash Memory Summit, SIC & MLC Hybrid, Santa Clara, CA, August 2008, No. 19 of Applicant's IDS submitted 11 August 2016).

Regarding claim 1, Gorobets et al. teach,

A system for storing data (e.g. Fig. 20) comprising:

at least one MLC non-volatile memory module (Fig. 20 Main Portion MLC No. 2003) comprising a plurality of individually erasable blocks (this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one SLC non-volatile memory module (Fig. 20 Binary Portion No. 2001) comprising a plurality of individually erasable blocks (again, this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]); and

a controller (Fig. 8 Memory Manager No. 300) coupled to the (Flash Memory No. 200) at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module (See Fig. 20), the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules (maps logical addresses to physical addresses, see ¶ [0096]), the address map comprising a list of logical address ranges (e.g. a block) accessible by a computer system (logical addresses), the list of logical address ranges having a minimum quanta of addresses (the minimum quantity of addresses is different depending on the operation, for an erase, a block is the minimum erase unit and a page is the minimum programming unit, see ¶ [0017]), wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or

within the at least one MLC non-volatile memory module (maps logical addresses to physical addresses, see ¶ [0096]); and

wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses (Fig. 20 block 2018) within the at least one MLC non-volatile memory module (Main Portion (MLC) No. 2003), fails a data integrity test (e.g. failure programming only the upper page, but still usable as binary, see ¶ [0165]), and, in the event of such a failure, the controller remaps (No. 2017) the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module (remapped to the spare binary block, see ¶ [0165]).

Gorobets et al. fail to teach,

the controller is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module.

Duann teaches, a hybrid MLC/SLC SSD where the controller is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently (pg. 11, first two bullets) and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module (second bullet) and those blocks that receive infrequent writes into the at least one MLC nonvolatile module (third bullet).

Duann teaches that this increases read/write & endurance closer to SLC levels while having the capacity and cost closer to MLC levels. See pg. 13 third bullet.

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the SLC/MLC device taught by Gorobets et al. to incorporate and take advantage of this portion of the wear leveling scheme taught by Duann for increased endurance.

Regarding claim 2, both Gorobets et al. (Fig. 5 or ¶ [0010]) and Duann (pg. 3 SLC and MLC NAND) teach the MLC and SLC each comprise flash memories.

Regarding claim 6, Gorobets et al. teach,

A system for storing data (e.g. Fig. 20) comprising:

at least one MLC non-volatile memory module (Fig. 20 Main Portion MLC No. 2003) comprising a plurality of individually erasable blocks (this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one SLC non-volatile memory module (Fig. 20 Binary Portion No. 2001) comprising a plurality of individually erasable blocks (again, this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]); and

a controller (Fig. 8 Memory Manager No. 300) coupled to the (Flash Memory No. 200) at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module (See Fig. 20), the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules (maps logical addresses to physical addresses, see ¶ [0096]), the address map comprising a list of logical address ranges (e.g. a block) accessible by a computer system (logical addresses), the list of

logical address ranges having a minimum quanta of addresses (the minimum quantity of addresses is different depending on the operation, for an erase, a block is the minimum erase unit and a page is the minimum programming unit, see ¶ [0017]), wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module (maps logical addresses to physical addresses, see ¶ [0096]); and

wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses (Fig. 20 block 2018) within the at least one MLC non-volatile memory module (Main Portion (MLC) No. 2003), fails a data integrity test (e.g. failure programming only the upper page, but still usable as binary, see ¶ [0165]), and, in the event of such a failure, the controller remaps (No. 2017) the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module (remapped to the spare binary block, see ¶ [0165]).

Gorobets et al. fail to teach,

the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and

the controller is further adapted to maintain a count of those blocks that are accessed most frequently and, on a periodic basis, transfer the contents of those blocks into the SLC non-volatile memory module.

Duann teaches,

the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks (pg. 11 bullet two) and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks (bullet three); and

the controller is further adapted to maintain a count of those blocks that are accessed most frequently (see pg. 11 Logical block write count table) and, on a periodic basis, transfer the contents of those blocks into the SLC non-volatile memory module (pg.11 bullet two, "Move 'hot (physical) blocks'...into SLC area").

Duann teaches that this increases read/write & endurance closer to SLC levels while having the capacity and cost closer to MLC levels. See pg. 13 third bullet.

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the SLC/MLC device taught by Gorobets et al. to incorporate and take advantage of this portion of the wear leveling scheme taught by Duann for increased endurance.

Regarding claim 7, both Gorobets et al. (Fig. 5 or ¶ [0010]) and Duann (pg., 3 SLC and MLC NAND) teach the MLC and SLC each comprise flash memories.

15. Claims 3 and 8 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al and Duann as applied to claims 1, 2, 6 and 7 above, and further in view of Kund et al. (US 2010/0058018 A1).

Regarding claims 3 and 8, Gorobets et al. and Duann et al. teach that both the MLC and SLC are flash (see Fig. 5 and pg. 3 respectively).

Kund et al. teach generally that “Emerging memory technologies such as resistive memory (e.g., resistive random access memories such as phase change random access memory (PCRAM), conductive bridge random access memory (CBRAM), and magnetic random access memory (MRAM)) offer certain advantages over DRAM, Flash and other conventional types of memory devices in terms of switching speeds, size, power consumption, and non-volatility.” Kund et al. teach that these memories are typically binary or SLC. See ¶ [0022].

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the SLC flash EEPROM taught by Gorobels et al. with the PCM or other resistive memory like CBRAM or MRAM taught by Kund et al. in view of the advantages over flash EEPROM.

Response to Arguments

16. Applicant's arguments with respect the rejection under nonstatutory double patenting filed 16 September 2016 have been fully considered but they are not persuasive. See the rejection above.

17. Applicant's arguments, see Remarks pp. 5-6, filed 16 September 2016, with respect to the rejection under pre-AIA 35 USC § 102(b) have been fully considered and are persuasive. The rejection of claim 1 under this statute has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made under 35 USC § 103(a) as presented above.

Pertinent Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Schuetz et al. (US 2010/0325352 A1) teach it's typical to use SRAM or DRAM as volatile cache in a flash system. See ¶ [0005]. Schuetz et al. further teach having SRAM or DRAM in a PCRAM Flash hybrid memory. See Fig. 1.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R LANCE REIDLINGER whose telephone number is (571)270-7353. The examiner can normally be reached on 11:30am - 9:00pm Mon-Thur and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571)272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/R LANCE REIDLINGER/
Examiner, Art Unit 2824

Notice of References Cited	Application/Control No. 14/950,553		Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER		Art Unit 2824	Page 1 of 1

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	Filing Date	2015-11-24
	First Named Inventor	RAO, G. R. Mohan
	Art Unit	2824
	Examiner Name	REIDLINGER, RONALD LANCE
	Attorney Docket Number	GRTD-32800

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Gregory M. Howison, Reg. #30646/	Date (YYYY-MM-DD)	2016-08-11
Name/Print	Gregory M. Howison	Registration Number	30,646

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	488	SLC with (resist\$3 RRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/23 19:06
L2	7880	MLC with flash	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/23 19:07
L3	330	1 and 2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/23 19:07
L4	323	1 with 2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/23 19:07
L8	1	("20100058018").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/12/23 19:14
L9	16	("20090268513" "20090307418" "20100058018" "20100172179" "20110060870" "20110271043" "7855916").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/23 19:59
L10	102	DRAM with SRAM with cache with SSD	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/23 20:03
S131	2	((("8891298") or ("9196385"))).PN.	USPAT; USOCR	OR	OFF	2016/12/22 19:56
S132	627	(DRAM SRAM) with Cache with SSD	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/23 14:37
S133	16169	frequent\$2 near2 (writ\$3 program\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/23 14:38
S134	0	S132 same S133	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/23 14:39

EAST Search History

S135	3463	(DRAM SRAM) with Cache and SSD	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/23 14:39
S136	146	S133 and S135	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/23 14:39

EAST Search History (Interference)

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12/ 23/ 2016 8:16:48 PM

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Search Notes 	Application/Control No. 14950553	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner R LANCE REIDLINGER	Art Unit 2824

CPC- SEARCHED		
Symbol	Date	Examiner
G11C 11/5621, 2211/5641, 2029/1806, 29/50004, 29/76, 29/765	3/7/2016	RLR
G06F 11/1068, 11/1072	3/7/2016	RLR

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Reviewed Parent Applications' Search/Prosecution History	3/7/2016	RLR
Inventor Search Conducted in EASt	3/7/2016	RLR
See Attached EAST Search History	3/7/2016	RLR
See Attached EAST Search History	12/23/2016	RLR

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/R LANCE REIDLINGER/ Examiner.Art Unit 2824	
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To: patents@dalpat.com,,
From: PAIR_eOfficeAction@uspto.gov
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Subject: Private PAIR Correspondence Notification for Customer Number 25883

Dec 29, 2016 03:45:14 AM

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Application	Document	Mailroom Date	Attorney Docket No.
14950553	CTFR	12/29/2016	GRTD-32800
	892	12/29/2016	GRTD-32800
	1449	12/29/2016	GRTD-32800

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UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: RAO, G.R. Mohan
Serial No.: 14/950,553
Confirmation No.: 1038
Filed: November 24, 2015
Group: 2824
Examiner: REIDLINGER, Ronald Lance
For: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

AMENDMENT AFTER FINAL

This communication is responsive to the Examiner's Office Action dated December 29, 2016. Applicant is submitting herewith a Request for Continued Examination. Applicant requests that any previously non-entered Amendments not be entered. Reconsideration is respectfully requested.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

5 at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;

15 wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module; and

20 wherein the controller is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module, and on a periodic basis, transfer the contents of the blocks in the MLC non-volatile memory module determined to received frequent writes to the SLC non-volatile memory module and which determined blocks in the SLC are determined in accordance with the next equivalent range of physical addresses determined by the controller.

2. (Previously Presented) The system of Claim 1, wherein the MLC and SLC each comprise flash memories.

3. (Previously Presented) The system of Claim 1 wherein the MLC comprises a flash memory and the SLC comprises a resistive RAM (RRAM).

4. (Currently Amended) The system of Claim 1, wherein the MLC comprises a flash memory and SLC comprises ~~a dynamic random access memory (DRAM)~~ a phase change memory (PCM).

5. (Currently Amended) The system of Claim 1, wherein the MLC comprises a flash memory and the SLC comprises ~~an SRAM~~ a magnetic random-access memory (MAGRAM).

6. (Currently Amended) A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

5 at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;

15 wherein the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and

wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the

20 controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

wherein the controller is further adapted to maintain a count of those blocks that are accessed most frequently and, on a periodic basis, transfer the contents of those blocks into the SLC non-volatile memory module, wherein the blocks transferred to are determined in accordance with the next equivalent range of physical addresses determined by the controller.
25

7. (Previously Presented) The system of Claim 6, wherein the MLC and SLC each comprise flash memories.

8. (Previously Presented) The system of Claim 6 wherein the MLC comprises a flash memory and the SLC comprises a resistive RAM (RRAM).

9. (Currently Amended) The system of Claim 6, wherein the MLC comprises a flash memory and SLC comprises ~~a dynamic random access memory (DRAM)~~ a phase change memory (PCM).

10. (Currently Amended) The system of Claim 6, wherein the MLC comprises a flash memory and the SLC comprises ~~an SRAM~~ a magnetic random-access memory (MAGRAM).

REMARKS

Applicant has carefully reviewed the Office Action dated December 29, 2016. Applicant has amended Claims 1, 4-6, 9, and 10 to more clearly point out the present inventive concept. Reconsideration and favorable action is respectfully requested.

Double Patenting Rejection

Claims 1-3 and 6-8 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 4-7, and 11 of U.S. Patent No. 9,196,385. A Terminal Disclaimer is submitted concurrently with this response with respect to U.S. Patent No. 9,196,385.

Claims 1-3 and 6-8 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 and 4-6 of U.S. Patent No. 8,891,298. A Terminal Disclaimer is submitted concurrently with this response with respect to U.S. Patent No. 8,891,298.

Rejections Under 35 U.S.C. § 112

Claims 4, 5, 9, and 10 stand rejected under 35 U.S.C. § 112(a) or 35 U.S.C. § 112 (pre-AIA), first paragraph. In response, Applicant has amended claims 4 and 9 to recite that the SLC comprises a phase change memory (PCM) and claims 5 and 10 to recite that the SLC comprises a magnetic random-access memory (MAGRAM). As noted in the Office Action, these limitations are supported at least at paragraph [0002] of the Specification. Therefore, Applicant respectfully requests withdrawal of the § 112 rejections with respect to Claims 4, 5, 9, and 10.

Rejections Under 35 U.S.C. § 103

Claims 1, 2, 6, and 7

Claims 1, 2, 6, and 7 stand rejected under 35 U.S.C. § 103 as being unpatentable over US 2010/0172179 to Gorobets et al. (“*Gorobets*”) in view of No. 19 of Applicant’s IDS submitted 11 August 2016: Silicon Motion Inc., Flash Memory Summit, SIC & MIC Hybrid, Santa Clara, CA, August 2008 (“*Duann*”). Applicant respectfully traverses.

As discussed in the previous Amendment and Response to Office Action filed September 16, 2016, *Gorobets* does not disclose the limitation of Claim 1 that states:

wherein the controller is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module

nor the limitations of Claim 6 which state:

where in the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and

wherein the controller is further adapted to maintain a count of those blocks that are accessed most frequently and, on a periodic basis, transfer the contents of those blocks into the SLC non-volatile memory module.

Additionally, in the present Response, Claims 1 and 6 have been amended to include the following language:

wherein the blocks transferred to are determined in accordance with the next equivalent range of physical addresses determined by the controller.

Applicant respectfully submits that such is not taught by *Gorobets* or *Duann*, taken alone or in combination, and thus Claims 1 and 6 are allowable over *Gorobets* and *Duann*. Claim 2 depends

from Claim 1 and Claim 7 depends from Claim 6. Thus, Applicant respectfully submits that Claims 2 and 7 are similarly allowable over *Gorobets* and *Duann*. Therefore, Applicant respectfully requests withdrawal of the § 103 rejection with respect to Claims 1, 2, 6, and 7.

Claims 3 and 8

Claims 3 and 8 stand rejected under 35 U.S.C. § 103 as being unpatentable over *Gorobets* and *Duann* in view of US 2010/0058018 to Kund et al. (“*Kund*”).

Claim 3 depends from Claim 1 and Claim 8 depends from Claim 6. As described above with respect to Claims 1 and 6, the *Gorobets* and *Duann* do not teach or suggest all the limitations of Claims 1 and 6. Since *Kund* does not cure the deficiencies of *Gorobets* and *Duann*, Applicant respectfully submits that Claims 3 and 8 are also allowable. Therefore, Applicant respectfully requests withdrawal of the § 103 rejection with respect to Claims 3 and 8.

Applicant has now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicant respectfully requests full allowance of the claims as amended. Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 20-0780/GRTD-32800 of HOWISON & ARNOTT, L.L.P.

Respectfully submitted,
HOWISON & ARNOTT, L.L.P.
Attorneys for Applicant

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June 29, 2017

AMENDMENT AND RESPONSE
SN: 14/950,553
Atty. Dkt. No. GRTD-32800

Page 7 of 7



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/950,553	11/24/2015	G.R. Mohan Rao	GRTD-32800	1038
25883 7590 07/21/2017 HOWISON & ARNOTT, L.L.P. P.O. BOX 741715 DALLAS, TX 75374-1715			EXAMINER REIDLINGER, RONALD LANCE	
			ART UNIT 2824	PAPER NUMBER
			NOTIFICATION DATE 07/21/2017	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@dalpat.com

Office Action Summary	Application No. 14/950,553	Applicant(s) RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 June 2017.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-10 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-10 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 15 February 2016 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.
2. Claims 1-10 are pending.
3. Claims 1 and 6 are independent.

Claim Rejections - 35 USC § 103

4. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.
5. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:
 1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. **Claims 1, 2, 6 and 7 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. (US 2010/0172179 A1) in view of Duann (Silicon Motion Inc., Flash Memory Summit, SIC & MIC Hybrid, Santa Clara, CA, August 2008).**

Regarding claim 1, Gorobets et al. teach,

A system for storing data (e.g. Fig. 20) comprising:

at least one MLC non-volatile memory module (Fig. 20 Main Portion MLC No. 2003) comprising a plurality of individually erasable blocks (this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one SLC non-volatile memory module (Fig. 20 Binary Portion No. 2001) comprising a plurality of individually erasable blocks (again, this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]); and

a controller (Fig. 8 Memory Manager No. 300) coupled to the (Flash Memory No. 200) at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module (See Fig. 20), the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules (maps logical addresses to physical addresses, see ¶ [0096]), the address map comprising a list of logical address ranges (e.g. a block) accessible by a computer system (logical addresses), the list of logical address ranges having a minimum quanta of addresses (the minimum quantity of addresses is different depending on the operation, for an erase, a block is the

minimum erase unit and a page is the minimum programming unit, see ¶ [0017]), wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module (maps logical addresses to physical addresses, see ¶ [0096]); and

wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses (Fig. 20 block 2018) within the at least one MLC non-volatile memory module (Main Portion (MLC) No. 2003), fails a data integrity test (e.g. failure programming only the upper page, but still usable as binary, see ¶ [0165]), and, in the event of such a failure, the controller remaps (No. 2017) the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module (remapped to the spare binary block, see ¶ [0165]).

Gorobets et al. fail to teach,

the controller is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module, and on a periodic basis, transfer the contents of the blocks in the MLC non-volatile memory module determined to received frequent writes to the SLC non-volatile memory module

and which determined blocks in the SLC are determined in accordance with the next equivalent range of physical addresses determined by the controller.

Duann teaches, a hybrid MLC/SLC SSD where the controller is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently (pg. 11, first two bullets) and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module (second bullet) and those blocks that receive infrequent writes into the at least one MLC nonvolatile module (third bullet), and on a periodic basis, transfer the contents of the blocks in the MLC non-volatile memory module determined to received frequent writes to the SLC non-volatile memory module (pg.11 bullet two, "Move 'hot (physical) blocks'...into SLC area" and pg. 13, bullet 3) and which determined blocks in the SLC are determined in accordance with the next equivalent range of physical addresses determined by the controller (See pg. 12 controller maps logical blocks to physical blocks in the SLC).

Duann teaches that this increases read/write & endurance closer to SLC levels while having the capacity and cost closer to MLC levels. See pg. 13 third bullet.

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the SLC/MLC device taught by Gorobets et al. to incorporate and take advantage of this portion of the wear leveling scheme taught by Duann for increased endurance.

Regarding claim 2, both Gorobets et al. (Fig. 5 or ¶ [0010]) and Duann (pg. 3 SLC and MLC NAND) teach the MLC and SLC each comprise flash memories.

Regarding claim 6, Gorobets et al. teach,

A system for storing data (e.g. Fig. 20) comprising:

at least one MLC non-volatile memory module (Fig. 20 Main Portion MLC No. 2003) comprising a plurality of individually erasable blocks (this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one SLC non-volatile memory module (Fig. 20 Binary Portion No. 2001) comprising a plurality of individually erasable blocks (again, this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]); and

a controller (Fig. 8 Memory Manager No. 300) coupled to the (Flash Memory No. 200) at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module (See Fig. 20), the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules (maps logical addresses to physical addresses, see ¶ [0096]), the address map comprising a list of logical address ranges (e.g. a block) accessible by a computer system (logical addresses), the list of logical address ranges having a minimum quanta of addresses (the minimum quantity of addresses is different depending on the operation, for an erase, a block is the minimum erase unit and a page is the minimum programming unit, see ¶ [0017]), wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module (maps logical addresses to physical addresses, see ¶ [0096]); and

wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses (Fig. 20 block 2018) within the at least one MLC non-volatile memory module (Main Portion (MLC) No. 2003), fails a data integrity test (e.g. failure programming only the upper page, but still usable as binary, see ¶ [0165]), and, in the event of such a failure, the controller remaps (No. 2017) the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module (remapped to the spare binary block, see ¶ [0165]).

Gorobets et al. fail to teach,

the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and

the controller is further adapted to maintain a count of those blocks that are accessed most frequently and, on a periodic basis, transfer the contents of those blocks into the SLC non-volatile memory module, wherein the blocks transferred to are determined in accordance with the next equivalent range of physical addresses determined by the controller.

Duann teaches,

the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks (pg. 11 bullet two) and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks (bullet three); and

the controller is further adapted to maintain a count of those blocks that are accessed most frequently (see pg. 11 Logical block write count table) and, on a periodic basis, transfer the contents of those blocks into the SLC non-volatile memory module (pg.11 bullet two, "Move 'hot (physical) blocks'...into SLC area") wherein the blocks transferred to are determined in accordance with the next equivalent range of physical addresses determined by the controller (see pg. 12, controller maps logical blocks to physical blocks in the SLC).

Duann teaches that this increases read/write & endurance closer to SLC levels while having the capacity and cost closer to MLC levels. See pg. 13 third bullet.

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the SLC/MLC device taught by Gorobets et al. to incorporate and take advantage of this portion of the wear leveling scheme taught by Duann for increased endurance.

Regarding claim 7, both Gorobets et al. (Fig. 5 or ¶ [0010]) and Duann (pg., 3 SLC and MLC NAND) teach the MLC and SLC each comprise flash memories.

8. Claims 3-5 and 8-10 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al and Duann as applied to claims 1, 2, 6 and 7 above, and further in view of Kund et al. (US 2010/0058018 A1).

Regarding claims 3-5 and 8-10, Gorobets et al. and Duann et al. teach that both the MLC and SLC are flash (see Fig. 5 and pg. 3 respectively).

Kund et al. teach generally that "Emerging memory technologies such as resistive memory (e.g., resistive random access memories such as phase change

random access memory (PCRAM), conductive bridge random access memory (CBRAM), and magnetic random access memory (MRAM)) offer certain advantages over DRAM, Flash and other conventional types of memory devices in terms of switching speeds, size, power consumption, and non-volatility.” Kund et al. teach that these memories are typically binary or SLC. See ¶ [0022].

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the SLC flash EEPROM taught by Gorobets et al. with the PCM or other resistive memory like CBRAM or MRAM taught by Kund et al. in view of the advantages over flash EEPROM.

Response to Arguments

9. The double patenting rejections have been withdrawn as appropriate terminal disclaimers have been filed.

10. The rejections under 35 USC §112(a) have been withdrawn due to the amendments to claims 4, 5, 9 and 10.

11. Applicant has argued that Gorobets et al. fail to teach portions of the claims. As is shown in the rejections above Duann teaches these portions and they would have been obvious to one of ordinary skill in the art prior to the effective filing date.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R LANCE REIDLINGER whose telephone number is (571)270-7353. The examiner can normally be reached on 11:30am - 9:00pm Mon-Thur and alternate Fridays.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571)272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R LANCE REIDLINGER/
Examiner, Art Unit 2824

Search Notes 	Application/Control No. 14950553	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner R LANCE REIDLINGER	Art Unit 2824

CPC- SEARCHED		
Symbol	Date	Examiner
G11C 11/5621, 2211/5641, 2029/1806, 29/50004, 29/76, 29/765	3/7/2016	RLR
G06F 11/1068, 11/1072	3/7/2016	RLR

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
Reviewed Parent Applications' Search/Prosecution History	3/7/2016	RLR
Inventor Search Conducted in EAST	3/7/2016	RLR
See Attached EAST Search History	3/7/2016	RLR
See Attached EAST Search History	12/23/2016	RLR

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/R LANCE REIDLINGER/ Examiner.Art Unit 2824	
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To: patents@dalpat.com,,
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Application	Document	Mailroom Date	Attorney Docket No.
14950553	CTNF	07/21/2017	GRTD-32800

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PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: RAO, G.R. Mohan
Serial No.: 14/950,553
Confirmation No.: 1038
Filed: November 24, 2015
Group: 2824
Examiner: REIDLINGER, Ronald Lance
For: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

AMENDMENT AND RESPONSE TO OFFICE ACTION

This communication is responsive to the Examiner's Office Action dated July 21, 2017.
Reconsideration is respectfully requested.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

5 at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;

15 wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module; and

20 wherein the controller is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module, and maintain a count value of the blocks in the MLC non-volatile memory module determined to have received frequent writes and that are accessed most frequently on a periodic basis when the count value is a predetermined count value, transfer the contents of the counted blocks in the MLC non-volatile memory module determined to have received frequent writes after reaching the predetermined count value to the SLC non-volatile memory

30 module and which determined blocks in the SLC are determined in accordance with the next equivalent range of physical addresses determined by the controller.

2. (Previously Presented) The system of Claim 1, wherein the MLC and SLC each comprise flash memories.

3. (Previously Presented) The system of Claim 1 wherein the MLC comprises a flash memory and the SLC comprises a resistive RAM (RRAM).

4. (Previously Presented) The system of Claim 1, wherein the MLC comprises a flash memory and SLC comprises a phase change memory (PCM).

5. (Previously Presented) The system of Claim 1, wherein the MLC comprises a flash memory and the SLC comprises a magnetic random-access memory (MAGRAM).

6. (Currently Amended) A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

5 at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;

10

wherein the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and

15

20 wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

25 wherein the controller is further adapted to maintain a count value of those blocks that are accessed most frequently and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller.

7. (Previously Presented) The system of Claim 6, wherein the MLC and SLC each comprise flash memories.

8. (Previously Presented) The system of Claim 6 wherein the MLC comprises a flash memory and the SLC comprises a resistive RAM (RRAM).

9. (Previously Presented) The system of Claim 6, wherein the MLC comprises a flash memory and SLC comprises a phase change memory (PCM).

10. (Previously Presented) The system of Claim 6, wherein the MLC comprises a flash memory and the SLC comprises a magnetic random-access memory (MAGRAM).

REMARKS

Applicant has carefully reviewed the Office Action dated July 21, 2017. Applicant has amended Claims 1 and 6 to more clearly point out the present inventive concept. Reconsideration and favorable action is respectfully requested.

Rejections Under 35 U.S.C. § 103

Claims 1, 2, 6, and 7

Claims 1, 2, 6, and 7 stand rejected under 35 U.S.C. § 103 as being unpatentable over US 2010/0172179 to Gorobets et al. (“*Gorobets*”) in view of No. 19 of Applicant’s IDS submitted 11 August 2016: Silicon Motion Inc., Flash Memory Summit, SIC & MIC Hybrid, Santa Clara, CA, August 2008 (“*Duann*”). Applicant respectfully traverses this rejection in view of the claims as currently presented.

As discussed in the previous Amendment and Response to Office Action filed September 16, 2016, *Gorobets* does not disclose the limitation of Claim 1 that states:

wherein the controller is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module

nor the limitations of Claim 6 which state:

where in the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and

wherein the controller is further adapted to maintain a count of those blocks that are accessed most frequently and, on a periodic basis, transfer the contents of those blocks into the SLC non-volatile memory module.

Additionally, in the present Response, Claims 1 and 6 have been amended to include the following language:

Claim 1:

and maintain a count value of the blocks in the MLC non-volatile memory module determined to have received frequent writes and that are accessed most frequently on a periodic basis when the count value a predetermined count value, transfer the contents of the counted blocks in the MLC non-volatile memory module determined to have received frequent writes after reaching the predetermined count value to the SLC non-volatile memory module

Claim 6:

on a periodic basis when the count value a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller.

Applicant respectfully submits that such is not taught by *Gorobets* or *Duamm*, taken alone or in combination, and thus Claims 1 and 6 are allowable over *Gorobets* and *Duamm*. Claim 2 depends from Claim 1 and Claim 7 depends from Claim 6. Thus, Applicant respectfully submits that Claims 2 and 7 are similarly allowable over *Gorobets* and *Duamm*. Therefore, Applicant respectfully requests withdrawal of the § 103 rejection with respect to Claims 1, 2, 6, and 7.

Claims 3 and 8

Claims 3-5 and 8-10 stand rejected under 35 U.S.C. § 103 as being unpatentable over *Gorobets* and *Duamm* in view of US 2010/0058018 to Kund et al. ("*Kund*").

Claims 3-5 depend from Claim 1 and Claims 8-10 depends from Claim 6. As described above with respect to Claims 1 and 6, the *Gorobets* and *Duann* do not teach or suggest all the limitations of Claims 1 and 6. Since *Kund* does not cure the deficiencies of *Gorobets* and *Duann*, Applicant respectfully submits that Claims 3-5 and 8-10 are also allowable. Therefore, Applicant respectfully requests withdrawal of the § 103 rejection with respect to Claims 3-5 and 8-10.

Applicant has now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicant respectfully requests full allowance of the claims as amended. Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 20-0780/GRTD-32800.

Respectfully submitted,
MUNCK WILSON MANDALA, LLP
Attorneys for Applicant

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January 22, 2018



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NOTICE OF ALLOWANCE AND FEE(S) DUE

25883 7590 04/16/2018
MUNCK WILSON MANDALA L.L.P.
P.O. Drawer 800889
DALLAS, TX 75380

EXAMINER

REIDLINGER, RONALD LANCE

ART UNIT PAPER NUMBER

2824

DATE MAILED: 04/16/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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14/950,553

11/24/2015

G.R. Mohan Rao

GRTD-32800

1038

TITLE OF INVENTION: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$500	\$0	\$0	\$500	07/16/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

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If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

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III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

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(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/950,553	11/24/2015	G.R. Mohan Rao	GRTD-32800	1038

TITLE OF INVENTION: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$500	\$0	\$0	\$500	07/16/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
REIDLINGER, RONALD LANCE	2824	365-185030

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/950,553	11/24/2015	G.R. Mohan Rao	GRTD-32800	1038

25883 7590 04/16/2018
MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

EXAMINER

REIDLINGER, RONALD LANCE

ART UNIT	PAPER NUMBER
----------	--------------

2824

DATE MAILED: 04/16/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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The information provided by you in this form will be subject to the following routine uses:

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/950,553	Applicant(s) RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 22 January 2018.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-10. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/HARRY W BYRNE/ Primary Examiner, Art Unit 2824	/R. L. R./ Examiner, Art Unit 2824
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DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.
2. Claims 1-10 are pending.
3. Claims 1 and 6 are independent.

Allowable Subject Matter

4. Claims 1-10 are allowed.
5. The following is an examiner's statement of reasons for allowance:

Regarding claims 1-5, the prior art of record fails to teach the combination of,

A system for storing data comprising:

at least one MLC non-volatile memory module;

at least one SLC non-volatile memory module

in the event of a failure of the entry in one MLC non-volatile memory module, the controller remaps to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module; and

the controller maintains a count value of the blocks in the MLC non-volatile memory module determined to have received frequent writes and that are accessed most frequently, when the count value is a predetermined count value, transfer the contents of the counted blocks in the MLC non-volatile memory module determined to

have received frequent writes after reaching the predetermined count value to the SLC non-volatile memory module.

Regarding claims 6-10, the prior art of record fails to teach the combination of,

A system for storing data comprising:

at least one MLC non-volatile memory module;

at least one SLC non-volatile memory module;

wherein the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks;

in the event of a failure of the entry in one MLC non-volatile memory module, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

the controller is further adapted to maintain a count value of those blocks that are accessed most frequently and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Pertinent Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Moshayed (US 2009/0327591 A1 US 8,825,941 B2) teaches moving data from the blocks of MLC flash to SLC flash upon reaching an erase count threshold. See e.g. ¶ [0032].

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R LANCE REIDLINGER whose telephone number is (571)270-7353. The examiner can normally be reached on 11:30am - 9:00pm Mon-Thur and alternate Fridays.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571)272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R. L. R./
Examiner, Art Unit 2824

/HARRY W BYRNE/
Primary Examiner, Art Unit 2824

Notice of References Cited	Application/Control No. 14/950,553		Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER		Art Unit 2824	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2009/0327591 A1	12-2009	Moshayedi; Mark	G06F11/1441	711/103
*	B	US-8,825,941 B2	09-2014	Moshayedi; Mark	G06F11/1441	711/103
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S145	46896	count near5 (writ\$3 program\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/03/29 14:20
S146	4928	S145 with block	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/03/29 14:24
S147	69	S146 same mov\$3 adj2 data	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/03/29 14:24

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	24241	(G11C11/5635 or G11C16/16 or G06F11/1068 or G11C29/76 or G11C29/52 or G06F11/1072 or G11C11/5678 or G11C11/5621 or G06F12/0246 or G11C16/3495 or G11C2211/5641 or G06F2212/7202).cpc.	US- PGPUB; USPAT	OR	OFF	2018/03/30 23:20
L2	36441	data near3 test\$3.clm.	US- PGPUB; USPAT	OR	OFF	2018/03/30 23:20
L3	1810	MLC.clm.	US- PGPUB; USPAT	OR	OFF	2018/03/30 23:20
L4	1141	SLC.clm.	US- PGPUB; USPAT	OR	OFF	2018/03/30 23:21
L5	366085	count\$3.clm.	US- PGPUB; USPAT	OR	OFF	2018/03/30 23:21
L6	5	2 3 4 5	US- PGPUB; USPAT	AND	OFF	2018/03/30 23:21
L7	5	1 6	US- PGPUB; USPAT	AND	OFF	2018/03/30 23:21

3/ 30/ 2018 11:23:24 PM**C:\ Users\ rreidlinger\ Documents\ EAST\ Workspaces\ 13455267.wsp**

Issue Classification 	Application/Control No. 14950553	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	

CPC						
Symbol					Type	Version
G11C		11		5635	F	2013-01-01
G11C		16		3495	I	2013-01-01
G06F		12		0246	I	2013-01-01
G06F		2212		7202	A	2013-01-01
G06F		11		1068	I	2013-01-01
G06F		11		1072	I	2013-01-01
G11C		11		5621	I	2013-01-01
G11C		11		5678	I	2013-01-01
G11C		29		52	I	2013-01-01
G11C		29		76	I	2013-01-01
G11C		2211		5641	A	2013-01-01
G11C		16		16	I	2013-01-01

CPC Combination Sets						
Symbol			Type	Set	Ranking	Version

/R LANCE REIDLINGER/ Examiner.Art Unit 2824 (Assistant Examiner)	03/30/2018 (Date)	Total Claims Allowed: 10	
/HARRY W BYRNE/ Primary Examiner.Art Unit 2824 (Primary Examiner)	04/01/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 4

Issue Classification 	Application/Control No. 14950553	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner R LANCE REIDLINGER	Art Unit 2824

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED								
						G	1	1	C	16 / 04 (2006.01.01)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		

/R LANCE REIDLINGER/ Examiner.Art Unit 2824 (Assistant Examiner)	03/30/2018 (Date)	Total Claims Allowed: 10	
/HARRY W BYRNE/ Primary Examiner.Art Unit 2824 (Primary Examiner)	04/01/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 4

Search Notes 	Application/Control No. 14950553	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner R LANCE REIDLINGER	Art Unit 2824

CPC- SEARCHED		
Symbol	Date	Examiner
G11C 11/5621, 2211/5641, 2029/1806, 29/50004, 29/76, 29/765	3/7/2016	RLR
G06F 11/1068, 11/1072	3/7/2016	RLR

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
Reviewed Parent Applications' Search/Prosecution History	3/7/2016	RLR
Inventor Search Conducted in EAST	3/7/2016	RLR
See Attached EAST Search History	3/7/2016	RLR
See Attached EAST Search History	12/23/2016	RLR

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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Bibliographic Data

Application No: 14950553

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged:

Examiner's Signature

Initials

Title:

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/24/2015	365	2824	GRTD-32800
RULE			

APPLICANTS

Greenthread, LLC, Dallas, TX,

INVENTORS

G.R. Mohan Rao, Allen, TX, UNITED STATES

CONTINUING DATA

This application is a CON of 14525411 10/28/2014 PAT 9196385

14525411 is a DIV of 13455267 04/25/2012 PAT 8891298

13455267 has PRO of 61509257 07/19/2011

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

12/11/2015

STATE OR COUNTRY

UNITED STATES

ADDRESS

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P.O. Drawer 800889

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Application	Document	Mailroom Date	Attorney Docket No.
14950553	NOA	04/16/2018	GRTD-32800
	892	04/16/2018	GRTD-32800

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